

Features

- XuanTie C906 RISC-V CPU
- HiFi4 DSP
- Memories
 - DDR2/DDR3 SDRAM
 - SD3.0/SDIO3.0/eMMC5.0
- Video Engine
 - H.265/H.264/MPEG-1/2/4/JPEG/VC1/Xvid/Sorenson Spark decoding, up to 4K
 - JPEG/MJPEG encoding, up to 1080p@60fps
- Video and Graphics
 - Allwinner SmartColor2.0 post processing for an excellent display experience
 - Supports de-interlacer (DI) up to 1080p@60fps
 - Supports Graphic 2D (G2D) hardware accelerator including rotate, mixer, LBC decompression functions
- Video Output
 - RGB interface up to 1920 x 1080@60fps
 - Dual link (VDS interface up to 1920 x 1080@60fps
 - 4-lane MIPI DSI up to 1920 x 1200@60fps
 - HDMI TX interface up to 4K@30fps
 - CVBS OUT interface, supporting NTSC and PAL format
- - 8-bit parallel CSI interface
 - CVBS IN interface, supporting NTSC and PAL format
- Analog Audio Codec
 - 2 DACs and 3 ADCs
 - Analog audio interfaces: LINEOUTLP/N, LINEOUTRP/N, HPOUTL/R, MICIN1P/1N, MICIN1P/2N, MICIN3P/3N, LINEINL/R, FMINL/R
- Three I2S/PCM external interfaces (I2S0, I2S1, I2S2)
- Maximum 8 digital PDM microphones (DMIC)
- OWA TX and OWA RX, compliance with S/PDIF interface
- Security System
 - AES, DES, 3DES, RSA, MD5, SHA, HMAC
 - Integrated 2 Kbits OTP storage space
- **External Peripherals**
 - USB 2.0 DRD (USB0) and USB 2.0 HOST (USB1)
 - 10/100/1000 Mbps Ethernet port with RGMII and RMII interfaces
 - Up to 6 UART controllers (UARTO, UART1, UART2, UART3, UART4, UART5)
 - Up to 2 SPI controllers (SPIO, SPI1)
 - Up to 4 TWI controllers (TWI0, TWI1, TWI2, TWI3)
 - CIR RX and CIR TX
 - 8 independent PWM channels (PWM0 to PWM7)
 - 2-ch GPADC
 - 4-ch TPADC
 - 1-ch LRADC
 - **LEDC**
- **Package**
 - LFBGA 337 balls, 13 mm x 13 mm





Revision	Date	Author	Description
1.0	January 18, 2022	KPA0570	Initial release version.





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About This Documentation



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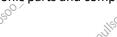
Purpose

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package, and part reliability of the D1-H processor. For details about register descriptions of each module, see the *D1-H_User_Manual*.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components





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Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
MARNING	Indicates potential risk of injury or death exists if the instructions are not obeyed.
A CAUTION	Indicates potential risk of equipment damage, data loss, performance degradation, or unexpected results exists if the instructions are not obeyed.
NOTE	Provides additional information to emphasize or supplement important points of the main text.



Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.



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Туре	Symbol	Value 📎
Julisce Co.	JR N	1024
Data capacity	1M	1,048,576
	1G	1,073,741,824
	1k	1000
Frequency, data rate	1M	1,000,000
	1G	1,000,000,000

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1 Overview

D1-H is an advanced application processor designed for RISC-V Multi-Media decoding platform. It integrates a 64-bit XuanTie C906 RISC-V CPU and a HiFi4 DSP to provide the high-efficient computing power. D1-H supports full format decoding such as H.265, H.264, MPEG-1/2/4, JPEG, VC1, and so on. The independent encoder can encode in JPEG or MJPEG. Integrated multi ADCs/DACs and I2S/PCM/DMIC/OWA audio interfaces can work seamlessly with the CPU to accelerate multimedia algorithms and improve the user experience. D1-H supports RGB/LVDS/MIPI DSI/HDMI/CVBS OUT display output interfaces to meet the requirements of the different screen display. D1-H comes with extensive connectivity and interfaces, such as USB, SDIO, EMAC, TWI, UART, SPI, PWM, GPADC, LRADC, TPADC, IR TX&RX, and so on. Besides, D1-H can connect with other different peripherals like WiFi and BT via SDIO and UART.

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2 Features

2.1 CPU Architecture

- XuanTie C906 RISC-V CPU
- 32 KB I-cache + 32 KB D-cache

2.2 DSP Architecture

- HiFi4
- 32 KB L1 I-cache and 32 KB L1 D-cache
- 64 KB I-ram and 64 KB D-ram

2:3 Memory Subsystem

2.3.1 Boot ROM (BROM)

- On-chip memory
- Supports system boot from the following devices:
 - SD card
 - eMMC
 - SPI NOR Flash
 - SPI NAND Flash
- Supports mandatory upgrade process through USB and SD card
- Supports GPIO pin and eFuse module to select the boot media type

2.3.2 SDRAM

- Supports DDR2/DDR3 SDRAM
- Maximum capacity up to 2 GB
- Supports clock frequency up to 533 MHz for DDR2
- Supports clock frequency up to 800 MHz for DDR3

2.3.3 SMHC

- Three SD/MMC host controller (SMHC) interfaces
- The SMHCO controls the devices that comply with the protocol Secure Digital Memory (SD mem-version 3.0)

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- The SMHC1 controls the device that complies with the protocol Secure Digital I/O (SDIO-version 3.0)
- The SMHC2 controls the device that complies with the protocol Multimedia Card (eMMC-version 5.0)
- Maximum performance:
 - SDR mode 150 MHz@1.8 V IO pad
 - DDR mode 50 MHz@1.8 V IO pad
 - DDR mode 50 MHz@3.3 V IO pad
- Supports 1-bit or 4-bit data width
- Supports block size of 1 to 65535 bytes
- Internal 1024-Bytes RX FIFO and 1024-Bytes TX FIFO
- Supports card insertion and removal interrupt
- Supports hardware CRC generation and error detection
- Supports descriptor-based internal DMA controller

2.4 **Video Engine**

- Video decoding
 - H.265 MP@L5.0 up to 4K@30fps
 - H.264 BP/MP/HP@L5.0 up to 4K@24fps
 - H.263 BP up to 1080p@60fps
 - MPEG-4 SP/ASP L5 up to 1080p@60fps
 - MPEG-2 MP/HL up to 1080p@60fps
 - MPEG-1 MP/HL up to 1080p@60fps
 - Xvid up to 1080p@60fps
 - Sorenson Spark up to 1080p@60fps
 - WMV9/VC-1 SP/MP/AP up to 1080p@60fps
 - MJPEG up to 1080p@30fps
- Video encoding
 - JPEG/MJPEG up to 1080p@60fps
 - Supports input picture scaler up/down

Video and Graphics 2.5

2.5.1 Display Engine (DE)

Output size up to 2048 x 2048



- Supports two alpha blending channels for main display and one channel for aux display
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports LBC buffer decoder
- Supports dither output to TCON
- Supports input format Semi-planar YUV422/YUV420/YUV411 and Planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565/palette
- Supports SmartColor2.0 for excellent display experience
 - Adaptive detail/edge enhancement
 - Adaptive color enhancement
 - Adaptive contrast enhancement and fresh tone rectify
- Supports write back for aux display

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2.5.2 De-interlacer (DI)

- Supports YUV420 (Planar/NV12/NV21) and YUV422 (Planar/NV16/NV61) data format
- Supports video resolution from 32x32 to 2048x1280 pixel
- Supports Inter-field interpolation/motion adaptive de-interlace method
- Performance: module clock 600M for 1080p@60Hz YUV420

2.5.3 Graphic 2D (G2D)

- Supports layer size up to 2048 x 2048 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function
- Supports 1/16× to 32× resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter and 32-phase 4-tap vertical anti-alias filter
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit and MaskBlit
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate for normal buffer
- Supports horizontal flip, clockwise 0/90/270 degree rotate for LBC buffer

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2.6 Video Output

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2.6.1 RGB and LVDS LCD

- Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
- Supports LVDS interface with dual link, up to 1920 x 1080@60fps
- Supports LVDS interface with single link, up to 1366 x 768@60fps
- Supports i8080 interface, up to 800 x 480@60fps
- Supports BT656 interface for NTSC and PAL
- RGB666 and RGB565 with dither function
- Gamma correction with R/G/B channel independence

2.6.2 MIPI D\$1

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- Compliance with MIPI DSI v1.01
- Supports 4-lane MIPI DSI, up to 1280 x 720@60fps and 1920 x 1200@60fps
- Supports non-burst mode with sync pulse/sync event and burst mode
- Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports continuous and non-continuous lane clock modes
- Supports bidirectional communication of all generic commands in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and escape modes
- Hardware checksum capabilities

2.6.3 HDMI

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- Compatible with HDMI 1.4
- Supports DDC
- Integrated CEC hardware engine
- Optional color space converter (CSC): RGB (4:4:4) to/from YCbCr (4:4:4 or 4:2:2)
- Video formats:
 - Optional HDMI 1.4b video formats
 - All CEA-861-E video formats up to 1080p at 120 Hz
 - HDMI 1.4b 4K x 2K video formats
 - HDMI 1.4b 3D video modes with up to 340 MHz (TMDS clock)

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- Audio formats:
 - Uncompressed audio formats: IEC60985 L-PCM audio samples, up to 192 kHz
 - Compressed audio formats: IEC61937 compressed audio, up to 768 kHz

2.6.4 **CVBS OUT**

- 1-channel CVBS output
- Supports NTSC and PAL format
- Plug status auto detecting
- 10 bits DAC output

Video Input 2.7

2.7.1 Parallel CSI \infty

- Supports 8-bit digital camera interface (RAW8/YUV422/YUV420)
- Supports BT656, BT601 interface (YUV422)
- Supports ITU-R BT.656 time-multiplexed format up to 2*1080p@30fps in DDR sample mode
- Maximum pixel clock of 148.5 MHz
- Supports de-interlacing for interlace video input
- Supports conversion from YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400
- Supports horizontal and vertical flip

2.7.2 **CVBS IN**

- 2-channel CVBS input and 1-channel CVBS decoder
- Supports NTSC and PAL format
- Supports YUV422/YUV420 format
- With 1 channel 3D comb filter
- Detection for signal locked and 625 lines
- Programmable brightness, contrast, and saturation
- 10-bit video ADCs

2.8 **System Peripherals**

2.8.1 Timer

The timer module implements the timing and counting functions, which includes timer0, timer1, watchdog, and audio video synchronization (AVS)



- The timer0/timer1 is a 32-bit down counter. The timer0 and timer1 are completely consistent
- The watchdog is used to transmit a reset signal to reset the entire system when an exception occurs in the system
- The AVS is used to synchronize the audio and video. The AVS sub-block includes AVS0 and AVS1, which are completely consistent

2.8.2 **High Speed Timer (HSTimer)**

- The HSTimer module consists of HSTimer0 and HSTimer1. HSTimer0 and HSTimer1 are down counters that implement timing and counting functions. They are completely consistent.
- Configurable 56-bit down timer
- Supports 5 prescale factors
- The clock source is synchronized with AHBO clock, much more accurate than other timers
- Supports 2 working modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

2.8.3 Platform-Level Interrupt Controller (PLIC)

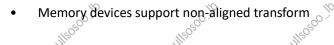
- Sampling, priority arbitration and distribution for external interrupt sources
- The interrupt can be configured as machine mode and super user mode
- Up to 256 interrupt source sampling, supporting level interrupt and pulse interrupt
- 32 levels of interrupt priority
- Maintains independently the interrupt enable for each interrupt mode (machine/super user)
- Maintains independently the interrupt threshold for each interrupt mode (machine/super user)
- Configurable access permission for PLIC registers

2.8.4 DMAC

- Up to 16-ch DMA
- Provides 32 peripheral DMA requests for data reading and 32 peripheral DMA requests for data writing
- Flexible data width of 8/16/32/64-bit
- Programmable DMA burst length
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transferring data with a linked list
- DRQ response includes waiting mode and handshake mode



• DMA channel supports pause function





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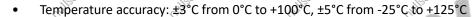
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2.8.5 Clock Controller Unit (CCU)

- 8 PLLs
- One on-chip RC oscillator
- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator
- Supports clock configuration and clock generation for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.8.6 Thermal Sensor Controller (THS)

One thermal sensor located in CPU



- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

2.8.7 LDO Power

- Integrated 2 LDOs (LDOA, LDOB)
- LDOA: 1.8 V power output, LDOB: 1.35 V/1.5 V/1.8 V power output
- LDOA for IO and analog module, LDOB for SDRAM
- Input voltage is 2.4 V to 3.6 V

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2.8.8 RTC

- Implements time counter and timing wakeup
- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- 8 general purpose registers for storing power-off information

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2.8.9 I/O Memory Management Unit (IOMMU)

- Supports virtual address to physical address mapping by hardware implementation
- Supports VE, CSI, DE, G2D, DI parallel address mapping
- Supports VE, CSI, DE, G2D, DI bypass function independently
- Supports VE, CSI, DE, G2D, DI pre-fetch independently
- Supports VE, CSI, DE, G2D, DI interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

2.8.10 Message Box (MSGBOX)

- Supports two CPU to transmit information through channels. Each CPU has a MSGBOX
 - CPU 1: DSP
 - CPU 2: RISC-V
- The channel between two CPU has 4 channels, and the FIFO depth of a channel is 8 x 32 bits

2.8.11 Spinlock

- Provides hardware synchronization mechanism in multi-core systems
- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

2.8.12 Reset

- Integrated internal reset
- Reset D1-H or other IC

2.9 Audio Subsystem

2.9.1 Audio Codec

- Two audio digital-to-analog converter (DAC) channels
 - Supports 16-bit and 20-bit sample resolution
 - 8 kHz to 192 kHz DAC sample rate

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- $100 \pm 2 \text{ dB SNR@A-weight}$, $-85 \pm 3 \text{ dB THD+N}$
- Two audio outputs:
 - None stereo headphone output: HPOUTL/R
 - One stereo differential lineout output: LINEOUTLP/N and LINEOUTRP/N
- Three audio analog-to-digital converter (ADC) channels
 - Supports 16-bit and 20-bit sample resolution
 - 8 kHz to 48 kHz ADC sample rate
 - 95 ± 3dB SNR@A-weight, -80 ± 3dB THD+N
- Five audio inputs:
 - Three differential microphone inputs: MICIN1P/1N, MICIN2P/2N, MICIN3P/3N, or three single-end microphone inputs: MICIN1P, MICIN2P, MICIN3P
 - One stereo LINEIN input: LINEINL/R
 - One Stereo FMIN input: FMINL/R
- Supports Dynamic Range Controller adjusting the DAC playback and ADC recording
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports interrupts and DMA
- Two LDOs integrated:
 - ALDO: internal ALDO output for AVCC
 - HPLDO: internal HPLDO output for HPVCC

2.9.2 I2S/PCM

- - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
 - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and Receive data FIFOs
 - Programmable FIFO thresholds
 - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clock
 - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral 12S/PCM satisfy Timing Parameters)
 - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode

Three I2S/PCM external interfaces (I2S0, I2S1, I2S2) for connecting external power amplifier and MIC ADC Compliant with standard Philips Inter-IC sound (I2S) bus specification



- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
 - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
 - Sample rate from 8 kHz to 384 kHz (CHAN = 2)
 - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

2.9.3 **DMIC**

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

One Wire Audio (OWA) 2.9.4

- One OWA TX and one OWA RX
- Compliance with S/PDIF interface
- IEC-60958 and IEC-61937 transmitter and receiver functionality
 - IEC-60958 supports 16-bit, 20-bit, and 24-bit data formats
 - IEC-61937 uses the IEC-60958 series for the conveying of non-linear PCM bit streams, each sub-frame transmits 16-bit
- **TXFIFO** and RXFIFO
 - One 128×24bits TXFIFO and one 64×24bits RXFIFO for audio data transfer
 - Programmable FIFO thresholds
- Supports TX/RX DMA slave interface
- Supports multiple function clock
 - Separate clock for OWA TX and OWA RX
 - The clock of TX function includes 24.576 MHz and 22.579 MHz frequency
 - The clock of RX function includes 24.576*8MHz frequency
- Supports hardware parity on TX/RX
 - Hardware parity checking on the receiver
 - Hardware parity generation on the transmitter
- Supports channel status capture on the receiver
- Supports channel sample rate capture on the receiver
- Supports insertion detection for the receiver
- Supports channel status insertion for the transmitter



• Supports interrupts and DMA

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2.10 Security System

2.10.1 Crypto Engine (CE)

- Supports Symmetrical algorithm for encryption and decryption: AES, DES, TDES
 - Supports ECB, CBC, CTS, CTR, CFB, OFB mode for AES
 - Supports 128/192/256-bit key for AES
 - Supports ECB, CBC, CTR mode for DES/TDES
- Supports Hash algorithm for tamper proofing: MD5, SHA, HMAC
 - Supports SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
 - Supports HMAC-SHA1, HMAC-SHA256 for HMAC
 - Supports multi-package mode for MD5/SHA1/SHA224/SHA256/SHA384/SHA512
- Supports Asymmetrical algorithm for signature verification: RSA
 - RSA supports 512/1024/2048-bit width
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Internal DMA controller for data transfer with memory

2.10.2 Security ID (SID)

- Supports 2 Kbits eFuse
- Backup eFuse information by using SID_SRAM
- Burning the key to the SID
- Reading the key use status in the SID
- Loading the key to the CE

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2.11 External Peripherals

2.11.1 USB DRD

- One USB 2.0 DRD (USB0), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- Supports USB Host function
 - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
 - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a

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- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)
- Supports only 1 USB Root port shared between EHCI and OHCI
- Supports USB Device function
 - Supports High-Speed (HS, 480 Mbit/s) and Full-Speed (FS, 12 Mbit/s)
 - Supports bi-directional endpoint0 (EP0) for Control transfer
 - Up to 10 user-configurable endpoints (EP1+, EP1-, EP2+, EP2-, EP3+, EP3-, EP4+, EP4-, EP5+, EP5-) for Bulk transfer, Isochronous transfer and Interrupt transfer
 - Up to (8 KB + 64 Bytes) FIFO for all EPs (including EP0)
 - Supports interface to an external Normal DMA controller for every EP
- Supports an internal DMA controller for data transfer with memory
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral modes
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power optimization and power management capabilities
- Device and host controller share a 8K SRAM and a physical PHY

2.11.2 USB HOST

- One USB 2.0 HOST (USB1), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- Supports USB2.0 Host function
 - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
 - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
 - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) Device
 - Supports only 1 USB Root port shared between EHCI and OHCI
- An internal DMA Controller for data transfer with memory

2.11.3 EMAC

- One EMAC interface for connecting external Ethernet PHY

Compliant with IEEE 802.3-2002 standard



- Supports both full-duplex and half-duplex operations
- Provides the management data input/output (MDIO) interface for PHY device configuration and management with configurable clock frequencies
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
 - Supports linked-list descriptor list structure
 - Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
 - Comprehensive status reporting for normal operation and transfers with errors
- 4 KB TXFIFO for transmission packets and 16 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

2.11.4 UART

- Up to 6 UART controllers (UARTO, UART1, UART2, UART3, UART4, UART5)
- UARTO, UART4, UART5: 2-wire; UART1, UART2, UART3: 4-wire
- Compatible with industry-standard 16450/16550 UARTs
- Supports IrDA-compatible slow infrared (SIR) format
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
 - Each of them is 64 bytes (For UARTO)
 - Each of them is 256 bytes (For UART1, UART2, UART3, UART4, and UART5)
- The working reference clock is from the APB bus clock
 - Speed up to 4 Mbit/s with 64 MHz APB clock
 - Speed up to 1.5 Mbit/s with 24 MHz APB clock
- 5 to 8 data bits for RS-232 characters, or 9 bits RS-485 format
- 1, 1.5 or 2 stop bits
- Programmable parity (even, odd, or no parity)
- Supports TX/RX DMA slave controller interface
- Supports software/hardware flow control
- Supports RX DMA Master interface (Only for UART1)
- Supports auto-flow by using CTS & RTS (Only for UART1/2/3)

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2.11.5 SPI and SPI DBI

- Up to 2 SPI controllers (SPIO, SPI1)
- The SPIO only supports SPI mode; The SPI1 supports SPI mode and display bus interface (DBI) mode
- SPI mode:
 - Full-duplex synchronous serial interface
 - Master/slave configurable
 - Mode0 to Mode3 are supported for both transmit and receive operations
 - 8-bit wide by 64-entry FIFO for both transmit and receive data
 - Polarity and phase of the Chip Select (SPI-CS) and SPI Clock (SPI-CLK) are configurable
 - Supports 3-wire/4-wire SPI
 - Supports programmable serial data frame length: 1-bit to 32-bit
 - Supports Standard SPI, Dual-Output/Dual-Input SPI, Dual IO SPI, Quad-Output/Quad-Input SPI
- DBI mode:
 - Supports DBI Type C 3 Line/4 Line Interface Mode
 - Supports 2 Data Lane Interface Mode
 - Supports RGB111/444/565/666/888 video format
 - Maximum resolution of RGB666 240 x 320@30Hz with single data lane
 - Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
 - **Supports Tearing effect**
 - Supports software flexible control video frame rate

2.11.6 Two Wire Interface (TWI)

- Up to 4 TWI controllers (TWI0, TWI1, TWI2, TWI3)
- Compliant with I2C bus standard
- Supports standard mode (up to 100 kbit/s) and fast mode (up to 400 kbit/s)
- Supports 7-bit and 10-bit device addressing modes
- Supports master mode or slave mode
- Master mode features:
 - Supports the bus arbitration in the case of multiple master devices
 - Supports clock synchronization and bit and byte waiting
 - Supports packet transmission and DMA
- Slave mode features:
 - Interrupt on address detection



The TWI controller includes one TWI engine and one TWI driver. And the TWI driver supports packet transmission and DMA mode when TWI works in master mode

2.11.7

CIR Receiver (CIR_RX)

- One CIR_RX interface (IR-RX)
- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.14.8 CIR Transmitter (CIR TX)

- One CIR_TX interface (IR-TX)
- Supports arbitrary wave generator
- Configurable carrier frequency
- Supports handshake mode and waiting mode of DMA
- 128 bytes FIFO for data buffer

2.11.9 PWM

- Supports 8 independent PWM channels (PWM0 to PWM7)
 - Supports PWM continuous mode output
 - Supports PWM pulse mode output, and the pulse number is configurable
 - Output frequency range: 0 to 24 MHz or 100 MHz
 - Various duty-cycle: 0% to 100%
 - Minimum resolution: 1/65536
- Supports 4 complementary pairs output
 - PWM01 pair (PWM0 + PWM1), PWM23 pair (PWM2 + PWM3), PWM45 pair (PWM4 + PWM5), PWM67 pair (PWM6 + PWM7)
 - Supports dead-zone generator, and the dead-zone time is configurable
- Supports 4 group of PWM channel output for controlling stepping motors
 - Supports any plural channels to form a group, and output the same duty-cycle pulse
 - In group mode, the relative phase of the output waveform for each channel is configurable
- Supports 8 channels capture input



- Supports rising edge detection and falling edge detection for input waveform pulse
- Supports pulse-width measurement for input waveform pulse

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2.11.10 General Purpose ADC (GPADC)

- 2-ch successive approximation register (SAR) analog-to-digital converter (ADC)
- 12-bit sampling resolution and 8-bit precision
- 64 FIFO depth of data register
- Power reference voltage: AVCC, analog input voltage range: 0 to AVCC
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode

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2.11.11 Touch Panel ADC (TPADC)

- 12 bit SAR type A/D converter
- Configurable sample frequency up to 1 MHz
- One 32x12 FIFO for storing A/D conversion result
- Supports DMA slave interface
- Supports 4-wire resistive touch panel input detection
 - Supports pen down detection with programmable sensitivity
 - Supports single touch coordinate measurement
 - Supports dual touch detection
 - Supports touch pressure measurement with programmable threshold
 - Supports median and averaging filter for noise reduction
 - Supports X and Y coordinate exchange function
- Supports Aux ADC with up to 4 channels

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2.11.12 Low Rate ADC (LRADC)

- One LRADC input channel
- 6-bit sampling resolution and 5-bit precision
- Sample rate up to 2 kHz
- Supports hold Key and general Key
- Supports normal, continuous and single working mode

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Power supply voltage: AVCC, power reference voltage: 0.75*AVCC, analog input and detected voltage range: 0 to 1.266 V

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2.11.13 LEDC

- LEDC is used to control the external intelligent control LED lamp
- Configurable LED output high/low level width
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- LED data transfer rate up to 800 kbit/s

2.12 Package

• LFBGA 337 balls, 13 mm x 13 mm body size, 0.65 mm ball pitch, 0.35 mm ball size

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3 Block Diagram

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Figure 3-1 shows the system block diagram of the D1-H.

Figure 3-1 D1-H System Block Diagram



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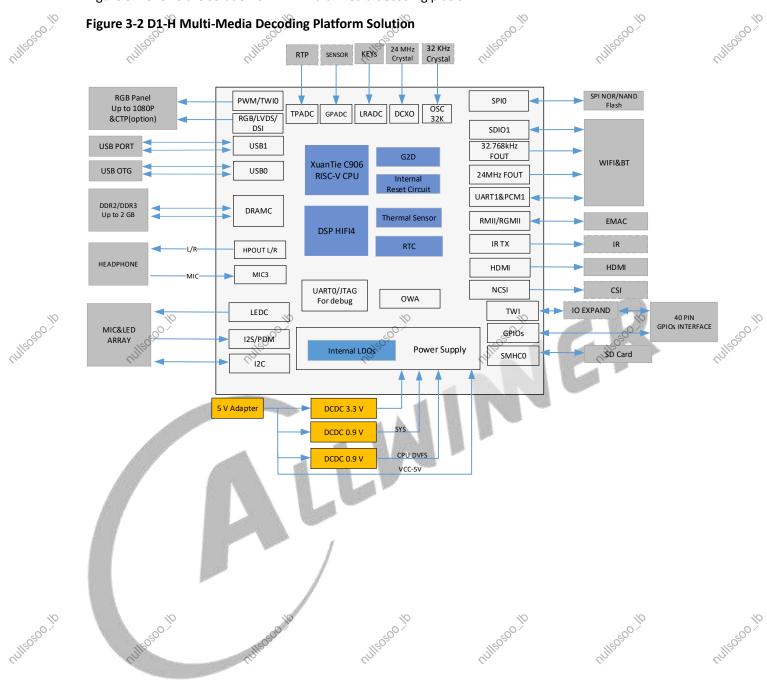
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Figure 3-2 shows the solution of D1-H multi-media decoding platform.







4 Pin Description

4.1 Pin Quantity

Table 4-1 lists the pin quantity of the D1-H.

Table 4-1 D1-H Pin Quantity

Pin Type	Quantity
1/0	202
Power	35
Ground	92
DDR Power	8
Total Total	337
Ultegs Ultegs	Theog.

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4.2 Pin Characteristics

Table 4-2 lists the characteristics of the D1-H pins from the following seven aspects.

[1].Ball#: Package ball numbers associated with each signal.

[2].Pin Name: The name of the package pin.

[3]. Type: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

- [4].Ball Reset State: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.
- [5].Pull Up/Down: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.
- **[6].Default Buffer Strength**: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.
- [7]. Power Supply: The voltage supply for the IO buffers of the terminal.

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Table 4-2 Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
SDRAM	·					
V13	SA0	0	NA	NA	NA	VCC-DRAM
W13	SA1	0	NA	NA	NA	VCC-DRAM
V14	SA2	0	NA	NA	NA	VCC-DRAM
U13	SA3	0	NA	NA	NA	VCC-DRAM
U15	SA4	0	NA	NA	NA	VCC-DRAM
V11	SA5	0	NA	NA	NA ×	VCC-DRAM
W11	SAG	O III SO SOO	NA IIIIEOEOO	NA NIIS	NA Juleos	VCC-DRAM
Y13	SA7	0	NA	NA	NA	VCC-DRAM
W14	SA8	0	NA	NA	NA	VCC-DRAM
Y15	SA9	0	NA NA	NA	NA	VCC-DRAM
W12	SA10	0	NA	NA	NA	VCC-DRAM
W15	SA11	0	NA	NA	NA	VCC-DRAM
W16	SA12	0	NA	NA	NA	VCC-DRAM
R15	SA13	0	NA	NA	NA	VCC-DRAM
V16	SA14	O TENSOR IN	NA NA	NA NA	NA SO	VCC-DRAM
T15	SA15	0	NA RIP	NA	NA	VCC-DRAM
V10	SBA0	0	NA	NA	NA	VCC-DRAM
W10	SBA1	0	NA	NA	NA	VCC-DRAM
Y11	SBA2	0	NA	NA	NA	VCC-DRAM
W9	SCKE0	0	NA	NA	NA	VCC-DRAM
Y9	SCKE1	0	NA	NA	NA	VCC-DRAM
U10	SCKN	0	NA	NA	NA	VCC-DRAM



	Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
16	T10	SCKP	Ourillage	NA NIIISOS	NA NINS	NA rulliso	VCC-DRAM
	R12	SCS0	0	NA	NA	NA	VCC-DRAM
	R13	SCS1	0	NA	NA	NA	VCC-DRAM
	W7	SDQ0	I/O	NA	NA	NA	VCC-DRAM
	V7	SDQ1	I/O	NA	NA	NA	VCC-DRAM
	W8	SDQ2	I/O	NA	NA	NA	VCC-DRAM
	V8	SDQ3	I/O	NA	NA	NA	VCC-DRAM
	W4	SDQ4	1/0	NA 🦠	NA	NA .	VCC-DRAM
150	Y4	SDQ5	1/0/15050	NA NIIISOSO	NA NIIE	NA Rulled	VCC-DRAM
	V5	SDQ6	1/0	NA	NA	NA	VCC-DRAM
	W5	SDQ7	1/0	NA NA	NA	NA	VCC-DRAM
	U4	SDQ8	1/0	NA	NA	NA	VCC-DRAM
	U7	SDQ9	1/0	NA	NA	NA	VCC-DRAM
	U5	SDQ10	1/0	NA	NA	NA	VCC-DRAM
	Т6	SDQ11	I/O	NA	NA	NA	VCC-DRAM
	U6	SDQ12	1/0	NA	NA	NA %	VCC-DRAM
150	R7	SDQ13	I/O ECECIÓ	NA JUNSOSOO	NA NA	NA UIII	VCC-DRAM
	T4	SDQ14	1/0	NA	NA	NA	VCC-DRAM
	R6	SDQ15	I/O	NA	NA	NA	VCC-DRAM
	Y8	SDQM0	0	NA	NA	NA	VCC-DRAM
	W2	SDQM1	0	NA	NA	NA	VCC-DRAM
	Y6	SDQSON	I/O	NA	NA	NA	VCC-DRAM
	W6	SDQS0P	I/O	NA	NA	NA	VCC-DRAM
	Y3	SDQS1N	I/O	NA	NA	NA	VCC-DRAM



Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
W3	SDQS1P	I/O	NA PULISO	NA RIJIS	NA Rulliso	VCC-DRAM
T12	SODT0	0	NA	NA	NA	VCC-DRAM
U12	SODT1	0	NA	NA	NA	VCC-DRAM
Т9	SCAS	0	NA	NA	NA	VCC-DRAM
U9	SRAS	0	NA	NA	NA	VCC-DRAM
Y17	SRST	0	NA	NA	NA	VCC-DRAM
U16	SVREF	Р	NA	NA	NA	VCC-DRAM
R90	SWE	0 %	NA 🦠	NA NA	NA .	VCC-DRAM
U17	SZQ	AĮ,jl ^s 0s00	NA NIIISOSO	NA RIJIEC	NA Rulled	VCC-DRAM
N8, N9, N10, P8, P9, P10	VCC-DRAM	P	NA	NA	NA	NA
P14	VDD18-DRAM	Р	NA	NA	NA	NA
GPIOB	7					
J16	РВО	1/0	Z	PU/PD	4	VCC-IO
J17	PB1	1/0	z /	PU/PD	4	VCC-IO
M16	PB2	1/0	Z	PU/PD	4	VCC-IO
M15	PB3	1/0	Z RIJESSO JY	PU/PD		VCC-IO
K16	PB4	1/0	Z rullis	PU/PD RUITE	4 rullish	VCC-IO
K15	PB5	1/0	Z	PU/PD	4	VCC-IO
K17	PB6	1/0	Z	PU/PD	4	VCC-IO
J15	PB7	1/0	Z	PU/PD	4	VCC-IO
G15	PB8	1/0	Z	PU/PD	4	VCC-IO
G16	PB9	1/0	Z	PU/PD	4	VCC-IO
F17	PB10	1/0	Z	PU/PD	4	VCC-IO



	Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
lle,	F15	PB11	1/0	Z NIIISOS	PU/PD Rulls	4 Pulls	VCC-IO
	F16	PB12	I/O	Z	PU/PD	4	VCC-IO
	GPIOC						
•	F2	PC0	I/O	Z	PU/PD	4	VCC-PC
	F1	PC1	I/O	Z	PU/PD	4	VCC-PC
	G3	PC2	I/O	Z	PU/PD	4	VCC-PC
	G2	PC3	1/0	PU	PU/PD	4	VCC-PC
	H30	PC4	1/0	PU	PU/PD	4%	VCC-PC
lle.	F5	, 8 C5	1/0/15050	PU NINESON	PU/PD NIE	4 7,11180	VCC-PC
	G6	PC6	1/0	Z	PU/PD	4	VCC-PC
	G5	PC7	1/0	Z	PU/PD	4	VCC-PC
•	G4	VCC-PC	Р	NA	NA	NA	NA
	GPIOD	7					
•	W19	PD0	1/0	Z	PU/PD	4	VCC-PD
•	V20	PD1	I/O	Z	PU/PD	4	VCC-PD
•	V19	PD2	1/0	Z	PU/PD	4	VCC-PD
11/5	U20	PD3	I/O BUSIN	Z _{UII} sosoo)	PU/PD	4	VCC-PD
•	U19	PD4	1/0	Z	PU/PD	4	VCC-PD
•	U18	PD5	I/O	Z	PU/PD	4	VCC-PD
•	T19	PD6	I/O	Z	PU/PD	4	VCC-PD
	T18	PD7	I/O	Z	PU/PD	4	VCC-PD
	R20	PD8	I/O	Z	PU/PD	4	VCC-PD
	R19	PD9	I/O	Z	PU/PD	4	VCC-PD
	T17	PD10	I/O	Z	PU/PD	4	VCC-PD
L	10	10	10	1	,	10	10



	Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4] Z	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
16	R17	PD11	I/O	Z Pulls	PU/PD Nills	4 rullso	VCC-PD
	P19	PD12	I/O	Z	PU/PD	4	VCC-PD
	P18	PD13	I/O	Z	PU/PD	4	VCC-PD
	N17	PD14	I/O	Z	PU/PD	4	VCC-PD
	N16	PD15	I/O	Z	PU/PD	4	VCC-PD
	N20	PD16	1/0	Z	PU/PD	4	VCC-PD
	N19	PD17	1/0	Z	PU/PD	4	VCC-PD
	M19	PD18	1/0	Z	PU/PD	4%	VCC-PD
1202	M18	, BD19	I/O//SOS	Z NINEGEO I	PU/PD RIJIES	4 / / / / / / / / / / / / / / / / / / /	VCC-PD
	W18	PD20	1/0	Z	PU/PD	4	VCC-PD
	V18	PD21	1/0	Z	PU/PD	4	VCC-PD
	Y18	PD22	1/0	Z	PU/PD	4	VCC-PD
	R16	VCC-LVDS	P	NA	NA	NA	NA
	T16	VCC-PD	Р	NA	NA	NA	NA
	GPIOE			/			
	V1	PEO 👋	1/0	Z	PU/PD	4	VCC-PE
1505	U1	RE1	I/O Ededo	Z _{nulls} osoo 2	PU/PD NIJES	4 (1)1505	VCC-PE
	U2	PE2	1/0	Z	PU/PD	4	VCC-PE
	U3	PE3	1/0	Z	PU/PD	4	VCC-PE
	T2	PE4	I/O	Z	PU/PD	4	VCC-PE
	Т3	PE5	I/O	Z	PU/PD	4	VCC-PE
	R1	PE6	1/0	Z	PU/PD	4	VCC-PE
	R2	PE7	I/O	Z	PU/PD	4	VCC-PE
	R3	PE8	I/O	Z	PU/PD	4	VCC-PE



	Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
18	P2	PE9	1/0	Z nullsos	PU/PD NIII	4 (1)1150	VCC-PE
	Р3	PE10	1/0	Z	PU/PD	4	VCC-PE
	N1	PE11	1/0	Z	PU/PD	4	VCC-PE
	R5	PE12	1/0	Z	PU/PD	4	VCC-PE
	R4	PE13	1/0	Z	PU/PD	4	VCC-PE
	N4	PE14	1/0	Z	PU/PD	4	VCC-PE
	N5	PE15	1/0	Z	PU/PD	4	VCC-PE
	N6.	PE16 %	1/0	Z	PU/PD	4,0	VCC-PE
150	M6	PE17	I/O/ISOS	Z _{NJ} IISOSO	PU/PD RUJIEC	4 7,11130	VCC-PE
	M4	VCC-PE	P	NA	NA NA	NA	NA
	GPIOF			- 11			
	C2	PFO	1/0	Z	PU/PD	4	VCC-PF
	C1	PF1	١/٥	Z	PU/PD	4	VCC-PF
	D2	PF2	1/0	Z	PU/PD	4	VCC-PF
	D1	PF3	1/0	z	PU/PD	4	VCC-PF
	E3 (5)	PF4	1/0	Z	PU/PD	4	VCC-PF
150	E2	RES CONTRACTOR	I/O Ededo	Z _{ullsosoo})	PU/PD RIJIES	4 (1)1505	VCC-PF
	D3	PF6	1/0	Z	PU/PD	4	VCC-PF
	F4	VCC-PF	Р	NA	NA	NA	NA
	GPIOG						
	B2	PG0	1/0	Z	PU/PD	4	VCC-PG
	В3	PG1	1/0	Z	PU/PD	4	VCC-PG
	A3	PG2	1/0	Z	PU/PD	4	VCC-PG
	C3	PG3	I/O	Z	PU/PD	4	VCC-PG



	3a[[# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
Δ	.4	PG4	I/O	Z KIIISOS	PU/PD Nills	4 (11)	VCC-PG
В	34	PG5	I/O	Z	PU/PD	4	VCC-PG
В	35	PG6	I/O	Z	PU/PD	4	VCC-PG
C	C5	PG7	I/O	Z	PU/PD	4	VCC-PG
Δ	۸6	PG8	I/O	Z	PU/PD	4	VCC-PG
В	36	PG9	I/O	Z	PU/PD	4	VCC-PG
C	6	PG10	I/O	Z	PU/PD	4	VCC-PG
	040	PG11	1/0	Z	PU/PD	4%	VCC-PG
, C)5	, PG12	1/0/1/20/20	Z _{rullsogo j}	PU/PD NIE	4	VCC-PG
С	96	PG13	1/0	Z	PU/PD	4	VCC-PG
Ε	6	PG14	1/0	Z	PU/PD	4	VCC-PG
F	6	PG15	1/0	Z	PU/PD	4	VCC-PG
F	7	PG16	I/O	Z	PU/PD	4	VCC-PG
Е	7	PG17	1/0	Z	PU/PD	4	VCC-PG
С	07	PG18	I/O	z	PU/PD	4	VCC-PG
Е	4	VCC-PG	P	NA	NA	NA %	NA
S	ystem	7111E0500	THEOROG	nills0s00	aille	500 , UII5056	0/
Ν	13	NMI	I/O, OD	NA	NA	NA	VCC-RTC
Ν	12	TEST	I	PD	PU/PD	NA	VCC-RTC
Д	18	FEL	1	PU	PU/PD	NA	VCC-IO
٨	/12	RESET	I, OD	NA	NA	NA	VCC-RTC
L	RADC					'	
В	312	LRADC	Al	NA	NA	NA	AVCC
G	SPADC .						



Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
C13	GPADC0	Afullson	NA (IIII)	NA RUITS	NA RIJIS	AVCC
B13	GPADC1	Al	NA	NA	NA	AVCC
TPADC						
C12	TP-X1	AI	NA	NA	NA	AVCC
A11	TP-X2	Al	NA	NA	NA	AVCC
B11	TP-Y1	Al	NA	NA	NA	AVCC
C11	TP-Y2	Al	NA	NA	NA	AVCC
USB	0)0	0/10		>	00)9	0/0
C7	USB0-DM	A J/O	NA NINGO	NA MILIE	NA Rullso	VCC-IO
В7	USB0-DP	A I/O	NA	NA	NA	VCC-IO
B8	USB1-DM	A I/O	NA A	NA	NA	VCC-IO
A8	USB1-DP	A I/O	NA	NA	NA	VCC-IO
CVBS IN	7					
В9	TVIN0	Al	NA	NA	NA	VCC-TVIN
C9	TVIN1	Al	NA	NA	NA	VCC-TVIN
E10	TVIN-VRP	Al	NA	NA	NA %	VCC-TVIN
F10	TVIN-VRN	Al Hededa	NA UIIEOEOO	NA NA	.00	VCC-TVIN
D9	VCC-TVIN	Р	NA	NA	NA	NA
E9	GND-TVIN	G	NA	NA	NA	NA
CVBS OUT	·	•				
E19	TVOUT0	AO	NA	NA	NA	VCC-TVOUT
E18	VCC-TVOUT	Р	NA	NA	NA	NA
HDMI	'	•				•
F19	HCEC	1/0	NA	NA	NA	VCC-HDMI
10	100	10		\$	10	10



	Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
19	F20	ННРD	I/O	NA RIJISOS	NA RIJIS	NA (iJIIS	VCC-HDMI
-	G19	HSCL	0	NA	NA	NA	VCC-HDMI
	G18	HSDA	1/0	NA	NA	NA	VCC-HDMI
	K19	HTX0N	AO	NA	NA	NA	VCC-HDMI
	K18	НТХОР	AO	NA	NA	NA	VCC-HDMI
•	J19	HTX1N	AO	NA	NA	NA	VCC-HDMI
	J18	HTX1P	AO	NA	NA	NA	VCC-HDMI
-	H20	HTX2N	AO 🔊	NA S	NA NA	NA O	VCC-HDMI
15	H19	HTX2P	AQIISOSO	NA NIISOSO	NA RIJIEC	NA Rullsos	VCC-HDMI
	L20	HTXCN	AO	NA	NA	NA	VCC-HDMI
•	L19	НТХСР	AO	NA A	NA	NA	VCC-HDMI
	M17	VCC-HDMI	P	NA	NA	NA	NA
	Audio Codec			46			
	D20	MICIN1P	Al	NA	NA	NA	AVCC
-	D19	MICIN1N	AI	NA	NA	NA	AVCC
-	E15	MICIN2P	Al	NA	NA	NA %	AVCC
15	D15	MICIN2N	Al III GEORGE	NA NIISOSOO	NA NINS	NA _{UII} SOS	AVCC
	D17	MICIN3P	Al	NA	NA	NA	AVCC
-	D16	MICIN3N	AI	NA	NA	NA	AVCC
	C17	FMINR	AI	NA	NA	NA	AVCC
	B17	FMINL	AI	NA	NA	NA	AVCC
	C16	LINEINR	AI	NA	NA	NA	AVCC
	B16	LINEINL	AI	NA	NA	NA	AVCC
	C15	LINEOUTLN	AO	NA	NA	NA	AVCC
-	10	10	10)	10	10



	Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
IIe,	B15	LINEOUTLP	AO	NA NITTO	NA RIIII	NA Pulls	AVCC
	C14	LINEOUTRN	AO	NA	NA	NA	AVCC
	B14	LINEOUTRP	AO	NA	NA	NA	AVCC
	D13	HPOUTR	AO	NA	NA	NA	HPVCC
	F13	HPOUTL	AO	NA	NA	NA	HPVCC
	E13	HPOUTFB	Al	NA	NA	NA	HPVCC
	D10	HPVCC	Р	NA	NA	NA	NA
	A13	HP-DET	Al NO	NA 🦠	NA	NA NA	AVCC
1100	E12	HPLDO	P _N IISOSC	NA RIJISOSO	NA MILIE	NA RUISO	NA
	D12	HPLDOIN	Р	NA	NA NA	NA	NA
	E17	HBIAS	AO	NA NA	NA	NA	VCC-IO
	E16	MBIAS	AO	NA	NA	NA	VCC-IO
	A17	MIC-DET	Al	NA	NA	NA	AVCC
	B19	VRA1	AO	NA	NA	NA	AVCC
	B18	VRA2	AO	NA	NA	NA	AVCC
	C20	VDD33	P	NA	NA	NA	NA
1150	C18	AVCC	Pullsdsdd	NA IIIISOSOO	NA NA	NA LIHEOS	NA
Ī	C19	ALDO	Р	NA	NA	NA	NA
	D18	AGND	G	NA	NA	NA	NA
Ī	RTC & PLL						
Ī	L2	X32KIN	AI	NA	NA	NA	VCC-RTC
j	L3	X32KOUT	AO	NA	NA	NA	VCC-RTC
	K5	VCC-RTC	Р	NA	NA	NA	NA
	J5	VCC-PLL	Р	NA	NA	NA	NA



,	Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]
11/5	DCXO	Phillips.	Rills	Willso	Aillise	hilliso	4)
	K1	DXIN	AI	NA	NA	NA	VCC-DCXO
	K2	DXOUT	AO	NA	NA	NA	VCC-DCXO
	J2	REFCLK-OUT	AO	NA	NA	NA	VCC-DCXO
	K4	VCC-DCXO	Р	NA	NA	NA	NA
	Power						
	M7	LDO-IN	Р	NA	NA	NA	NA
	L7.0	LDOA-OUT	P 19	NA ×	NA NA	NA.	NA
119	N7	LDOB-OUT	Prillsoad	NA NIIISOSOO	NA nulls		NA S
	G17	VCC-IO	Р	NA	NA NA	NA	NA
	J4	VCC-EFUSE	Р	NA NA	NA	NA	NA
	G13, G14, H13, H14, J13, J14	VDD-SYS	P	NA	NA	NA	NA
	G7, G8, H7, H8, H9	VDD-CPU	P	NA	NA	NA	NA
	G9	VDD-CPUFB	Р	NA	NA	NA	NA
	GND	10	Jan	14		10	10
	A1, A15, A19, A2, A20, B1, B10, B20, C10, C4, C8, E5, F12, F18, F3, F9, G10, G11, G12,		P.H. Berger	RIHESO X	Hillec	RIJISOS	
	H1, H10, H11, H12, H18, H2, J10, J11, J12, J3, J6, J7, J8, J9, K10, K11, K12, K13, K14, K3, K6, K7, K8, K9, L10, L11,	GND	G	NA	NA	NA NA	NA



(Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/ Down ^[5]	Default Buffer Strength ^[6] (mA)	Power Supply ^[7]	00/10
Uille	L12, L13, L14,	Uille	Ullip	Rills	Rills	Rills	Cillis.	
	L18, L8, L9,							
	M10, M11,							
	M12, M13,							
	M14, M3, M5,							
	M8, M9, N11,							
	N12, N13, N14,							
	N15, N18, P11,							
	P12, P13, P7,							
	R10, R18, T13,							
	T5, T7, V12,							
	V15, V17, V2,							
	V3, V4, V6, V9,							
	W1, W17,	.20	.50	.,~				
	W20, Y1, Y19,	20)	11180800 110	.oo)	,	00,1	1505	.00 //
Mills	Y2, Y20	MILSOS	Rillsos	rull ⁵⁰ 500)	nulls	30 N	Silleos	2



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4.3 **GPIO Multiplex Function**

The following table provides a description of the D1-H GPIO multiplex function.



For each GPIO, Function0 is input function; Function1 is output function; Function9 to Function13 are reserved.

		0-/			_	. 0
Table	12	CBIO	N/III+i	nlov	Eunc	tio'r
Iable	4-3	GRIO	iviuiti	DIEX	runc	LIVII

	1112		1113	11500	11/2	11/202	1113		11/2	11500
Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PB0		1/0	PWM3	IR-TX	TWI2-SCK	SPI1-WP/ DBI-TE	UARTO-TX	UART2-TX	OWA-OUT	PB-EINTO
PB1		1/0	PWM4	I2S2-DOUT3	TWI2-SDA	I2S2-DIN3	UARTO-RX	UART2-RX	IR-RX	PB-EINT1
PB2		I/O	LCD0-D0	I2S2-DOUT2	TWI0-SDA	I2S2-DIN2	LCD0-D18	UART4-TX		PB-EINT2
PB3		1/0	LCD0-D1	I2S2-DOUT1	TWI0-SCK	I2S2-DINO	LCD0-D19	UART4-RX		PB-EINT3
PB4	,,,	I/O	LCD0-D8	I2S2-DOUTO	TWI1-SCK	I2S2-DIN1	LCD0-D20	UART5-TX		PB-EINT4
PB5	150500 10	I/O	LCD0-D9	I2S2-BCLK	TWI1-SDA	PWM0	LCD0-D21	UART5-RX	1150500 JH	PB-EINT5
PB6)	I/O	LCD0-D16	I2S2-LRCK	TWI3-SCK	PWM1	LCD0-D22	UART3-TX	CPUBIST0	PB-EINT6
PB7		I/O	LCD0-D17	I2S2-MCLK	TWI3-SDA	IR-RX	LCD0-D23	UART3-RX	CPUBIST1	PB-EINT7
PB8	GPIOB	1/0	DMIC-DATA3	PWM5	TWI2-SCK	SPI1-HOLD/ DBI-DCX/ DBI-WRX	UARTO-TX	UART1-TX		PB-EINT8
PB9	,	1/0	DMIC-DATA2	PWM6	TWI2-SDA	SPI1-MISO/ DBI-SDI/ DBI-TE/ DBI-DCX	UARTO-RX	UART1-RX	, o /	PB-EINT9
PB10		I/O	DMIC-DATA1	PWM7	TWI0-SCK	SPI1-MOSI/ DBI-SDO	CLK-FANOUTO	UART1-RTS	Nege .	PB-EINT10
PB11		1/0	DMIC-DATA0	PWM2	TWI0-SDA	SPI1-CLK/ DBI-SCLK	CLK-FANOUT1	UART1-CTS		PB-EINT11
PB12		1/0	DMIC-CLK	PWM0	OWA-IN	SPI1-CS/ DBI-CSX	CLK-FANOUT2	IR-RX		PB-EINT12
PC0		I/O	UART2-TX	TWI2-SCK	LEDC-DO					PC-EINTO
PC1		1/0	UART2-RX	TWI2-SDA						PC-EINT1
PC2	1150500 110	1/0	SPIO-CLK	SDC2-CLK	2010	00/9	200	10	, o jo	PC-EINT2
PC3	GPIOC	1/0	SPIO-CSO	SDC2-CMD	rilled	rullsoft	Rillege	Ć,		RC-EINT3
PC4	GFIOC	I/O	SPI0-MOSI	SDC2-D2	BOOT-SEL0					PC-EINT4
PC5		I/O	SPI0-MISO	SDC2-D1	BOOT-SEL1					PC-EINT5
PC6		I/O	SPIO-WP	SDC2-D0	UART3-TX	TWI3-SCK	DBG-CLK			PC-EINT6
PC7		I/O	SPI0-HOLD	SDC2-D3	UART3-RX	TWI3-SDA	TCON-TRIG			PC-EINT7
PD0	CDICE	I/O	LCD0-D2	LVDS0-V0P	DSI-DOP	TWI0-SCK				PD-EINT0
PD1	GPIOD	I/O	LCD0-D3	LVDS0-V0N	DSI-DON	UART2-TX				PD-EINT1

Illso

1150500

1150500



Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PD2		I/O	LCD0-D4	LVDS0-V1P	DSI-D1P	UART2-RX				PD-EINT2
PD3		1/0	LCD0-D5	LVDS0-V1N	DSI-D1N	UART2-RTS				PD-EINT3
PD4		1/0	LCD0-D6	LVDS0-V2P	DSI-CKP	UART2-CTS				PD-EINT4
PD5	10	1/0	LCD0-D7	LVDS0-V2N	DSI-CKN	UART5-TX		10	1/0	PD-EINT5
PD6	1150500 110	1/0	LCD0-D10	LVDSQ-CKP	DSI-D2P	UART5-RX	nulsosoc		We0200 Y	PD-EINT6
PD7		I/O	LCD0-D11	LVDS0-CKN	DSI-D2N	UART4-TX				PD-EINT7
PD8		I/O	LCD0-D12	LVDS0-V3P	DSI-D3P	UART4-RX				PD-EINT8
PD9		1/0	LCD0-D13	LVDS0-V3N	DSI-D3N	PWM6				PD-EINT9
PD10		1/0	LCD0-D14	LVDS1-V0P	SPI1-CS/DBI-CSX	UART3-TX				PD-EINT10
PD11		1/0	LCD0-D15	LVDS1-V0N	SPI1-CLK/DBI-SCLK	UART3-RX				PD-EINT11
PD12		1/0	LCD0-D18	LVDS1-V1P	SPI1-MOSI/DBI-SDO	TWI0-SDA				PD-EINT12
PD13	12500 JD	I/O	LCD0-D19	LVDS1-V1N	SPI1-MISO/DBI-SDI/ DBI-TE/DBI-DCX	UART3-RTS	.05	") ⁽²⁾	PD-EINT13
PD14	NEO'S	I/O	LCD0-D20	LVDS1-V2P	SPI1-HOLD/DBI-DCX /DBI-WRX	UART3-CTS	Hillsogy		Neo.	PD-EINT14
PD15		I/O	LCD0-D21	LVDS1-V2N	SPI1-WP/DBI-TE	IR-RX	16			PD-EINT15
PD16		I/O	LCD0-D22	LVDS1-CKP	DMIC-DATA3	PWM0	ALG			PD-EINT16
PD17		1/0	LCD0-D23	LVDS1-CKN	DMIC-DATA2	PWM1	9-			PD-EINT17
PD18		1/0	LCD0-CLK	LVDS1-V3P	DMIC-DATA1	PWM2				PD-EINT18
PD19		1/0	LCD0-DE	LVDS1-V3N	DMIC-DATA0	PWM3				PD-EINT19
PD20		1/0	LCD0-HSYNC	TWI2-SCK	DMIC-CLK	PWM4				PD-EINT20
PD21	150500 10	1/0	LCD0=VSYNC	TWI2-SDA	UART1-TX	PWM5	Society	10	,5050 Jp	PD-EINT21
PD22		1/0	OWA-OUT	IR-RX	UART1-RX	PWM7	Ulfe	Ś	700	PD-EINT22
PEO		1/0	NCSIO-HSYNC	UART2-RTS	TWI1-SCK	LCD0-HSYNC			RGMII-RXCTRL /RMII-CRS-DV	PE-EINTO
PE1		1/0	NCSIO-VSYNC	UART2-CTS	TWI1-SDA	LCD0-VSYNC			RGMII-RXD0/ RMII-RXD0	PE-EINT1
PE2		1/0	NCSIO-PCLK	UART2-TX	TWI0-SCK	CLK-FANOUT0	UARTO-TX		RGMII-RXD1/ RMII-RXD1	PE-EINT2
PE3	.>>	1/0	NCSIO-MCLK	UART2-RX	TWI0-SDA	CLK-FANOUT1	UARTO-RX	10	RGMII-TXCK/ RMII-TXCK	PE-EINT3
PE4	GPIOE	1/0	NCSIO-DO	UARTA TX	TWI2-SCK	CLK-FANOUT2	D-JTAG-MS	R-JTAG-MS	RGMII-TXD0/ RMII-TXD0	PEREINT4
PE5		I/O	NCSI0-D1	UART4-RX	TWI2-SDA	LEDC-DO	D-JTAG-DI	R-JTAG-DI	RGMII-TXD1/ RMII-TXD1	PE-EINT5
PE6		1/0	NCSI0-D2	UART5-TX	TWI3-SCK	OWA-IN	D-JTAG-DO	R-JTAG-DO	RGMII-TXCTRL /RMII-TXEN	PE-EINT6
PE7		1/0	NCSI0-D3	UART5-RX	TWI3-SDA	OWA-OUT	D-JTAG-CK	R-JTAG-CK	RGMII-CLKIN/ RMII-RXER	PE-EINT7
PE8		1/0	NCSIO-D4	UART1-RTS	PWM2	UART3-TX			MDC	PE-EINT8
PE9		1/0	NCSI0-D5	UART1-CTS	PWM3	UART3-RX			MDIO	PE-EINT9



Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PE10		1/0	NCSIO-D6	UART1-TX	PWM4	IR-RX			EPHY-25M	PE-EINT10
PE11		1/0	NCSIO-D7	UART1-RX	I2SO-DOUT3	I2SO-DIN3			RGMII-TXD2	PE-EINT11
PE12		1/0	TWI2-SCK	NCSIO-FIELD	I2SO-DOUT2	I2SO-DIN2			RGMII-TXD3	PE-EINT12
PE13	10	1/0	TWI2-SDA	PWM5	I2SO-DOUTO	I2SO-DIN1	DMIC-DATA3	<i>1</i> 0	RGMII-RXD2	PE-EINT13
PE14	1150500 110	1/0	TW/1-SCK	D-JTAG-MS	I2SO-DOUT1	I2SO-DINO	DMIC-DATA2	· ·	RGMII-RXD3	PE-EINT14
PE15		1/0	TWI1-SDA	D-JTAG-DI	PWM6	I2SO-LRCK	DMIC-DATA1		RGMII-RXCK	PE-EINT15
PE16		1/0	TWI3-SCK	D-JTAG-DO	PWM7	I2SO-BCLK	DMIC-DATA0			PE-EINT16
PE17		1/0	TWI3-SDA	D-JTAG-CK	IR-TX	I2SO-MCLK	DMIC-CLK			PE-EINT17
PF0		I/O	SDC0-D1		R-JTAG-MS	I2S2-DOUT1	I2S2-DIN0			PF-EINTO
PF1		1/0	SDC0-D0		R-JTAG-DI	I2S2-DOUT0	12S2-DIN1			PF-EINT1
PF2		1/0	SDC0-CLK	UARTO-TX	TWI0-SCK	LEDC-DO	OWA-IN			PF-EINT2
PF3	GPIOF	I/O	SDC0-CMD		R-JTAG-DO	I2S2-BCLK				PF-EINT3
PF4	1150500 Jp	I/O	SDC0-D3	UARTO-RX	TWI0-SDA	PWM6	IR-TX	7	1180500 JD	PF-EINT4
PF5		1/0	SDC0-D2	Light	R-JTAG-CK	I2S2-LRCK	Lilli		,	PF-EINT5
PF6		1/0		OWA-OUT	IR-RX	I2S2-MCLK	PWM5	K		PF-EINT6
PG0		I/O	SDC1-CLK	UART3-TX	RGMII-RXCTRL/ RMII-CRS-DV	PWM7	Ne	d		PG-EINTO
PG1		I/O	SDC1-CMD	UART3-RX	RGMII-RXD0/ RMII-RXD0	PWM6				PG-EINT1
PG2		1/0	SDC1-D0	UART3-RTS	RGMII-RXD1/ RMII-RXD1	UART4-TX				PG-EINT2
PG3	180500 110	I/O	SDC1-D1	UART3-CT\$	RGMII-TXCK/ RMII-TXCK	UART4-RX	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	<i>"</i>	150 10 10 10 10 10 10 10 10 10 10 10 10 10	PG-EINT3
PG4	,	I/O	SDC1-D2	UART5-TX	RGMII-TXD0/ RMII-TXD0	PWM5	%	Ċ	S.	PG-EINT4
PG5		1/0	SDC1-D3	UART5-RX	RGMII-TXD1/ RMII-TXD1	PWM4				PG-EINT5
PG6		1/0	UART1-TX	TWI2-SCK	RGMII-TXD2	PWM1				PG-EINT6
PG7	GPIOG	1/0	UART1-RX	TWI2-SDA	RGMII-TXD3	OWA-IN				PG-EINT7
PG8		1/0	UART1-RTS	TWI1-SCK	RGMII-RXD2	UART3-TX				PG-EINT8
PG9		1/0	UART1-CTS	TWI1-SDA	RGMII-RXD3	UART3-RX				PG-EINT9
PG10	15050010	1/0	PWM3	TWI3-SCK	RGMII-RXCK	CLK-FANOUTØ	IR-RX	19	150500 JD	PG-EINT10
PG11		1/0	12S1-MCLK	TWI3-SDA	EPHY-25M	CLK-FANOUT1	TCON-TRIG	Ś	The same of the sa	PG-EINT11
PG12		I/O	I2S1-LRCK	TWI0-SCK	RGMII-TXCTRL/ RMII-TXEN	CLK-FANOUT2	PWM0	UART1-TX		PG-EINT12
PG13		I/O	I2S1-BCLK	TWI0-SDA	RGMII-CLKIN/ RMII-RXER	PWM2	LEDC-DO	UART1-RX		PG-EINT13
PG14		I/O	I2S1-DIN0	TWI2-SCK	MDC	I2S1-DOUT1	SPIO-WP	UART1-RTS		PG-EINT14
PG15		1/0	I2S1-DOUT0	TWI2-SDA	MDIO	I2S1-DIN1	SPIO-HOLD	UART1-CTS		PG-EINT15
PG16		1/0	IR-RX	TCON-TRIG	PWM5	CLK-FANOUT2	OWA-IN	LEDC-DO		PG-EINT16

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Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PG17		I/O	UART2-TX	TWI3-SCK	PWM7	CLK-FANOUT0	IR-TX	UARTO-TX		PG-EINT17
PG18		I/O	UART2-RX	TWI3-SDA	PWM6	CLK-FANOUT1	OWA-OUT	UARTO-RX		PG-EINT18

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HINE OF DE LANGE OF THE PARTY O	nulsos o lo	hillsoko lib	hillige go lip	Hills beat Ip	HIJE DE OO JID	HUISOSO JO	rulls beat lib	hillsogo lib
RIJISOSO NO	NIES SOND	CHISOSO NO	nulls of O Ib	hulls 6500 lb	Tullsos of It	NIII868O NO	RUISOSO NO	nulles oo lib
KINISO DE LA COLLEGA DE LA COL	nulsoso lo	hillsogo lib	hillige go lip	hillige go lip	KIIISOSOO JIO	Willson in	KINISO SO NO	NIIIEO O ID

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4.4 Detailed Signal Description

Table 4-4 shows the detailed function description of every signal based on the different interface.

- [1].Signal Name: The name of every signal.
- [2]. Description: The detailed function description of every signal.
- [3].Type: Denotes the signal direction:
 - I (Input),
 - O (Output),
 - I/O (Input/Output),
 - OD (Open-Drain),
 - A (Analog),
 - AI (Analog Input),
 - AO (Analog Output),
 - A I/O (Analog Input/Output)
 - P (Power),
 - G (Ground)

Table 4-4 Detailed Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
DRAM		
SA[15:0]	DRAM Address Signal to the Memory Device	0
SBA[2:0]	DRAM Bank Address Signal to the Memory Device	0
SCKE[1:0]	DRAM Clock Enable Signal to the Memory Device	0 0000
SCKN Pulle	DRAM Active-Low Clock Signal to the Memory Device	Orulls
SCKP	DRAM Active-High Clock Signal to the Memory Device	0
SCS[1:0]	DRAM Chip Select Signal to the Memory Device	0
SDQ[15:0]	DRAM Bidirectional Data line to the Memory Device	1/0
SDQM[1:0]	DRAM Data Mask Signal to the Memory Device	0
SDQS[1:0]N	DRAM Active-Low Bidirectional Data Strobes to the Memory Device	1/0
SDQS[1:0]P	DRAM Active-High Bidirectional Data Strobes to the	1/0

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Signal Name ^[1]	Description ^[2]	Type ^[3]
1150500	Memory Device	11/50500
SODT[1:0]	DRAM On-Die Termination Output Signal	O _{Vin}
SCAS	DRAM Column Address Strobe	0
SRAS	DRAM Row Address Strobe	0
SRST	DRAM Reset Signal to the Memory Device	0
SVREF	DRAM Reference Voltage	Р
SWE	DRAM Write Enable	0
SZQ	DRAM External Reference Resistor for Impedance Calibration	AI
VCC-DRAM	DRAM Power Supply	P UISOSOO
VDD18-DRAM	Power Supply for DRAM Controller	Р
System Control		
BOOT-SEL[1:0]	Boot Media Select	I
RESET	Reset Signal (low active)	I, OD
NMI	Non-maskable Interrupt	I/O, OD
TEST	Test Signal	I
FEL Jules 60 JD	Boot Select Jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process. For more details, see section 3.3 "BROM System" in the D1-H_User_Manual.	I rillseso jp
Clock		
X32KIN	Clock Input of 32.768 kHz Crystal	Al
X32KOUT	Clock Output of 32.768 kHz Crystal	AO
VCC-RTC	RTC Power	Р
VCC-PLL	PLL Power Supply	Р

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Signal Name[1] Description^[2] Type^[3] DCXO **REFCLK-OUT** Digital Compensated Crystal Oscillator Clock Fanout AO DXIN Digital Compensated Crystal Oscillator Input ΑI **DXOUT** Digital Compensated Crystal Oscillator Output ΑO VCC-DCXO Digital Compensated Crystal Oscillator Power **USB** USB0-DM A I/O **USB DRD Data Signal DM** USB0-DP USB DRD Data Signal DP A I/O USB1-DM A I/O USB HOST Data Signal DM USB1-DP USB HOST Data Signal DP A I/O **GPADC** General Purpose ADC Input Channel 0 GPADC0 ΑI GPADC1 General Purpose ADC Input Channel 1 ΑI **TPADC** TP-X1 Touch Panel X1 Input ΑI Touch Panel X2 Input TP-X2 ΑI TP-Y1 Touch Panel Y1 Input ΑI TP-Y2 Touch Panel Y2 Input **LRADC** ΑI **LRADC** Low Rate ADC **HDMI HCEC** 1/0 **HDMI Consumer Electronics Control** HHPD 1/0 HDMI Hot Plug Detection Signal **HSCL HDMI Serial Clock** 0

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Signal Name ^[1]	Description ^[2]	Type ^[3]
HSDA NECONO	HDMI Serial Data	1/01150500
HTXON	HDMI Negative TMDS Differential Line Driver Data0 Output	AO
НТХОР	HDMI Positive TMDS Differential Line Driver Data0 Output	AO
HTX1N	HDMI Negative TMDS Differential Line Driver Data1 Output	AO
HTX1P	HDMI Positive TMDS Differential Line Driver Data1 Output	AO
HTX2N	HDMI Negative TMDS Differential Line Driver Data2 Output	AO (80
HTX2P	HDMI Positive TMDS Differential Line Driver Data2 Output	AO
HTXCN	HDMI Negative TMDS Differential Line Driver Clock Output	AO
НТХСР	HDMI Positive TMDS Differential Line Driver Clock Output	AO
VCC-HDMI	HDMI Power	Р
CVBS OUT	/	
TVOUT0	TV CVBS Output	AO
VCC-TVOUT	TV CVBS DAC Power	P 1500 10
CVBS IN	Lin, Lin,	Light.
TVIN0	TV CVBS Input 0	Al
TVIN1	TV CVBS Input 1	Al
TVIN-VRP	TV CVBS ADC Positive Reference Voltage	Р
TVIN-VRN	TV CVBS ADC Negative Reference Voltage	Р
VCC-TVIN	TV CVBS ADC Power	Р
AUDIO CODEC	•	1



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Signal Name ^[1]	Description ^[2]	Type ^[3]
LINEOUTEN	Lineout Left Channel Negative Differential Output	AO _{JIE} SOO
LINEOUTLP	Lineout Left Channel Positive Differential Output	AO
LINEOUTRN	Lineout Right Channel Negative Differential Output	AO
LINEOUTRP	Lineout Right Channel Positive Differential Output	AO
HPOUTR	Headphone Right Output	AO
HPOUTL	Headphone Light Output	AO
HPOUTFB	Pseudo Differential Headphone Ground Reference	Al
HPVCC	Headphone Power 1.8 V	Р
MICIN1P	Microphone Differential Positive Input 1	Al
MICIN1N	Microphone Differential Negative Input 1	AIRU
MICIN2P	Microphone Differential Positive Input 2	Al
MICIN2N	Microphone Differential Negative Input 2	Al
MICIN3P	Microphone Differential Positive Input 3	Al
MICIN3N	Microphone Differential Negative Input 3	Al
FMINR	FMIN Right Input	Al
FMINL	FMIN Left Input	Al
LINEINR 50%	LINEIN Right Single-End Input	AI 🔊
LINEINL	LINEIN Left Single-End Input	Akille
HP-DET	Headphone Jack Detect	Al
HPLDO	Headphone LDO 1.8 V (bonding with HPVCC)	Р
HPLDOIN	Headphone LDO Input 3.3 V	Р
VDD33	Analog Power 3.3 V	Р
ALDO	Analog Power 1.8 V (bonding with AVCC)	Р
HBIAS	Second Bias Voltage Output for Headset Microphone	AO

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Signal Name^[1] Description^[2] Type[3] First Bias Voltage Output for Main Microphone **MBIAS** MIC-DET Headphone MIC Detect ΑI VRA1 Internal Reference Voltage ΑO VRA2 ΑO Internal Reference Voltage **AVCC** Power Supply for Analog Part G AGND **Analog Ground** LCD LCD0-D[23:0] LCD Data Output 0 LCD Clock LCD0-CLK The pixel data are synchronized by this clock LCD Vertical Sync LCD0-VSYNC 0 It indicates one new frame LCD Horizontal Sync LCD0-HSYNC 0 It indicates one new scan line LCD0-DE 0 LCD Data Output Enable **TCON-TRIG** LCD Sync (TCON outputs to LCD for sync) 0 **LVDS** LVDS0-CKP LVDS0 Positive Port of Clock 0 LVDS0-CKN LVDS0 Negative Port of Clock LVDS0-V[3:0]P 0 LVDS0 Positive Port of Data Channel [3:0] LVDS0-V[3:0]N LVDSO Negative Port of Data Channel [3:0] 0 LVDS1-CKP LVDS1 Positive Port of Clock 0 0 LVDS1-CKN LVDS1 Negative Port of Clock 0 LVDS1-V[3:0]P LVDS1 Positive Port of Data Channel [3:0] LVDS1-V[3:0]N LVDS1 Negative Port of Data Channel [3:0] 0

Type^[3]

1/0

0

I/O

0

I/O, OD



Signal Name[1]

DSI-D[3:0]P

DSI

Description^[2]

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DSI Differential Data [3:0] Negative Signal 0 DSI-D[3:0]N DSI-CKP 0 DSI Differential Clock Positive Signal DSI-CKN DSI Differential Clock Negative Signal O Parallel CSI NCSIO-PCLK Parallel CSI Pixel Clock NCSIO-MCLK Parallel CSI Master Clock 0 NCSIO-HSYNC Parallel CSI Horizontal Synchronous NCSIO-VSYNC Parallel CSI Vertical Synchronous NCSI0-D[7:0] Parallel CSI Data Bit NCSIO-FIELD Parallel CSI Field Index SMHC SDC0-CMD Command Signal for SD Card I/O, OD SDC0-CLK Clock for SD Card O Data Input and Output for SD Card 1/0 SDC0-D[3:0] Command Signal for SDIO WIFI SDC1-CMD I/O, OD % Clock for SDIO WIFI SDC1-CLK

DSI Differential Data [3:0] Positive Signal

JII80800 JD

SDC1-D[3:0]

SDC2-CMD

SDC2-CLK

I2S/PCM

12SO-MCLK

SDC2-D[3:0]

Data Input and Output for SDIO WIFI

Data Input and Output for eMMC

Command Signal for eMMC

Clock for eMMC

12SO Master Clock

Type^[3]

0



Signal Name^[1]

12SO-LRCK

Description^[2]

12S0/PCM0 Sample Rate Clock/Sync

771180500 JD

12SO-BCLK 12SO/PCM0 Bit Rate Clock 1/0 12S0-DOUT[3:0] I2SO/PCM0 Serial Data Output Channel [3:0] 0 12S0-DIN[3:0] I2SO/PCM0 Serial Data Input Channel [3:0] **I2S1-MCLK** O **I2S1 Master Clock I2S1-LRCK** I2S1/PCM1 Sample Rate Clock/Sync 1/0 I2S1-BCLK 1/0 I2S1/PCM1 Bit Rate Clock I2S1-DOUT[1:0] I2S1/PCM1 Serial Data Output Channel [1:0] 0 12S1-DIN[1:0] I2S1/PCM1 Serial Data Input Channel [1:0] 12S2-MCLK **12S2 Master Clock** 0 12S2-LRCK I2S2/PCM2 Sample Rate Clock/Sync 1/0 12S2-BCLK I2S2/PCM2 Bit Rate Clock 1/0 12S2-DOUT[3:0] 12S2/PCM2 Serial Data Output Channel [3:0] 0 I2S2/PCM2 Serial Data Input Channel [3:0] I2S2-DIN[3:0] **DMIC**

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DMIC-CLK

DMIC-DATA[3:0]

EMAC RGMII-RXD3 **RGMII Receive Data3** RGMII-RXD2 **RGMII Receive Data2** RGMII-RXD1/RMII-RXD1 RGMII/RMII Receive Data1 RGMII-RXD0/RMII-RXD0 RGMII/RMII Receive Data0 ı **RGMII-RXCK RGMII Receive Clock** RGMII-RXCTRL/ RGMII Receive Control/RMII Carrier Sense Receive Data Valid RMII-CRS-DV

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Digital Microphone Clock Output

Digital Microphone Data Input



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Signal Name ^[1]	Description ^[2]	Type ^[3]
RGMII-CLKIN/RMII-RXER	RGMII Transmit Clock from External/RMII Receive Error	1 11150500
RGMII-TXD3	RGMII Transmit Data3	0
RGMII-TXD2	RGMII Transmit Data2	0
RGMII-TXD1/RMII-TXD1	RGMII/RMII Transmit Data1	0
RGMII-TXD0/RMII-TXD0	RGMII/RMII Transmit Data0	0
RGMII-TXCK/RMII-TXCK	RGMII/RMII Transmit Clock	
	For RGMII, IO type is output;	1/0
	For RMII, IO type is input	
RGMII-TXCTRL/	RGMII Transmit Control/RMII Transmit Enable	0 00
RMII-TXEN	IIIE CONTROL CONTROL TRANSMIT ENABLES	11130500
MDC	RGMII/RMII Management Data Clock	0
MDIO	RGMII/RMII Management Data Input/Output	1/0
EPHY-25M	25 MHz Output for EMAC PHY	0
OWA		
OWA-IN	One Wire Audio Input	I
OWA-OUT	One Wire Audio Output	0
LEDC		
LEDC-DO	Intelligent Control LED Signal Output	0 150500 110
Interrupt	Little Little	Lilly,
PB-EINT[12:0]	GPIO B Interrupt	I
PC-EINT[7:0]	GPIO C Interrupt	I
PD-EINT[22:0]	GPIO D Interrupt	1
PE-EINT[17:0]	GPIO E Interrupt	I
PF-EINT[6:0]	GPIO F Interrupt	I
PG-EINT[18:0]	GPIO G Interrupt	1



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Signal Name^[1] Type[3] Description^[2] **CIR Receiver** IR-RX Consumer Infrared Receiver **CIR Transmitter Consumer Infrared Transmitter** 0 IR-TX **PWM** 1/0 PWM[7:0] Pulse Width Modulation Output Channel [7:0] SPI&SPI_DBI SPIO-CS SPIO Chip Select Signal, Low Active 1/0 SPIO Clock Signal SPIO-CLK Provides serial interface timing. SPI0-MOSI SPIO Master Data Out, Slave Data In 1/0 SPIO Master Data In, Slave Data Out 1/0 SPIO-MISO SPIO Write Protect, Low Active Protects the memory area against all program or erase SPIO-WP instructions. 1/0 It also can be used for serial data input and output for SPI Quad Input or Quad Output mode. SPIO Hold Signal Pauses any serial communication with the device SPIO-HOLD without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode. SPI1-CS 1/0 SPI1 Chip Select Signal, Low Active SPI1 Clock Signal 1/0 SPI1-CLK Provides serial interface timing. SPI1 Master Data Out, Slave Data In SPI1-MOSI 1/0 SPI1-MISO SPI1 Master Data In, Slave Data Out 1/0 SPI1-WP 1/0 SPI1 Write Protect, Low Active

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Type[3]



Signal Name[1]

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SPI Quad Input or Quad Output mode. SPI1 Hold Signal Pauses any serial communication with the device SPI1-HOLD 1/0 without resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode. DBI-CSX Chip Select Signal, Low Active 1/0 **DBI-SCLK** Serial Clock Signal 1/0 DBI-SDO Data Output Signal I/O **Data Input Signal** DBI-SDI 1/0 The data is sampled on the rising edge and the falling edge **Tearing Effect Input** DBI-TE 1/0 It is used to capture the external TE signal edge. The rising and falling edge is configurable. DCX pin is the select output signal of data and command. **DBI-DCX** 1/0 DCX = 0: register command; DCX \neq 1: data or parameter. When DBI operates in dual data lane format, the 1/0 **DBI-WRX** RGB666 format 2 can use WRX to transfer data **UART**

Protects the memory area against all program or erase

It also can be used for serial data input and output for

Description^[2]

instructions.

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UARTO-TX

UARTO-RX

UART1-TX

UART1-RX

UART1-CTS

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UARTO Data Transmit

UARTO Data Receive

UART1 Data Transmit

UART1 Data Receive

UART1 Data Clear to Send

0



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Signal Name^[1] Description^[2] Type^[3] UART1-RTS **UART1** Data Request to Send **UART2-TX UART2 Data Transmit** UART2-RX **UART2** Data Receive **UART2-CTS** UART2 Data Clear to Send ı **UART2-RTS UART2** Data Request to Send O 0 **UART3-TX UART3 Data Transmit UART3-RX UART3 Data Receive** UART3 Data Clear to Send **UART3-CTS** UART3-RTS UART3 Data Request to Send UART4-TX **UART4 Data Transmit** 0 UART4-RX **UART4** Data Receive UART5-TX **UART5 Data Transmit** 0 **UART5-RX UART5 Data Receive** TWI TWI0-SCK TWIO Serial Clock Signal 1/0 TWIO Serial Data Signal 1/0 TWI0-SDA TWI1-SCK TWI1 Serial Clock Signal 1/0 1/0 TWI1-SDA TWI1 Serial Data Signal TWI2-SCK TWI2 Serial Clock Signal 1/0 TWI2-SDA TWI2 Serial Data Signal 1/0 TWI3-SCK 1/0 TWI3 Serial Clock Signal TWI3-SDA I/O TWI3 Serial Data Signal **JTAG D-JTAG-MS** DSP JTAG Mode Select ı

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Signal Name ^[1]	Description ^[2]	Type ^[3]
D-JTAG-CK	DSP JTAG Clock Signal	1 11150500
D-JTAG-DO	DSP JTAG Data Output	0
D-JTAG-DI	DSP JTAG Data Input	I
R-JTAG-MS	RISC-V JTAG Mode Select	I
R-JTAG-CK	RISC-V JTAG Clock Signal	I
R-JTAG-DO	RISC-V JTAG Data Output	0
R-JTAG-DI	RISC-V JTAG Data Input	I

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5 Electrical Characteristics

5.1 Parameter Conditions

5.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at Ta = 25 °C and Ta = Ta max.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical Values

Unless otherwise specified, the typical data are based on Ta = 25 °C. They are given only as design guidelines.

5.1.3 Temperature Definitions

- Ambient Temperature— the temperature of the surrounding environment.
- Junction Temperature— the hottest temperature of the silicon chip inside the package.
- Absolute Maximum Junction Temperature— the temperature beyond which damage occurs to the device.
 The device may not function or meet expected performance at this temperature.
- Recommended Operating Temperature— the junction temperature at which the device operates
 continuously at the designated performance over the designed lifetime. The reliability of the device may
 be degraded if the device operates above this temperature. Some devices will not function electrically
 above this temperature.

5.2 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings.



Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.3, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

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Table 5-1 Absolute Maximum Ratings

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Symbol	Parameter CHESTON CHES	Min ⁽¹⁾	Max ⁽¹⁾	Unit
AVCC	Power Supply for Analog Part	-0.3	TBD	V
HPVCC	Headphone Power	-0.3	TBD	V
VCC-PC	Digital GPIO C Power	-0.3	3.96	V
VCC-PD	Digital GPIO D Power	-0.3	3.96	V
VCC-PE	Digital GPIO E Power	-0.3	3.96	V
VCC-PF	Digital GPIO F Power	-0.3	3.96	V
VCC-PG	Digital GPIO G Power	-0.3	3.96	V
VCC-IO	Power Supply for 3.3 V Digital Part	-0.3	3.96	V
VCC-RTC	Power Supply for RTC	-0.3	TBD	V
VCC-PLL	Power Supply for System PLL	-0.3	TBD	V
VCC-LVDS	Power Supply for LVDS	-0.3	TBD	V
VCC-TVIN	Power Supply for CVBS IN	-0.3	TBD	V
VCC-TVOUT	Power Supply for CVBS OUT	-0.3	TBD	V
VCC-HDMI	Power Supply for HDMI	-0.3	TBD	V
VCC-DRAM	Power Supply for DRAM IO and DDR2/DDR3	-0.3	TBD	V
VDD18-DRAM	Power Supply for DRAM Controller	-0.3	TBD	V
VCC-EFUSE	Power Supply for EFUSE Program Mode	-0.3	TBD	V
VCC-DCXO	Power Supply for DCXO	-0.3	TBD	V
VDD-CPU	Power Supply for CPU	-0.3	TBD	V
VDD-SYS	Power Supply for System	-0.3	TBD	V
LDO-IN	Internal LDOA/B Input Voltage	-0.3	3.96	V
LDOA-OUT	Internal LDOA Output Voltage for Analog Device and IO	-0.3	2.16	V
LDOB-OUT	Internal LDOB Output Voltage for VCC-DRAM	-0.3	2.16	V

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71180800 JC

Symbol	Parameter	Min ⁽¹⁾	Max ⁽¹⁾	Unit	
T _{STG}	Storage Temperat	-40	150 150	°C	
Tj	Working Junction	-20	125	°C	
.,	Electrostatic Discharge ⁽²⁾	Human Body Model(HBM) ⁽³⁾	-2000	2000	V
V _{ESD}		Charged Device Model(CDM) ⁽⁴⁾	-250	250	V
I _{Latch-up}	Latch-up I-test per on each IO pin ⁽⁵⁾		TBD		
	Latch-up over-volt on each IO pin ⁽⁶⁾	TBD			

- (1) The min/max voltages of power rails are guaranteed by design, not tested in production.
- (2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.
- (3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.
- (4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.
- (5) Based on JESD78E; each device is tested with IO pin injection of ±200 mA at room temperature.
- (6) Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

5.3 Recommended Operating Conditions

Table 5-2 describes operating conditions of the D1-H.





Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2 Recommended Operating Conditions

Symbol	Parameter	Min	Тур	Max	Unit
Ta VCC-DRAM uses extern Ambient Operating Tem	Ambient Operating Temperature (when VCC-DRAM uses external power)	-25	-	85	°C
	Ambient Operating Temperature (when VCC-DRAM uses internal LDO)	-25	-	85	°C

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Unit **Symbol Parameter** Min Тур Max TBD49 Working Junction Temperature Range -20 °C Τj ٧ **AVCC** Power Supply for Analog Part 1.782 1.8 1.818 ٧ **HPVCC Headphone Power** 1.782 1.8 1.818 Digital GPIO C Power ٧ VCC-PC 1.62 1.8 1.98 1.8 V voltage 3.3 3.3 V voltage 2.97 3.63 Digital GPIO D Power VCC-PD 1.8 V voltage 1.62 1.8 1.98 ٧ 2.97 3.63 3.3 V voltage 3.3 Digital GPIO E Power 1.62¹ 1.8 1.98 1.8 V voltage VCC-PE 3.08 2.52 2.8 2.8 V voltage 3.3 V voltage 2.97 3.3 3.63 Digital GPIO F Power VCC-PF 1.8 V voltage 1.62 1.8 1.98 3.3 V voltage 2.97 3.3 3.63 Digital GPIO G Power VCC-PG ٧ 1.8 V voltage 1.8 1.98 1.62 3.3 V voltage 2.97 3.3 3.63 Power Supply for Digital Part 2.97₁₁₁₈05 VCC-IO 3.3 3.63 ٧ 3.3 V voltage ٧ VCC-RTC TBD 1.8 **TBD** Power Supply for RTC VCC-PLL Power Supply for System PLL **TBD** 1.8 **TBD** ٧ TBD ٧ VCC-LVDS Power Supply for LVDS TBD 1.8 TBD ٧ **VCC-TVIN** Power Supply for CVBS IN TBD 1.8 3.3 TBD ٧ VCC-TVOUT Power Supply for CVBS OUT TBD ٧ VCC-HDMI Power Supply for HDMI TBD 1.8 **TBD**

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Symbol	Parameter	Min	Тур	Max	Unit
VCC-DRAM	Power Supply for DRAM IO and DDR2	1.7 NIISOSOO	1.8	1.9,0500	V
VCC-DIVAIVI	Power Supply for DRAM IO and DDR3	1.425	1.5	1.575	V
VDD18-DRAM	Power Supply for DRAM Controller	1.7	1.8	1.95	V
VCC-EFUSE	Power Supply for EFUSE Program Mode	TBD	1.8	TBD	V
VCC-DCXO	Power Supply for DCXO	TBD	1.8	TBD	V
VDD-CPU	Power Supply for CPU	TBD	0.9(2)	TBD	V
VDD-SYS	Power Supply for System	TBD	0.9	TBD	V
LDO-IN	Internal LDOA/B Input Voltage	2.4	3.3	3.6	V
LDOA-OUTO 100	Internal LDOA Output Voltage for Analog Device and 10	1.782	1.8	1.81800,00	V
LDOB-OUT	Internal LDOB Output Voltage for VCC-DRAM	1.31 1.455	1.35 ⁽³⁾ 1.5	1.39 1.545	V
	1.746	1.8	1.854		

- (1). The chip junction temperature in normal working condition should be less than or equal to the maximum junction temperature in Table 5-2.
- (2). The voltage and frequency are related. For more details on voltage requirements, see the CPU_AP_Note.pdf.
- (3). The default voltage of LDOB-OUT is 1.35 V.

5.4 Power Consumption Parameters

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in the following table.



Since the data presented in the following table is based on empirical measurements on small sample size, the results presented are not guaranteed.

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Table 5-3 Power Consumption Parameters

Parameter	Sub Parameter	Power Supply	Condition	Тур	Max	Unit
Internal CPU		VDD-CPU	1.0 V,@1.5 GHz, 2 memtester	-	TBD	mA
Core Power	SYS	VDD-SYS	0.9 V	-	TBD	mA
		VCC-IO	For GPIO, voltage 3.3 V, N=13	-	78	mA
		VCC-PC	For GPIO, voltage 3.3 V, N=8		48	mA
GPIO Power		VCC-PD	For GPIO, voltage 3.3 V, N=23	-	138	mA
GFIO FOWEI		VCC-PE	For GPIO, voltage 3.3 V, N=18	-	108	mA
	10	VCC-PF	For GPIO, voltage 3.3 V, N=7	10	42	mA
nulleo soci)/	VCC-PG	For GPIO, voltage 3.3 V, N=19	-16	114500	mA
Memory I/C		VCC-DRAM	DDR3, 792 MHz, 1.5 V, 2 memtester	Ne	TBD	mA
LVDS Power		VCC-LVDS	1.8 V, 700 MHz dual link	-	50	mA
HDMI Powe	r	VCC-HDMI	1.8 V, 4K@30fps		35	mA
24 MHz Oscillator	z Crystal	VCC-PLL	1.8 V	-	2	mA
RTC Power	100	VCC-RTC	1.8 V	-	0.01	mA
ADC Analog Power AVCC		1.8 V, 48 kHz sample rate, 5-chs are enabled	99	TBD //	mA	
DAC Analog Power AVCC		1.8 V, 48 kHz sample rate, 2-chs are enabled	-	TBD	mA	
USB Power		VCC-IO	2 x USB, 3.3 V	-	35	mA

General equation for estimated, maximum power consumption of an group IO power supply:

 $Imax = N \times 6 mA$

Where:

N—Number of IO pins supplied by the power line.

The maximum power consumption for each IO is 6 mA.

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DC Electrical Characteristics

Table 5-4 summarizes the DC electrical characteristics of the D1-H. For the interfaces of GPIQ function port, refer to the DC parameters in Table 5-4 unless otherwise stated.

Table 5-4 DC Electrical Characteristics

(VCC-IO/VCC-PC/VCC-PD/VCC-PE/VCC-PF/VCC-PG)

Symbol	Parameter		Min	Тур	Max	Unit
V _{IH}	High-Level Input Vol	tage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V _{IL}	Low-Level Input Volt	age	-0.3	-	0.3 * VCC-IO	V
		PC3 to PC7, PF3, PF6	12	15	18	kΩ
R _{PU}	Input Pull-up Resistance	PG0 to PG5	26	33	40	kΩ
ے	65.	Other GPIOs	80	100	120	kΩ
Ulliso	Ulleg	PC3 to PC7, PF3, PF6	12 rullsosoc	15	18	kΩ (VIIISO)
R _{PD}	Input Pull-down Resistance	PG0 to PG5	26	33	40	kΩ
		Other GPIOs	80	100	120	kΩ
I _{IH}	High-Level Input Cur	rent		-	10	uA
III	Low-Level Input Cur	rent	-	-	10	uA
V _{OH}	High-Level Output V	oltage	VCC-IO - 0.3	-	VCC-IO	V
V _{OL}	Low-Level Output Voltage		0	-	0.2	V
l _{OZ}	Tri-State Output Leakage Current		-10	1/0	10	uA
CIN RUITEOE	Input Capacitance		- 11150505	-	5/150500	pF NIIISOE
Соит	Output Capacitance	•	-	-	5	pF

SDIO Electrical Characteristics 5.6

The SDIO electrical parameters are related to different supply voltage.

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Figure 5-1 SDIO Voltage Waveform



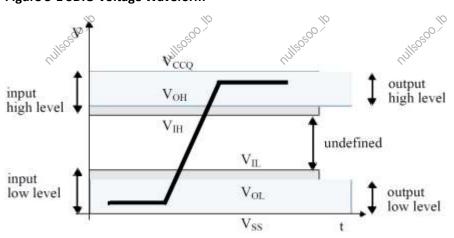


Table 5-5 shows 3.3 V SDIO electrical parameters.

Table 5-5 3.3 V SDIO Electrical Parameters

Symbol	Parameter Parame	Min	Type	Max _{[i][SOSOO}	Unit
VDD	Power voltage	2.7	BAL	3.6	V
V _{CCQ}	I/O voltage	2.7		3.6	V
V _{OH}	Output high-level voltage	0.75 * V _{CCQ}	-	-	V
Vol	Output low-level voltage		-	0.125 * V _{CCQ}	V
V _{IH}	Input high-level voltage	0.625 * V _{CCQ}	-	V _{CCQ} + 0.3	V
V _{IL}	Input low-level voltage	V _{SS} - 0.3	-	0.25 * V _{CCQ}	V

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Table 5-6 shows 1.8 V SDIO electrical parameters.

Ta

able 5-6 1.8 V	SDIO	Electrical Parameters	
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Symbol	Parameter	Min	Тур	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V _{CCQ}	I/O voltage	1.7		1.95	V
V _{OH}	Output high-level voltage	V _{CCQ} - 0.45	-	-	V
V _{OL}	Output low-level voltage	-	-	0.45	V
V _{IH}	Input high-level voltage	0.625 * V _{CCQ} ⁽¹⁾	-	V _{CCQ} + 0.3	V
V _{IL}	Input low-level voltage	V _{SS} – 0.3	- %	0.35 * V _{CCQ} (2)	V



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Symbol	Parameter	Min	Тур	Max	Unit
null's	or MMC4.3 or lower.	Willege OO	hills 6200	Lillso soo	<

5.7 GPADC Electrical Characteristics

The GPADC contains a 2-ch analog-to-digital (ADC) converter. The GPADC is a type of successive approximation register (SAR) converter. Table 5-7 lists GPADC electrical characteristics.

Table 5-7 GPADC Electrical Characteristics

Parameter	Min	Тур	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale input Range	0 ,115050	- ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	AVCC	, Moo
Quantizing Error	-	8	NG	LSB
Clock Frequency	-	1 1 1	1	MHz
Conversion Time	1 VA	14	-	ADC Clock Cycles

5.8 LRADC Electrical Characteristics

The LRADC is 6-bit resolution ADC for key application. The LRADC can work up to 2 kHz conversion rate. Table 5-8 lists LRADC electrical characteristics.

Table 5-8 LRADC Electrical Characteristics

10	10		10	1/0
Parameter	Min Ullsocoo	Typ UIISOSO	Max	Unit
ADC Resolution	-	6	-	bits
Full-scale Input Range	0	-	LEVELB ⁽¹⁾	V
Quantizing Error	-	2	-	LSB
Clock Frequency	-	-	2	kHz
Conversion Time	-	6	-	ADC Clock Cycles

⁽¹⁾ The maximum value of LEVELB is 1.266 V. For details, see the register description of LRADC in D1-H_User_Manual.

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Audio Codec Electrical Characteristics

VDD-SYS = 0.9 V, AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, ADC fs = 16 kHz, Input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 5-9 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit		
	DAC to HPOUTL or HPOUTR							
	Full-scale	OdBFS 1 kHz	-	540	-	Vrms		
	SNR (A-weighted)	Odata	-	95	-	dB		
	THD+N	OdBFS 1 kHz	-	-85	-	dB		
DAC Path	Crosstalk Rulle	R_OdB_L_Odata 1 kHz L_OdB_R_Odata 1 kHz	- 6	TBD	0,10	dB		
DAC Path	DAC to LINEOUTLP	/N or LINEOUTRP/N						
	Full-scale	OdBFS 1 kHz	-	1.1	-	Vrms		
	SNR (A-weighted)	Odata	-	100	-	dB		
	THD+N	OdBFS 1 kHz	-	-88	-	dB		
	Crosstalk	R_0dB_L_0data 1 kHz L_0dB_R_0data 1 kHz	-	-105	-	dB		
	LINEINLR via ADC							
rule of oc	Output Level	1.7 Vpp, 1 kHz	-	875	0 <u>,</u> %	mFFS		
Lo	SNR (A-weighted)	0 Vpp	-	94	-	dB		
	THD+N	1.7 Vpp, 1 kHz	-	-88	-	dB		
ADC Path	FMINLR via ADC							
	Output Level	1.7 Vpp, 1 kHz	-	875	-	mFFS		
	SNR (A-weighted)	0 Vpp	-	94	-	dB		
	THD+N	1.7 Vpp, 1 kHz	-	-88	-	dB		
	MICIN via ADC							



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Symbol	Parameter N	Test Conditions	Min	Тур	Max	Unit
nulsosof.	Output Level	, mesoo ; mesoo ;	-	880	<u>-</u>	mFFS
	SNR (A-weighted)	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1 kHz, 0 dB Gain	-	98	-	dB
	THD+N	1 Kill, 6 dB Gaill	-	-90	-	dB
	Output Level		-	880	-	mFFS
	SNR (A-weighted)	MICP=1.695Vpp/2, MICN=1.695Vpp/2, 1 kHz, 6 dB Gain	-	97	-	dB
	THD+N	1 Kill, 6 dB Gaill	-	-93	-	dB
	Output Level		-	880	-	mFFS
	SNR (A-weighted)	MICP=0.788Vpp/2, MICN=0.788Vpp/2, 1 kHz,12 dB Gain	-	94		dB
hillsosog	THD+N	MICP=0.392Vpp/2, MICN=0.392Vpp/2, 1 kHz, 18 dB Gain	-	-85	20/10	dB
RIJI,	Output Level		-	880	-	mFFS
	SNR (A-weighted)			92	-	dB
	THD+N		-	-83	-	dB
	Output Level		-	880	-	mFFS
	SNR (A-weighted)	MICP=0.197Vpp/2, MICN=0.197Vpp/2, 1 kHz,24 dB Gain	-	87	-	dB
	THD+N	T KIIZ,Z4 GB GGIII	-	-80	-	dB
	Output Level		-	880	-	mFFS
00	SNR (A-weighted)	MICP=0.101Vpp/2, MICN=0.101Vpp/2,	-	82	0-10	dB
ruleoso	THD+N	1 kHz,30 dB Gain of the little	-	-73 ⁵⁰⁵	-	dB
	Output Level		-	880	-	mFFS
	SNR (A-weighted)	MICP=0.053Vpp/2, MICN=0.053Vpp/2, 1 kHz,36 dB Gain	-	76	-	dB
	THD+N	1 K12,30 GD Gaill	-	-65	-	dB
	Current	-	-	2.0	-	mA
MBIAS	Voltage	-	1.8	2.0	2.55	V
	Noise	20 Hz—20 kHz	-	3	-	uV



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Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
nills 05 OC	Current	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	ı	2.0	<u> </u>	mA
HBIAS	Voltage	-	1.8	2.0	2.55	٧
	Noise	20 Hz—20 kHz	-	TBD	-	uV

5.10 External Clock Source Characteristics

5.10.1 High-speed Crystal/Ceramic Resonator Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator (oscillation mode). The 24 MHz crystal resonator provides 24 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 5-10 High-speed 24 MHz Crystal Circuit Characteristics

Symbol	Parameter III Pa	Min NIIISOS	Тур	Max	Unit
f _{X24M_IN}	Crystal parallel resonance frequency		24		MHz
	Crystal frequency stability and tolerance at 25 °C $^{(1)}$	-50		+50	ppm
	Oscillation mode	Fundamenta	al		-
C ₀	Shunt capacitance (2)	-	6.5	-	pF

- 1. The 50 ppm frequency stability and tolerance can meet the requirement of D1-H. We recommend selecting 20 ppm crystal devices. If the REFCLK-OUT (24 MHz fanout) is used for Wi-Fi chip, the crystal uses the recommended specification or the specified model for Wi-Fi chip.
- 2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C₀) is given by the crystal manufacturer.

Table 5-11 Crystal Circuit Parameters

Symbol	Parameter				
C ₁	C ₁ capacitance				
C ₂	C ₂ capacitance				
CL	Equivalent load capacitance, specified by the crystal manufacturer				
C ₀	Crystal shunt capacitance, specified by the crystal manufacturer				
C _{shunt}	Total shunt capacitance				

30 J



Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C₁, C₂, and C_{shunt}.

The total load capacitance is $C_L = [(C_1 * C_2)/(C_1 + C_2)] + C_{shunt}$.

- C₁ and C₂ represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. C₁ and C₂ are usually the same size.
- C_{shunt} is the crystal shunt capacitance (C₀) plus any mutual capacitance (C_{pkg} + C_{PCB}) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.





For the above capacitances of 24 MHz crystal circuit, refer to the capacitance recommended in the D1-H Schematic Diagram.

5.10.2 Low-speed Crystal/Ceramic Resonator Characteristics

The D1-H contains an RC oscillation circuit that generates a 32.768 kHz clock, meanwhile, the DCXO module can calibrate the RC oscillation circuit regularly. If the product does not have a high requirement for the accuracy of the system clock, the external 32.768 kHz crystal circuit can be omitted and the internal RC oscillation circuit can be adopted, meanwhile, the relevant clock configuration needs to be turned on by the software.



The D1-H also can connect to a 32.768 kHz crystal resonator (oscillation mode). The 32.768 kHz crystal resonator provides 32.768 kHz reference clock which is connected to the X32KIN and X32KOUT terminals. In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

Table 5-12 Low-speed 32.768 kHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Тур	Max	Unit
f _{X32K_IN}	Crystal parallel resonance frequency	-	32.768	-	kHz
	Crystal frequency stability and tolerance at 25 °C ⁽¹⁾	-	-	-	ppm
	Oscillation mode	Fundamental			-

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Symbol	14	Parameter	1/0	Min	Тур	Max	Unit
C ₀	2500/	Shunt capacitance (2)	ull ² 0500	- ullsos	1.1	- 11150500	pF

- The D1-H has no requirement for the frequency stability and tolerance of 32.768 kHz crystal. If the actual product has requirement for the accuracy of timing function, the 20 ppm stability and tolerance is recommended.
- The 1.1 pF is only a simulation value. The crystal shunt capacitance (C₀) is given by the crystal manufacturer.



For capacitances of 32.768 kHz crystal circuit, refer to the capacitance recommended in the D1-H_Schematic_Diagram.

Internal Reset Electrical Characteristics

Table 5-13 Internal Reset Electrical Characteristics

Parameter	Test Condition	Min	Тур	Max	Unit
Power-on threshold voltage of VDD-SYS on which the reset signal is excited	Ta= -20°C to 85°C	-	0.4	i	V
Reset active timeout period	Ta= -20°C to 85°C	1	64	-	ms
Reset open-drain output voltage	Ta= -20°C to 85°C, pull up 3.3 V	-0.3	-	0.3*VCC	V

External Memory Electrical Characteristics 5.12

5.12.1 SMHC AC Electrical Characteristics

5.12.1.1 HS-SDR Mode



IO voltage is 1.8 V or 3.3 V.

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Figure 5-2 SMHC HS-SDR Mode Output Timing Diagram



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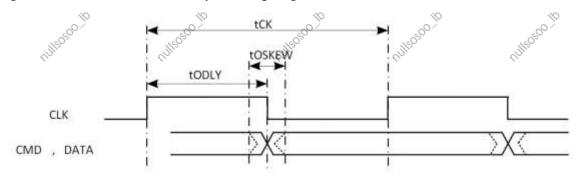


Table 5-14 SMHC HS-SDR Mode Output Timing Constants

Symbol	Min	Тур	Max	Unit				
СІК								
tCK	0	50	50	MHz				
DC _{III} EOEO	45 _{NI} IISOSO	50 _{NIII} EO ^{EO}	55 _{NUII} 305	%				
ferenced to CLK)		4 0	AP.					
tODLY	- 1	0.25	0.5	UI				
tOSKEW	0.5	-	0.8	ns				
	tCK DC DC DC Terenced to CLK) tODLY	tCK 0 DC, Websel 45 NIBERS TO THE TODLY -	tCK 0 50 DC_IIIS 50 45IIIS 50 ferenced to CLK) tODLY - 0.25	tCK 0 50 50 50 50 DC_NIEDED 50 55 RAILED 50 TODLY - 0.25 0.5				



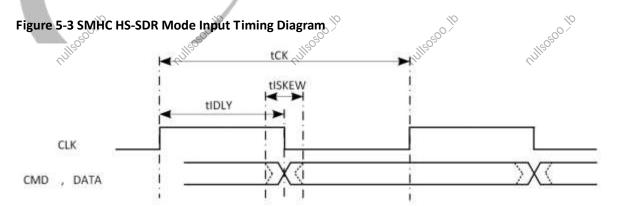


Table 5-15 SMHC HS-SDR Mode Input Timing Constants

(2). The driver strength level of GPIO is 2 for test.

Parameter	Symbol	Min	Тур	Max	Unit



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Parameter	Symbol	Min	Тур	Max	Unit
CTK UNIPOSOO	CIN 50500 /	01150500	aull ^s osoo /	auli ^g os	9/
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(refer	enced to CLK 50 N	ЛНz)			
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	-	ns
Data input skew time in SDR mode	tiskew	0.5 NIIEOSOO JE	- RIHEGEOD	0.8	ns

(1). The driver strength level of GPIO is 2 for test.

5.12.1.2 HS-DDR Mode

Figure 5-4 SMHC HS-DDR Mode Output Timing Diagram

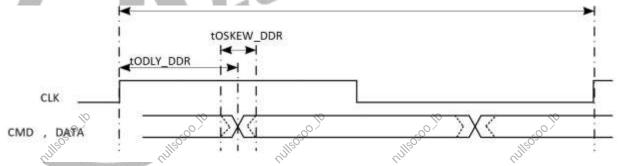


Table 5-16 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Тур	Мах	Unit			
СІК								
Clock frequency	tCK	0	50	50	MHz			
Duty cycle	DC	45	50	55	%			
Output CMD, DATA(referenced to CLK)								
CMD, Data output	tODLY_DDR	-	0.25	0.25	UI %			





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Parameter	Symbol	Min	Тур	Max	Unit
delay time in DDR mode	hillsosoo ,	nillsosoo ,	hills0800	Rullege	SO /
Data output delay skew time	tOSKEW_DDR	0.5	-	0.8	ns

- (1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz.
- (2). The driver strength level of GPIO is 2 for test.

Figure 5-5 SMHC HS-DDR Mode Input Timing Diagram

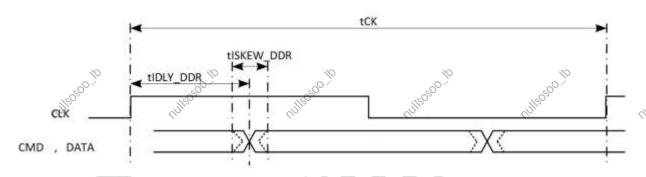


Table 5-17 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Тур	Max	Unit	
CLK		1				
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Input CMD, DATA (referenced to CLK 50 MHz)						
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	-	ns	
Data input skew time in DDR mode	tISKEW_DDR	0.5	-	0.8	ns	
(1). The driver strength	n level of GPIO is 2	for test.	ı	1	1	

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5.12.1.3 HS200 Mode

CMD , DATA

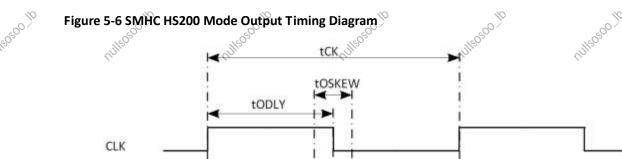


Table 5-18 SMHC HS200 Mode Output Timing Constants

Parameter	Symbol	Min	Тур	Max	Unit
CLK	o lib	, W	,%		10
Clock frequency	tCKIIISOSO	0 111150500	- Rullsosod	150 _{[NI] 8} 05	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA (re	ferenced to CLK)	44	Ma		
CMD, Data output delay time	tODLY	LV	0.25	0.5	UI
Data output delay skew time	tOSKEW	0.5	-	0.8	ns

(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.

(2). The driver strength level of GPIO is 3 for test.



Figure 5-7 SMHC HS200 Mode Input Timing Diagram

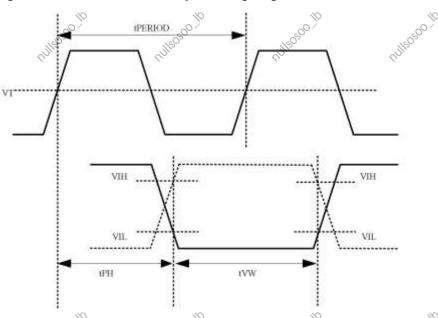


Table 5-19 SMHC HS200 Mode Input Timing Constants

Parameter	Symbol	Min	Тур	Max	Unit	Remark		
CLK	CLK							
Clock period	tPERIOD	6.66		-	ns	Max: 150 MHz		
Duty cycle	DC	45	50	55	%			
Rise time, fall time	tTLH, tTHL	-/	-	0.2	UI			
Input CMD, DATA	referenced to C	LK)	2500/10	2500/10		20010		
Input delay	tPH RUMB	0		2 Rulls	UI RIII			
Input delay variation due to temperature change after tuning	dPH	-350 ^[3]	-	1550 ^[4]	ps			
CMD, Data valid window	tVW	0.575	-	-	UI			

- (1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.
- (2). The driver strength level of GPIO is 3 for test.

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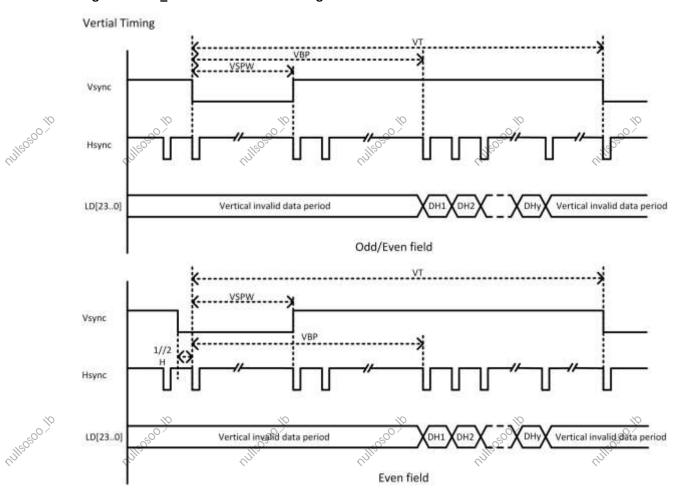


Parameter	Symbol	Min	Тур	Max	Unit	Remark	
(3). Temperature v	11/503		IIIEGEOO	hillso soo	hills	1500	JIIISOS

5.13 External Peripheral Electrical Characteristics

5.13.1 LCD AC Electrical Characteristics

Figure 5-8 HV_IF Interface Vertical Timing



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Figure 5-9 HV_IF Interface Horizontal Timing

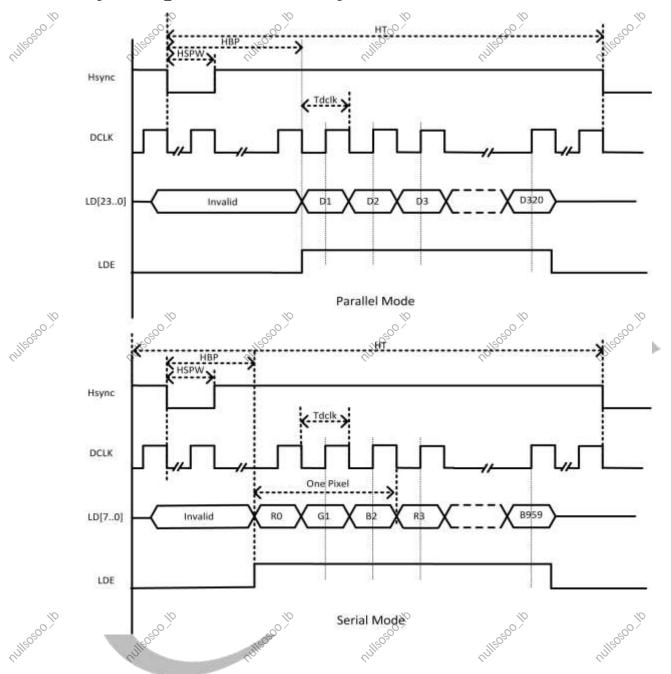


Table 5-20 LCD HV_IF Interface Timing Constants

Parameter	Symbol	Min	Тур	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
Hsync period time	tHT	-	HT+1	-	tDCLK
Hsync width	tHSPW	-	HSPW+1	-	tDCLK
Hsync back porch	tHBP	-	HBP+1	-	tDCLK
Vsync period time	tVT	-	VT/2	- 10	tHT

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Parameter	Symbol	Min	Тур	Max	Unit
Vsync width Wsync with the work of the winds of the winds of the work of the w	tVSPW NIIBOSOO	- Ollisc	VSPW+1	- UIISOSOO	tHT
Vsync back porch	tVBP	-	VBP+1	-	tHT

(1) Vsync: Vertical sync, indicates one new frame.

(2) Hsync: Horizontal sync, indicates one new scan line.

(3) DCLK: Dot clock, pixel data are sync by this clock.

(4) LDE: LCD data enable.

(5) LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.

5.13.2 CSI AC Electrical Characteristics

PCLK

DATA

Pigure 5-10 CSI Data Sample Timing

toperiod

thigh-level

tdst

tdhd

Table 5-21 CSI Interface Timing Constants

Parameter	Symbol	Min	Тур	Max	Unit
Pclk period	tperiod	6.73	-	- 10	ns
Pclk frequency	1/tperiod	² 000,	- [1]	148.5	MHz
Pclk duty	t _{high-level} /t _{period}	40	50	60	%
Data input setup time	t _{dst}	0.6	-	-	ns
Data input hold time	t _{dhd}	0.6	-	-	ns





5.13.3 EMAC AC Electrical Characteristics

5.13.3.1 RGMII

Figure 5-11 RGMII Interface Transmit Timing

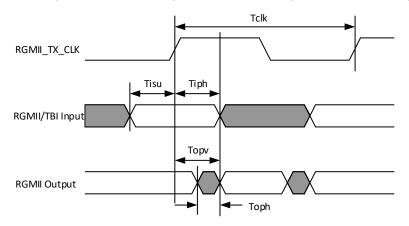


Table 5-22 RGMII Transmit Timing Constants

Parameter	Symbol	Min	Тур	Max	Unit
RGMII_TX_CLK clock period	Tclk	8		DC	ns
RGMII/TBI input setup prior to RGMII_TX_CLK	Tisu	2.8	-	-	ns
RGMII/TBI input data hold after RGMII_TX_CLK	Tiph	0.1	-	-	ns
RGMII output data valid after RGMII_TX_CLK	Торv	-	-	0.85	ns
RGMII output data hold after RGMII_TX_CLK	Toph	0	-	-	ns

Figure 5-12 RGMII Interface Receive Timing

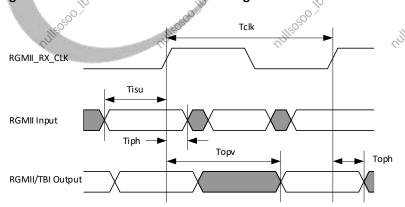


Table 5-23 RGMII Receive Timing Constants

Parameter		Symbol	Min	Тур	Max	Unit
99	10	10	10		10	
0 /	0 /	0 /	0 /		0 /	

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Parameter	Symbol	Min	Тур	Max	Unit
RGMII_RX_CLK clock period	Telk Ullso	<u></u>	-	DC DC	ns
RGMII input setup prior to RGMII_RX_CLK	Tisu	2.6	-	1	ns
RGMII input data hold after RGMII_RX_CLK	Tiph	0.8	1	-	ns
RGMII/TBI input data valid after RGMII_RX_CLK	Торv	-	-	5.2	ns
RGMII output data hold after RGMII_RX_CLK TBI output data hold after RGMII_RX_CLK	Toph	0.1 0.5	-	-	ns

5.13.3.2 RMII





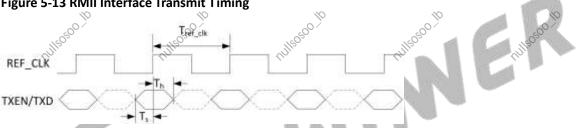


Table 5-24 RMII Transmit Timing Constants

Parameter	Symbol	Min	Тур	Max	Unit
Reference clock period	T _{ref_clk}	-	20	-	ns
TXD/TXEN to REF_CLK setup time	Ts	4	-	-	ns
TXD/TXEN to REF_CLK hold time	Th 000	2 %	-	- 0/10	ns

Figure 5-14 RMII Interface Receive Timing

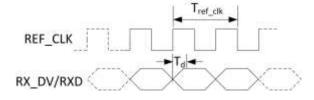


Table 5-25 RMII Receive Timing Constants

|--|

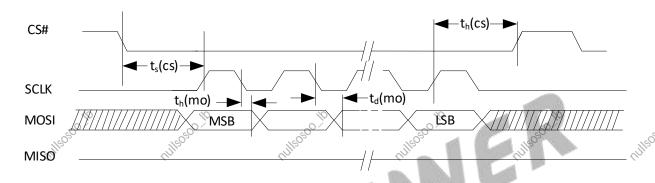


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Parameter	Symbol	Min	Тур	Max	Unit
Reference clock period	Tref_clk_llsos	500/	20	500/	ns
REF_CLK rising edge to RX_DV/RXD	Td	-	10	12	ns

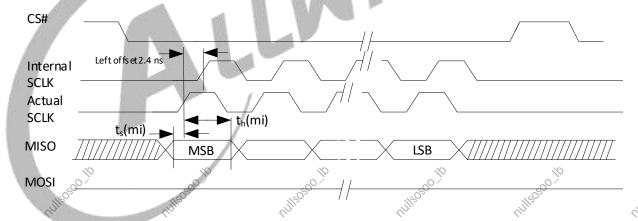
5.13.4 SPI AC Electrical Characteristics

Figure 5-15 SPI Writing Timing



U1180500 110

Figure 5-16 SPI Reading Timing



KIII50500 JD

Table 5-26 SPI Timing Constants

Parameter	Symbol	Min	Тур	Max	Unit
CS# active setup time	t _s (cs)	-	2T ⁽¹⁾	-	ns
CS# active hold time	t _h (cs)	-	2T ⁽¹⁾	-	ns
Data output delay time	t _d (mo)	-	T ⁽¹⁾ /2-3	-	ns
Data output hold time	t _h (mo)	-	T ⁽¹⁾ /2-3	-	ns
Data input setup time	t _s (mi)	0.2	-	-	ns

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Parameter	10	Symbol	Min	Тур	Max	Unit
Data input hold time	nills0500/	t _h (mi)	0.2	-	JIISOSOO /	ns

(1).T is the cycle of clock.

5.13.5 SPI_DBI AC Electrical Characteristics

Figure 5-17 DBI 3-line Serial Interface Timing

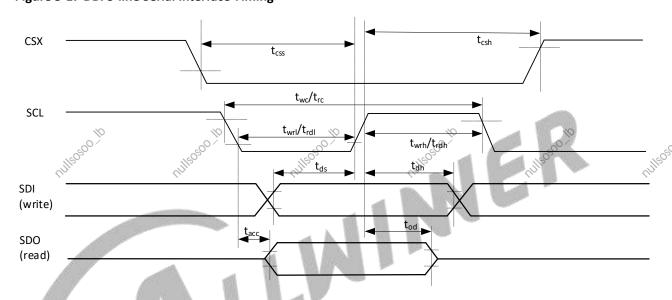


Table 5-27 DBI 3-line Serial Interface Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time (Write)	t _{css}	15		ns
100	Chip select setup time (Read)	t csh	60%	00/10	ns
Unite of s	Write cycle Rules Rullson	t _{wc}	16	Ullege	ns
SCL (write)	Control pulse "H" duration	t _{wrh}	7		ns
	Control pulse "L" duration	t _{wrl}	7		ns
	Read cycle	t _{rc}	150		ns
SCL (read)	Control pulse "H" duration	t _{rdh}	60		ns
	Control pulse "L" duration	t _{rd1}	60		ns
SDI/SDO	Data setup time	t _{ds}	7		ns
(write)	Data hold time	t _{dt}	7	10	ns

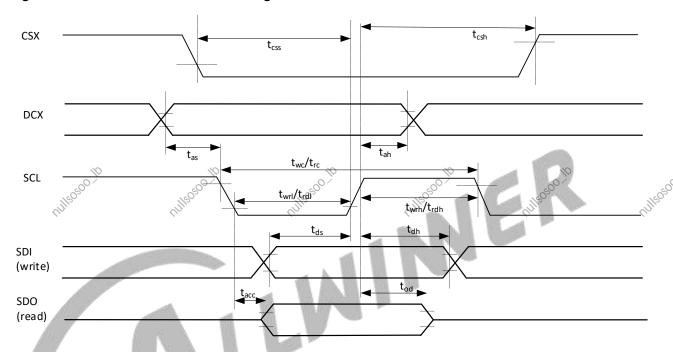
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Signal	Parameter	Symbol	Min	Max	Unit
SDI/SDQ	Read access time	tracc	10	50 150500	ns
(read)	Output disable time	t _{od}	15	50	ns

Figure 5-18 DBI 4-line Serial Interface Timing



NIII50500 ×

Table 5-28 DBI 4-line Serial Interface Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time (Write)	t _{css}	15		ns
CSX	Chip select setup time (Read)	t _{csh}	60	1150500 110	ns
DCX	Address setup time	t _{as}	10	City.	ns
BEX	Address hold time (Write/Read)	t _{ah}	10		ns
661	Write cycle	t _{wc}	16		ns
SCL (write)	Control pulse "H" duration	t _{wrh}	7		ns
,	Control pulse "L" duration	t _{wr} ı	7		ns
SCL	Read cycle	t _{rc}	150		ns
(read)	Control pulse "H" duration	t _{rdh}	60		ns

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Signal	Parameter	Symbol	Min	Max	Unit
21/150500	Control pulse "E" duration	t _{rdl}	₃ 60	211180800	ns
SDI/SDO	Data setup time	t _{ds}	7		ns
(write)	Data hold time	t _{dt}	7		ns
SDI/SDO	Read access time	t _{racc}	-	50	ns
(read)	Output disable time	t _{od}	15	50	ns

5.13.6 UART AC Electrical Characteristics

Figure 5-19 UART RX Timing

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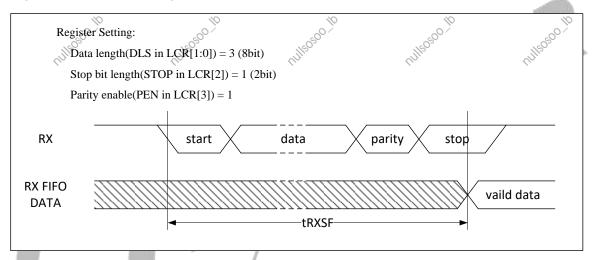
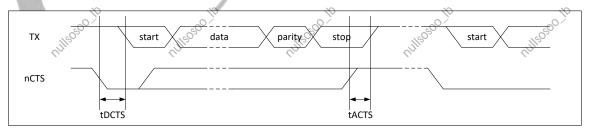


Figure 5-20 UART nCTS Timing





UIII80800 JY



Figure 5-21 UART nRTS Timing



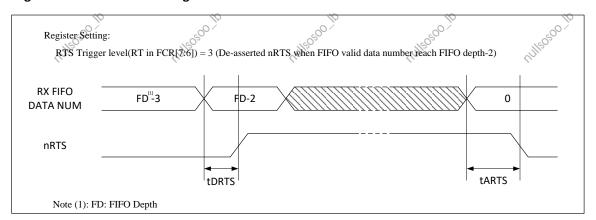


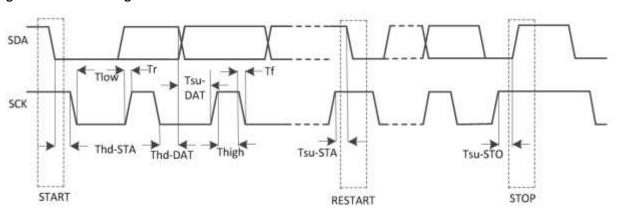
Table 5-29 UART Timing Constants

U1180800 JY

Parameter	Symbol	Min	Тур	Max	Unit
RX start to RX FIFO	tRXSF	10.5 * BRP ⁽¹⁾	30300	11 * BRP ⁽¹⁾	ns
Delay time of de-asserted nCTS to TX start	tDCTS		R	BRP ⁽¹⁾	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP ⁽¹⁾ /4		-	ns
Delay time of de-asserted nRTS	tDRTS		-	BRP ⁽¹⁾	ns
Delay time of asserted nRTS	tARTS	-	-	BRP ⁽¹⁾	ns
(1). BRP: Baud-Rate Period.					

5.13.7 TWI AC Electrical Characteristics

Figure 5-22 TWI Timing



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Table 5-30 TWI Timing Parameters

UIII80800 JD

Parameter	Symbol	Standard m	ode (150500)	Fast mode	1150500 110	Unit
Un.	rillo rull	Min	Max	Min	Max	Ċ.
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in Start	Tsu-STA	4.7	-	0.6	-	us
Hold time in Start	Thd-STA	4.0	-	0.6	-	us
Setup time in Data	Tsu-DAT	250	-	100	-	ns
Hold time in Data	Thd-DAT	5.0	-	-	-	ns
Setup time in Stop	Tsu-STO	4.0	-	6.0	-	us
SCK low level time	Tlow	4.70	-	1.3	- 00/0	us
SCK high level time	Thigh !!!!	4.0	- Ulleg	0.6	Tills	ns d
SCK/SDA falling time	Tf	- 41	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

W1180800 110

5.13.8 I2S/PCM AC Electrical Characteristics

Figure 5-23 I2S/PCM Timing in Master Mode



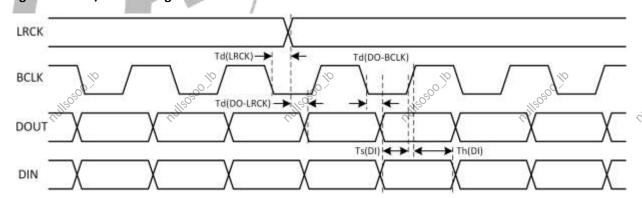


Table 5-31 I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Тур	Max	Unit
LRCK delay	T _d (LRCK)	-	-	10	ns
LRCK to DOUT delay (For LJF)	T _d (DO-LRCK)	-	-	10	ns

112000 JP

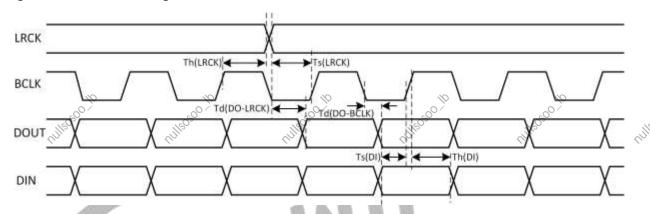
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UIII80800 JD

BCLK to DOUT delay	T _d (DO-BCLK)	-	- 10	10	ns
DIN setup	T _s (DI)	4	50°	- 01/150500 ×	ns
DIN hold	T _h (DI)	4	-	-	ns
BCLK rise time	Tr	-	-	8	ns
BCLK fall time	T _f	-	-	8	ns

Figure 5-24 I2S/PCM Timing in Slave Mode



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Table 5-32 I2S/PCM Timing Constants in Slave Mode

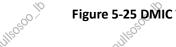
Parameter	Symbol	Min	Тур	Max	Unit
LRCK setup	T _s (LRCK)	4	-	-	ns
LRCK hold	T _h (LRCK)	4	-	-	ns
LRCK to DOUT delay (For LJF)	T _d (DO-LRCK)	- 3	Q-	10	ns
BCLK to DOUT delay	T _d (DO-BCLK) _[1]	- Villega	-	10150500	ns
DIN setup	T _s (DI)	4	-	-	ns
DIN hold	T _h (DI)	4	-	-	ns
BCLK rise time	Tr	-	-	4	ns
BCLK fall time	Tf	-	-	4	ns

KIII50500 JD

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5.13.9 **DMIC AC Electrical Characteristics**



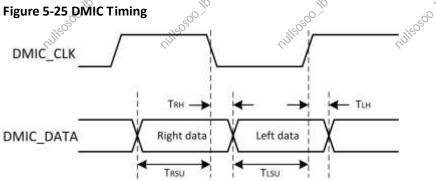


Table 5-33 DMIC Timing Constants

Parameter	Symbol	Min	Тур	Max	Unit
DMIC_DATA (Right) setup time to falling edge of DMIC_CLK	TRSU !!	15	<u>.</u>	11808010	ns
DMIC_DATA (Right) hold time from falling edge of DMIC_CLK	TRH	0		R	ns
DMIC_DATA (Left) setup time to rising edge of DMIC_CLK	TLSU	15	-	-	ns
DMIC_DATA (Left) hold time from rising edge of DMIC_CLK	TLH	0	-	-	ns

5.13.10 OWA AC Electrical Characteristics

Figure 5-26 OWA Timing

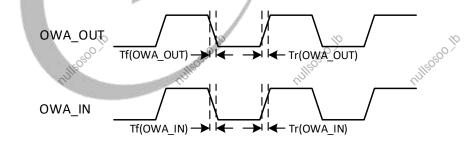


Table 5-34 OWA Timing Constants

Parameter	Symbol	Min	Тур	Max	Unit
OWA_OUT rise time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT fall time	Tf(OWA_OUT)	-	-	8	ns
OWA_IN rise time	Tr(OWA_IN)	-	-	4	ns

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Parameter	10	Symbol	Min	Тур	Max	Unit
OWA_IN fall time	11150500	Tf(QWA_IN)	- ₁₁₁₅ 0500	-	4,1150500	ns

5.13.11 CIR_RX AC Electrical Characteristics

Figure 5-27 CIR_RX Timing

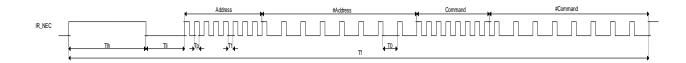


Table 5-35 CIR_RX Timing Constants

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Parameter	Symbol	Min	Тур	Max	Unit
Frame period	Tf (ill)	- rulls	67.5	III	ms
Lead code high time	Tlh	-	9	-	ms
Lead code low time	П	-	4.5	-	ms
Pulse time	Тр	-	560	-	us
Logical 1 low time	T1	-	1680	-	us
Logical 0 low time	то	-	560	-	us

5.14 Power-On and Power-Off Sequence

5.14.1 Power-On Sequence

Figure 5-28 shows an example of the power-on sequence for the D1-H device. The description of the power-on sequence is as follows.

- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90–110% of their nominal voltage, unless stated otherwise.
- VCC-RTC must be ramped no later than other power rails.
- VCC-IO must be ramped before VDD-SYS and VDD-CPU with a minimum delay of 2 ms.
- VCC-DRAM needs be stable before SDRAM driver initialization.
- During the entire power on sequence, the RESET signal must be held on low until all other power rails (except 24 MHz CLK) are stable for more than 64 ms.
- 24 MHz clock starts oscillating after the RESET signal is released.

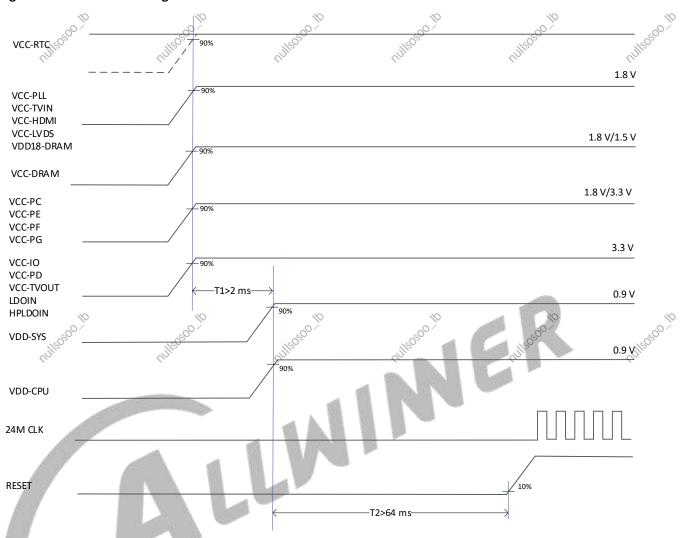
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Power-Off Sequence 5.14.2

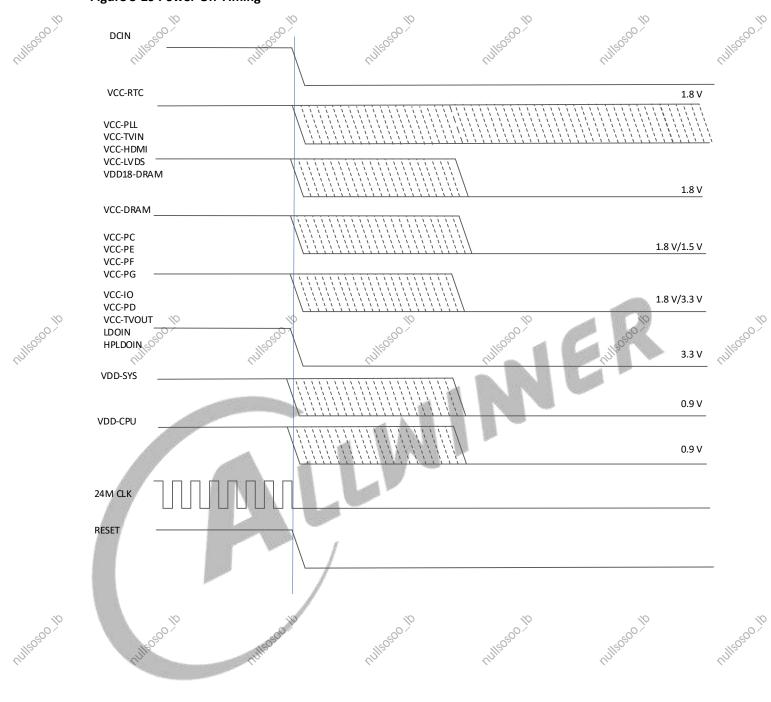
The power-off requirements are as follows.

After the RESET signal goes low, the 24 MHz clock starts to stop oscillating.

No special restrictions for other power rails.



Figure 5-29 Power-Off Timing







6 Package Thermal Characteristics

The maximum chip junction temperature (T_J max) must never exceed the values given in *Table 5-2* Recommended Operating Conditions.

The maximum chip-junction temperature T_J max, in degrees Celsius, may be calculated using the following equation:

 $T_1 \max = T_a \max + (P_D \max x \theta_{JA})$

Where:

T_a max is the maximum ambient temperature in °C.

P_D max is the maximum power dissipation.

 θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.

°C/W = degrees Celsius per watt.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following table shows the thermal resistance characteristics of the D1-H. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 6-1 D1-H Package Thermal Characteristics

Symbol	Parameter	Min	Typ ⁽¹⁾	Max	Unit
OJA PUTEOS	Junction-to-Ambient Thermal Resistance	- hillsos	TBD	- UIII202	°C/W
θ _{ЈВ}	Junction-to-Board Thermal Resistance	-	TBD	-	°C/W
θις	Junction-to-Case Thermal Resistance	1	TBD	-	°C/W

1. Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.

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7 Pin Assignment

7.1 Pin Map

The co h

For D1-H, LFBGA 337 balls, 13 mm x 13 mm package is offered. The following figure shows the pin map of the D1-H.

Figure 7-1 D1-H Pin Map

TP-82 USB1-08 HP-DET LINEOUTL PSS #61 PG5 poe 800 USBO-DE TF-YI DRADIC VKAL USEL-DN SPADES VRA2 PG00 PFR PFS 255 PGU PIGER 254 VCC-RG PGS4 9617 MICHON TVOUTE HESTO PCI **PC0** VCC-0F PCS PISS5 1911 PE12. P810 OIND CM GND HTX25 PCE VDID-SY HTX2F REFELE HTRIN X32KIN **X32KOUT** ABAD 100 131433 -OND HTXCF OND PERF LEICHN OND. (GND) IMO GND GNO POIN ROSET OND 1019 PELL POZE 169 PEIG OND P013 PDIZ P96 #E8 PELI PELI SWE MEM SCE1 P09 P67 765 3813 sport. CONTRACT OF FIR SDQ1 SAZ 3414 102 PED 5003 58A0 545 5004 5007 50/050F 1000 5002 SCKEO SBAI 546 5410 5A1 SALT P00

711180800 110

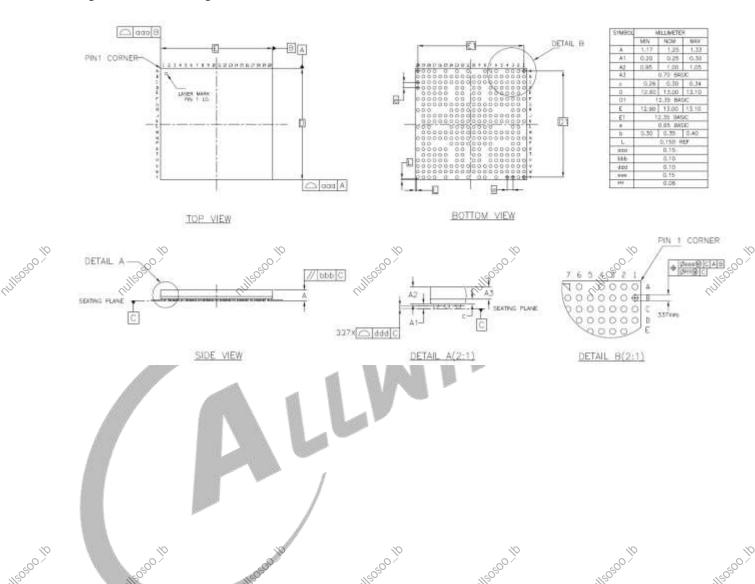
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7.2 Package Dimension

Figure 7-2 shows the top, bottom, and side views of D1-H package dimension.

Figure 7-2 D1-H Package Dimension







Carrier, Storage and Baking Information

8.1

8.1.1 **Matrix Tray Information**

Table 8-1 shows the D1-H matrix tray carrier information.

Table 8-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315 mm x 136 mm x 7.62 mm	119 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	Rullsoo
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

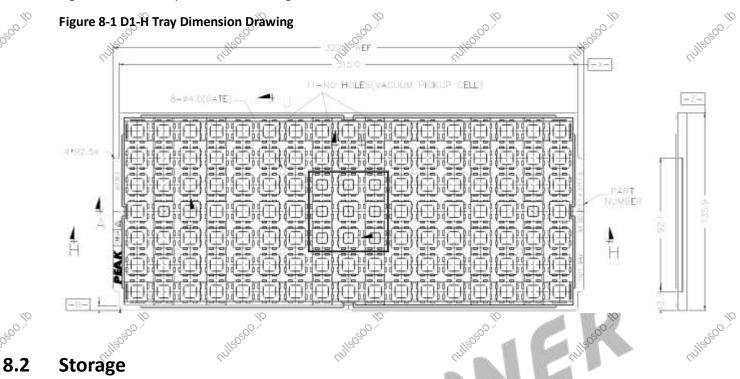
Table 8-2 shows the D1-H packing quantity.

Table 8-2 D1-H Packing Quantity Information

Sample	Size (mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
D1-H	13 x 13	119	10	1190	6	7140



Figure 8-1 shows tray dimension drawing of the D1-H.



Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

8.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 8-3 defines all MSL.



The D1-H device samples are classified as MSL3.

Table 8-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH

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UIII80800 JD

MSL	<i>%</i>	Out-of-bag floor life	Comments
5	allsosoo?	48 hours Night College	≤30°C / 60%RH
5a		24 hours	≤30°C / 60%RH
6		Time on Label (TOL)	≤30°C / 60%RH

8.2.2 Bagged Storage Conditions

Table 8-4 defines the shelf life of the D1-H device samples.

Table 8-4 Bagged Storage Conditions

Packing mode	Vacuum packing	
Storage temperature	20–26°C	10
Storage humidity	40%-60%RH NINGSON RUITE CONTROL RUITE	hills0500
Shelf life	12 months	



8.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of the D1-H is as follows.

Table 8-5 Out-of-bag Duration

Storage temperature	20–26°C
Storage humidity	40%–60%RH
Moisture sensitive level (MSL)	3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Floor life NIII	168 hours rulls rulls rulls



For no mention of storage rules in this document, refer to the latest *IPC/JEDEC J-STD-020C*.

8.3 Baking

It is not necessary to bake the D1-H if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded. It is necessary to bake the D1-H if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.



It is necessary to bake the D1-H if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to a risk of deformation.

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9 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

Figure 9-1 shows the appropriate reflow profile.

Figure 9-1 Lead-free Reflow Profile

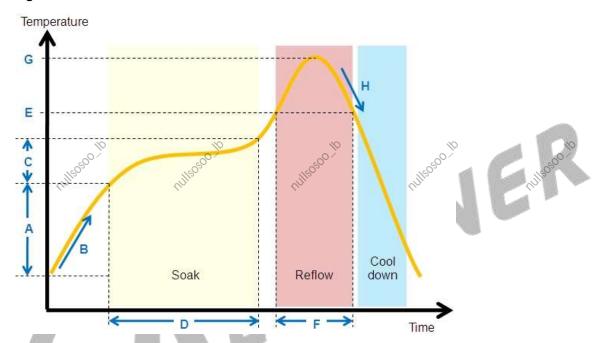


Table 9-1 Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions(for reference only)	
V 0	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
Α	Preheat ramp up temperature range	25°C -> 150°C
В	Preheat ramp up rate	1.5~2.5 °C/sec
С	Soak temperature range	150°C -> 190°C
D	Soak time	80–110 sec
Е	Liquidus temperature	217°C
F	Time above liquidus	60–90 sec

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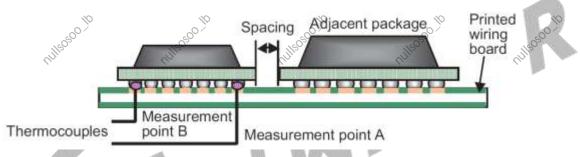
70	QTI typical SMT reflow profile conditions(for reference only)	
Julis0500 Jr	Step CO	Reflow condition
G	Peak temperature	240–250°C
Н	Cool down temperature rate	≤4°C/sec

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

Figure 9-2 Measuring the Reflow Soldering Process







To measure the temperature of the QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.



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10 FT/QA/QC Test

10.1 FT Test

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FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.

10.2 QA Test

QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.

10.3 QC Test 📎

QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.



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Part Marking

Figure 11-1 shows the D1-H marking.

Figure 11-1 D1-H Marking

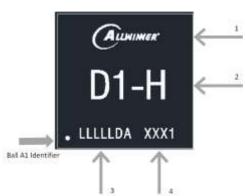


Table 11-1 describes the D1-H marking definitions.

Table 11-1 D1-H Marking Definitions



Marking Description Fixed/Dynamic No. **ALLWINNER** 1 Allwinner logo or name Fixed 2 D1-H Product name Fixed LLLLLAA Lot number 3 Dynamic XXX1 Date code Dynamic

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