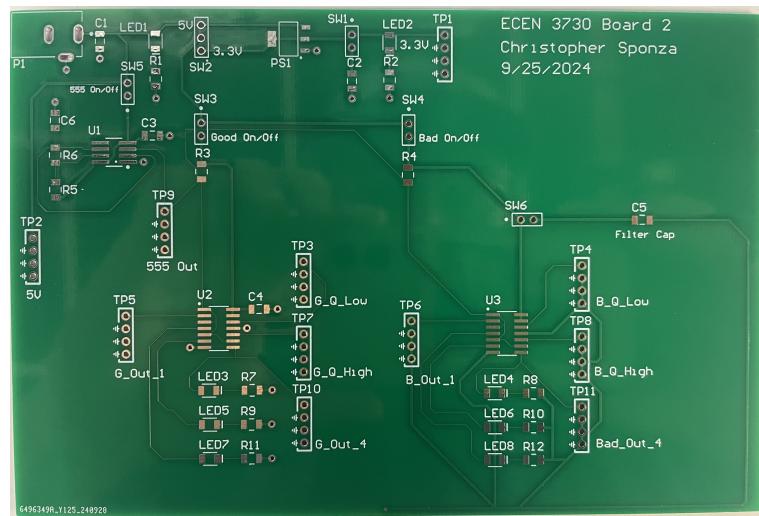


ECEN 3730 Board 2

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October 19, 2024



1 Plan of Record

1.0.1 Introduction

The purpose of this board is to demonstrate how choices in board layout can influence the switching noise and overall quality of a PCB. This board utilizes a 555-timer to provide a $\approx 500\text{Hz}$ square wave to one of two hex inverter circuits. One of these circuits will demonstrate ideal design choices including a decoupling capacitor and a continuous ground plane and the other will have a decoupling capacitor that can be isolated as well as a common return path for all signals and no ground plane.

1.1 "Back-of-Napkin" Sketch

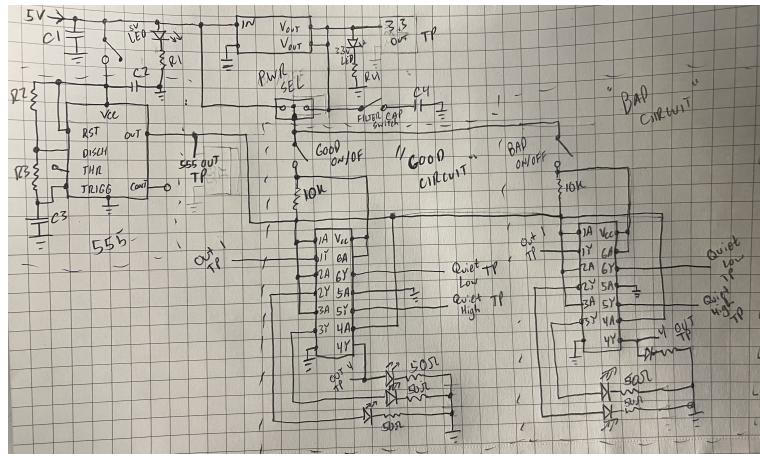


Figure 1: "Back-of-Napkin Sketch"

1.1.1 Engineering Specifications

The following were the specifications that were required to be met in order for the board to "work":

- Provide either 5V or 3.3V to the hex inverter circuits.
- Provide a switch to isolate the filter capacitor of the 3.3V LDO.
- Produce a $\approx 500\text{Hz}$ square with a 50-70% duty cycle.
- Be able to switch between supplying power to the "good" hex inverter circuit or the "bad".
- Provide test points for the 5V rail, 3.3V rail, 555 Timer Output, and the outputs of two inverters as well as the quiet high and low outputs of both hex inverter circuits.

1.2 Bill of Materials

Part	Value	Quantity
NE555DR (555 Timer)	-	1
74HC14D (Hex Inverter)	-	2
AMS1117-3.3 (LDO)	-	1
Resistor	$1K\Omega$	4
-	$10K\Omega$	2
-	47Ω	1
Capacitor	$1\mu F$	1
-	$22\mu F$	5
LED (Red)	-	8
10x Probe TP	-	11
Power Jack (Barrel)	-	1
2-Pin Header (Switch)	-	5
3-Pin Header (Switch)	-	1

1.3 Datasheets

- **555 Timer:** [555 Datasheet](#)
- **Hex Inverter:** [Hex Inverter Datasheet](#)
- **LDO:** [LDO Datasheet](#)

1.4 Milestones

The following are the main design milestones to reach the final product in chronological order:

- Define the engineering specifications
- "Back-of-Napkin" Sketch
- Complete schematic and PCB design in Altium
- Critical Design Review (CDR)
- Board Assembly and Bring-Up
- Testing and accumulation of results

1.5 Testing Plan

- Measure 5V and 3.3V output from barrel switch and LDO (With and without the filter capacitor)
- Measure 555 Timer Output

- Supply power to the "good" hex inverter circuit and measure the outputs of the first and fourth hex inverter as well as the quiet high and low signals
- Perform the previous for the "bad" circuit"
- Measure the switching noise on both the "good" and "bad" circuit at the same time to make comparison of the results easier

1.6 Final Product

Using the BON sketch from Figure 1 and the engineering specifications, the following schematic and PCB were designed in Altium:

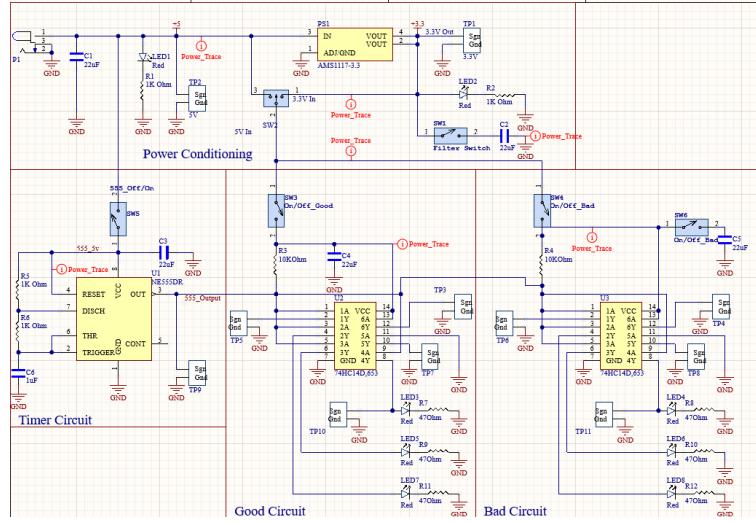


Figure 2: Schematic Designed in Altium

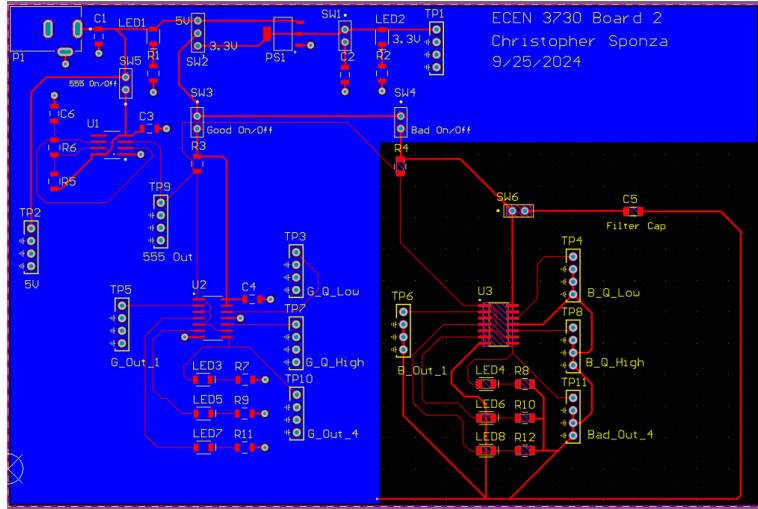


Figure 3: PCB Created in Altium

The blue section of Figure 3 represents the ground plane on the bottom layer and the black section is bare. Below is the board received from the vendor both bare and assembled:

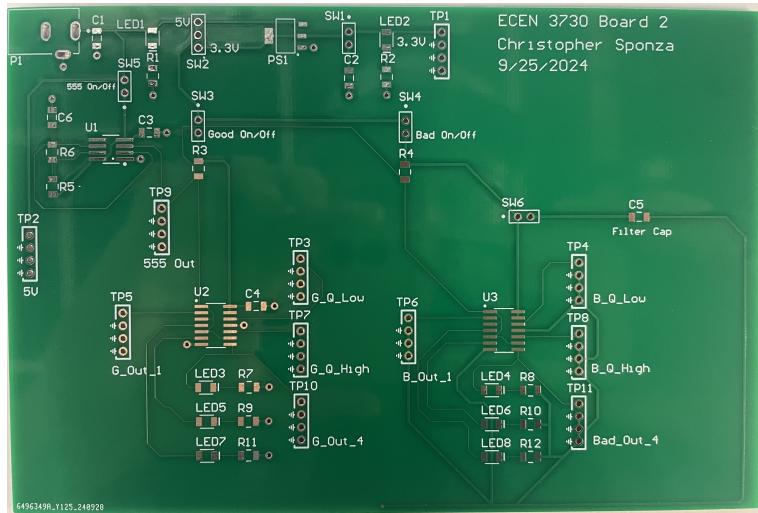


Figure 4: Bare board received from the vendor

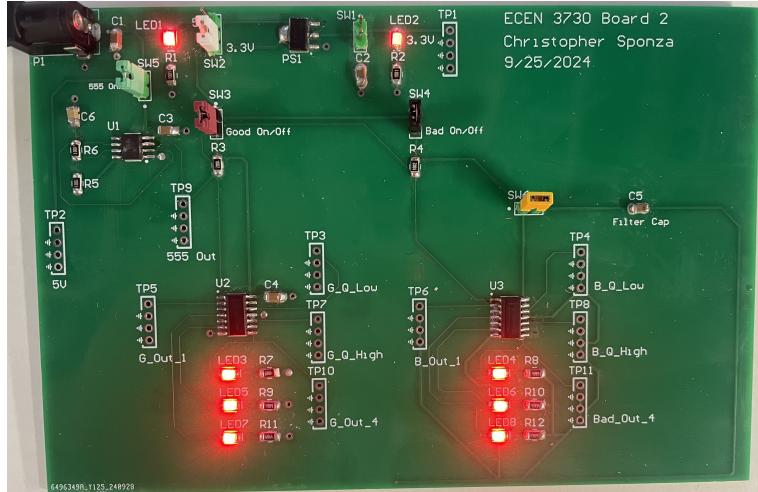


Figure 5: Assembled Board

2 Project Analysis and Measurement

2.1 What Worked

Based on the engineering specifications the board "worked". The 5V and 3.3V rails, output of the 555 timer, and hex inverter outputs were able to be measured and the LEDs provided the necessary indications.

2.2 Test Plan

The board was tested as follows:

- Bring up 5V section, 3V section, 555-Timer, good hex circuit, and bad hex circuit in that order and verify LEDs light up as expected.
- Measure the 5V rail.
- Measure the 3.3V rail with and without the filter capacitor.
- Measure the 555-Timer output
- Measure the good and bad (with the filter capacitor) outputs from the 1st, 4th, quiet high, and quiet low test points on the same scope to compare.
- Measure the 1st, 4th, quiet high, and quiet low test points of the bad circuit both with and without the filter capacitor.

2.3 Measurements

The measurements for the 5V and 3.3V rail were taken simultaneously:

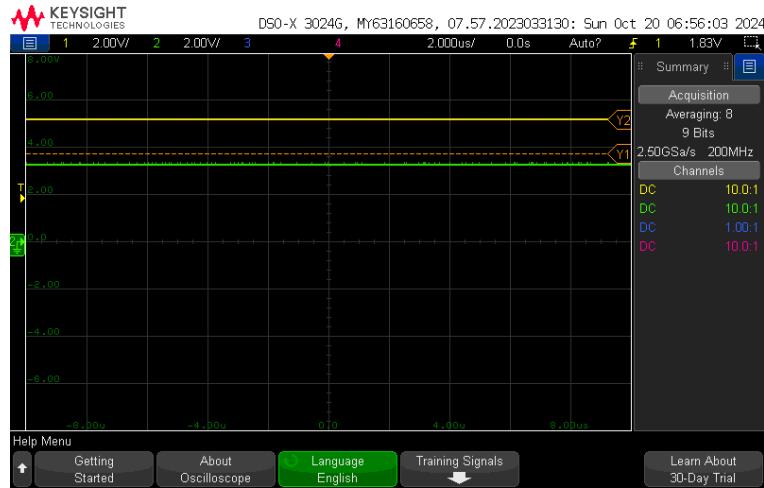


Figure 6: 5V and 3.3V Output on the Same Scope

The small amount of noise for the 3.3V rail (green) in Figure 6 was due to the isolation of the filter capacitor. However, the variation in voltage was too low to measure on the scope. Below is the measurement of the 3.3V rail with the filter capacitor:

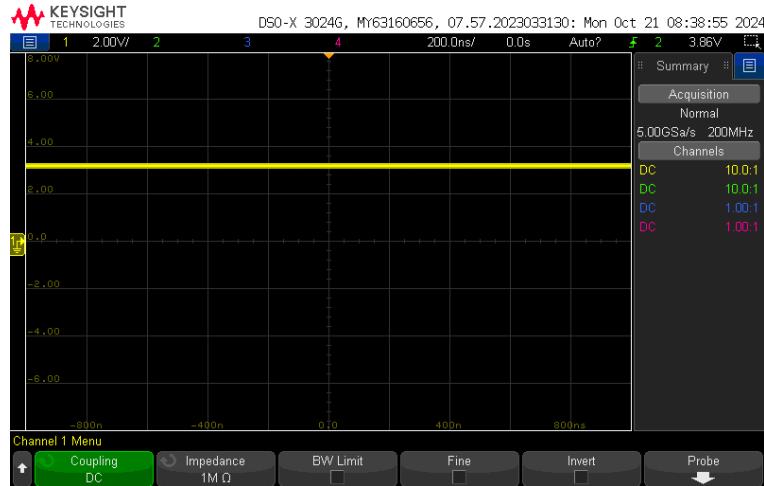


Figure 7: 3.3V Rail Output with a Filter Capacitor

This measurement had no noticeable noise. Next I measured the output of the

555 timer circuit which produced the following:

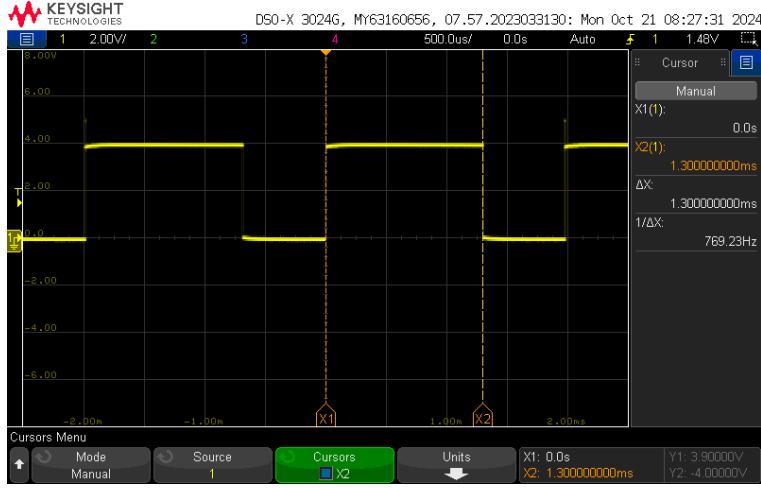


Figure 8: Output of the 555 Timer

Figure 8 shows a period of just under 2ms which corresponds to a frequency of roughly 500Hz. The time high was 1.3ms which corresponds to a duty cycle of 65%. These values are within the engineering specifications. Following the 555 timer I moved on to the testing of the hex circuits. Below are the outputs from the good and bad (with decoupling capacitor) circuits measured simultaneously: As seen in Figure 10 The bad circuit design (green) has roughly +/-0.5V of noise



Figure 9: Rising Edge of the Hex Inverter Output from the First Inverter From Both the Good (Yellow) and Bad (Green) Circuit Designs



Figure 10: Falling Edge of the Hex Inverter Output from the First Inverter From Both the Good (Yellow) and Bad (Green) Circuit Designs

at the falling edge and the good circuit design produces at most 100-200mV of noise. On the rising edge the noise was both minimal and comparable but the signal from the bad design took roughly $30\mu\text{s}$ (2.3% of the time on) of the time

high to reach the same voltage as the good circuit design as seen in Figure 11

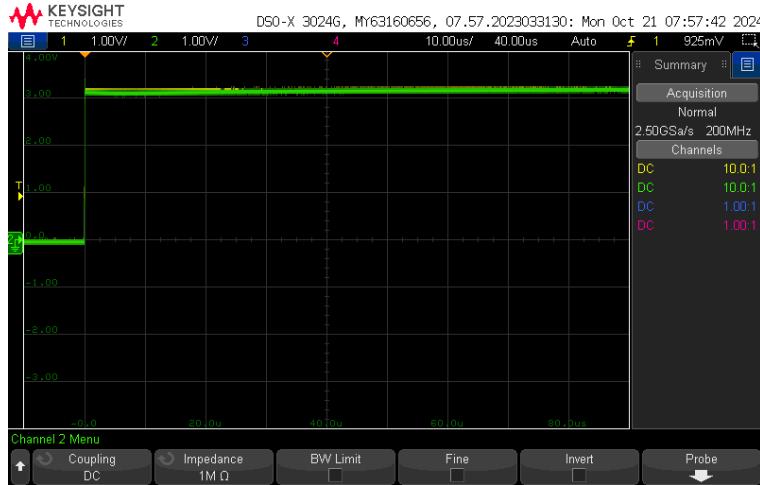


Figure 11: Zoomed-Out Measurement of the Rising Edge of the Good and Bad Circuit Designs

The measurements for the output from the fourth inverter were similar to that of the first and are shown below:

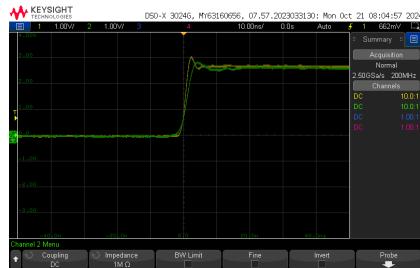


Figure 12: Rising Edge of the Hex Inverter Output from the First Inverter From Both the Good (Yellow) and Bad (Green) Circuit Designs

The rising edge of shown in Figure 12 shows a similar output to the first inverter output as seen in Figure 11. This

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Next I measured and compared the results of the bad circuit design both with

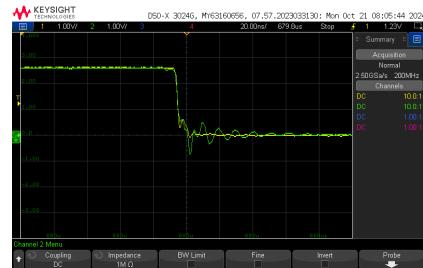


Figure 13: Falling Edge of the Hex Inverter Output from the First Inverter From Both the Good (Yellow) and Bad (Green) Circuit Designs

and without the filter capacitor:

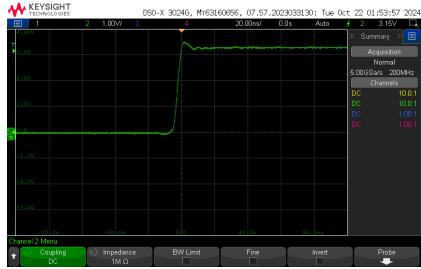


Figure 14: Scope Trace of the Rising Edge of the First Hex Inverter of the Bad Circuit Design with a Decoupling Capacitor

Looking at the rising edge of both the

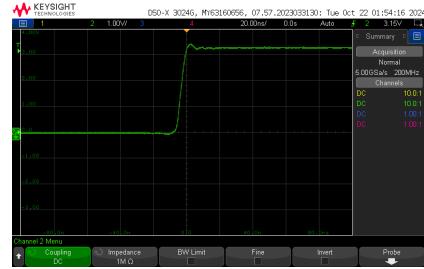


Figure 15: Scope Trace of the Rising Edge of the First Hex Inverter of the Bad Circuit Design with the Decoupling Capacitor Isolated

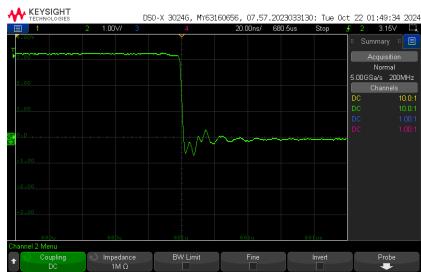


Figure 16: Scope Trace of the Falling Edge of the First Hex Inverter of the Bad Circuit Design with a Decoupling Capacitor

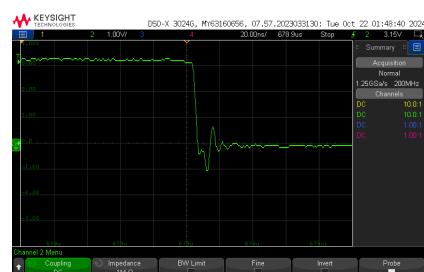


Figure 17: Scope Trace of the Falling Edge of the First Hex Inverter of the Bad Circuit Design with the Decoupling Capacitor Isolated

outputs of the first and fourth hex inverters (Figures 14, 15, 18, and 19) I noticed that there was very little if any effect on the noise of the output from the decoupling capacitor. I attribute this to the nature of the CMOS transistors within the 74HC14D hex inverter IC. Because CMOS transistors have a shorter fall time than rise time the change in current has a greater effect on the noise for the falling edge. This can be seen in Figures 16, 17, 20, and 21 where the decoupling capacitor has a noticeable effect on the noise of the signal. In the case of the outputs of the falling edge of the first and fourth inverter I measured the following:

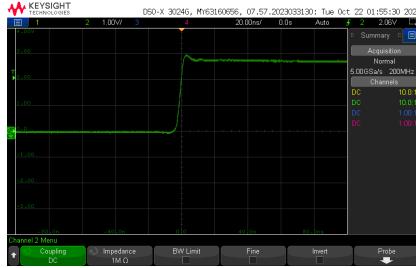


Figure 18: Scope Trace of the Rising Edge of the Fourth Hex Inverter of the Bad Circuit Design with a Decoupling Capacitor

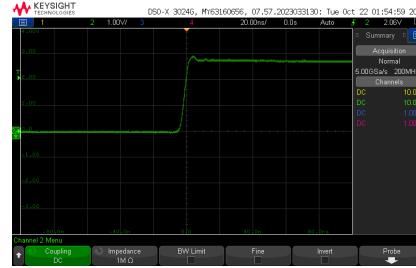


Figure 19: Scope Trace of the Rising Edge of the Fourth Hex Inverter of the Bad Circuit Design with the Decoupling Capacitor Isolated

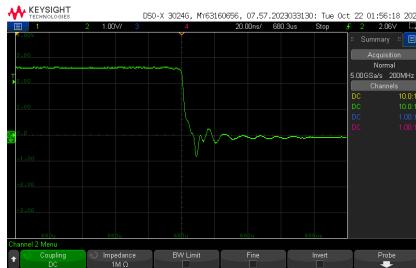


Figure 20: Scope Trace of the Falling Edge of the Fourth Hex Inverter of the Bad Circuit Design with a Decoupling Capacitor

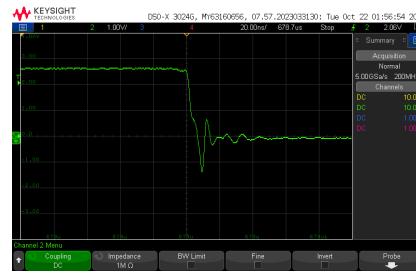


Figure 21: Scope Trace of the Falling Edge of the Fourth Hex Inverter of the Bad Circuit Design with the Decoupling Capacitor Isolated

Output	Decoupling Capacitor?	Voltage
1 (falling)	Yes	+0.2V/-0.8mV
1 (falling)	No	+0.8mV/-1V
4 (falling)	Yes	+0.2V/-0.9V
4 (falling)	No	+0.8V/-1.25V

Isolating the capacitor introduces a considerable amount of noise, especially when you consider that the noise without the capacitor is anywhere from 1.2-3.37 times the original value and, in the case of the output of the fourth inverter, a change equal to roughly half of the original signal. In the case of the quiet high and low signals of the bad circuit design I also measured significant differences in switching noise. From Figures 22, 23, 24, and 25 I measured:

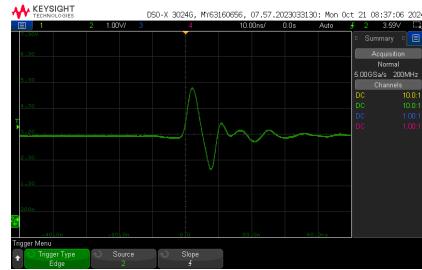


Figure 22: Scope Trace of the High Signal of the Bad Circuit Design with a Decoupling Capacitor

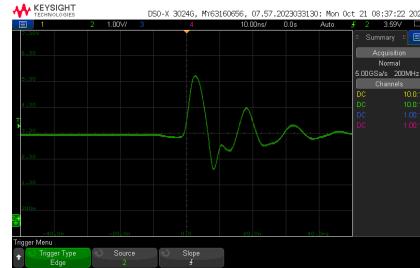


Figure 23: Scope Trace of the High Signal of the Bad Circuit Design with the Decoupling Capacitor Isolated

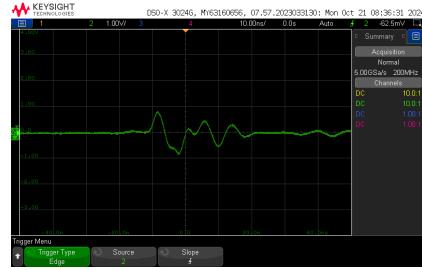


Figure 24: Scope Trace of the Low Signal of the Bad Circuit Design with a Decoupling Capacitor

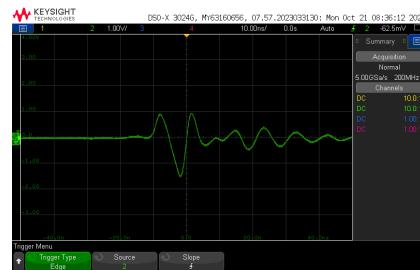


Figure 25: Scope Trace of the High Signal of the Bad Circuit Design with the Decoupling Capacitor Isolated

Output	Decoupling Capacitor?	Voltage
High	Yes	+1.8V/-1.4V
High	No	+2.2V/-1.4V
Low	Yes	+0.8V/-0.8V
Low	No	+1.8V/-0.8V

The reason for the larger amount of noise on the quiet high signals is due to ground bounce. As the circuit switches from high to low a considerable amount of current flows through the ground path causing a significant change in the circuits reference voltage. In this case the outputs are from that of inverters so the switch from high to low is seen on the quiet high test point.

3 Comparison to a Different Design

In order to better understand the quality of my design I have made similar measurements on a comparable board:

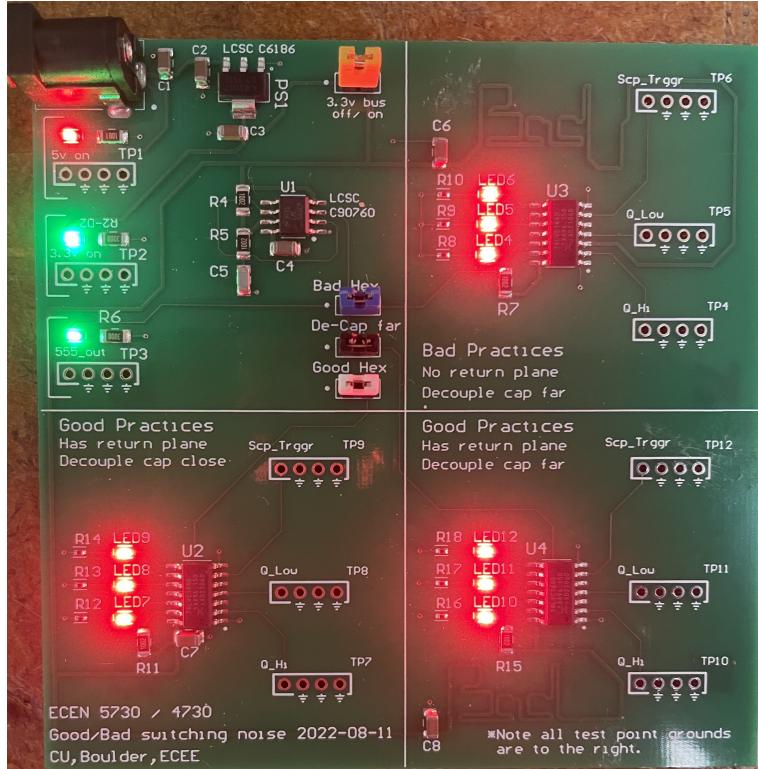


Figure 26: Board Used to Compare My Design

As one can see in Figure 26 There are three sections, good practices, good practices with a decoupling capacitor far, and bad practices. For the purposes of this report I will refer to this board as the "test" board. I analyzed this board in the following manner:

- Compare the measurements of the good circuit of the test board with the decoupling capacitor close and far.
- Compare the measurements of the good circuit (with the capacitor close) and bad circuit of the test board.

Because the frequency of the 555 timer of the test board and that of my own design were different I chose not to directly compare the two.

3.1 Test Board Good Circuit Vs. Test Board Good Circuit W/ Decoup. Cap. Far

Figures 27, 28, 29, 30, 31, and 32 display similar data to that of my design. The rising edge shows very little difference in noise due to the nature of the CMOS transistors within the IC and the falling edge shows a notable change

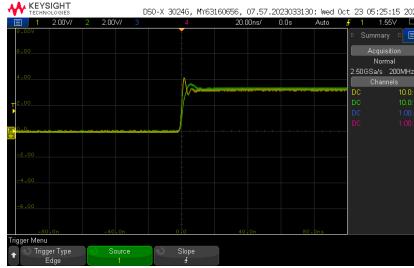


Figure 27: Rising Edge of Signal of the Good Circuit Design (yellow) vs Good Circuit Design with Capacitor Far (green)

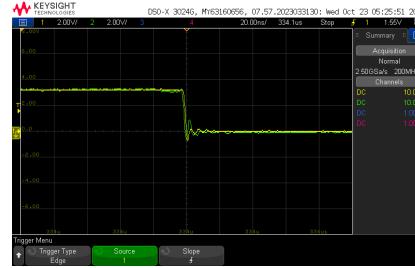


Figure 28: Falling Edge of Signal of the Good Circuit Design (yellow) vs Good Circuit Design with Capacitor Far (green)



Figure 29: Quiet Low Signal of the Good Circuit Design



Figure 30: Quiet Low Signal of the Good Circuit Design with Decoupling Capacitor Far

in noise with the capacitor far. The good design shows no noise and the less ideal design shows noise on both high and low signals with more noise on the high signal. Having the capacitor far added $\pm 0.2V$ to the quiet low signal and $+0.6V/-0.9V$ to the quiet high signal. A similar result was extracted from the bad circuit design where $\pm 0.2V$ of noise was measured on the quiet low signal and $+2V/-1V$ of noise was measured on the quiet high signal as can be seen in Figures 36 and 38 in the next section.

3.2 Test Board Good Circuit Vs. Test Board Bad Circuit

As in the previous section the rising edges shown in Figure 33 show very little difference in noise between the good and bad designs where as the difference in noise of the the falling edges displayed in Figure 34 is notable.

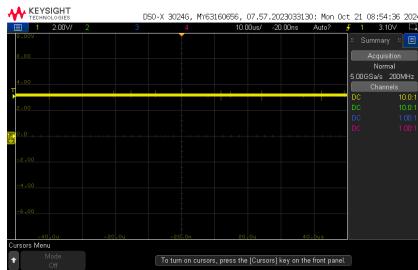


Figure 31: Quiet High Signal of the Good Circuit Design

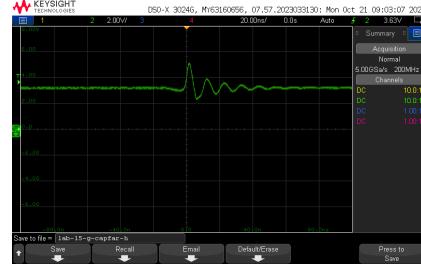


Figure 32: Quiet High Signal of the Good Circuit Design with Decoupling Capacitor Far

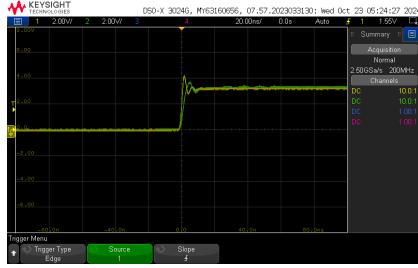


Figure 33: Rising Edge of Signal of the Good Circuit Design (yellow) vs Bad Circuit Design (green)



Figure 34: Falling Edge of Signal of the Good Circuit Design (yellow) vs Bad Circuit Design (green)

4 Conclusion

4.1 Errors

There was a "hard error" in my design that can be seen when power is supplied to the 555 timer but not to one or both of the hex inverter circuits. Because in my design the 555 timer signal can not be isolated from the hex inverter circuit capacitors C4 and C5 from Figure 2 charge through R3 and R4 respectively when the 555 signal is high. When the 555 signal goes low the capacitors discharge through the Vcc pin of the hex inverter IC causing the LEDs to turn on as seen in Figures 39 and 40. Figure 39 shows the circuit when the decoupling capacitor for the bad circuit design is isolated which eliminates this error. I should have designed the switches not to isolate the ICs from power but from the 555 timer output instead.

4.2 What I Would Do Differently

When the hex inverters are not isolated the board works as intended and met all of the engineering specifications. However there are a few things I would

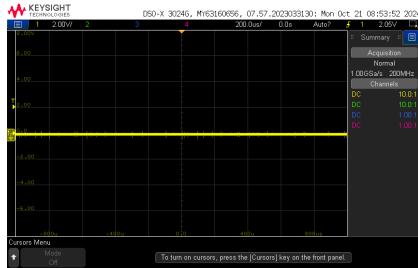


Figure 35: Quiet Low Signal of the Good Circuit Design

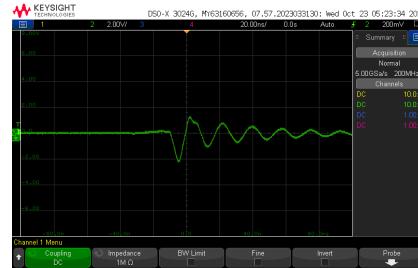


Figure 36: Quiet Low Signal of the Bad Circuit Design

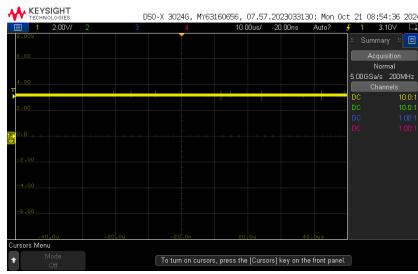


Figure 37: Quiet High Signal of the Good Circuit Design

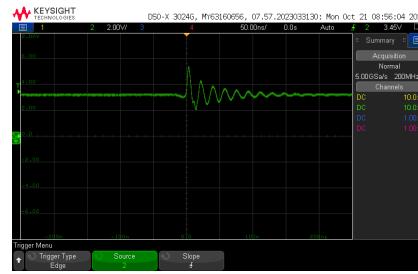


Figure 38: Quiet High Signal of the Bad Circuit Design

change with this design:

- Have the inverter IC switches isolate the 555 timer signal rather than the power.
- Made better use of the space on the board by routing longer traces for the return path by winding them back and forth.
- Placed the decoupling capacitor further from the IC in the bad design.
- Added lines on the silkscreen separating the different section of the board for better readability.

4.3 Learning Take-Aways

- Ground planes play a crucial role in reduction of switching noise and should always be used unless there is a strong compelling reason otherwise.
- LEDs can provide important "at a glance" data for debugging and board bring-up.
- Filter capacitors should be placed as close to an IC as possible.

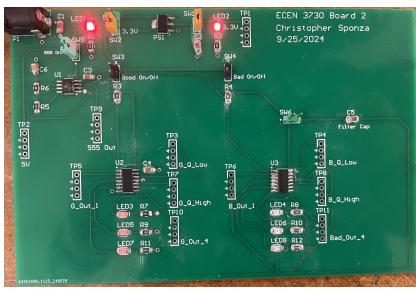


Figure 39: Scope Trace of the Low Signal of the Bad Circuit Design with a Decoupling Capacitor

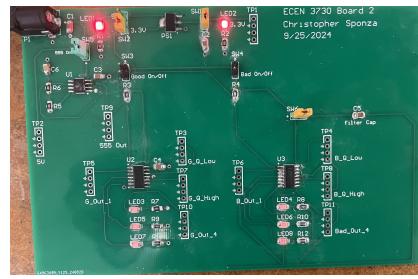


Figure 40: Scope Trace of the High Signal of the Bad Circuit Design with the Decoupling Capacitor Isolated