2017 National Power Electronics Conference (NPEC)
College of Engineering Pune, India. Dec 18-20, 2017

Double Pulse Test Based Switching Characterization of SiC MOSFET

S. S. Ahmad and G. Narayanan
Department of Electrical Engineering
Indian Instiute of Science, Bangalore - 560012 INDIA
email: shahjahans@iisc.ac.in, gnar@iisc.ac.in

***Abstract*—Switching characteristics of a 1200 V, 90 A SiC MOSFET in an asymmetric H-bridge power converter are measured. Double pulse tests are carried out at different current and voltage levels. The experimental set-up and procedure are explained in detail. The switching waveforms are used to obtain the voltage and current transition times of the MOSFET. The turn-on and turn-off energy losses are also calculated. Since these are influenced by layout of the power circuit, the power converter layout and its effect on the switching waveform are reported. The turn-off energy loss is lower than the data-sheet specified value, while the turn-on energy loss is higher; the total loss is close to the data-sheet value.**

***Index Terms*—Asymmetric H-bridge converter, double pulse test, SiC MOSFET, switching characteristics**

I. Introduction

Wide band-gap devices, such as those based on SiC and GaN, offer superior performance than their Si based counterparts [1]–[4]. Due to their higher breakdown electric field strength, the drift region length required to have the same blocking voltage is lower than that of Si based devices. Consequently, these devices have better trade-off between specific on-resistance and blocking voltage. Among the wide band-gap devices, SiC based power MOSFET's are commercially available with much larger blocking voltage than Si MOSFET's. SiC MOSFET's having blocking voltage in the range of 1.2 kV up to 15 kV can potentially replace Si IGBT's, while offering faster switching transients, lower losses and high frequency operation [2]. The high blocking voltage and high switching frequency operation of SiC MOSFET's are particularly advantageous in high-speed motor drives [5]–[7], where the modulation frequency is quite high [8]. In the present context, a SiC MOSFET based converter is considered for high-speed switched reluctance machine (SRM) drive.

One of the advantages of SiC devices is lower turn-on and turn-off switching losses than Si devices. Evaluation of switching losses requires knowledge of the device switching characteristics. In this paper double pulse test is used to characterize the device [9]. This test is fast, and the energy lost in the measurement process is quite low.

This work was supported by the Ministry of Human Resources Development and the Ministry of Power, Government of India, under an IMPRINT project titled "Design, Development and Control of High-Speed Switched Reluctance Generator for Direct-Coupled Operation with Thermal Turbo-Machinery"

The switching characteristics depend not only on the device internal parameters and operating conditions, but also on the external circuit and its layout [10], [11]. In [12]–[14] double pulse tests have been carried out in a dedicated double pulse test set-up. A separate double-pulse test circuit allows for more accurate measurement of voltage and current waveform, but may not reflect the actual circuit layout in a power converter. Therefore it is useful to measure the switching characteristics of the device as it is used in the power converter. The most commonly used power converter for SRM is the asymmetric H-bridge power converter, one phase of which is shown in Fig. 1. The characterization is carried out in this power converter. The tests in this paper are carried out at two different voltage levels (600 V and 800 V), which are representative of the voltage levels used in a power converter utilizing 1200 V devices. At each voltage level, the switching transient characteristics are reported for different device current levels from 10 A to 70 A.

II. Experimental Set-up

One phase of an asymmetric H-bridge (AHB) power converter is shown in Fig. 1. The converter consists of as many phases as the switched reluctance machine (SRM). In the present case, the converter is designed for a 20 kW, 800 V DC bus, 3 phase SRM. Based on this requirement, the devices and the DC bus capacitor are sized appropriately. Each phase of the converter is assembled on separate printed circuit board (PCB).

A. Circuit Components

In the present design, the DC bus capacitor, C_{dc} in Fig. 1 consists of eight 50 µF metallized polypropylene film capacitors, four 3 µF metallized polypropylene film capacitors and four 0.1 µF surface-mount capacitors, all in parallel. Also, each switch in Fig. 1 consists of two parallel devices. Totally, there are four MOSFET's and four diodes per phase. The parallel devices are laid out symmetrically in the PCB as far as possible. Each MOSFET-diode pair has two 50 µF capacitors, one 3 µF capacitor and one 0.1 µF placed nearby.

The AHB circuit has one high-side switch and one low-side switch. The double pulse tests are carried out on the high-side switch. The modified circuit connections are shown in Fig. 2. The other low-side switch is kept off. Also, only one MOSFET-diode pair is used for the tests; the parallel MOSFET-diode pair

978-1-5386-3236-9/17/$31.00 ©2017 IEEE

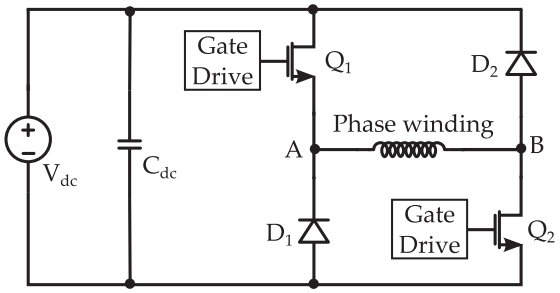


Fig. 1. One phase of the asymmetric H-bridge power converter

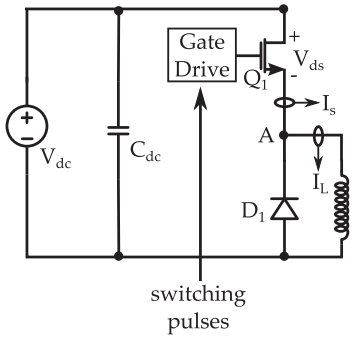


Fig. 2. Schematic of the double pulse test circuit used

and their associated capacitors are not connected to the circuit. A 830 µH air-core inductor is used as the load inductor.

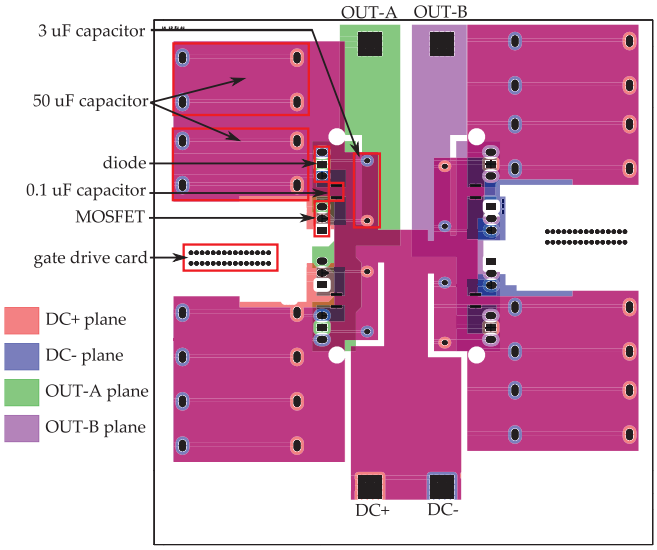
The SiC MOSFET tested is C2M0025120D which is rated for 1200 V and 90 A continuous current at a case temperature of 25 °C. The free-wheeling diode is SiC schottky diode C4D40120D. The diode is specified for 1200 V and 113 A continuous current, also at a case temperature of 25 °C. During the tests, the device case was at room temperature, which was about 25 °C.

B. Gate Driver

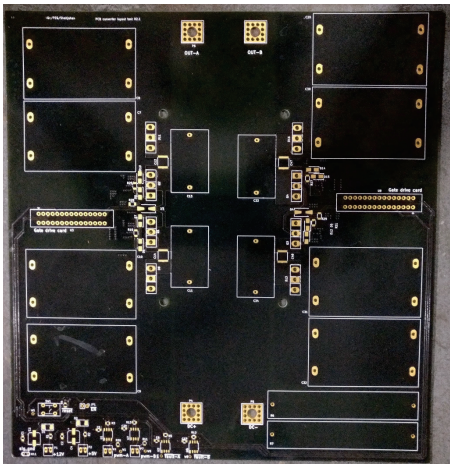
The gate driver unit consists of an isolator, an isolated gate power supply, an output buffer and a short-circuit protection unit. The isolator used is ISO7842, which is rated for 8 kV peak transient isolation voltage. The isolated gate power supply (MGJ2D122005SC) is rated for 2 W average power. This provides the required isolated gate drive voltage levels of +20 V during the on-state and -5 V during the off-state of the SiC MOSFET. These voltage levels are as per the manufacturer's recommendation. The gate of the MOSFET is driven by an output buffer (IXDD609), which can provide up to 9 A of peak current. A 9 Ω gate resistance is used in the tests. The short-circuit protection is based on the device drain-source voltage sensing. The device voltage is compared with a set-point voltage to indicate faulty or normal operation. The set-point is set so that, if the device current rises beyond 75 A, a fault is indicated and the device is quickly turned off. Further details on the gate driver are provided in [15].

C. PCB layout

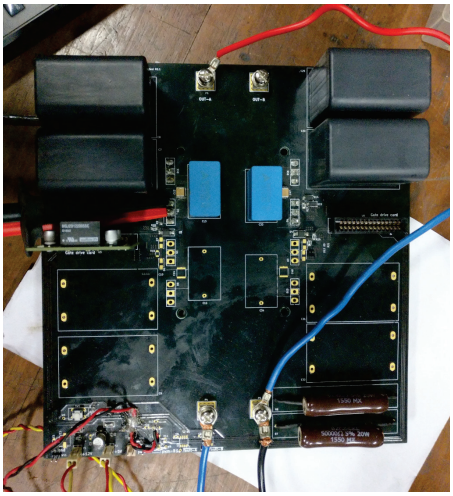
The double pulse test results depend on the PCB layout and component placement to a certain extent. Care has been taken



(a)



(b)



(c)

Fig. 3. (a) Layout of the power converter showing only the power planes, DC bus capacitor, power devices and gate drive placement. Components for only one part of the layout has been marked for clarity. (b) Photograph of unpopulated PCB for reference (c) Photograph of populated PCB

to minimize inductance in the traces carrying switching current. As mentioned earlier, the PCB layout used here is the same layout as that in the power converter. The PCB layout is shown in Fig. 3(a). The power carrying components are highlighted. Overlapping DC bus planes are used to minimize the bus inductance. The DC bus capacitors are placed physically close to the switching devices. The MOSFET and the free wheeling diode are placed close to each other as well. Photographs of the unpopulated PCB and the assembled PCB are shown in Fig. 3(b) and 3(c), respectively.

It is a four layer PCB. Layer 2 is the positive DC bus (DC+) and layer 3 is the negative DC bus (DC-). Layer 4 consists of OUT-A and OUT-B copper planes. These correspond to the output terminals A and B of the converter leg. Layer 1 does not have any large current carrying trace. The layer structure influences the capacitances, which in turn affects the switching loss. This is further discussed in the results section.

D. Current and voltage measurement

The data-sheet specified rise and fall times of V_{ds} of the MOSFET are both about 30 ns. The rise and fall times both increase as the gate resistance is increased. Therefore for V_{ds} measurement, a voltage probe of adequate bandwidth is needed. Although single-ended voltage probes offer large bandwidth, the noise pick-up was found to be unacceptable. Therefore, Tektronix P5200A differential high voltage probe is used. This has a bandwidth of 50 MHz, and a rise time of 7 ns. The data-sheet specified delay of the voltage probe is 21 ns [16].

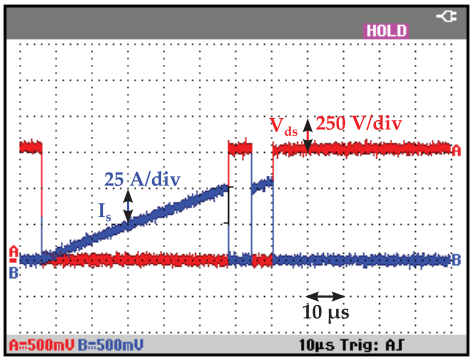
The device current is measured using PEM CWT-UM-1 Rogowski coil. The Rogowski coil is chosen since it is suitable for measuring the source current of the TO-247 packaged SiC MOSFET, without any modifications in the circuit. It is rated for 300 A peak current, and measurement frequency range from 9.2 Hz to 30 MHz. The current probe is suitable for 20 $\mathrm{kA/\mu s}$ peak $\frac{di}{dt}$. The current probe delay is about 28 ns [17]. Since the delays of the two probes are nearly matched, no additional compensation for probe delays is carried out.

III. Experimental Results

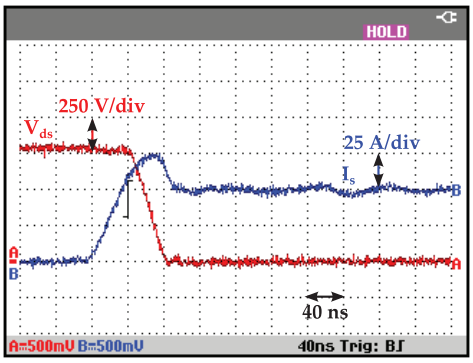
The tests are carried out at two DC bus voltages, namely 800 V and 600 V. The inductor current I_L during turn-on and turn-off of the MOSFET is varied from 10 A to 70 A, in steps of 10 A. The turn-on and turn-off transitions of the MOSFET voltage and current are recorded using a 500 MHz oscilloscope.

A. Experimental Procedure

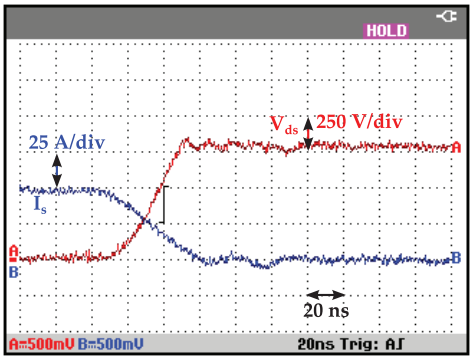
In the double pulse test, firstly a long turn-on pulse is applied to the top device in Fig. 2. Positive voltage $+V_{dc}$ is applied across the inductor during this time interval, and therefore the current rises. The duration of this pulse is adjusted according to the required test current. The device is turned off at the end of the first pulse. The inductor current free-wheels through the diode while the MOSFET is off. After a short while the device is turned on again, and the inductor current commutates from the free wheeling diode to the MOSFET. The device off time between these two pulses is kept small so that change in inductor current is small. The device is turned off again after a small time interval, and the inductor current flows through the free wheeling diode until it gradually reduces to zero. The device turnoff characteristics is obtained at the falling edge of the first pulse, and the turn-on characteristics is obtained at the rising edge of the second pulse [9], [12].



(a)



(b)



(c)

Fig. 4. Double test waveform at 800 V and 50 A (a) Device voltage and current during the complete test (b) Device voltage and current during turn-on (b) Device voltage and current during turn-off

B. Measured Current and Voltage Waveforms

The double pulse test waveforms for 800 V and 50 A are shown in Figs. 4(a)-(c). In Fig. 4(a) the overall record during the double pulse test is shown, while Fig. 4(b) shows the turn-on transition and Fig. 4(c) presents the turn-off transition. The

width of the first pulse is set according to the desired switching current level, which is 50 A in this particular case. At the end of the first pulse, the device turns off, and the device voltage and current during the turn-off process are recorded, which is shown in Fig. 4(c). After a short while the device is turned on again, and the device voltage and current during the turn-on transient are also recorded, which is shown in Fig. 4(b). During turn-on transient, the voltage falls at a rate of 20 $\mathrm{V/ns}$, while current rises at a rate of 1.28 $\mathrm{A/ns}$. During turn-off transient, voltage rises at a rate of 21.3 $\mathrm{V/ns}$, and current falls at a rate of 0.97 $\mathrm{A/ns}$.

Waveforms corresponding to 600 V and 50 A are shown in Figs. 5(a)-(b). In both Figs. 4 and 5 an overshoot in current during the turn-on and an overlap between current fall and voltage rise during the turn-off transition can be observed. These are due to the parasitic capacitances present in the circuit. These include the junction capacitance of the free wheeling diode, the parasitic capacitance between the OUT-A and DC+ copper plane in the PCB, the parasitic capacitance between the OUT-A and DC- copper planes, and also in the load cable and inductor.

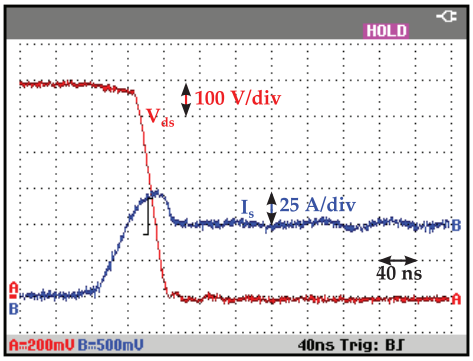
The capacitance between OUT-A and DC+ plane adds to the MOSFET C_{ds}, slows down the v_{ds} transition, and increases the switching loss [11]. The diode capacitance, capacitance between OUT-A and DC-, and that between the load terminals are all in parallel. These increase the turn-on loss, and reduce the turn-off loss [11]. The charging current causes overshoot during turn-on current transient and increases the device turn-on loss, while discharging current reduces the turn-off loss.

In the present PCB, layer 2 is positive DC plane (DC+), layer 3 is negative DC plane (DC-) and layer 4 is OUT-A copper plane. Therefore, between DC+ and OUT-A is the DC- plane, which reduces the capacitance between DC+ and OUT-A. Hence the switching losses do not increase much. The capacitance between DC- and OUT-A will be higher, but its effect on the overall switching energy loss is small. However, the same layer structure will increase capacitance between DC- and OUT-B plane, which comes in parallel to the C_{ds} of the low-side MOSFET; this may increase its switching loss.

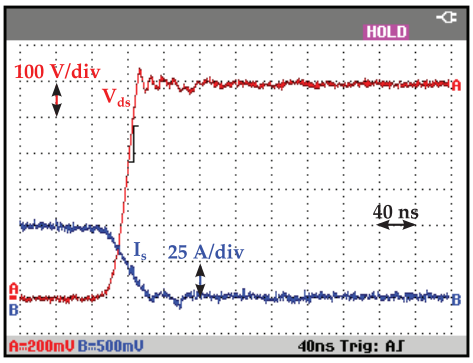
C. Measured Switching Transient Time

The 10% to 90% rise and fall times of device voltage and current during the switching transients have been obtained using the experimental switching waveforms. Figs. 6(a)-(b) show the voltage fall and current rise times during turn-on transient. These values are obtained at different values of current (i.e. 10 A to 70 A) and at two different DC bus voltages (i.e. 600 V and 800 V). Due to the initial current overshoot during turn-on transient, there is not much effect of inductor current on the voltage fall time. At higher DC voltage, the voltage fall time increases. In Fig. 6(b) the current rise time is nearly insensitive to DC bus voltage, and increases with load inductor current. Note that the device data-sheet does not specify the switching transition times for inductive current switching.

The voltage rise and current fall times are shown in 7(a)-(b), which are measured during the device turn-off transient. Like voltage fall time, voltage rise time also increases with



(a)



(b)

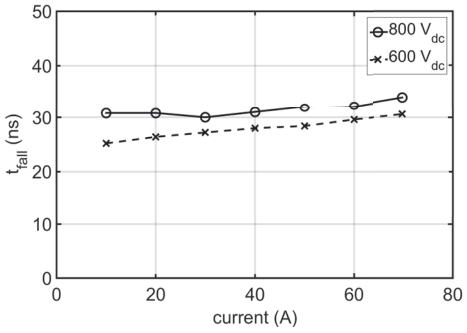
Fig. 5. Device voltage and current during switching transient at 600 V and 50 A (a) Turn-on (b) Turn-off

increase in DC bus voltage. Also, the voltage rise time increases significantly at low currents. The current fall time increases with load current as seen in Fig. 7(b).

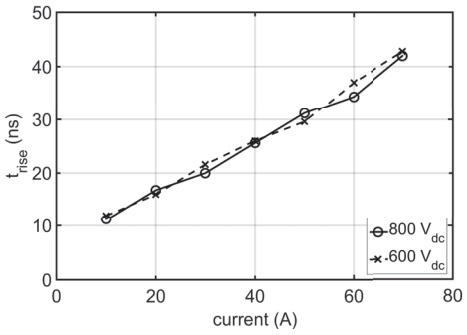
D. Switching Energy Loss

The switching energy loss is obtained by numerically integrating the product of measured current and voltage waveform during the turn-on and turn-off transients. The results are shown in Fig. 8(a)-(b) for different current levels. The results corresponding to 600 V DC bus voltage are shown Fig. 8(a), while Fig. 8(b) corresponds to 800 V. Losses are higher at higher voltage. It can be observed that, in all the cases, turn-on loss dominates the total loss. Small negative turn-off loss is obtained at low current is due to inaccuracies in the measurement. The measuring instruments are not suitable for measuring very low loss values. Turn-off energy loss at low currents could be taken as zero for practical purposes.

The turn-off switching energy loss obtained here is lower than the data-sheet specified values, while the measured turn-on switching energy loss is higher. This is due to the effects of parasitic capacitance as explained earlier. The total switching energy loss measured is close to the data-sheet specified value at 9 Ω gate resistance.

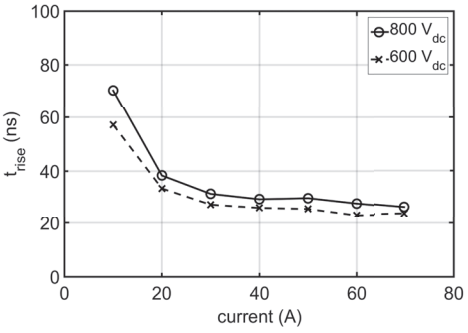


(a)

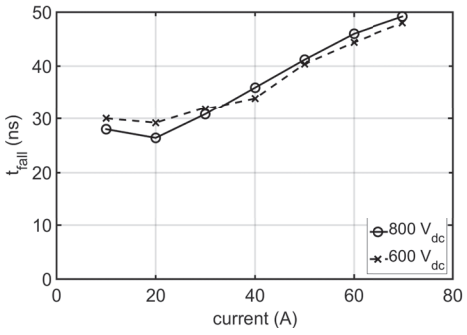


(b)

Fig. 6. Measured device voltage fall and current rise time variation with inductor current and DC bus voltage during device turn-on transient (a) Voltage fall time (b) Current rise time

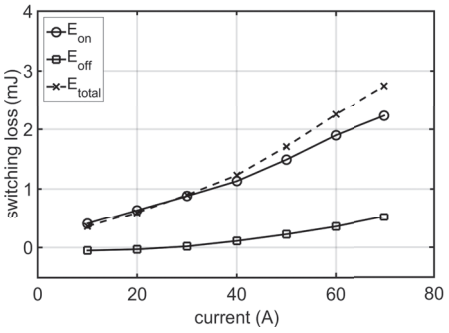


(a)

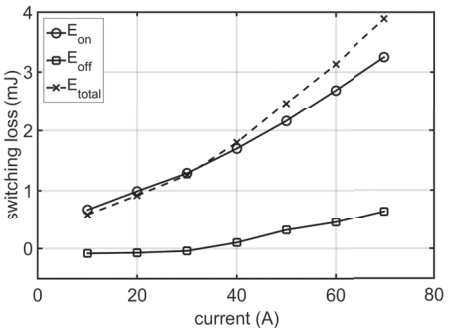


(b)

Fig. 7. Measured device voltage rise and current fall time variation with inductor current and DC bus voltage during device turn-off transient (a) Voltage rise time (b) Current fall time



(a)



(b)

Fig. 8. Measured device switching energy loss - turn-on loss (E_{on}), turn-off loss (E_{off}) and total loss (E_{total}) at different current levels (a) at 600 V DC bus (b) at 800 V DC bus

IV. Conclusion

In this paper, test results of double pulse test of a 1200 V, 90 A SiC MOSFET are given. The tests are carried out in the asymmetric H-bridge power converter layout. Since PCB layout, component selection and their placement effect the characteristics, these are discussed in detail. Turn-on and turn-off transients waveforms are presented, and effect of PCB layout on these are given. The rise and fall times of current and voltage during turn-on and turn-off transitions of the device, are measured at different device currents and DC bus voltages. It is observed that current transition time is not much dependent on the DC bus voltage, while voltage transition times increase with DC bus voltage. The current transition times are strong functions of device current, and increase with current. Also, at low currents, the voltage rise times increase sharply. The losses are also obtained from the experimental data at different voltage and current levels.

References

[1] J. Milln, P. Godignon, X. Perpi, A. Prez-Toms, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[2] J. W. Palmour, L. Cheng, V. Pala, E. V. Brunt, D. J. Lichtenwalner, G. Y. Wang, J. Richmond, M. O'Loughlin, S. Ryu, S. T. Allen, A. A. Burk, and C. Scozzie, "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *Int. Symp. Power Semiconductor Devices*, June 2014, pp. 79–82.

[3] T. Ueda, "Recent advances and future prospects on GaN-based power devices," in *Int. Power Electron. Conf.*, May 2014, pp. 2075–2078.

[4] E. Gurpinar and A. Castellazzi, "Single-phase t-type inverter performance benchmark using Si IGBTs, SiC MOSFETs, and GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7148–7160, Oct 2016.
[5] S. Madhusoodhanan, K. Mainali, A. Tripathi, K. Vechalapu, and S. Bhattacharya, "Medium voltage ($\geq$ 2.3 kV) high frequency three-phase two-level converter design and demonstration using 10 kv sic mosfets for high speed motor drive applications," in *Appl. Power Electron. Conf. and Expo.*, March 2016, pp. 1497–1504.
[6] A. Morya, M. Moosavi, M. C. Gardner, and H. A. Toliyat, "Applications of wide bandgap (WBG) devices in AC electric drives: A technology status review," in *Int. Electric Machines and Drives Conf.*, May 2017, pp. 1–8.
[7] R. Togashi, Y. Inoue, S. Morimoto, and M. Sanada, "Performance improvement of ultra-high-speed PMSM drive system based on DTC by using SiC inverter," in *Int. Power Electronics Conf.*, May 2014, pp. 356–362.
[8] A. Tripathi and G. Narayanan, "Evaluation and minimization of low-order harmonic torque in low-switching-frequency inverter-fed induction motor drives," *IEEE Trans. Ind. Applicat.*, vol. 52, no. 2, pp. 1477–1488, 2016.
[9] R. O. Lyra, B. J. Cardoso Filho, V. John, and T. A. Lipo, "Coaxial current transformer for test and characterization of high-power semiconductor devices under hard and soft switching," *IEEE Trans. Ind. Applicat.*, vol. 36, no. 4, pp. 1181–1188, 2000.
[10] P. Nayak and K. Hatua, "Modeling of switching behavior of 1200 V SiC MOSFET in presence of layout parasitic inductance," in *Int. Conf. Power Electron., Drives and Energy Systems*, Dec 2016, pp. 1–6.
[11] J. Wang, H. S. h. Chung, and R. T. h. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan 2013.
[12] G. P, M. R, R. K. R, and R. J. Vijayan, "Characterisation of 1200 V, 35 A SiC Mosfet using double pulse circuit," in *Int. Conf. Power Electron., Drives and Energy Systems*, Dec 2016, pp. 1–6.
[13] H. Li and S. Munk-Nielsen, "Detail study of SiC MOSFET switching characteristics," in *Int. Symp. Power Electron. Distributed Generation Sys.*, June 2014, pp. 1–5.
[14] B. N. Torster, S. Tiwari, R. Lund, and O. M. Midtgrd, "Experimental evaluation of switching characteristics, switching losses and snubber design for a full SiC half-bridge power module," in *Int. Symp. Power Electron. Distributed Generation Sys.*, June 2016, pp. 1–8.
[15] A. Kar, S. S. Ahmad, G. Narayanan, and M. Sengupta, "Design, performance evaluation, fabrication and testing of a SiC MOSFET gate driver," in *Int. Conf. Signal Processing, Informatics, Communication and Energy Sys.*, August 2017.
[16] Tektronix. (2017, Oct.) High-voltage differential probes. [Online]. Available: http://download.tek.com/manual/P5200A-High-Voltage-Differential-Probe-Instruction-Manual-077053602.pdf
[17] PEM. (2017, Oct.) Cwt ultra mini technical notes. [Online]. Available: http://www.pemuk.com/Userfiles/CWTum/CWTUM%20-%20Technical%20notes%20-%20001.pdf