309 Processor Core May Execute Incorrect Instructions on Concurrent L2 and Northbridge Response

Description

Under a specific set of internal timing conditions, an instruction fetch may receive responses from the L2 and the northbridge concurrently. When this occurs, the processor core may execute incorrect instructions.

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

BIOS should set MSRC001_1023[23].

Fix Planned

Yes