776 Incorrect Processor Branch Prediction for Two Consecutive Linear Pages

Description

Under a highly specific and detailed set of internal timing conditions, the processor core may incorrectly fetch instructions when the instruction pointer (rIP) changes (via a branch or other call, return) between two consecutive linear address 4K pages with the same offset in rIP[11:6].

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

BIOS should set MSRC001_1021[26] = 1b.

Fix Planned

No fix planned