372 Processor Read That Matches The Address of an Earlier Uncompleted Write May Be Incorrect

Description

Under a highly specific and detailed set of internal timing conditions, processor data for a read may be corrupted when a read occurs that matches the address of an earlier uncompleted write or L3 eviction.

This erratum applies only when both of the following conditions are satisfied on any processor node:

- DRAM controllers are in DCT link unganged mode ([DRAM Controller Select Low Register] F2x110[DctGangEn] = 0b).
- The northbridge current operating frequency (COF) is less than 3 times the memory clock frequency.

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

On systems supporting DDR3-1333 or northbridge P-state 1, and using DCT link unganged mode, system software should set MSRC001_001F[52:51] to 11b.

Fix Planned

No