# 691 Processors Using 1 MB L3 Subcaches May Execute a Write-Back Invalidate Operation Incorrectly

### Description

The processor may fail to flush the full address range of L3 cache when executing a WBINVD instruction, or INVD instruction with Hardware Configuration Register[INVDWBINVD] = 1b (MSRC001_0015[4]). This occurs when the L3 cache is less than 8 MB per northbridge and is configured using at least one 1 MB L3 subcache, as indicated by the L3SubcacheSize fields (L3 Cache Parameter Register[L3SubcacheSize[3:0]], D18F3x1C4[[15:12],[11:8],[7:4],[3:0]] = Dh or Eh).

### Potential Effect on System

Unpredictable system behavior. This has only been observed by AMD as a system hang while using cache as general storage during boot.

### Suggested Workaround

Contact your AMD representative for information on a BIOS update.

### Fix Planned

No fix planned