561 Processor May Incorrectly Walk Page Tables in I/O or Non-Cacheable Memory

Description

When HWCR[TlbCacheDis] (MSRC001_0015[3]) is 1b and the page tables reside in I/O or DRAM that is marked non-cacheable, the processor may incorrectly perform page table walks.

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

None required. No operating system places page tables in memory that is not marked as WB DRAM, and therefore HWCR[TlbCacheDis] can always be at its reset state of 0b.

Fix Planned

No