784 Processor May Incorrectly Provide Control Register Data as the Result of a Load Operation

Description

Under a highly specific and detailed set of internal timing conditions, the processor core may provide control register data as the result of an instruction that is performing a load from memory. In order to observe this incorrect data, the processor must be at the highest privilege level (CPL 0) and be speculatively or non-speculatively executing certain invalid opcodes.

Potential Effect on System

Data corruption causing unpredictable system behavior.

Suggested Workaround

Contact your AMD representative for information on an update.

Fix Planned

No