564 Processor May Fail to Set Auto-Halt Restart in SMM Save State

Description

The processor core may not set the auto-halt restart flag (offset FEC9h of the SMM save state area) when a HLT instruction causes the processor core to enter the core C6 (CC6) state and is then interrupted by an SMI. After the SMM code executes the RSM instruction, the processor core does not re-enter the HLT or CC6 state due to this incorrect auto-halt restart flag.

Potential Effect on System

The processor may continue execution after the HLT instruction, resulting in unpredictable system behavior. The operating system is not required to have a valid instruction after a HLT instruction when rFLAGS.IF = 1.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

No