

EEC 315 / 316

Electronics Laboratory Manual

**Department of Electrical Engineering and
Computer Science
Cleveland State University**

December 2021

* This manual has been edited with the support by the Ohio Space Grant Consortium (OSGC) Curriculum Innovation Proposal (CIP) Grant Award.

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Forward

The experiments in this manual complement the material covered in the course EEC 313 Electronics I and EEC 314 Electronics II. This manual has been developed with the following goals.

- We would like every student to have an opportunity to conduct experiments individually because group-work oftentimes justifies placing more students than appropriate in a work bench. We have evaluated inexpensive, portable lab kits including ADALM 2000, OpenScope MZ, and Analog Discovery 2 for this purpose since 2018.
- We'd like to create a consistent, single document manual. Over the years, instructors have developed pre-lab and post-lab assignments associated with each lab experiment. But they cause confusions because they are in separate documents and not consistent with each other.
- We'd like to include theory review sessions to make the manual self-contained. This is necessary because some students take this course, EEC 315/316 Electronics Lab, without taking EEC 313 Electronics I and/or EEC 312 Electric Circuit Lab. This is not desirable, but it happens. We included three theory review sessions in the manual (Lab 1, Lab 5 and Lab 11).

Note that during Spring 2020 through Summer 2021, COVID-19 rendered us to deliver all classes including laboratory courses remotely. Luckily, we were able to deliver lab experience remotely without having to resort to simulations. We chose Analog Discovery 2 (AD2) and the lab manual has been revised accordingly.

- We divided the laboratories into three parts, i.e., Diodes, Transistors, and Op Amplifiers to give a better idea of this lab course structure.
- AD2 is used in Part II and III of the manual in the form of post-lab assignments. We assume AD2 and the corresponding lab kits including a breadboard and a multimeter are supplied to students before Part II begins.
- Students are encouraged to simulate the lab using PSPICE as pre-lab assignments to gain an intuitive understanding of the electronics involved, to hand work a simplified analysis, and to compare these with the observed experimental behavior.

This lab manual was supported by Ohio Space Grant Consortium (OSGC) Curriculum Innovation Proposal (CIP) Grant Award. I appreciate Dr. Lili Dong, Ms. Anusree Mandali and Mr. Joel Folkmann for the development of this manual. Note that some experiments are from H. M. Berlin, Experiments in Electronic Devices, 5th Edition, Prentice Hall, 1999. Note also that this lab manual is continually being redeveloped. Please give your feedback concerning the lab experiments and procedures so that the future manuals can be as error-free as possible.

Prof. Chansu Yu
December 2021

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Part I

Diodes

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Lab 1

Introduction to Electronics/Electronics Devices Lab

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1- Basic Components

1.1 Breadboard

Has power strip and terminal strip as shown in Fig. 1.

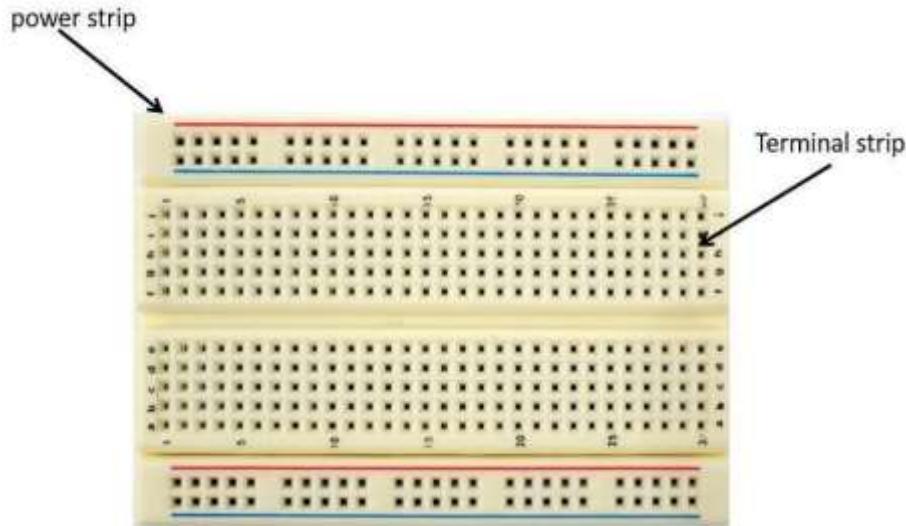


Fig. 1 Breadboard

- Each number in the terminal strip represents single node.
- The power strip on either side is not connected internally.
- Entire red line and blue line in the power strip are connected internally.
- The internal connection of the breadboard is shown Fig. 2.
- From Fig. 2, A and D sections are not connected internally. In the same way B and C sections are also not connected internally.

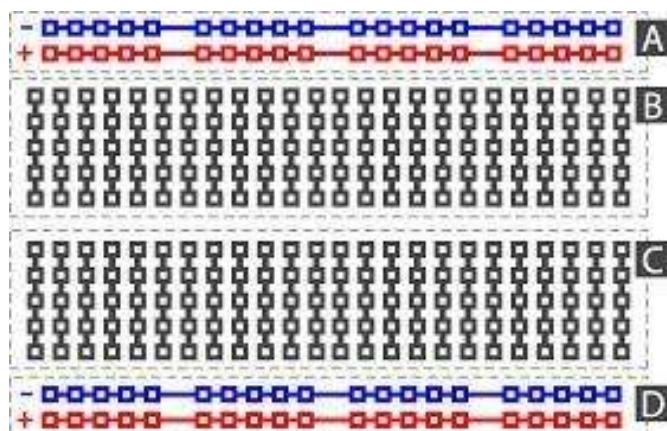


Fig. 2. Internal connections of a breadboard

1.2 Resistors

- No polarity
- Color code chart for the resistors is shown in Fig. 3.

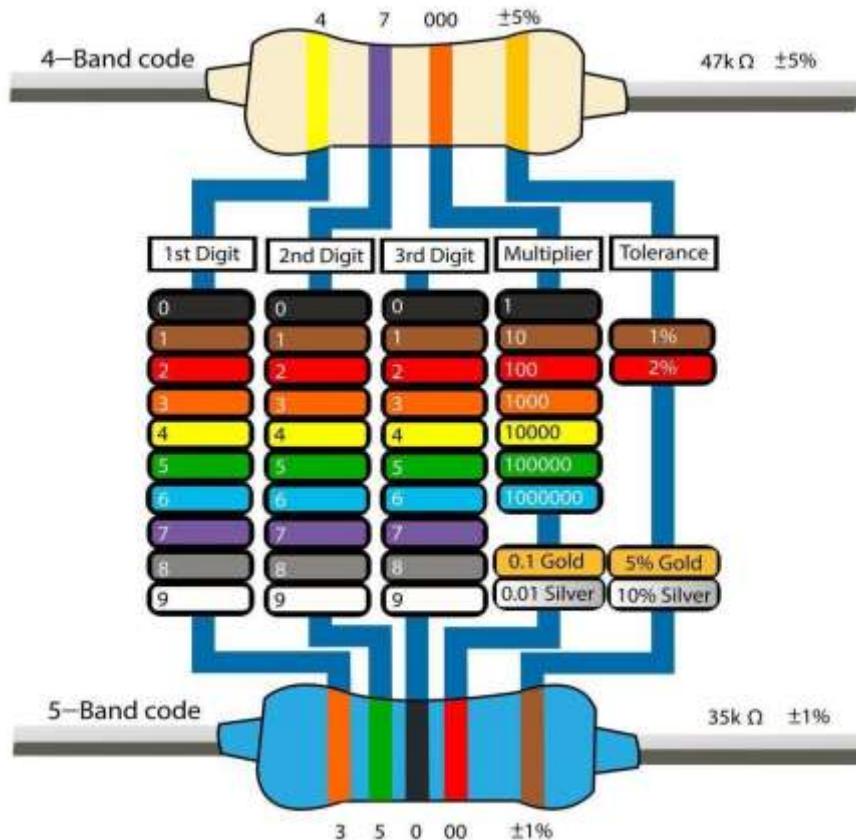


Fig. 3. Resistor color code table

1.3 Capacitors

polarized and nonpolarized capacitors

- Polarized capacitors
 - Polarized capacitor is shown in Fig. 4(a) Silver band (or polarity band) on the capacitor represents negative terminal
 - The capacitance value and the voltage ratings are written on the capacitor

- The polarized capacitor symbol is shown in Fig. 4(b), where the curve line indicates the negative terminal, and the straight line indicates the positive terminal.

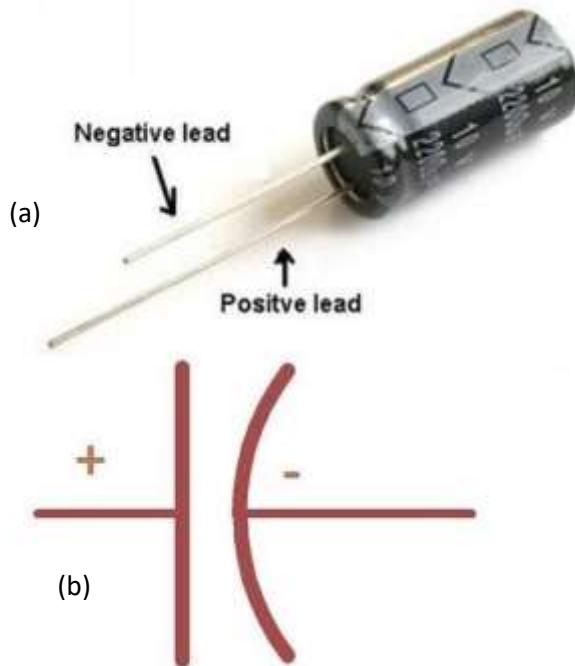


Fig. 4 (a) Polarized capacitor (b) Capacitor symbol

- Nonpolarized capacitors o Nonpolarized capacitor is shown in Fig. 5.



Fig. 5 Nonpolarized capacitor

1.4 Oscilloscope

- 4 channel digital storage oscilloscope model is shown in Fig. 6.
- Some of the commonly used features are auto scale, run control keys, measure controls, USB port, Analog channel input, Demo2 and ground, horizontal controls, vertical controls, entry knob, and file keys.

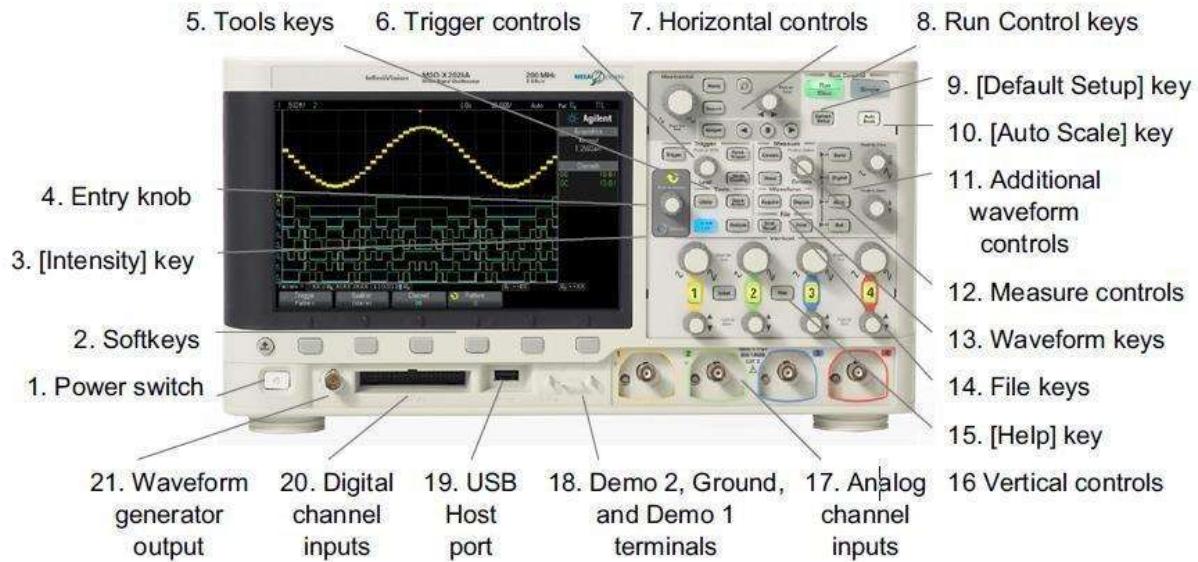


Fig. 6 Oscilloscope

- Entry knob: The Entry knob is used to select items from menus and to change values. The function of the Entry knob changes based upon the current menu and softkey selections. Note that the curved arrow symbol above the entry knob illuminates whenever the entry knob can be used to select a value.
- Horizontal controls: The Horizontal controls consist of
 - Horizontal scale knob — Turn the knob in the Horizontal section that is marked to adjust the time/div (sweep speed) setting.
 - Horizontal position knob — Turn the knob marked to pan through the waveform data horizontally. You can see the captured waveform before the trigger (turn the knob clockwise) or after the trigger (turn the knob counterclockwise). If you pan through the waveform when the oscilloscope is stopped (not in Run mode) then you are looking at the waveform data from the last acquisition taken.
- Run Control keys: When the [Run/Stop] key is green, the oscilloscope is running, that is, acquiring data when trigger conditions are met. To stop acquiring data, press [Run/Stop]. When the [Run/Stop] key is red, data acquisition is stopped. To start acquiring data, press [Run/Stop].

- [Auto Scale] key: When you press the [Auto Scale] key, the oscilloscope will quickly determine which channels have activity, and it will turn these channels on and scale them to display the input signals.
- Measure controls: The measure controls consist of:
 - Cursors knob — Push this knob select cursors from a popup menu. Then, after the popup menu closes (either by timeout or by pushing the knob again), rotate the knob to adjust the selected cursor position.
 - [Cursors] key — Press this key to open a menu that lets you select the cursors mode and source.
 - [Meas] key — Press this key to access a set of predefined measurements.
- File keys: Press the [Save/Recall] key to save or recall a waveform or setup.
- Vertical controls: The Vertical controls consist of:
 - Analog channel on/off keys — Use these keys to switch a channel on or off, or to access a channel's menu in the softkeys. There is one channel on/off key for each analog channel.
 - Vertical scale knob — There are knobs marked for each channel. Use these knobs to change the vertical sensitivity (gain) of each analog channel.
 - Vertical position knobs — Use these knobs to change a channel's vertical position on the display. There is one Vertical Position control for each analog channel.
- Analog channel inputs: Attach oscilloscope probes or BNC cables to these BNC connectors. In the InfiniiVision 2000X-Series oscilloscopes, the analog channel inputs have $1\text{ M}\Omega$ impedance.
- Demo 2, Ground, and Demo 1 terminals:
 - Demo 2 terminal — This terminal output the Probe Comp signal which helps you match a probe's input capacitance to the oscilloscope channel to which it is connected.
 - Ground terminal — Use the ground terminal for oscilloscope probes connected to the Demo 1 or Demo 2 terminals.
- USB Host port: This port is for connecting USB mass storage devices or printers to the oscilloscope. Connect a USB compliant mass storage device (flash drive, disk drive, etc.) to save data and screen images.

1.5 Function Generator

- Sine, square, pulse, ramp, and triangle waveforms can be generated.
- Enter amplitude, frequency for the signals
- Connect the BNC probe to the output
- One of the commonly used function generators with its components is shown in Fig. 7.

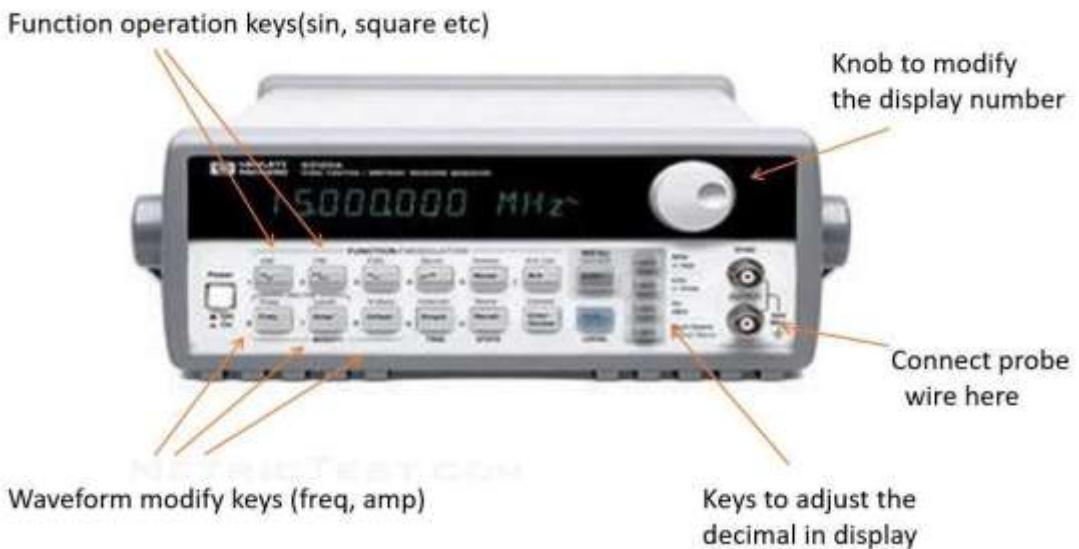


Fig. 7 Function generator

1.6 Multimeter

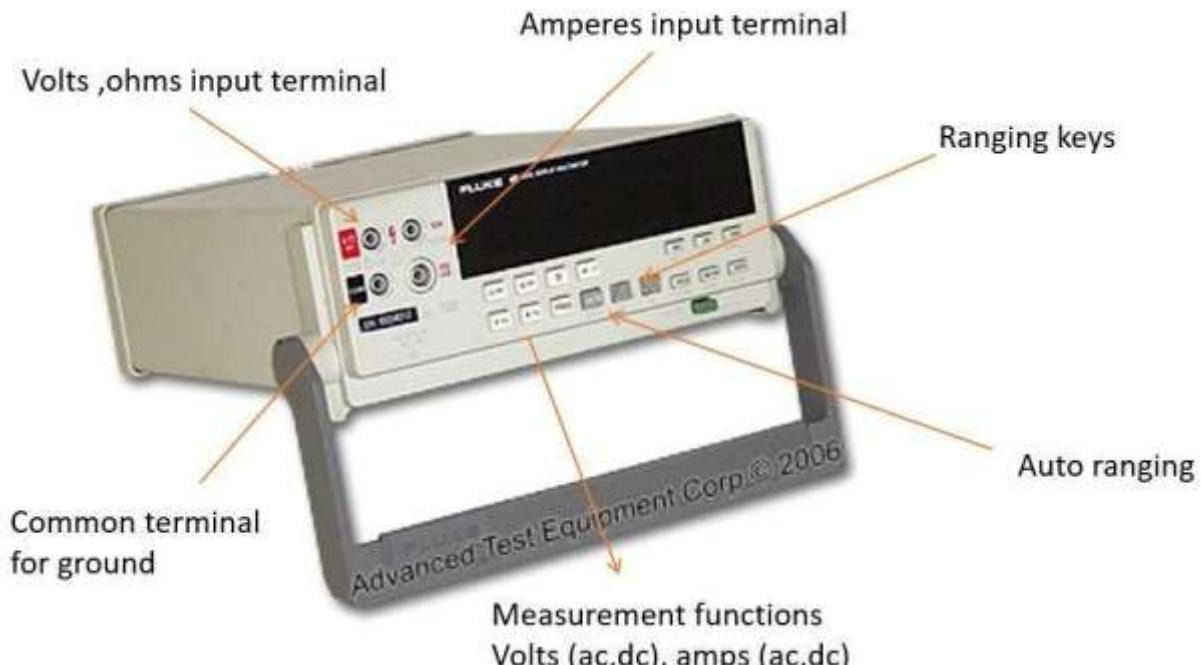


Fig. 8 Multimeter

1.7 Power supply

- Variac – to supply AC power



Fig. 9 Variac

- DC power supply



Fig. 10 Dual channel DC power supply

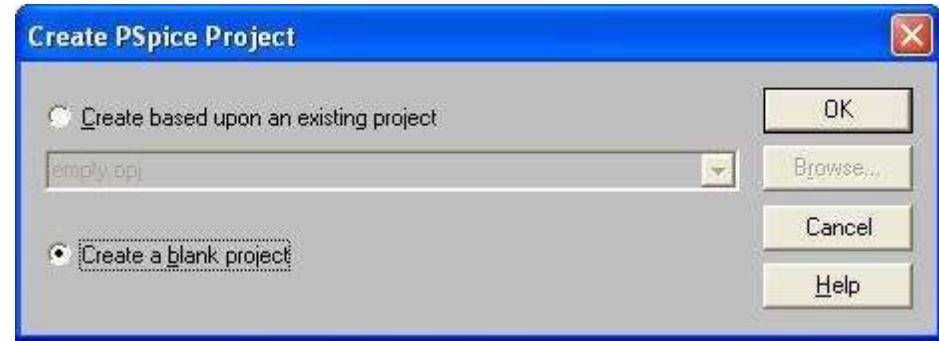
2- PSpice Software

2.1 How to Start

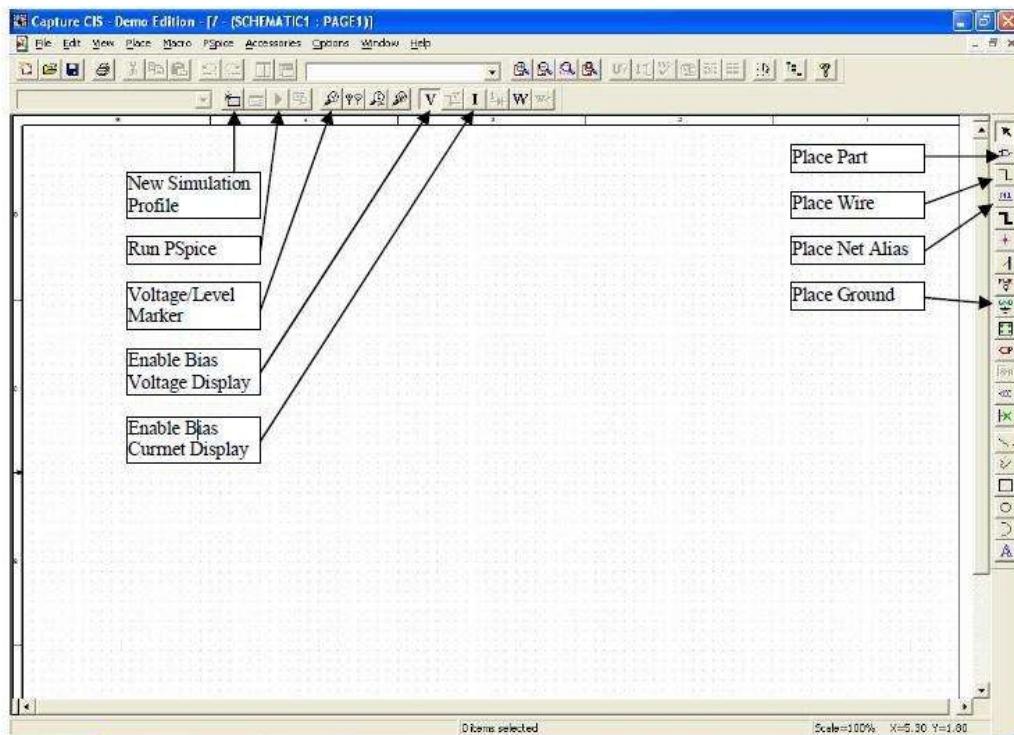
- Open PSpice CIS capture
- File → New → Project



- Enter a file name
- Select “Analog or Mixed A/D” and to specify the location click on browse and select the file location where you want to save the files.
- Click **OK** to create the new project.

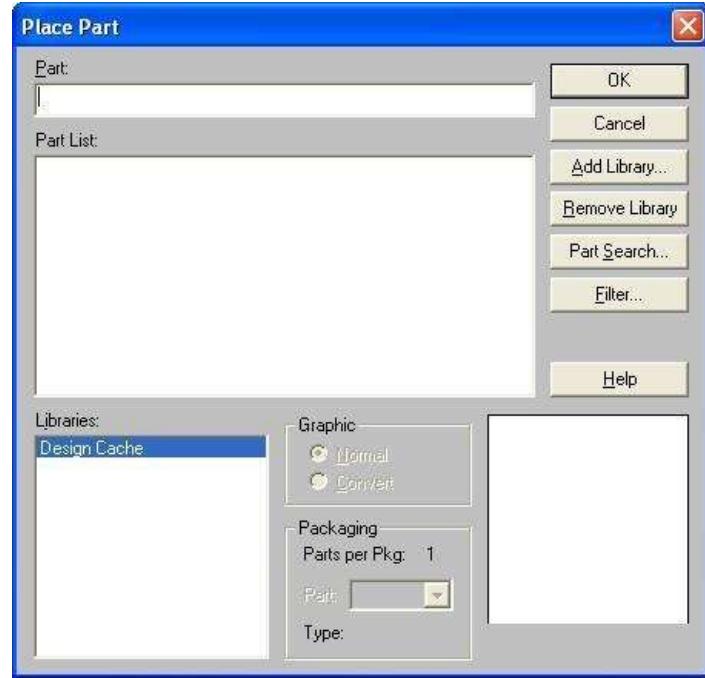


- Select **Create a blank project**. Click OK. This will open the schematic editor.

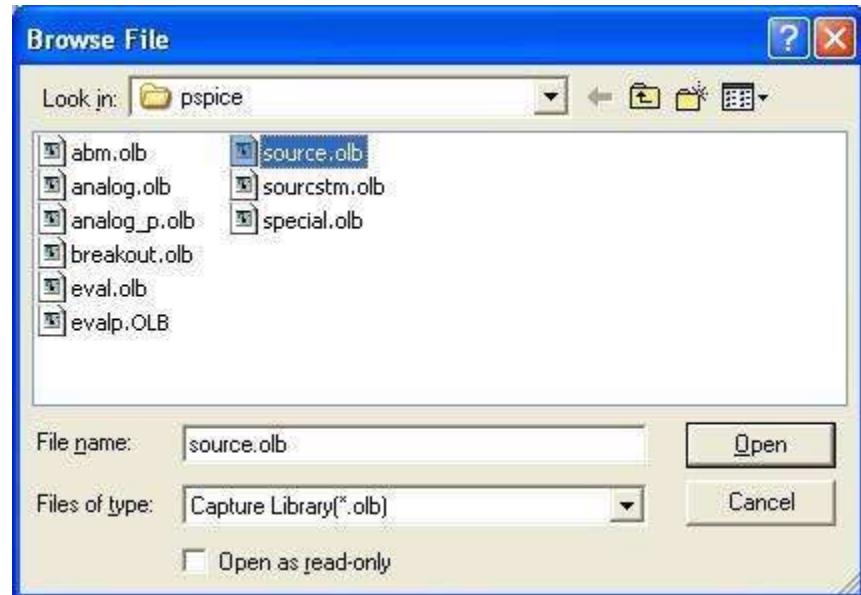


Schematic Editor with all the buttons used in this tutorial labeled.

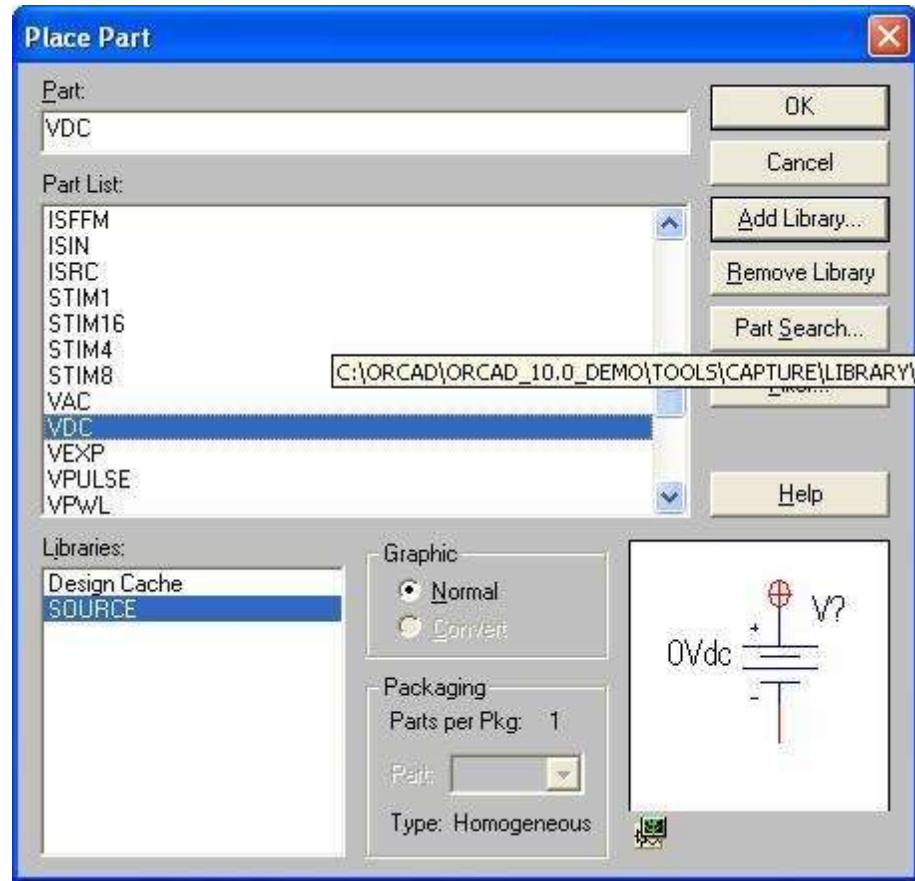
- After the schematic editor opens, select the Place Part tool by clicking on the second button on the vertical toolbar on the right side shown above.



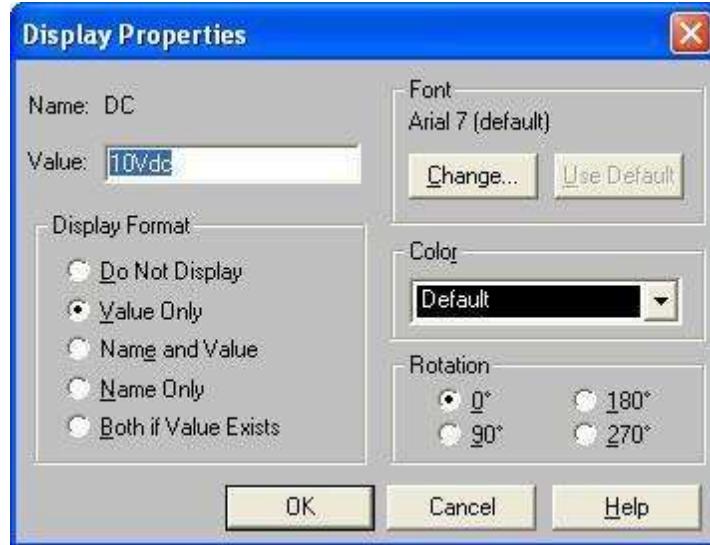
- Select Add Library...



- Ctrl+A and click on Open

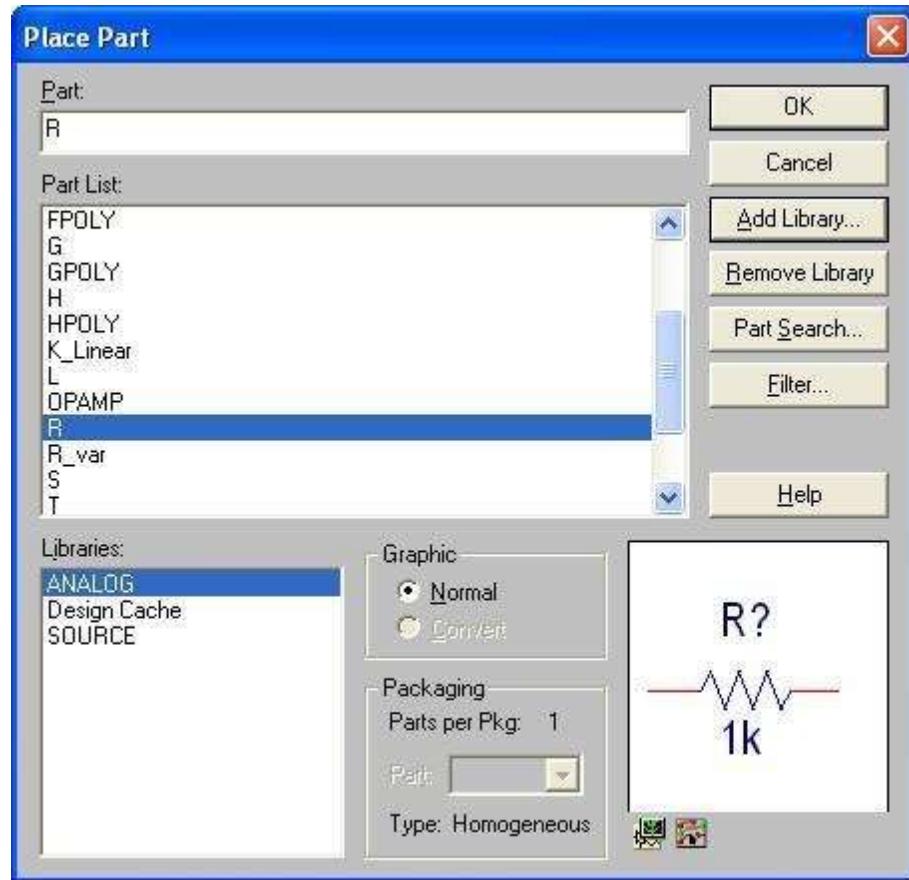


- On this screen select a battery (VDC) then **OK**. Place the battery on the work area by clicking on the blank schematic page and click ESC to stop placing DC sources. Then double click on 0VDC to change the DC voltage. The following dialog box will be displayed:

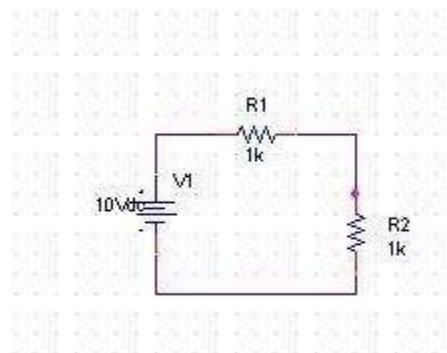


- Change value to 10VDC and then click **OK**.

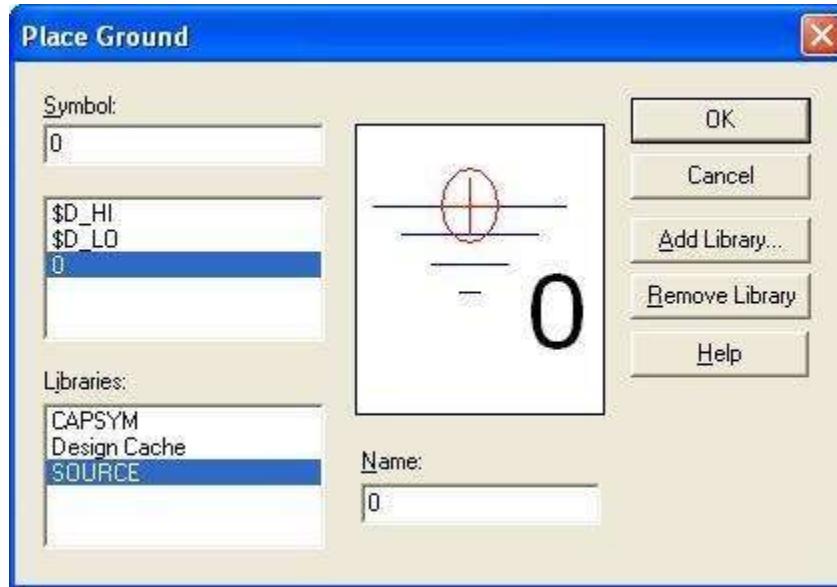
- Select the **ANALOG** library and select **R** from the **Part List**. Click **OK**.



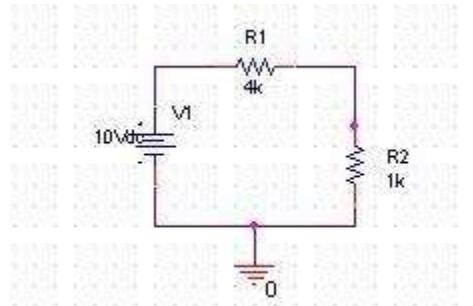
- Place two resistors in the work space. To stop placing parts, press ESC or right click an item and select “End Mode”. To rotate a part, select the part and press ‘r’ or right click and select rotate from the drop-down menu. If you need to delete a part, select the part and press the Delete key.
- To connect the items in the circuit, select the **Place Wire** tool by clicking on the third button from the top on the vertical toolbar on the right side. Drag the mouse between the terminals of your placed parts to connect them.



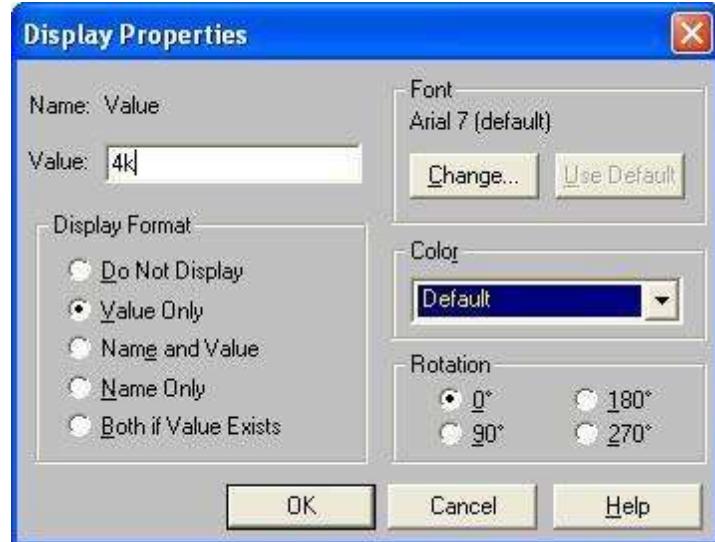
- For PSpice to simulate your circuit, it must have a “zero” node for a ground. To add this ground, select the **Place Ground** tool by clicking on the 9th button from the top on the vertical toolbar on the right side. The following dialog box will appear.



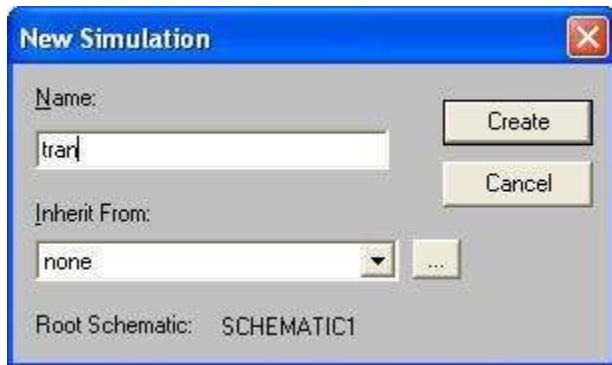
- Select the **SOURCE** Library and the **0** Symbol followed by **OK**.
- Place the ground for your circuit by clicking on the schematic page and connect it with the **Place Wire** tool. Your diagram should look like this:



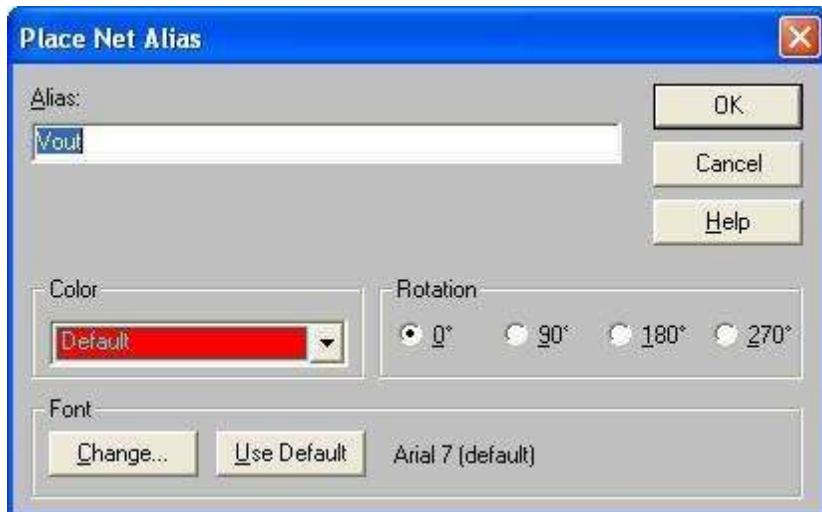
- To change the value for an item, double click the value you want to change and enter the value you want on the dialog box that appears. Double click on the **1k** value of the horizontally placed resistor and change the **Value** to **4k** as shown below.



- It is important to name the nodes you want to plot in PSpice so you can find them easily.

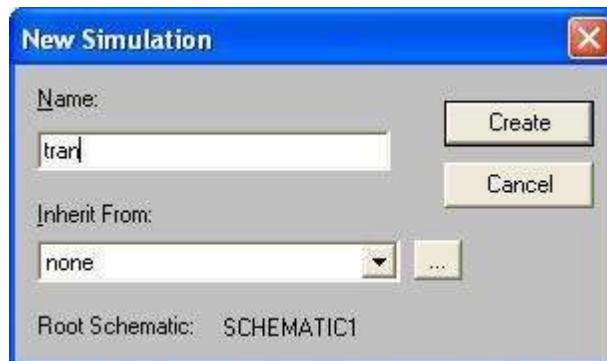


- To name a node, select the **Place Net Alias** tool and the following dialog box appears. Change the **Alias** to Vout and click **OK**.

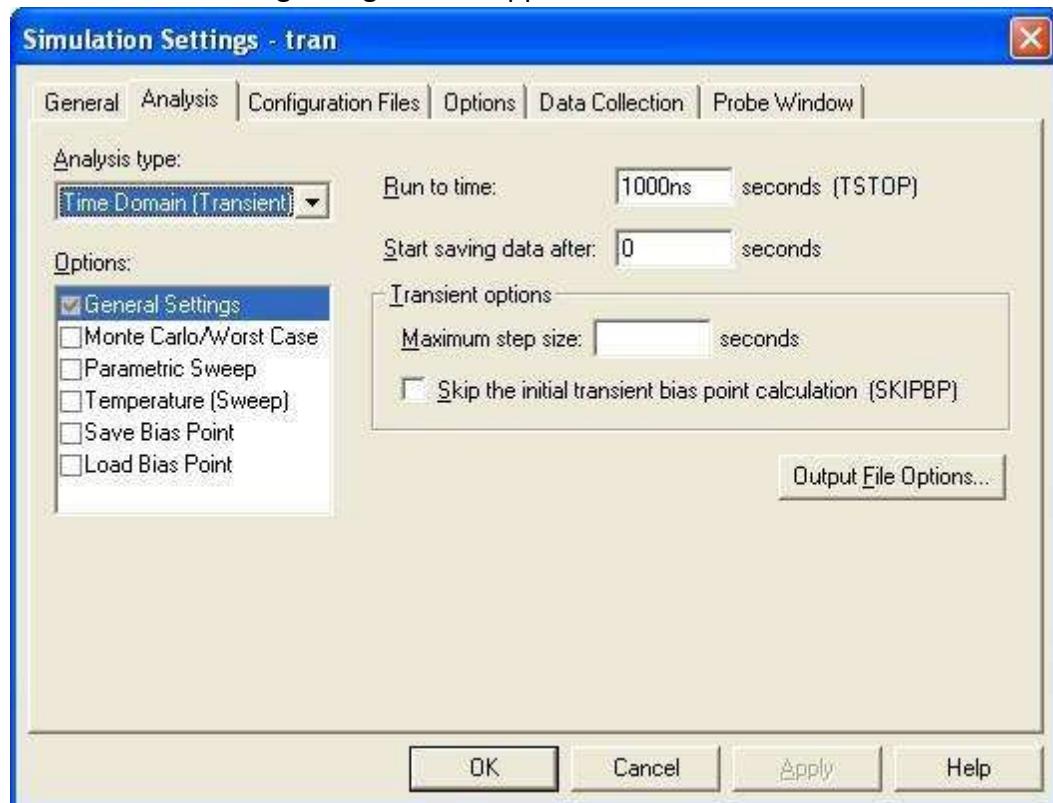


- Then place the alias on the desired node for Vout (i.e. the junction of the 2 resistors).

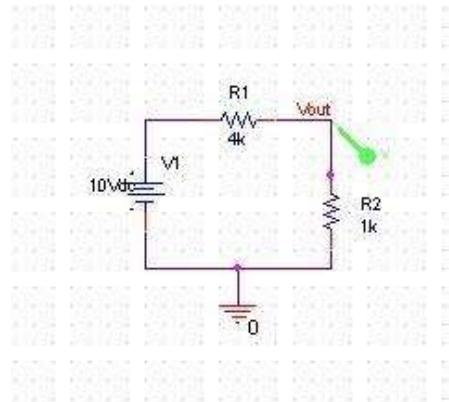
- Next, configure the simulation by clicking the **New Simulation Profile** button on the top toolbar. Enter the **Name** tran as shown below.



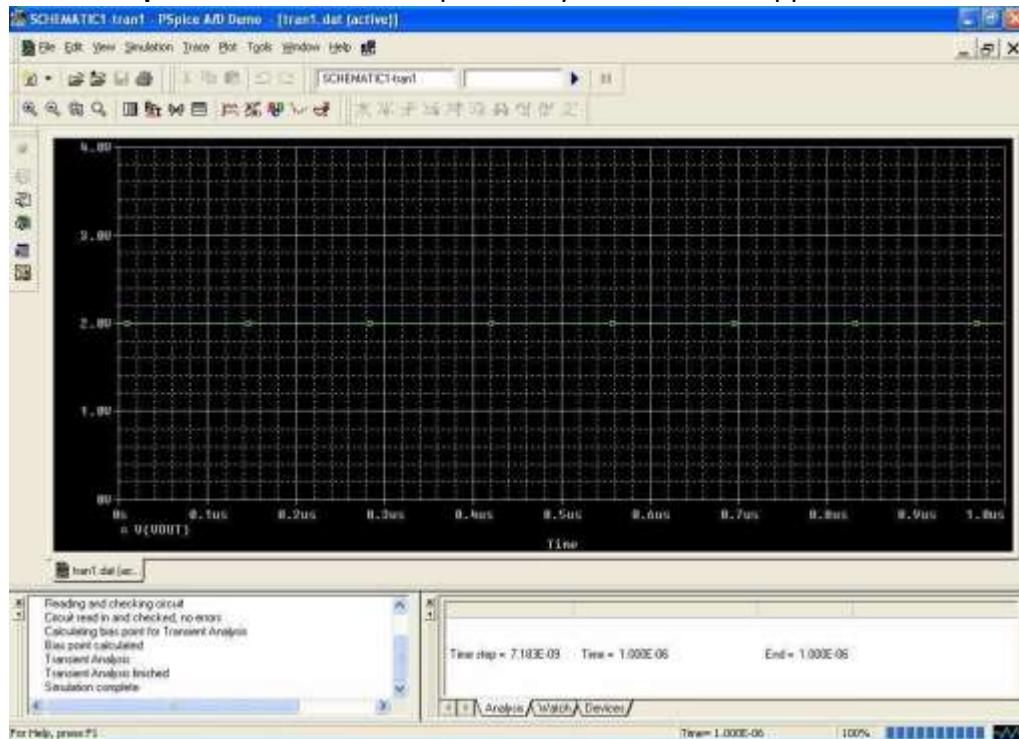
- Click **Create** and the following dialog box will appear.



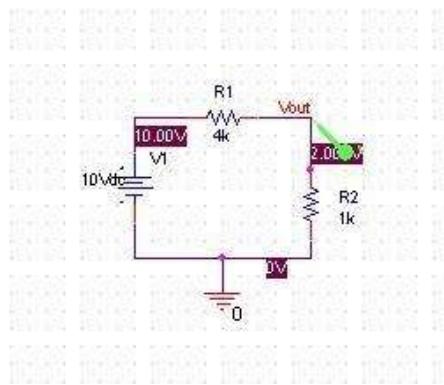
- Click **OK** to accept the default settings of the **Time Domain (transient)** analysis.
- From the top menu select **PSpice _ Create Netlist**. This is only necessary so that you can add the **Voltage Level Marker**.
- Click on the **Voltage/Level Marker** button to add a marker to the Vout node by clicking on it as shown below.



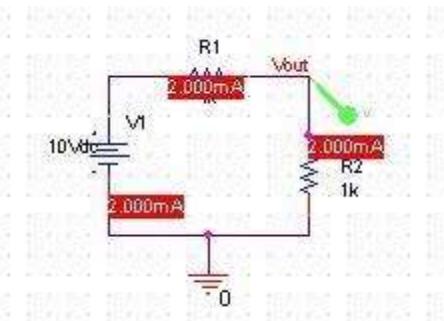
- Click the **Run PSpice** button and the PSpice Analysis results will appear as shown below.



- This automatically plots nodes with Voltage (or Current) markers on them. In this case, the voltage divider gives you 2V for Vout.
- Close the PSpice window. On the schematic, click the **Enable Bias Voltage Display** button to see all the DC voltages in the circuit as shown below.

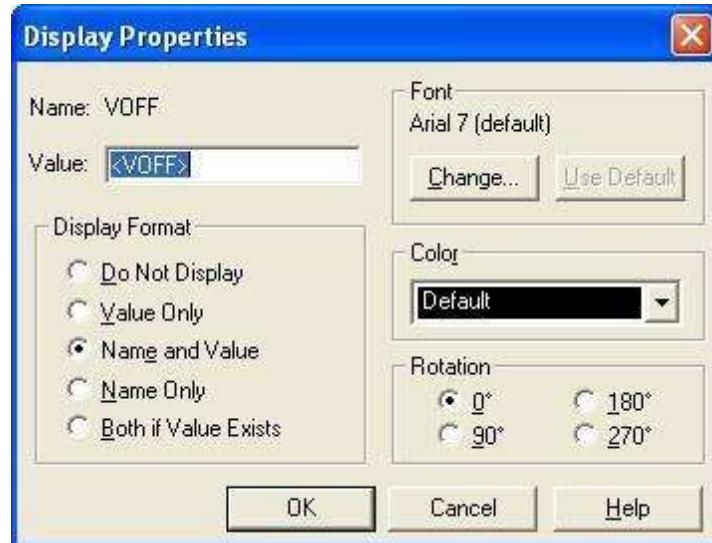


- On the schematic, click the **Enable Bias Voltage Display** button to toggle it off. Then, click on the **Enable Bias Current Display** button to see all the DC current(s) in the circuit as shown below.

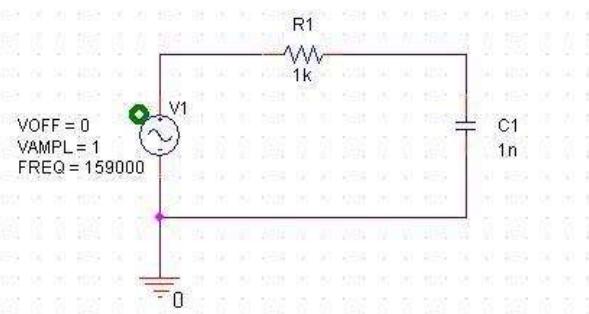


2.2 Transient Analysis:

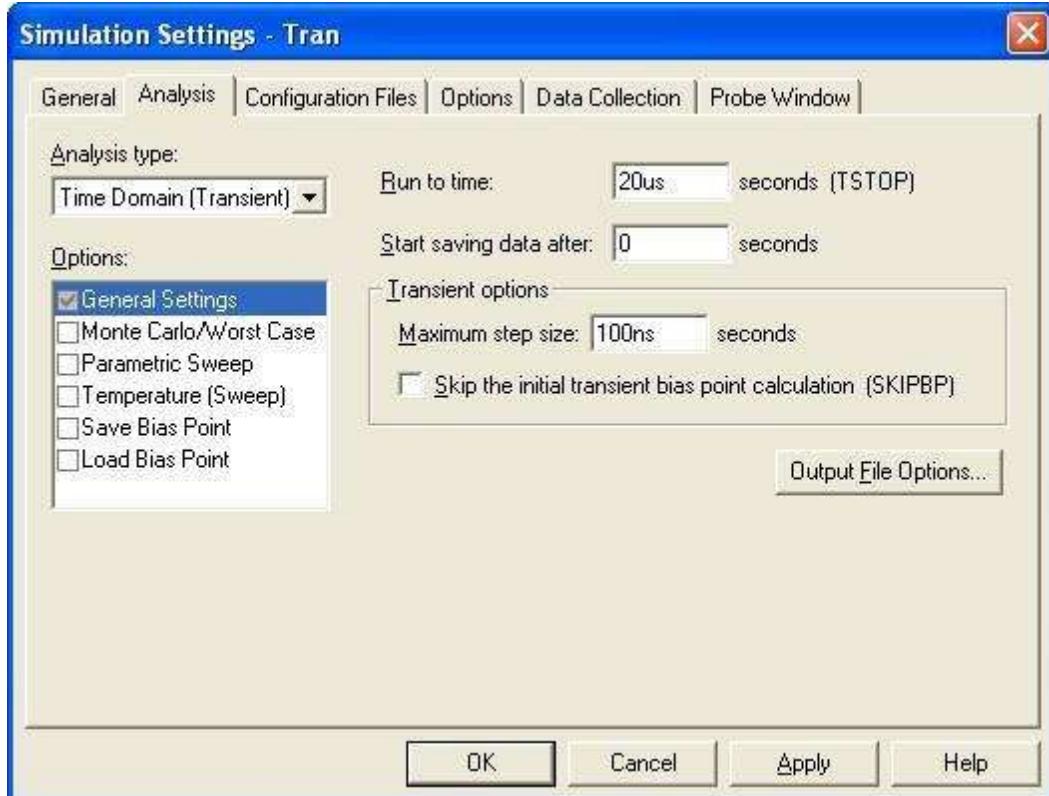
- For this circuit, select and wire these components: Capacitor (Place Part C in ANALOG library), Resistor (Place Part R in ANALOG library), Sinusoidal Source (Place Part VSIN in SOURCE library), and Ground (Place Ground 0 SOURCE library). Double click on the VOFF attribute of the VSIN component. The dialog box shown below should appear.



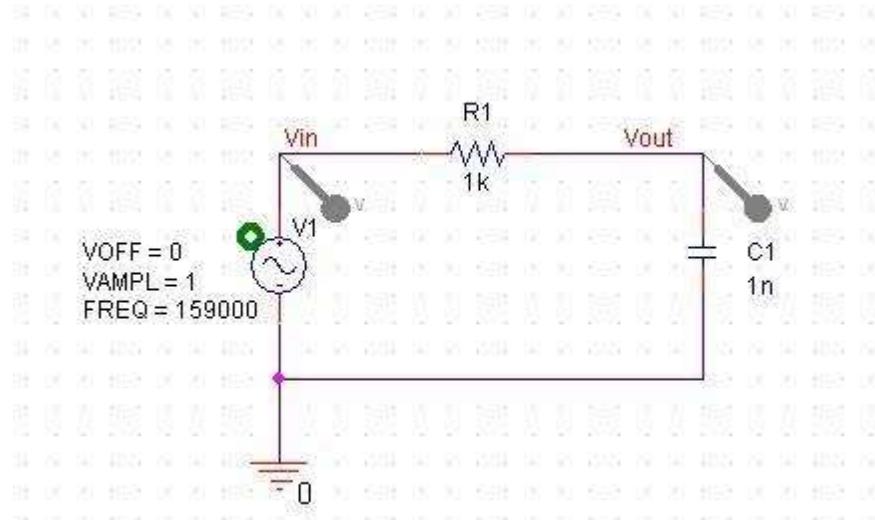
- Change the value from **<VOFF>** to 0. Click OK. Similarly, set the **VAMPL** attribute to 1 and the **FREQ** attribute to 159000. ($1/(2\pi R C)$). This circuit is shown below:



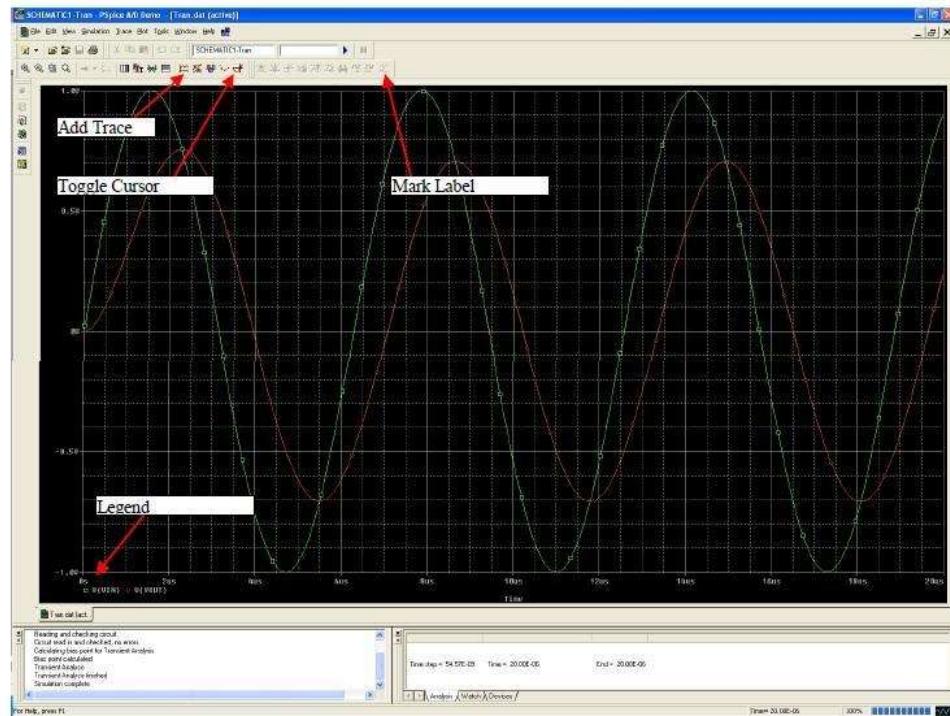
- Next, configure the simulation by clicking the **New Simulation Profile** button on the top toolbar. Enter the **Name** Tran and the following dialog box will appear. Set Analysis type: **Time Domain (transient)**, **Run To Time**: 20us, and **Maximum Step Size** to 100ns. Click **OK**.



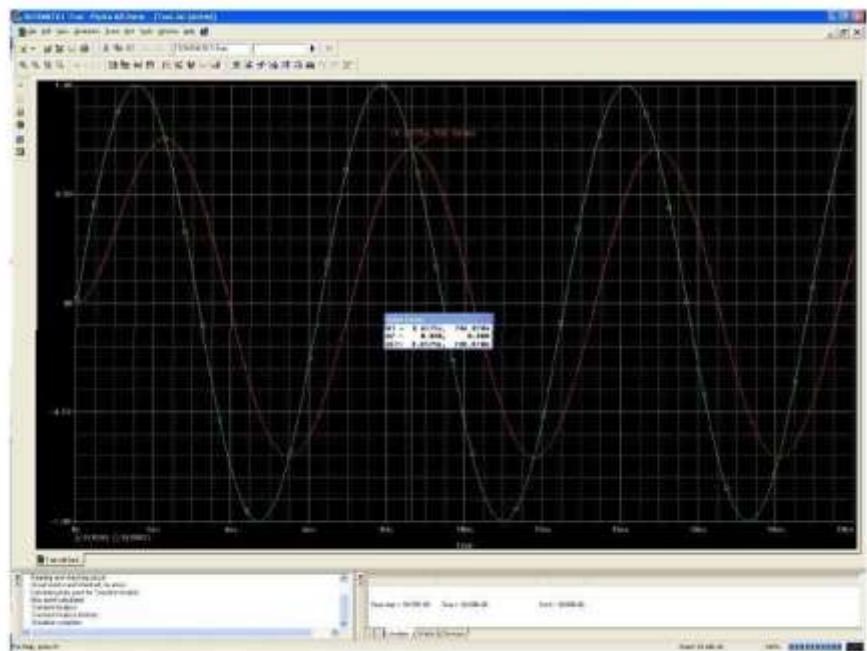
- Click on the **Voltage/Level Marker** button and place a marker at the junction of the **R** and **C** and at the junction between the **Source** and the **R**. If you are unable to place the marker, you need to create the netlist first (**PSpice _ Create Netlist**). Give the junction between the **R** and **C** the Alias of **Vout** using the **Net Alias** tool as shown below. Give the junction between the **Source** and the **R** the alias **Vin**. This circuit is shown below:



- Click the **Run PSpice** button and the PSpice Analysis results will appear as shown below.



- Click the **Toggle Cursor** button to display the cursors and the **Probe Cursor** window. Left mouse click on the red dot in the legend next to $V(Vin)$. This will assign the left mouse button to the V_{out} trace. Drag the mouse using the left mouse button to 2nd peak of V_{out} and note the amplitude. It should be 3dB smaller than V_{in} (0.707V). Click on the **Mark Label** button to label that point as shown below.



3 – Diode Rectifier Circuits

3.1 Diode

- Diodes are small two-terminal which conducts current when forward biased and blocks current flow when reverse biased.

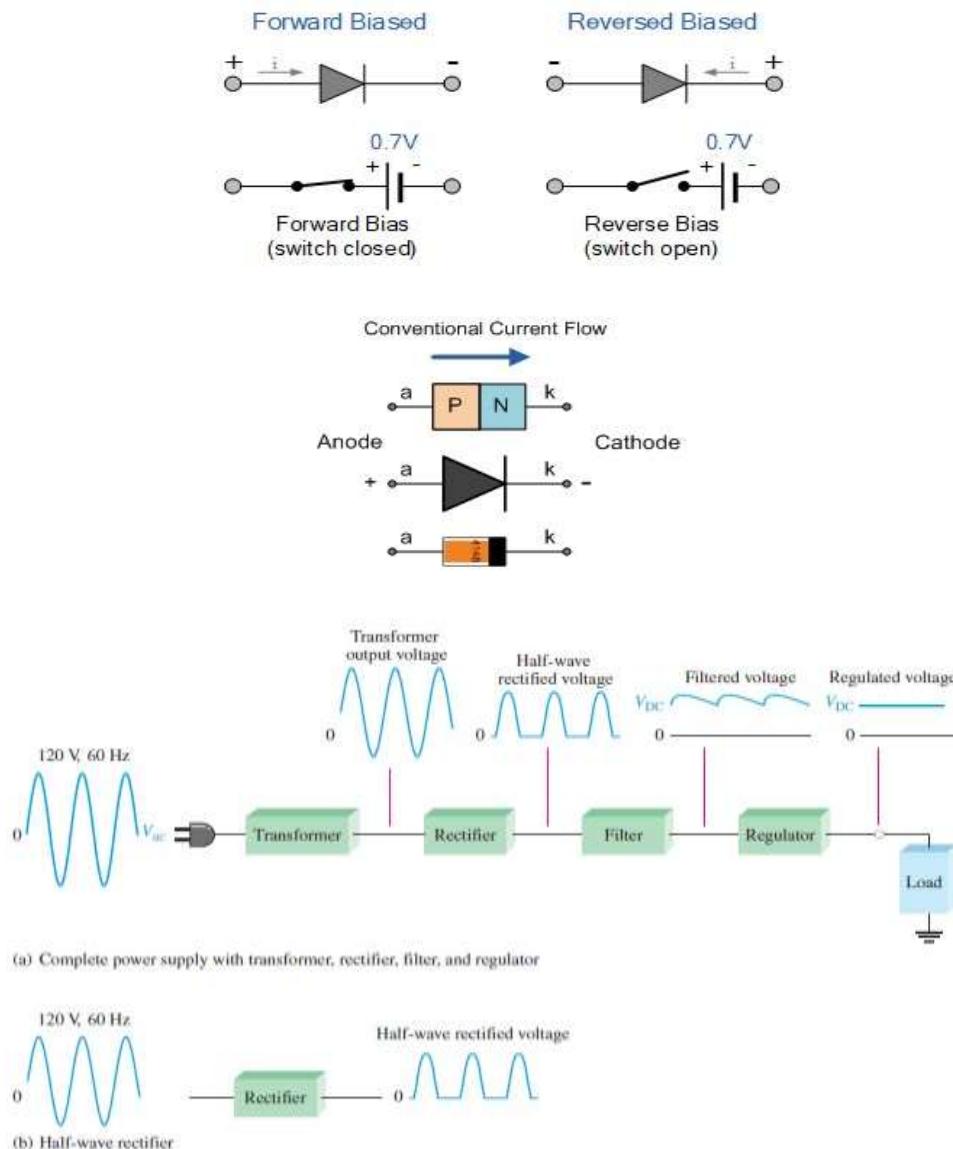
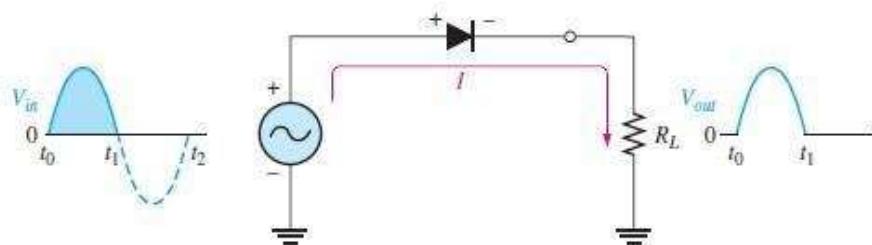


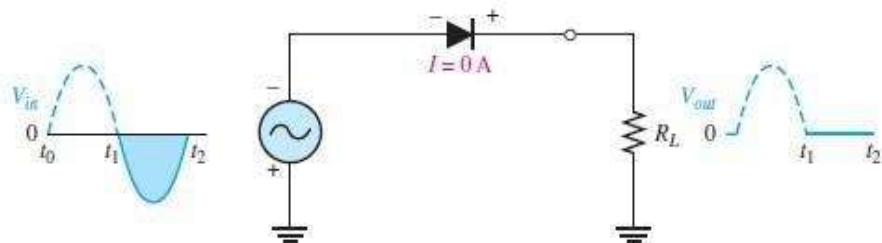
Fig. 11 Block diagram of DC power supply with a load and a rectifier

3.2 Half-wave rectifier operation

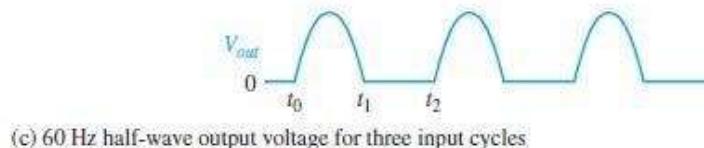
- When an input sine positive half cycle goes through the diode, the diode acts as a closed circuit and the current pass through it as shown in Fig 12(a)
- The current produces an output voltage across the load R_L , which has the same shape as the positive half-cycle of the input voltage.
- When the input voltage goes negative during the second half of its cycle, the diode is reverse-biased. There is no current, so the voltage across the load resistor is 0 V, as shown in Fig. 12 (b). The net result is that only the positive half-cycles of the ac input voltage appear across the load. Since the output does not change polarity, it is a pulsating dc voltage with a frequency of 60 Hz, as shown in part Fig. 12(c).



(a) During the positive alternation of the 60 Hz input voltage, the output voltage looks like the positive half of the input voltage. The current path is through ground back to the source.



(b) During the negative alternation of the input voltage, the current is 0, so the output voltage is also 0.



(c) 60 Hz half-wave output voltage for three input cycles

Fig. 12 Half wave rectifier operation

- When the practical diode model is used then the barrier potential of 0.7 V is considered. During the positive half-cycle, the input voltage must overcome the barrier potential before the peak value of the input, as shown in Figure 2–23. The expression for the peak output voltage is

$$(out) = V_{p(in)} - 0.7V \quad (1)$$

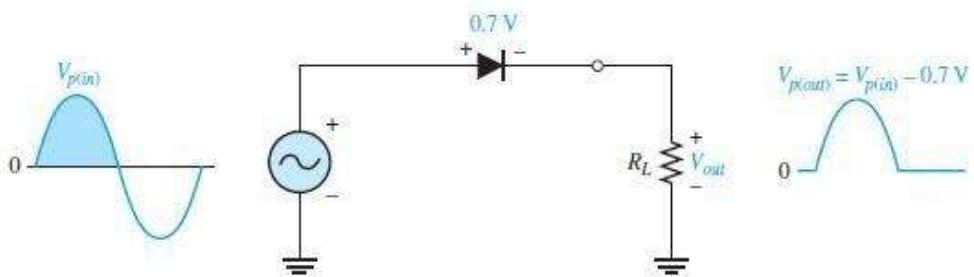


Fig. 13 Effect of potential barrier on the half wave rectifier

- The DC output voltage is derived using average value of the half wave output voltage.
- Average value is determined mathematically by finding the area under the curve over a full cycle as shown in fig. 2.3, and then dividing by 2π , the number of radians in a full cycle.

$$V_{AVG} = \frac{V_p}{\pi} \quad (2)$$

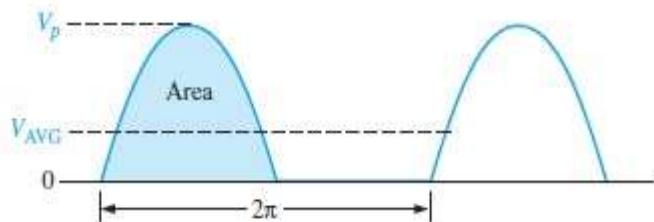


Fig. 14 Average value of the half-wave rectified signal

- When the sine input is replaced by the transformer. A transformer is often used to couple the ac input voltage from the source to the rectifier as shown in Fig. 2.4
- Figure 15 is similar to the schematic circuit given in Experiment 2, Figure 2-1 (a).

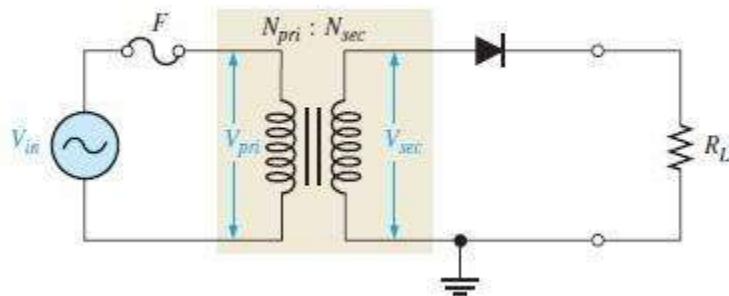


Fig. 15 Half wave rectifier with transformer

- The source voltage 120V AC from the transmission line is stepped down using a stepdown transformer to lower voltage.
- The secondary voltage of a transformer equals the turns ratio, n , times the primary voltage.

$$V_{sec} = n V_{pri} \quad (3)$$

- When $n=1$, then

$$V_{sec} = V_{pri} \quad (4)$$

On using (1), (2), and (4), the DC output voltage is

$$V_{out} = V_{out} = \frac{V_p - 0.7}{\pi} \quad (5)$$

3.3 Center-Tapped full wave rectifier operation

- Figure 16 is similar to the schematic diagram shown in experiment 2 Figure2-1(b).
- A center-tapped rectifier is a type of full-wave rectifier that uses two diodes connected to the secondary of a center tapped transformer, as shown in Figure 16. The input voltage is coupled through the transformer to the center-tapped secondary. Half of the total secondary voltage appears between the center tap and each end of the secondary winding as shown.

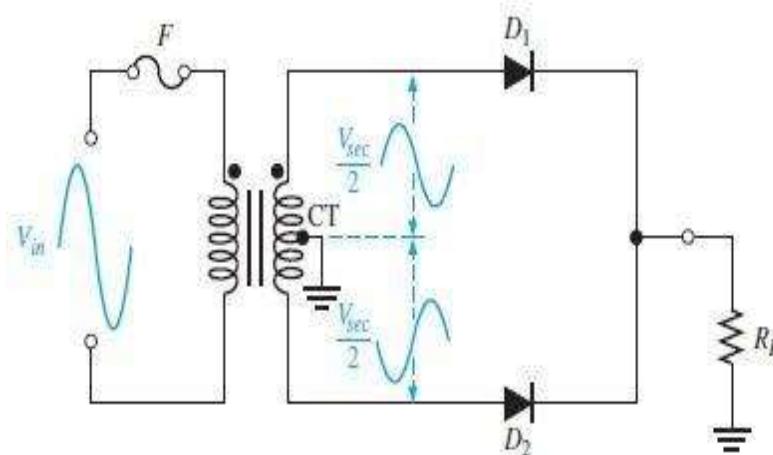
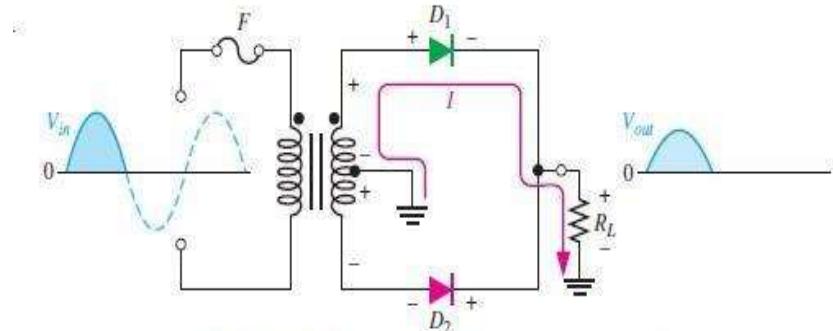


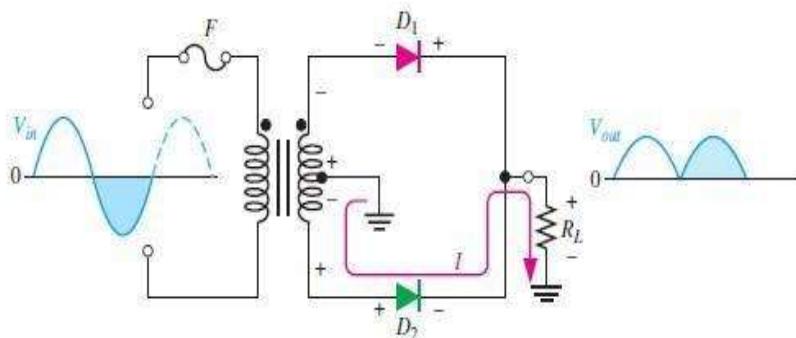
Fig. 16 Center-tapped full rectifier

- For a positive half-cycle of the input voltage, the polarities of the secondary voltages are as shown in Figure 17(a). This condition forward-biases diode D_1 and reverse-biases diode D_2 . The current path is through D_1 and the load resistor R_L , as indicated. For a negative half cycle of the input voltage, the voltage polarities on the secondary are as shown in Figure 17(b). This condition reverse-biases D_1 and forward-biases D_2 . The current path is through D_2 and R_L , as indicated. Because the output current during both the positive and negative

portions of the input cycle is in the same direction through the load, the output voltage developed across the load resistor is a full-wave rectified dc voltage, as shown.



(a) During positive half-cycles, D_1 is forward-biased and D_2 is reverse-biased.



(b) During negative half-cycles, D_2 is forward-biased and D_1 is reverse-biased.

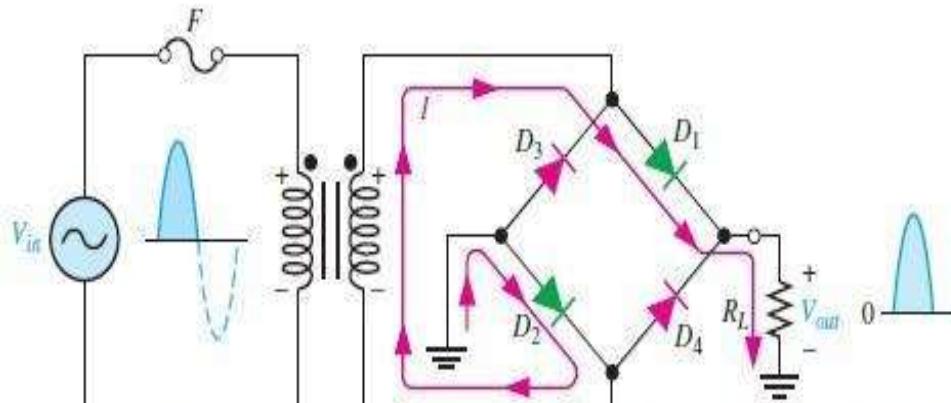
Fig 17 Center-tapped full wave rectifier operations

- For the center-tapped transformer the turns ratio $n=2$.
- The DC output voltage is given as

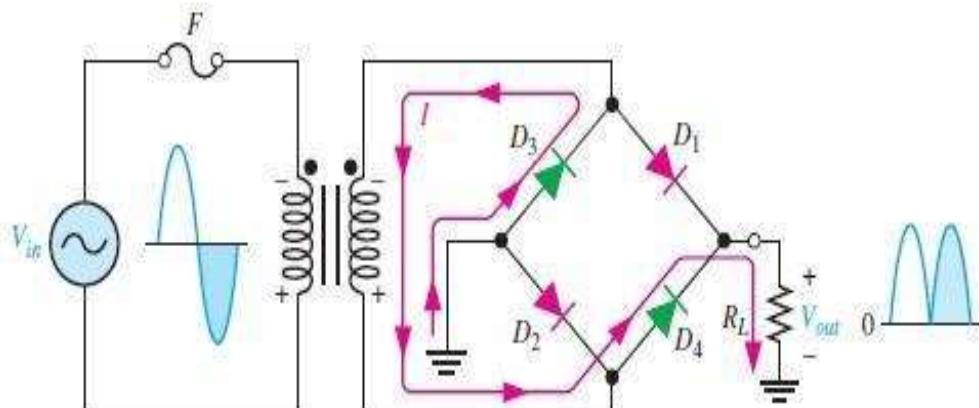
$$V_{out} = \frac{V_{in}}{\pi} \quad (6)$$

3.4 Full wave bridge rectifier:

- Figure 18 is similar to the schematic diagram shown in experiment 3 Figure 3-1(a).
- The **bridge rectifier** uses four diodes connected as shown in Figure 18. When the input cycle is positive as in part (a), diodes D_1 and D_2 are forward-biased and conduct current in the direction shown. A voltage is developed across RL that looks like the positive half of the input cycle. During this time, diodes D_3 and D_4 are reverse-biased.



(a) During the positive half-cycle of the input, D_1 and D_2 are forward-biased and conduct current. D_3 and D_4 are reverse-biased.



(b) During the negative half-cycle of the input, D_3 and D_4 are forward-biased and conduct current. D_1 and D_2 are reverse-biased.

Fig. 18 Operation of full wave bridge rectifier

- When the input cycle is negative as in Figure 18(b), diodes D_3 and D_4 are forward biased and conduct current in the same direction through R_L as during the positive half-cycle. During the negative half-cycle, D_1 and D_2 are reverse-biased. A full-wave rectified output voltage appears across R_L as a result of this action.
- The DC output voltage is given as

$$V_{out} = 2 * \frac{V_p - 0.7}{\pi} \quad (7)$$

3.5 Full wave bridge rectifier with filter

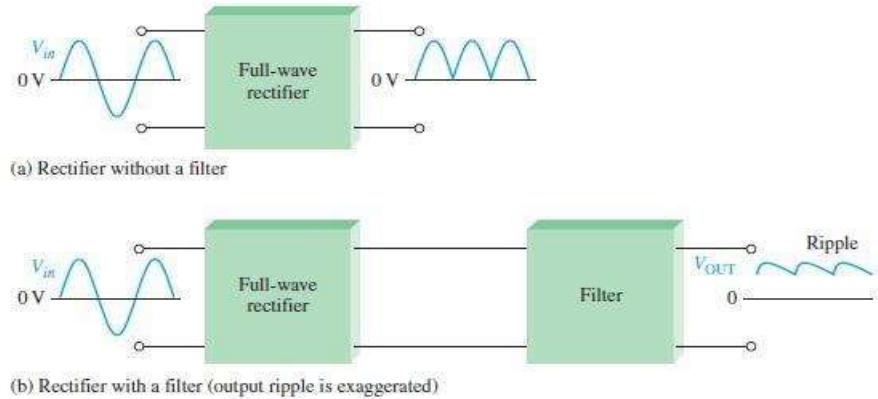
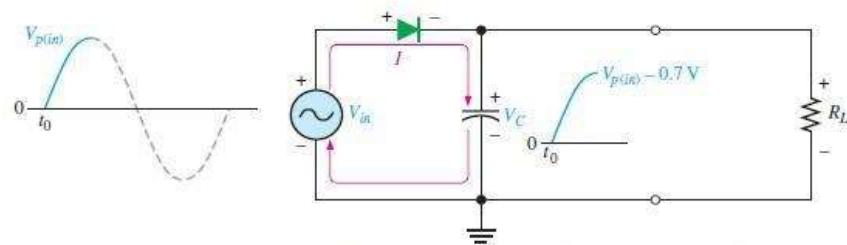
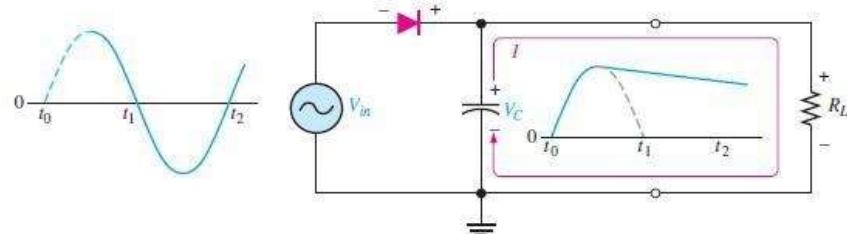


Fig. 19 Rectifier with filter

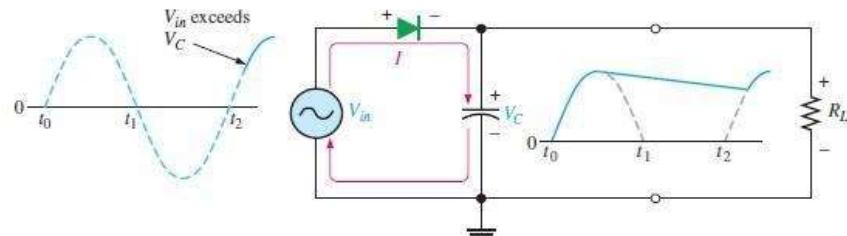
- During the positive first quarter-cycle of the input, the diode is forward-biased, allowing the capacitor to charge to within 0.7 V of the input peak, as illustrated in Figure 20(a). When the input begins to decrease below its peak, as shown in part (b), the capacitor retains its charge, and the diode becomes reverse-biased because the cathode is more positive than the anode. During the remaining part of the cycle, the capacitor can discharge only through the load resistance at a rate determined by the RLC time constant, which is normally long compared to the period of the input. The larger the time constant, the less the capacitor will discharge. During the first quarter of the next cycle, as illustrated in part (c), the diode will again become forward biased when the input voltage exceeds the capacitor voltage by approximately 0.7 V.



(a) Initial charging of the capacitor (diode is forward-biased) happens only once when power is turned on.



(b) The capacitor discharges through R_L after peak of positive alternation when the diode is reverse-biased. This discharging occurs during the portion of the input voltage indicated by the solid dark blue curve.



(c) The capacitor charges back to peak of input when the diode becomes forward-biased. This charging occurs during the portion of the input voltage indicated by the solid dark blue curve.

Fig. 20 Operation of half wave rectifier with capacitor filter

- The **ripple factor (r)** is an indication of the effectiveness of the filter and is defined as

$$r = \frac{V_{r(pp)}}{V_{DC}}$$

where $V_{r(pp)}$ is the peak-to-peak ripple voltage and V_{DC} is the dc (average) value of the filter's output voltage, as illustrated in Figure 21. The lower the ripple factor, the better the filter. The ripple factor can be lowered by increasing the value of the filter capacitor or increasing the load resistance.

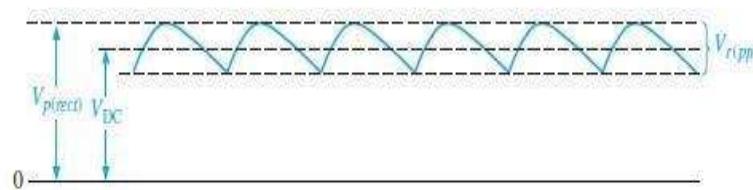


Fig. 21 V_r and V_{DC} determine the ripple factor

4- Prelab and Lab report

4.1 Prelab

- The prelab will consist of results obtained from circuit simulations using PSpice, and other preliminary calculations/derivations.
- Circuits for each prelab will be handed out or made available the week before.
- The prelab is due one day before a particular experiment is to be performed, at 23:59. Late Submissions are not accepted.

4.2 Lab report

- All lab recordings, including numerical data, waveforms, spectra, and other observations should be included in the lab report. Sketches or pictures of waveforms and spectra **must be labeled** with all relevant information such as axes, time, frequency, amplitude, etc. The sketches must be clean, clear and in proper scale.
- Analysis or explanation of data and waveforms compared with theoretical calculations should be included.
- Students must **not** copy from or refer to lab reports from previous years. Such copying will incur **severe penalty** in grade and appropriate disciplinary action.
- Each student is expected to record lab data and waveforms. Before the end of the session, you should present these to the instructor to verify your results.
- Lab report format is given below.

Lab Report Format:

The report for this laboratory is a semi-formal report which is a shortened version of a formal report. This report will be written to one who is somewhat familiar with the problem and who is to be informed of the results of the laboratory investigation.

Contents of a Report:

The contents of a laboratory report should, in general, include the following items in the same general order:

a. Title

b. Objective: A brief statement of the objective

c. Theory: Derivation and/or calculations of expected results.

d. Experiment: This is the main part of the report, and it includes interpretation of results and observations.

1. Procedure: Brief description of the procedure used. Circuits must be included in your report.
2. Data and Observations: Waveforms, frequencies, voltages, etc. should appear here. This includes snapshots from the oscilloscope and recorded data from Tables. Data must be plotted or tabulated where appropriate.
3. Calculations and Results: Complete calculation for each result (or a sample calculation for repeated calculations of the same type)
4. Comparisons: Comparisons of results with theoretical predictions and possible explanation of unexpected results and/or observations. Estimation of the error in the results where appropriate.
5. Comments: Difficulties encountered shortcomings of the method used, possible alternative, etc.

e. Conclusion A brief explanation of what was your conclusion of this experiment.

Lab 2

Diode Rectifier Circuits

PURPOSE AND BACKGROUND

The purpose of this experiment is to demonstrate the characteristics of two different diode rectifier circuits: a half-wave rectifier and a center-tapped full-wave rectifier. Each type of rectifier circuit causes an AC input voltage to be converted into a pulsed waveform.

REQUIRED PARTS AND EQUIPMENT

- ❖ 1 k Ω resistor (1/2 W)
- ❖ Four 1N4007 silicon rectifier diodes
- ❖ 12.6 V_{rms} secondary center-tapped transformer
- ❖ Dual trace oscilloscope
- ❖ DMM (preferred) or VOM
- ❖ 120 V Variac
- ❖ Breadboard

PROCEDURE

1. Wire the half-wave rectifier circuit shown in Figure 2-1, paying careful attention to the polarity of the 1N4007 diode. You should be very careful to make sure that your connections to the 120-V primary of the transformer are properly protected so that you will not get a shock by accidentally touching them. Furthermore, you should have a $\frac{1}{2}$ -A fuse on the primary side of the transformer. Note that neither of the transformer's primary leads are grounded, while the center-tapped secondary lead is not used in this section!
2. Set your oscilloscope to the following approximate settings:
 - a. Channels 1 and 2: 10 V/division, dc coupling
 - b. Time base: 5 ms/division

Apply 120 VAC (rms) to the transformer's primary leads. Connect one scope probe to the anode terminal of the IN4007 diode (point A), and the other probe to the terminal (point B). If everything is working properly, you should obtain the waveforms shown in Figure 2-2.

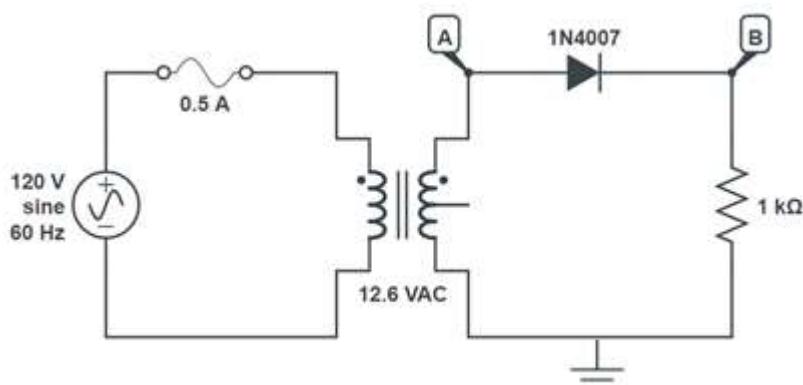


FIGURE 2-1: Schematic diagram of Half-wave rectifier circuit

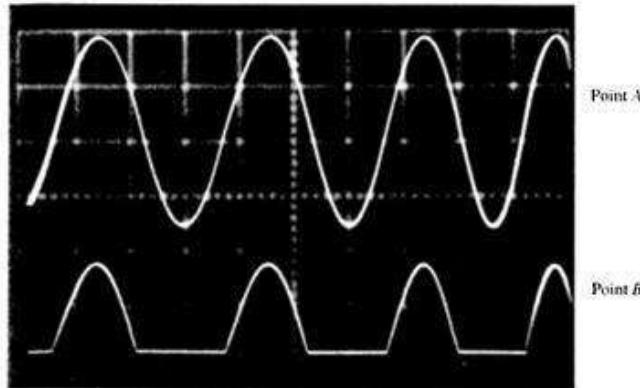


FIGURE 2-2: Time base: 5 ms/division

3. From the oscilloscope, measure the transformer's peak secondary voltage [V_s (peak)], as well as the peak voltage [V_o (peak)] across the 1-kΩ resistor, recording your results in Table 2-1. Are the two readings the same?
 - a. You should find that these two readings differ slightly. The voltage difference is the barrier potential of the diode (V_B), which is approximately 0.7 V for silicon diodes. When the peak voltage is at least ten times larger than this diode voltage drop, the barrier potential usually can be safely neglected, so that these two readings can be considered essentially the same for most calculations.
4. With your multimeter, measure the dc voltage (V_{DC}) across the 1-kΩ resistor, and record your result in Table 2-1. Compare this result with that obtained from the equation for the average or dc voltage of a half-wave rectifier (Equation 1)
 - a. Observe both waveforms. Notice that the frequency of the rectified output sine wave is the same as that of the input sine wave though half of each cycle of the output is zero. Why?
5. Turn off the power to the transformer and wire the center-tapped full-wave circuit shown in Figure 2-3. Again, pay careful attention to the polarity of both diodes and the connections to the 120-V primary of the transformer. The center-tapped lead is grounded for this section.

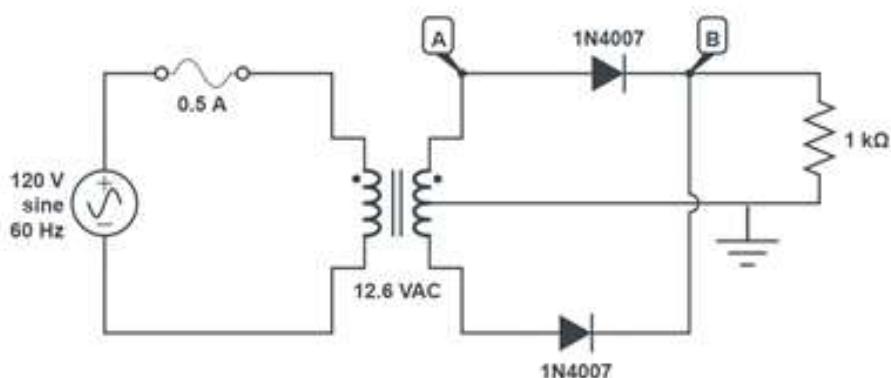


FIGURE 2-3: Schematic Diagram of Full-wave bridge rectifier circuit

6. Now set your oscilloscope to the following approximate settings:

- Channels 1 and 2: 5 V/division, dc coupling
- Time base: 5 ms/division

Apply 120 VAC (rms) to the transformer's primary leads. Connect one probe to the anode terminal for the IN4007 diode (point A) and the other probe to one of the diode's cathode terminals (point B). If everything is working properly, you should obtain the waveforms as shown in Figure 2-4.

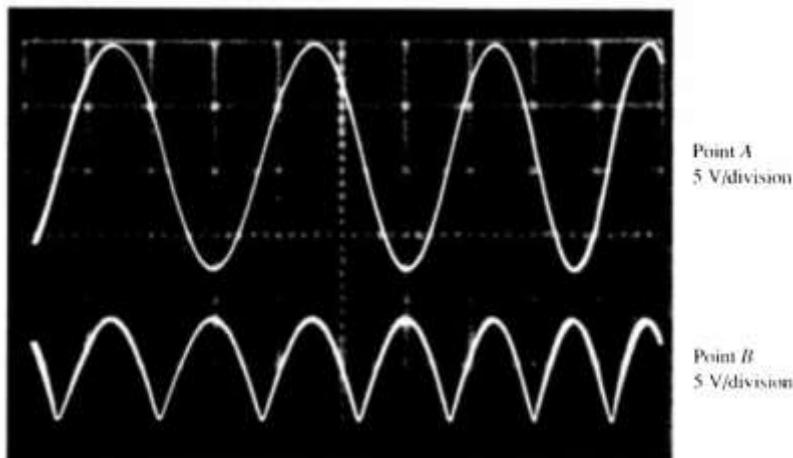


FIGURE 2-4: Time base: 5 ms/division

- With your oscilloscope, measure the transformer's peak secondary voltage (V_s) with respect to the grounded center tap, as well as the peak voltage V_o (peak) across the 1-k Ω resistor, recording your results in Table 2-1. How do these readings compare with those of Step 3? The peak secondary voltage should be half that of Step 3.
- With your multimeter measure the *dc* voltage (V_{DC}) across the 1-k Ω resistor and record your result in Table 2-1. Compare this result with that obtained from the equation for the average or *dc* voltage of a center-tapped full-wave rectifier (Equation 3).
 - Observe both waveforms. Notice that the frequency of the rectified output sine wave is now twice that of the input since wave. Why?

FOR FUTURE INVESTIGATION (OPTIONAL)

Reverse the diodes for both rectifier circuits and repeat Steps 1 through 8. Compare the waveforms for each circuit with those of the original circuit.

WHAT YOU HAVE DONE

This experiment compared the output characteristics of two types of rectifier circuits, A half-wave rectifier, and a full-wave bridge rectifier. Each converts an ac voltage into a pulsed waveform having an average or dc voltage output.

DATA FOR EXPERIMENT: DIODE RECTIFIER CIRCUITS

<i>Rectifier type</i>	<i>Measured</i>			<i>Expected V_{DC}</i>	<i>% Error of V_{DC}</i>
	$V_s(\text{peak})$	$V_o(\text{peak})$	V_{DC}		
<i>Half-Wave</i>					
<i>Full-Wave (center-tap)</i>					

TABLE 2-1: Rectifier data

POST LAB ASSIGNMENT (MUST BE INCLUDED IN LAB REPORT)

1. For an input frequency of 60 Hz, approximately what is the period of the half wave rectifier circuit shown in Figure 2-1? Explain your answer.
2. For the half-wave rectifier of figure 2-1, why is the frequency of the input cycle the same as the frequency of the output cycle even though there is a zero amplitude for half of the cycle?
3. From your data, what are the voltage drops from the input to the output for the half-wave rectifier and for the center-tapped full-wave rectifier? Explain your reason for this drop.
4. What is the typical value of the reverse RMS voltage for 1N4007 diode? (*Hint: Look in the datasheet*)
5. Complete the following table.

	<i>Input frequency</i>	<i>Output frequency</i>
<i>Half wave rectifier</i>		
<i>Full wave center-tapped rectifier</i>		

USEFUL FORMULAS

Half-Wave Rectifier

$$(1) \quad DC\ output\ voltage = \frac{V_s(\text{peak}) - V_B}{\pi} \quad (\text{sine wave input})$$

$$(2) \quad Output\ frequency = \text{input frequency}$$

Center-Tapped Full-Wave Rectifier

$$(3) \quad DC\ output\ voltage = \frac{2[V_s(\text{peak}) - V_B]}{\pi} \quad (\text{sine wave input})$$

$$(4) \quad Output\ frequency = 2 \times (\text{input frequency})$$

Percent Error

$$(5) \quad \% \text{error} = \left| \frac{\text{Actual Value} - \text{Expected Value}}{\text{Expected Value}} \right| \times 100\%$$

(blank)

Lab 3

Capacitor Input Rectifier Filter

PURPOSE AND BACKGROUND

The purpose of this experiment is to demonstrate the operation of a full-wave bridge rectifier, as well as a capacitor input filter when it is connected to the output of a full-wave bridge rectifier. The full-wave bridge rectifier causes an AC input voltage to be converted into a pulsed waveform which has an average, or DC voltage output. The filter, which consists of a single resistor and capacitor in parallel, smooths out the pulsating output voltage of the rectifier.

REQUIRED PARTS AND EQUIPMENT

- ❖ 120VAC variac
- ❖ 12.6 V-rms Center-Tapped Transformer
- ❖ 100 μ F Capacitor
- ❖ 470 μ F Capacitor
- ❖ 1 k Ω Resistor
- ❖ Four 1N4007 Silicon Rectifier Diodes
- ❖ DMM (preferred) or VOM
- ❖ Breadboard
- ❖ Oscilloscope

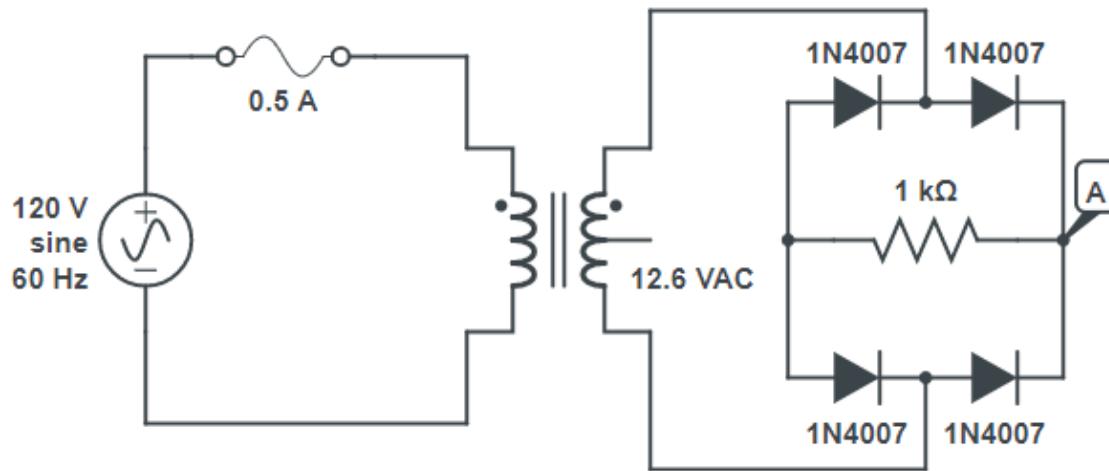


FIGURE 3-1: Full-Wave Bridge Rectifier Circuit

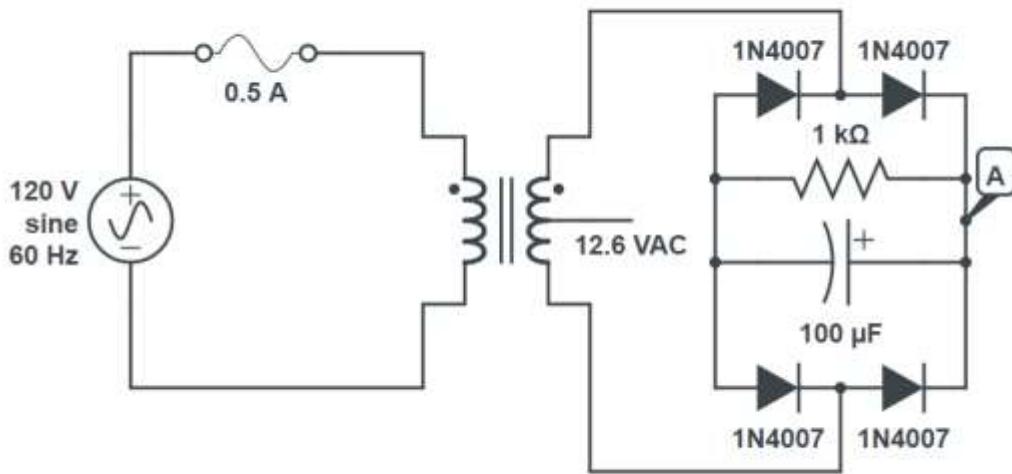


FIGURE 3-2: Capacitor Input Rectifier Filter Circuit

PROCEDURE

1. Wire the full-wave bridge rectifier circuit according to Figure 3-1. Be sure to pay close attention to the polarities of all four of the 1N4007 diodes and the connections to the 120 V primary side of the transformer. The center-tapped lead will not be used for this section.
2. Apply 120 VAC (rms) to the transformer's primary leads. With the channel set to dc coupling, connect the probe across the 1 kΩ resistor (*Node A*). Measure the peak voltage V_o (peak) across the 1 kΩ resistor (*Node A*) and record your results in Table 3-1. You should find that the peak voltage across the 1 kΩ resistor is smaller than the secondary voltage by twice the barrier potential. Why?
3. With your multimeter, measure the *dc* voltage (V_{DC}) across the 1-kΩ resistor, and record you result in Table 3-1. Compare this result with that obtained from the equation for the average or dc voltage of a full-wave bridge rectifier (Equation 1).
4. Wire the full-wave bridge rectifier circuit with the capacitor input filter as shown in Figure 3-2. Pay close attention to the polarities of the 1N4007 diodes. You should also be very careful to observe the polarity of the 100 μ F filter capacitor.
5. Set your scope to the following approximate settings:
 - a. Channel 1: 1 V/division
 - b. Time base: 5 ms/division

Connect the scope probe across the 1 kΩ resistor, or the 100 μ F capacitor. If everything is working properly, you should obtain the waveform shown in Figure 3-3.

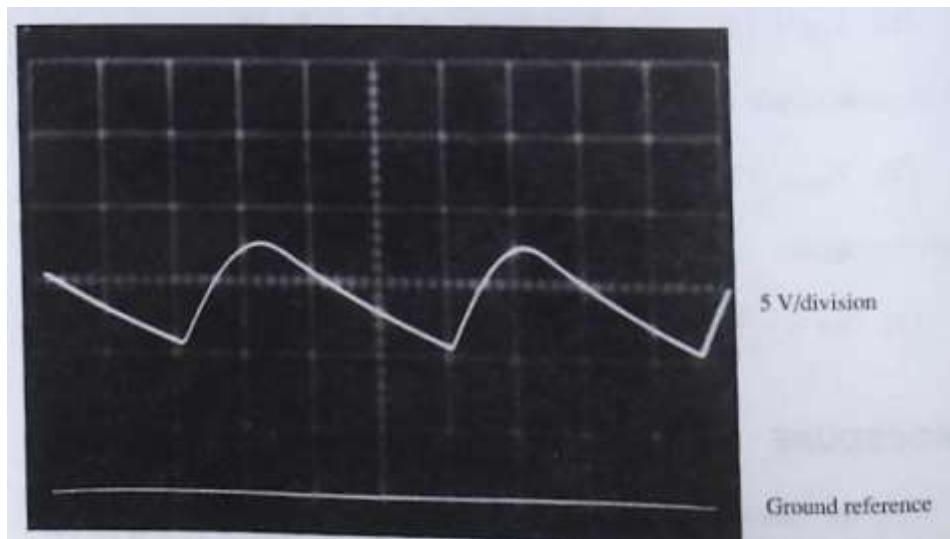


FIGURE 3-3 Time base:2 ms/division

6. With the oscilloscope, measure the peak (maximum) output voltage V_o (rectified) and the peak-to-peak ripple voltage across the $1\text{ k}\Omega$ resistor or the $100\text{ }\mu\text{F}$ capacitor. With your multimeter, measure the DC voltage (V_{DC}) and compute the expected dc voltage, peak-to-peak ripple voltage, and the percentage ripple using Equations 3, 4, and 5. Record all results in Table 3-2.
7. Replace the capacitor with $470\text{ }\mu\text{F}$. With your scope, measure the peak output voltage and the peak-to-peak ripple voltage across the $1\text{ k}\Omega$ resistor or the $470\text{ }\mu\text{F}$ capacitor. As in Step 6, measure the DC output voltage and using Equations 3, 4, and 5, calculate the expected values for the dc voltage, peak-peak ripple voltage and percent ripple. Record all the results in Table 3-2.
8. If you have wired the circuit correctly, you should now observe very little ripple voltage on the scope's display.
9. For each capacitor value, compare your values for dc output voltage, ripple voltage, and percent ripple. When you increase the value of the filter capacitor, what happens to the dc output voltage, ripple voltage, and percent ripple.
 - a. For fixed load resistance of $1\text{ k}\Omega$, increasing the capacitance of the input filter capacitor should decrease both the peak-to-peak ripple voltage and the percent ripple
10. Turn off all power from the function generator and then reverse the polarity of all four diodes. In addition, reverse the polarity of the $470\text{ }\mu\text{F}$ capacitor so that its positive terminal is connected to ground
11. Apply power to the transformer's primary and repeat Steps 7, 8, and 9. Compare these results with the positive rectifier using a $470\text{ }\mu\text{F}$ capacitor.

WHAT YOU HAVE DONE

This experiment demonstrated the operation of a capacitor input filter when connected to the output of a full-wave bridge rectifier. The filter, using a parallel resistor capacitor circuit, smooths out the pulsating output voltage of the rectifier. As the RC time constant of the filter was made larger, the ripple voltage for

the filter was reduced further. Check the data sheet for additional technical information on the 1N4007 diode.

DATA FOR EXPERIMENT: DIODE RECTIFIER CIRCUITS

<i>Rectifier Type</i>	<i>Measured</i>			<i>Expected V_{DC}</i>	<i>% Error V_{DC}</i>
	v_s (peak)	v_o (peak)	V_{DC}		
<i>Full-Wave Bridge</i>					

TABLE 3-1: Rectifier data

<i>Parameter</i>	<i>Step 3: 100 μF</i>	<i>Step 4: 470 μF</i>	<i>Step 7: 470 μF (Reverse Polarity)</i>
<i>Measured V_o(peak)</i>			
<i>Measured V_{DC}</i>			
<i>Calculated V_{DC}</i>			
<i>% Error of V_{DC}</i>			
<i>Measured peak-peak ripple voltage</i>			
<i>Calculated peak-peak ripple voltage</i>			
<i>% Error of peak-peak ripple voltage</i>			
<i>% Ripple (from measured values)</i>			

TABLE 3-2: Rectifier data

USEFUL FORMULAS

Full-wave Bridge Rectifier

$$(1) \quad DC\ output\ voltage = \frac{2[V_s(\text{peak}) - V_B]}{\pi} \quad (\text{sine wave input})$$

$$(2) \quad Output\ frequency = 2 \times (\text{input frequency})$$

DC Output Voltage

$$(3) \quad V_{DC} = \left(\frac{1}{2fR_L C} \right) \times V_o(\text{rect}) \quad (f = 120\ Hz)$$

Peak-to-Peak Ripple Voltage

$$(4) \quad V_{r(p-p)} \cong \left(\frac{1}{fR_L C} \right) \times V_o(\text{rect}) \quad (f = 120\ Hz)$$

Percent Ripple

$$(5) \quad \%r = \left(\frac{V_{r(p-p)}}{V_{DC}} \right) \times 100\%$$

Percent Error

$$(6) \quad \%error = \left| \frac{\text{Actual Value} - \text{Expected Value}}{\text{Expected Value}} \right| \times 100\%$$

Lab 4

Zener Diode and Voltage Regulation

PURPOSE AND BACKGROUND

The purpose of this experiment is to (1) test a Zener diode using a multimeter, and to (2) demonstrate the characteristics of a Zener diode and (3) its uses as a simple voltage regulator. Unlike rectifier diodes, Zener diodes are normally reverse biased, so they maintain a constant voltage across their terminals over a specified range of current. Like a rectifier diode, a Zener diode can be approximated by a constant DC voltage source in series with a resistor. When used as a regulator, the Zener diode maintains a DC output voltage that is essentially constant even though the lead current may vary.

PRELAB ASSIGNMENT (MUST BE SUBMITTED ONE DAY PRIOR TO CLASS)

Build the circuit in Figure 4-1 C in PSpice and measure peak-to-peak and maximum voltages for both input (at node A) and output (at node B) waveforms and write a report on what you observed from the input and the output waveforms and why? (NOTE: In PSpice look for 1N4733 Zener diode or any Zener diode which have similar characteristics.)

REQUIRED PARTS AND EQUIPMENT

- ❖ 100 Ω Resistor (1/4 W)
- ❖ Two 220 Ω Resistors (1/2 W)
- ❖ 0-15 V variable DC power supply
- ❖ Dual Trace Oscilloscope
- ❖ Two DMMs or VOMs
- ❖ Breadboard
- ❖ 1N4733A, 5.1 V Zener Diode

PROCEDURE

1. Test the Zener diode using a multimeter. Record your results in Table 4-1.
2. Wire Circuit A as shown in the schematic diagram in Figure 4-1.
3. Increase the DC supply voltage in small steps (as given in Table 4-1A) while simultaneously measuring the voltage (V_z) across the Zener diode, and the current (I_z) through the Zener diode. Record all measured values in Table 4-2A, and plot your results for the corresponding Zener current and voltage values in a graph. What do you notice about the current voltage curve for the Zener diode?

Note that initially the Zener diode current is essentially zero for the diode voltages less than the knee voltage. You should find that as the voltage drop approaches the diode's knee voltage, the diode current increases rapidly, while the voltage essentially remains constant. Consequently, the Zener diode maintains a near constant voltage drop when it is sufficiently reverse biased.

The 1N4733A is rated at 5.1 V with a tolerance of 10%. From your graph, determine the voltage across the Zener diode at a current of approximately 49 mA. Within a 10% margin of error, your value should be at 6.2 V. Measure and record the Zener voltage in Table 4-2B.

Determine the internal resistance (R_z) of your 1N4733A Zener diode from your data by taking the change in Zener voltage (ΔV_z), divided by the corresponding change in Zener current (ΔI_z). Perform this

calculation only on the straight-line breakdown region of your diode curve that you plotted in Step 3. Record your result for the internal Zener resistance in Table 4-2B.

4. Now wire Circuit B shown in the schematic diagram of Figure 4-1.

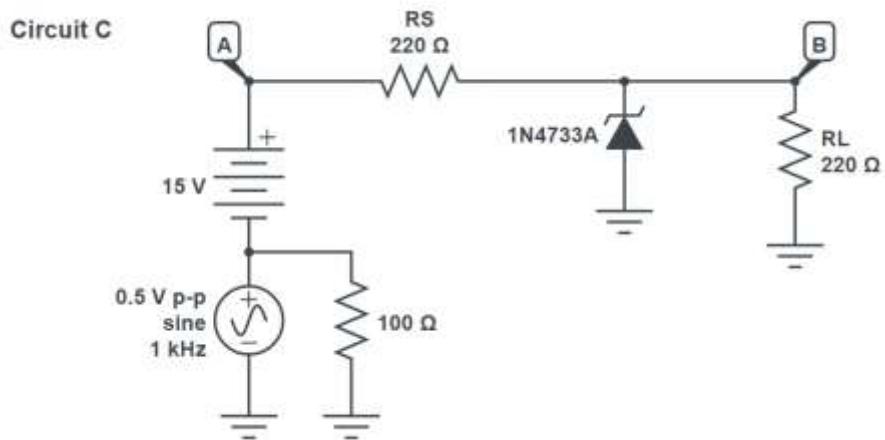
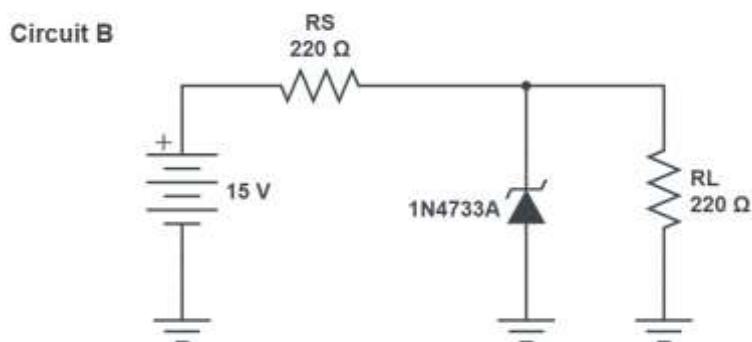
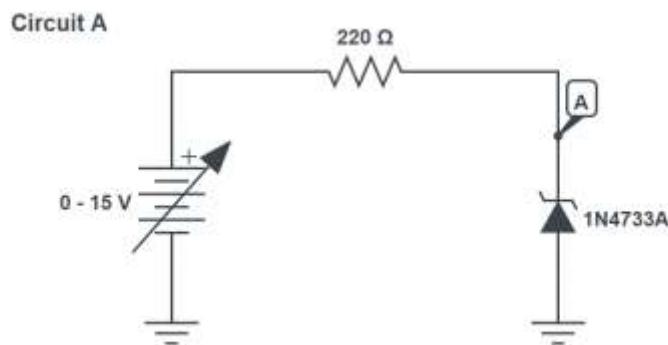


FIGURE 4- 1: Schematic diagram of circuits

5. Apply dc voltage (V_{in}) to the breadboard. Measure the source current (I_s), Zener current (I_z), load current (I_L), and full-load output voltage (V_{FL}). Record these values in Table 4-3A. Using the Zener voltage and the internal Zener resistance calculated in Steps 3 and 4, compare the measured output voltage with the expected value (Equation 3).
6. Now disconnect the 220- Ω load resistor. Measure the source current (I_s), Zener current (I_z), and output voltage with no load (V_{NL}). Record these values in Table 4-3B. Using the Zener voltage and the internal Zener resistance determined in Steps 3 and 4, compare the measured no-load output voltage with the expected value.
7. Determine the percent load regulation. Record the result in Table 4-3B.
8. Now, add a signal generator in series with the dc voltage source as shown in Figure 4-1, Circuit C. Adjust the output of the signal generator to 0.5 V peak-to-peak with a frequency of 1 kHz.
9. With your oscilloscope at point A. Observe both the dc and the ac voltage levels, using the oscilloscope. You should see a 0.5V peak to peak sine wave superimposed on a 15 V dc level above the ground.
10. With your oscilloscope at point B, measure the DC output voltage of the Zener diode regulator, record your value in Table 4-3C. At this point you should see virtually no ripple voltage on the regulator's output signal. How does this voltage compare with that which was measured in Step 6?
11. Notice that the Zener diode regulator provides a relatively constant output voltage if the input voltage is greater than the Zener's knee voltage. If there is any voltage variation or ripple on the input voltage signal, the output essentially remains constant.

WHAT YOU HAVE DONE

This experiment demonstrated the characteristic of a 6.2 V Zener diode. The Zener diode is normally reverse biased so that it maintains a constant voltage between its anode and cathode terminals over a specified range of currents. This experiment also demonstrated the concept of voltage regulation where the output remains constant with changes in load current. Check the data sheet for the 1N4733A Zener Diode for technical specifications.

DATA FOR EXPERIMENT: THE ZENER DIODE AND VOLTAGE REGULATION

<i>Meter Leads</i>		<i>Result</i>
<i>+</i>	<i>-</i>	
<i>Anode</i>	<i>Cathode</i>	
<i>Cathode</i>	<i>Anode</i>	

TABLE 4- 1: Multimeter tests

<i>Voltage Source</i>	<i>Zener Voltage V_Z(V)</i>	<i>Zener Current I_Z (mA)</i>
500 mV		
800 mV		
1 V		
2 V		
3 V		
4 V		
4.2 V		
4.5 V		
4.8 V		
5 V		
5.2 V		
5.5 V		
5.8 V		
6 V		
7 V		
8 V		
9 V		
10 V		
11 V		
12 V		
13 V		
14 V		
15 V		

TABLE 4-2A: Zener Diode Characteristic Curve A.

<i>Zener knee voltage @ $I_z=49\text{mA}$</i>	5.1 V
<i>Internal Zener resistance</i>	Ω

TABLE 4-2B: Zener Diode

Parameter	Measured Value	Expected Value	% Error
I_s			
I_z			
I_L			
V_{FL}			

TABLE 4-3A: Zener Diode Voltage Regulator Full-Load data

Parameter	Measured Value	Expected Value	% Error
I_s			
I_z			
I_L			
V_{FL}			
<i>% Load regulation, % VR</i>			

TABLE 4-3B: Zener Diode Voltage Regulator No-Load data

Parameter	Measured Value	Expected Value	% Error
<i>DC input voltage, V_{in} (DC)</i>			
<i>AC input ripple voltage, v_{in} (ripple), peak-to-peak</i>			
<i>DC output voltage, V_{out} (DC)</i>			

*AC output ripple
voltage, v_{out} (ripple),
peak-to-peak*

TABLE 4-3C: Zener Diode Voltage Regulator

USEFUL FORMULAS

Maximum limiting series resistance

$$(1) \quad R_s(\max) = \frac{V_{in}(\min) - V_{out}}{I_L(\max)}$$

Output voltage

$$(2) \quad V_{out} = V_z \quad (\text{ideal})$$

$$(3) \quad R_Z = \text{Zener Diode Internal Resistance} = \frac{\Delta V_z}{\Delta I_z}$$

I_z = Zener Diode Current

Zener Diode Current

$$(4) \quad I_z = I_s - I_L \text{ where } \left(I_L = \frac{V_z}{R_L} \right)$$

Source current

$$(5) \quad I_s = \frac{V_{in} - V_{out}}{R_s}$$

Zener diode power dissipation

$$(6) \quad P_z = I_z \cdot V_z$$

Percent Load Regulation

$$(7) \quad \% VR = \frac{V_{NL} - V_{FL}}{V_{FL}} \cdot 100\%$$

V_{NL} = No Load (Open-Circuit) Output Voltage

V_{FL} = Full Load Output Voltage

Output Ripple Voltage

$$(8) \quad V_o(\text{ripple}) = \left(\frac{R_L || R_Z}{R_s + (R_L || R_Z)} \right) \cdot V_{in}(\text{ripple})$$

Percent Error

$$(9) \quad \% \text{ error} = \left| \frac{\text{Expected Value} - \text{Actual Value}}{\text{Expected Value}} \right| \cdot 100\%$$

POST LAB ASSIGNMENT (MUST BE INCLUDED IN LAB REPORT)

1. What is the difference between a Zener diode and a regular PN junction diode?
2. Plot the V - I characteristics using this data from Table 4-2A
3. From your data, what Zener diode did we use in this experiment? What approximately is its Zener voltage?
4. For the circuit in Figure 4-1B, if the input voltage is less than 4 Volts, what will the output voltage be?
5. What is the maximum reverse leakage current for a 1N4733A Zener diode? (*Hint: check the data sheet*)

(blank)

1N4001-G Thru. 1N4007-G

Voltage: 50 to 1000 V

Current: 1.0 A

RoHS Device

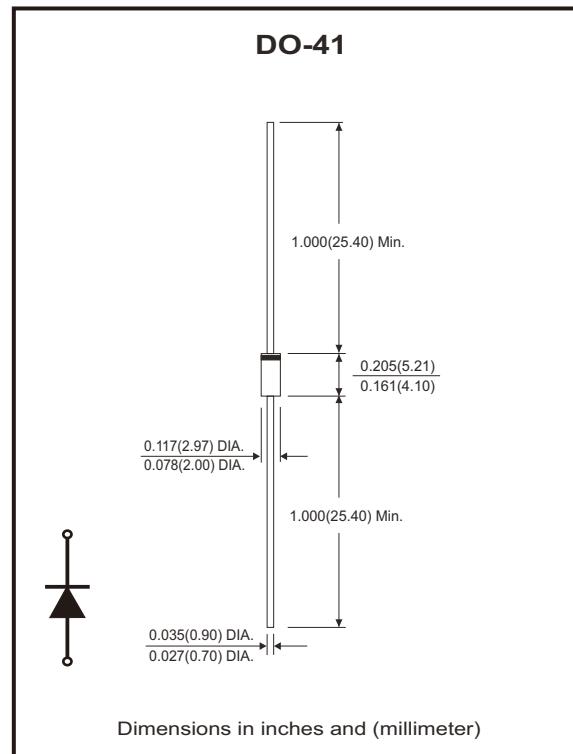


Features

- Low cost construction.
- Fast forward voltage drop.
- Low reverse leakage.
- High forward surge current capability.
- High soldering temperature guarantee: 260 °C/10 seconds, 0.375"(9.5mm) lead length at 5lbs(2.3kg) tension.

Mechanical data

- Case: Transfer molded plastic, DO-41
- Epoxy: UL 94V-0 rate flame retardant
- Polarity: Indicated by cathode band
- Lead: Plated axial lead, solderable per MIL-STD-750, method 2026
- Mounting position: Any
- Weight: 0.012ounce, 0.34 grams(approx.).



Electrical Characteristics (at TA=25°C unless otherwise noted)

Ratings at 25°C ambient temperature unless otherwise specified.
Single phase, half wave, 60Hz, resistive or inductive load.
For capacitive load derate current by 20%.

Parameter	Symbol	1N4001 -G	1N4002 -G	1N4003 -G	1N4004 -G	1N4005 -G	1N4006 -G	1N4007 -G	Unit
Maximum Repetitive Peak Reverse Voltage	V _{RRM}	50	100	200	400	600	800	1000	V
Maximum RMS Voltage	V _{RMS}	35	70	140	280	420	560	700	V
Maximum DC Blocking Voltage	V _{DC}	50	100	200	400	600	800	1000	V
Maximum Average Forward Rectified Current 0.375"(9.5mm) Lead Length @T _A =55°C	I _(AV)					1.0			A
Peak Forward Surge Current, 8.3mS single half sine-wave superimposed on rated load (JEDEC method)	I _{FSM}					30			A
Maximum Instantaneous Forward Voltage @1.0A	V _F				1.1				V
Maximum DC Reverse Current at Rated DC Blocking voltage per element	T _A =25°C	I _R			5.0				µA
	T _A =100°C				50				
Typical Junction Capacitance (Note 1)	C _J				15				pF
Typical Thermal Resistance (Note 2)	R _{θJA}				60				°C/W
Operating Temperature Range	T _J				-55 ~ +150				°C
Storage Temperature Range	T _{STG}				-55 ~ +150				°C

NOTES:

1. Measured at 1.0MHz and applied reverse voltage of 4.0V DC.

2. Thermal Resistance from junction to ambient and junction to lead at 0.375"(9.5mm) lead length P.C.B mounted.

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REV:B

General Purpose Silicon Rectifiers

Comchip
SMD Diode Specialist

Rating and Characteristic Curves (1N4001-G Thru. 1N4007-G)

Fig.1 - Typical Forward Current Derating Curve

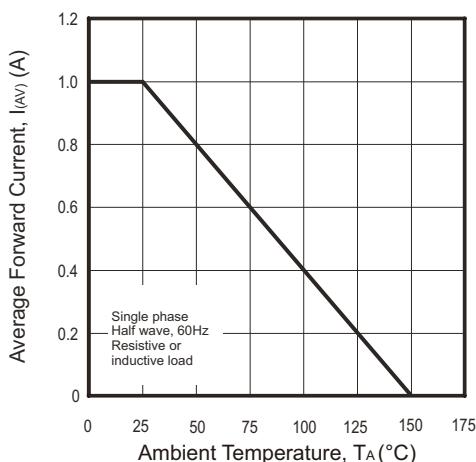


Fig.2 - Maximum, Non-Repetitive Peak Forward Surge Current

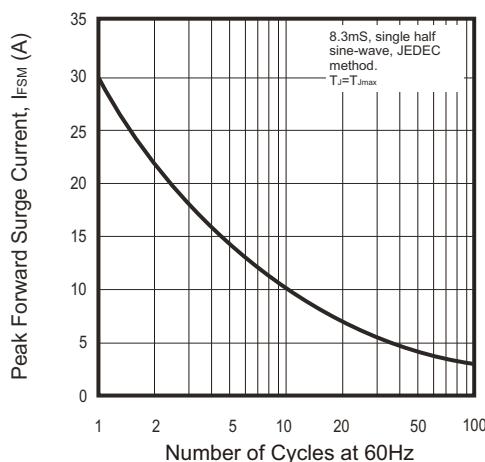


Fig.3 - Typical Instantaneous Forward Characteristics

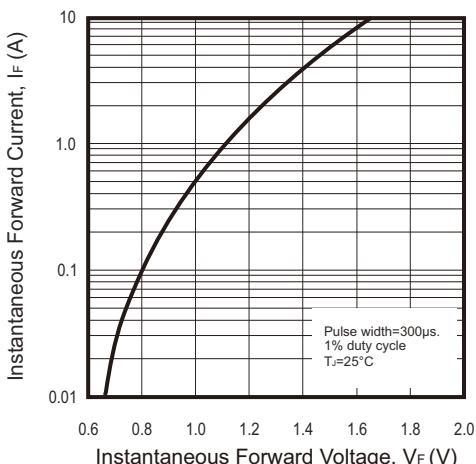


Fig.4 - Typical Reverse Characteristics

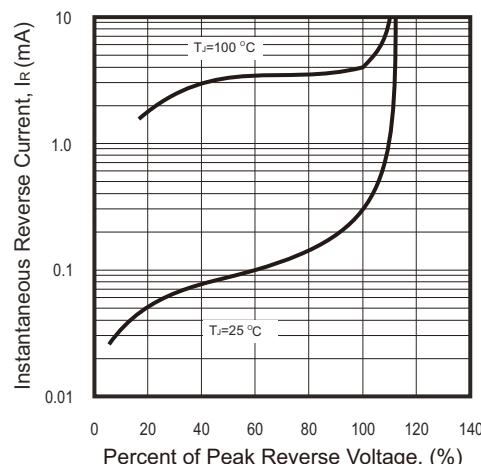
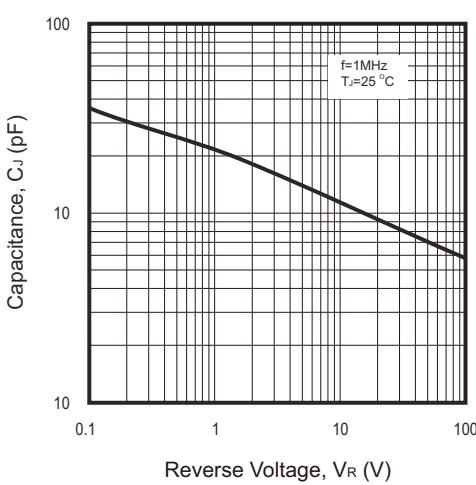


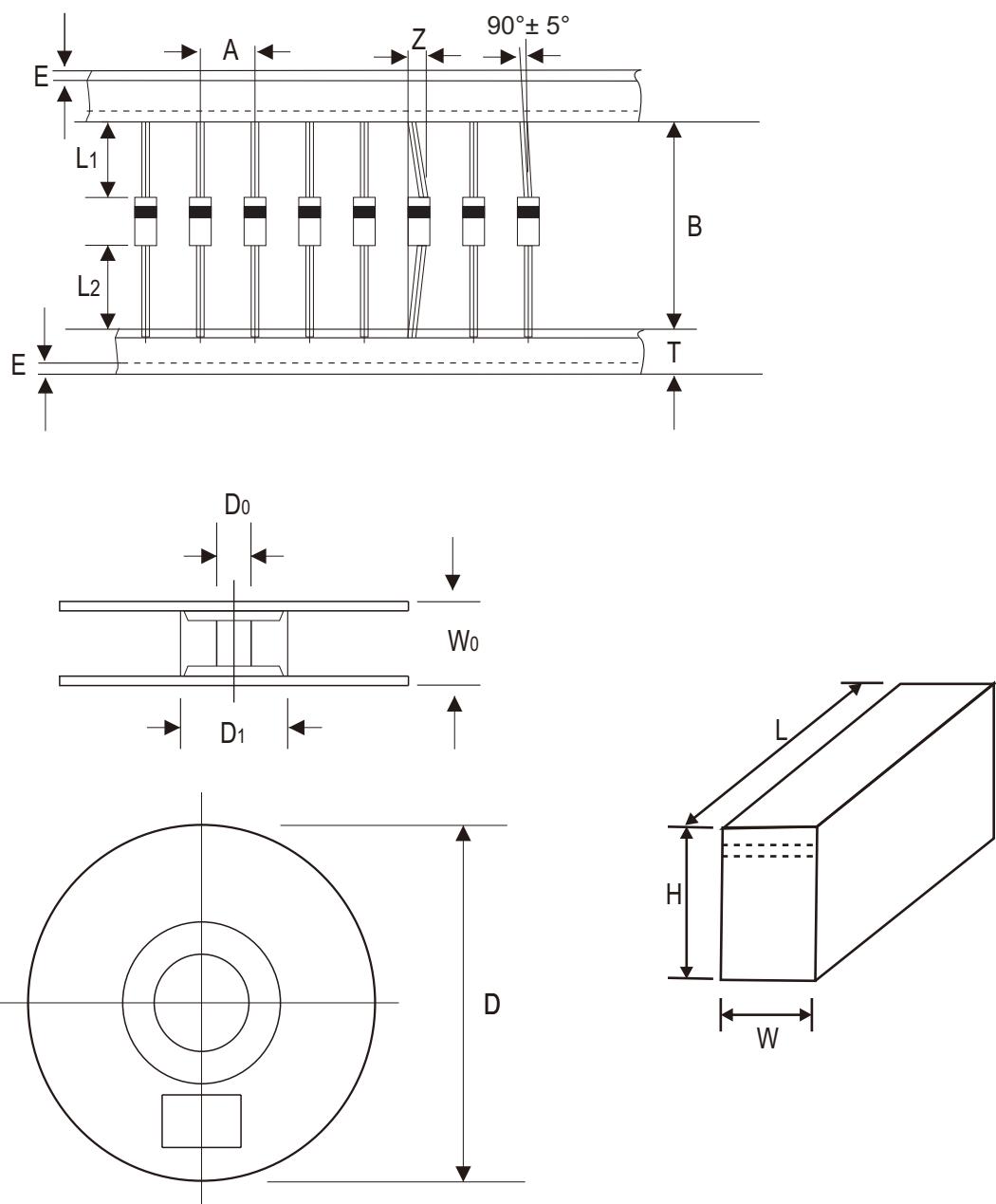
Fig.5 - Typical Junction Capacitance



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REV:B

Taping Specification For Axial Lead Diodes



DO-41	SYMBOL	A	B	Z	T	E	L1-L2
	(mm)	5.00 ± 0.50	52.40 ± 1.50	1.60 (max)	6.00 ± 0.40	3.00 (max)	1.00 (max)
	(inch)	0.197 ± 0.020	2.063 ± 0.059	0.063 (max)	0.236 ± 0.016	0.118 (max)	0.039 (max)

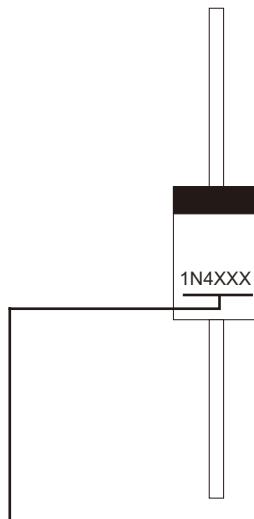
DO-41	SYMBOL	D1	D0	D	W0	L	W	H
	(mm)	85.70 ± 0.30	16.60 ± 0.40	330.00	72.00 ± 3.00	260.00 ± 5.00	75.00 ± 5.00	150.00 ± 5.00
	(inch)	3.374 ± 0.012	0.654 ± 0.016	12.992	2.835 ± 0.118	10.236 ± 0.197	2.953 ± 0.197	5.906 ± 0.197

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REV:B

Marking Code

Part Number	Marking Code	Packaging
1N4001T-G	1N4001	REEL
1N4002T-G	1N4002	REEL
1N4003T-G	1N4003	REEL
1N4004T-G	1N4004	REEL
1N4005T-G	1N4005	REEL
1N4006T-G	1N4006	REEL
1N4007T-G	1N4007	REEL
1N4001A-G	1N4001	AMMO
1N4002A-G	1N4002	AMMO
1N4003A-G	1N4003	AMMO
1N4004A-G	1N4004	AMMO
1N4005A-G	1N4005	AMMO
1N4006A-G	1N4006	AMMO
1N4007A-G	1N4007	AMMO
1N4001B-G	1N4001	BULK
1N4002B-G	1N4002	BULK
1N4003B-G	1N4003	BULK
1N4004B-G	1N4004	BULK
1N4005B-G	1N4005	BULK
1N4006B-G	1N4006	BULK
1N4007B-G	1N4007	BULK



1N4XXX = Product type marking code

Note:

1) Suffix code after part number to specify packaging item .

Packaging	Code
REEL PACK	T
AMMO PACK	A
BULK PACK	B

Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
DO-41	5,000	13

Case Type	BULK PACK	
	BOX (pcs)	
DO-41		1,000

Case Type	AMMO PACK	
	BOX (pcs)	
DO-41		5,000

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REV:B



ON Semiconductor®

1N4728A - 1N4758A

Zener Diodes

Tolerance = 5%



DO-41 Glass case

COLOR BAND DENOTES CATHODE

Absolute Maximum Ratings *

$T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
P_D	Power Dissipation @ $TL \leq 50^\circ\text{C}$, Lead Length = 3/8"	1.0	W
	Derate above 50°C	6.67	mW/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to +200	$^\circ\text{C}$

* These ratings are limiting values above which the serviceability of the diode may be impaired.

Electrical Characteristics

 $T_a = 25^\circ\text{C}$ unless otherwise noted

Device	V _Z (V) @ I _Z (Note 1)			Test Current I _Z (mA)	Max. Zener Impedance			Leakage Current I _R (μA)	V _R (V)	Non-Repetitive Peak Reverse Current I _{ZSM} (mA) (Note 2)
	Min.	Typ.	Max.		Z _Z @ I _Z (Ω)	Z _{ZK} @ I _{ZK} (Ω)	I _{ZK} (mA)			
1N4728A	3.135	3.3	3.465	76	10	400	1	100	1	1380
1N4729A	3.42	3.6	3.78	69	10	400	1	100	1	1260
1N4730A	3.705	3.9	4.095	64	9	400	1	50	1	1190
1N4731A	4.085	4.3	4.515	58	9	400	1	10	1	1070
1N4732A	4.465	4.7	4.935	53	8	500	1	10	1	970
1N4733A	4.845	5.1	5.355	49	7	550	1	10	1	890
1N4734A	5.32	5.6	5.88	45	5	600	1	10	2	810
1N4735A	5.89	6.2	6.51	41	2	700	1	10	3	730
1N4736A	6.46	6.8	7.14	37	3.5	700	1	10	4	660
1N4737A	7.125	7.5	7.875	34	4	700	0.5	10	5	605
1N4738A	7.79	8.2	8.61	31	4.5	700	0.5	10	6	550
1N4739A	8.645	9.1	9.555	28	5	700	0.5	10	7	500
1N4740A	9.5	10	10.5	25	7	700	0.25	10	7.6	454
1N4741A	10.45	11	11.55	23	8	700	0.25	5	8.4	414
1N4742A	11.4	12	12.6	21	9	700	0.25	5	9.1	380

Device	V _Z (V) @ I _Z (Note 1)			Test Current I _Z (mA)	Max. Zener Impedance			Leakage Current		Non-Repetitive Peak Reverse Current I _{ZSM} (mA) (Note 2)
	Min.	Typ.	Max.		Z _Z @I _Z (Ω)	Z _{ZK} @I _{ZK} (Ω)	I _{ZK} (mA)	I _R (μA)	V _R (V)	
1N4743A	12.35	13	13.65	19	10	700	0.25	5	9.9	344
1N4744A	14.25	15	15.75	17	14	700	0.25	5	11.4	304
1N4745A	15.2	16	16.8	15.5	16	700	0.25	5	12.2	285
1N4746A	17.1	18	18.9	14	20	750	0.25	5	13.7	250
1N4747A	19	20	21	12.5	22	750	0.25	5	15.2	225
1N4748A	20.9	22	23.1	11.5	23	750	0.25	5	16.7	205
1N4749A	22.8	24	25.2	10.5	25	750	0.25	5	18.2	190
1N4750A	25.65	27	28.35	9.5	35	750	0.25	5	20.6	170
1N4751A	28.5	30	31.5	8.5	40	1000	0.25	5	22.8	150
1N4752A	31.35	33	34.65	7.5	45	1000	0.25	5	25.1	135
1N4753A	34.2	36	37.8	7	50	1000	0.25	5	27.4	125
1N4754A	37.05	39	40.95	6.5	60	1000	0.25	5	29.7	115
1N4755A	40.85	43	45.15	6	70	1500	0.25	5	32.7	110
1N4756A	44.65	47	49.35	5.5	80	1500	0.25	5	35.8	95
1N4757A	48.45	51	53.55	5	95	1500	0.25	5	38.8	90
1N4758A	53.2	56	58.8	4.5	110	2000	0.25	5	42.6	80

Notes:

1. Zener Voltage (V_Z)

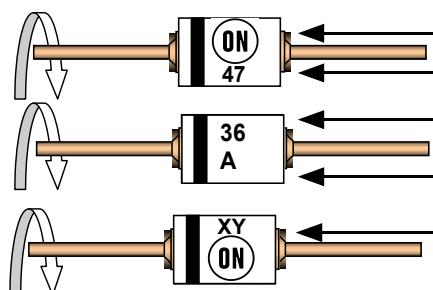
The zener voltage is measured with the device junction in the thermal equilibrium at the lead temperature (T_L) at 30°C ± 1°C and 3/8" lead length.

2. 2 Square wave Reverse Surge at 8.3 msec soak time.

Top Mark Information

Device	Line 1	Line 2	Line 3	Line 4	Line 5
1N4728A	LOGO	47	28	A	XY
1N4729A	LOGO	47	29	A	XY
1N4730A	LOGO	47	30	A	XY
1N4731A	LOGO	47	31	A	XY
1N4732A	LOGO	47	32	A	XY
1N4733A	LOGO	47	33	A	XY
1N4734A	LOGO	47	34	A	XY
1N4735A	LOGO	47	35	A	XY
1N4736A	LOGO	47	36	A	XY
1N4737A	LOGO	47	37	A	XY
1N4738A	LOGO	47	38	A	XY
1N4739A	LOGO	47	39	A	XY
1N4740A	LOGO	47	40	A	XY
1N4741A	LOGO	47	41	A	XY
1N4742A	LOGO	47	42	A	XY
1N4743A	LOGO	47	43	A	XY
1N4744A	LOGO	47	44	A	XY
1N4745A	LOGO	47	45	A	XY
1N4746A	LOGO	47	46	A	XY
1N4747A	LOGO	47	47	A	XY
1N4748A	LOGO	47	48	A	XY
1N4749A	LOGO	47	49	A	XY
1N4750A	LOGO	47	50	A	XY
1N4751A	LOGO	47	51	A	XY
1N4752A	LOGO	47	52	A	XY
1N4753A	LOGO	47	53	A	XY
1N4754A	LOGO	47	54	A	XY
1N4755A	LOGO	47	55	A	XY
1N4756A	LOGO	47	56	A	XY
1N4757A	LOGO	47	57	A	XY
1N4758A	LOGO	47	58	A	XY

Top Mark Information (Continued)



1st line: F - ON Semiconductor Logo
 2nd line: Device Name - 3rd to 4th characters of device name for 1Nxx series
 or 4th to 6th characters for BZXyy series
 3rd line: Device Name - 5th to 6th characters of device name for 1Nxx series
 or Voltage rating for BZXyy series
 4th line: Device Name - 7th to 8th characters of device name for 1Nxx series
 or Large Die identification only for BZXyy series
 5th line: Date Code - Two Digit - Six Weeks Date Code

General Requirements:

- 1.0 Cathode Band
- 2.0 First Line: **(ON)** - ON Semiconductor Logo
- 3.0 Second Line: Device name - For 1Nxx series: 3rd to 4th characters of the device name.
For BZxx series: 4th to 6th characters of the device name.
- 4.0 Third Line: Device name - For 1Nxx series: 5th to 6th characters of the device name.
For BZXyy series: Voltage rating
- 5.0 Third Line: Device name - For 1Nxx series: 7th to 8th characters of the device name.
(the 8th character is the large die identification)
For BZXyy series: Large Die Identification character
- 6.0 Fourth Line: Date Code - Two Digit - Six Weeks Date Code
Where: X represents the last digit of the calendar year
Y represents the Six weeks numeric code
- 7.0 Devices shall be marked as required in the device specification (PID or ON Semiconductor Test Spec).
- 8.0 Maximum no. of marking lines: 5
- 9.0 Maximum no. of digits per line: 3
- 10.0 ON Semiconductor logo must be 20 % taller than the alphanumeric marking and should occupy the 2 characters of the specified line.
- 11.0 Marking Font: Arial (Except ON Semiconductor Logo)
- 12.0 First character of each marking line must be aligned vertically.
- 13.0 All device markings must be based on ON Semiconductor device specification.

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[1N4744A-T50A](#) [1N4744A-T50R](#) [1N4754A-T50A](#) [1N4738A-T50A](#) [1N4738A-T50R](#) [1N4747A-T50A](#) [1N4736A-T50A](#)
[1N4736A-T50R](#) [1N4733A-T50A](#) [1N4733A-T50R](#) [1N4734A-T50A](#) [1N4734A-T50R](#) [1N4751A-T50A](#) [1N4752A-T50A](#)
[1N4732A-T50A](#) [1N4737A-T50A](#) [1N4746A-T50A](#) [1N4755A-T50A](#) [1N4742A-T50A](#) [1N4758A-T50A](#) [1N4740A-T50A](#)
[1N4735A-T50R](#) [1N4735A-T50A](#) [1N4745A-T50A](#) [1N4749A-T50A](#) [1N4749A-T50R](#) [1N4739A-T50A](#) [1N4741A-T50A](#)
[1N4753A-T50A](#) [1N4728A-T50A](#) [1N4743A-T50R](#) [1N4743A-T50A](#) [1N4748A-T50A](#) [1N4730A-T50A](#) [1N4750A-T50A](#)

Part II

Transistors

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Lab 5

Introduction to Analog Discovery 2 and Transistors

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1. Introduction to Analog Discovery 2

Digilent Analog Discovery 2 is a USB oscilloscope, logic analyzer, and multi-function instrument that allows users to measure, visualize, generate, record, and control mixed-signal circuits of all kinds. Developed in conjunction with Analog Devices and supported by Xilinx University Program. The analog and digital inputs and outputs can be connected to a circuit using simple wire probes.

Driven by the free WaveForms software (Mac, Linux, and Windows compatible) software, Analog Discovery 2 can be configured to work as any one of several traditional test and measurement instruments including an Oscilloscope, Waveform Generator, Power Supply, Voltmeter, Data Logger, Logic Analyzer, Pattern Generator, Static I/O, Spectrum Analyzer, Network Analyzer, Impedance Analyzer, and Protocol Analyzer.

1.1 Specifications of AD2

- Two-channel USB digital oscilloscope ($1M\Omega$, $\pm 25V$, differential, 14-bit, 100MS/s, 30MHz+*)
- Two-channel arbitrary waveform generator ($\pm 5V$, 14-bit, 100MS/s, 12MHz+ bandwidth*)
- 16-channel digital logic analyzer (3.3V CMOS and 1.8V or 5V tolerant, 100MS/s)
- 16-channel pattern generator (3.3V CMOS, 100MS/s)
- 16-channel virtual digital I/O including buttons, switches, displays, and LEDs, which is perfect for logic training applications
- Two input/output digital trigger signals for linking multiple instruments or providing an external trigger source
- Two channel voltmeter
- Network Analyzer with Bode, Nyquist, Nichols transfer diagrams of a circuit. The Network Analyzer has a range of 1Hz to 10MHz
- Spectrum Analyzer capable of the power spectrum and spectral measurements (noise floor, SFDR, SNR, THD, etc.)
- Data Logger with exportable data and plot functionality
- Impedance Analyzer for analyzing capacitive and inductive elements
- Protocol Analyzer with SPI, I2C, CAN, AVR, and UART
- Two programmable power supplies (0...+5V, 0...-5V). The maximum available output current and power depend on the Analog Discovery 2 powering choice.
- Stereo audio amplifier to drive external headphones or speakers with replicated Arbitrary Waveform Generator signals
- An available Software Development Kit for programming with Python and C++, and a toolkit for programming with LabVIEW.
- MATLAB support for the Data Acquisition Toolbox.



Fig. 1. Analog Discovery 2

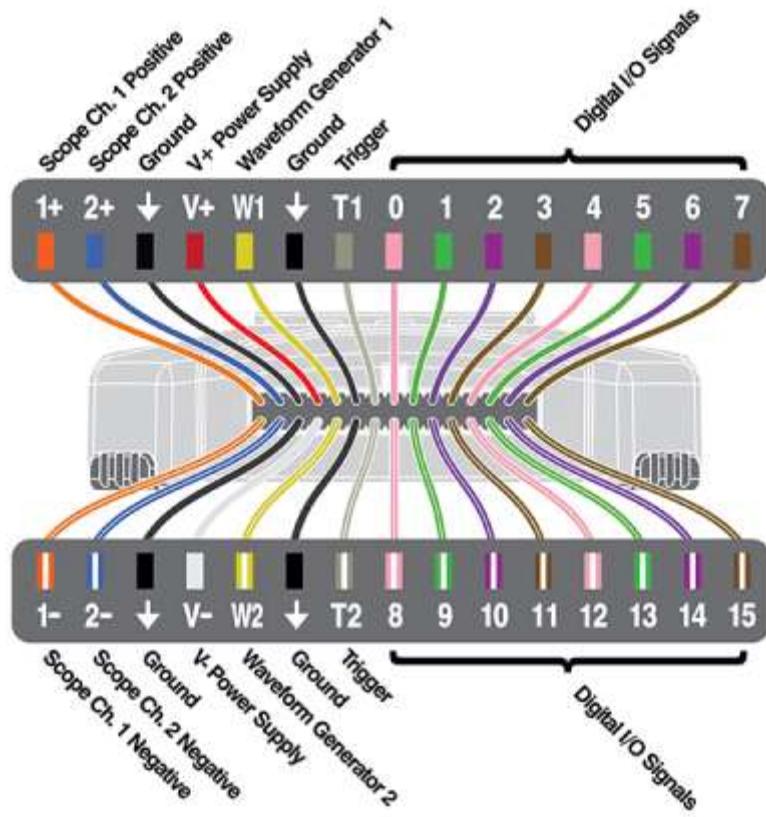


Fig. 2. Pinout diagram of analog discovery2

Connect the Analog Discovery2 device to your pc via USB cable. After connecting the device, a green LED inside the device must be flicking. Check it to make sure all thing is correct.



Fig. 3. Connect USB to AD2 device

Connect the I/O cable which exists in the Digital Discovery2 package, to the device.



Fig. 4. Connect I/O cables to the AD2 device

1.2 Waveforms GUI

Digilent's WaveForms application provides a user interface to the Analog Discovery 2.

- To download the WaveForms application, click on the following link.

<https://mautic.digilentinc.com/waveforms-download>

- And follow the instructions given in the below link to finish the installation process.

https://reference.digilentinc.com/test-and-measurement/analog-discovery-2/getting-started-guide#download_and_install_waveforms

- Connect your board to your PC using the USB connector and the supplied USB cable.
- Start the WaveForms application from the Start Menu > All Programs > Digilent > WaveForms > WaveForms.
- The application starts and connects to your board.
- When WaveForms initially opens, if you have no device plugged in it will give you a warning that no device was detected.



Fig. 5. Waveform GUI when no device is detected

- When you plug in your Analog Discovery 2 it will appear on the device manager and you can then select it to connect to it.

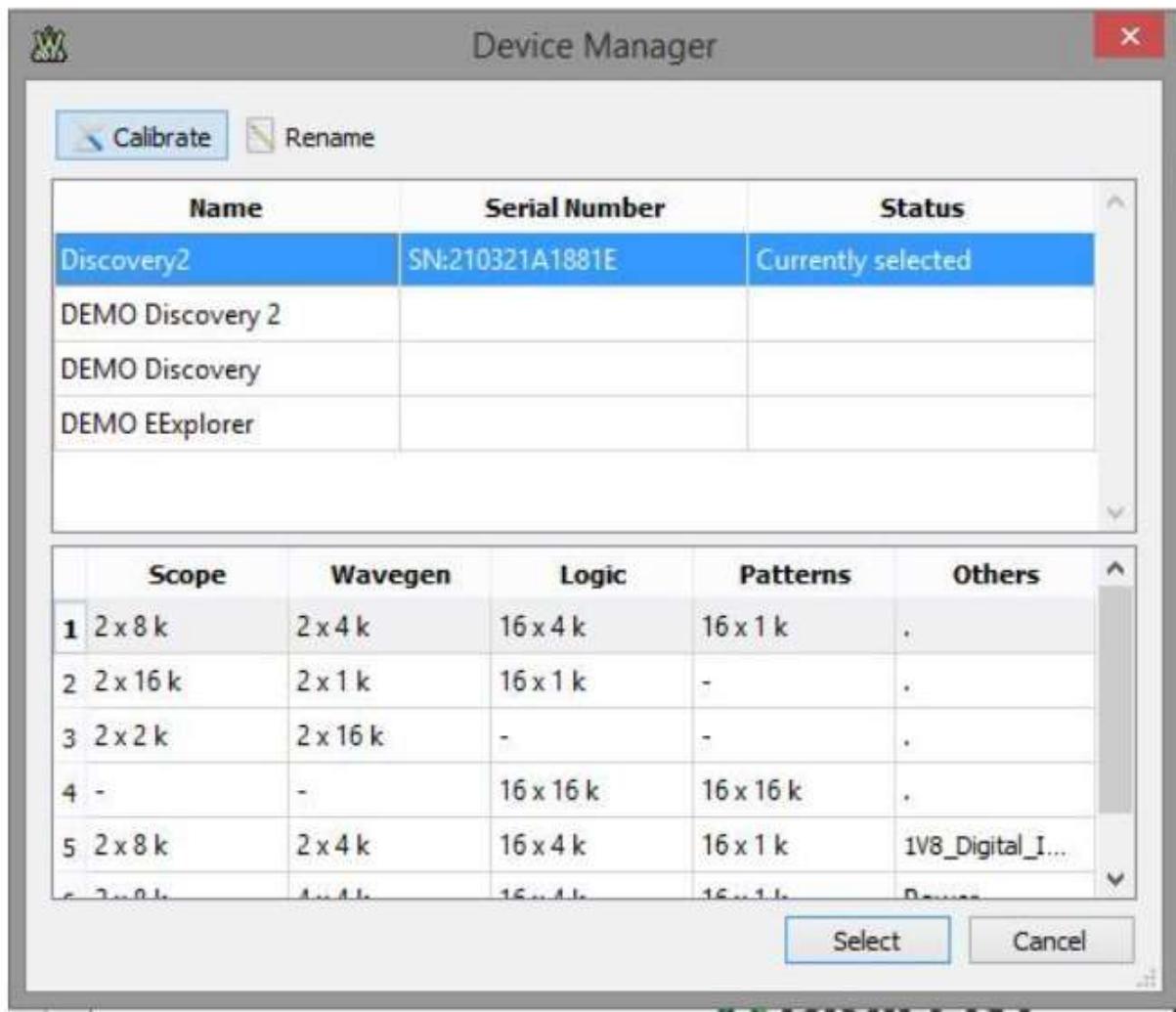


Fig. 6. Waveform device manager window

- The status bar of the WaveForms main window displays the device name and serial number, as shown below.

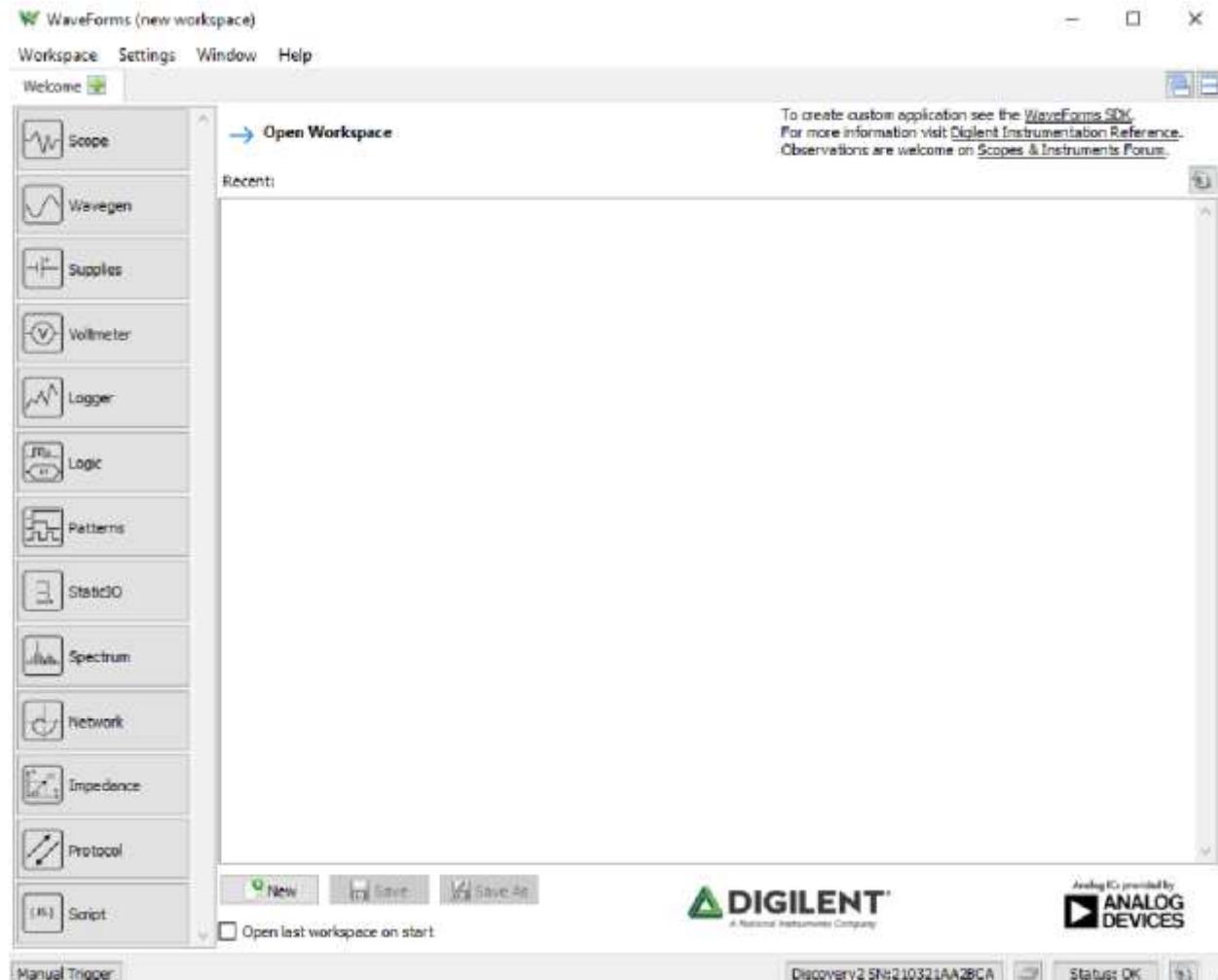


Fig. 7. Waveform GUI

1.2.1 Scope

- An oscilloscope (or “scope”) allows you to view signal voltages, typically in a two-dimensional graph where one or more electrical potential differences (on the vertical axis) are plotted as a function of time or some other voltage (on the horizontal axis).
- Has two channels
- From the pin-out diagram, Scope ch.1 positive (orange probe) and Scope ch.1 negative (orange with white probe) is used as channel 1 probes.
- From the pin-out diagram, Scope ch.2 positive (blue probe) and Scope ch.2 negative (blue with white probe) is used as channel 2 probes.
- GUI of the scope is shown in Fig. 8.

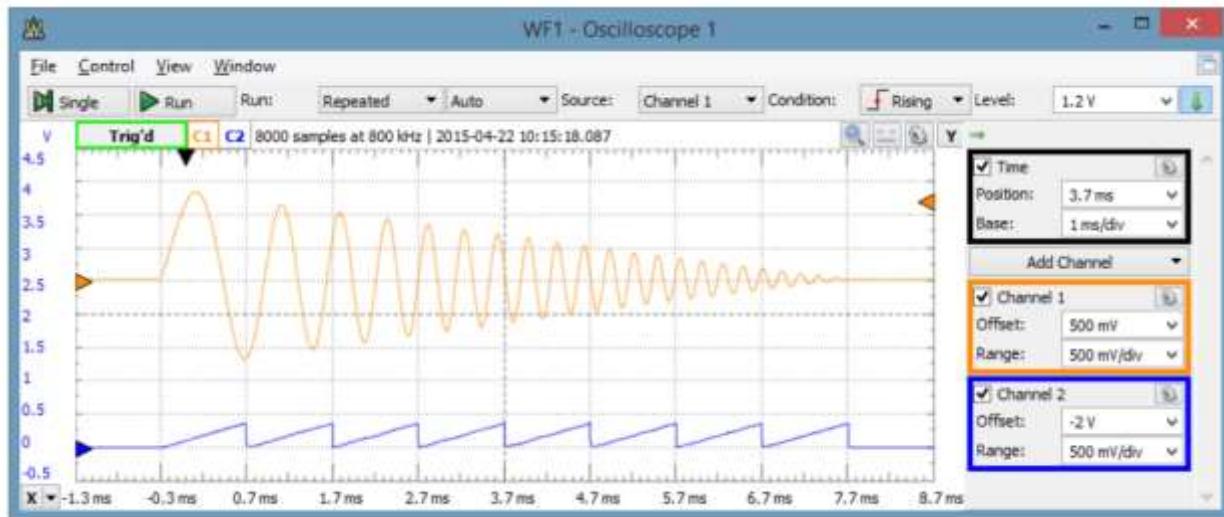
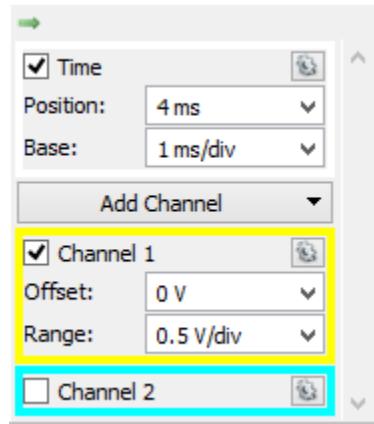


Fig. 8. Scope window

- This toolbar contains the time and channel configuration groups. The toggle button in the top-left corner enables/disables the auto-hiding of this toolbar.



- **Offset:** The offset (vertical position) control lets you move the waveform up or down to exactly where you want it on the screen. The offset is the voltage difference between the centerline of the oscilloscope screen and the actual ground. This difference is generated by an internal offset voltage source.
- **Range:** The range (volts/division) controls to determine the vertical scale of the graph drawn on the oscilloscope screen. The volts/div setting is a scale factor. For example, if the volts/div setting is 2 volts, then each of the ten vertical divisions represents 2 volts and the entire screen can show 20 volts from bottom to top. If the setting is 0.5 volts/div, the screen can display 5 volts from bottom to top, and so on. The maximum voltage you can display on the screen is the volts/div setting multiplied by the number of vertical divisions.
- The Measurements view shows the list of the selected measurements. The first column in the list shows the channel, the second shows the type, and the third shows the measurement result.

- Pressing the Add Default Measurement button opens the Add Measurement window. On the left side is the channel list, and on the right side is a tree view containing the measurement types in groups. Pressing the Add button here (or double-clicking an item) adds it to the measurement list.
- The Show menu options allow you to create statistics out of measurements between acquisitions, which can be cleared with the Reset button.

The screenshot shows two windows. The top window is titled "Measurements" and contains a table of measurements. The bottom window is titled "Add measurement" and is a dialog box for selecting measurements.

Measurements Window Data:

	Name	Value	Count	Average	Min	Max
C2	Peak2Peak	1.995161 V	253	1.994842 V	1.993823 V	1.996164 V
C1	Average	-0.015054 V	253	-0.01506 V	-0.015238 V	-0.014888 V
C1	Frequency	999.995765 Hz	253	999.990538 Hz	999.614302 Hz	1.000306 kHz
C1	Cycles	10	253	10	10	10
C1	RiseTime	0.295046 ms	253	0.295022 ms	0.294494 ms	0.295545 ms
C1	Amplitude	0.998643 V	162	0.998643 V	0.998643 V	0.998643 V

Add measurement Dialog Box:

The "Add measurement" dialog box has two main sections. On the left is a list of channels: "Channel1" and "Channel2". On the right is a tree view of measurement types under the "Horizontal" category. The "Horizontal" category is expanded, showing "Cycles", "Frequency", "Period", "PosDuty", "NegDuty", "PosWidth", "NegWidth", "RiseTime", "FallTime", and "Custom".

Vertical-axis measurements for each channel:

- **Maximum:** the absolute largest value.
- **Minimum:** the absolute smallest value.
- **Average:** the mean value between maximum and minimum values.
- **Peak2Peak:** the difference between the extreme maximum and minimum values.
- **High:** pulse top settled value according to the histogram.

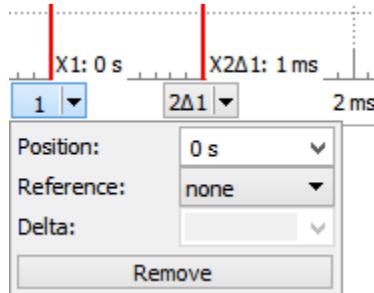
- **Low:** pulse bottom settled value according to the histogram.
- **Middle:** the middle value of the pulse between the top (High) and bottom (Low) settled values.
- **Overshoot:** = $(\text{Peak to Peak} / 2 - \text{Amplitude}) / \text{Amplitude}$.
- **Rise Overshoot:** = $(\text{Maximum} - \text{High}) / \text{Amplitude}$.
- **Fall Overshoot:** = $(\text{Minimum} - \text{Low}) / \text{Amplitude}$.
- **Amplitude:** half of the difference between the pulse top (High) and bottom (Low) settled value.
- **DC RMS:** Direct Current Root Mean Square is the entire power contained within the signal, including AC and DC components.
- **AC RMS:** Alternating Current Root Mean Square is used to characterize AC signals by subtracting out the DC power, leaving only the AC power component.

Horizontal-axis measurements for each channel:

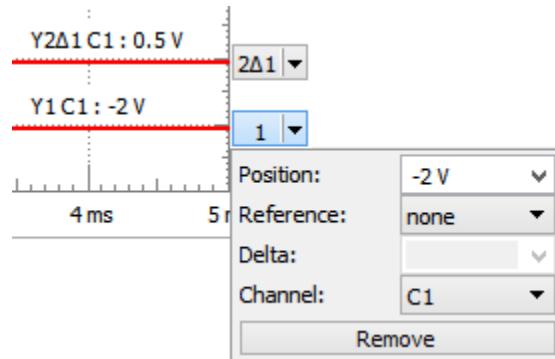
- **Cycles:** number of full cycles in visible acquisition data.
- **Frequency:** Frequency of the signal.
- **Period:** the period of the signal.
- **PosDuty:** positive duty of the signal.
- **NegDuty:** negative duty of the signal.
- **PosWidth:** positive pulse-width of the signal.
- **NegWidth:** negative pulse-width of the signal.
- **RiseTime:** rise time of the signal.
- **FallTime:** fall time of the signal.
- The **Cursors** are used to measure the amplitude, to indicate certain places on the waveform, such as band or channel limits. Using delta cursors, you can make measurements that deal with power change with frequency or time. These can be added by pressing the X button in the plot bottom left corner. The Y cursors in Scope main time plot can be added by the Y button in the top right corner. The first cursors are by default added as a normal cursor, the following ones as the delta of this, showing the difference. The cursors position can be modified by mouse drag, keyboard arrow keys, or adjustment control in the cursor's drop-down menu. The mouse button middle-click removes the cursor. The cursors can be selected with the channel number shortcut, pressing 1, 2,..
- The Cursor view enabled in the instrument's View menu shows the position and measurements in the table. The cursor's drop-down menu and the table as well, contain

adjustment controls for the reference cursor selection, position, delta value relative to reference cursor, and remove button. For horizontal cursors, the position is expressed in the horizontal axis unit and the vertical value is shown in intersection with each waveform.

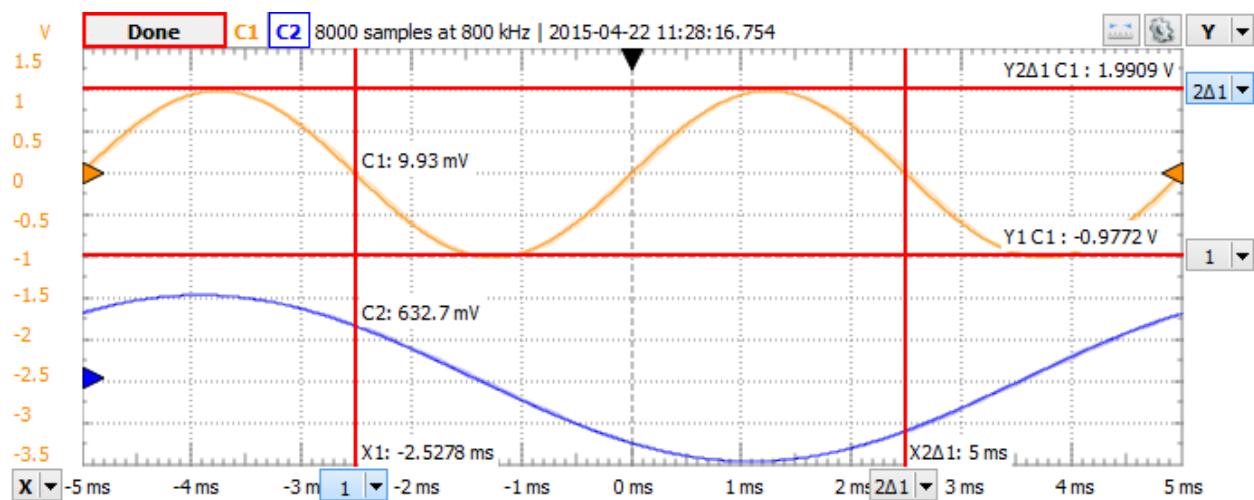
- The X and Y cursors are available for the main time view.



- The X cursor's drop-down menu contains adjustment controls for the position, reference cursor, *delta x* value, and remove button.

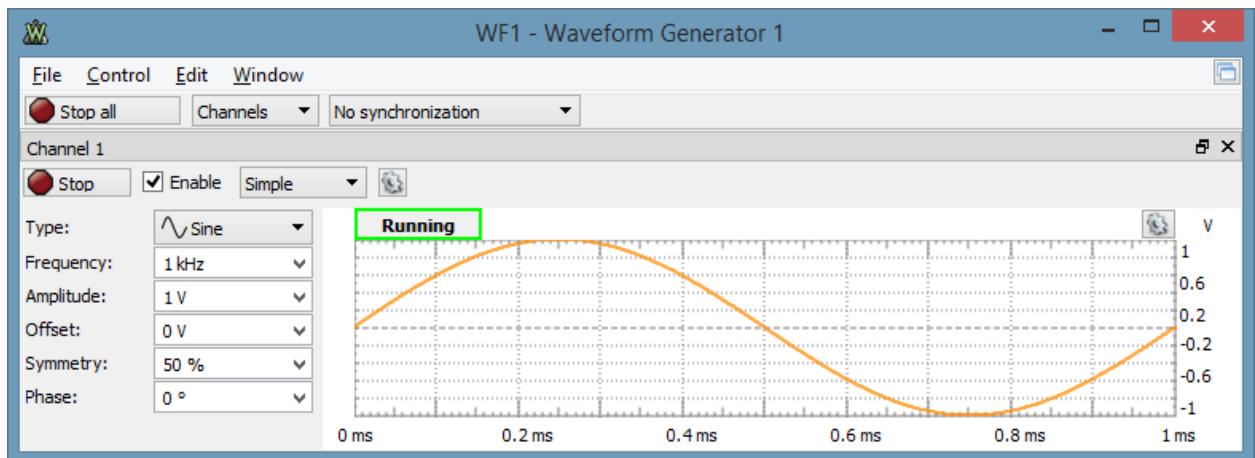


- The Y cursor's drop-down menu contains adjustment controls for the channel, position, reference cursor, delta value, and remove button.

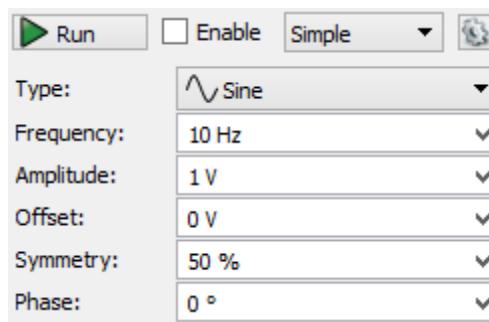


1.2.2 Wavegen

- Wave generator 1 (yellow) probe and wave generator 2 (yellow with white) probes are used to connect two channels of the wave generator.
- The Arbitrary Waveform Generator (or Wavegen) generates electronic waveforms. The waveforms can be either repetitive or single-shot. Different triggering sources can be used: internal (from other devices) or external.
- The resulting waveforms can be input into a device being tested and analyzed with the Oscilloscope as they progress through the device. This is useful for confirming the proper operation of the device or pinpointing a fault in the device.
- The main window has three areas: the control toolbar at the top, the configuration form(s) on the left side, and the signal preview plot(s) on the right side.



- The Simple configuration mode for a simple standard signal configuration.

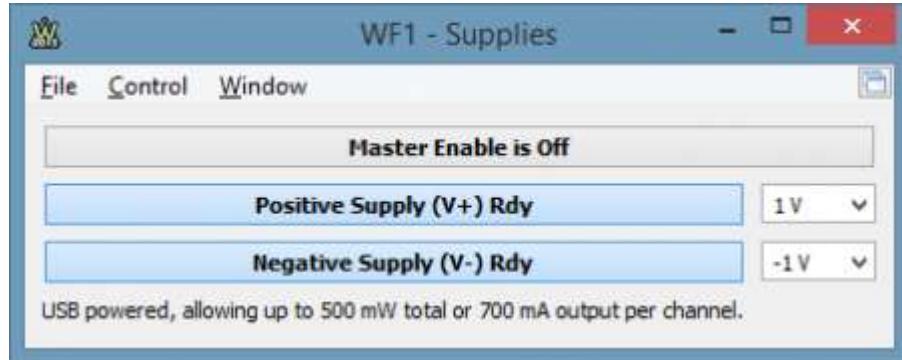


- **Type** represents the standard signal types: DC, Sine, Square, Triangle, Ramp-Up, Ramp-Down, Noise, Trapezium, and Sine-Power. Under the options menu, a Custom waveform can be created, and a file imported as a pattern or play data.
- For the Noise signal, the Frequency represents the DAC update rate, and the Symmetry and Phase parameters are disabled.

- Frequency, Amplitude, Offset, Symmetry, and Phase allows you to modify signal parameters.

1.2.3 Power Supplies

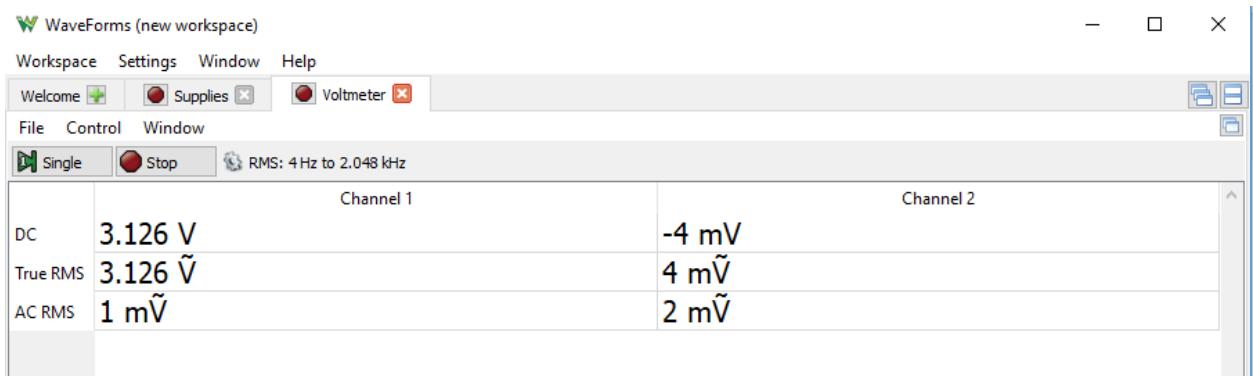
- V+ power supply (red probe) is used for positive power supply connection. V- power supply (white probe) is used for the negative power supply connection. Ground (black probe) is used as grounds for each connection respectively.
- This instrument allows you to enable the device's power supplies.



- **Master Enable** is the ON/OFF button: the master ON/OFF switches for the power supplies.
- **Positive/Negative Supply** button: the enable switches for each supply.
- **RDY** is shown when the supply is enabled but the master switch is OFF.
- **ON** is shown when the master switch is on and the supply is also enabled.
- **OFF** is shown when the supply is not enabled.

1.2.4. Voltmeter

- Both Scope ch.1 positive and negative probes, scope ch.2 positive and negative probes can be used for reading voltmeter readings as well.



2. Transistors Basics

2.1 Biasing: In order for a BJT to operate properly as an amplifier, the two pn junctions must be correctly biased with external dc voltages.

- Fig. 2.1 shows a bias arrangement of npn BJTs for operation as an amplifier. Notice that the base-emitter (BE) junction is forward-biased and the base-collector (BC) junction is reverse-biased. This condition is called forward-reverse bias

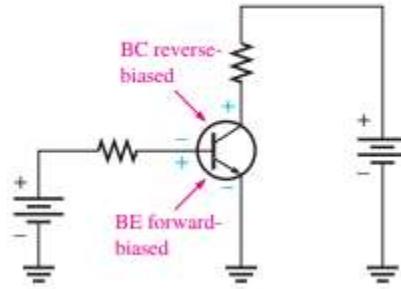


Fig. 2.1 Forward-reverse bias of a BJT

- The directions of the currents in an npn transistor and its schematic symbol are as shown in Fig. 2.2. Notice that the arrow on the emitter inside the transistor symbols points in the direction of conventional current. These diagrams show that the emitter current (I_E) is the sum of the collector current (I_C) and the base current (I_B), expressed as follows:

$$I_E = I_C + I_B \quad (1)$$

- As mentioned before, I_B is very small compared to I_E or I_C . The capital-letter subscripts indicate dc values.

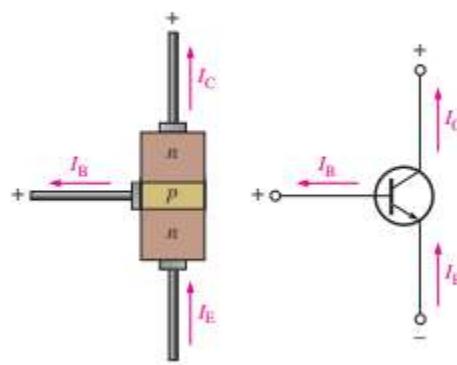


Fig. 2.2: Transistor currents

- When a transistor is connected to dc bias voltages, as shown in Fig. 2.3 for npn type, V_{BB} forward-biases the base-emitter junction, and V_{CC} reverse-biases the base-collector

junction. Although here we are using separate battery symbols to represent the bias voltages, in practice the voltages are often derived from a single dc power supply. For example, V_{CC} is normally taken directly from the power supply output and V_{BB} (which is smaller) can be produced with a voltage divider.

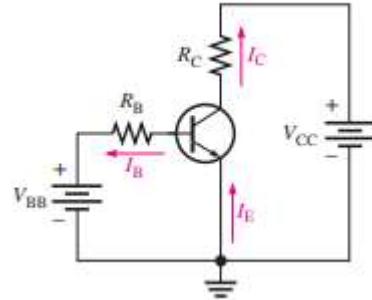


Fig. 2.3: Transistor dc bias circuit (similar to the circuit given in the lab manual 6 and fig. 6.1)

- The dc current gain of a transistor is the ratio of the dc collector current (I_C) to the dc base current (I_B) and is designated dc beta (β_{DC}).

$$\beta_{DC} = I_C / I_B \quad (2)$$

- The unsaturated BJT is a device with current input and a dependent current source in the output circuit, as shown in Fig. 2.4 for an npn. The input circuit is a forward-biased diode through which there is a base current. The output circuit is a dependent current source (diamond-shaped element) with a value that is dependent on the base current, I_B , and equal to $\beta_{DC}I_B$.

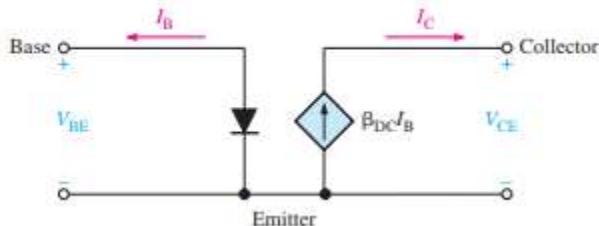


Fig. 2.4 Ideal dc model of an npn transistor

2.2 BJT circuit analysis:

- Consider the basic transistor bias circuit configuration in Fig. 2.5. Three transistor dc currents and three dc voltages can be identified.
 - I_B : dc base current
 - I_E : dc emitter current
 - I_C : dc collector current
 - V_{BE} : dc voltage at the base with respect to the emitter

- V_{CB} : dc voltage at collector with respect to the base
- V_{CE} : dc voltage at collector with respect to the emitter

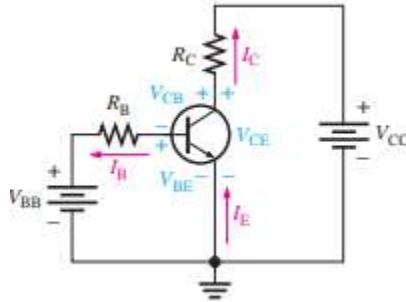


Fig. 2.5: Transistor currents and voltages

- The base-bias voltage source, V_{BB} , forward-biases the base-emitter junction, and the collector-bias voltage source, V_{CC} , reverse-biases the base-collector junction. When the base-emitter junction is forward-biased, it is like a forward-biased diode and has a nominal forward voltage drop of

$$V_{BE} \approx 0.7V \quad (3)$$

- Although in an actual transistor V_{BE} can be as high as 0.9 V and is dependent on current, we will use 0.7 V throughout this course in order to simplify the analysis of the basic concepts.
- Since the emitter is at ground (0 V), by Kirchhoff's voltage law, the voltage across R_B is

$$V_{R_B} = V_{BB} - V_{BE} \quad (4)$$

- Also, by Ohm's law,

$$V_{R_B} = I_B R_B \quad (5)$$

- Substituting for V_{R_B} yields

$$I_B R_B = V_{BB} - V_{BE} \quad (6)$$

- Solving for I_B ,

$$I_B = (V_{BB} - V_{BE}) / R_B \quad (7)$$

- The voltage at the collector with respect to the grounded emitter is

$$V_{CE} = V_{CC} - V_{R_C} \quad (8)$$

- Since the drop across R_C is

$$V_{R_C} = I_C R_C \quad (9)$$

- The voltage at the collector with respect to the emitter can be written as

$$V_{CE} = V_{CC} - I_C R_C \quad (10)$$

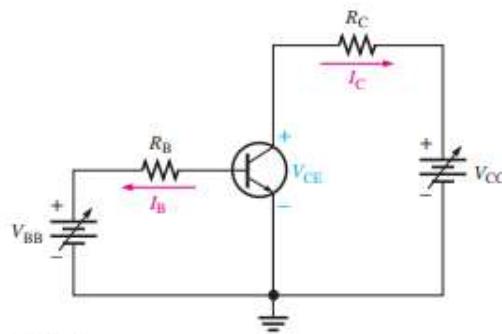
where $I_C = \beta_{DC} I_B$.

- The voltage across the reverse-biased collector-base junction is

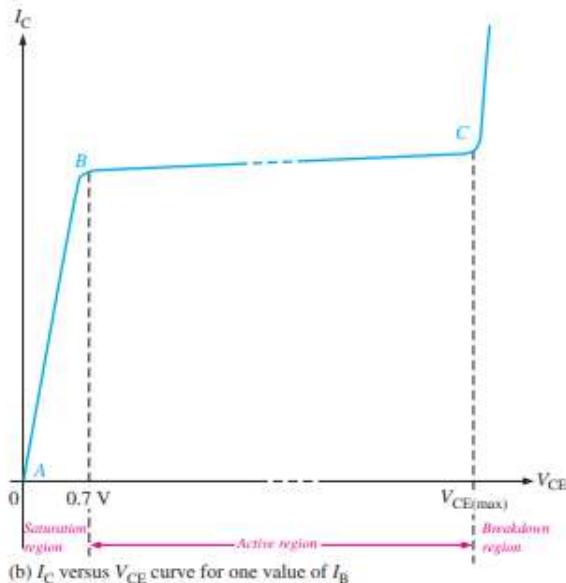
$$V_{CB} = V_{CE} - V_{BE} \quad (11)$$

2.3 Collector characteristic curves:

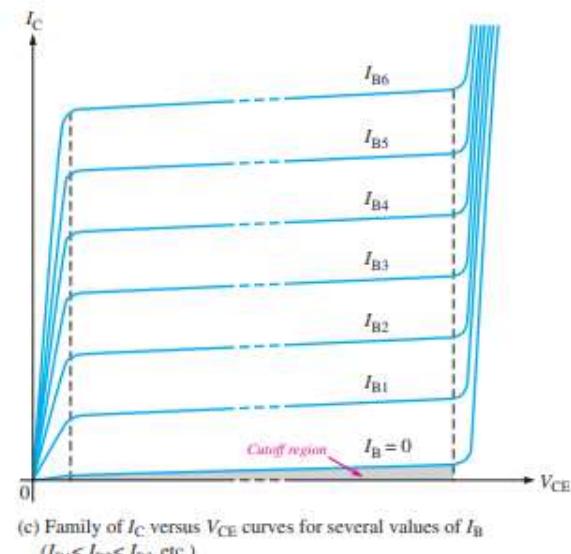
- Using a circuit like that shown in Fig. 2.6(a), a set of collector characteristic curves can be generated that show how the collector current, I_C , varies with the collector-to emitter voltage, V_{CE} , for specified values of base current, I_B . Notice in the circuit diagram that both V_{BB} and V_{CC} are variable sources of voltage. Assume that V_{BB} is set to produce a certain value of I_B and V_{CC} is zero. For this condition, both the base-emitter junction and the base-collector junction are forward-biased because the base is at approximately 0.7 V while the emitter and the collector are at 0 V. The base current is through the base-emitter junction because of the low impedance path to ground and, therefore, I_C is zero. When both junctions are forward-biased, the transistor is in the saturation region of its operation. *Saturation* is the state of a BJT in which the collector current has reached a maximum and is independent of the base current.
- As V_{CC} is increased, V_{CE} increases as the collector current increases. This is indicated by the portion of the characteristic curve between points A and B in Figure 4–10(b). I_C increases as V_{CC} is increased because V_{CE} remains less than 0.7 V due to the forward-biased base-collector junction.
- Ideally, when V_{CE} exceeds 0.7 V, the base-collector junction becomes reverse-biased and the transistor goes into the active, or linear, region of its operation. Once the base-collector junction is reverse-biased, I_C levels off and remains essentially constant for a given value of I_B as V_{CE} continues to increase. Actually, I_C increases very slightly as V_{CE} increases due to the widening of the base-collector depletion region. This results in fewer holes for recombination in the base region which effectively causes a slight increase in β_{DC} . This is shown by the portion of the characteristic curve between points B and C in Figure 4–10(b). For this portion of the characteristic curve, the value of I_C is determined only by the relationship expressed as $I_C = \beta_{DC} I_B$.
- When V_{CE} reaches a sufficiently high voltage, the reverse-biased base-collector junction goes into breakdown; and the collector current increases rapidly as indicated by the part of the curve to the right of point C in Fig 2.6(b). A transistor should never be operated in this breakdown region.
- A family of collector characteristic curves is produced when I_C versus V_{CE} is plotted for several values of I_B , as illustrated in Fig. 2.6(c). When $I_B = 0$, the transistor is in the cutoff region although there is a very small collector leakage current as indicated. The *cutoff* is the nonconducting state of a transistor. The amount of collector leakage current for $I_B = 0$ is exaggerated on the graph for illustration.



(a) Circuit



(b) I_C versus V_{CE} curve for one value of I_B



(c) Family of I_C versus V_{CE} curves for several values of I_B
($I_{B1} < I_{B2} < I_{B3}$, etc.)

Fig. 2.6 Collector characteristic curves

Cutoff: As previously mentioned, when $I_B=0$, the transistor is in the cutoff region of its operation. This is shown in Fig. 2.7 with the base lead open, resulting in a base current of zero. Under this condition, there is a very small amount of collector leakage current, I_{CEO} , due mainly to thermally produced carriers. Because I_{CEO} is extremely small, it will usually be neglected in circuit analysis so that $V_{CE}=V_{CC}$. In cutoff, neither the base-emitter nor the base-collector junctions are forward-biased. The subscript CEO represents collector-to-emitter with the base open.

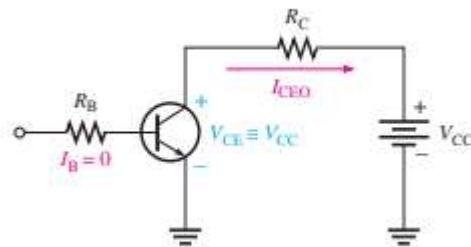


Fig. 2.7 Cutoff: collector leakage current

Saturation: When the base-emitter junction becomes forward-biased and the base current is increased, the collector current also increases ($I_C = \beta_{DC} I_B$) and V_{CE} decreases as a result of more drop across the collector resistor ($V_{CE} = V_{CC} - I_C R_C$). This is illustrated in Fig 2.8. When V_{CE} reaches its saturation value, $V_{CE}(\text{sat})$, the base-collector junction becomes forward-biased and I_C can increase no further even with a continued increase in I_B . At the point of saturation, the relation $I_C = \beta_{DC} I_B$ is no longer valid. $V_{CE}(\text{sat})$ for a transistor occurs somewhere below the knee of the collector curves, and it is usually only a few tenths of a volt.

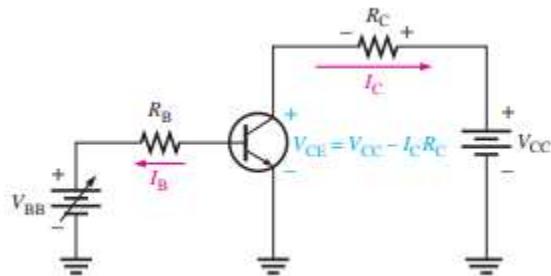


Fig. 2.8. Saturation

DC load line: Cutoff and saturation can be illustrated in relation to the collector characteristic curves by the use of a load line. Fig. 2.9 shows a dc load line drawn on a family of curves connecting the cutoff point and the saturation point. The bottom of the load line is at the ideal cutoff where $I_C = 0$ and $V_{CE} = V_{CC}$. The top of the load line is at saturation where $I_C = I_C(\text{sat})$ and $V_{CE} = V_{CE}(\text{sat})$. In between cutoff and saturation along the load line is the active region of the transistor's operation.

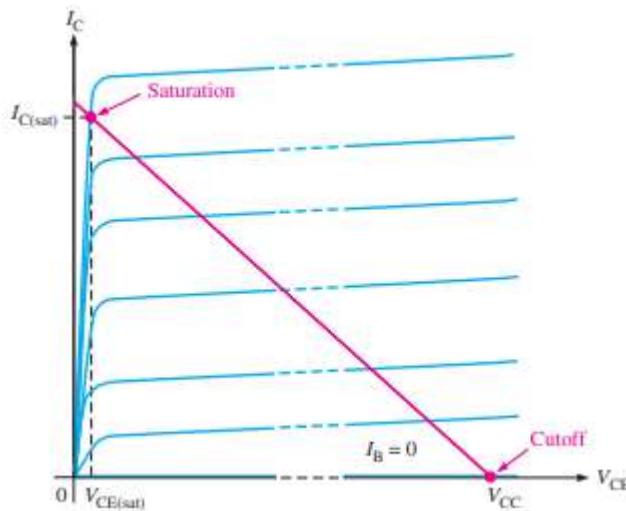


Fig. 2.9: DC load line on the family of collector characteristics curves.

2.4 Emitter Biasing: Emitter bias provides excellent bias stability in spite of changes in or temperature. It uses both a positive and a negative supply voltage. To obtain a reasonable estimate of the key dc values in an emitter-biased circuit, analysis is quite easy. In an npn circuit, such as shown in Fig2.10, the small base current causes the base voltage to be slightly below ground. The emitter voltage is one diode drop less than this. The combination of this small drop across R_B and V_{BE} forces the emitter to be at approximately -1V. Using this approximation, you can obtain the emitter current as

$$I_E = (-V_{EE} - 1V)/R_E \quad (12)$$

- V_{EE} is entered as a negative value in this equation.
- You can apply the approximation that $I_C \approx I_E$ to calculate the collector voltage.

$$V_C = V_{CC} - I_C R_C \quad (13)$$

- The approximation that $V_E \approx -1V$ and the neglect of β_{DC} may not be accurate enough for design work or detailed analysis. In this case, Kirchhoff's voltage law can be applied as follows to develop a more detailed formula for I_E . Kirchhoff's voltage law applied around the base-emitter circuit in Fig. 2.10(a), which has been redrawn in part (b) for analysis, gives the following equation:

$$V_{EE} + V_{R_B} + V_{BE} + V_{R_E} = 0 \quad (14)$$

- Substituting, using Ohm's law

$$V_{EE} + I_B R_B + V_{BE} + I_E R_E = 0 \quad (15)$$

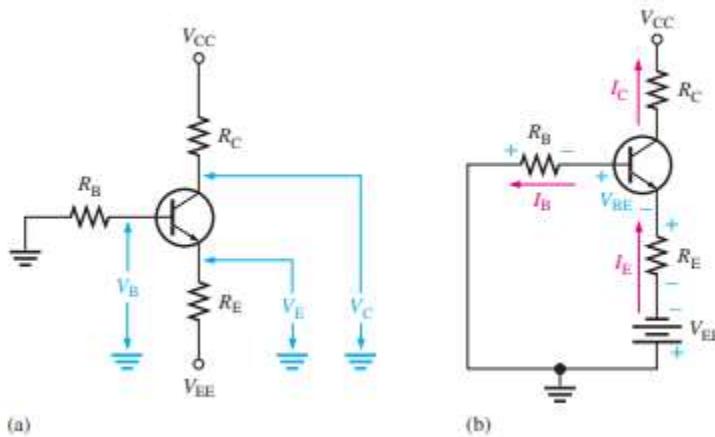


Fig. 2.10: Transistor emitter biasing (similar to the circuit diagram shown in lab # 6, figure6.2)

- Substituting for $I_B \approx I_E/\beta_{DC}$ and transposing V_{EE} ,

$$(I_E/\beta_{DC})R_B + I_E R_E + V_{BE} = -V_{EE} \quad (16)$$

- Factoring out I_E and solving for I_E ,

$$I_E = (-V_{EE} - V_{BE}) / (R_E + R_B / \beta_{DC}) \quad (17)$$

- Voltages with respect to the ground are indicated by a single subscript. The emitter voltage with respect to the ground is

$$V_E = V_{EE} + I_E R_E \quad (18)$$

- The base voltage with respect to ground is

$$V_B = V_E + V_{BE} \quad (19)$$

- The collector voltage with respect to ground is

$$V_C = V_{CC} - I_C R_C \quad (20)$$

2.5 Base Biasing: This method of biasing is common in switching circuits. Fig. 2.11 shows a base-biased transistor. The analysis of this circuit for the linear region shows that it is directly dependent on Starting with Kirchhoff's voltage law around the base circuit,

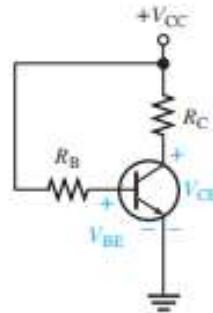


Fig. 2.11 Base biasing (similar to circuit shown in lab # 6, figure 6.1)

$$V_{CC} - V_{R_E} - V_{BE} = 0 \quad (21)$$

- Substituting $I_B R_B$ for V_{R_B} , we get

$$V_{CC} - I_B R_B - V_{EE} = 0 \quad (22)$$

- Then solving for I_B ,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad (23)$$

- Kirchhoff's voltage law applied around the collector circuit in Figure 2.11 gives the following equation:

$$V_{CC} - I_C R_C - V_{CE} = 0 \quad (24)$$

- Solving for V_{CE} ,

$$V_{CE} = V_{CC} - I_C R_C \quad (25)$$

- Substituting the expression for I_B into the formula $I_C = \beta_{DC}I_B$ yield

$$I_C = \beta_{DC} \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \quad (26)$$

Q-point stability of base bias: Notice that Equation (26) shows that I_C is dependent on β_{DC} . The disadvantage of this is that a variation in β_{DC} causes I_C and, as a result, V_{CE} to change, thus changing the Q-point of the transistor. This makes the base bias circuit extremely beta-dependent and unpredictable. Recall that β_{DC} varies with temperature and collector current. In addition, there is a large spread of values from one transistor to another of the same type due to manufacturing variations.

2.6 BJT as an Amplifier: Amplification is the process of linearly increasing the amplitude of an electrical signal and is one of the major properties of a transistor.

- Up to this point a separate dc source, V_{BB} was used to bias the base-emitter junction because it could be varied independently of V_{CC} and it helped to illustrate transistor operation. A more practical bias method is to use V_{CC} as the single-bias source, as shown in Fig. 2.12. To simplify the schematic, the battery symbol is omitted and replaced by a line termination circle with a voltage indicator (V_{CC}) as shown.

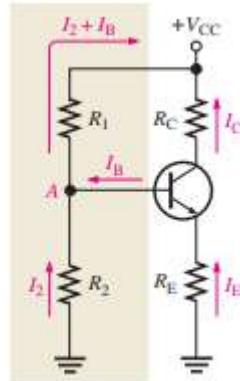


Fig. 2.12 Voltage-divider bias

- A dc bias voltage at the base of the transistor can be developed by a resistive voltage-divider that consists of R_1 and R_2 , as shown in Fig. 2.12. V_{CC} is the dc collector supply voltage. Two current paths are between point A and ground: one through R_2 and the other through the base-emitter junction of the transistor and R_E .
- Generally, voltage-divider bias circuits are designed so that the base current is much smaller than the current (I_2) through R_2 in Fig. 2.12. In this case, the voltage-divider circuit is very straightforward to analyze because the loading effect of the base current can be ignored. A voltage divider in which the base current is small compared to the current in R_2 is said to be a stiff voltage divider because the base voltage is relatively independent of different transistors and temperature effects.

- To analyze a voltage-divider circuit in which I_B is small compared to I_2 , first calculate the voltage on the base using the unloaded voltage-divider rule:

$$V_B \approx (R_2/R_1 + R_2)V_{CC} \quad (27)$$

- Once you know the base voltage, you can find the voltages and currents in the circuit, as follows:

$$V_E = V_B - V_{BE} \quad (28)$$

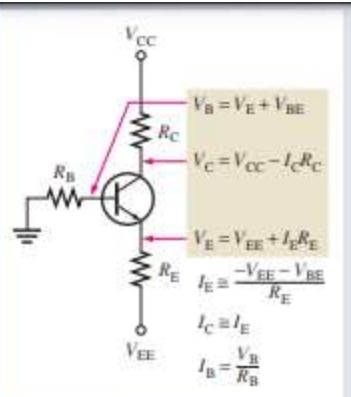
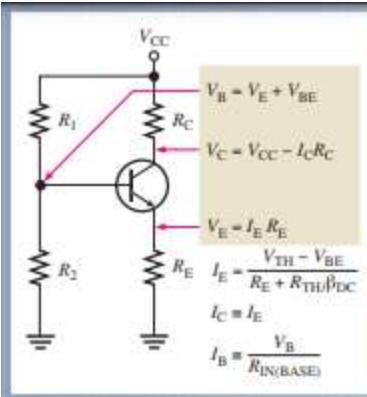
- and

$$I_C \approx I_E = V_E/R_E \quad (29)$$

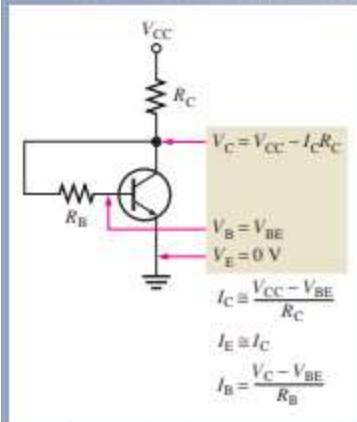
- then,

$$V_C = V_{CC} - I_C R_C \quad (30)$$

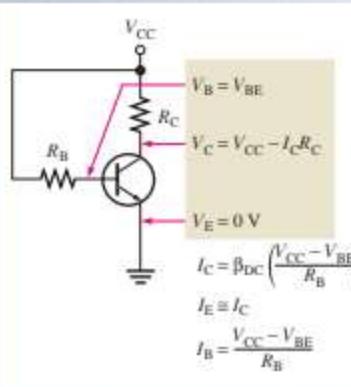
$$V_{CE} = V_C - V_E \quad (31)$$



COLLECTOR-FEEDBACK BIAS



BASE BIAS



EMITTER-FEEDBACK BIAS

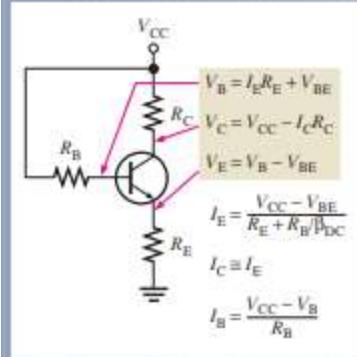


Fig. 2.13 summary of the transistor biasing circuits

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Lab 6

Transistor Base Biasing and Transistor Emitter Biasing

LAB 6.1: Transistor Base Biasing

PURPOSE AND BACKGROUND

The purpose of this experiment is to verify the voltages and currents in a base-biased circuit as well as to construct its dc load line. Despite its simplicity, a base-biased circuit does not efficiently stabilize a transistor's quiescent point. Consequently, the Q point is affected by the transistor's current gain (β).

PRELAB ASSIGNMENT (MUST BE SUBMITTED ONE DAY PRIOR TO CLASS)

Build circuits in Figures 6.1-1 and 6.2-1 in PSpice. Measure V_B , V_{CE} , I_B , I_C and β_{DC} values for the Transistor Base Biasing circuit shown in Figure 6.1-1. Measure V_B , V_E , V_C , V_{CE} , I_B , I_C and β_{DC} for the Transistor Emitter Biasing circuit shown in Figure 6.2-1. Calculate only the expected values for Tables 6.1-1, 6.2-1 and 6.2-2 using Useful Formulas at the end of this lab manual.

REQUIRED PARTS AND EQUIPMENT

- ❖ Resistors
 - 1 k Ω
 - 560 k Ω
 - 47 k Ω
- ❖ 9V battery
- ❖ DC power supply
- ❖ 1 M Ω potentiometer
- ❖ Two 2N3904 NPN silicon transistors
- ❖ DMM or VOM
- ❖ Breadboard
- ❖ Analog Discovery 2
- ❖ Jumper wires

PROCEDURE

1. Wire the circuit shown in the schematic diagram in Figure 6.1-1 and apply power to the breadboard. The pin diagram for the 2N3904 transistor is shown in Figure 6.1-2.
2. With your multimeter, measure the voltage across the base and collector resistors and using Ohm's law, determine the corresponding currents, recording your values in Table 6.1-1. From these two sets of values, determine the dc current gain or beta (β_{DC}) for this transistor so that

$$\beta_{DC} = I_C / I_B$$

Record this value of beta in Table 6-1.

3. Use your multimeter to measure individually V_B and V_{CE} . Record your results in Table 6.1-1.
4. Compare the values of Step 2 and 3 with the expected values, using the value of β_{dc} determined in Step 2 and a typical base emitter voltage of 0.7 V. Record these values in Table 6.1-1.

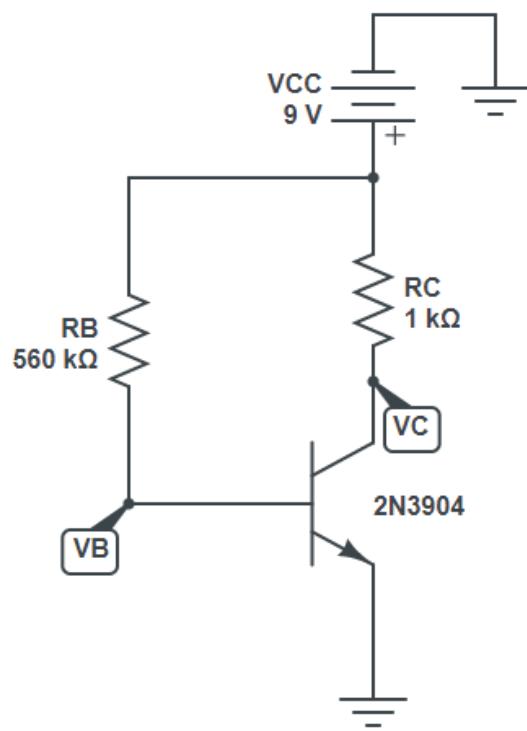


FIGURE 6.1-1: Schematic diagram of circuit

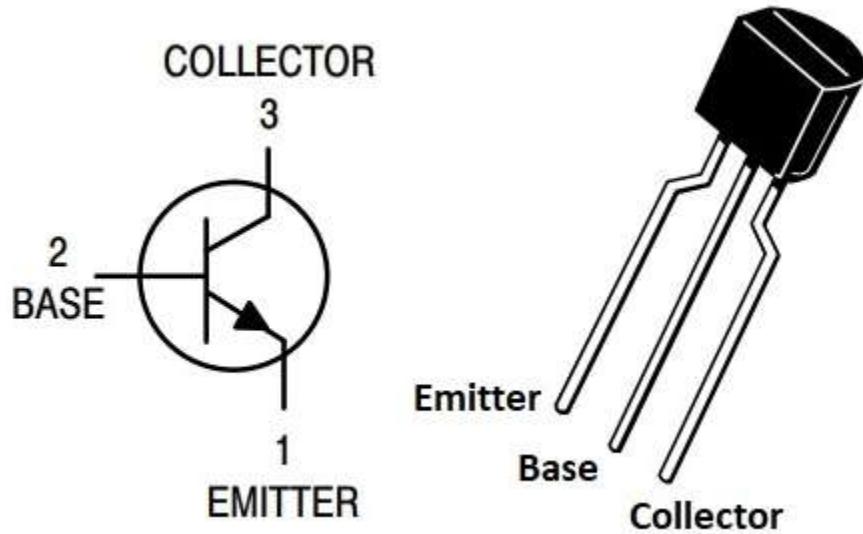


FIGURE 6.1-2: 2N3904 pin diagram

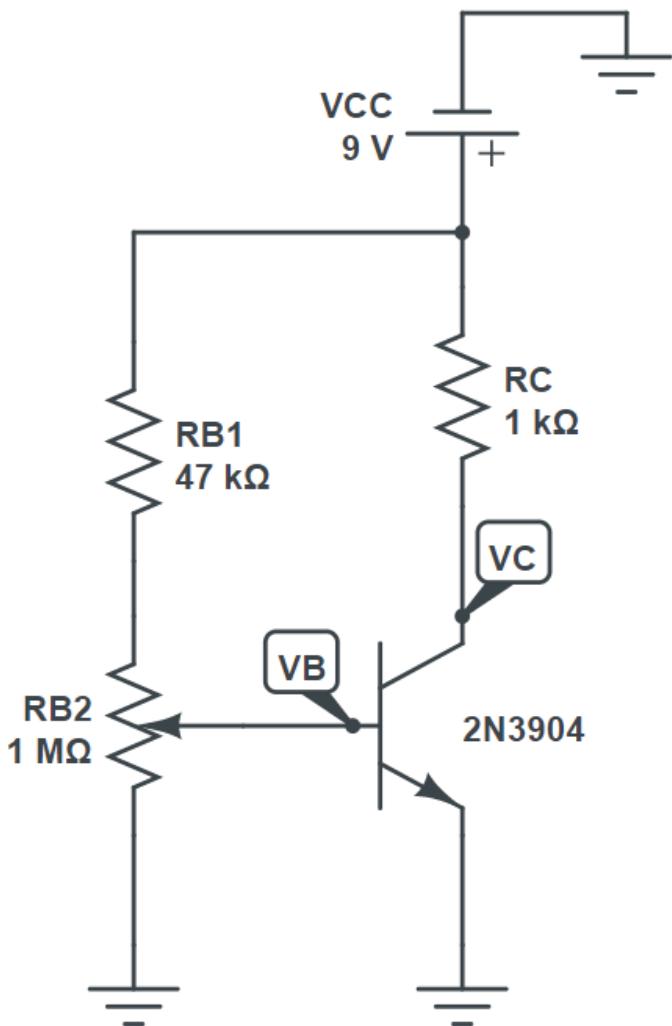


FIGURE 6.1-3: Schematic diagram of circuit

5. Using a different 2N3904 transistor, repeat Steps 2 through 4, and record your results in Table 6.1-1. Do you find any difference between the two transistors?
 - You will usually find that the two transistors give different values for the quiescent voltages and currents. In addition, you will usually find differences in the dc current gains
6. Using Equations 5 and 6 in the “Useful Formulas” section of this experiment, determine the saturation and cutoff points on the DC load line for this circuit and record these calculated values in Table 6.1-2. Create a graph and plot the DC load line using the calculated values of I_C (sat) and V_{CE} (off) as the endpoints of the load line. Plot the Q point based on the measured values of I_C and V_{CE} on the same graph. What do you notice about the Q point? (The graph can be created with computer software such as Microsoft Excel or drawn by hand.)
 - You should find that the measured Q point lies essentially on the DC load line.
7. Disconnect the power from the breadboard and rewire the circuit according to Figure 6.1-3. The 560 kΩ resistor (R_B) will be replaced with a 1 MΩ potentiometer in series with a 47 kΩ

resistor. Again, apply power to the breadboard and connect a voltmeter between the transistor's collector and emitter terminals.

8. Now vary the resistance of the potentiometer until V_{CE} as read by the voltmeter reaches a maximum value, V_{CE} (off). Then measure the corresponding collector current, I_C (off). Record both values in Table 6.1-2.
9. While continuing to measure the transistor's collector current (I_C), carefully vary the resistance of the $1\text{ M}\Omega$ potentiometer until the collector current reaches a maximum value. This then is the collector saturation current $I_{C(sat)}$. Now measure the corresponding collector-emitter voltage V_{CE} (sat). Record the values for both I_C (sat) and V_{CE} (sat) in Table 6.1-2.
 - At saturation, V_{CE} (sat) is ideally zero. While at cutoff, I_C (off) is zero. Plot the values for I_C and V_{CE} at cutoff and saturation on the graph constructed in Step 6. You should find that both points lie essentially on the dc load line very close to the ideal endpoints of cutoff and saturation.
10. Vary the potentiometer so that you can measure about five combinations of I_C and V_{CE} over the active region of the DC load line, while recording all values in Table 6.1-2. Then plot these values on the graph. As in Step 9, each point should lie essentially on the DC load line, as the load line is a plot of all possible combinations of I_C and V_{CE} .

FOR FURTHER INVESTIGATION

Try to design a base-biased circuit using a 15 V supply such that the collector-emitter voltage (V_{CE}) is set at approximately 7.5 V.

DATA FOR EXPERIMENT: TRANSISTOR BASE BIASING

Parameter	Transistor 1		Transistor 2	
	Measured Value	Expected Value	Measured Value	Expected Value
I_B				
I_C				
β_{DC}				
V_B		0.7 V (typical)		0.7 V (typical)
V_{CE}				

TABLE 6.1-1: DC Values

Condition	Calculated Values		Measured Values	
	I_C	V_{CE}	I_C	V_{CE}
Cutoff (Step 8)				
Saturation (Step 9)				
Active Region (Step 10)				

TABLE 6.1-2: DC Load Line

USEFUL FORMULAS

Quiescent DC base voltage

$$(1) \quad V_B = V_{CC} - I_B R_B \\ = V_{BE}$$

Quiescent DC collector (emitter)current

$$(2) \quad I_C = \frac{V_{CC} - V_{BE}}{R_B / \beta}$$

Quiescent DC base current

$$(3) \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Quiescent DC base current

$$(4) \quad V_{CE} = V_{CC} - I_C R_C$$

DC load line

$$(5) \quad I_C (\text{sat}) \cong \frac{V_{CC}}{R_C} \quad (\text{saturation})$$

$$(6) \quad V_{CE} (\text{off}) = V_{CC} (\text{cutoff})$$

...In general, make

$$(7) \quad V_{CC} \gg V_{BE}$$

LAB 6.2: Transistor Emitter Biasing

PURPOSE AND BACKGROUND

The purpose of this experiment is to verify the voltages and currents in an emitter-biased circuit as well as to construct its dc load line. Unlike other biasing schemes, emitter bias uses both a positive and a negative supply voltage. In this manner, the base is approximately at ground while the negative emitter-supply voltage forward biases the base-emitter junction.

PRELAB ASSIGNMENT (MUST BE SUBMITTED ONE DAY PRIOR TO CLASS)

(Included as part of 6.1 prelab assignment)

REQUIRED PARTS AND EQUIPMENT

- ❖ Resistors
 - Two 1 kΩ
 - 4.7 kΩ
- ❖ 9V battery
- ❖ Two 2N3904 NPN silicon transistors
- ❖ DMM or VOM
- ❖ Breadboard
- ❖ Digital Multimeter
- ❖ DC Power Supply
- ❖ Jumper wires

PROCEDURE

1. Wire the circuit shown in the schematic diagram in Figure 6.2-1 and apply power to the breadboard. The pin diagram for the 2N3904 transistor is shown in Figure 6.2-2.
2. With your Digital Multimeter, measure the base, emitter, and collector voltages, with respect to ground. Also measure the base and collector currents. Record the values in Table 6.2-1. From these two sets of values, determine the DC current gain or beta (β_{DC}) value for this transistor so that...
- 3.

$$\beta_{DC} = I_C / I_B$$

Record this value of beta in Table 6.2-1.

4. Use your multimeter to measure V_{CE} . Record the results in Table 6.2-1.
5. Compare the values of Steps 2 and 3 with the expected values, using the value of β_{DC} determined in Step 2 and a typical base-emitter voltage of 0.7 V. Record these values in Table 6.2-1.

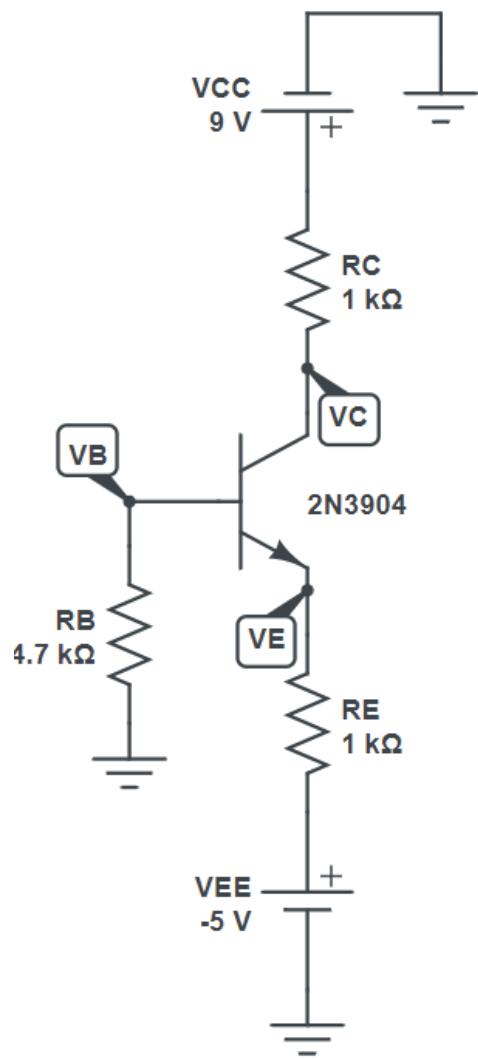


FIGURE 6.2-1: Schematic diagram of circuit

**(for use with AD2 device, use 9V battery for V_{CC} and -5V DC power supply from AD2 for V_{EE})*

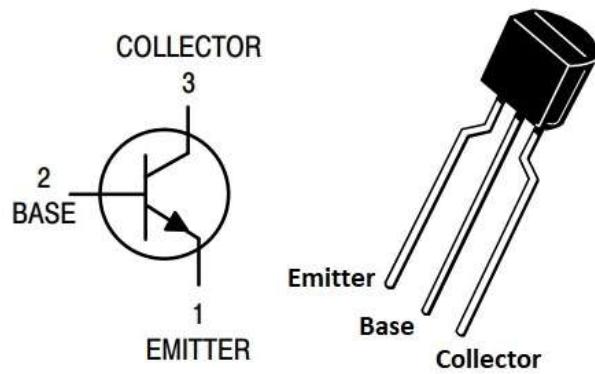


FIGURE 6.2-2: 2N3904 pin diagram

6. Using a different 2N3904 transistor, repeat Steps 2 through 4, and record your results in Table 6.2-1. Do you find any difference between the two transistors?
 - a. You will usually find that the two transistors give different values for the quiescent voltages and currents. In addition, you will usually find differences in the dc current gains
7. Using Equation 7 and 8 in the “Useful Formulas” section of this experiment, determine the saturation and cutoff points on the dc load line for this circuit and record these calculated values in Table 6.2-2. Create a new graph and plot the DC load line using the calculated values of $I_C(\text{sat})$ and $V_{CC}(\text{off})$ as the endpoints of the load line. Now plot the Q point based on the measured values of I_C and V_{CE} on this same graph. What do you notice about the Q point?
 - b. You should find that the measured Q point lies essentially on the DC load line.

DATA FOR EXPERIMENT: TRANSISTOR Emitter Biasing

Parameter	Transistor 1		Transistor 2	
	Measured Value	Expected Value	Measured Value	Expected Value
I_C				
I_B				
β_{DC}				
V_B				
V_C				
V_E				
V_{CE}				

TABLE 6.2-1: DC values

Parameter	Calculated Value
$V_{CE(\text{off})}$	
$I_C(\text{sat})$	

TABLE 6.2-2: Cutoff and Saturation

USEFUL FORMULAS

Quiescent DC emitter voltage

$$(1) V_E = V_C - V_{CE}$$

Quiescent DC base voltage

$$(2) V_B = |V_{EE}| - I_E R_E - V_{BE} \text{ (ideally equal to zero)}$$

Quiescent DC collector (emitter) current

$$(3) I_C = \frac{|V_{EE}| - V_{BE}}{R_E + (\frac{R_B}{\beta})} \quad (I_C \approx I_E \text{ for large } \beta)$$

Quiescent DC base current

$$(4) I_B = \frac{V_B}{R_B} \approx \frac{|V_{EE}| - V_{BE}}{\beta R_E + R_B}$$

Quiescent DC collector-to-emitter voltage

$$(5) V_{CE} = V_{CC} - I_C \cdot R_C + V_{BE}$$

$$(6) V_C = V_{CC} - I_C \cdot R_C$$

DC Load Line

$$(7) I_C (\text{sat}) = \frac{V_{CC} + |V_{EE}|}{R_C + R_E} \quad (\text{saturation})$$

$$(8) V_{CE} (\text{off}) = V_{CC} + |V_{EE}| \quad (\text{cutoff})$$

...In general, make

$$(9) |V_{EE}| \gg V_{BE}$$

$$(10) R_E \gg R_B / \beta$$

POST LAB ASSIGNMENT (MUST BE INCLUDED IN LAB REPORT)

* Must include screenshots of all measurements, using the Waveforms software, as well as a picture of the physical circuit.

** Use 9 V battery for V_{CC} and the negative power supply from the AD2 device for V_{EE} . Also use AD2 device for use of a voltmeter.

1. Why is BJT named as Bipolar Junction Transistor?

2. In the Base Biasing circuit in Figure 6.1-1, what happens if the current gain increases?
 - a) I_B decreases
 - b) I_C increases
 - c) V_{CE} decreases
 - d) All the above

3. In the Base Biasing circuit in Figure 6.1-1, if the base resistor (R_B) is reduced, then...
 - a) I_B decreases
 - b) V_{CE} decreases
 - c) I_C increases
 - d) All the above

4. In the Emitter Biasing circuit in Figure 6.2-1, what happens if the current gain increases?
 - a) I_C decreases
 - b) V_B increases
 - c) V_{CE} decreases
 - d) All the above

5. Modify the schematic of the circuit shown in Figure 6.1-1 so that $V_{CE} \approx 8.5$ V. Make sure the current gain remains almost the same, even after the circuit is modified. Measure I_B , I_C , β_{DC} , V_B and V_{CE} .
Note: Include your calculations for the resistor values that you used to get $V_{CE} \approx 8.5$ V. Also include your voltmeter reading screenshots for V_{CE} , I_B , I_C , β_{DC} , V_B in the report.

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Lab 7

Common-Emitter Amplifier

LAB 7: Common-Emitter Amplifier

PURPOSE AND BACKGROUND

The purposes of this experiment are to (1) demonstrate the operation and characteristics of the small-signal common-emitter amplifier and (2) investigate what influences its voltage gain. The common-emitter amplifier is characterized by application of the amplifier input signal to the base lead while its output is taken from the collector, which always gives a 180° phase shift.

PRELAB ASSIGNMENT (MUST BE SUBMITTED ONE DAY PRIOR TO CLASS)

Build the circuit in Figure 7-1 in PSpice and measure peak-to-peak voltages for both input and output waveforms. What is the phase relationship between the input and output waveforms? Calculate the expected values for Tables 7-1, 7-2, and 7-3 using Useful Formulas at the end of this lab manual.

REQUIRED PARTS AND EQUIPMENT

- ❖ Resistors
 - 100 Ω
 - 220 Ω
 - 1 k Ω
 - 4.7 k Ω
 - Two 10 k Ω
- ❖ Capacitors
 - Two 2.2 μF
 - 100 μF
- ❖ 2N3904 NPN silicon transistor
- ❖ DC power supply
- ❖ Analog Discovery 2
- ❖ Breadboard

PROCEDURE

1. Wire the circuit shown in Figure 7-1, omitting the signal generator and the power supply. The pin diagram for the 2N3904 diode is given in Figure 7-2.
2. After you have checked all connections, apply the 9 V supply voltage to the breadboard. With a multimeter, individually measure the transistor DC base, emitter, and collector voltages with respect to ground, recording your results in Table 7-1. Based on the resistor values of Figure 7-1, determine the expected values of these three voltages, assuming a base-emitter voltage drop of 0.7 V (Equations 6, 7 and 9). Compare these calculated values with the measured values in Table 7-1.

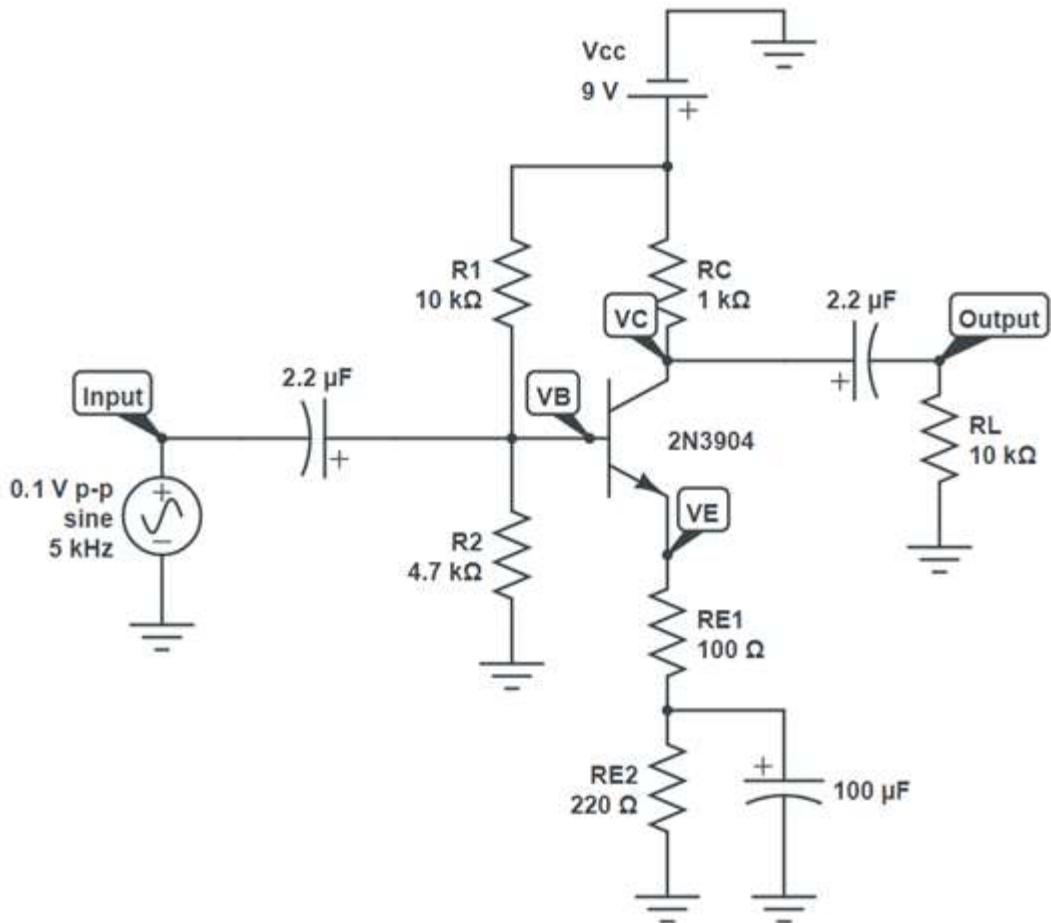


FIGURE 7-1: Schematic Diagram of Circuit
(*Use 9V external battery for use with AD2 device in post lab assignment)

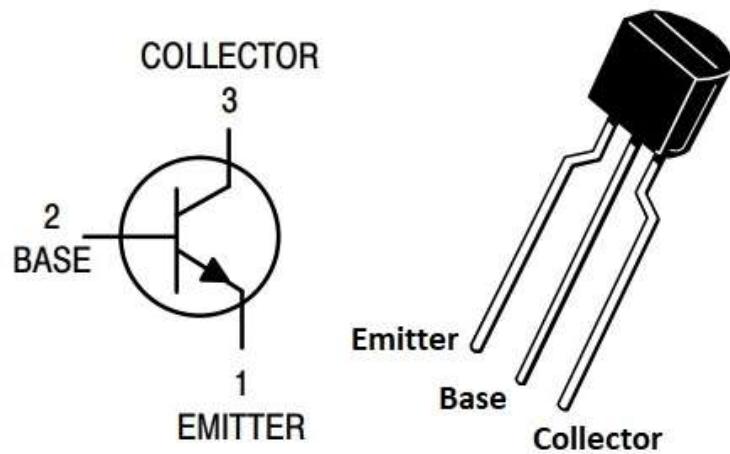


FIGURE 7-2: 2N3904 Transistor Pinout

3. Using the measured value for the DC emitter voltage in Step 2, calculate the DC emitter current (Equation 8) and the resultant transistor AC emitter resistance, r'_e (Equation 5). Record these values in table 7-2.
4. Connect the Channel 1 probe of the oscilloscope to the node labeled “Input” (v_{in}) and connect the Channel 2 probe to the node labeled “Output” (v_{out}), as depicted in Figure 7-1. Make sure that the sine wave output level of the signal generator is at 0.2 v_{p-p} at a frequency of 5 kHz.

You should observe that the output signal level (v_{out}) is greater than the input level (v_{in}). In addition, v_{out} is inverted, or 180° out of phase, with respect to the input. These points are two major characteristics of a common-emitter amplifier. Note, to observe the phase shift, you must display both signals simultaneously on the oscilloscope; otherwise, you will not see the phase shift.

5. With an oscilloscope, measure the AC peak-to-peak voltage at the junction of R_{E1} (100 Ω) and R_{E2} (220 Ω). Even at the oscilloscope’s highest input sensitivity, you should measure virtually no AC voltage at this point. The 100 μF bypass capacitor, in parallel with R_{E2} , serves essentially as a short-circuit path to ground since its reactance at 5 kHz is very small compared with the 220 Ω resistance. Consequently, the junction of R_{E1} and R_{E2} is effectively at AC ground.
6. Calculate the expected voltage gain from the base to the collector using the Equation 2 given in the “Useful Formulas” section and record the value in Table 7-2. Now measure the actual voltage v_{out} by the peak-to-peak input voltage v_{in} , recording your result in Table 7-3. Also record the measured gain from the measured input and output voltages in Table 7-3.
7. Now remove R_L . You should observe that the output voltage level increases. It does so because the load resistance affects the voltage gain of the amplifier stage. As in Step 6, experimentally determine the voltage gain by measuring v_{out} and v_{in} , comparing your measured result with the expected value (Equation 3). Record your results in Table 7-3.
8. Now reconnect the 10 k Ω resistor, R_L . Remove the 100 μF emitter bypass capacitor from the circuit. You should observe that the output voltage decreases tremendously. It does so because the total AC emitter resistance, r'_e . As in the previous two steps, experimentally determine the voltage gain by measuring v_{out} and v_{in} , comparing your results with the expected value (Equation 4). Record your results in Table 7-3.

From the results in Table 7-3, you should now understand how both the emitter bypass capacitor and the load resistance affect the base-to-collector voltage gain of a common-emitter amplifier.

WHAT YOU HAVE DONE

This experiment demonstrated the operation and characteristics of a small-signal common-emitter amplifier, which has 180° phase shift. Here, the input signal is applied to the transistor's base lead, while the output signal is taken from the collector lead. The experiment also showed how the load resistance and emitter bypass capacitor each influence the circuit's voltage gain.

DATA FOR EXPERIMENT: THE COMMON-EMITTER AMPLIFIER

Parameter	Measured Value	Expected Value	% Error
V_B			
V_E			
V_C			

TABLE 7-1: DC values

Parameter	Value
I_E (calculated)	mA
r'_e (calculated)	Ω

TABLE 7-2: AC emitter resistance

Condition	V_{in}	V_{out}	Measured Gain	Expected Gain	% Error
Normal Circuit (Step 6)					
No Load (Step 7)					
No Bypass Capacitor (Step 8)					

TABLE 7-3: Amplifier gain

USEFUL FORMULAS

Voltage gain from base to collector

$$(1) A_v = \frac{v_{out}}{v_{in}} \quad (\text{measured voltage gain})$$

$$(2) A_v = \frac{R_C || R_L}{R_{E1} + r'_e} \quad (\text{normal circuit with load})$$

$$(3) A_v = \frac{R_C}{R_{E1} + r'_e} \quad (\text{no load})$$

$$(4) A_v = \frac{R_C || R_L}{R_{E1} + R_{E2} + r'_e} \quad (\text{no bypass capacitor})$$

Transistor AC emitter resistance (at normal room temperature)

$$(5) r'_e \cong \frac{25 \text{ mV}}{I_E}$$

Quiescent DC base voltage

$$(6) V_B = \left(\frac{R_2}{R_1 + R_2} \right) \cdot V_{CC}$$

Quiescent DC emitter voltage

$$(7) V_E = V_B - V_{BE}$$

Quiescent DC emitter current

$$(8) I_E = \frac{V_E}{R_{E1} + R_{E2}} \quad (I_C \approx I_E \text{ for large } \beta)$$

Quiescent DC collector voltage

$$(9) V_C = V_{CC} - I_C \cdot R_C$$

Quiescent DC collector-emitter voltage

$$(10) V_{CE} = V_{CC} - I_C (R_C + R_{E1} + R_{E2})$$

POST LAB ASSIGNMENT (MUST BE INCLUDED IN LAB REPORT)

***Use AD2 device to complete post lab assignment. Note that since the AD2 does not support 9 V DC power supply, use 5 V for V_{cc} .**

Note: Include your circuit diagram, input-output waveforms, DC voltage readings screenshots for each of the following questions.

- 1) Restore the circuit to that of Figure 7-1. With a two-channel oscilloscope, compare the input and output waveforms. What is the phase relationship between v_{in} and v_{out} ?
- 2) Remove the 100 μ F bypass capacitor from the circuit. Measure the voltage gain of the amplifier. What conclusion can you make about the amplifier's performance with bypass capacitor open?
- 3) Replace the 100 μ F capacitor, and reduce R_L to 1 k Ω . Measure the voltage gain of the amplifier. What conclusion can you make about the amplifier's performance with R_L reduced to 1 k Ω ?
- 4) Replace R_L with the original 10 k Ω resistor and open R_{E1} . Measure the DC voltages at the base, emitter, and the collector. Is the transistor in cutoff or saturation? Explain.
- 5) Replace R_{E1} and open R_2 . Measure the DC voltages at the base, emitter, and the collector. Is the transistor in cutoff or saturation? Explain

Lab 8

Common-Collector Amplifier (Emitter-Follower)

LAB 8: Common-Collector Amplifier (Emitter-Follower)

PURPOSE AND BACKGROUND

The purposes of this experiment are (1) to demonstrate the operation and characteristics of the small-signal common-collector amplifier and (2) to investigate what influences its voltage gain. The common-collector amplifier, often referred to as an emitter-follower, is characterized by application of the amplifier input signal to the base lead while its output is taken from the emitter. The output signal is never larger than the input but is always in-phase with the input. Consequently, the output follows the input. The main advantage is that the input impedance of a common-collector amplifier is generally much higher than for other bipolar transistor circuits.

PRELAB ASSIGNMENT (MUST BE SUBMITTED ONE DAY PRIOR TO CLASS)

Build the circuit in Figure 8-1 in PSpice. Measure the peak-to-peak voltages for both input and output waveforms. What is the phase relationship between the input and output waveforms? Calculate the expected values for Tables 8-1, 8-2, and 8-3 using Useful Formulas at the end of this lab manual.

REQUIRED PARTS AND EQUIPMENT

- ❖ Resistors
 - 330 Ω
 - 100 Ω
 - Two 1 k Ω
 - 22 k Ω
 - 27 k Ω
- ❖ Capacitors
 - 2.2 μF
 - 100 μF
- ❖ 2N3904 NPN silicon transistor
- ❖ DC power supply
- ❖ Analog Discovery 2
- ❖ Breadboard

PROCEDURE

1. Wire the circuit shown in Figure 8-1, omitting the signal generator and the power supply.
2. After you have checked all the connections, apply the 9 V supply voltage to the breadboard. With a multimeter, individually measure the transistor DC base and emitter voltages with respect to ground, recording your results in Table 8-1. Based on the resistor values of Figure 8-1, determine the expected values of those two voltages (Equations 3 and 4), assume a base emitter (V_{BE}) voltage of 0.7 V, and calculate the % of Error (Table 8-1).

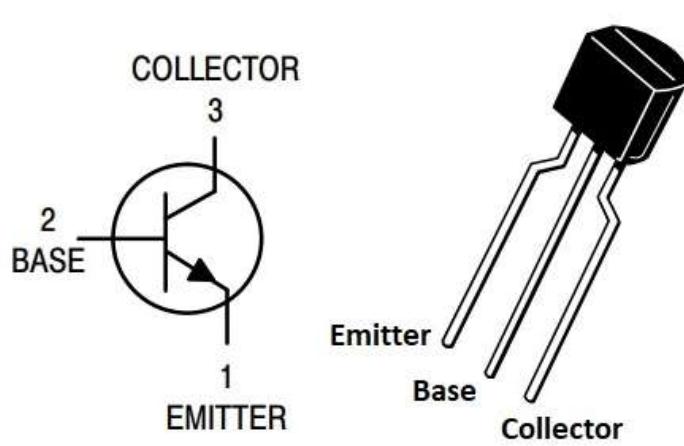
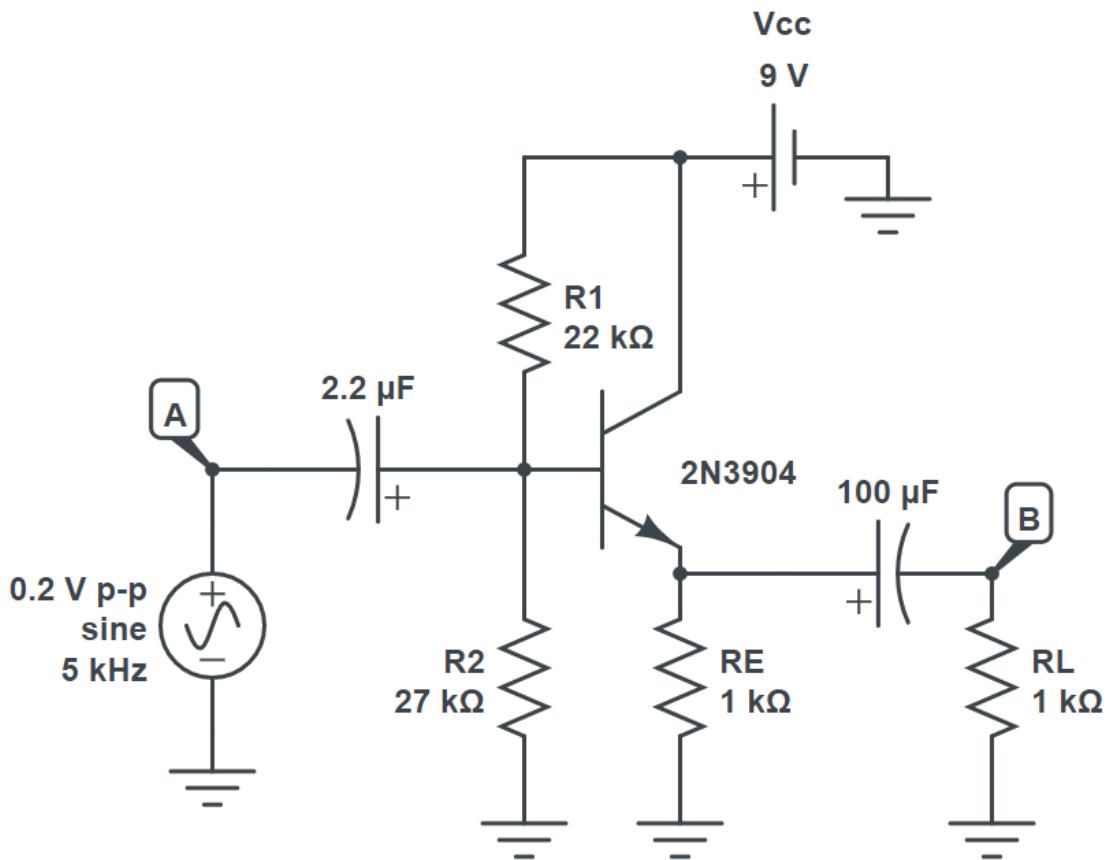


FIGURE 8-2: 2N3904 Pin Diagram

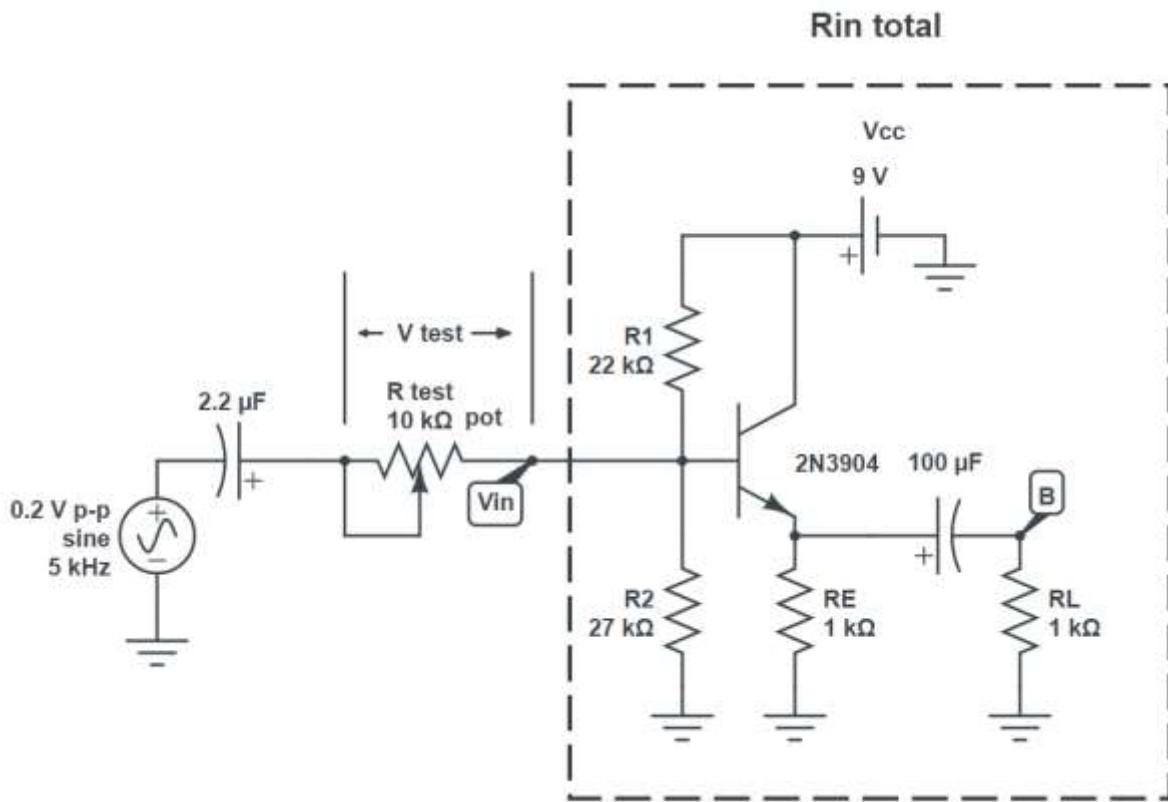


FIGURE 8-3: Measurement of $R_{in(total)}$

3. Using the measured value for the DC emitter voltage obtained in Step 2, calculate the DC emitter current I_E and the resultant transistor AC emitter resistance r'_e (Equations 5 and 2). Record these values in Table 8-2.
4. Connect Channel 1 of your oscilloscope at point A (v_{in}) and Channel 2 to point B (v_{out}). Then connect the signal generator to the circuit as shown in Figure 8-1 and adjust the sine wave output level of the generator at 0.2 V peak-to-peak at a frequency of 5 kHz.
You should observe that the output signal level (v_{out}) is very nearly the same as the input level (v_{in}). In addition, there is no phase shift. These points are two major characteristics of a common-collector amplifier.
5. Using the oscilloscope, measure the AC peak-to-peak at both input (point A) and output voltage across the 1 kΩ load resistor (or at point B). Calculate the expected voltage gain from base to emitter (Equation 1). Record this result in Table 8-3. Now measure the actual voltage gain by dividing the peak-to-peak output voltage v_{out} by the peak-to-peak input voltage v_{in} , record your result in Table 8-3.
6. Complete Table 8-3, repeating Step 4 and 5 with the load resistance values specified. You should observe that the output voltage level decreases slightly. It does so because the load resistance affects the voltage gain of the amplifier stage. As in Step 5, experimentally determine the voltage gain by measuring the v_{out} and v_{in} . Compare your measured result with the expected value (Equation 1). Record the results in Table 8-3.

7. Replace the load resistor R_L to $1k\ \Omega$. Insert a $10k\ \Omega$ potentiometer in between the base and the C1 capacitor as shown in Figure 8-3. Set the potentiometer to the point that the output peak to peak voltage (for $R_L = 1k\ \Omega$) drops to half of the previous output (Step 5). Then measure the resistance of the potentiometer, which will be $R_{in(tot)}$. Use the measured $R_{in(tot)}$ and R_L to determine the measured power gain. Record this value in Table 8-4.

WHAT YOU HAVE DONE

This experiment demonstrated the operation and characteristics of a small-signal common-collector amplifier (or emitter-follower), which has no phase shift. Here, the input signal is applied to the transistor's base lead, while the output signal is taken from the emitter lead. The experiment also showed the load resistance influenced the circuit's voltage gain.

DATA FOR EXPERIMENT: THE COMMON COLLECTOR AMPLIFIER (EMITTER-FOLLOWER)

Parameter	Measured Value	Expected Value	% Error
V_B			
V_E			

TABLE 8-1: DC Values

Parameter	Value
I_E (calculated)	mA
r'_e (calculated)	Ω

TABLE 8-2: AC Emitter Resistance

Load Resistance	v_{in}	v_{out}	Measured Gain	Expected Gain	% Error
$1 k\Omega$					
100Ω					
330Ω					

TABLE 8-3: Amplifier Gain

AC Parameter	Measured Value	Expected Value
R_{in} (total)		
A_p		

TABLE 8-4: Common-Collector AC Parameters

USEFUL FORMULAS

Voltage Gain from Base to Emitter

$$(1) \quad A_v = \frac{v_{out}}{v_{in}} = \frac{I_e(R_E||R_L)}{I_e((R_E||R_L)+r'_e)} = \frac{R_E||R_L}{R_E||R_L+r'_e}$$

Transistor AC Emitter Resistance (at normal room temperature)

$$(2) \quad r'_e \cong \frac{25 \text{ mV}}{I_E}$$

Quiescent DC Base Voltage

$$(3) \quad V_B = \left(\frac{R_2}{R_1+R_2} \right) \cdot V_{CC}$$

Quiescent DC Emitter Voltage

$$(4) \quad V_E = V_B - V_{BE}$$

Quiescent DC Emitter Current

$$(5) \quad I_E = \frac{V_E}{R_E}$$

Amplifier Input Impedance

$$(6) \quad R_{in} = R_1 || R_2 || (\beta_{ac} [(R_E || R_L) + r'_e])$$

Amplifier Power Gain

$$(7) \quad A_p = \frac{\frac{v_{out}^2}{R_L}}{\frac{v_{in}^2}{R_{in(tot)}}} = A_v^2 \left(\frac{R_{in(tot)}}{R_L} \right) = \frac{R_{in(tot)}}{R_L}$$

POST LAB ASSIGNMENT (TO BE INCLUDED IN LAB REPORT)

1. The voltage gain of a common-collector amplifier, or an emitter-follower, is always
 - a. greater than 1
 - b. equal to 1
 - c. less than 1
2. The output signal of a common-collector amplifier is out-of-phase with the input by
 - a. 0°
 - b. 45°
 - c. 90°
 - d. 180°
3. If the load resistor in the circuit is increased, the voltage gain will
 - a. Increase significantly
 - b. Decrease significantly
 - c. Remain essentially the same
4. For the voltage gain to approach 1...
 - a. R_L must be omitted
 - b. R_L must be shorted
 - c. β must be as large as possible
 - d. r_e' must be as small as possible
5. Design a common-collector amplifier circuit (similar to the circuit shown in Figure 8.1 in the lab manual) with a power gain of 3 and load resistor R_L as $1\text{ k}\Omega$. Include your circuit diagram, input and output waveforms from the Waveforms application.

Lab 9

Class B Push-Pull Emitter-Follower Power Amplifier

LAB 9: The Class B Push-Pull Emitter-Follower Power Amplifier

PURPOSE AND BACKGROUND

The purpose of this experiment is to demonstrate the design and operation of a Class B push-pull emitter-follower power amplifier. The Class B push-pull amplifier has a pair of complementary (NPN and PNP) transistors, each of which is biased at cutoff (that is, no collector current). Consequently, collector current in each transistor flows only for alternate half-cycles of the input signal. Since both transistors are biased at cutoff, the input signal must be sufficient to forward bias each transistor on the appropriate half-cycle of the input waveform. As a result, crossover distortion occurs.

To eliminate crossover distortion, both transistors should under quiescent conditions be slightly forward biased so that each transistor is biased slightly before cutoff, resulting in a small amount of current called the *trickle current*. Since we now have neither true Class A nor true Class B operation, but rather something in between, this operation is referred to as Class AB operation, although the term "Class B" is frequently used to describe this situation. Despite its complexity, a Class B push-pull amplifier can achieve efficiencies up to approximately 78%, which is more than three times better than can be obtained with a similar Class A amplifier without transformer coupling.

PRELAB ASSINGMENT (TO BE SUBMITTED ONE DAY PRIOR TO CLASS)

Build the circuit in Figure 9-1A in PSpice. Measure the peak-to-peak voltages of both the input and the output waveforms. Does the crossover distortion exist in output waveforms?

REQUIRED PARTS AND EQUIPMENT

- ❖ Resistors
 - 100 Ω
 - Two 10 k Ω
 - Three 1 k Ω
- ❖ Capacitors (25V)
 - Two 2.2 μ F
 - 100 μ F
- ❖ 10 k Ω potentiometer
- ❖ Two 1N914 silicon diodes
- ❖ 2N3904 NPN Silicon Transistor
- ❖ 2N3906 PNP Silicon Transistor
- ❖ DMM
- ❖ Breadboard
- ❖ Analog Discovery 2
- ❖ Jumper Wires
- ❖ DC power supply

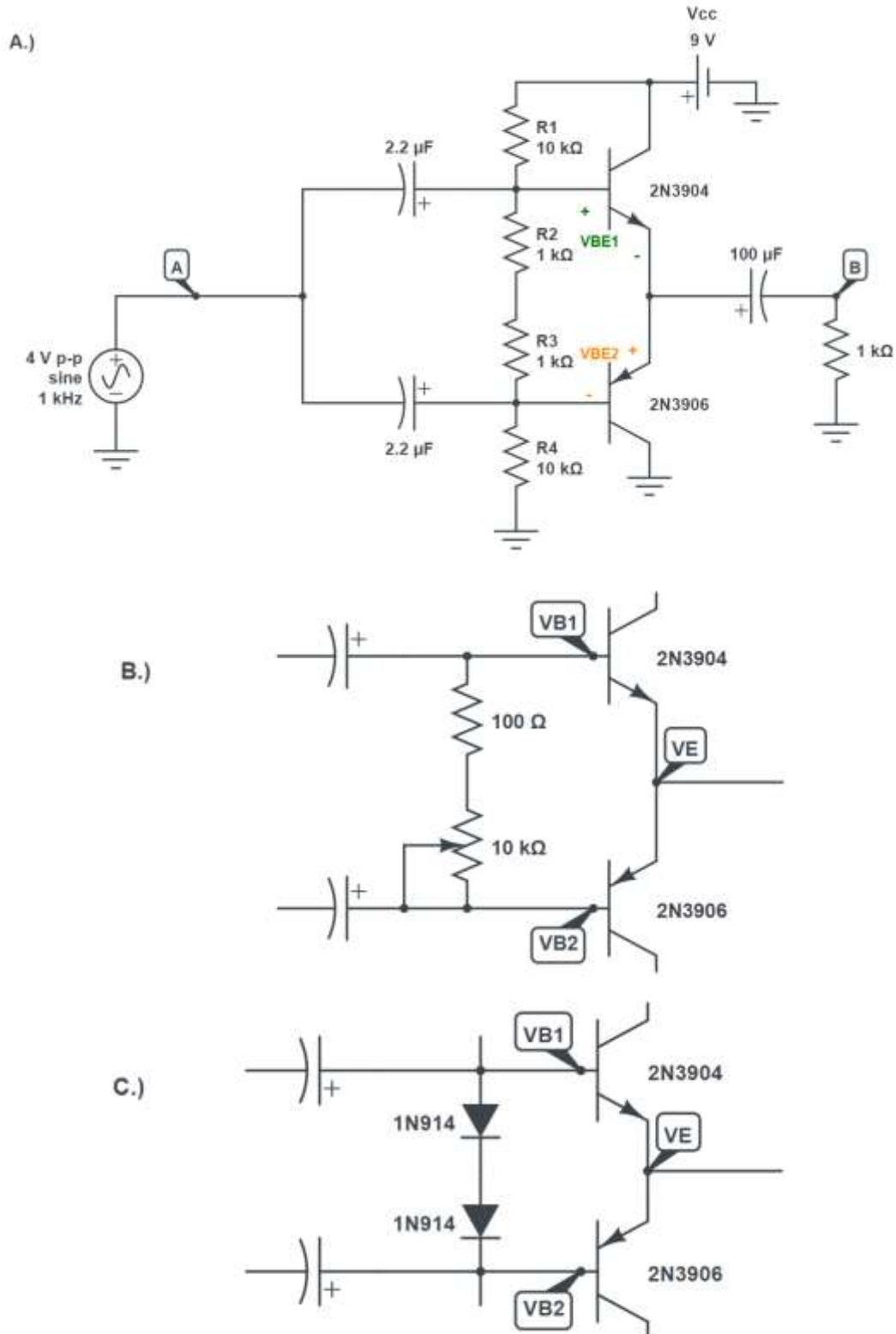


FIGURE 9-1: Schematic Diagram of Circuit
 *For use with AD2 Device, use 5V for V_{cc}

PROCEDURE

1. Wire the circuit shown in Figure 9-1A. Connect Channel 1 probe of oscilloscope at *point A* (v_{in}) and channel 2 to *point B* (v_{out}). Adjust your scope to the following approximate settings:

Channels 1 and 2: 1 V/division

Time base: 200 μ s/division

2. Apply power to the breadboard and adjust the sine wave output level of the waveform generator at 4 V peak-to-peak and a frequency of 1 kHz. You should observe amplifier input and output waveforms like those shown in Figure 9-3. Notice that the output waveform is distorted in the vicinity of zero volts. This condition referred to as *crossover distortion* results when the base-emitter diodes of both transistors are not forward biased until the input signal exceeds approximately 0.7 V in both directions.

- Using Figure 9-4 as a guide, measure the base-to-emitter voltages required for both transistors to become forward biased. Record these values in Table 9-1.

***MEASUREMENT INSTRUCTIONS FOR V_{BE} USING OSCILLOSCOPE:** Signals displayed on an oscilloscope are typically plotted out as voltage over time. The x-axis is time, and the y-axis is voltage. Cursors are used to measure specific points on a waveform for analysis. There will be two sets of cursors, one set (labeled A and B or 1 and 2) for the vertical axis and one set (A and B or 1 and 2) for the horizontal axis. Locate the *Cursors* button on the front panel of the oscilloscope. (Note that different oscilloscopes may have different menus or interfaces, but the principles will remain the same no matter what oscilloscope is being used). Choose *Manual* mode and select the vertical cursors. Move *cursor A* to the point where the crossover distortion just begins on the output waveform. Select *cursor B* and move it to the point where the crossover distortion ends. Now select the horizontal cursors and move *cursors A* and *B* to the points where the input waveform intersects with the vertical cursors have been placed. After placing the horizontal cursors in the correct position, the scope should display the voltages for *cursors A* and *B*, which represent V_{BE1} and V_{BE2} respectively.

****MEASUREMENT INSTRUCTIONS FOR V_{BE} IN WAVEFORMS APPLICATION:** Using Figure 9-4 as a guide, we first need to place Cursors 1 and 2 from Figure 9-4 on the oscilloscope. Open the oscilloscope in the Waveforms application and click on “View > x cursors”. Next, click on the “+ Normal” icon in the X Cursors window. Place two of the normal cursors on the output waveform where the crossover distortion just begins and ends for the output waveform (see Figure 9-4). Now, click on “View > y cursors”. Place two Y Cursors with the “+ Normal” icon, which will represent V_{BE1} and V_{BE2} . Click and drag one of the Y Cursors to the point at which one of the X Cursors that were previously created intersects with the positive cycle of the input waveform. This will be V_{BE1} . Now, click and drag the second Y Cursor to the point at which the previously created X Cursor intersects with the negative cycle of the input waveform. This will be V_{BE2} . See Figure 9-4 for reference.

- Note that the peak-to-peak output voltage is slightly smaller than the input, a difference approximately equal to two base-emitter voltage drops. In addition, since each half of the push-pull circuit is itself an emitter-follower, there is no phase shift between the input and output signals.
3. Disconnect the power and waveform generator leads from the breadboard and replace the series resistance $R_2 + R_3$ with a 10 k Ω potentiometer in series with a 100 Ω resistor as shown in Figure 9-1B. Again, connect the power and waveform generator leads to the breadboard.
4. With the signal generator set at 4 V peak-to-peak at 1 kHz, carefully adjust the potentiometer to the point that the crossover distortion disappears. Notice that the output voltage is very nearly equal to the input voltage. Therefore, the voltage gain is essentially equal to 1.
5. Again, disconnect the power and signal generator leads from the breadboard. Replace the potentiometer and 100 Ω resistor with two IN914 compensating diodes in series between the two transistor base leads, as shown in Figure 9-1C. Again, connect the power and waveform generator to the breadboard.

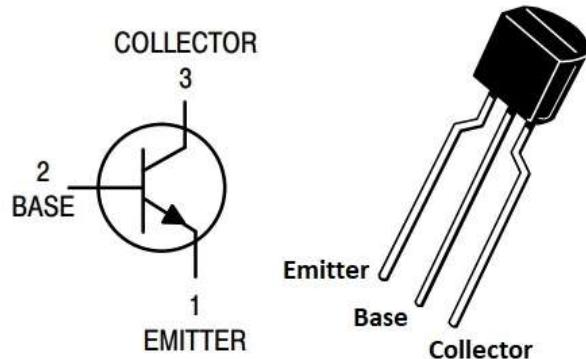


FIGURE 9-2: pinout for 2N3904 and 2N3906 Transistors

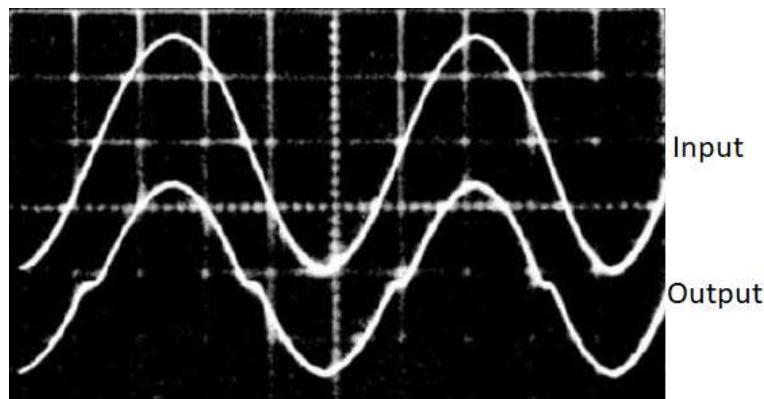


FIGURE 9-3: Input and Output Waveforms

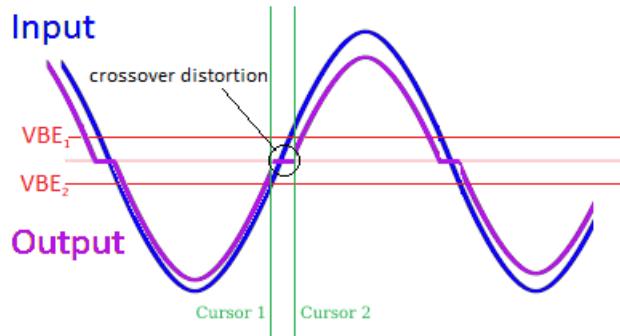


FIGURE 9-4: Crossover Distortion at Output

6. With the signal generator set at 2 V peak-to-peak at 1 kHz, how does the output signal compare with that seen in Step 4, after the potentiometer is adjusted?

You should find that there is virtually no crossover distortion. The voltage required to forward bias both transistor's is now supplied by the voltage drops of the two silicon diodes, which are also forward biased.

7. With a multimeter, individually measure the transistor DC base 1, base 2 and emitter voltages with respect to ground, recording your results in Table 9-2.
8. Now carefully increase the peak-to-peak input signal so that the output peaks just clip off. With your multimeter, measure the rms voltage across the 1 k Ω load resistor $|V_o(rms)|$, and compute the rms output power of the amplifier (Equation 2). Record these results in table 9-3.
9. To measure the DC power supplied to the amplifier while amplifying an input signal, use your multimeter to measure the DC collector current I_{CC} of either transistor. Compute the DC power supplied (Equation 3), recording your results in Table 9-3.
10. Finally, compute the percent efficiency of your amplifier and compare it with the theoretical maximum of 78.5% of Class B amplifiers. Record your results in Table 9-3.

WHAT YOU HAVE DONE

This experiment demonstrated the design and operation of a Class B push-pull emitter-follower power amplifier and how it compared with a Class A amplifier circuit. The circuit required a complementary pair of transistors (one NPN and PNP) that have almost identical characteristics. The cause of crossover distortion was demonstrated, and possible methods to eliminate it were investigated. The most effective of these methods was a current mirror biasing, using a pair of diodes. In addition, the efficiency of the amplifier was determined and compared with that of a Class A amplifier.

DATA FOR LAB 9: The Class B Push-Pull Emitter-Follower Power Amplifier

Parameter	Measured Value
V_{BE1}	
V_{BE2}	
V_E	

TABLE 9-1: Voltage-Divider Bias with No Crossover Distortion

*Use Oscilloscope Cursors to Complete Table 9-1

Parameter	Measured Value
V_{B1}	
V_{B2}	
V_E	

TABLE 9-2: Diode (Current Mirror) Bias with No Crossover Distortion

*Use Multimeter to Complete Table 9-2

Parameter	Measured Value
V_o (rms)	
I_{cc}	

Parameter	Calculated Value
P_o (rms)	
P_{DC}	
% η	

TABLE 9-3: Class B Amplifier Efficiency

USEFUL FORMULAS

Quiescent dc collector current (diode bias)

$$(1) I_{CQ} = \frac{V_{CC} - V_{BE}}{R_1 + R_4} \quad (if V_{BE1} = V_{BE2})$$

RMS output power

$$(2) P_o(rms) = \frac{v_o(rms)^2}{R_L}$$

DC supply power supplied to amplifier

$$(3) P_{DC} = V_{CC} \cdot I_{CC}$$

Amplifier percent efficiency

$$(4) \% \square = \left(\frac{P_o(rms)}{P_{DC}} \right) \cdot 100\%$$

Lab 10

MOSFETs and CMOS Inverter

LAB 10: MOSFETs and CMOS Inverter

BACKGROUND

The MOSFET is by far the most common transistor, and the basic building block of most modern electronics. Varying voltage applied to a conducting Metal electrode deposited on top of the oxide creates an electric field-effect that controls current flow through the substrate. This field-effect transistor (FET) element can perform as an amplifier, a switch, and other useful electronic functions while combining small size, low cost, and minimal energy consumption. The MOSFET was the first truly compact transistor that could be miniaturized and mass-produced for a wide range of uses. The MOSFET accounts for 99.9% of all transistors in the world.¹

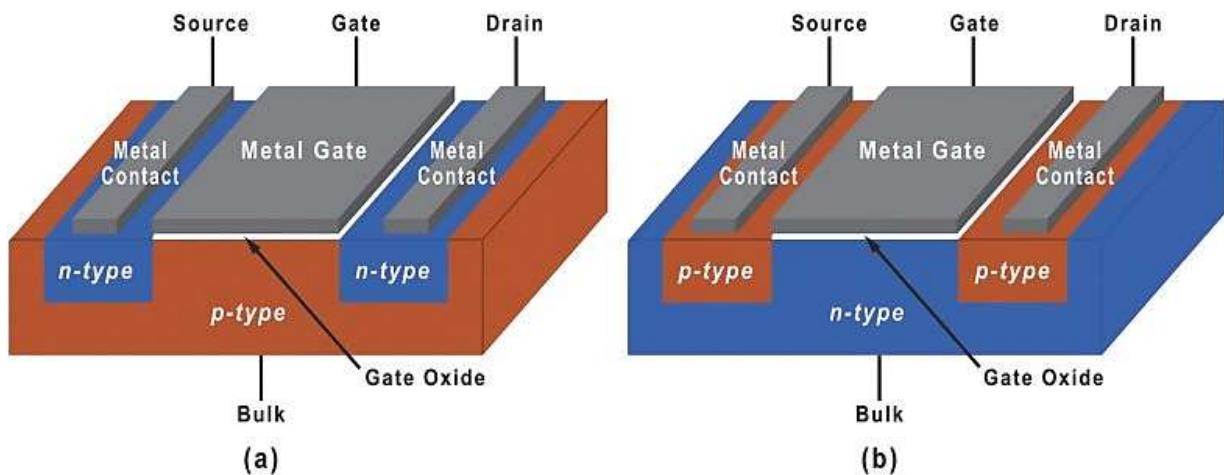


Figure 10-1: (a) n-type MOSFET; (b) p-type MOSFET

1. Introduction

MOSFET represents metal–oxide–semiconductor field-effect transistor which is also known as the metal–oxide–silicon transistor (MOS transistor, or MOS). The physical configuration of n-type and p-type MOSFET is shown in Fig. 10-1, where both types have gate, drain, and source terminals and both are controlled by a gate-to-source voltage. A key advantage of a MOSFET is that it requires almost no input current to control the load current, when compared with bipolar junction transistors (BJTs). Instead, MOSFET is voltage controlled. The principal feature that distinguishes a MOSFET from a junction FET (JFET) is the fact that the gate terminal in a MOSFET is insulated by a thin silicon oxide layer from its channel region. Because of the oxide, there is no current flowing into the gate electrode, only a field. Thus, the gate of a MOSFET can be considered as a capacitance.

There are depletion-mode and enhancement-mode MOSFETs. Enhancement-mode MOSFETs are the common switching elements in most integrated circuits. These devices are off at zero gate–source voltage. NMOS can be turned on by pulling the gate voltage higher than the source voltage, PMOS can be turned on by pulling the gate voltage lower than the source voltage. In a depletion-mode MOSFET,

¹ <https://en.wikipedia.org/wiki/Transistor>

the device is normally ON at zero gate–source voltage. In this lab, we will focus on N-type enhancement-mode MOSFET.

2. MOSFET circuit as a switch

A MOSFET circuit diagram is shown in Fig. 10-2, where V_{in} is the input gate voltage, V_{DD} is supply voltage, and V_{out} is output drain voltage. In this lab, we will look at using the enhancement-mode MOSFET as a switch as these transistors require a positive gate voltage to turn “ON” and a zero voltage to turn “OFF” making them easily understood as switches and easy to interface with logic gates.

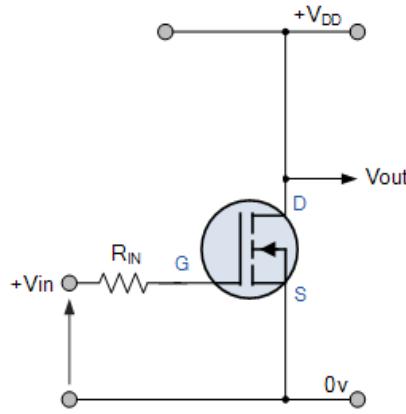


Figure 10-2: MOSFET circuit diagram

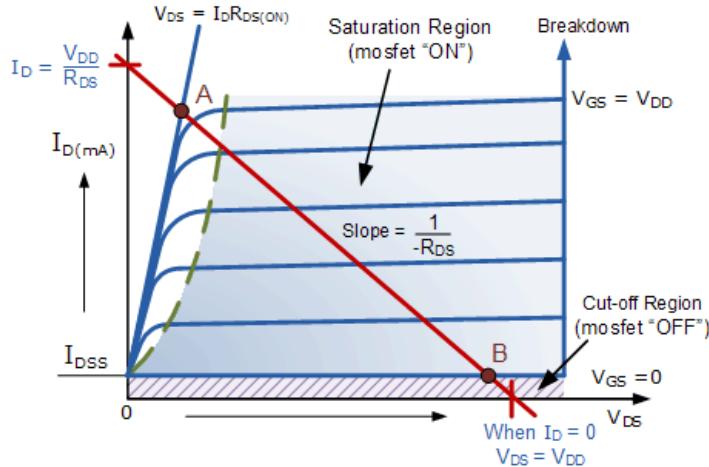


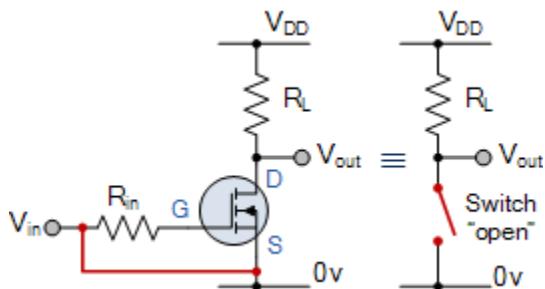
Figure 10-3: MOSFET characteristic curve

The operation of the enhancement-mode MOSFET, or e-MOSFET, can best be described using its I-V characteristics curves shown in Fig. 10-3. When V_{in} is HIGH or equal to V_{DD} , the MOSFET Q-point moves to point A along the load line. The drain current I_D increases to its maximum value due to a reduction in the channel resistance. I_D becomes a constant value independent of V_{DD} and is dependent only on V_{GS} . Therefore, the transistor behaves like a closed switch but the channel ON-resistance does not reduce fully to zero due to its $R_{DS(on)}$ value, but gets very small.

Likewise, when V_{in} is LOW or reduced to zero, the MOSFET Q-point moves from point A to point B along the load line. The channel resistance is very high, so the transistor acts like an open circuit and no current flows through the channel. Thus, if the gate voltage of the MOSFET toggles between two values, HIGH and LOW, the MOSFET will behave as a “single-pole single-throw” (SPST) solid state switch.

The “switching action” of MOSFET circuit is summarized as follows.

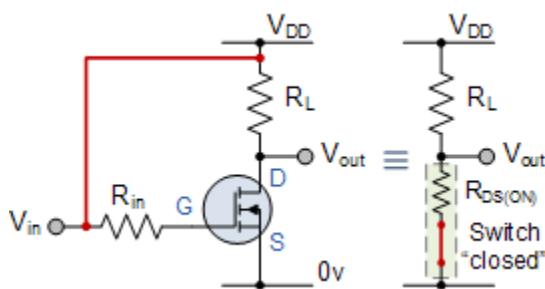
- Cut-off Characteristics



- The input and Gate are grounded (0V)
- Gate-source voltage less than threshold voltage $V_{GS} < V_{TH}$
- MOSFET is “OFF” (Cut-off region)
- No Drain current flows ($I_D = 0$ Amps)
- $V_{OUT} = V_{DS} = V_{DD} = "1"$
- MOSFET operates as an “open switch”

Then we can define the cut-off region or “OFF mode” when using an e-MOSFET as a switch as being, gate voltage, $V_{GS} < V_{TH}$ thus $I_D = 0$.

- Saturation Characteristics



- The input and Gate are connected to V_{DD}
- Gate-source voltage is much greater than threshold voltage $V_{GS} > V_{TH}$
- MOSFET is “ON” (saturation region)
- Max Drain current flows ($I_D = V_{DD} / R_L$)
- $V_{DS} = 0V$ (ideal saturation)
- Min channel resistance $R_{DS(on)} < 0.1\Omega$
- $V_{OUT} = V_{DS} \cong 0.2V$ due to $R_{DS(on)}$
- MOSFET operates as a low resistance “closed switch”

3. CMOS Inverter

Complementary metal–oxide–semiconductor (CMOS) is a type of MOSFET fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions. As of 2011, 99% of IC chips, including most digital, analog, and mixed-signal ICs, are fabricated using CMOS technology. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the MOSFET pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, like NMOS logic or transistor–transistor logic (TTL), which normally have some standing current even when not changing state².

² <https://en.wikipedia.org/wiki/CMOS>

Figure 10-4 shows how a pair of p-type and n-type MOSFETs is used to implement an inverter. In Figure 10-4(b), when A is low, the NMOS transistor (bottom) is in a high resistance state, disconnecting V_{ss} from Q. The PMOS transistor (top) is in a low resistance state, connecting V_{dd} to Q. Therefore Q is high. It is the opposite when A is low. Thus, it is an inverter.

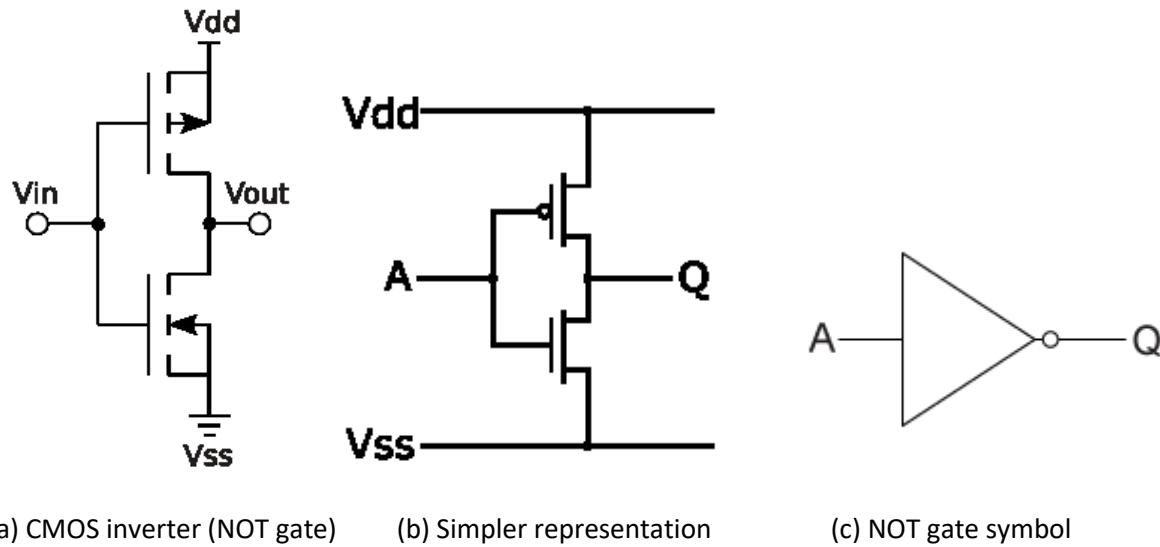


Figure 10-4. CMOS Inverter

PURPOSE

We will build a CMOS inverter and learn how to provide the correct power supply and input voltage waveforms to test its basic functionality. For a given supply V_{DD} , your voltage low should be zero, and voltage high should be V_{DD} .

By default, the function generator gives an output that varies from $\frac{-V_{pp}}{2}$ to $\frac{+V_{pp}}{2}$. For a square wave, the voltage low is $\frac{-V_{pp}}{2}$, voltage high is $\frac{+V_{pp}}{2}$. Set the DC offset to $\frac{V_{pp}}{2}$ to make voltage low 0.

REQUIRED COMPONENTS

- ❖ Resistors:
 - 150 Ω
 - 4.7 kΩ
- ❖ 0-15 V DC Power Supply
- ❖ 4558 Op-Amp
- ❖ ALD1105PBL
- ❖ 1 μF Capacitor
- ❖ Waveform Function Generator
- ❖ Dual Trace Oscilloscope
- ❖ Breadboard

PRELAB ASSIGNMENT

Download the data sheet for the ALD1105.

- Determine the threshold values of voltage range, maximum current I_D , maximum drain-source voltage, and the maximum allowed power dissipation, P_{total} .
- In which region should the MOSFET be operating when it is a closed switch? Why? In which region should it be operating when it is an open switch? Why?
- Draw a pin-level wiring diagram of a CMOS inverter. Use the pair of NMOS and PMOS gates on the right side of the ALD1105 IC.
- For a V_{DD} of 3V, 5V, 7V, sketch the input waveforms required to test the functionality of the CMOS inverter. Set the function generator to a square wave and determine the voltage peak-to-peak and the DC offset setting required.

**Note that it is important that the DC offset should always be $\frac{1}{2}$ the peak-to-peak voltage. This is because CMOS logic requires a voltage input of 0 Vdd and the function generator always provides a waveform with a DC component of 0 Volts. That is, “positive” peak is at $V_{pp}/2$, and the “negative” peak voltage is at $-V_{pp}/2$. Therefore, it is necessary to provide an offset equal to $\frac{1}{2} V_{pp}$ to move the “negative peak”, or voltage low to 0 Volts.*

PIN CONFIGURATION

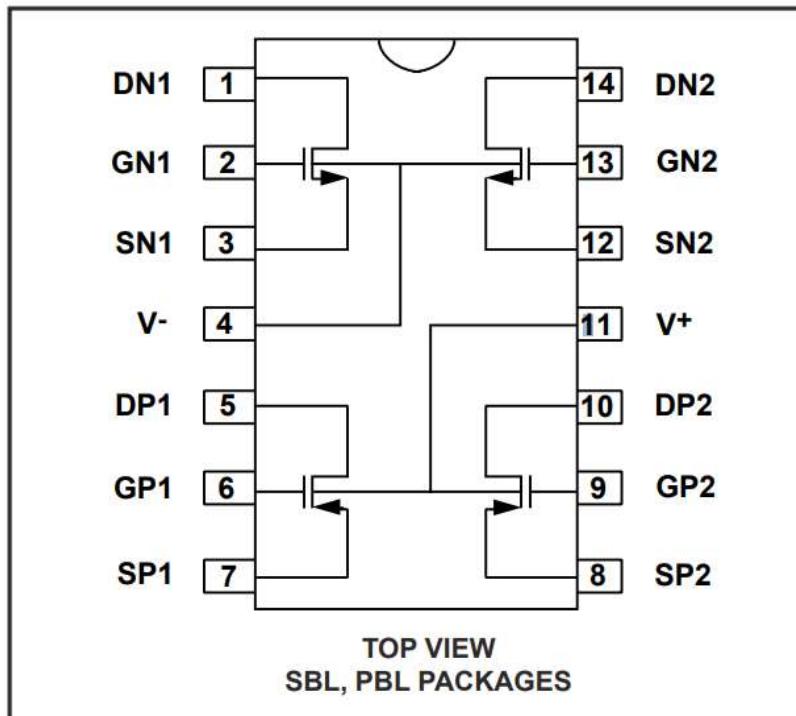


FIGURE 10-5: ALD1105 PBL Pinout

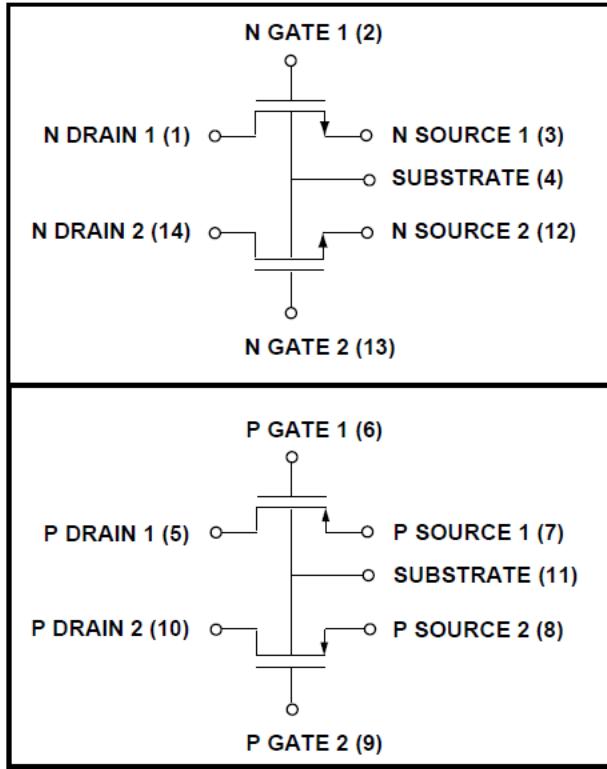


FIGURE 10-6: Circuit Symbol and Pin Numbers for the Pairs of N-channel and P-channel MOSFETs

PROCEDURE

1. Construct the circuit as shown in Figure 10-7, using the pin level diagram from the ALD1105 data sheet, or refer to Figure 10-5.
2. Set the waveform function generator to a square wave at 5 Hz, 5 volts peak-to-peak, and set the DC offset to +2.5 volts. The peak-to-peak voltage and DC offset combination gives a voltage low of 0 volts and voltage high of 5 volts. Also, set the DC power supply voltage to +5 volts.
3. Adjust the frequency until you can see a clear rise and fall of the output signal. Try increasing the frequency to see at what frequency the inverter has trouble completing the high to low and low to high transitions. Take oscilloscope screenshots of the output waveforms for frequencies that are too high such that transitions between 0 and V_{dd} are not complete.

*Note that the waveform function generator amplitude and DC offset should be the same voltage as the DC power supply.

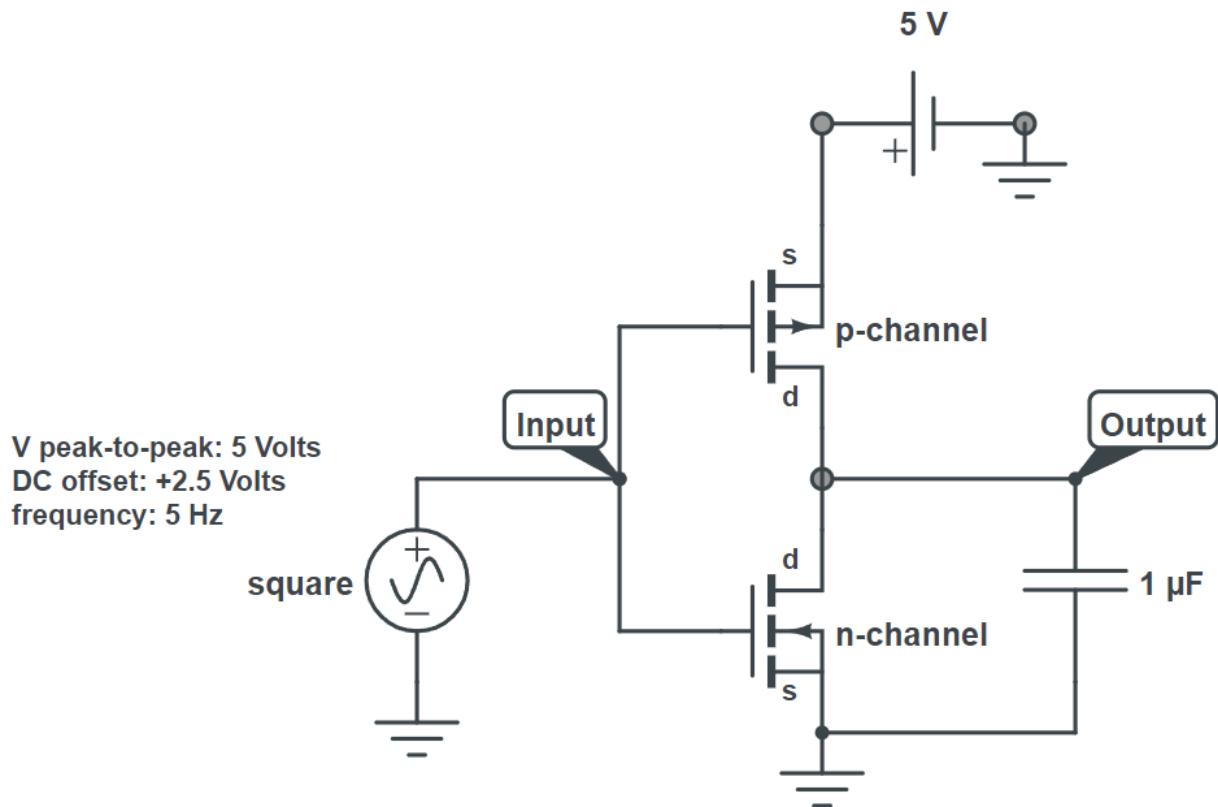


FIGURE 10-7: CMOS Inverter Schematic for Voltage Transfer Measurement

4. Now, the voltage transfer curve of the inverter will be measured.
5. Remove the capacitor from the circuit in Figure 10-7.
6. Set the DC voltage to +5 volts so that the CMOS inverter sees a V_{dd} of 5 volts.
7. Disconnect the function generator, instead connect another DC supply to the node labeled “Input” in Figure 10-7.
8. Increase the input DC voltage from 0V to 5V in small increments according to the values given in Table 10-1.
9. At each input voltage measure the DC output voltage at the node labeled as “Output”. Record these values in Table 10-1.
10. Plot the voltage transfer curve with V_{in} on x-axis and V_{out} on the y-axis.

FOR FURTHER INVESTIGATION

Try different V_{dd} values. You will see how the voltage transfer curve changes with V_{dd} .

ADDITIONAL READING

MOSFETs are a building block to implement a NAND logic gate as shown in Figure 10-8(a), which is in turn a building block to implement all other logic gates as in Figure 10-8(b).

Here is how it implements a NAND gate (output is 1 when both A and B are 0; otherwise, the output is 0). In Figure 10-7(a), when either A or B is low, one of the two NMOS transistors (bottom) is in a high resistance state, disconnecting V_{ss} from Q. One of the two PMOS transistors (top) is in a low resistance state, connecting V_{dd} to Q. Therefore Q is high. When both A and B are high, the two NMOS transistors (bottom) are in a low resistance state, connecting V_{ss} to Q. Both PMOS transistors (top) are in a high resistance state, disconnecting V_{dd} to Q. Therefore Q is low.

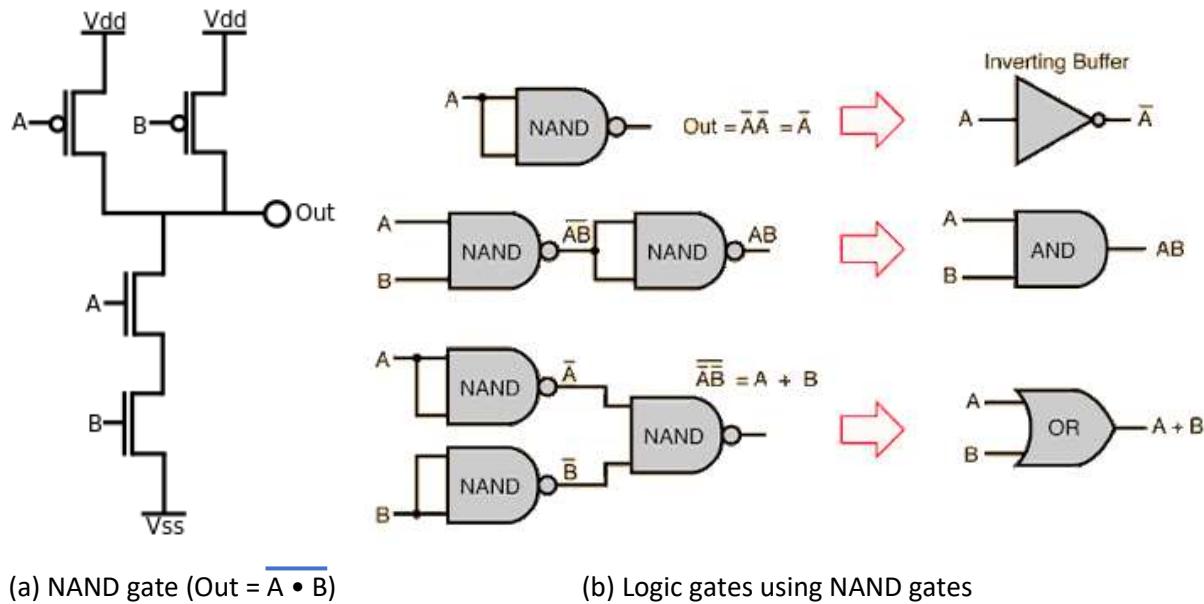


Figure 10-7. MOSFETs to implement a NAND gate and all other logic gates.

And, a pair of CMOS inverters is used to implement a memory cell. Figure 10-8(a) shows a SRAM (static random access memory) cell. SRAM is a type of digital memory consisting of cells each capable of storing one binary digit. An SRAM cell is constructed as two cross-coupled inverters, hence leading to two stable states.

Here is how it works. In Figure 10-8(a), when A is low, the NMOS transistor (T2) is in a high resistance state, disconnecting V_{ss} from Q. The PMOS transistor (T1) is in a low resistance state, connecting V_{dd} to Q. Therefore Q is high. When Q is high, the NMOS transistor (T4) are in a low resistance state, connecting V_{ss} to Q'. The PMOS transistor (T3) are in a high resistance state, disconnecting V_{dd} to Q'. Therefore Q' is low. Now, since Q' (low) connects to A, it itself is in a stable condition without any outside input. This constitutes a RAM cell.

Figure 10-8(c) shows the logical description of a SRAM cell (consisting of 6 MOSFET transistors, hence called 6T SRAM cell) that allows read and write operations. Two additional transistors are known as the pass transistors. The wordline (WL), bitline (BL), and its complement (BL') are used to access the cell.

- Hold
 - $WL = 0$, both pass transistors are OFF
 - Data is held in the two cross-coupled inverters
- Write
 - $WL = 1$, both pass transistors are ON
 - New data (voltage) applied to BL and BL'
 - Data held in the two cross-coupled inverters overwritten with new value
- Read
 - $WL = 1$, both pass transistors are ON
 - BL and BL' read by a sense amplifier

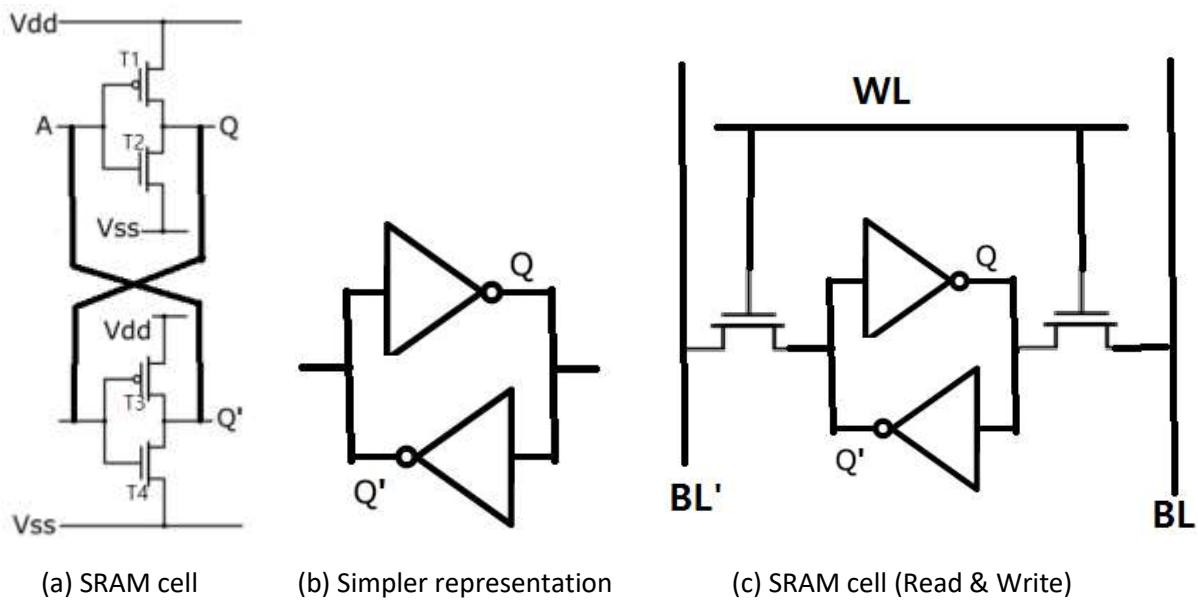


Figure 10-8. MOSFETs to implement a memory cell.

One recent development with SRAM cells is to use it as an intrinsic security primitive. While the two inverters in a SRAM cell are designed in a well-balanced, symmetrical way, the small and random submicron process variations in the manufacturing process cause different physical properties of the transistors. In other words, it is not clear from Figure 10-8 at what state it will be right after power-up of the memory, i.e. what happens when the supply voltage comes up? In fact, the random physical mismatch in the cell, caused by manufacturing variability, determines the power-up behavior.

SRAM-based PUF (Physical Unclonable Function) exploits this randomness to generate a unique digital value that can be used as a secret key. Secret keys are essential for digital security. PUF is based on the idea that two devices that are identical by design will have different electrical characteristics. Though silicon production processes are precise, this technology exploits the fact that there are still tiny variations in each circuit produced. The PUF uses these tiny differences to generate a unique digital value that can be used as a secret key. There is a broad taxonomy of PUFs today, such as delay-based arbiter PUFs and ring oscillator PUFs, memory-based SRAM PUFs, and butterfly PUFs. It is particularly

important for Internet of Thing (IoT) devices because the challenge is how to secure IoT devices without adding silicon real estate or cost, given the resource constraints in terms of maintaining minimum power consumption and optimizing the processing resources on the IoT devices.

WHAT YOU HAVE DONE

This experiment demonstrates the design and operation of a MOSFET and COMS inverter circuit. It uses a dual N-channel and dual P-channel complementary matched transistor pair intended for a broad range of analog applications. Here, the input signal is applied to both the gate terminals, while the output signal is taken from the either of the drain terminals. The experiment also showed the voltage transfer curve of the inverter.

DATA FOR LAB 10: MOSFETs and CMOS Inverter

V_{in}	V_{out}
0V	
0.2V	
0.4V	
0.6V	
0.8V	
1V	
1.2V	
1.4V	
1.6V	
1.8V	
2V	
2.2V	
2.4V	
2.6V	
2.8V	
3V	
3.2V	
3.4V	
3.6V	
3.8V	
4V	
4.2V	

4.4V	
4.6V	
4.8V	
5V	

TABLE 10-1: Voltage transfer curve

POSTLAB ASSIGNMENT (TO BE SUBMITTED WITH LAB REPORT)

Design a CMOS inverter circuit like the figure 10-7 with $V_{dd} = 3V$ and set the function generator to the according to the requirements of the circuit, so that your output will switch between 0V and 3V. Include your circuit diagram, function generator settings, input-output waveforms using AD2.



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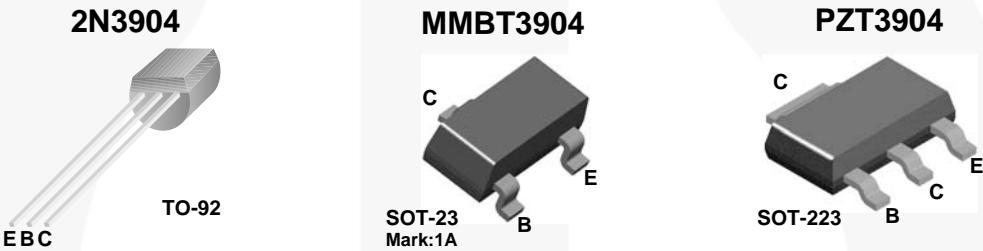


October 2014

2N3904 / MMBT3904 / PZT3904 NPN General-Purpose Amplifier

Description

This device is designed as a general-purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier.



Ordering Information

Part Number	Marking	Package	Packing Method	Pack Quantity
2N3904BU	2N3904	TO-92 3L	Bulk	10000
2N3904TA	2N3904	TO-92 3L	Ammo	2000
2N3904TAR	2N3904	TO-92 3L	Ammo	2000
2N3904TF	2N3904	TO-92 3L	Tape and Reel	2000
2N3904TFR	2N3904	TO-92 3L	Tape and Reel	2000
MMBT3904	1A	SOT-23 3L	Tape and Reel	3000
PZT3904	3904	SOT-223 4L	Tape and Reel	2500

Absolute Maximum Ratings^{(1), (2)}

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Notes:

1. These ratings are based on a maximum junction temperature of 150°C .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty cycle operations.

Thermal Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Maximum			Unit
		2N3904	MMBT3904 ⁽³⁾	PZT3904 ⁽⁴⁾	
P_D	Total Device Dissipation	625	350	1,000	mW
	Derate Above 25°C	5.0	2.8	8.0	$\text{mW}/^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	$^\circ\text{C}/\text{W}$

Notes:

3. Device is mounted on FR-4 PCB 1.6 inch X 1.6 inch X 0.06 inch.
4. Device is mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm, mounting pad for the collector lead minimum 6 cm^2 .

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
OFF CHARACTERISTICS					
$V_{(\text{BR})\text{CEO}}$	Collector-Emitter Breakdown Voltage	$I_C = 1.0 \text{ mA}, I_B = 0$	40		V
$V_{(\text{BR})\text{CBO}}$	Collector-Base Breakdown Voltage	$I_C = 10 \mu\text{A}, I_E = 0$	60		V
$V_{(\text{BR})\text{EBO}}$	Emitter-Base Breakdown Voltage	$I_E = 10 \mu\text{A}, I_C = 0$	6.0		V
I_{BL}	Base Cut-Off Current	$V_{CE} = 30 \text{ V}, V_{EB} = 3 \text{ V}$		50	nA
I_{CEX}	Collector Cut-Off Current	$V_{CE} = 30 \text{ V}, V_{EB} = 3 \text{ V}$		50	nA
ON CHARACTERISTICS⁽⁵⁾					
h_{FE}	DC Current Gain	$I_C = 0.1 \text{ mA}, V_{CE} = 1.0 \text{ V}$	40		
		$I_C = 1.0 \text{ mA}, V_{CE} = 1.0 \text{ V}$	70		
		$I_C = 10 \text{ mA}, V_{CE} = 1.0 \text{ V}$	100	300	
		$I_C = 50 \text{ mA}, V_{CE} = 1.0 \text{ V}$	60		
		$I_C = 100 \text{ mA}, V_{CE} = 1.0 \text{ V}$	30		
$V_{CE(\text{sat})}$	Collector-Emitter Saturation Voltage	$I_C = 10 \text{ mA}, I_B = 1.0 \text{ mA}$		0.2	V
		$I_C = 50 \text{ mA}, I_B = 5.0 \text{ mA}$		0.3	
$V_{BE(\text{sat})}$	Base-Emitter Saturation Voltage	$I_C = 10 \text{ mA}, I_B = 1.0 \text{ mA}$	0.65	0.85	V
		$I_C = 50 \text{ mA}, I_B = 5.0 \text{ mA}$		0.95	
SMALL SIGNAL CHARACTERISTICS					
f_T	Current Gain - Bandwidth Product	$I_C = 10 \text{ mA}, V_{CE} = 20 \text{ V}, f = 100 \text{ MHz}$	300		MHz
C_{obo}	Output Capacitance	$V_{CB} = 5.0 \text{ V}, I_E = 0, f = 100 \text{ kHz}$		4.0	pF
C_{ibo}	Input Capacitance	$V_{EB} = 0.5 \text{ V}, I_C = 0, f = 100 \text{ kHz}$		8.0	pF
NF	Noise Figure	$I_C = 100 \mu\text{A}, V_{CE} = 5.0 \text{ V}, R_S = 1.0 \text{ k}\Omega, f = 10 \text{ Hz to } 15.7 \text{ kHz}$		5.0	dB
SWITCHING CHARACTERISTICS					
t_d	Delay Time	$V_{CC} = 3.0 \text{ V}, V_{BE} = 0.5 \text{ V}$		35	ns
t_r	Rise Time	$I_C = 10 \text{ mA}, I_{B1} = 1.0 \text{ mA}$		35	ns
t_s	Storage Time	$V_{CC} = 3.0 \text{ V}, I_C = 10 \text{ mA}, I_{B1} = I_{B2} = 1.0 \text{ mA}$		200	ns
t_f	Fall Time			50	ns

Note:

5. Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2.0\%$.

Typical Performance Characteristics

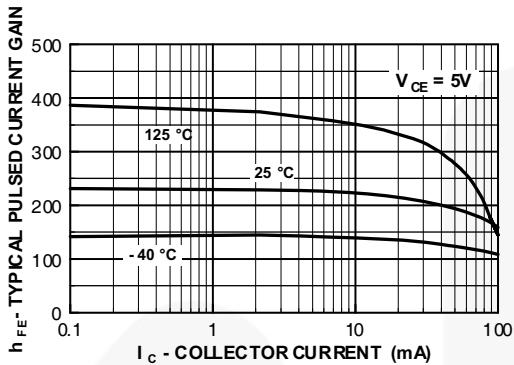


Figure 1. Typical Pulsed Current Gain vs. Collector Current

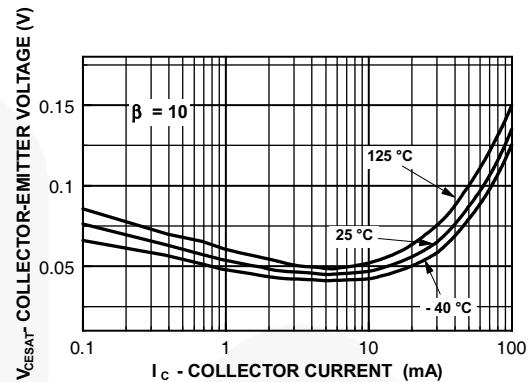


Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current

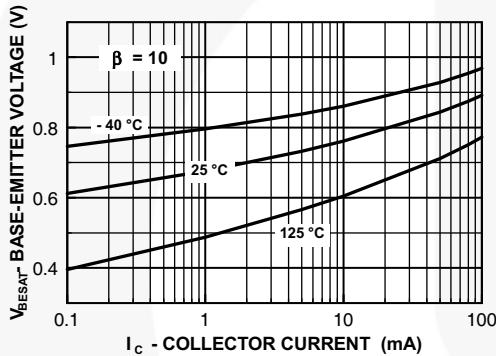


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

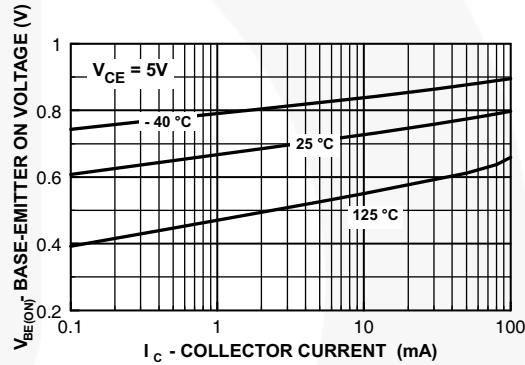


Figure 4. Base-Emitter On Voltage vs. Collector Current

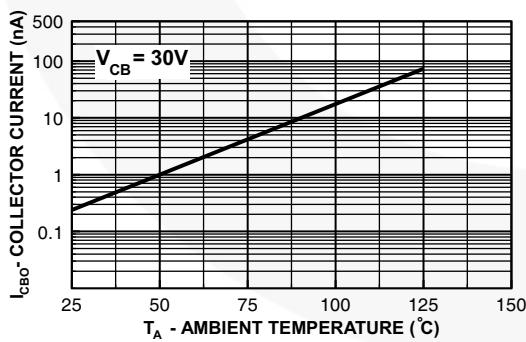


Figure 5. Collector Cut-Off Current vs. Ambient Temperature

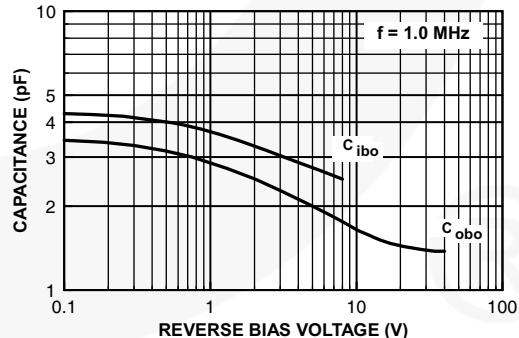


Figure 6. Capacitance vs. Reverse Bias Voltage

Typical Performance Characteristics (Continued)

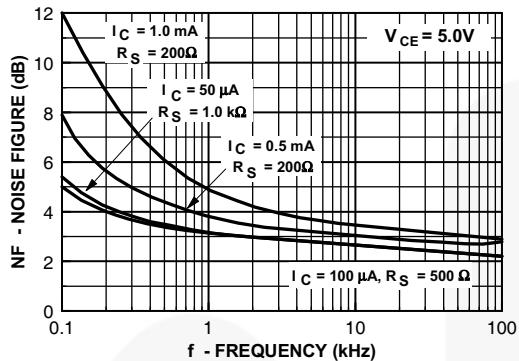


Figure 7. Noise Figure vs. Frequency

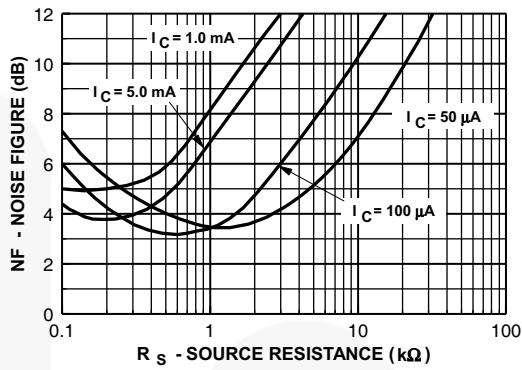


Figure 8. Noise Figure vs. Source Resistance

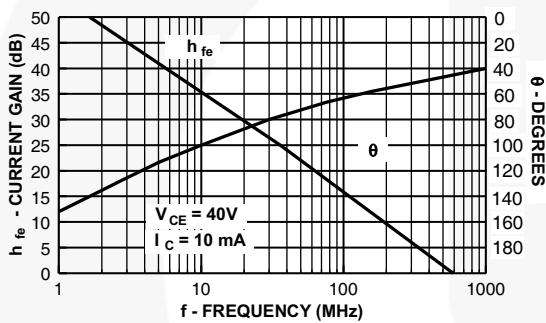


Figure 9. Current Gain and Phase Angle vs. Frequency

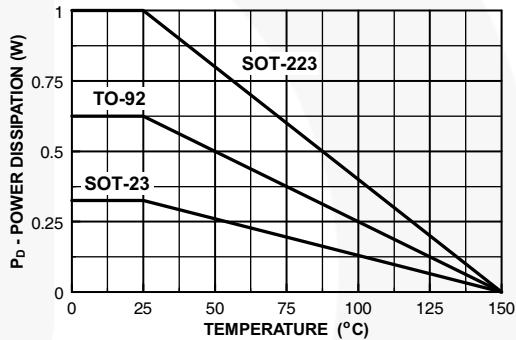


Figure 10. Power Dissipation vs. Ambient Temperature

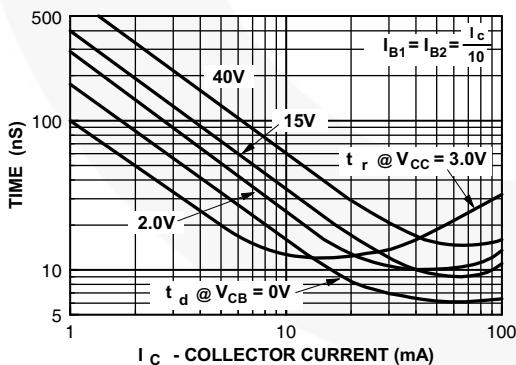


Figure 11. Turn-On Time vs. Collector Current

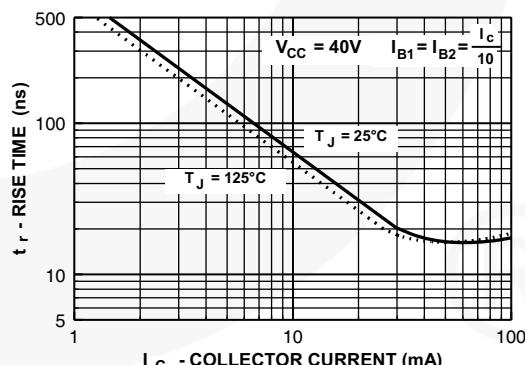


Figure 12. Rise Time vs. Collector Current

Typical Performance Characteristics (Continued)

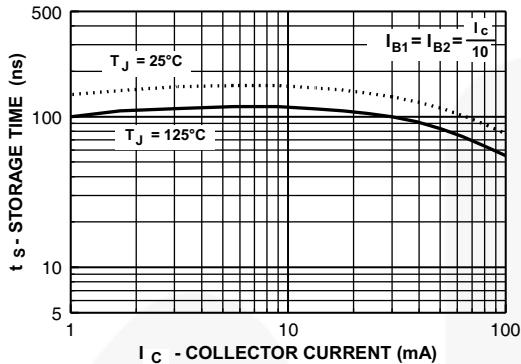


Figure 13. Storage Time vs. Collector Current

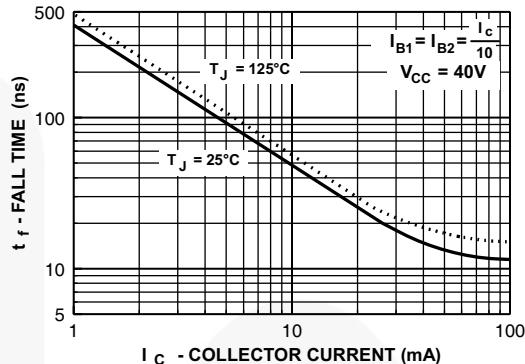


Figure 14. Fall Time vs. Collector Current

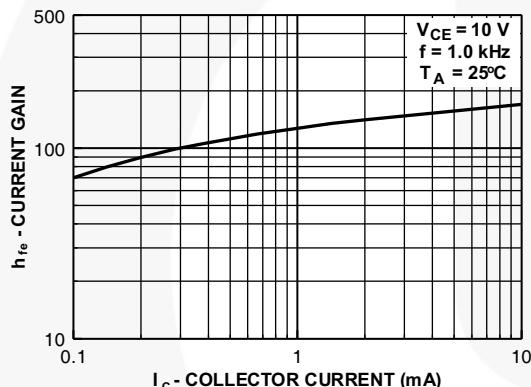


Figure 15. Current Gain

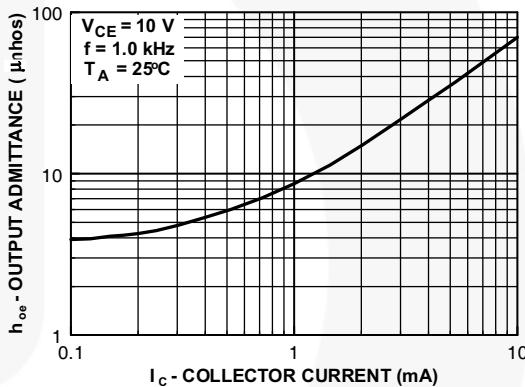


Figure 16. Output Admittance

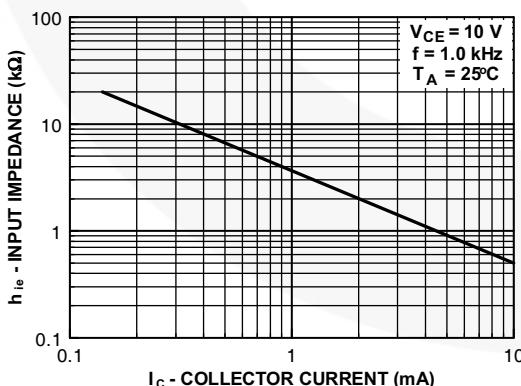


Figure 17. Input Impedance

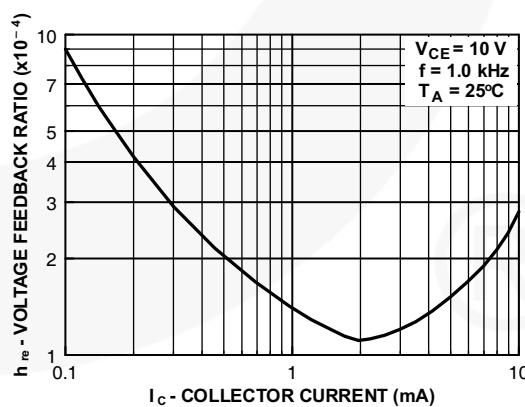


Figure 18. Voltage Feedback Ratio

Test Circuits

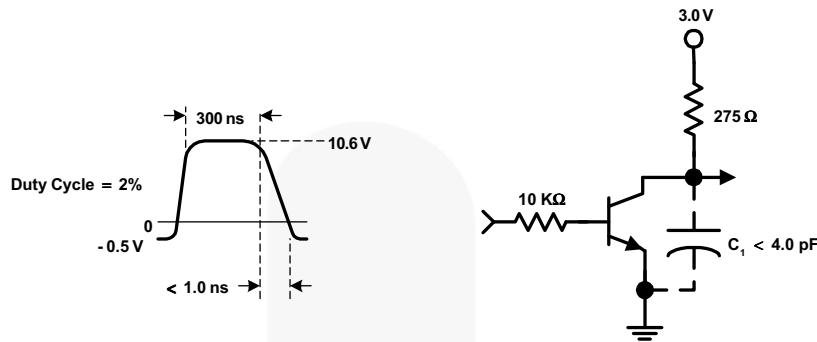


Figure 19. Delay and Rise Time Equivalent Test Circuit

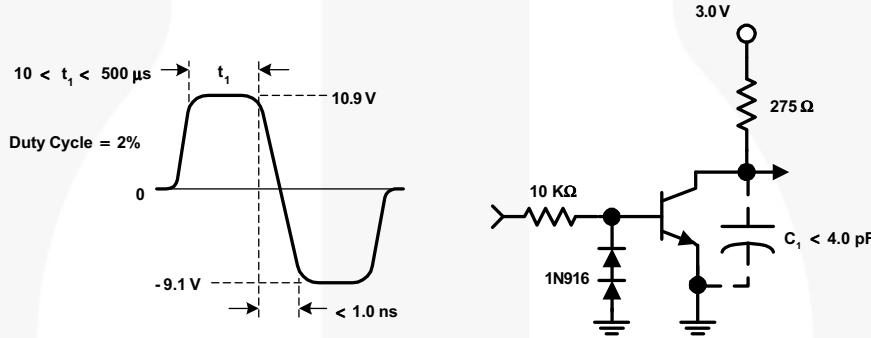
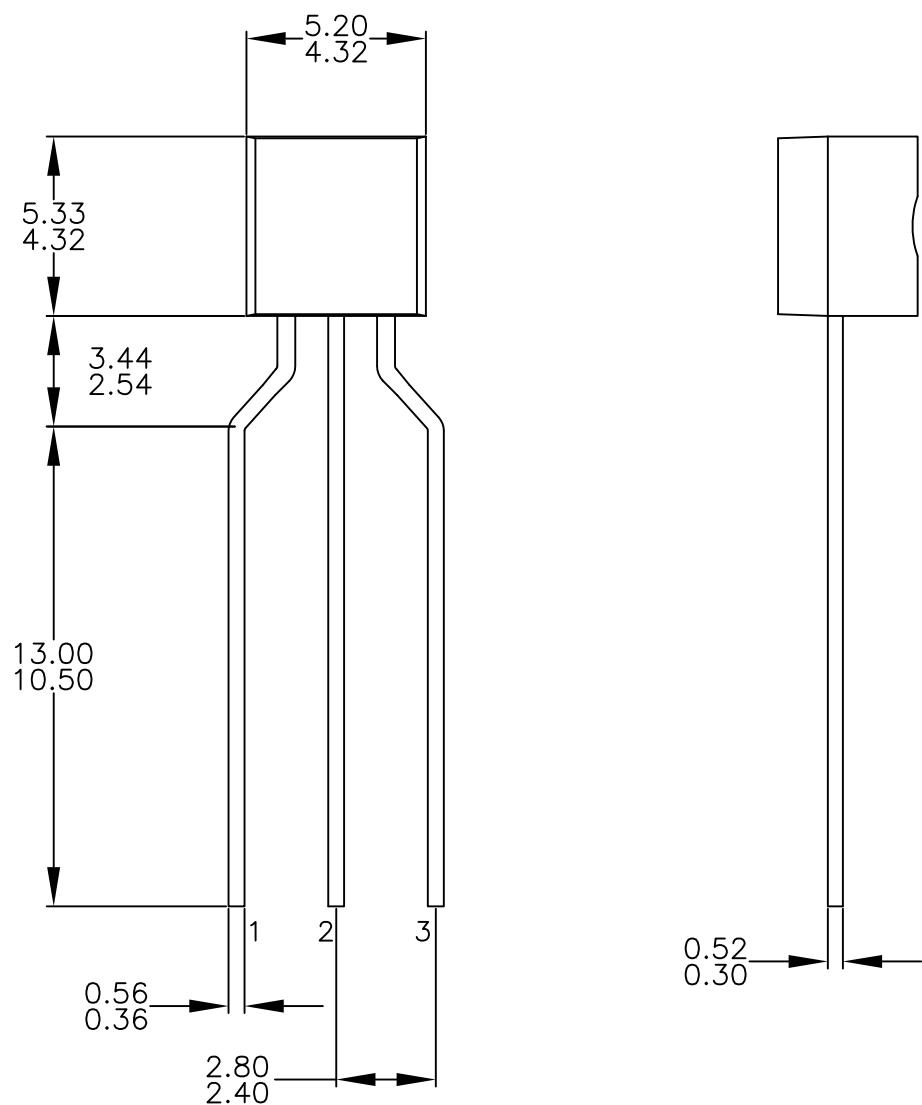
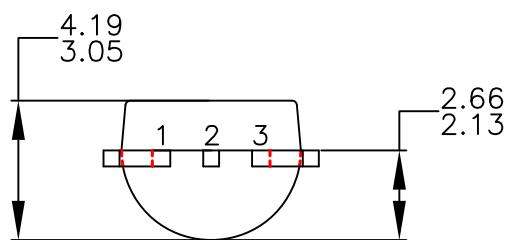


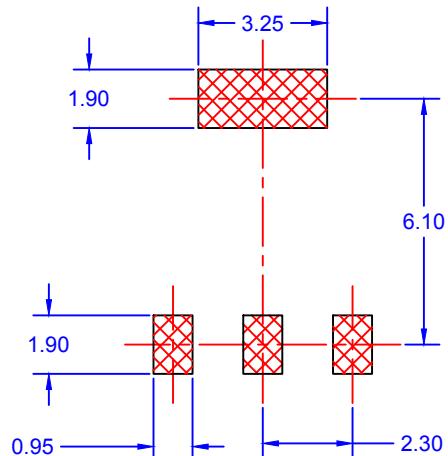
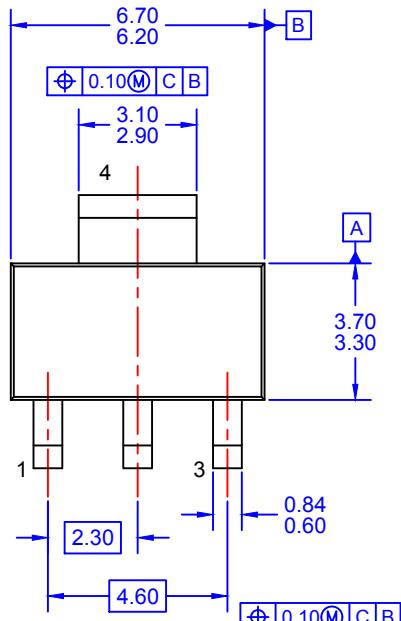
Figure 20. Storage and Fall Time Equivalent Test Circuit



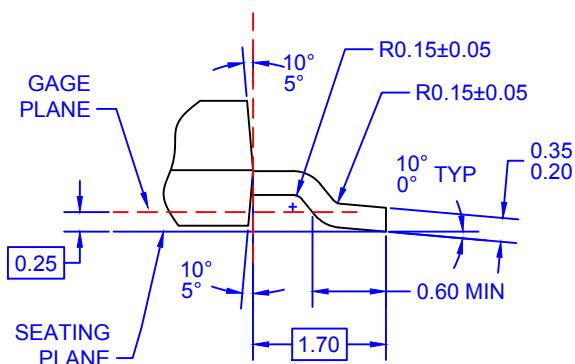
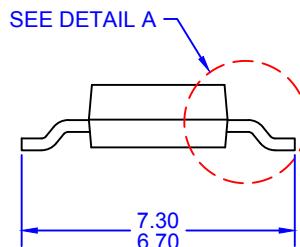
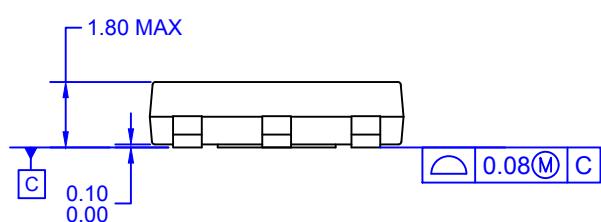
NOTES: UNLESS OTHERWISE SPECIFIED

- A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREV3.
- E. FAIRCHILD SEMICONDUCTOR.





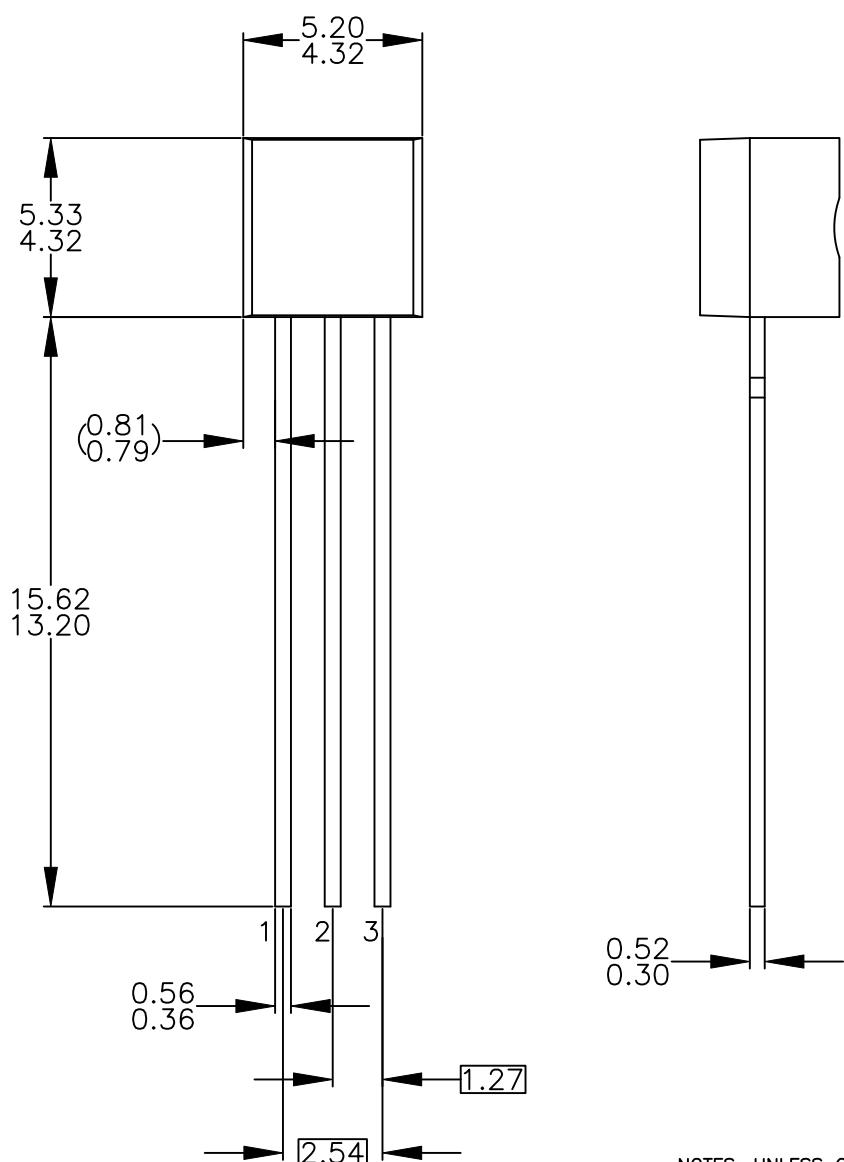
LAND PATTERN RECOMMENDATION



DETAIL A
SCALE: 2:1

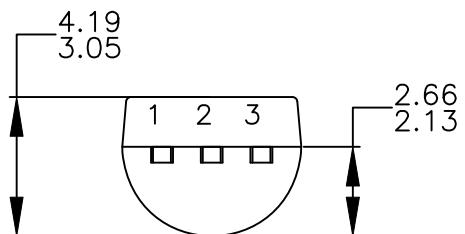
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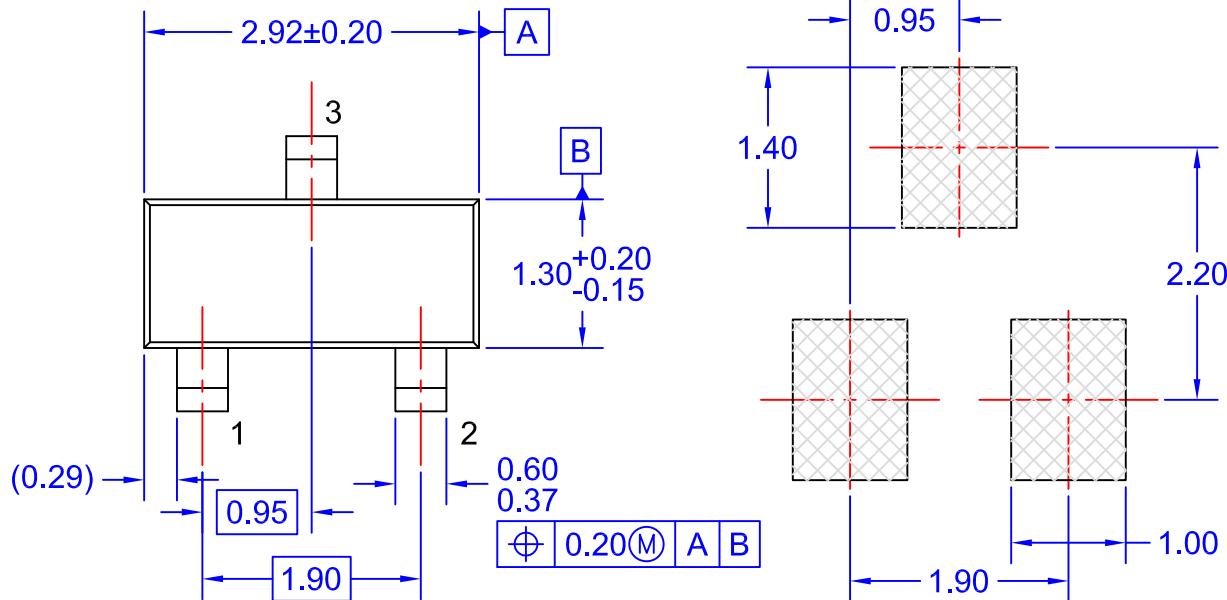




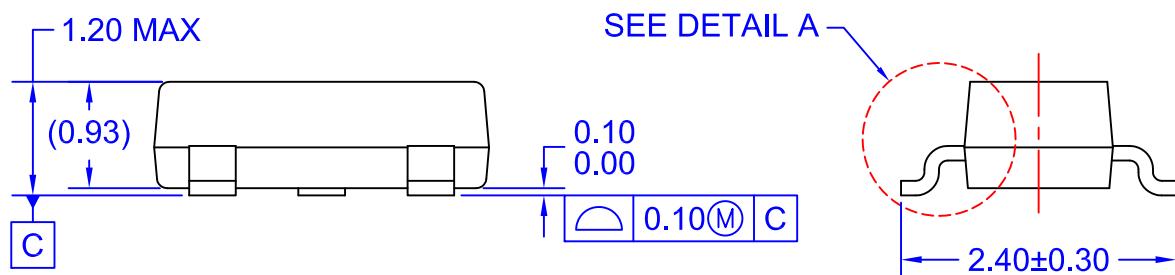
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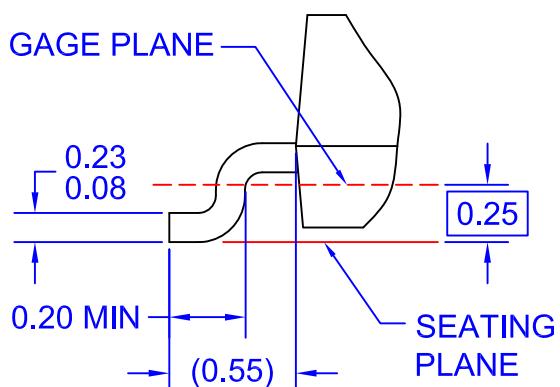




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ADVANCED
LINEAR
DEVICES, INC.

ALD1105

DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED PAIR MOSFET

GENERAL DESCRIPTION

The ALD1105 is a monolithic dual N-channel and dual P-channel complementary matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1116 N-channel MOSFET pair and an ALD1117 P-channel MOSFET pair in one package. The ALD1105 is a low drain current, low leakage current version of the ALD1103.

The ALD1105 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +1V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in complementary pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1105 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1105 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the field effect transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 30pA at room temperature. For example, DC beta of the device at a drain current of 3mA at 25°C is = 3mA/30pA = 100,000,000.

FEATURES

- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETs
- Low input capacitance
- Low V_{os} -- 10mV
- High input impedance -- $10^{13}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^9
- Matched N-channel pair and matched P-channel pair in one package

ORDERING INFORMATION

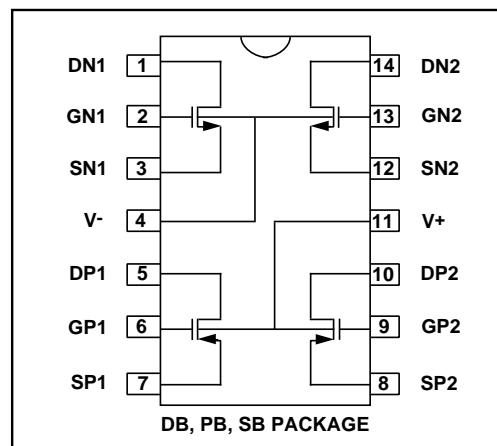
Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1105 DB	ALD1105 PB	ALD1105 SB

* Contact factory for industrial temperature range.

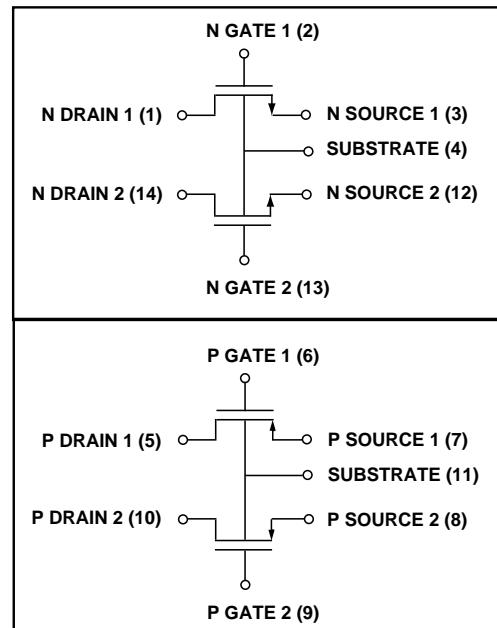
APPLICATIONS

- Precision current mirrors
- Complementary push-pull linear drives
- Discrete Analog switches
- Analog signal Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog current inverter
- Precision matched current sources

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Drain-source voltage, V _{DS}	13.2V
Gate-source voltage, V _{GS}	13.2V
Power dissipation	500 mW
Operating temperature range PB, SB package	0°C to +70°C
DB package	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature, 10 seconds	+260°C

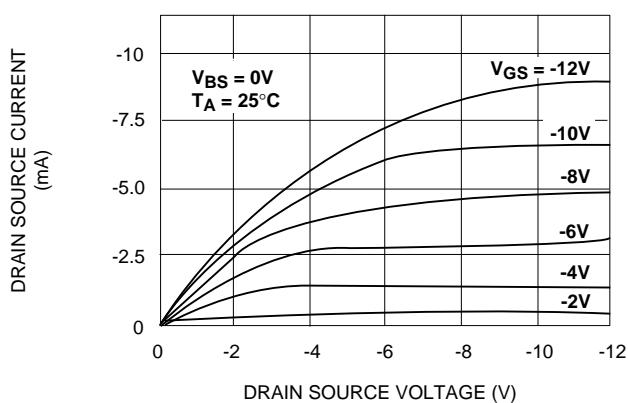
OPERATING ELECTRICAL CHARACTERISTICS

T_A = 25°C unless otherwise specified

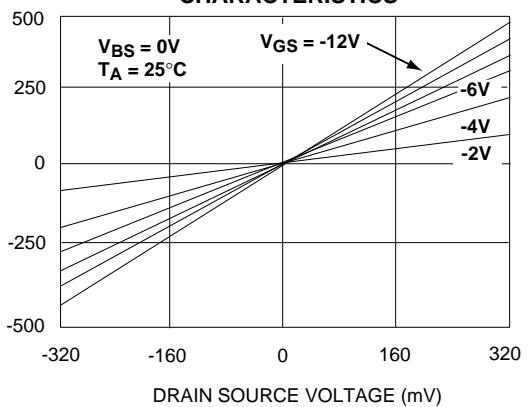
Parameter	Symbol	N - Channel			Unit	Test Conditions	P - Channel			Unit	Test Conditions
		Min	Typ	Max			Min	Typ	Max		
Gate Threshold Voltage	V _T	0.4	0.7	1.0	V	I _{DS} = 1µA V _{GS} = V _{DS}	-0.4	-0.7	-1.0	V	I _{DS} = -1µA V _{GS} = V _{DS}
Offset Voltage V _{GGS1} - V _{GGS2}	V _{os}		2	10	mV	I _{DS} = 10µA V _{GS} = V _{DS}		2	10	mV	I _{DS} = -10µA V _{GS} = V _{DS}
Gate Threshold Temperature Drift	T _{CVT}		-1.2		mV/°C			-1.3		mV/°C	
On Drain Current	I _{DS} (ON)	3	4.8		mA	V _{GS} = V _{DS} = 5V	-1.3	-2		mA	V _{GS} = V _{DS} = -5V
Trans.-conductance	G _{fs}	1	1.8		mmho	V _{DS} = 5V I _{DS} = 10mA	0.25	0.67		mmho	V _{DS} = -5V I _{DS} = -10mA
Mismatch	ΔG _{fs}		0.5		%			0.5		%	
Output Conductance	G _{OS}		200		µmho	V _{DS} = 5V I _{DS} = 10mA		40		µmho	V _{DS} = -5V I _{DS} = -10mA
Drain Source ON Resistance	R _{DS(ON)}		350	500	Ω	V _{DS} = 0.1V V _{GS} = 5V		1200	1800	Ω	V _{DS} = -0.1V V _{GS} = -5V
Drain Source ON Resistance Mismatch	ΔR _{DS(ON)}		0.5		%	V _{DS} = 0.1V V _{GS} = 5V		0.5		%	V _{DS} = -0.1V V _{GS} = -5V
Drain Source Breakdown Voltage	BV _{DSS}	12			V	I _{DS} = 1µA V _{GS} = 0V	-12			V	I _{DS} = -1µA V _{GS} = 0V
Off Drain Current	I _{DS(OFF)}		10	400 4	pA nA	V _{DS} = 12V I _{GS} = 0V T _A = 125°C		10	400 4	pA nA	V _{DS} = -12V V _{GS} = 0V T _A = 125°C
Gate Leakage Current	I _{GSS}		0.1	30 1	pA nA	V _{DS} = 0V V _{GS} = 12V T _A = 125°C		1	30 1	pA nA	V _{DS} = 0V V _{GS} = -12V T _A = 125°C
Input Capacitance	C _{ISS}		1	3	pF			1	3	pF	

P- CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

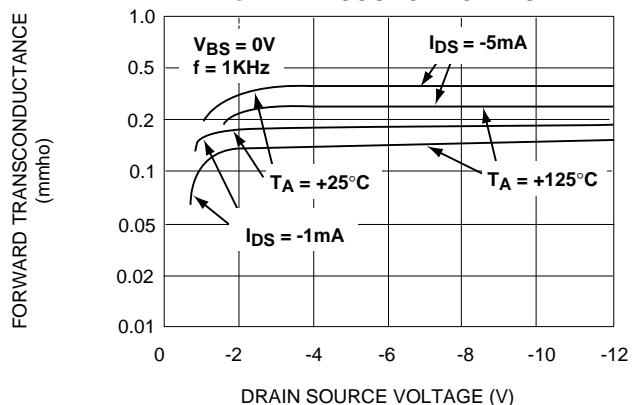
OUTPUT CHARACTERISTICS



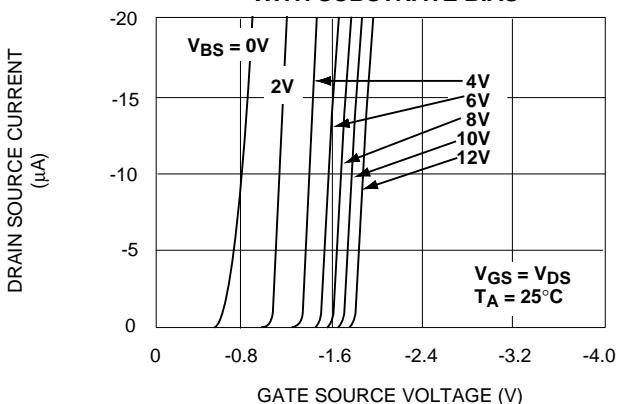
LOW VOLTAGE OUTPUT CHARACTERISTICS



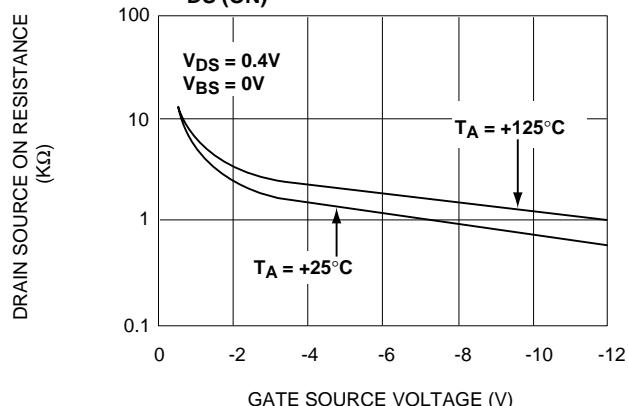
FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



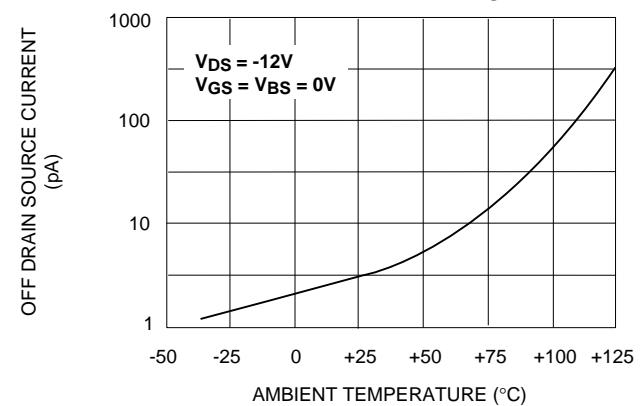
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



DRAIN SOURCE ON RESISTANCE R_{DSON} VS. GATE SOURCE VOLTAGE

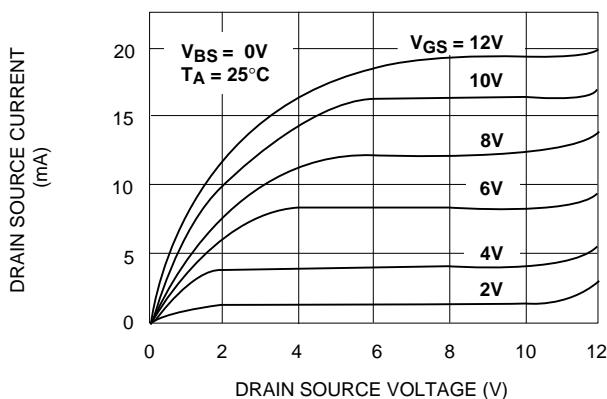


OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE

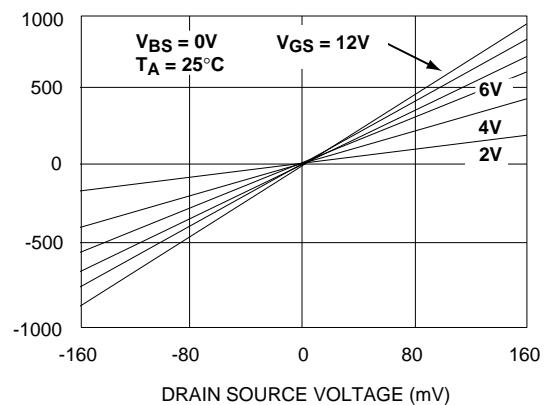


N- CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

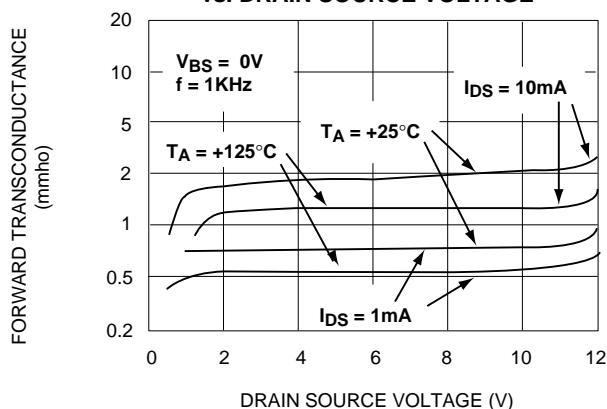
OUTPUT CHARACTERISTICS



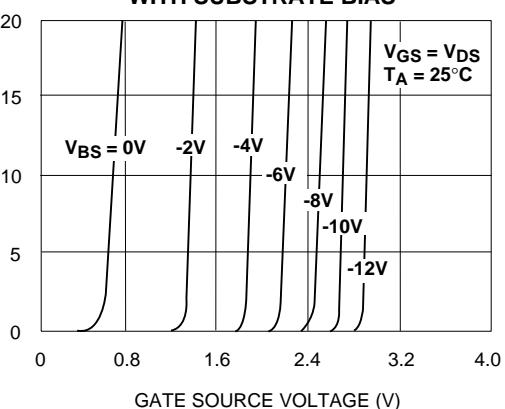
LOW VOLTAGE OUTPUT CHARACTERISTICS



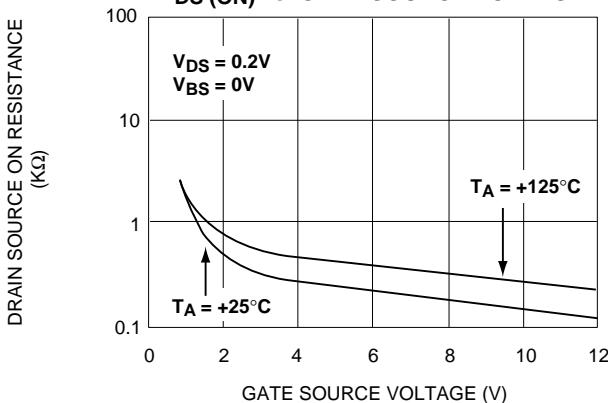
FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



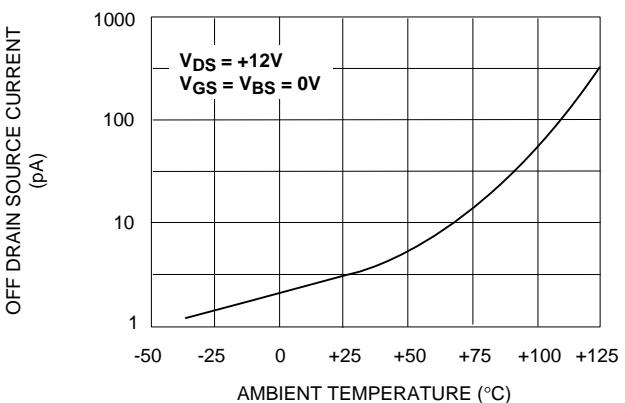
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



DRAIN SOURCE ON RESISTANCE R_DS (ON) vs. GATE SOURCE VOLTAGE

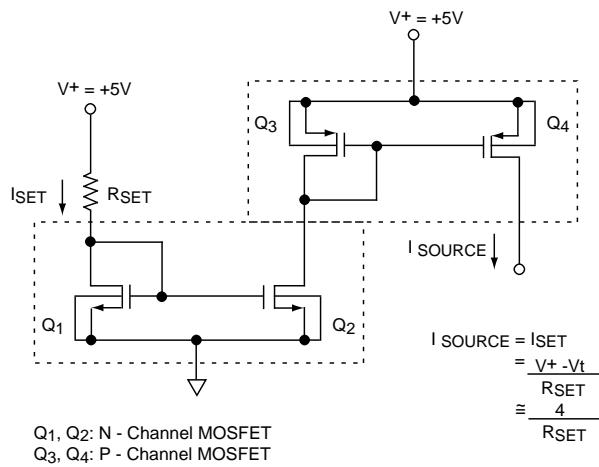


OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE

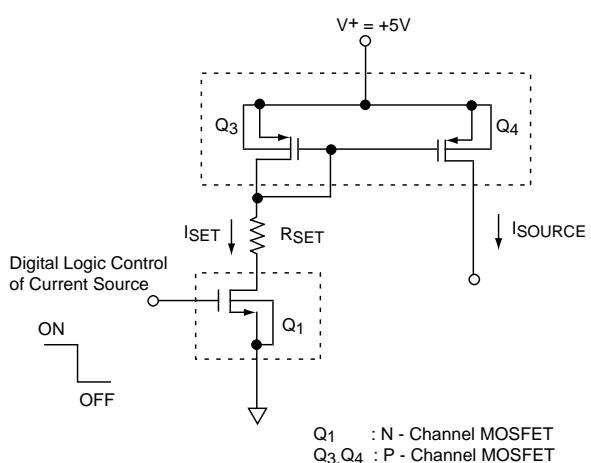


TYPICAL APPLICATIONS

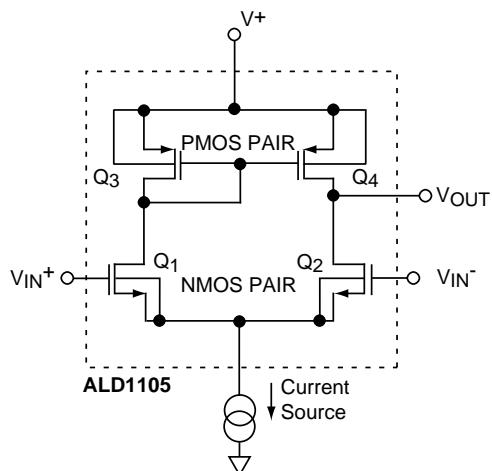
CURRENT SOURCE MIRROR



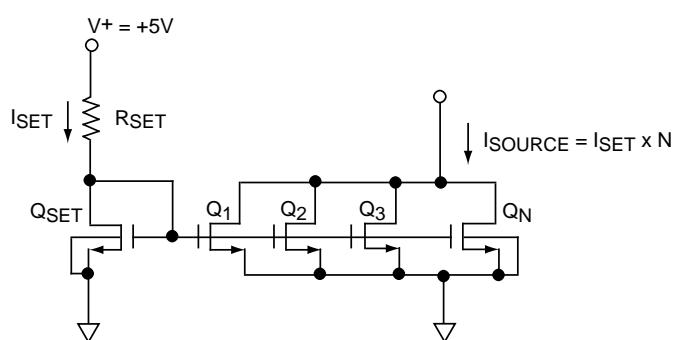
CURRENT SOURCE WITH GATE CONTROL



DIFFERENTIAL AMPLIFIER



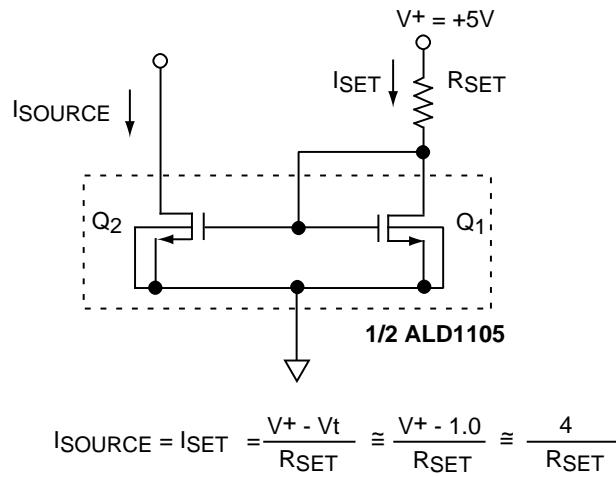
CURRENT SOURCE MULTIPLICATION



TYPICAL APPLICATIONS

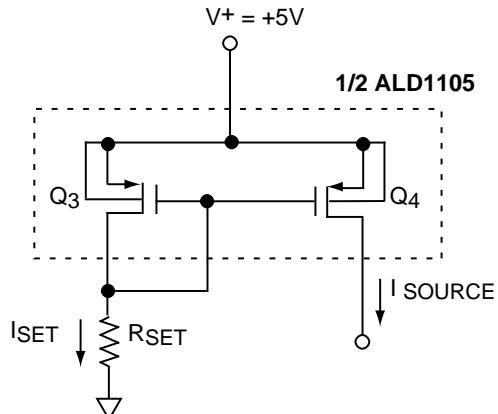
BASIC CURRENT SOURCES

N- CHANNEL CURRENT SOURCE



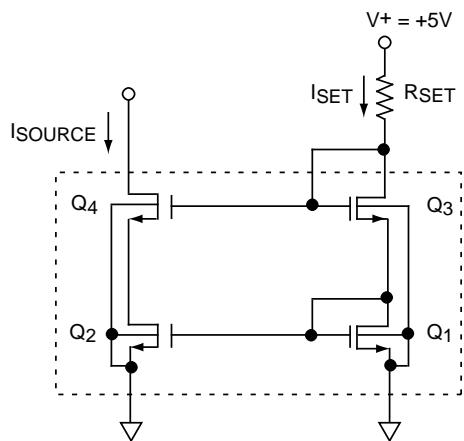
Q_1, Q_2 : N - Channel MOSFET

P- CHANNEL CURRENT SOURCE

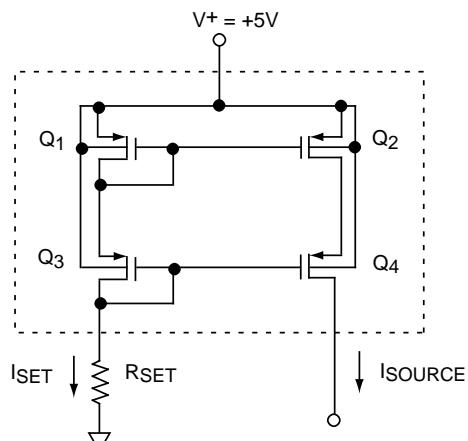


Q₃, Q₄: P - Channel MOSFET

CASCODE CURRENT SOURCES



Q1, Q2, Q3, Q4: N - Channel MOSFET
(1/2 ALD1105 + ALD1116)



$$I_{\text{SOURCE}} = I_{\text{SET}} = \frac{V^+ - 2V_t}{R_{\text{SET}}} \cong \frac{3}{R_{\text{SET}}}$$

Part III

Op Amplifiers

(blank)

Lab 11

Introduction to Operational Amplifiers

Table of Contents

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1.3.	Differential Mode	6
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2.2.	Slew Rate	7
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1. Operation Amplifier:

The standard operational amplifier (op-amp) symbol is shown in Figure 1(a). It has two input terminals, the inverting (-) input and the noninverting (+) input, and one output terminal. Most op-amps operate with two dc supply voltages, one positive and the other negative, as shown in Figure 1(b).

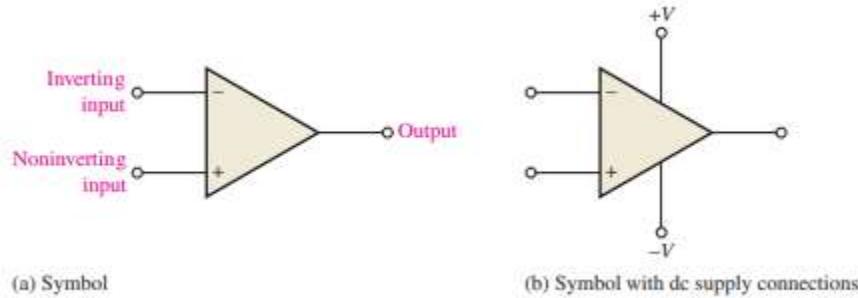


Figure 1. Op-amp symbols

1.1. Ideal Op-Amp:

The ideal op-amp has infinite voltage gain and infinite bandwidth. Also, it has an infinite input impedance (open) so that it does not load the driving source. Finally, it has a zero-output impedance. Op-amp characteristics are illustrated in Figure 2(a). The input voltage, V_{in} , appears between the two input terminals, and the output voltage is $A_v V_{in}$, as indicated by the internal voltage source symbol. The concept of infinite input impedance is a particularly valuable analysis tool for the various op-amp configurations.

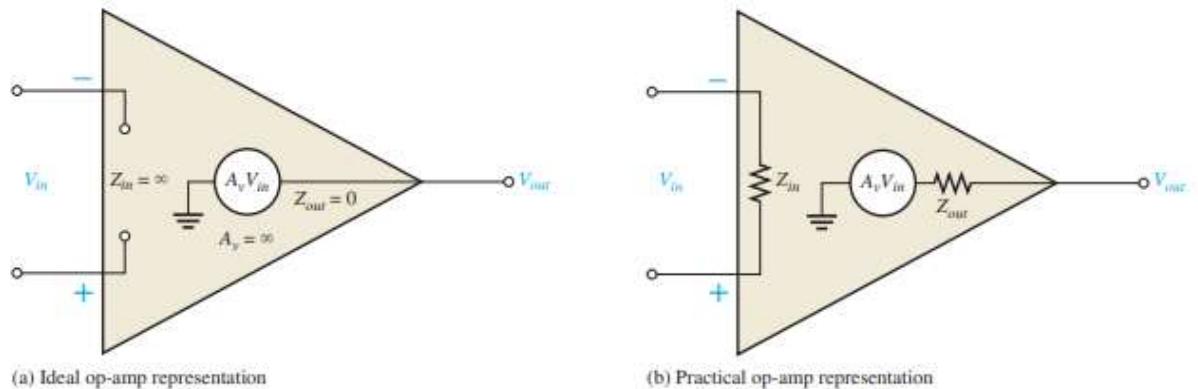


Figure 2. Basic Op-Amp representation

1.2. Practical Op-Amp:

Op-amps have both voltage and current limitations. Peak-to-peak output voltage, for example, is usually limited to slightly less than the two supply voltages. Output current is also limited by internal restrictions such as power dissipation and component ratings. Characteristics of a practical op-amp are very high voltage gain, very high input impedance, and very low output impedance. These are labelled in Figure 2(b). Another practical consideration is that there is always noise generated within the op-amp.

1.3. Differential Mode:

In the differential mode, either one signal is applied to an input with the other input grounded or two opposite-polarity signals are applied to the inputs. When an op-amp is operated in the single-ended differential mode, one input is grounded and a signal voltage is applied to the other input, as shown in Figure 3. In the case where the signal voltage is applied to the inverting input as in part (a), an inverted, amplified signal voltage appears at the output. In the case where the signal is applied to the noninverting input with the inverting input grounded, as in Figure 3(b), a noninverted, amplified signal voltage appears at the output.

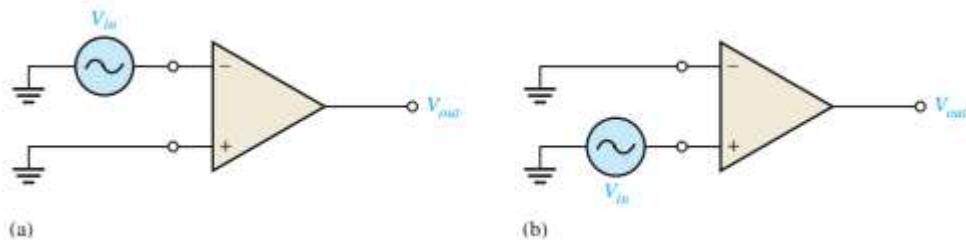


Figure 3. Single-ended differential mode

In the double-ended differential mode, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in Figure 4(a). The amplified difference between the two inputs appears on the output. Equivalently, the double-ended differential mode can be represented by a single source connected between the two inputs, as shown in Figure 4(b).

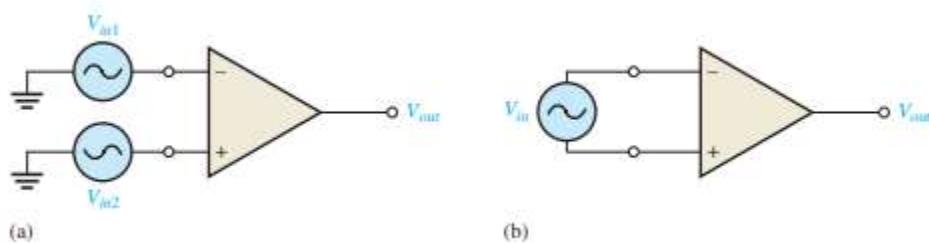


Figure 4. Double-ended differential mode

1.4. Common Mode:

In the common mode, two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in Figure 5. When equal input signals are applied to both inputs, they tend to cancel, resulting in a zero-output voltage.

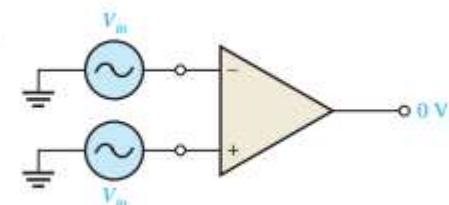


Figure 5. Common-mode operation

This action is called common-mode rejection. Its importance lies in the situation where an unwanted signal appears commonly on both op-amp inputs. Common-mode rejection means that this unwanted signal will not appear on the output and distort the desired signal. Common-mode signals (noise) generally are the result of the pick-up of radiated energy on the input lines, from adjacent lines, the 60 Hz power line, or other sources.

2. Op-Amp Parameters:

2.1. Common-mode rejection ratio:

Desired signals can appear on only one input or with opposite polarities on both input lines. These desired signals are amplified and appear on the output as previously discussed. Unwanted signals (noise) appearing with the same polarity on both input lines are essentially cancelled by the op-amp and do not appear on the output. The measure of an amplifier's ability to reject common-mode signals is a parameter called the CMRR (common-mode rejection ratio).

Ideally, an op-amp provides a very high gain for differential-mode signals and zero gain for common-mode signals. Practical op-amps, however, do exhibit a very small common-mode gain (usually much less than 1), while providing a high open-loop differential voltage gain (usually several thousand). The higher the open-loop gain with respect to the common-mode gain, the better the performance of the op-amp in terms of rejection of common-mode signals. This suggests that a good measure of the op-amp's performance in rejecting unwanted common-mode signals is the ratio of the open-loop differential voltage gain, A_{ol} , to the common-mode gain, A_{cm} . This ratio is the common-mode rejection ratio, CMRR.

$$CMRR = \frac{A_{ol}}{A_{cm}}$$

The higher the CMRR, the better. A very high value of CMRR means that the open-loop gain, A_{ol} , is high and the common-mode gain, A_{cm} , is low. The CMRR is often expressed in decibels (dB) as

$$CMMR = 20$$

2.2. Slew Rate:

The maximum rate of change of the output voltage in response to a step input voltage is the slew rate of an op-amp. The slew rate is dependent upon the high-frequency response of the amplifier stages within the op-amp.

Slew rate is measured with an op-amp connected as shown in Figure 6(a). This particular op-amp connection is a unity-gain. It gives a worst-case (slowest) slew rate. Recall that the high frequency components of a voltage step are contained in the rising edge and that the upper critical frequency of an amplifier limits its response to a step input. For a step input, the slope on the output is inversely proportional to the upper critical frequency. Slope increases as upper critical frequency decreases.

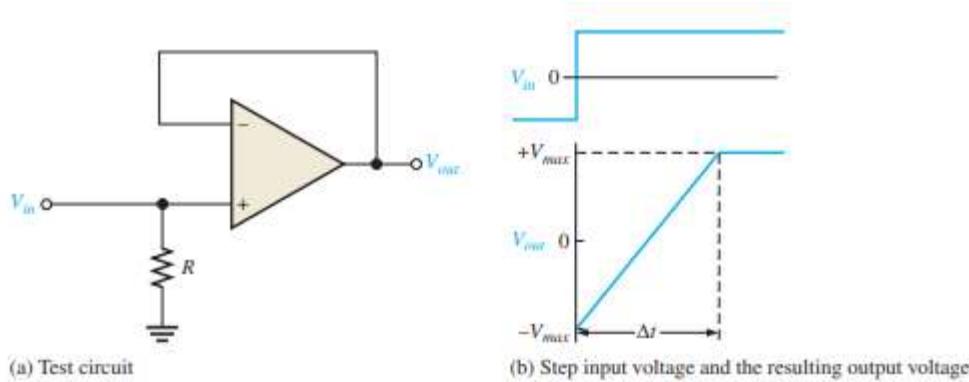


Figure 6. Slew rate measurement

A pulse is applied to the input and the resulting ideal output voltage is indicated in Figure 6(b). The width of the input pulse must be sufficient to allow the output to “slew” from its lower limit to its upper limit. A certain time interval, is required for the output voltage to go from its lower limit to its upper limit once the input step is applied. The slew rate is expressed as $+V_{max} - V_{min}$

$$\text{Slew rate} = \frac{\Delta V_{out}}{\Delta t}$$

Where $\Delta V_{out} = + V_{max} - (V_{min})$. The unit of slew rate is volts per microsecond ($V/\mu\text{sec}$).

2.3. Noninverting Amplifier:

An op-amp connected in a closed-loop configuration as a noninverting amplifier with a controlled amount of voltage gain is shown in Figure 7. The input signal is applied to the noninverting (+) input. The output is applied back to the inverting input through the feedback circuit (closed loop) formed by the input resistor R_i and the feedback resistor R_f . This creates negative feedback as follows. Resistors R_i and R_f form a voltage-divider circuit, which reduces V_{out} and connects the reduced voltage V_f to the inverting input. The feedback voltage is expressed as

$$V_f = \left(\frac{R_i}{R_i + R_f} \right) V_{out}$$

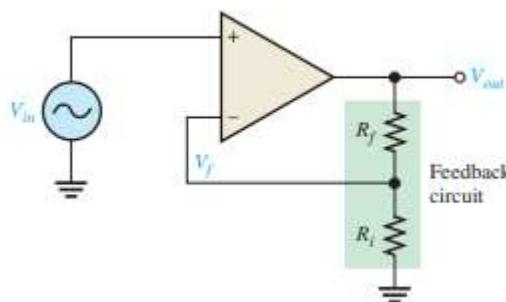


Figure 7. Noninverting amplifier

The difference of the input voltage, V_{in} , and the feedback voltage, V_f , is the differential input to the op-amp, as shown in Figure 12–17. This differential voltage is amplified by the open-loop voltage gain of the op-amp (A_{ol}) and produces an output voltage expressed as

$$V_{out} = A_{ol}(V_{in} - V_f)$$

The attenuation, B of the feedback circuit is

$$B = \frac{R_i}{R_i + R_f}$$

Substituting BV_{out} for V_f in the V_{out} equation,

$$V_{out} = A_{ol}(V_{in} - BV_{out})$$

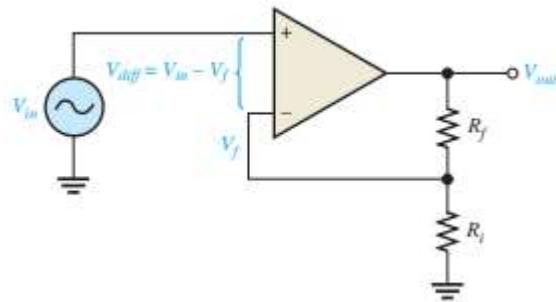


Figure 8. Differential input, $V_{in} - V_f$

Then applying basic algebra,

$$\begin{aligned} V_{out} &= A_{ol}V_{in} - A_{ol}BV_{out} \\ V_{out} + A_{ol}BV_{out} &= A_{ol}V_{in} \\ V_{out}(1 + A_{ol}B) &= A_{ol}V_{in} \end{aligned}$$

Since the overall voltage gain of the amplifier in Figure 7 is V_{out}/V_{in} , it can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{A_{ol}}{1 + A_{ol}B}$$

The product of $A_{ol}B$ is typically much greater than 1, so the equation simplifies to

$$\frac{V_{out}}{V_{in}} \cong \frac{A_{ol}}{A_{ol}B} = \frac{1}{B}$$

The closed-loop gain of the noninverting (NI) amplifier is the reciprocal of the attenuation (B) of the feedback circuit (voltage-divider).

$$A_{cl(NI)} = \frac{V_{out}}{V_{in}} \cong \frac{1}{B} = \frac{R_i + R_f}{R_i}$$

Therefore,

$$A_{cl(NI)} = 1 + \frac{R_f}{R_i}$$

Notice that the closed-loop voltage gain is not at all dependent on the op-amp's open-loop voltage gain under the condition $A_{ol}B \gg 1$. The closed-loop gain can be set by selecting values of R_i and R_f .

2.4. Inverting Amplifier:

An op-amp connected as an inverting amplifier with a controlled amount of voltage gain is shown in Figure 9. The input signal is applied through a series input resistor R_i to the inverting input. Also, the output is fed back through R_f to the same input. The noninverting (+) input is grounded.

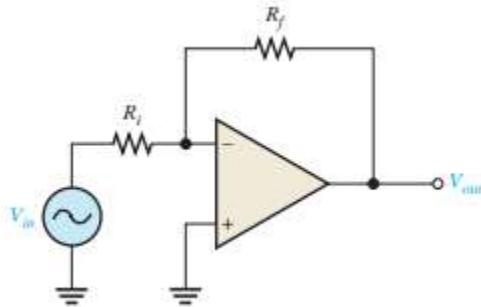


Figure 9. Inverting amplifier

At this point, the ideal op-amp parameters mentioned earlier are useful in simplifying the analysis of this circuit. In particular, the concept of infinite input impedance is of great value. An infinite input impedance implies zero current at the inverting input. If there is zero current through the input impedance, then there must be no voltage drop between the inverting and noninverting inputs. This means that the voltage at the inverting input is zero because the noninverting (+) input is grounded. This zero voltage at the inverting input terminal is referred to as virtual ground. This condition is illustrated in Figure 10(a). Since there is no current at the inverting input, the current through R_i and the current through R_f are equal, as shown in Figure 10(b).

$$I_{in} = I_f$$

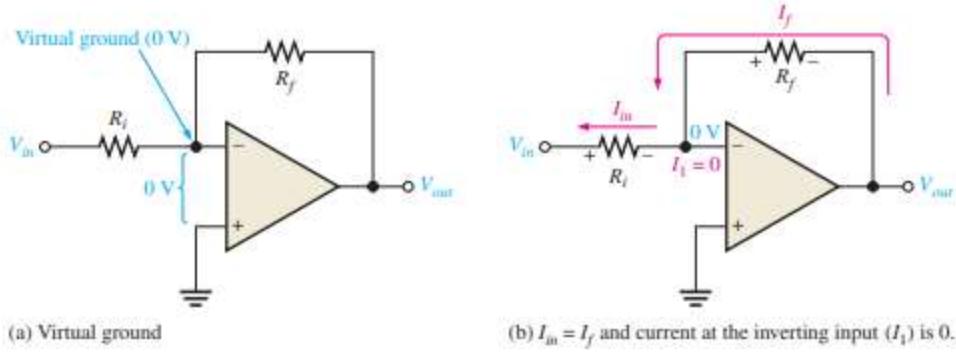


Figure 10. Virtual ground concept and closed loop voltage gain development for the inverting amplifier.

The voltage across R_i equals V_{in} because the resistor is connected to virtual ground at the inverting input of the op-amp. Therefore,

$$I_{in} = \frac{V_{in}}{R_i}$$

Also, the voltage across R_f equals $-V_{out}$ because of virtual ground, and therefore,

$$I_f = -\frac{V_{out}}{R_f}$$

Since $I_f = I_{in}$,

$$-\frac{V_{out}}{R_f} = \frac{V_{in}}{R_i}$$

Rearranging the terms,

$$\frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$$

Of course, V_{out}/V_{in} is the overall gain of the inverting (I) amplifier.

$$A_{cl(I)} = -\frac{R_f}{R_i}$$

Above equation shows that the closed-loop voltage gain of the inverting amplifier ($A_{cl(I)}$) is the ratio of the feedback resistance (R_f) to the input resistance (R_i). The closed loop gain is independent of the op-amp's internal open-loop gain. Thus, the negative feedback stabilizes the voltage gain. The negative sign indicates inversion.

(blank)

Lab 12

Op-Amp Slew Rate and Common- Mode Rejection

LAB 12.1: Op-Amp Slew Rate

PURPOSE AND BACKGROUND

The purpose of this experiment is to measure the slew rate of a 741 operational amplifier. The slew rate, a large parameter, is defined as the maximum time rate of change of the output voltage of an op-amp in response to a step input voltage. Expressed in units of volts per microsecond ($V/\mu s$), the slew rate is dependent upon the frequency response of the internal stages of the op-amp. Thus, the higher the slew rate, the better the frequency response of the amplifier.

The measurement of the operational amplifier's slew rate is always accomplished with a large signal amplifier having a *unity gain* with a high frequency input signal.

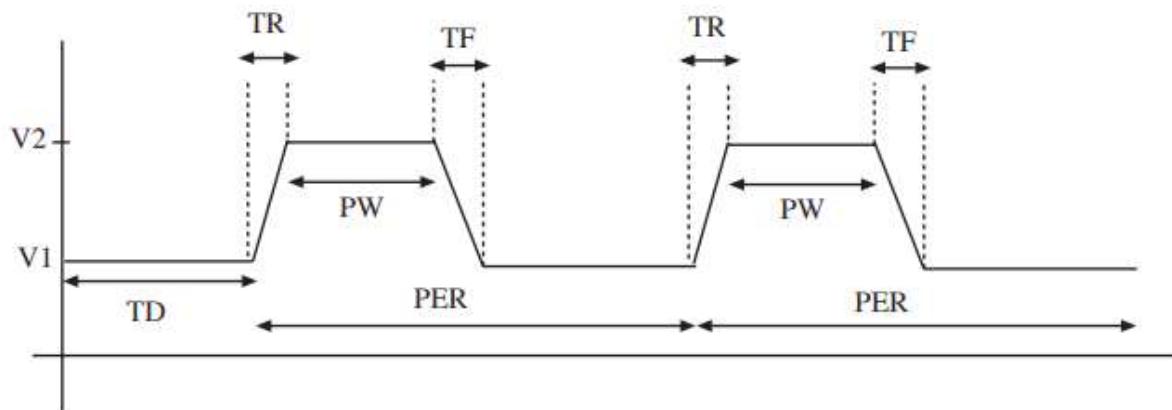
PRELAB ASSIGNMENT (MUST BE SUBMITTED ONE DAY PRIOR TO CLASS)

Using PSpice, simulate the circuits in Figures 12.1-1 and 12.2-1. Using the *USEFUL FORMULAS*, calculate the slew rate and observe the phase relationship between the input and output waveforms of the circuit in Figure 12.1-1. With the circuit in Figure 12.2-1, observe the phase relationship between the input and output waveforms, and calculate the common-mode voltage gain, differential amplifier gain, and common-mode rejection ratio using Useful Formulas at the end of this lab manual.

HOW TO GENERATE A SQUARE WAVE (PULSE WAVEFORM) IN PSpice:

Place a pulse voltage source by selecting *Place>PSpice Component>Source>Voltage Sources>Pulse*. An icon should appear, place the component on the design.

The icon represents a pulse waveform with the parameters, $V1$, $V2$, TD , TR , TF , PW , and PER . The image below depicts what each of the parameters represent in the pulse waveform, and how to create a square wave.

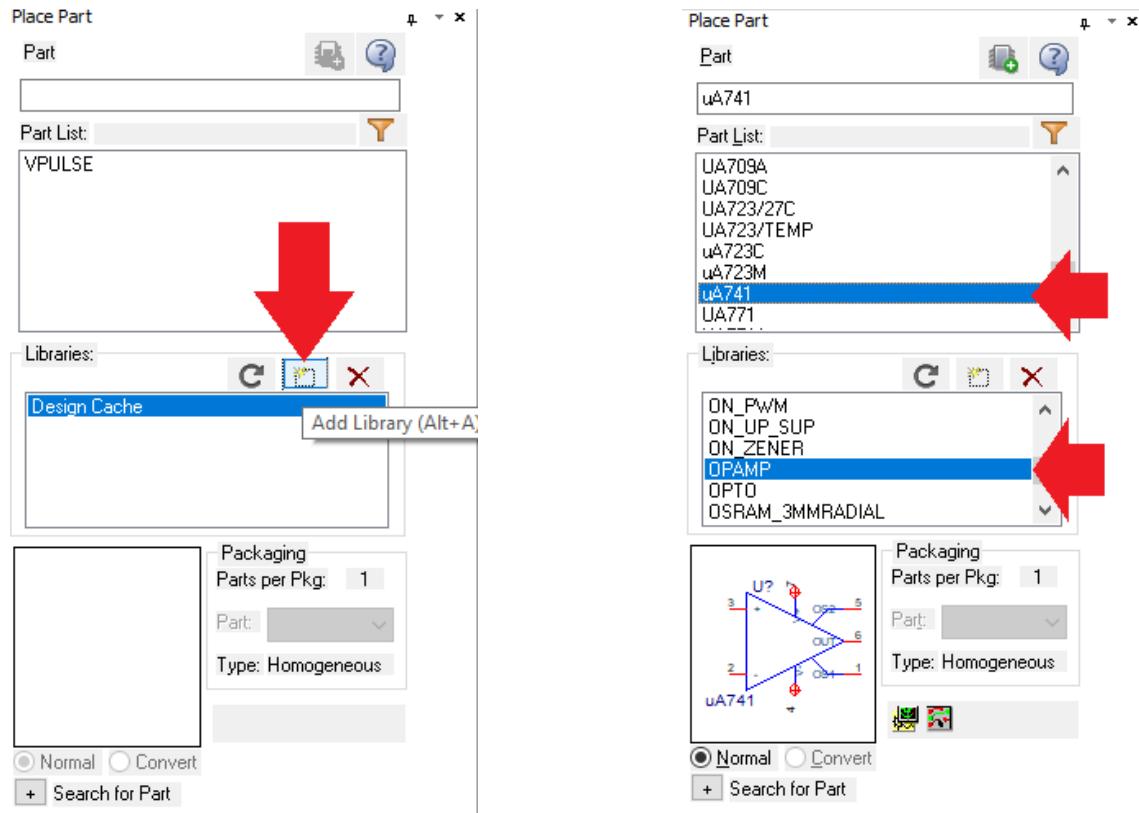


Therefore, the period would be $\frac{1}{frequency\ (Hz)} = PER$. TD is the time delay before the output waveform begins. PW is the pulse width, or the time of the period that the square wave is at the

peak value. Also, TR and TF are the time rise and time fall values, which will be zero for a true square wave. Finally, V1 and V2 represent the minimum and maximum voltage levels.

HOW TO ADD THE CORRECT LMT741 OP-AMP TO PSpice LIBRARY:

Before assembling the circuit in PSpice, the correct op amp library needs to be added. If the Place Part tab is not visible, select *Place>Part* and from the Place Part tab, click on the *Add Library* icon, which is the middle of the three icons, just below *Libraries*.



Open the folder “*pspice*” and select every element in this folder, excluding any subfolders and click *Open*. Now, several entries should be seen under *Libraries* in the *Place Part* tab. Select the “*OPAMP*” library and in the above *Part List*, scroll until you find the uA741 Op-Amp. This is the correct part that will be needed to properly run the simulations for the prelab assignments.

The pinout of the Op-Amp is available in the LM741 data sheet. Note that the offset null pins (1 and 5), as well as pin 8 are all connected to an open circuit (See Figure 12.1-2).

REQUIRED PARTS AND EQUIPMENT

- ❖ Two 10 kΩ Resistors (1/4 W)
- ❖ Two 0-15 V DC power supplies
- ❖ 741 Op-Amp (8 pin DIP)
- ❖ Signal Generator
- ❖ Dual Trace Oscilloscope

❖ Breadboard

PROCEDURE

- 1) Wire the circuit depicted in Figure 12.1-1, and set your oscilloscope to the following approximate settings:
Channel 1: 5V/division
Channel 2: 1V/division
Time Base: 10 μ s/division
- 2) Apply power to the breadboard and adjust the square-wave input signal at 5 V peak-to-peak with a frequency of 10 kHz. The output signal should have a trapezoidal shape, as shown in Figure 12.1-3. If the operational amplifier were ideal (infinite slew rate), the output signal would look the same as the input signal at very high frequencies, except for the phase shift. Because the op-amp is not ideal, it does take a finite amount of time for the large-signal amplifier to switch from one voltage extreme to the other.
- 3) Measure the peak-to-peak voltage, ΔV , and record your result in Table 12.1-1.

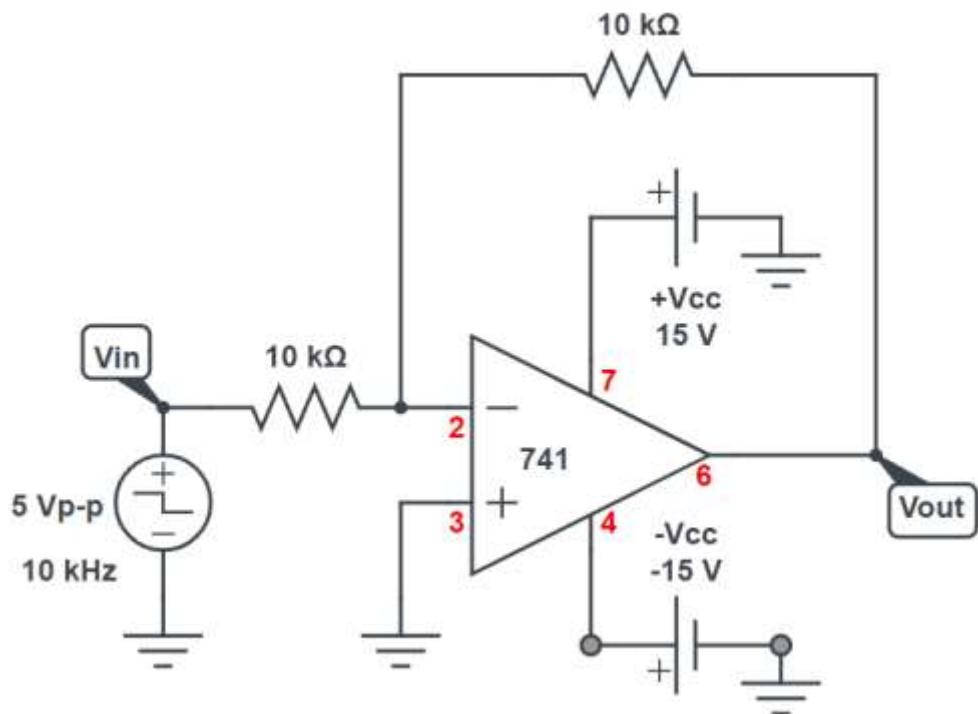


FIGURE 12.1-1: Schematic Diagram of Op-Amp Circuit

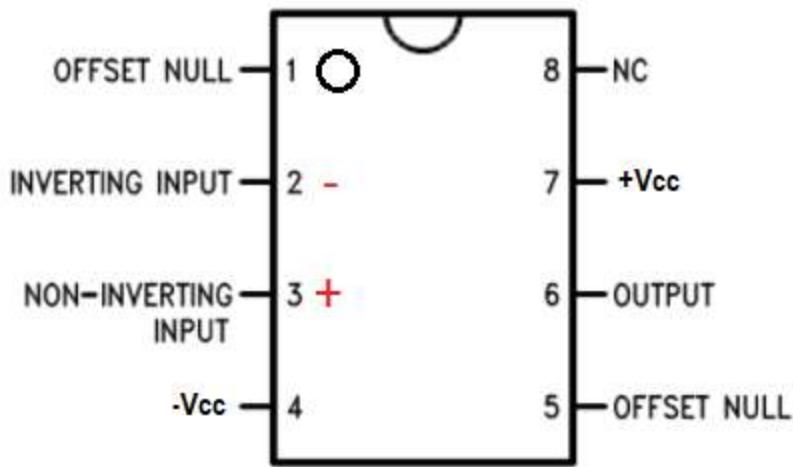


FIGURE 12.1-2: Pin Diagram of 741 Op-Amp

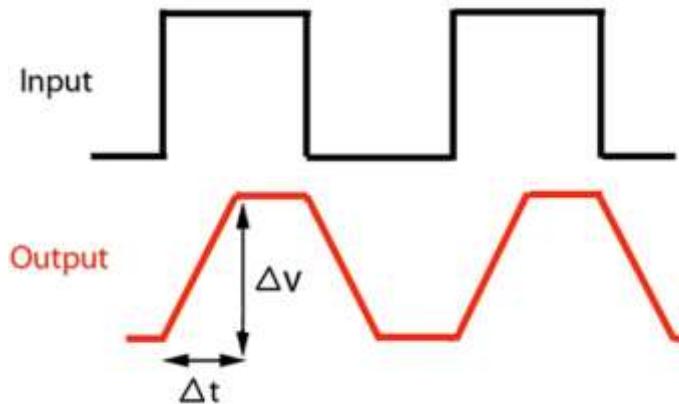


FIGURE 12.1-3

- 4) Measure Δt , the time in microseconds that it takes the output voltage to swing from its minimum to its maximum value, or vice versa. Record the value in Table 12.1-1.
 - 5) From the measurements in Steps 3 and 4, calculate the slew rate ($\Delta V/\Delta t$), for the 741 amplifier and record the results in table 12.1-1.
- Slew rate for an operational amplifier is measured with an amplifier in a closed loop gain of unity.

DATA FOR EXPERIMENT – OP-AMP SLEW RATE

ΔV	V
Δt	μs
<i>Slew Rate</i>	$V/\mu s$

TABLE 12.1-1: Slew Rate Data

LAB 12.2: Common-Mode Rejection

PURPOSE AND BACKGROUND

The purpose of this experiment is to measure the common-mode rejection of a 741 operational amplifier. If the same signal is applied simultaneously to both inputs, called the *common-mode input*, then the output voltage of an ideal op-amp should be zero. Since the operational amplifiers are not ideal devices, a small but finite amount of output voltage will be present when both the input voltages are the same. The ratio of the common-mode input voltage to the generated output voltage is termed as the *common-mode rejection*, or *CMR*, and is expressed in decibels. The higher the CMR, the better the rejection and the smaller the output voltage.

REQUIRED PARTS AND EQUIPMENT

- ❖ Resistors
 - Two 100 kΩ
 - Two 100 Ω
 - 10 kΩ
- ❖ Two 0-15 V DC Power Supplies
- ❖ 100 kΩ Potentiometer or 10 Turn Trim Pot
- ❖ 741 Operational Amplifier (8-pin mini-DIP)
- ❖ Signal Generator
- ❖ Dual Trace Oscilloscope
- ❖ Breadboard

PROCEDURE

- 1) Wire the circuit shown in the schematic diagram in Figure 12.2-1, and set the oscilloscope for the following approximate settings
 - Channel 1: 2 V/division, AC coupling
 - Channel 2: 0.02 V/division, AC coupling
 - Time Base: 5 ms/division
- 2) Apply power to the breadboard and set the input voltage, called the *common-mode input voltage* ($V_{in(com)}$), to 10 V peak-to-peak at a frequency of approximately 60 Hz. You should make this voltage setting as accurate as possible.
- 3) Using the oscilloscope, measure the peak-to-peak common-mode input and output voltages. Record your results in Table 12.2-1. From the common-mode input and output voltages, calculate the common-mode voltage gain, A_{com} (Equation 2), recording this result in Table 12.2-1.

- 4) This circuit is called a *difference*, or *differential amplifier* and the differential voltage gain A_d , is based upon all four resistors, as given in the *USEFUL FORMULAS* section of this experiment (Equation 1). First, calculate the differential voltage gain, and then use it to calculate the common-mode rejection (in decibels) for the 741 operational amplifier. Record the results in Table 12.2-1.

Most manufacturers of the 741 op-amp cite a minimum CMR of 70 dB, although a value of 90 dB is typical.

- 5) In some instances, the CMR may be improved by trimming one or more of the resistors of the circuit in Figure 12.2-1. Disconnect the AC signal generator and DC power supplies from the circuit. Replace R_4 with a series connection of a $100\text{ k}\Omega$ potentiometer and a $10\text{ k}\Omega$ resistor.

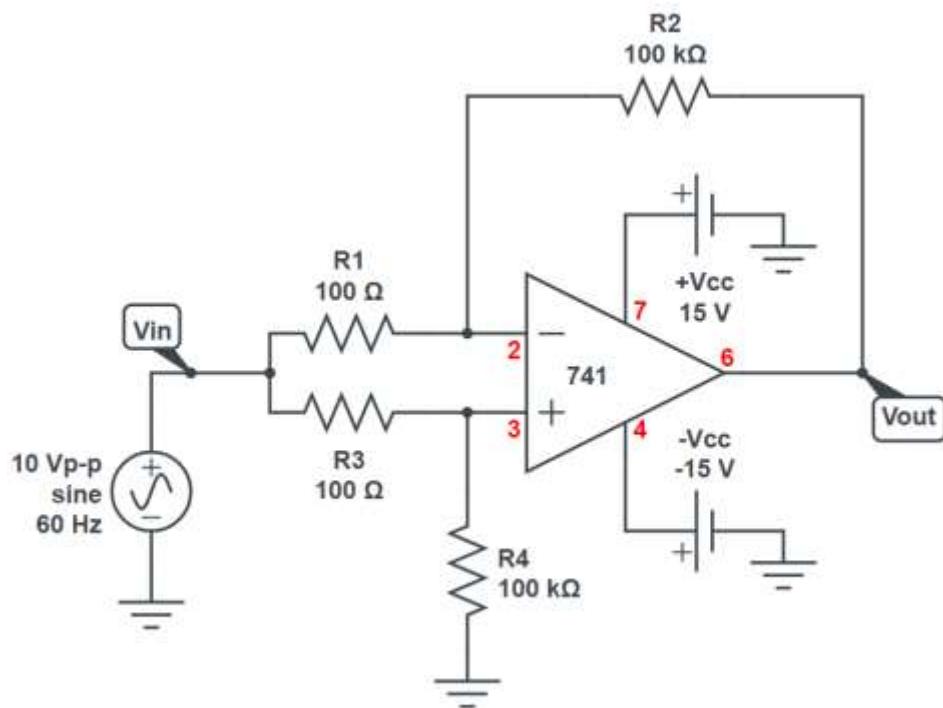


FIGURE 12.2-1: Schematic Diagram of Circuit

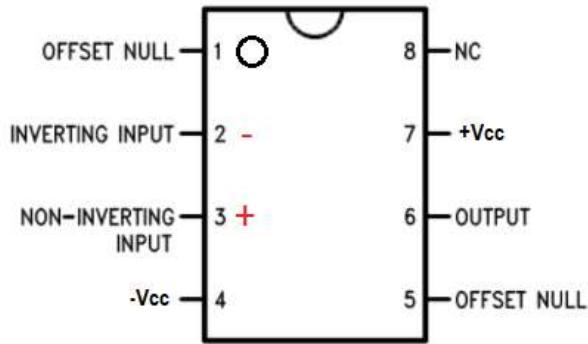


FIGURE 12.2-2: Pin Diagram of 741 Operational Amplifier

- 6) Apply power to the breadboard, and again adjust the common-mode input voltage to 10 V peak-to-peak at a frequency of 60 Hz.
- 7) Using the oscilloscope to observe the output of the operational amplifier at pin 6 and adjust the 100 kΩ potentiometer for a minimum output voltage.
- 8) Repeat Steps 3 and 4, using a differential gain of 1000. Record your results in Table 12.2-2. Do you see an improvement in the CMR?

FOR FURTHER INVESTIGATION

Use another 741 operational amplifier and repeat the experiment. Without adjustment, is the CMR for the second device significantly different from the first one?

WHAT YOU HAVE DONE

This experiment demonstrated how to measure the common-mode rejection (CMR) of a 741 operational amplifier and how to maximize the CMR of a difference amplifier. For an ideal operational amplifier, the common-mode input voltage should be zero, giving an infinite value for the CMR. The ratio for the common-mode input voltage to the generated output voltage is termed the *common-mode rejection ratio* or CMRR. When expressed in decibels, it is called the *common-mode rejection* (CMR). The higher the CMR, the better the rejection, resulting in a smaller output voltage.

DATA FOR EXPERIMENT – OP-AMP COMMON-MODE REJECTION

Measured common-mode input voltage, $V_{in(com)}$	V
Measured common-mode output voltage, $V_{out(com)}$	V
Calculated common-mode voltage gain, A_{com}	
Calculated differential voltage gain, A_d	
Calculated common-mode rejection, CMR	dB

FIGURE 12.2-1: Common-Mode Rejection

<i>Measured common-mode input voltage, $V_{in(com)}$</i>	V
<i>Measured common-mode output voltage, $V_{out(com)}$</i>	V
<i>Calculated common-mode voltage gain, A_{com}</i>	
<i>Calculated differential voltage gain, A_d</i>	
<i>Calculated common-mode rejection, CMR</i>	dB

FIGURE 12.2-2: Common-Mode Rejection (Adjusted)

USEFUL FORMULAS

Differential Amplifier Voltage Gain

$$1) \quad A_d = \frac{R_2}{R_1} \text{ where } R_1 = R_3 \text{ and } R_2 = R_4$$

Common-Mode Voltage Gain

$$2) \quad A_{com} = \frac{V_{out(com)}}{V_{in(com)}}$$

dB Common-Mode Rejection

$$3) \quad CMR(dB) = 20 \cdot \log\left(\frac{A_d}{A_{com}}\right)$$

POST LAB ASSIGNMENT (TO BE SUBMITTED WITH LAB REPORT)

- 1) The Maximum time rate of change of output voltage of the circuit in Figure 12.1-1 in response to a step input is termed as _____ and its units are expressed in terms of _____.

- 2) From the LM741 data sheet, what is the typical slew rate and the common-mode rejection?

- 3) In a differential amplifier, the signal applied simultaneously to both inputs, is the _____.
 - a) Differential Input
 - b) Noninverting Input
 - c) Inverting Input
 - d) Common-Mode Input

- 4) An increase in common-mode rejection means an increase in the amplifier's _____.
 - a) Input Impedance
 - b) Frequency Response
 - c) Voltage Gain
 - d) Noise Immunity

- 5) For an ideal operational amplifier, the common-mode output voltage should be _____ and the units of common-mode rejection is expressed in terms of _____.

Lab 13

Op-Amp Inverting, Non-Inverting Amplifiers and Comparators

LAB 13.1: OP-AMP INVERTING AND NON-INVERTING AMPLIFIERS

PURPOSE AND BACKGROUND

The purpose of this experiment is to demonstrate the operation of both inverting and noninverting amplifier circuits using a 741 operational amplifier. Both circuits operate in the closed-loop mode. The inverting amplifier's closed loop voltage gain can be less than, equal to, or greater than unity (1). As the name implies, its output signal is always inverted with respect to its input signal. On the other hand, the noninverting amplifier's closed-loop voltage gain is always greater than unity (1), while the input and output signals are always in-phase.

PRELAB ASSIGNMENT (MUST BE SUBMITTED ONE DAY PRIOR TO CLASS)

Simulate the circuits in Figures 13.1-1A, 13.1-1B, 13.2-1A, and 13.2-1B. in PSpice, observe both the input and the output waveforms of the circuits and describe the phase relationship between the input and output of the respective circuits. Calculate the expected values for Tables 13.1-1, and 13.1-2 using the equations in the *Useful Formulas* section of this lab manual. What is the voltage gain from the input-output waveforms of circuits 13.1-1A and 13.1-1B?

REQUIRED PARTS AND EQUIPMENT

- ❖ Resistors:
 - 1 kΩ
 - 4.7 kΩ
 - Two 10 kΩ
 - 22 kΩ
 - 47 kΩ
 - 100 kΩ
- ❖ Breadboard
- ❖ 741 Operational Amplifier
- ❖ Analog Discovery 2
- ❖ Jumper Wires
- ❖ Breadboard

PROCEDURE

1. Wire the inverting amplifier circuit shown in the schematic diagram in Figure 13.1-1A.
2. Apply the power to the breadboard and adjust the input voltage (v_{in}) to 1 V peak-to-peak at a frequency of 500 Hz. Position the input voltage above the output voltage on the scope's display. What is the difference between the two signals?

Notice that the output signal is of opposite form, or is inverted, compared to the input signal (shown in Figure 13.1-3). The output voltage is then said to be inverted from, or 180° out-of-phase with, the input signal since the positive peak of the output signal occurs when the input's peak voltage is negative.

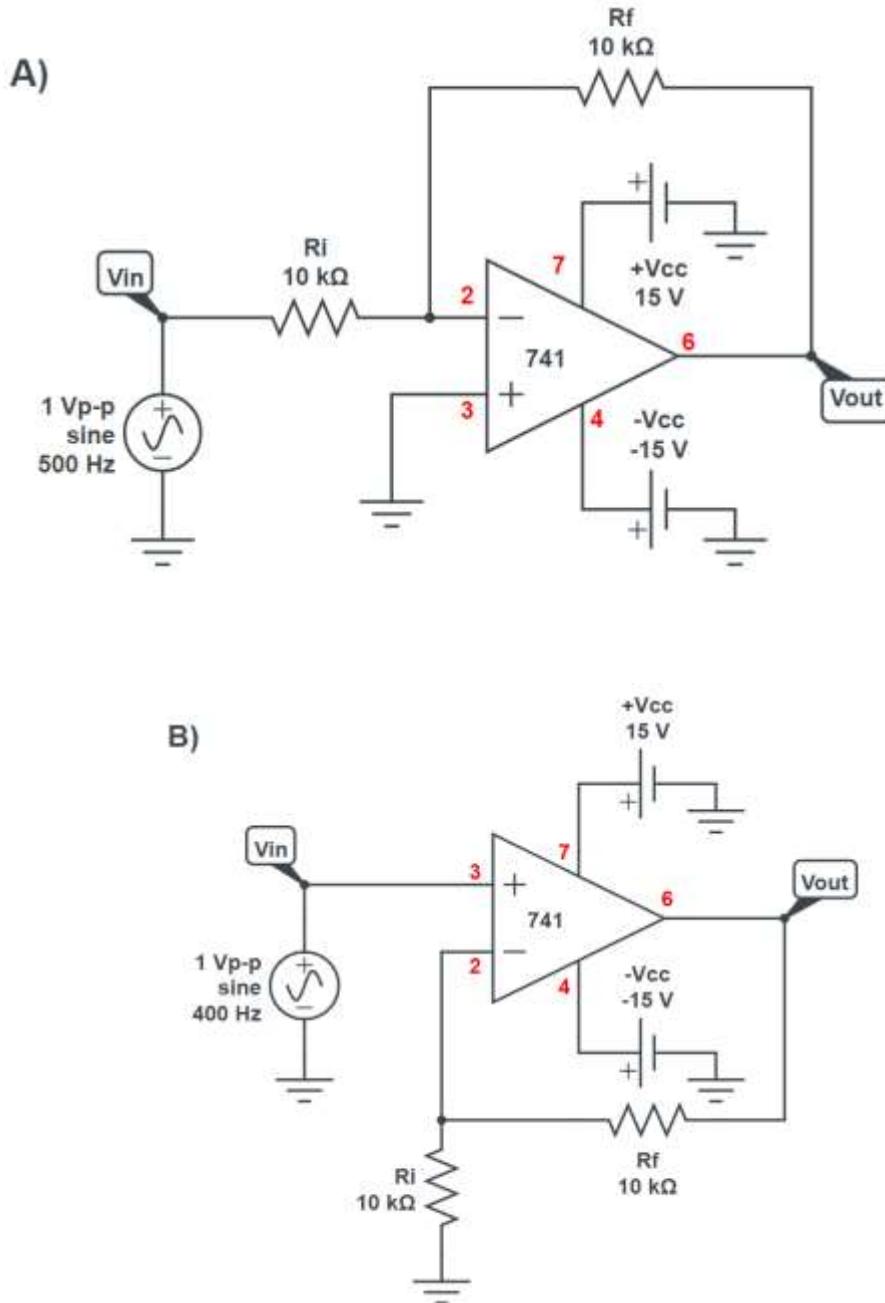


FIGURE 13.1-1: Schematic Diagram of Circuits

*Note the orientation of pins 2 and 3 in Figures 13.1-1 A and B

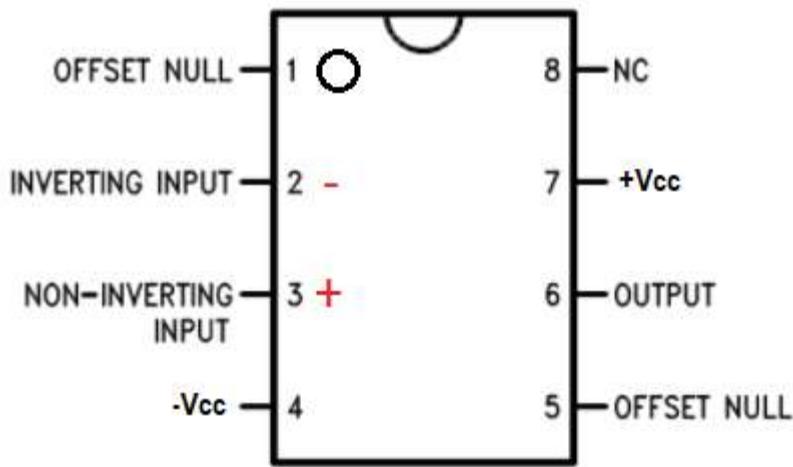


FIGURE 13.1-2: Pin Diagram of 741 Op-Amp

3. Measure the peak-to-peak output voltage (v_{out}), then determine the voltage gain (A_v) and compare it to the expected value. Record the results in Table 13.1-1.

The peak-to-peak output voltage should be the same as the input so that the voltage gain is -1. The negative sign indicates that the output is inverted with respect to the input.

4. Keeping the input signal at 1 V peak-to-peak, change the R_f resistor according to Table 13.1-1, recording the results as in Step 3. Each time, disconnect the power supplies and waveform generator before the resistors are changed. Do the results agree with those obtained from the equation for the inverting amplifier voltage gain (Equation 1)?

As the results of Table 13.1-1 indicate, the voltage gain of an inverting amplifier can be made to be less than, equal to, or greater than unity (1).

5. Now wire the non-inverting amplifier circuit shown in the schematic diagram shown in Figure 13.1-1B. Apply the power to the breadboard and adjust the input voltage to 1 V peak-to-peak and the frequency at 400 Hz. Again, position the input voltage above the output voltage on the scope's display. What is the difference between the two signals?

The only difference is that the output signal is larger than the input signal, as shown in Figure 13.1-4. Both signals are said to be in-phase since the output signal goes positive exactly when the input signal does.

6. Measure the peak-to-peak output voltage (v_{out}). Then determine the voltage gain (A_v) and compare it to the expected value. Record the results in Table 13.1-2.

The peak-to-peak output voltage should be approximately 2 V, so that the voltage gain is 2.

7. Keeping the input signal at 1 V peak-to-peak, change resistor R_f according to Table 13.1-2 and record the results as in Step 6. Be sure to disconnect the power supplies and the waveform

generator each time a resistor is changed. Do the results correlate with those obtained from the equation for the non-inverting amplifier voltage gain (Equation 2)?

As the results of Table 13.1-2 indicate, the voltage gain of a non-inverting amplifier can never be less than or equal to 1. It will always be greater than 1.

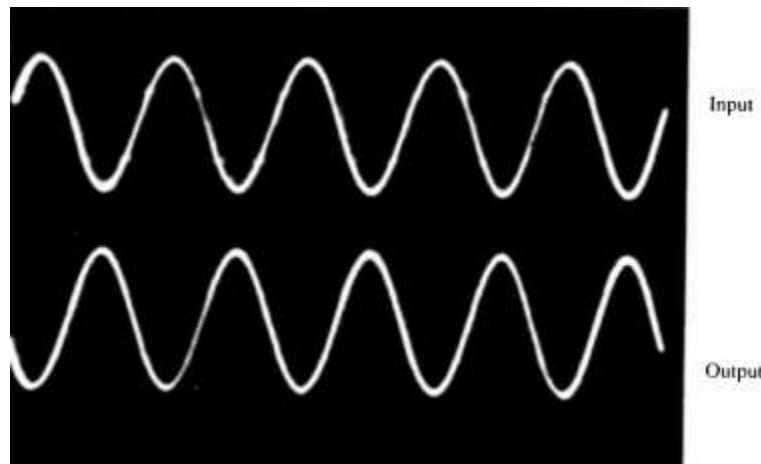


FIGURE 13.1-3

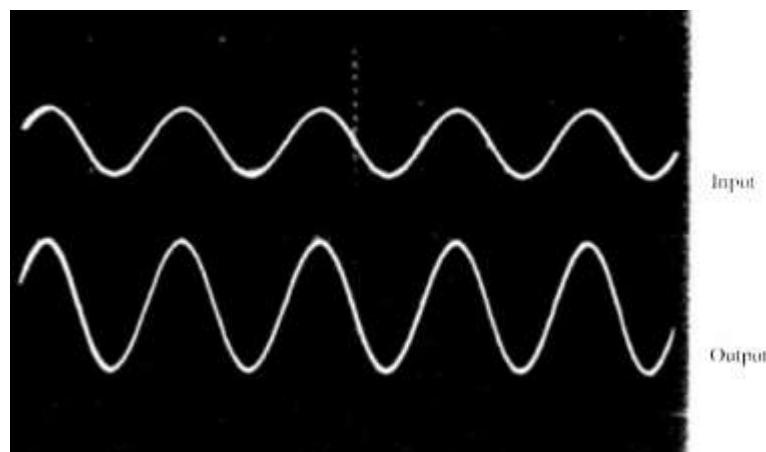


FIGURE 13.1-4

DATA FOR LAB 13.1 – INVERTING AND NON-INVERTING AMPLIFIERS

R_f	Measured v_{out}	Measured Gain	Expected Gain	% Error
$10 \text{ k}\Omega$				
$22 \text{ k}\Omega$				
$47 \text{ k}\Omega$				
$100 \text{ k}\Omega$				
$4.7 \text{ k}\Omega$				
$1 \text{ k}\Omega$				

FIGURE 13.1-1: Inverting Amplifier

R_f	Measured v_{out}	Measured Gain	Expected Gain	% Error
$10 \text{ k}\Omega$				
$22 \text{ k}\Omega$				
$47 \text{ k}\Omega$				
$100 \text{ k}\Omega$				
$4.7 \text{ k}\Omega$				
$1 \text{ k}\Omega$				

FIGURE 13.1-2: Non-Inverting Amplifier

USEFUL FORMULAS

Inverting Amplifier Closed-Loop Voltage Gain

$$1) \ A_v = -\frac{R_f}{R_i} = \frac{v_{out}}{v_{in}}$$

Non-Inverting Amplifier Closed-Loop Voltage Gain

$$2) \ A_v = 1 + \frac{R_f}{R_i} = \frac{v_{out}}{v_{in}}$$

LAB 13.2: OP-AMP COMPARATORS

PURPOSE AND BACKGROUND

The purpose of this experiment is to demonstrate the operation of non-inverting and inverting comparator circuits using a 741 operational amplifier. A comparator determines whether an input voltage is greater or less than a predetermined reference level. Since a comparator operates in an open-loop mode, the output voltage approaches either its positive or its negative supply voltage.

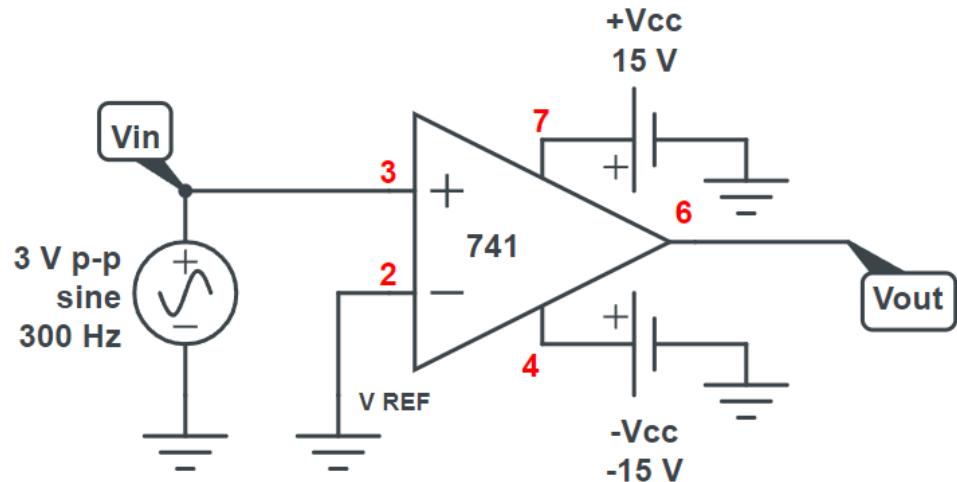
REQUIRED PARTS AND EQUIPMENT

- ❖ Resistors
 - Two 1 kΩ
 - 4.7 kΩ
 - Two 10 kΩ
 - 47 kΩ
 - 100 kΩ
- ❖ 1N914 (or 1N4148) Diode
- ❖ LED
- ❖ 2N3904 NPN Transistor
- ❖ Breadboard
- ❖ 741 Op-Amp (8-pin DIP)
- ❖ 100 kΩ Potentiometer
- ❖ Analog Discovery 2
- ❖ Jumper Wires

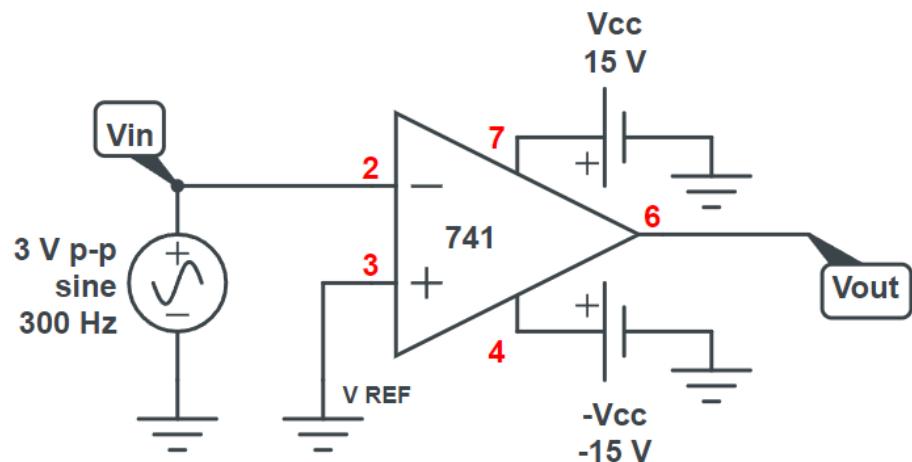
PROCEDURE

1. Wire the circuit shown in the schematic diagram in Figure 13.2-1A.
2. Apply power to the breadboard and adjust the input voltage at 3 V peak-to-peak and set the frequency to 300 Hz. What is the polarity of the output voltage when the input signal goes positive? When the input goes negative?
When the input signal v_{in} is applied to the op-amp's non-inverting input, the output signal's polarity will be the same as that of the input, so that this circuit is a non-inverting comparator. In this case, the reference voltage v_{REF} is zero (the inverting input is grounded). Because of the high open-loop gain of the op-amp, the output immediately goes positive when v_{in} is greater than zero volts (v_{REF}), and vice versa, as shown in Figure 13.2-3. This circuit is also referred to as a non-inverting zero-level, or zero-crossing, detector since it detects the polarity of the input signal.
3. Disconnect the power and signal leads to the breadboard and reverse the input connections to the op-amp so that the input signal is now connected to the inverting input while the non-inverting input is grounded, as shown in Figure 13.2-1B.

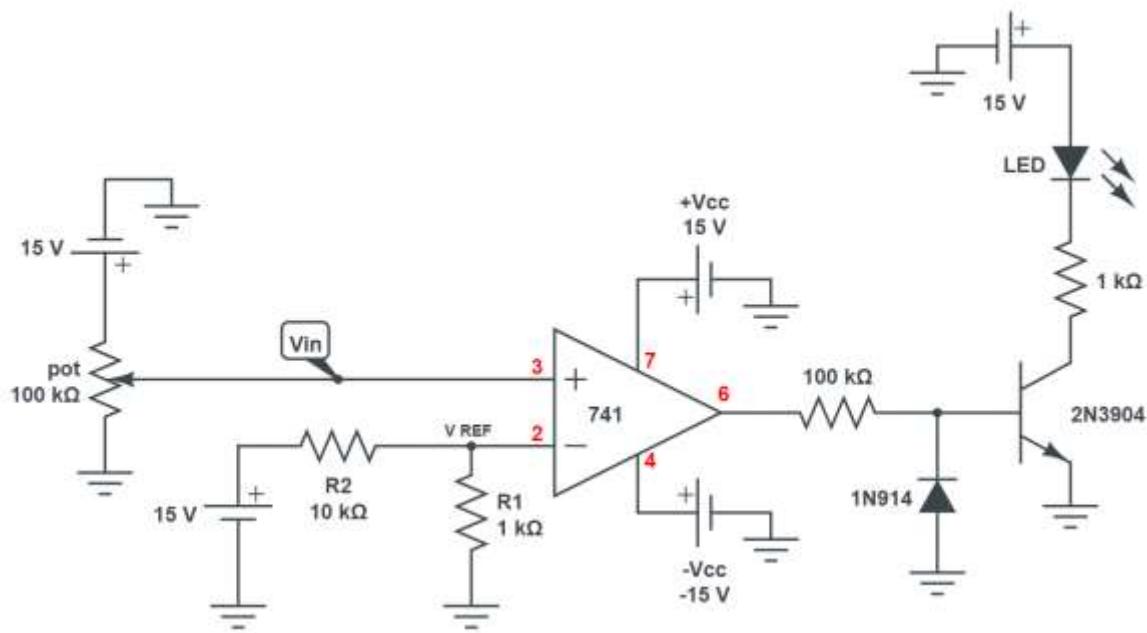
A)



B)



C)



D)

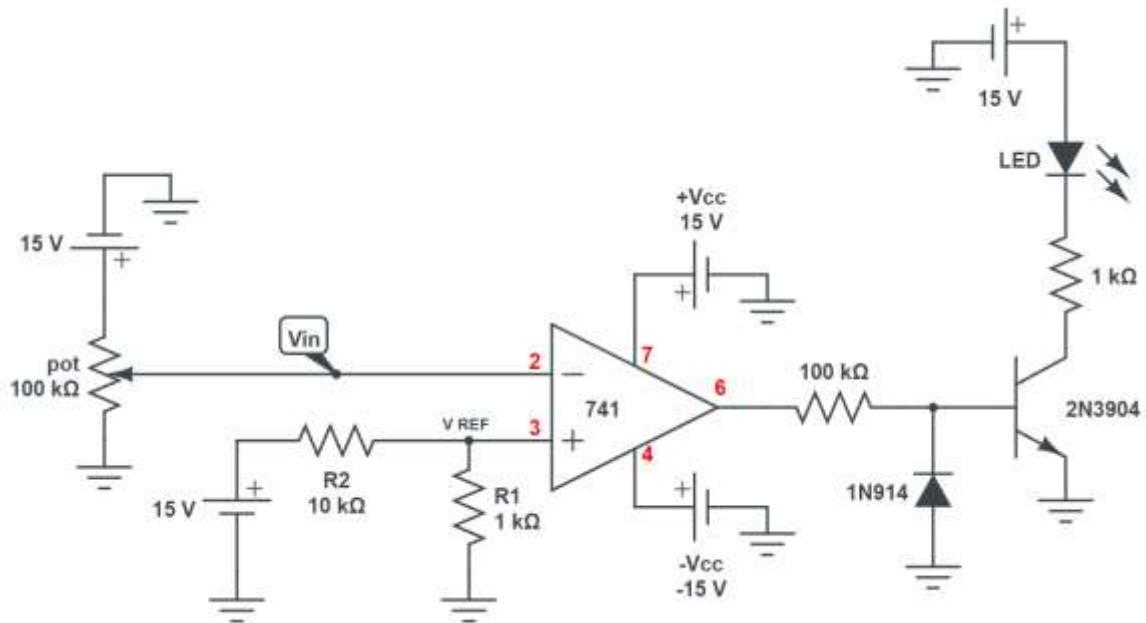


FIGURE 13.2-1: Schematic Diagrams of Circuits (A-D)

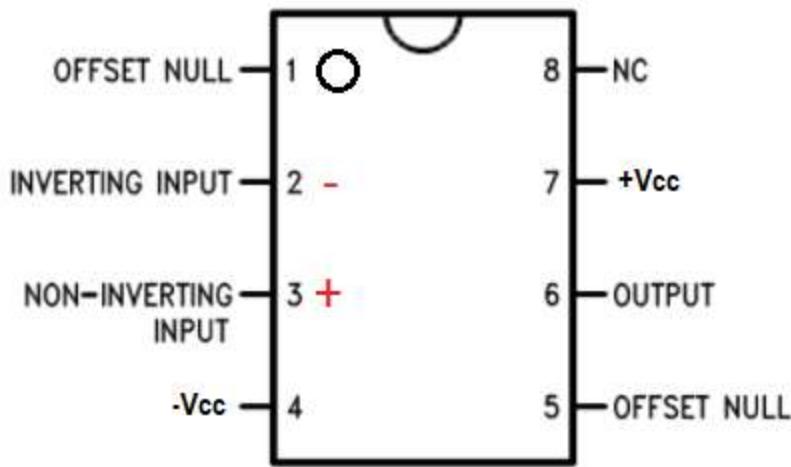


FIGURE 13.2-2: Pin Diagram of 741 Op-Amp

4. Again, apply both the power and signal leads to the breadboard. Now what is the difference between the operation of this circuit and that of the circuit used earlier?

Notice that the output of this comparator circuit has a polarity that is inverted, with respect to the input signal. Such a circuit is called an inverting comparator. Furthermore, since the reference voltage (the voltage at the non-inverting input) is zero, this circuit is also referred to as an inverting zero-level detector. When the polarity of the input signal is positive, the output voltage equals $-V_{SAT}$, and vice versa, as shown in Figure 13.2-4. As can be seen, both circuits are useful in converting sine waves into square waves.

5. Disconnect the power and signal leads from the breadboard and wire the circuit shown in Figure 13.2-1C. Make sure that you have the 1N914 diode and LED, as well as the NPN transistor wired correctly.
6. Apply power to the breadboard. Depending on the current settings of the potentiometer, the LED may or may not be lit when the power is connected. If the LED is off, adjust the potentiometer past the point at which the LED just turns on.
7. With your voltmeter, measure the voltage at the op-amp's inverting terminal (pin 2), which is the reference voltage (V_{REF}) for the comparator, and measure the voltage at the op-amp's non-inverting terminal (pin 3), which is the input voltage (V_{in}), and record the value in Table 13.2-1.
8. Now connect the voltmeter to the op-amp's non-inverting input (pin 3). While watching the LED, vary the potentiometer just until the LED is off. Measure this voltage at pin 3, (v_{in} , LED off), and measure the voltage at the op-amp's inverting terminal (pin 2), which is the reference voltage, and record the results in Table 13.2-1. How does this value compare with the one you determined in Step 7?

These two values should be virtually the same. When the input voltage (v_{in}) at the non-inverting input exceeds the comparator's reference voltage at the inverting input, the op-amp comparator's output switches from its negative saturation voltage to its positive saturation voltage. This circuit is a non-inverting comparator, with a non-zero reference voltage that is set by the 10 kΩ and 1 kΩ resistors connected as a simple voltage divider.

The transistor-LED circuit is connected to the output of the comparator, allows one to determine visually whether the input voltage is greater or less than the reference voltage. When the output voltage is at $+V_{SAT}$, the LED is lit.

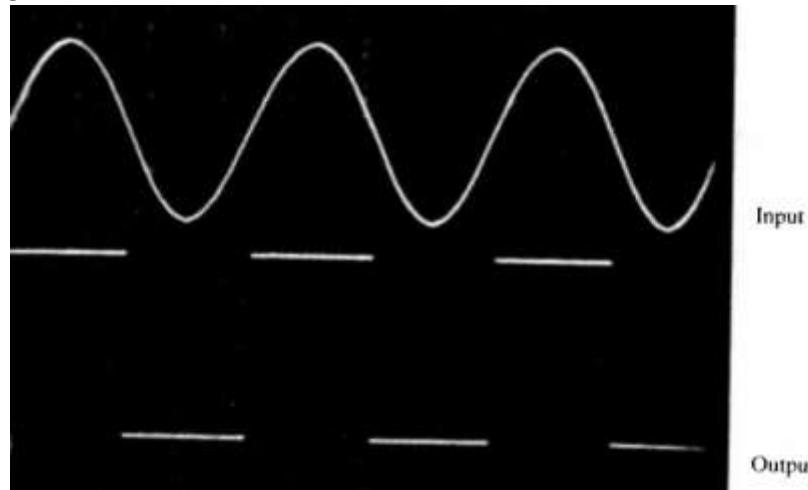


FIGURE 13.2-3

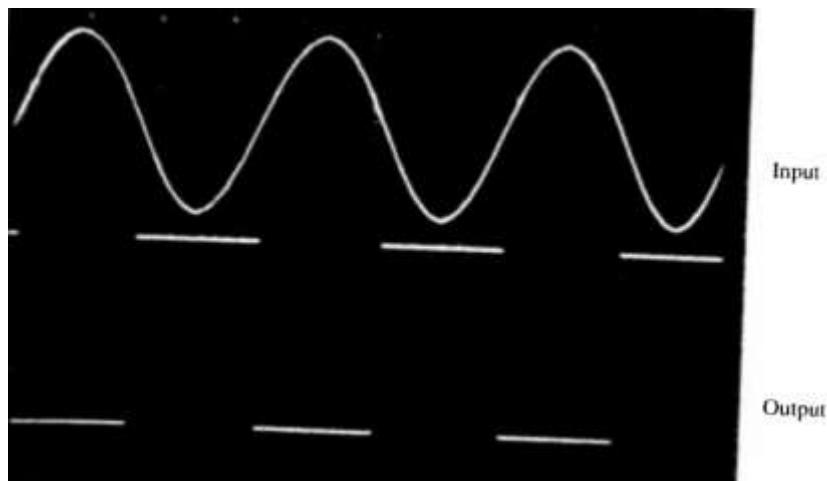


FIGURE 13.2-4

9. Disconnect the power to the breadboard. Verify the operation of the non-inverting comparator by varying the voltage divider resistors, repeating Steps 6, 7 and 8 according to Table 13.2-2.
10. Disconnect the power to the breadboard and reverse the input connections to the op-amp. The output of the potentiometer should be connected to the op-amp's inverting input (pin 2). This is not an inverting comparator. Repeat Steps 6, 7, 8 and 9, keeping in mind that the results should now be the opposite of those in Table 13.2-1. Record the results in Table 13.2-2.

WHAT YOU HAVE DONE

This experiment demonstrated the operation of non-inverting and inverting comparator circuits using a 741 operational amplifier. It showed that the basic comparator determines if an input voltage is greater than a predetermined reference level. Since comparators detect whether the input signal either exceeds or drops below a given voltage level, they are also referred to as level detectors. Comparators operate in

the open-loop mode, and therefore the output voltage always approaches either its positive, or negative supply voltage level.

DATA FOR EXPERIMENT 13.2 – OP-AMP COMPARATORS

R_1	<i>Measured V_{ref} (pin 2)</i>	<i>Measured V_{in} (ON) (pin 3)</i>	V_{out} (pin 6)	<i>LED ON/OFF</i>
1 kΩ				ON
				OFF
10 kΩ				ON
				OFF
47 kΩ				ON
				OFF

TABLE 13.2-1: Non-Inverting Comparator

R_1	<i>Measured V_{ref} (pin 3)</i>	<i>Measured V_{in} (ON) (pin 2)</i>	V_{out} (pin 6)	<i>LED ON/OFF</i>
1 kΩ				ON
				OFF
10 kΩ				ON
				OFF
47 kΩ				ON
				OFF

TABLE 13.2-2: Inverting Comparator

USEFUL FORMULAS

Non-Inverting Comparator

1. $V_{out} = +V_{SAT}$ when $V_{in} > V_{REF}$
2. $V_{out} = -V_{SAT}$ when $V_{in} < V_{REF}$

Inverting Comparator

3. $V_{out} = +V_{SAT}$ when $V_{in} < V_{REF}$
4. $V_{out} = -V_{SAT}$ when $V_{in} > V_{REF}$

POSTLAB ASSIGNMENT (TO BE SUBMITTED WITH LAB REPORT)

- 1) The output signal of a non-inverting amplifier is out-of-phase with its input signal by _____.

- 2) The voltage gain of an inverting amplifier can be _____.
 - a) Less than 1
 - b) Equal to 1
 - c) Greater than 1
 - d) All the above.

- 3) The voltage gain of a non-inverting amplifier can be _____.
 - a) Less than 1
 - b) Equal to 1
 - c) Greater than 1
 - d) All the above

- 4) The reference voltage for a comparator, in Figure 13.2-1A is _____.

- 5) Based on Figure 13.1-1, design an inverting amplifier circuit with a voltage gain of -6, and a non-inverting amplifier circuit with a voltage gain of +8. Create this circuit using the Analog Discovery 2 device.
*Note, Replace $+V_{cc}$ with +5 Volts (pin 7) and $-V_{cc}$ with -5 Volts (pin 4) when using AD2.
**Must include circuit diagram, necessary calculations, and Waveforms application screenshot of input and output signals.

(blank)

Lab 14

Op-Amp Differentiator and Integrator Circuits

LAB 14: OP-AMP DIFFERENTIATOR AND INTEGRATOR

PURPOSE AND BACKGROUND

The purpose of this experiment is to demonstrate the operation of both a differentiator and an integrator using an op-amp. A differentiator is a circuit that calculates the area underneath the curve of a given waveform. Differentiation and integration are paired mathematical operations in that one has the opposite effect of the other. For example, if you integrate a waveform and then differentiate it, you obtain the original waveform.

REQUIRED PARTS

- ❖ Resistors (1/4 W):
 - 22 kΩ
 - Two 10 kΩ
 - 100 kΩ
 - 2.2 kΩ
- ❖ Two 0-15 V DC power supplies
- ❖ 741 Op-Amp (8 pin mini DIP)
- ❖ Function Generator
- ❖ Dual Trace Oscilloscope
- ❖ Breadboard
- ❖ Capacitors:
 - 0.0022 μF (2.2 nF)
 - 0.0047 μF (4.7 nF)

PROCEDURE

1. Wire the inverting amplifier circuit shown in the schematic diagram in Figure 14-1A, and set the oscilloscope for the following approximate settings:
 - Channel 1: 0.5 V/division, DC coupling
 - Channel 2: 0.05 V/division, DC coupling
 - Time Base: 0.5 ms/division
2. Apply the power to the breadboard and adjust the peak-to-peak voltage (v_{in}) of the input triangle wave at 1 V and the frequency at 400 Hz. As depicted in Figure 14-3, the output signal is a square wave that is 180° out-of-phase with the input signal.
3. Temporarily remove the probe connected to Channel 2 of the oscilloscope and adjust the resulting straight line (ground level) at some convenient position on the screen. Reconnect the probe to the output of the differentiator and measure the negative peak voltage (with respect to ground) of the square wave. Record the results in Table 14-1.
4. Now, measure the time duration for which the square wave signal is negative (t_1). The peak voltage of a square that results from differentiating a triangle waveform having a peak voltage v_{in} is given by...

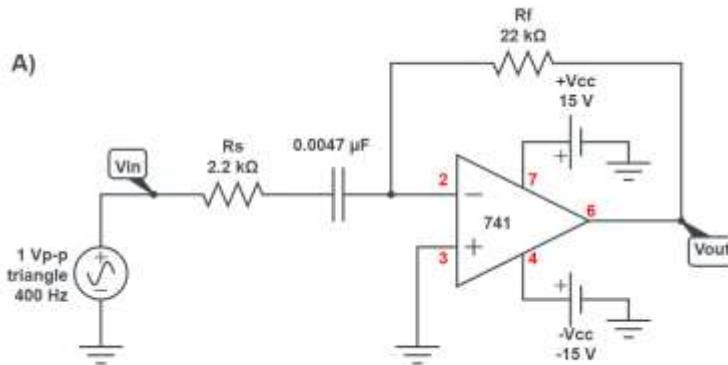
$$V_{out}(\text{peak}) = -\frac{2 \cdot R_F \cdot C \cdot V_{in}(\text{peak})}{t_1}$$

Compute the expected value of the negative peak voltage and compare it with the measured value above. Record the results in Table 14-1.

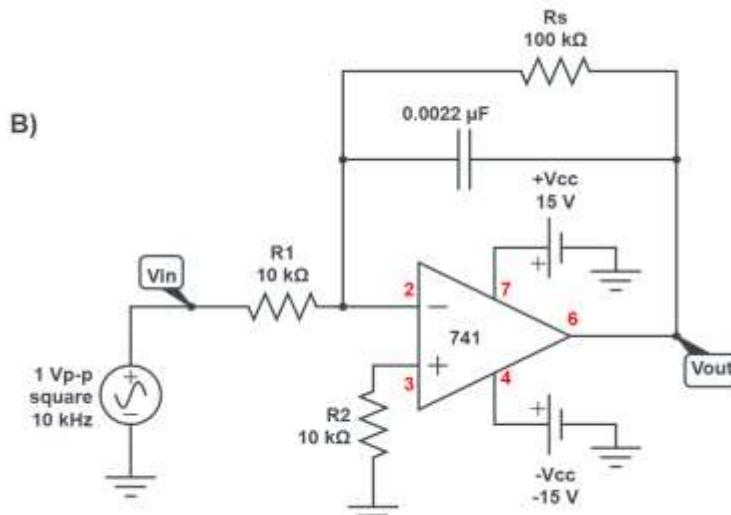
5. Now set change the time base on the oscilloscope to 0.2 ms/division and Channel 2 (at output) to 0.1 V/division. Adjust the input frequency to 1 kHz. Repeat steps 3 and 4. It should be seen that the peak output voltage increases.
6. Change the input frequency to 30 kHz. Adjust the time base to 10 μ s/division and set Channel 2 to 2 V/division.

Notice that the output signal looks like a triangle wave with a 180° phase shift. Explain why in the lab report.

Above approximately 15.4 kHz, the circuit ceases to act as a differentiator since the reactance of the 0.0047 μ F capacitor is now less than that of the 2.2 k Ω resistor (R_s). Above this frequency, the circuit functions like that of an inverting amplifier, having a voltage gain of R_f/R_s .



$$v_{out} = -R_f \cdot C \left(\frac{dv_{in}}{dt} \right)$$



$$v_{out} = -\frac{1}{R_1 \cdot C} \int_0^t v_{in} dt$$

FIGURE 14-1: Schematic Diagram of Circuits

* (for simulation with AD2 device, use +/- 5 Volts for the positive and negative rails of the 741 Op-Amp.)

**Note the schematic depicts sine wave inputs for the supply voltages, but the Triangle and Square waves are being used respectively.

7. Measure the peak-to-peak output voltage and determine the voltage gain, recording the values in Table 14-1. How does the voltage gain compare to that of an inverting amplifier?
8. Wire the integrator circuit shown in the schematic diagram of Figure 14-1B. Set the oscilloscope to the following approximate settings:
 Channel 1: 0.5 V/division
 Channel 2: 0.5 V/division
 Time Base: 20 μ s/division
9. Apply the power to the breadboard and adjust the square wave input to 1 V peak-to-peak and set the frequency to 10 kHz. As shown in Figure 14-4, the output signal is a triangle wave that is 180° out-of-phase with the input signal

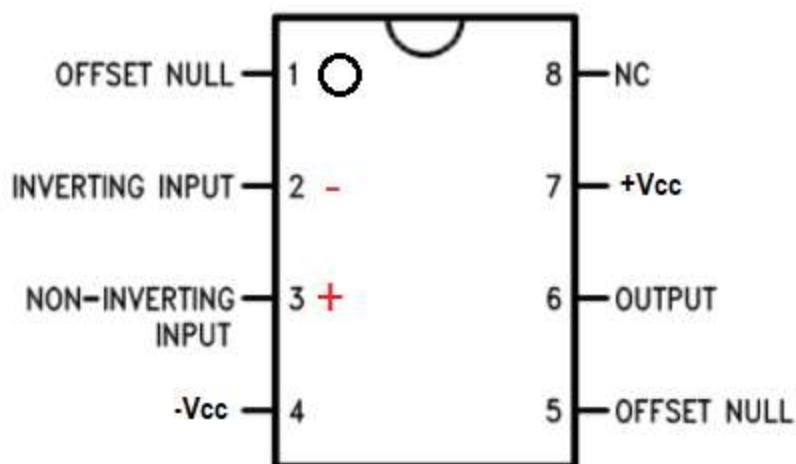


FIGURE 14-2: Pin Diagram of 741 Op-Amp

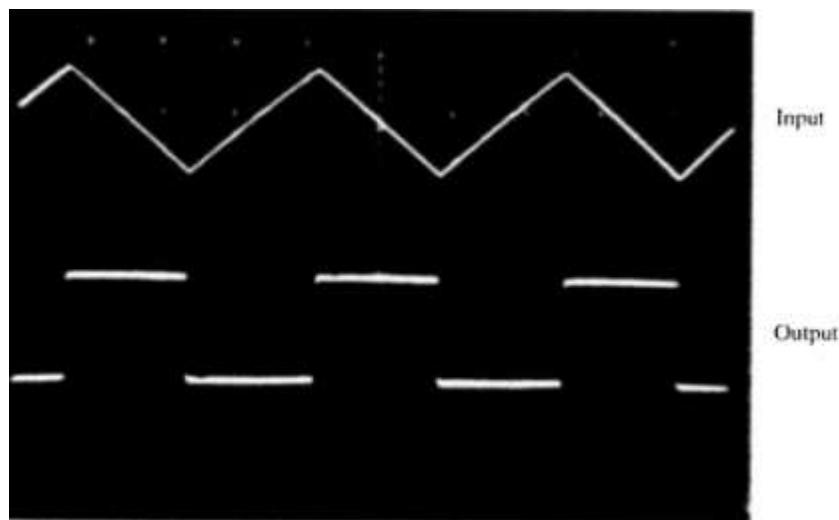


FIGURE 14-3

10. Temporarily remove the probe connected to Channel 2 of the oscilloscope and adjust the resulting straight line (ground level) at some convenient position on the screen. Reconnect the

probe to the output of the integrator and measure the negative peak-to-peak voltage (with respect to ground) of the triangle-wave, recording the results in Table 14-2.

11. Now measure the time duration for which the triangle-wave signal is negative (t_1). The peak voltage of a triangle-wave is that results from integrating a square waveform having a peak voltage V_m is given by...

$$v_{out}(\text{peak}) = -\frac{V_m \cdot t_1}{2 \cdot R_1 \cdot C}$$

12. Change the time base to 50 $\mu\text{s}/\text{division}$ and Channel 2 to 1 V/division. Then adjust the input frequency to 4 kHz. Repeat steps 10 and 11. You should find that the peak output voltage increases.

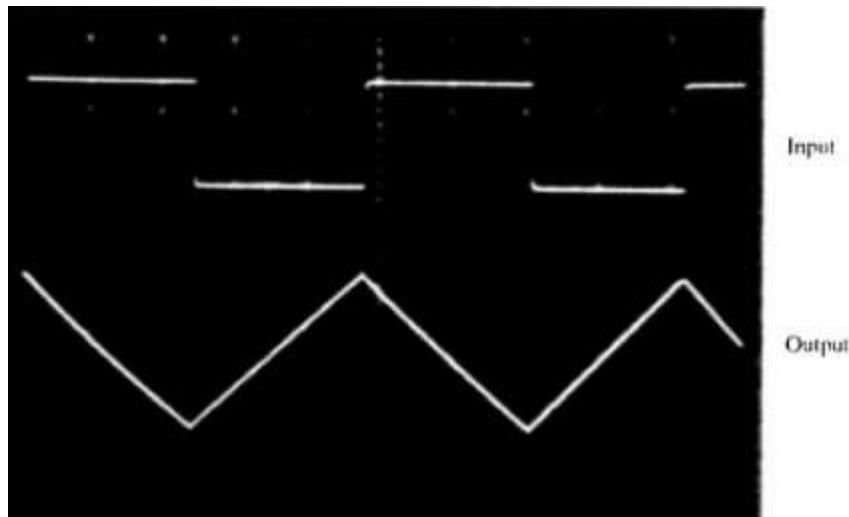


FIGURE 14-4

13. Now change the input frequency to 100 Hz. Adjust the time base to 2 ms/division and Channel 2 to 5 V/division. What does the output signal look like?

Notice that the output signal looks like a square wave with a phase shift of 180°. Why?

Below approximately 724 Hz, the circuit ceases to act as an integrator since the reactance of the 0.0022 μF capacitor is now greater than that of the 100 $\text{k}\Omega$ resistor (R_s). Below this frequency, the circuit functions like that of an integrating amplifier having a voltage gain of R_s/R_1 .

14. Measure the peak-to-peak output voltage and determine the voltage gain, recording the values in Table 14-2. How does the voltage gain compare to that of an inverting amplifier?

FOR FURTHER INVESTIGATION

Repeat this experiment using different component values as follows:

Differentiator: $R_f = 15 \text{ k}\Omega$
 $C = 0.0022 \mu\text{F}$

Integrator: $R_s = 47 \text{ k}\Omega$

$$C = 0.0047 \mu F$$

Compare the performance of the two versions for each circuit.

WHAT YOU HAVE DONE

This experiment demonstrated the operation of the differentiator and integrator using 741 operational amplifiers. The differentiator is a circuit that calculates the instantaneous slope of the line at every point on a waveform. On the other hand, the integrator generates a signal that is proportional to the accumulative “area under the curve” of a given waveform. Besides these mathematical operations, differentiators and integrators are often used as signal processing circuits because of their ability to change the shapes of the input signals. Further information on the 741 operational amplifiers can be found in the included data sheet.

DATA FOR EXPERIMENT 14 – OP-AMP DIFFERENTIATOR AND INTEGRATOR

<i>Input Frequency</i>	t_1	<i>Measured Peak Output</i>	<i>Expected Peak Output</i>	<i>% Error</i>
400 Hz				
1 kHz				
30 kHz				

TABLE 14-1

<i>Input Frequency</i>	t_1	<i>Measured Peak Output</i>	<i>Expected Peak Output</i>	<i>% Error</i>
10 kHz				
4 kHz				
100 Hz				

TABLE 14-2

USEFUL FORMULAS

DIFFERENTIATOR

Output Voltage

$$(1) \quad v_{out} = -R_f \cdot C \left(\frac{dv_{in}}{dt} \right)$$

Differentiator Low-Frequency Response

$$(2) \quad f_c = \frac{1}{2\pi R_s C}$$

...when $f_{in} < f_c$, the circuit acts as a differentiator.

...when $f_{in} > f_c$, the circuit approaches an inverting amplifier with a voltage gain of $-\frac{R_f}{R_s}$.

INTEGRATOR

Output Voltage

$$(3) \quad v_{out} = -\frac{1}{R_1 \cdot C} \int_0^1 v_{in} dt$$

$$(4) \quad f_c = \frac{1}{2\pi R_s C}$$

...when $f_{in} > f_c$, the circuit acts as an integrator.

...when $f_{in} < f_c$, the circuit approaches an inverting amplifier with a voltage gain of $\frac{R_s}{R_1}$.

For minimum output offset due to operational amplifier input bias currents:

$$(5) \quad R_2 = \frac{R_1 R_s}{R_1 + R_s}$$

POSTLAB ASSIGNMENT (TO BE SUBMITTED WITH LAB REPORT)

- (1) Define integrator and differentiator.
- (2) What are the corner-frequency responses (f_c) of the Op-Amp differentiator and integrator circuit in Figure 14-1A and 14-1B?
- (3) How does the circuit shown in Figure 14-1A work when the input frequency is greater than f_c ?
 - a) Differentiator
 - b) Integrator
 - c) Inverting Amplifier
 - d) Non-Inverting Amplifier
- (4) How does the circuit shown in Figure 14-1B work when the input frequency is less than f_c ?
 - a) Differentiator
 - b) Integrator
 - c) Inverting Amplifier
 - d) Non-Inverting Amplifier
- (5) Design an Op-Amp differentiator circuit with a corner frequency of approximately 3.3 kHz. Answers must include calculations, circuit diagram, and Waveforms application screenshots of input and output signals. Change the input from 1 V peak-to-peak @ 400 Hz to 1 V peak-to-peak @ 5 kHz. Record the measured peak output voltages for both input values.

(blank)

Lab 15

Butterworth 2nd Order Low-Pass Active Filter

LAB 15: THE BUTTERWORTH 2ND-ORDER LOW-PASS ACTIVE FILTER

PURPOSE AND BACKGROUND

The purpose of this experiment is to demonstrate the operation and characteristics of a Butterworth Sallen and Key 2nd-order low pass active filter. A Butterworth low-pass filter passes all signals with the frequencies below its cutoff frequency with, a virtually constant, or *maximum flat*, passband gain. The cutoff frequency is also referred to as the *critical, corner, or break* or *3-dB frequency*. Above this frequency, the input signal is attenuated at a rate of -12 dB/octave, a rate that is equivalent to -40 dB/decade for such a 2nd-order filter. Because of the component values used in this experiment, the passband gain is ideally fixed at 1.568 (4 dB), although other arrangements allowing other, higher passband gains are possible. In addition, for input frequencies well below the cutoff frequency, there is no phase shift between the input and the output signals.

PRELAB ASSIGNMENT (MUST BE SUBMITTED ONE DAY PRIOR TO CLASS)

Please simulate the circuit shown in Figure 15-1 in PSpice. Include both the input and output waveforms in the per-lab report. Calculate the cutoff frequency and calculate the expected values of Table 15-1.

REQUIRED PARTS AND EQUIPMENT

- ❖ Resistors (1/4 W):
 - Two 6.8 kΩ
 - 27 kΩ
 - 47 kΩ
- ❖ Two 0-15 V_{DC} Power Supplies
- ❖ 741 Op-Amp (8-pin mini-DIP)
- ❖ Signal Generator
- ❖ Dual Trace Oscilloscope
- ❖ Breadboard
- ❖ Two 0.0033 μF (3.3 nF) Capacitors

PROCEDURE

1. Wire the circuit depicted in Figure 15-1.
2. Apply power to the breadboard and adjust the input signal voltage to 5 V peak-to-peak at a frequency of 100 Hz. You should make this voltage setting as accurate as possible.
3. With the resistor and capacitor values used in this circuit, what do you expect the cutoff voltage to be?

From the formula for cutoff, the cutoff frequency is approximately 710 Hz.

4. With the input frequency set at 100 Hz, what is the peak-to-peak output voltage?

You should find that the output voltage is larger than the input. You should also observe that both the input and output signals are essentially in-phase.

5. Now vary the generator frequency (f_{in}), keeping the input voltage at a constant 5 V peak-to-peak to complete the required data in Table 15-1. At the higher frequencies, you may have to increase the input voltage (example: 10 V peak-to-peak) to obtain a measurable output level.

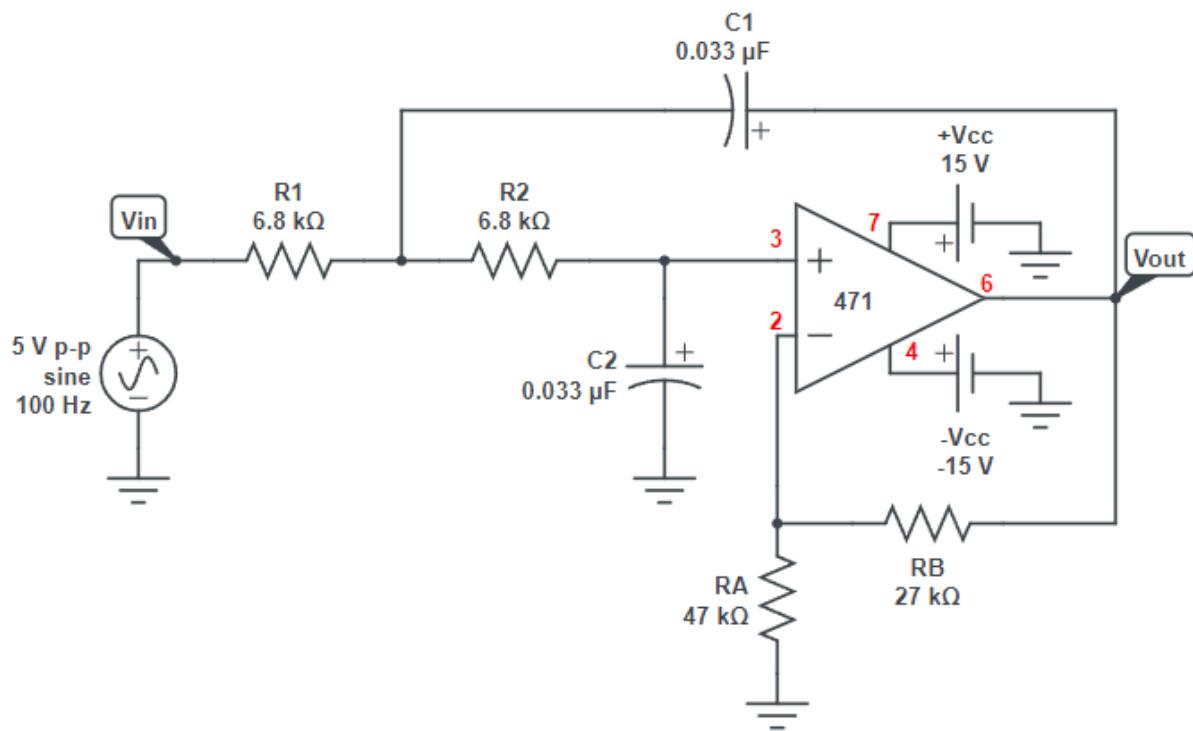


FIGURE 15-1: Schematic Diagram of Circuit

*For simulating circuit with AD2 device, use +/- 5 Volts for the positive and negative voltage rails of the 741 Op-Amp.

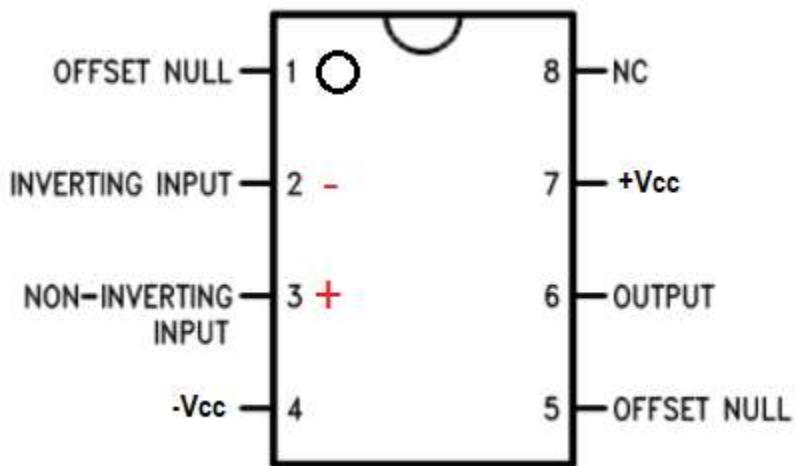


FIGURE 15-2: Pin Diagram of 741 Op-Amp

Using the dB frequency response formula (Equation 5), calculate the expected dB response using a cutoff frequency of 710 kHz. Then plot both, experimental and expected results on dB-frequency graph (plot graphs as a part of post lab assignment).

6. From your plotted results, you should find that both response curves are parallel. How closely are they parallel will depend on how close the actual resistor and capacitor values are to the values shown in the schematic diagram.
7. Notice that the filter's gain at low frequency is essentially constant up to some point (that is the *passband*), after which it decreases at a linear rate with increasing input frequency. This linear decrease in gain as a function of frequency is termed as the *rolloff*. To determine the rolloff of your filter, you must determine the slope of a line. Using the data in Table 15-1, subtract the decibel gain measured at 1 kHz from that measured at 10 kHz. The frequency difference from 1 kHz to 10 kHz is *one decade* (that is, a factor of 10). Consequently, the rolloff is the difference in the decibel gain over a one-decade frequency range. From your measurements, determine the filter's rolloff. How does it compare with what you should expect for a Butterworth 2nd order low-pass filter? Record your result in Table 15-2.
8. The rolloff can also be measured in terms of an *octave* or doubling in frequency. In this case, determine the filter's rolloff for the octave from 2 kHz to 4kHz. Record the results in Table 15-2.

You should find that the low-pass filter's rolloff frequency is nearly -40 dB/decade, or -12 dB/octave.
9. The filter's cutoff frequency is the frequency at which the dB frequency response is 3 dB *less* than the dB passband gain. This value is equivalent to an output voltage that is 0.707 times the input voltage of the filter. From your graph, estimate the filter's cutoff frequency and compare it with the value calculated in Step 3.

You should have estimated a critical frequency of approximately 710 Hz. In this case, the passband gain is 1.586 or 4 dB, so the critical frequency occurs when the filter's dB response is 4 dB – 3 dB, or +1 dB.

FOR FURTHER INVESTIGATION

Select a different cutoff frequency by changing both R_1 and R_2 and or both C_1 and C_2 . This should be kept below 5 kHz.

DATA FOR EXPERIMENT – THE BUTTERWORTH 2ND-ORDER LOW-PASS ACTIVE FILTER

<i>Input Frequency (Hz)</i>	V_{in}	V_{out}	<i>Measured Gain (V_{out}/V_{in})</i>	<i>Experimental dB Gain</i>	<i>Expected dB Gain</i>
100					
200					
300					
400					
500					
550					
600					
650					
700					
710					
750					
800					
900					
1000					
2000					
3000					
4000					
5000					
6000					
7000					
8000					
9000					
10000					

TABLE 15-1: Frequency Response Data

<i>Input Frequency</i>	<i>Experimental dB Response</i>	<i>2nd-Order Rolloff</i>
1 kHz		
10 kHz		<i>dB/decade</i>
2 kHz		
4 kHz		<i>dB/octave</i>

TABLE 15-2: 2nd-Order Rolloff

USEFUL FORMULAS

$$1) \quad R_1 = R_2 \quad \text{and} \quad C_1 = C_2$$

$$2) \quad R_B = 0.586 \cdot R_1$$

Cutoff Frequency

$$3) \quad f_c = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_1}$$

dB Frequency Response

$$4) \quad A_{dB} = 20 \cdot \log \left(\frac{v_{out}}{v_{in}} \right)$$

$$5) \quad A_{dB} = 20 \cdot \log \left\{ \frac{1.586}{\sqrt{1 + \left(\frac{f_{in}}{f_c} \right)^4}} \right\}$$

POST LAB ASSIGNMENT (TO BE SUBMITTED WITH LAB REPORT)

Please complete the next lab, Lab 16, and create the Bode Plot for the input frequency vs. experimental dB gain and input frequency vs. expected dB gain from Table 16-1.

Lab 16

Butterworth 2nd Order High-Pass Active Filter

LAB 16: THE BUTTERWORTH 2ND-ORDER HIGH-PASS ACTIVE FILTER

PURPOSE AND BACKGROUND

The purpose of this experiment is to demonstrate the operation and characteristics of a Butterworth Sallen and Key 2nd-order high-pass active filter. A Butterworth high-pass filter has an operation that is opposite that of a low-pass filter. That is a high-pass filter passes all signals with frequencies above its cutoff frequency with, virtually a constant, or *maximally flat*, passband gain. Below this frequency, the input signal is attenuated at a rate of 12 dB/octave, a rate that is equivalent to 40 dB/decade for such a 2nd-order filter. Because of the component values used in this experiment, the passband voltage gain is ideally fixed at 1.586 (4 dB), although other arrangements allowing other, higher passband gains are possible. In addition, frequencies well below the cutoff frequency, there is no phase shift between input and output signals.

REQUIRED PARTS AND EQUIPMENT

- ❖ Resistors (1/4 W):
 - Two 6.8 kΩ
 - 27 kΩ
 - 47 kΩ
- ❖ Two 0.0047 μF (4.7 nF) Capacitors
- ❖ 741 Op-Amp (8-pin mini-DIP)
- ❖ Analog Discovery 2 / Waveforms Application
- ❖ Jumper Wires
- ❖ Breadboard

PRELAB ASSIGNMENT (TO BE SUBMITTED ONE DAY PRIOR TO CLASS)

Please use PSpice to simulate the circuit in Figure 16-1. Include both input and output waveforms in the prelab report. Calculate the cutoff frequency. Also, calculate the expected values of Table 16-1.

PROCEDURE

1. Wire the circuit shown in the schematic diagram in Figure 16-1.
2. Apply power to the breadboard and adjust the input signal voltage to 5 V peak-to-peak at the frequency of 10 kHz. You should make this voltage setting as accurate as possible.
3. With a resistor and capacitor values used in the circuit, what do you expect the cutoff frequency to be?

From the formula for the cutoff frequency, the cutoff frequency is approximately 5 kHz.

4. With the input frequency set to 10 kHz, what is the peak-to-peak output voltage?

You should find that the output voltage is larger than the input. You should also observe that both the input and output signals are essentially in-phase.

5. Now vary the generators frequency (f_{in}), keeping the input voltage constant at 5 V peak-to-peak to complete the required data in Table 16-1. You may have to increase the input voltage (e.g., 10 V peak-to-peak) at the lower frequencies to obtain a measurable output level. Using the dB frequency response formula (Equation 5), calculate the expected dB response using a cutoff

frequency of 5 kHz. Plot both, expected and the experimentally found results in a graph and attach this graph to your report.

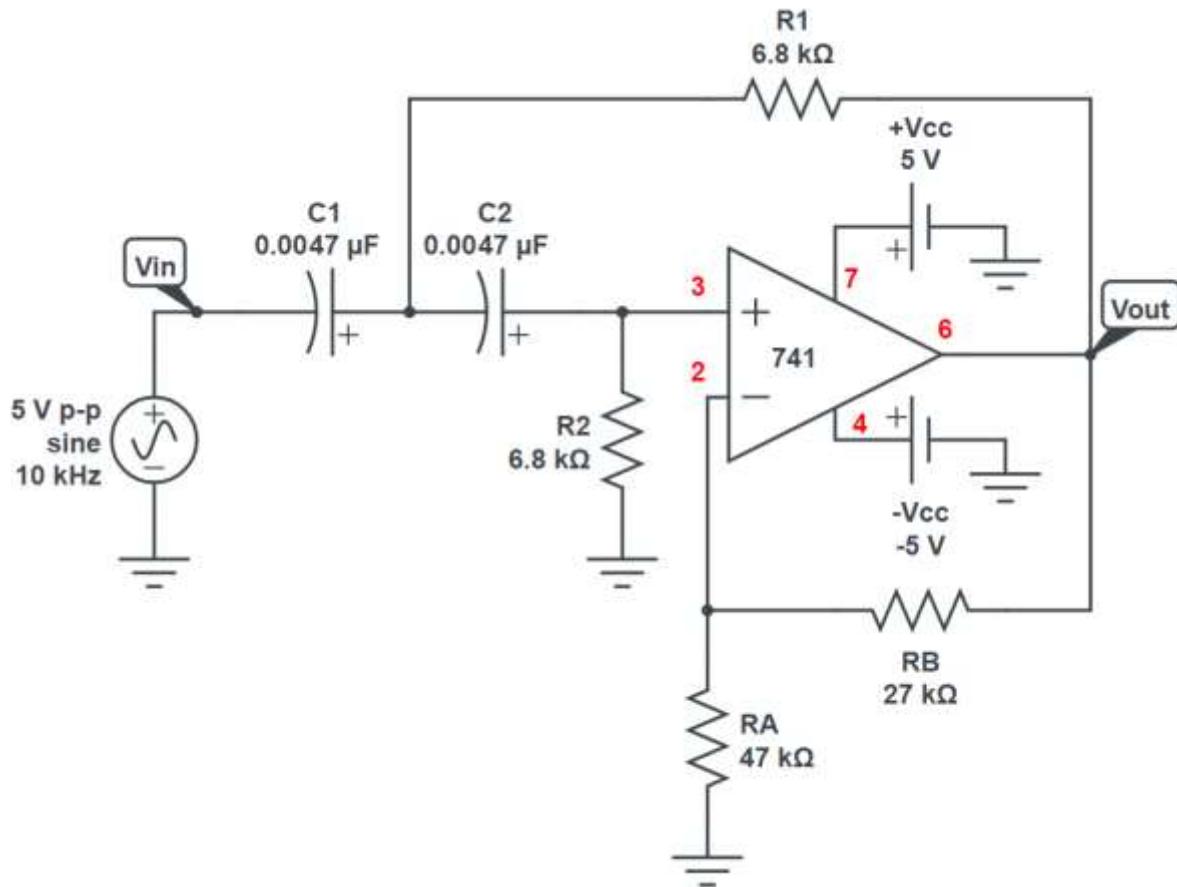


FIGURE 16-1: Schematic Diagram of Circuit

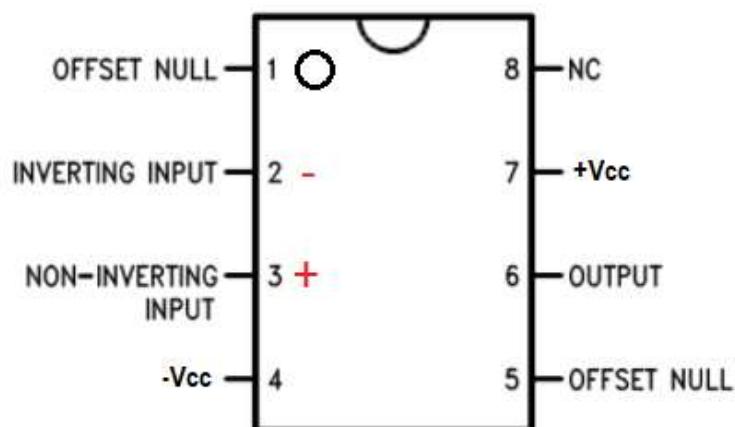


FIGURE 16-2: Pin Diagram of 741 Op-Amp

6. From your plotted results, you should find that both response curves are parallel. How closely they are parallel will depend on how close the actual resistor and capacitor values are to the values shown in the schematic diagram.
7. Notice that the filter's gain at high frequencies is essentially constant up to some point (that is, the *passband*), after which it increases at a linear rate with increasing input frequency. This linear decrease in gain as a function of frequency is termed the *rolloff*. To determine the rolloff of your filter, you must determine the slope of a line. Using the data in Table 16-1, subtract the decibel gain measured at 100 Hz from that measured at 1 kHz. The frequency difference from 100 Hz to 1 kHz is one *decade* (that is, a factor of 10). Consequently, the rolloff is the difference in the decibel gain or a one-decade frequency range. From your measurements, determine the filter's rolloff. How does it compare with what you should expect for a Butterworth 2nd-order low-pass filter? Record your result in Table 16-2.

You should find that the low-pass filter's rolloff is nearly 40 dB/decade, or 12 dB/octave.

8. The rolloff can also be measured in terms of an *octave*, or a doubling in frequency. In this case, determine the filter's rolloff for the octave from 200 Hz to 400 Hz, recording your result in Table 16-2.
9. The filter's cutoff frequency is the frequency at which the dB frequency response is 3 dB *less* than the dB passband gain. This value is equivalent to an output voltage that is 0.707 times the input voltage of the filter. From your graph, estimate the filter's cutoff frequency and compare it with the value calculated in Step 4.

You should have estimated a critical frequency of approximately 5 kHz. In this case, the ideal passband gain is 1.586 or 4 dB, so the critical frequency occurs when the filter's dB response is 4 dB – 3 dB, or + 1 dB.

FOR FURTHER INVESTIGATION

Select a different cutoff frequency in a range of 5 kHz to 10 kHz by changing both R_1 and R_2 and/or both C_1 and C_2 .

DATA FOR EXPERIMENT

<i>Input Frequency (Hz)</i>	<i>V_{in}</i>	<i>V_{out}</i>	<i>Measured Gain (V_{out}/V_{in})</i>	<i>Experimental dB Gain</i>	<i>Expected dB Gain</i>
100					
200					
300					
400					
500					
600					
700					
800					
900					
1,000					
2,000					
3,000					
4,000					
4,500					
5,000					
5,500					
6,000					
7,000					
8,000					
9,000					
10,000					

TABLE 16-1: Frequency Response Data

<i>Input Frequency</i>	<i>Experimental dB Response</i>	<i>2nd-Order Rolloff</i>
100 Hz		
1 kHz		<i>dB/decade</i>
200 Hz		
400 Hz		<i>dB/octave</i>

TABLE 16-2: 2nd-Order Rolloff

USEFUL FORMULAS

$$6) \quad R_1 = R_2 \quad \text{and} \quad C_1 = C_2$$

$$7) \quad R_B = 0.586 \cdot R_1$$

Cutoff Frequency

$$8) \quad f_c = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_1}$$

dB Frequency Response

$$9) \quad A_{dB} = 20 \cdot \log \left(\frac{v_{out}}{v_{in}} \right)$$

$$10) \quad A_{dB} = 20 \cdot \log \left\{ \sqrt{\frac{1.586}{1 + \left(\frac{f_c}{f_{in}} \right)^4}} \right\}$$

LM741 Operational Amplifier

1 Features

- Overload Protection on the Input and Output
- No Latch-Up When the Common-Mode Range is Exceeded

2 Applications

- Comparators
- Multivibrators
- DC Amplifiers
- Summing Amplifiers
- Integrator or Differentiators
- Active Filters

3 Description

The LM741 series are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439, and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common-mode range is exceeded, as well as freedom from oscillations.

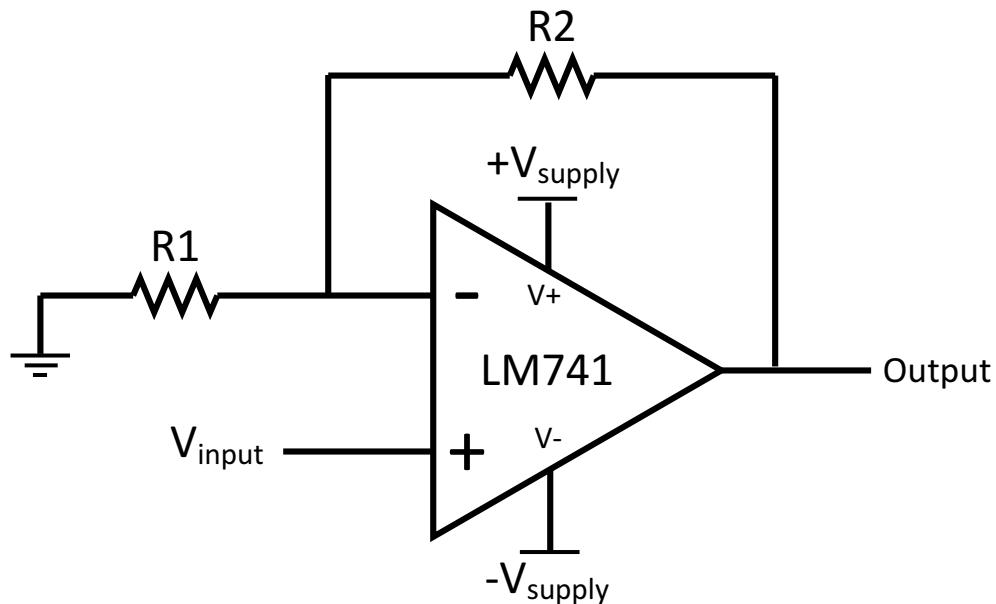
The LM741C is identical to the LM741 and LM741A except that the LM741C has their performance ensured over a 0°C to +70°C temperature range, instead of -55°C to +125°C.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM741	TO-99 (8)	9.08 mm × 9.08 mm
	CDIP (8)	10.16 mm × 6.502 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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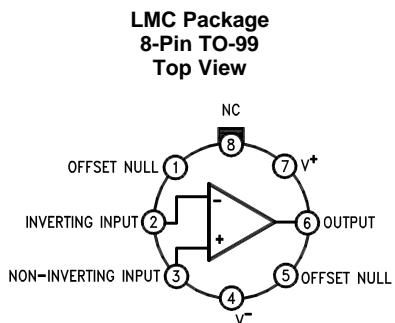
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

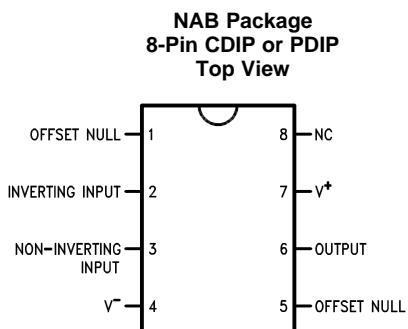
Changes from Revision C (October 2004) to Revision D	Page
• Added <i>Applications</i> section, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Removed NAD 10-Pin CLGA pinout	3
• Removed obselete M (S0-8) package from the data sheet	4
• Added recommended operating supply voltage spec	4
• Added recommended operating temperature spec	4

Changes from Revision C (March 2013) to Revision D	Page
• Added <i>Applications</i> section, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Removed NAD 10-Pin CLGA pinout	3
• Removed obselete M (S0-8) package from the data sheet	4
• Added recommended operating supply voltage spec	4
• Added recommended operating temperature spec	4

5 Pin Configuration and Functions



LM741H is available per JM38510/10101



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INVERTING INPUT	2	I	Inverting signal input
NC	8	N/A	No Connect, should be left floating
NONINVERTING INPUT	3	I	Noninverting signal input
OFFSET NULL	1, 5	I	Offset null pin used to eliminate the offset voltage and balance the input voltages.
OFFSET NULL			
OUTPUT	6	O	Amplified signal output
V+	7	I	Positive supply voltage
V-	4	I	Negative supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

		MIN	MAX	UNIT
Supply voltage	LM741, LM741A		±22	V
	LM741C		±18	
Power dissipation ⁽⁴⁾		500		mW
Differential input voltage		±30		V
Input voltage ⁽⁵⁾		±15		V
Output short circuit duration		Continuous		
Operating temperature	LM741, LM741A	-50	125	°C
	LM741C	0	70	
Junction temperature	LM741, LM741A		150	°C
	LM741C		100	
Soldering information	PDIP package (10 seconds)		260	°C
	CDIP or TO-99 package (10 seconds)		300	
Storage temperature, T _{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) For military specifications see RETS741X for LM741 and RETS741AX for LM741A.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (4) For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). T_j = T_A + (θ_{JA} P_D).
- (5) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±400

- (1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage (VDD-GND)	LM741, LM741A	±10	±15	±22	V
	LM741C	±10	±15	±18	
Temperature	LM741, LM741A	-55		125	°C
	LM741C	0		70	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LM741			UNIT
	LMC (TO-99)	NAB (CDIP)	P (PDIP)	
	8 PINS	8 PINS	8 PINS	
R _{θJA} Junction-to-ambient thermal resistance	170	100	100	°C/W
R _{θJC(top)} Junction-to-case (top) thermal resistance	25	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics, LM741⁽¹⁾

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \leq 10 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$		1	5	mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$			6	mV
Input offset voltage adjustment range	$T_A = 25^\circ\text{C}, V_S = \pm 20 \text{ V}$		± 15			mV
Input offset current		$T_A = 25^\circ\text{C}$		20	200	nA
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		85	500	
Input bias current		$T_A = 25^\circ\text{C}$		80	500	nA
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$			1.5	μA
Input resistance	$T_A = 25^\circ\text{C}, V_S = \pm 20 \text{ V}$		0.3	2		$\text{M}\Omega$
Input voltage range	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		± 12	± 13		V
Large signal voltage gain	$V_S = \pm 15 \text{ V}, V_O = \pm 10 \text{ V}, R_L \geq 2 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	50	200		V/mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	25			
Output voltage swing	$V_S = \pm 15 \text{ V}$	$R_L \geq 10 \text{ k}\Omega$	± 12	± 14		V
		$R_L \geq 2 \text{ k}\Omega$	± 10	± 13		
Output short circuit current	$T_A = 25^\circ\text{C}$			25		mA
Common-mode rejection ratio	$R_S \leq 10 \Omega, V_{CM} = \pm 12 \text{ V}, T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		80	95		dB
Supply voltage rejection ratio	$V_S = \pm 20 \text{ V} \text{ to } V_S = \pm 5 \text{ V}, R_S \leq 10 \Omega, T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		86	96		dB
Transient response	Rise time Overshoot	$T_A = 25^\circ\text{C}$, unity gain		0.3		μs
				5%		
Slew rate	$T_A = 25^\circ\text{C}$, unity gain			0.5		$\text{V}/\mu\text{s}$
Supply current	$T_A = 25^\circ\text{C}$			1.7	2.8	mA
Power consumption	$V_S = \pm 15 \text{ V}$	$T_A = 25^\circ\text{C}$		50	85	mW
		$T_A = T_{A\text{MIN}}$		60	100	
		$T_A = T_{A\text{MAX}}$		45	75	

(1) Unless otherwise specified, these specifications apply for $V_S = \pm 15 \text{ V}, -55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$.

6.6 Electrical Characteristics, LM741A⁽¹⁾

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \leq 50 \Omega$	$T_A = 25^\circ\text{C}$		0.8	3	mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$			4	mV
Average input offset voltage drift					15	$\mu\text{V}/^\circ\text{C}$
Input offset voltage adjustment range	$T_A = 25^\circ\text{C}, V_S = \pm 20 \text{ V}$		± 10			mV
Input offset current		$T_A = 25^\circ\text{C}$		3	30	nA
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$			70	
Average input offset current drift					0.5	$\text{nA}/^\circ\text{C}$
Input bias current		$T_A = 25^\circ\text{C}$		30	80	nA
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$			0.21	μA
Input resistance		$T_A = 25^\circ\text{C}, V_S = \pm 20 \text{ V}$		1	6	$\text{M}\Omega$
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}, V_S = \pm 20 \text{ V}$		0.5		
Large signal voltage gain	$V_S = \pm 20 \text{ V}, V_O = \pm 15 \text{ V}, R_L \geq 2 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	50			V/mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	32			
		$V_S = \pm 5 \text{ V}, V_O = \pm 2 \text{ V}, R_L \geq 2 \text{ k}\Omega, T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	10			

(1) Unless otherwise specified, these specifications apply for $V_S = \pm 15 \text{ V}, -55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$.

Electrical Characteristics, LM741A⁽¹⁾ (continued)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT		
Output voltage swing	$V_S = \pm 20 \text{ V}$	$R_L \geq 10 \text{ k}\Omega$	± 16		± 15	V		
		$R_L \geq 2 \text{ k}\Omega$	± 15					
Output short circuit current	$T_A = 25^\circ\text{C}$		10	25	35	mA		
	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		10	40				
Common-mode rejection ratio	$R_S \leq 50 \Omega$, $V_{CM} = \pm 12 \text{ V}$, $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		80	95	dB			
Supply voltage rejection ratio	$V_S = \pm 20 \text{ V}$ to $V_S = \pm 5 \text{ V}$, $R_S \leq 50 \Omega$, $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		86	96	dB			
Transient response	Rise time	$T_A = 25^\circ\text{C}$, unity gain		0.25	0.8	μs		
	Overshoot			6%	20%			
Bandwidth ⁽²⁾	$T_A = 25^\circ\text{C}$		0.437	1.5	MHz			
Slew rate	$T_A = 25^\circ\text{C}$, unity gain		0.3	0.7	V/ μs			
Power consumption	$V_S = \pm 20 \text{ V}$	$T_A = 25^\circ\text{C}$	80	150	mW			
		$T_A = T_{A\text{MIN}}$	165					
		$T_A = T_{A\text{MAX}}$	135					

(2) Calculated value from: BW (MHz) = 0.35/Rise Time (μs).

6.7 Electrical Characteristics, LM741C⁽¹⁾

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \leq 10 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	2		6	mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	7.5		mV	
Input offset voltage adjustment range	$T_A = 25^\circ\text{C}$, $V_S = \pm 20 \text{ V}$		± 15		mV	
	$T_A = 25^\circ\text{C}$	20	200	nA		
Input offset current			300			
$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	80	500	nA			
Input bias current	$T_A = 25^\circ\text{C}$		0.8		0.8	μA
	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	± 12	± 13	V		
Input resistance	$T_A = 25^\circ\text{C}$, $V_S = \pm 20 \text{ V}$		0.3	2	M Ω	
	$T_A = 25^\circ\text{C}$	20	200	V/mV		
Input voltage range			15			
$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	25		mV			
Large signal voltage gain	$V_S = \pm 15 \text{ V}$, $V_O = \pm 10 \text{ V}$, $R_L \geq 2 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	20	200	V/mV	
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	15			
Output voltage swing	$V_S = \pm 15 \text{ V}$	$R_L \geq 10 \text{ k}\Omega$	± 12	± 14	V	
		$R_L \geq 2 \text{ k}\Omega$	± 10	± 13		
Output short circuit current	$T_A = 25^\circ\text{C}$		25		mA	
Common-mode rejection ratio	$R_S \leq 10 \text{ k}\Omega$, $V_{CM} = \pm 12 \text{ V}$, $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		70	90	dB	
Supply voltage rejection ratio	$V_S = \pm 20 \text{ V}$ to $V_S = \pm 5 \text{ V}$, $R_S \leq 10 \Omega$, $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		77	96	dB	
Transient response	Rise time	$T_A = 25^\circ\text{C}$, Unity Gain		0.3	μs	
	Overshoot	5%				
Slew rate	$T_A = 25^\circ\text{C}$, Unity Gain		0.5		V/ μs	
Supply current	$T_A = 25^\circ\text{C}$		1.7	2.8	mA	
Power consumption	$V_S = \pm 15 \text{ V}$, $T_A = 25^\circ\text{C}$		50	85	mW	

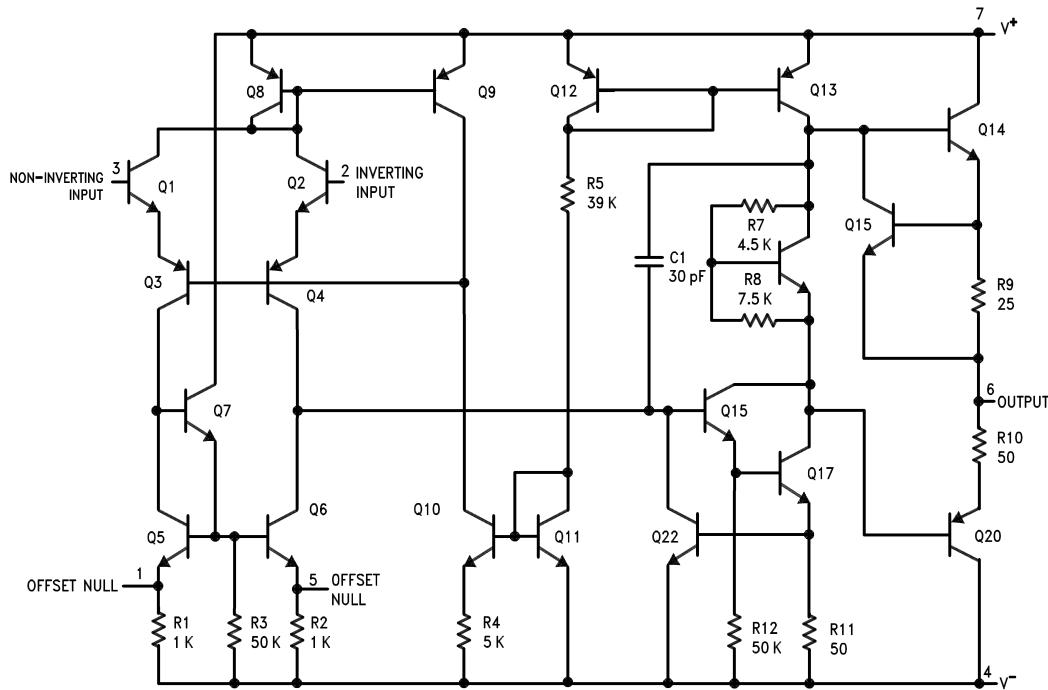
(1) Unless otherwise specified, these specifications apply for $V_S = \pm 15 \text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$.

7 Detailed Description

7.1 Overview

The LM74 devices are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. It is intended for a wide range of analog applications. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications. The LM741 can operate with a single or dual power supply voltage. The LM741 devices are direct, plug-in replacements for the 709C, LM201, MC1439, and 748 in most applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Overload Protection

The LM741 features overload protection circuitry on the input and output. This prevents possible circuit damage to the device.

7.3.2 Latch-up Prevention

The LM741 is designed so that there is no latch-up occurrence when the common-mode range is exceeded. This allows the device to function properly without having to power cycle the device.

7.3.3 Pin-to-Pin Capability

The LM741 is pin-to-pin direct replacements for the LM709C, LM201, MC1439, and LM748 in most applications. Direct replacement capabilities allows flexibility in design for replacing obsolete parts.

7.4 Device Functional Modes

7.4.1 Open-Loop Amplifier

The LM741 can be operated in an open-loop configuration. The magnitude of the open-loop gain is typically large thus for a small difference between the noninverting and inverting input terminals, the amplifier output will be driven near the supply voltage. Without negative feedback, the LM741 can act as a comparator. If the inverting input is held at 0 V, and the input voltage applied to the noninverting input is positive, the output will be positive. If the input voltage applied to the noninverting input is negative, the output will be negative.

7.4.2 Closed-Loop Amplifier

In a closed-loop configuration, negative feedback is used by applying a portion of the output voltage to the inverting input. Unlike the open-loop configuration, closed loop feedback reduces the gain of the circuit. The overall gain and response of the circuit is determined by the feedback network rather than the operational amplifier characteristics. The response of the operational amplifier circuit is characterized by the transfer function.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM741 is a general-purpose amplifier than can be used in a variety of applications and configurations. One common configuration is in a noninverting amplifier configuration. In this configuration, the output signal is in phase with the input (not inverted as in the inverting amplifier configuration), the input impedance of the amplifier is high, and the output impedance is low. The characteristics of the input and output impedance is beneficial for applications that require isolation between the input and output. No significant loading will occur from the previous stage before the amplifier. The gain of the system is set accordingly so the output signal is a factor larger than the input signal.

8.2 Typical Application

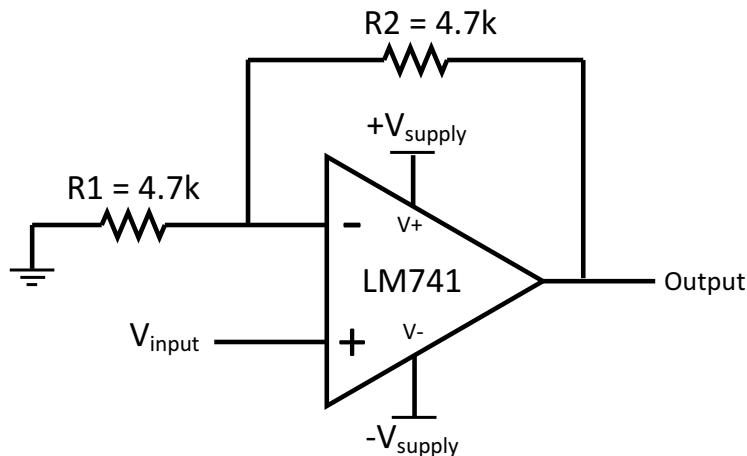


Figure 1. LM741 Noninverting Amplifier Circuit

8.2.1 Design Requirements

As shown in Figure 1, the signal is applied to the noninverting input of the LM741. The gain of the system is determined by the feedback resistor and input resistor connected to the inverting input. The gain can be calculated by Equation 1:

$$\text{Gain} = 1 + (R2/R1) \quad (1)$$

The gain is set to 2 for this application. R1 and R2 are 4.7-k resistors with 5% tolerance.

8.2.2 Detailed Design Procedure

The LM741 can be operated in either single supply or dual supply. This application is configured for dual supply with the supply rails at ± 15 V. The input signal is connected to a function generator. A 1-Vpp, 10-kHz sine wave was used as the signal input. 5% tolerance resistors were used, but if the application requires an accurate gain response, use 1% tolerance resistors.

Typical Application (continued)

8.2.3 Application Curve

The waveforms in [Figure 2](#) show the input and output signals of the LM741 non-inverting amplifier circuit. The blue waveform (top) shows the input signal, while the red waveform (bottom) shows the output signal. The input signal is 1.06 V_{pp} and the output signal is 1.94 V_{pp}. With the 4.7-k Ω resistors, the theoretical gain of the system is 2. Due to the 5% tolerance, the gain of the system including the tolerance is 1.992. The gain of the system when measured from the mean amplitude values on the oscilloscope was 1.83.

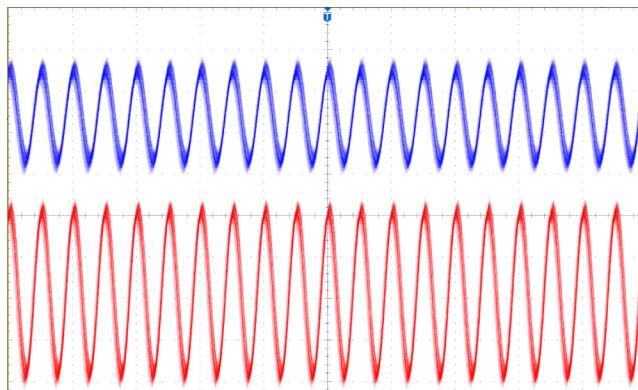


Figure 2. Waveforms for LM741 Noninverting Amplifier Circuit

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, a 0.1- μ F capacitor is recommended and should be placed as close as possible to the LM741 power supply pins.

10 Layout

10.1 Layout Guidelines

As with most amplifiers, take care with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize pick-up and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground. As shown in [Figure 3](#), the feedback resistors and the decoupling capacitors are located close to the device to ensure maximum stability and noise performance of the system.

10.2 Layout Example

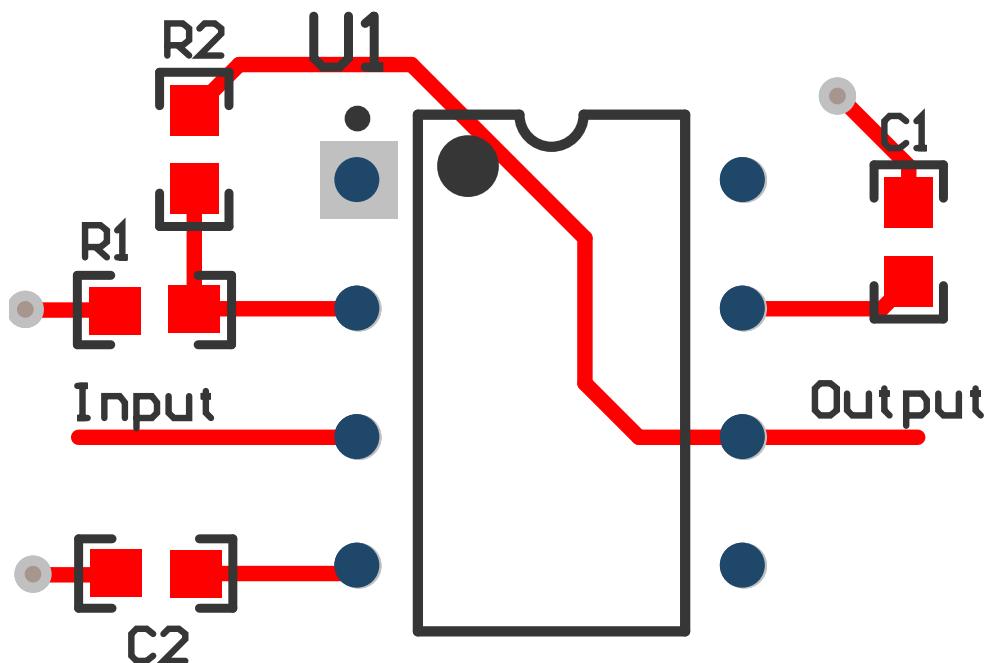


Figure 3. LM741 Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

 These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022 — TI Glossary.](#)

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM741C-MWC	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-40 to 85		Samples
LM741CN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	Call TI SN	Level-1-NA-UNLIM	0 to 70	LM 741CN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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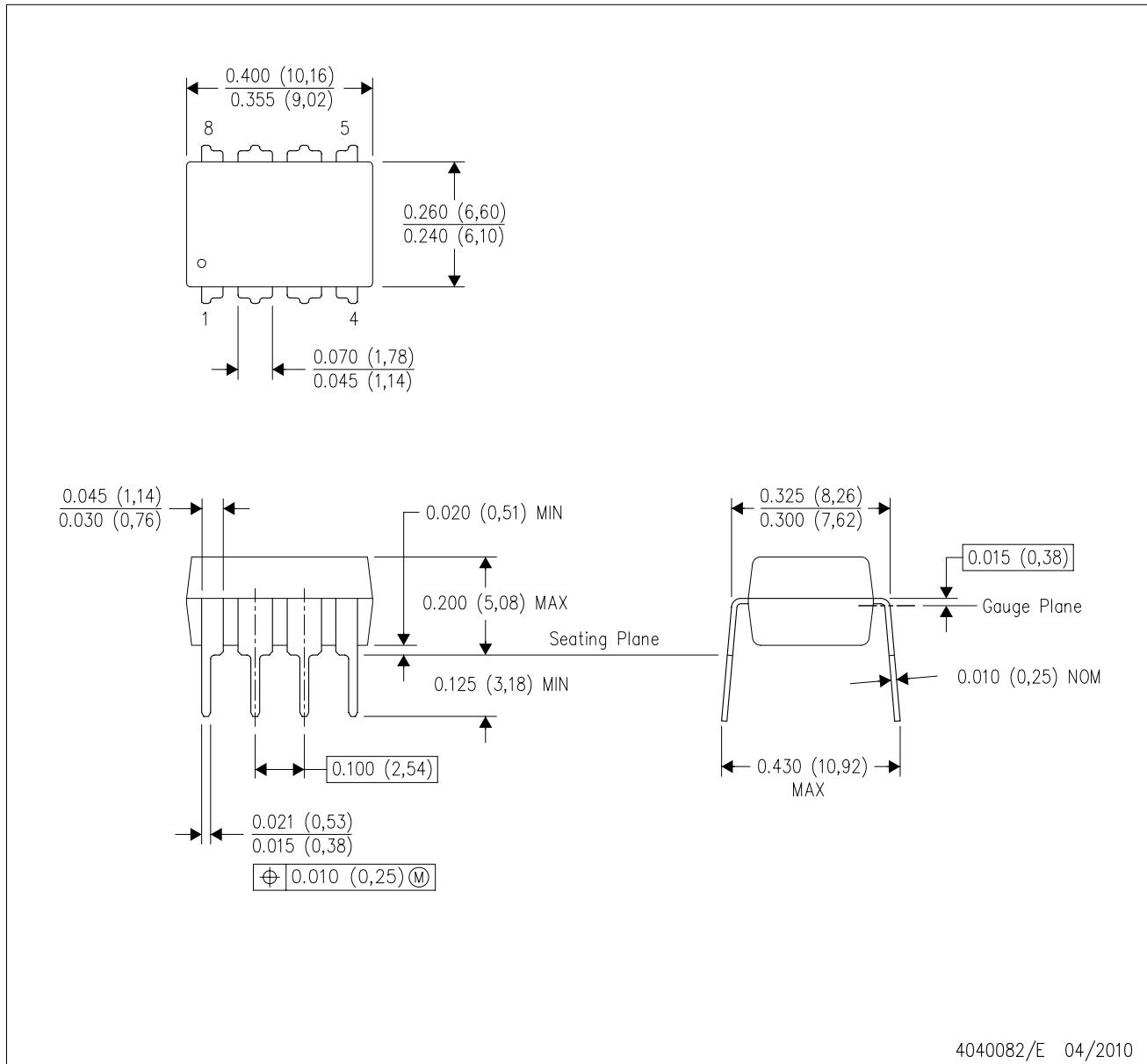
PACKAGE OPTION ADDENDUM

10-Dec-2020

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Falls within JEDEC MS-001 variation BA.

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