DATA SHEET

FT3519T

True Multi-Touch
Capacitive Touch Panel Controller

Dec. 6, 2021

Version: 1.5

Table of Contents

INTRODUCTION

The FT3519T is a single-chip capacitive touch panel controller with built-in enhanced Micro-controller unit (MCU) with 54KB PRAM, 18KB DRAM and 128KB Flash. It provides the benefits of full screen common mode scan technology, fast response time and high level of accuracy. It can drive capacitive type touch panel with up to 23 driving (TX) and 36 sensing lines (RX).

FEATURES

- Mutual Capacitive Sensing Techniques
- Full Screen Common Mode Scan Techniques
- True Multi-touch up to 10 Points of absolute X and Y Coordinates
- High immunity to RF and power Interferences
- Supports up to 23TX + 36RX
- Supports up to 10 fingers
- High immunity to inductive power noise
- Automatic mode switching (Active, Monitor, Sleep)
- Support up to 2 fingers 300Hz touch sensing rate
- Auto-calibration
- 11-Bit ADC Accuracy
- Serial interfaces:
  - I2C, up to 400Kbps
  - SPI, up to maximum 20MHz
- Power
  - 2.7 to 3.6V Operating Voltage
  - IOVCC supports 1.7V~3.6V
- Built-in 128KB Flash
- Features “short I/O” testing for sense pins
- 3 Operating Modes
  - Active
  - Monitor
  - Sleep
- Operating Temperature Range: -30°C to +85°C
- Package:
  - BGA76 5x5x0.47mm, 0.5mm/pitch

1. OVERVIEW

1.1. TYPICAL APPLICATIONS

FT3519T accommodates a wide range of applications with a set of buttons up to a 2D touch sensing device;

It's powerful design for below applications.

- Tablets
- Mobiles
- Navigation systems, GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras

FT3519T support Touch Panel, the spec is listed in the following table,

Part Number	Package	TX	RX	Total Channels	Recommended for Smart Phone TP Size
FT3519T	BGA76 5x5x0.47mm Pitch =0.5mm	23	36	59	7.0"

2. FUNCTIONAL BLOCK DESCRIPTION

2.1. Architecture Overview

Figure2-1 shows the overall architecture for the FT3519T.

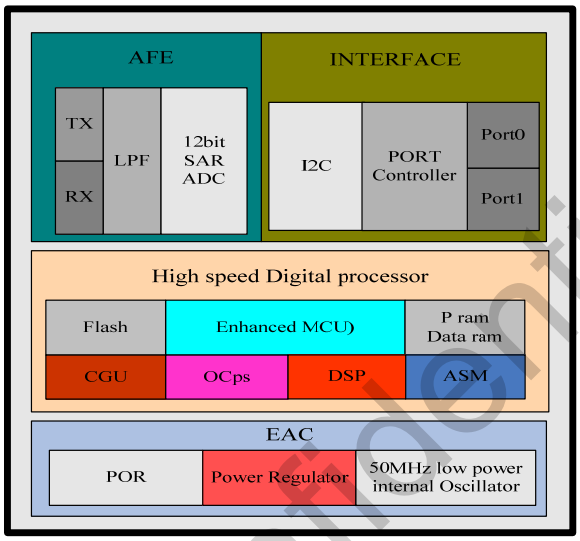


Figure 2-1 System Architecture Diagram

The FT3519T is comprised of five main functional parts listed below,

- **Touch Panel Interface Circuits**

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. It includes both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces.

- **Enhanced MCU with DSP accelerator**

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash memory is implemented to store programs and some key parameters.

Complex signal processing algorithms are implemented by MCU and DSP accelerator to detect the touches reliably and efficiently.

Communication protocol software is also implemented in this MCU to exchange data and control information with the host processor.

- **External Interface**
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip. The port is also use to wake up the FT3519T from the Sleep mode.
- **A watch dog timer is implemented to ensure the robustness of the chip.**
- **A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply**
- **Power-On Reset (POR) is active until VDDD is higher than some level and hold decades of μs.**

2.2. MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- A DSP accelerator cooperates with MCU to process the complex algorithms
- Timer: A number of timers are available to generate different clocks
- Clock Manager: To control various clocks under different operation conditions of the system

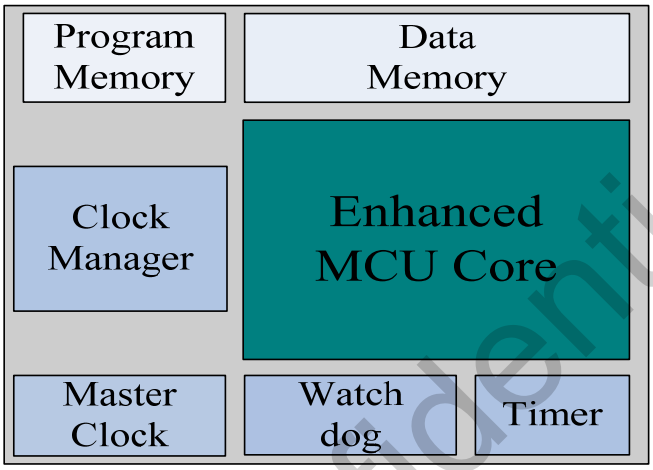


Figure 2-2 MCU Block Diagram

2.3. Operation Modes

FT3519T offers following three modes:

- **Active Mode**

When in this mode, FT3519T actively scans the panel. The default scan rate is 100 frames per second. The host processor can configure it to speed up or to slow down.

- **Monitor Mode**

In this mode, FT3519T scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. In this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT3519T shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- **Sleep Mode**

In this mode, the chip is set in a power down mode. It shall only respond to the “RESET” signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.4. Interface

Figure 2-3 shows the interface between a host processor and FT3519T. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT3519T to the Host
- Reset Signal from the Host to FT3519T

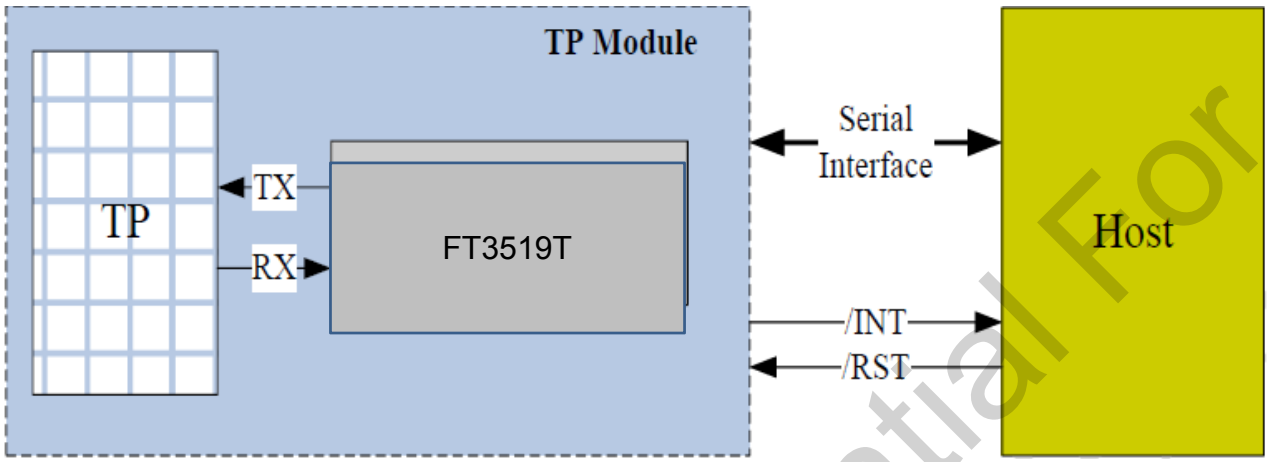


Figure 2-3 Host Interface Diagram

The serial interface of FT3519T is I2C/SPI. The detail of the interface is described in detail in Section 2.5. The interrupt signal (/INT) is used for FT3519T to inform the host that data are ready for the host to receive. The /RST signal is used for the host to wake up FT3519T from the Hibernate mode. After resetting, FT3519T shall enter the Active mode.

2.5. Serial Interface

➢ **I2C Interface**

FT3519T supports the I2C interfaces, which can be used by a host processor or other devices.

The default I2C address is 0x70 and can be changed to the other assigned address by setting.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4**.

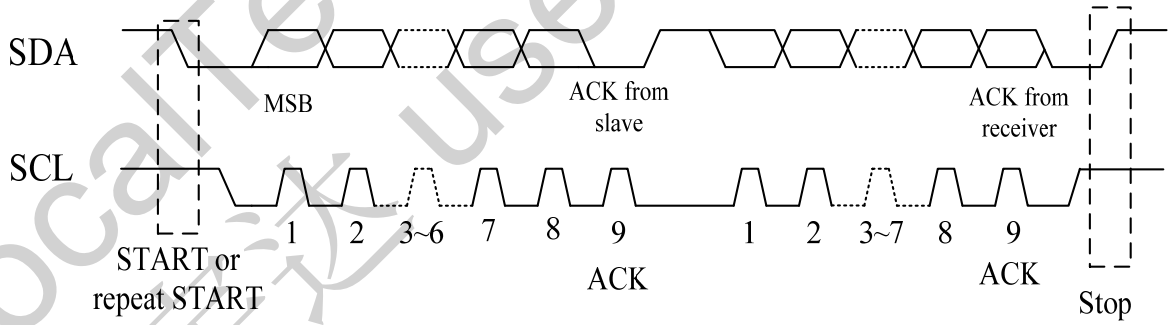


Figure 2-4 I2C Serial Data Transfer Format

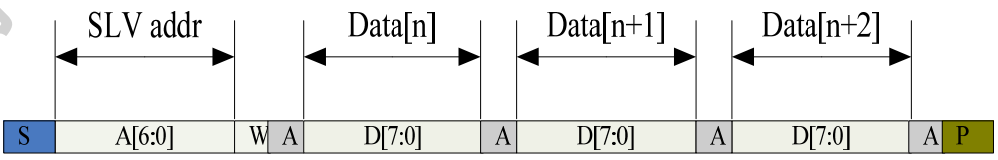


Figure 2-5I2C master write, slave read

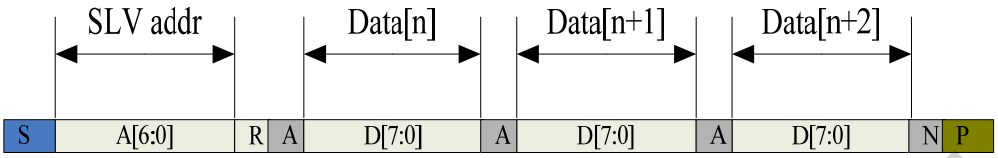


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

- **SPI Interface**

SPI is a 4-wire serial interface, which is always configured in the Slave mode, and transfers data at 8-bit packets. The phase relationship between the data and the clock had been defined be default Mode0, CPOL = 0 & CPHA = 0. The following is a list of the 4 wires:

- CSN: active low select signal
- SCLK: serial data clock
- MISO: data line from slave to master
- MOSI: data line from master to slave

The SPI Mode0 (CPOL = 0 & CPHA = 0) timing diagram is shown in *Figure 2-47.*

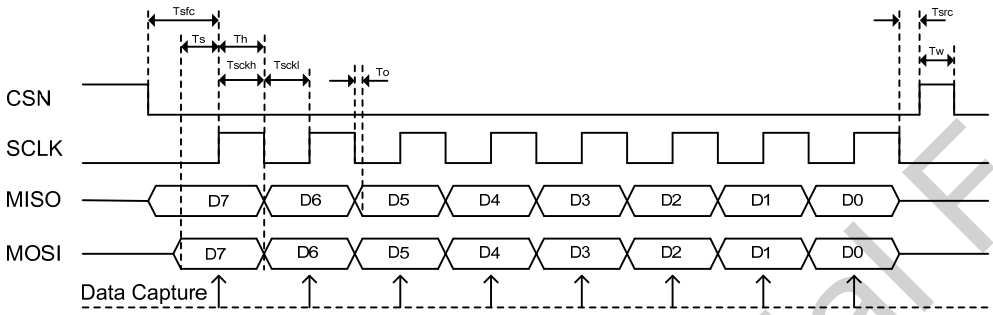


Figure 2-7 SPI Slave, Mode0 (CPOL = 0 & CPHA = 0) timing

SPI Interface Timing Characteristics is shown in Table 2-3.

Table 2-3 SPI Timing Characteristics

Parameter	Description	Min	Max	Unit
Tsckh	SCLK high time	85	--	ns
Tsckl	SCLK low time	85	--	ns
Tw	CSN idle time	1	--	us
Ts	MOSI data valid to SCLK sample edge	40	--	ns
Th	SCLK sample edge to MOSI data change	40	--	ns
To	SCLK shift edge to MISO data change	0	40	ns
Tsfc	CSN falling edge to first SCLK edge	40	--	ns
Tsrc	Last SCLK edge to CSN rising edge	40	--	ns

3. ELECTRICAL SPECIFICATIONS

3.1. Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDD3 – VSS	2.7 ~ +3.6	V	1, 2
I/O Digital Voltage	IOVCC	1.7~ +3.6	V	1
Operating Temperature	Topr	-30 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1
ESD “Human Body Mode”	HBM	8000	V	3
ESD “Charged Device Mode”	CDM	≧1000	V	4
Latch up	I latch-up	+/-200@1.5Vmax	mA	5

Notes

1. If used beyond the absolute maximum ratings, FT3519T may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDD (high) ≥VSS (low)
3. ESD HBM refers to ANSI/ESDA/JEDEC JS-001-2014.
4. ESD CDM is based on JESD22-C101-E.
5. Latch up refers to JESD78

3.2. DC Characteristics

Table 3-2 DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	**VIH**	**V**		0.7 x IOVCC	--	IOVCC+0.3	
Input low -level voltage	**VIL**	**V**		-0.3	--	0.3 x IOVCC	
Output high -level voltage	**VOH**	**V**		0.7 x IOVCC	--	--	
Output low -level voltage	**VOL**	**V**		--	--	0.3 x IOVCC	
I/O leakage current	**ILI**	**uA**		-1	--	1	
Step-up output voltage	**VDD5**	**V**	VDD3=2.8V		5V		
Power Supply voltage	**VDD3**	**V**		2.8	--	3.5	

Notes:

This sample data is intended for design guidance only. Values shown are typical for a 16Tx × 28Rx sensor configured at 103 Hz report rate. Actual current will depend on the particular sensor design and firmware options. The DC characteristics are tested under the temperature 25℃.

3.3. AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3=2.8V; Ta=25℃	62.7	64	65.3	

Table 3-3 AC Characteristics of TX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		50	150	400	KHz	

3.4. I/O PORTS CIRCUITS

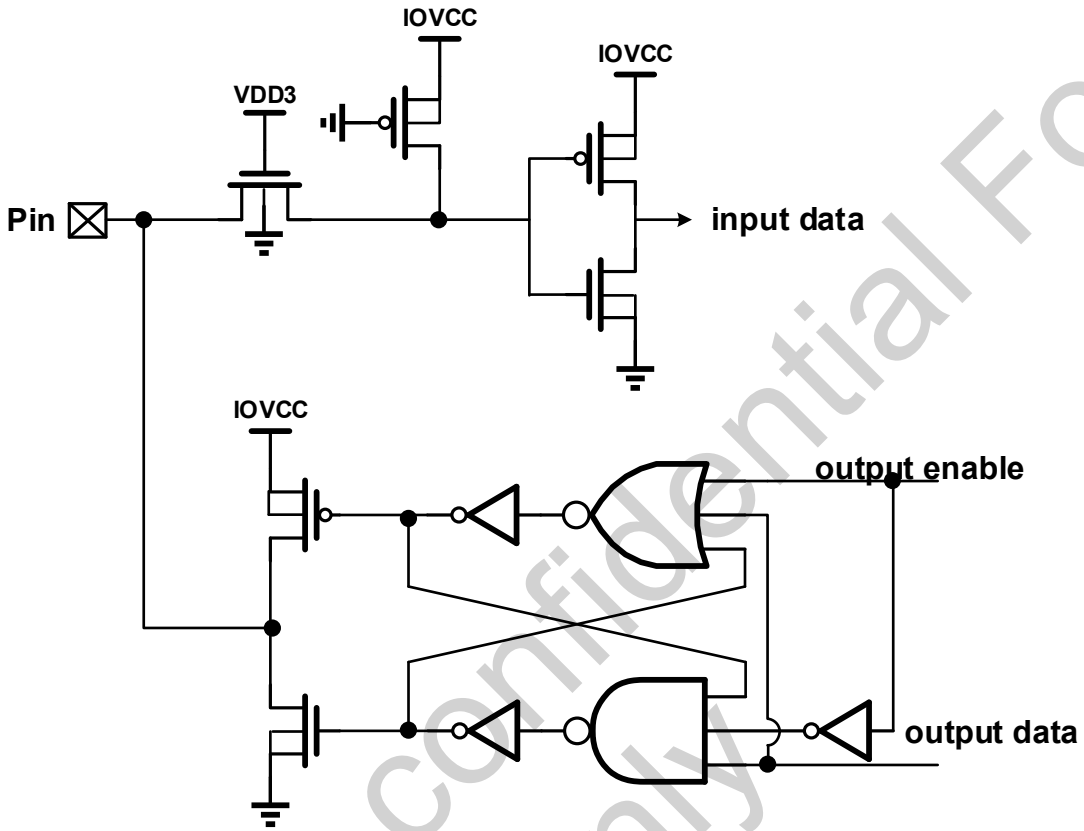


Figure 3-1 General Purpose *In/Out Port Circuit*.

The input/output property can be configured via firmware setting. The firmware can also control its output behavior as push-pull or as open-drain that SDA of I2C interface is required.

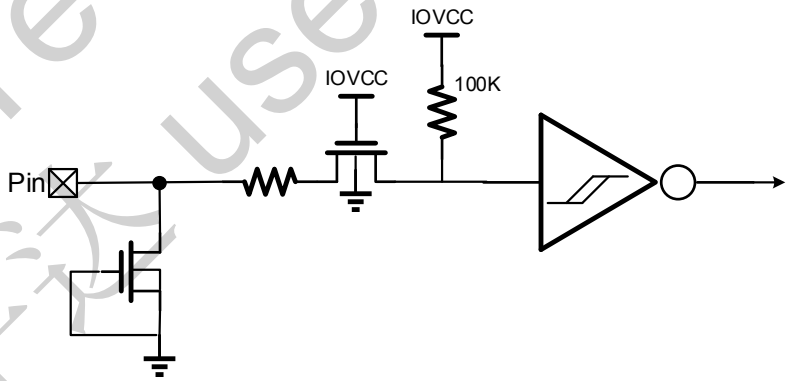


Figure 3-2 Reset Input Port Circuits

3.5. Power ON/ Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

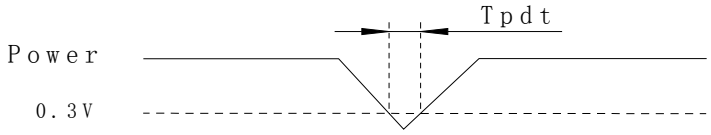


Figure 3-3 Power Cycle requirement

There are two power supply configurations, in one mode, VDD supplies whole chip exclude the communication I/O and GPIO, IOVCC supplies this part power, as figure 3-4-1and figure 3-4-2. And the other mode, VDD supplies whole chip power, as figure 3-4-3 and figure 3-4-4;

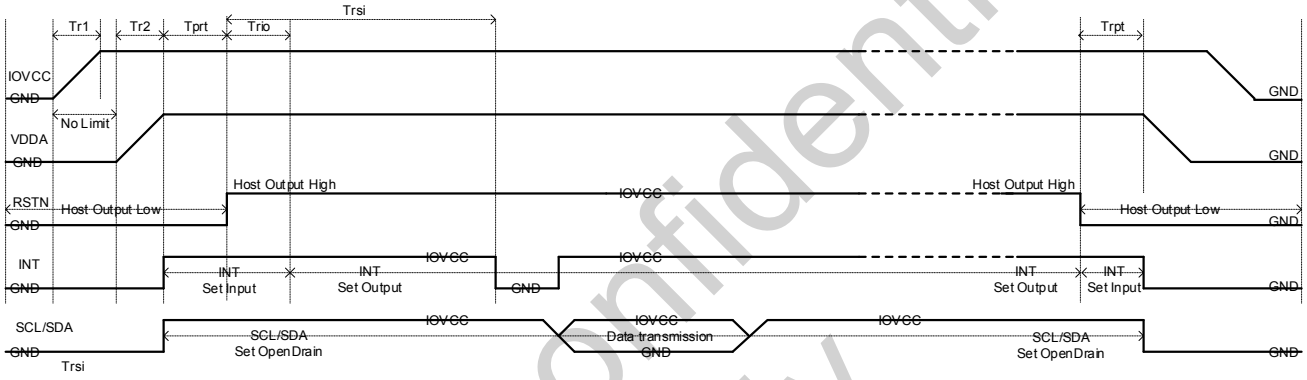


Figure 3-4-1 Power on Sequence for 2 power sources—I2C interface

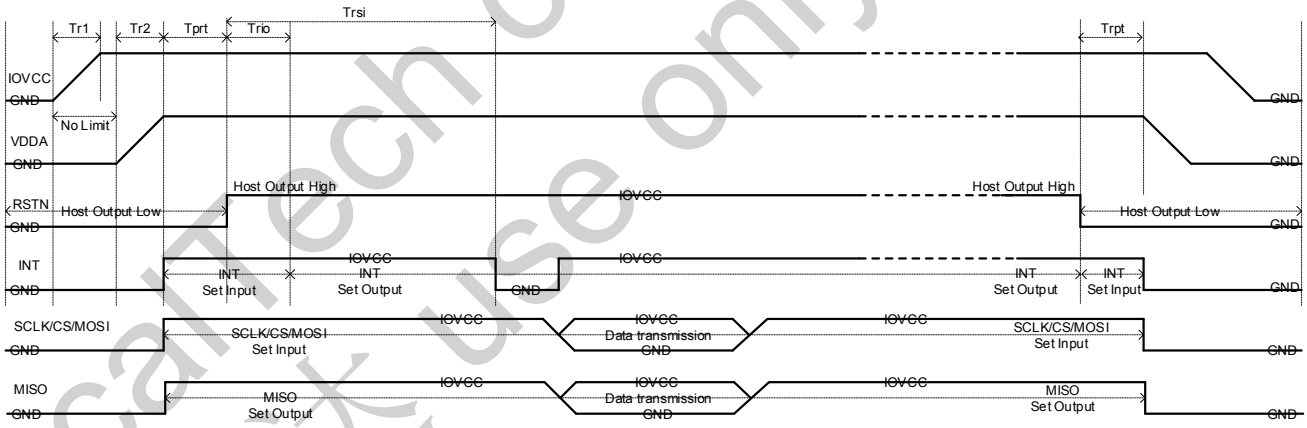


Figure 3-4-2 Power on Sequence for 2 power sources—SPI interface

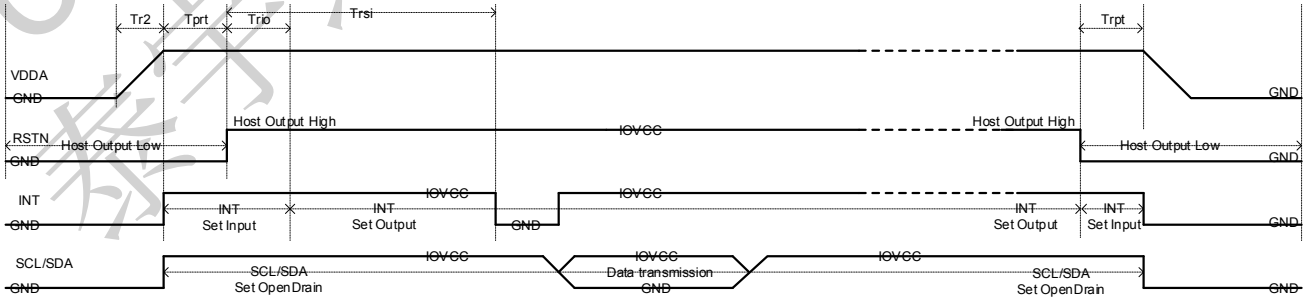


Figure 3-4-3 Power on Sequence for 1 power source—I2C interface

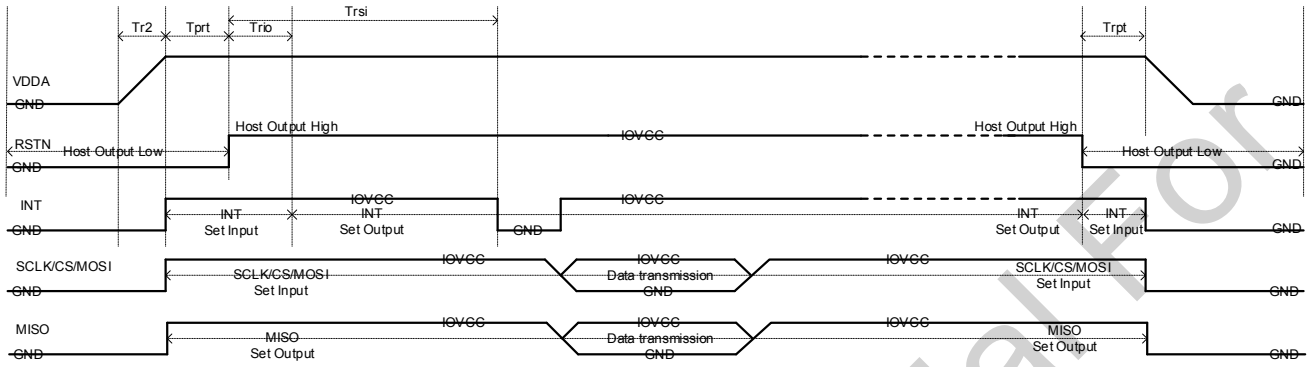


Figure 3-4-4 Power on Sequence for 1 power source—SPI interface

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

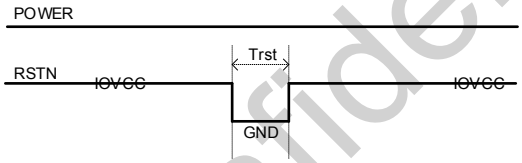


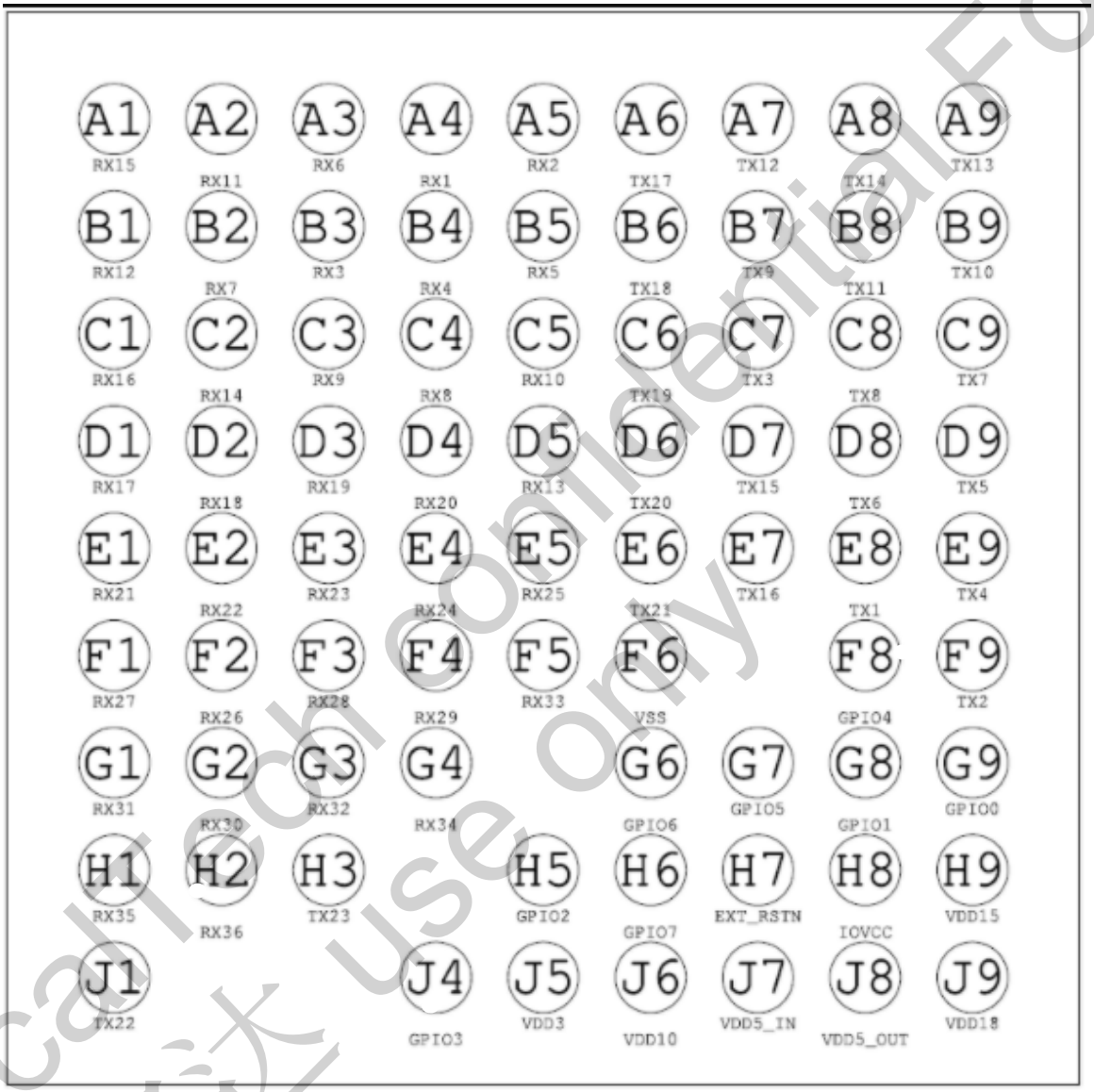
Figure 3-5 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tr1	Rise time of IOVCC from 0% to 100%	0.1	10	ms
Tr2	Rise time of VDDA from 0% to 100%	0.1	10	ms
Tprt	Time for RSTN to remain low after IOVCC/VDDA power is ready	1	--	ms
Trio	Time for INT to set input to output after RSTN becomes high	6	--	ms
Trsi	Time of starting to report point after resetting	TBD	TBD	ms
Trpt	Time for RSTN to remain low before power off	1	--	ms
Trst	Reset time	10	--	us

4. Pin Configurations

Pin List of FT3519T



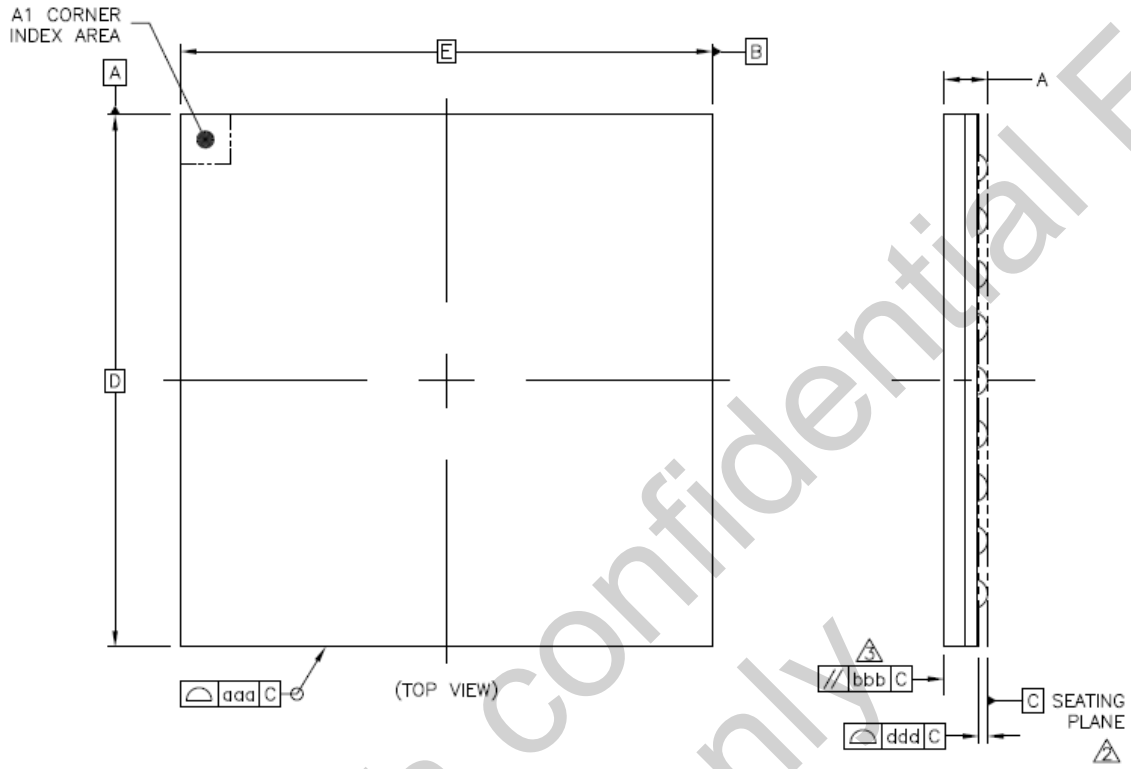
FT3519T Package Diagram

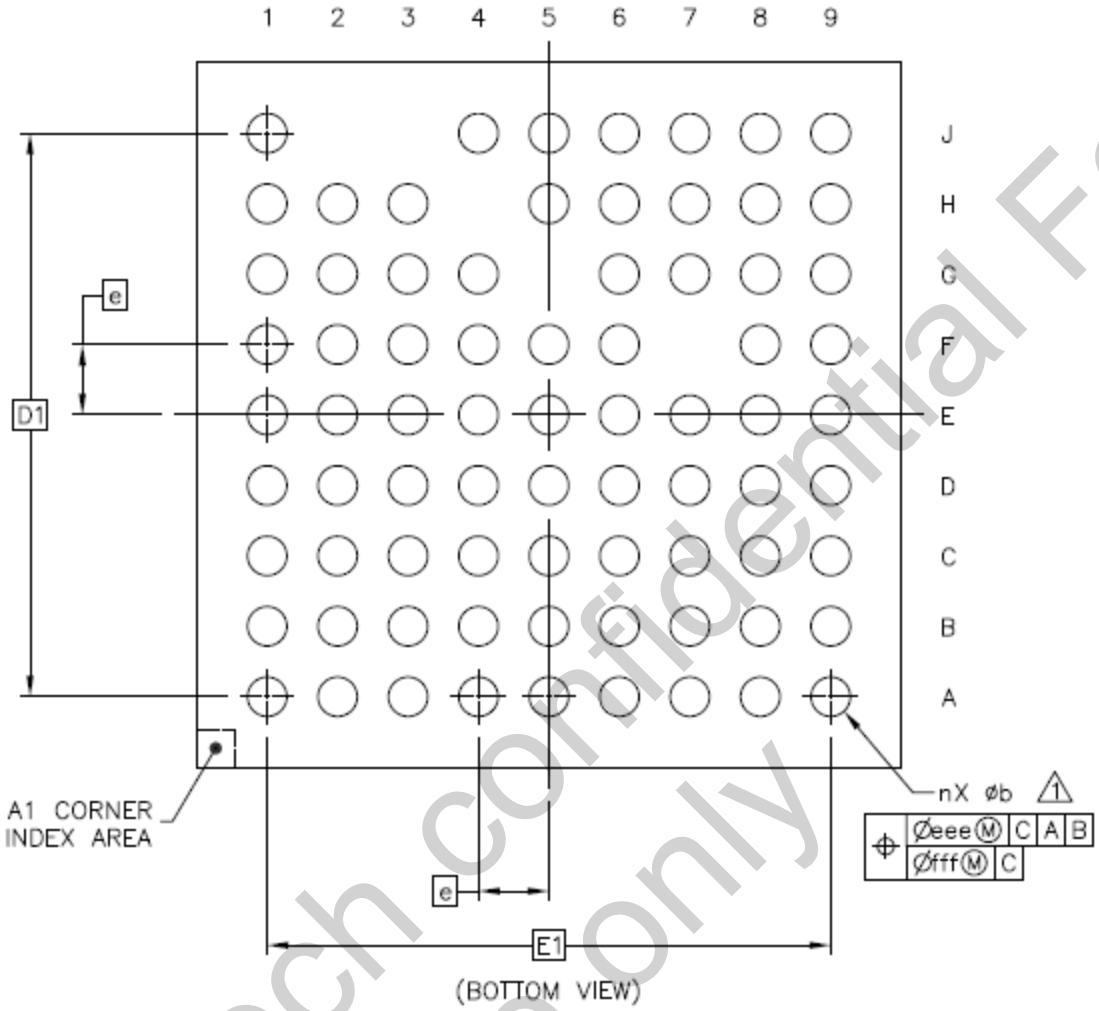
Table 5-1 Pin Definition

Signal	I/O	PAD Type	Function Description
Power Supply Pad			
VDD3	I	Analog Power	VDD3 is IC's Power supply. Connect a capacitor for stabilization (2.7V~3.6V)
IOVCC	I	IO Digital Power	IOVCC is GPIO Power supply. Connect a capacitor for stabilization (1.7V~3.6V)
GND	I	Ground	Ground for whole chip
Regulator & Pump Pad			
VDD15	O	Digital Power	Internal voltage regulator power output for digital circuit（1.35V~1.65V), Connect a capacitor for stabilization
VDD18	O	Digital Power	Internal voltage regulator power output for IO digital circuit （1.7V~1.9V), Connect a capacitor for stabilization
VDD5_OUT	O	Charge Pump	Charge Pump output voltage, external connect to VDD5_IN (4.5V~6.5V), Connect a capacitor for stabilization
VDD5_IN	I	Charge Pump	Charge Pump voltage, external connect to VDD5_OUT (4.5V~6.5V)
VDD10	O	Charge Pump	Charge Pump output voltage for TX driving (7V~11.5V). Connect a capacitor for stabilization
IO Interface PAD			
GPIO0	I/O	Digital IO	General Purpose for Input or Output Pin. When interface is configured as I2C, GPIO0 is SCL
GPIO1	I/O	Digital IO	General Purpose for Input or Output Pin. When interface is configured as I2C, GPIO1 is SDA
GPIO2	I/O	Digital IO	General Purpose for Input or Output Pin. When interface is configured as SPI, GPIO2 is MOSI As input，internal 0.8MΩ pull-up resistor
GPIO3	I/O	Digital IO	General Purpose for Input or Output Pin or TE input for display SYNC signal from display driver IC As input，internal 0.8MΩ pull-up resistor
GPIO4	I/O	Digital IO	General Purpose for Input or Output Pin. When interface is configured as SPI, GPIO4 is SPI_CS As input，internal 0.8MΩ pull-up resistor
GPIO5	I/O	Digital IO	General Purpose for Input or Output Pin. When interface is configured as SPI, GPIO5 is SPI_CLK As input，internal 0.8MΩ pull-up resistor
GPIO6	I/O	Digital IO	INT signal. As input，internal 0.8MΩ pull-up resistor
GPIO7	I/O	Digital IO	General Purpose for Input or Output Pin. When interface is configured as SPI, GPIO7 is SPI_MISO
RSTN	I	Digital IO	Hardware Reset Pin, Low：Reset
TX & RX Pad			
TX1~ TX23	I/O	TX	Scan Drive channel
RX1~ RX36	I/O	RX	Receive channel

5. PACKAGE INFORMATION

5.1. Package Information of BGA-5x5-76 Package





	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.47
BODY SIZE	D		5 BSC	
	E		5 BSC	
BALL DIAMETER			0.2	
BALL PITCH	e		0.5 BSC	
BALL COUNT	n		76	
EDGE BALL CENTER TO CENTER	D1		4 BSC	
	E1		4 BSC	
BODY CENTER TO CONTACT BALL	SD		--- BSC	
	SE		--- BSC	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

5.2. Order Information

Product Name	Package Type	# TX Pins	# RX Pins
FT3519T	BGA-76	23	36

6. POWER CONSUNMPTION REFERENCE

Test conditions: VDD3=3.3V, VDD18=1.8V. Temperature 25℃

Mode	Typ	Unit	Test Condition: Dual power supplies	Note
Active, 120Hz	35.6	mW	VDD3=3.3V,IOVCC=1.8V	One finger
Active, 180Hz	48.7	mW	VDD3=3.3V, IOVCC=1.8V	One finger
Active, 240Hz	50.4	mW	VDD3=3.3V, IOVCC=1.8V	One finger
Active, 270Hz	53.4	mW	VDD3=3.3V, IOVCC=1.8V	One finger
Idle, 100Hz	3.7	mW	VDD3=3.3V, IOVCC=1.8V	
Doze, 90Hz	3.4	mW	VDD3=3.3V, IOVCC=1.8V	
Sleep	0.21	mW	VDD3=3.3V, IOVCC=1.8V	

Notes: This sample data is intended for the design guidance only. The typical value are for a 16TX*34RX sensor panel. The actual current will depend on the sensor design and firmware configuration.

7.Application Schematic

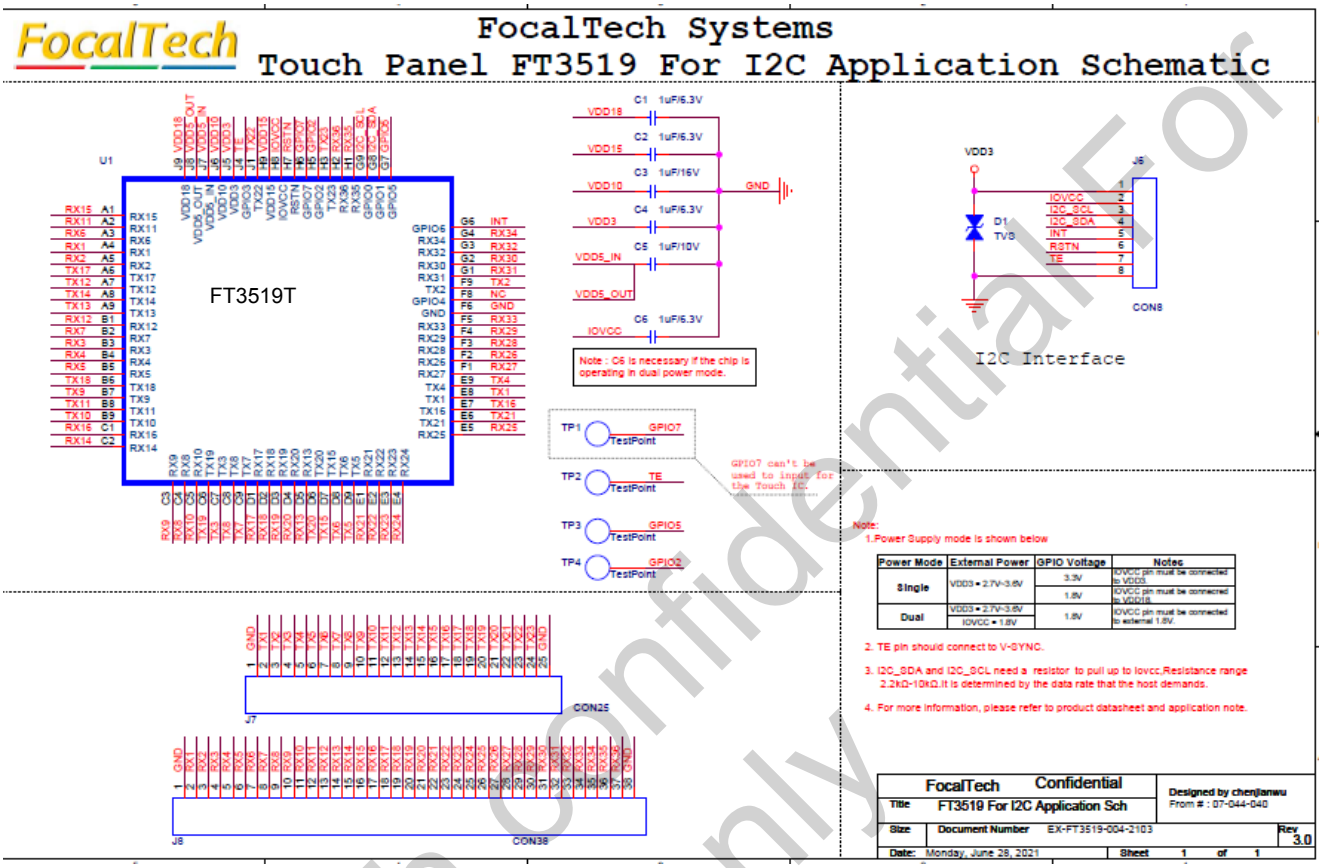


Figure 7-1 I2C Application Schematic

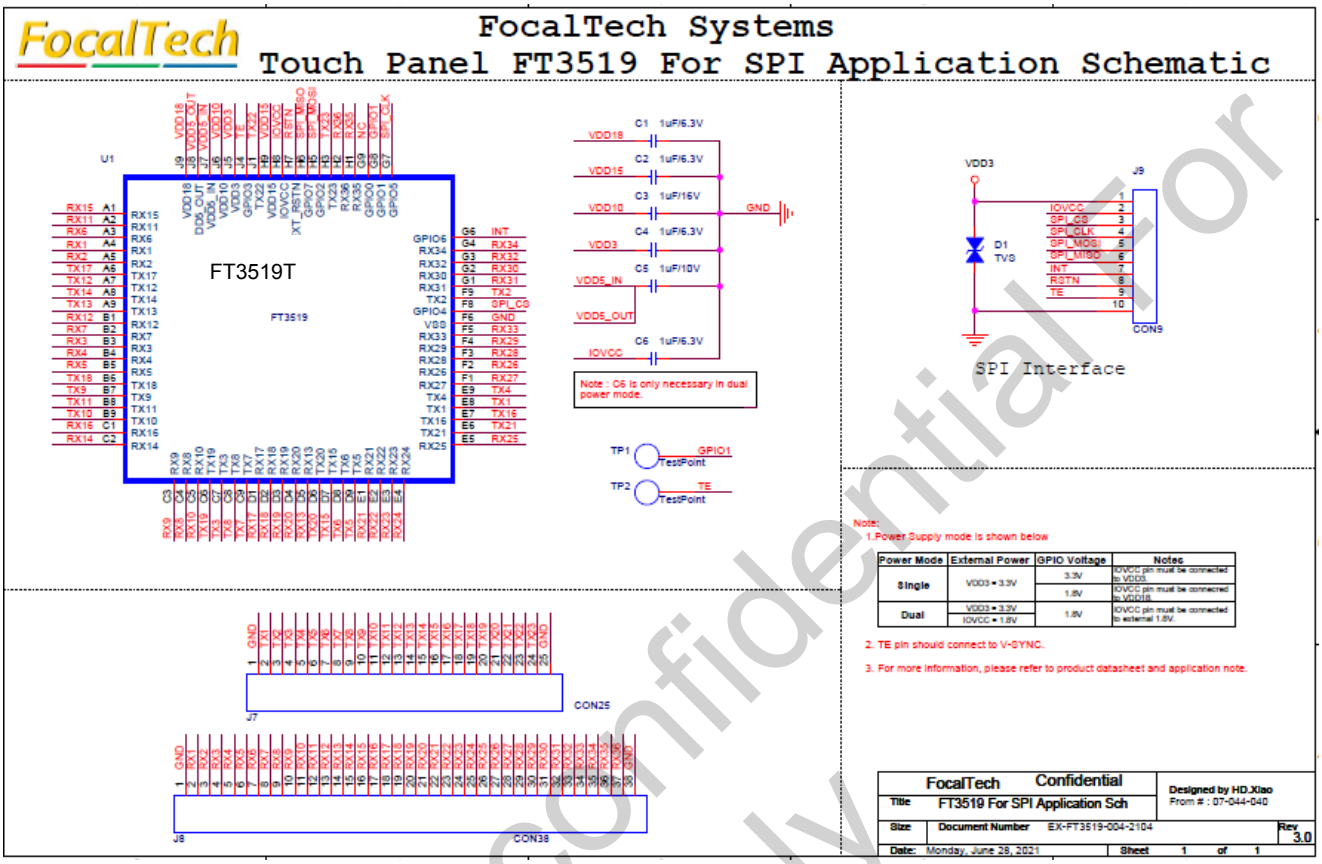


Figure 7-2 SPI Application Schematic

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9. REVISION HISTORY

Date	Revision #	Description	Page	Auditor
Dec.6, 2021	1.5	IO port circuit, power on & reset sequence, IO pin pad description	13, 14, 15, 17	Tom
Nov.12, 2021	1.4	Update IO pin description, application circuits, DC characteristics	12, 17, 22, 23	Tom
Jul.6, 2021	1.3	Update thickness 0.47mm, Add reference application circuit	All	Tom
Apr.26, 2021	1.0	Original. Chip thickness is 0.5mm.	All	Tom