

AMOLED Display Driver IC Specification

ICNA3512

Data Sheet

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Revision History

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1. Description

This document is written for providing a complete reference specification of ICNA3512. IC design engineers would be referring to this specification to design the IC, and test engineers to test the compliance of the manufactured IC to guarantee the performance, and system application engineers to assist the customers to make sure that they are using this IC properly.

The ICNA3512 Support flexible resolution for SPR Panel.

- 1200RGBG x 2950 with 1:1/1:2 MUX (Max. DSC 2-SS)
- 1280RGBG x 2800 with 1:1/1:2 MUX
 - Horizontal Resolution : 720+4N ~ 1280(Max.)
720 ~ 1280 (SPR) x H-line with MUX 1:1 (2560 source channels)
 - 720 ~ 1280 (SPR) x H-line with MUX 1:2 (1280 source channels)
- Vertical Resolution : 2N(Max:2800@1280H)

The ICNA3512 is LTPS AMOLED driver IC for an AMOLED panel with SPR. This IC is a highly integrated Source driver, Panel Gate controller, GRAM, Power management and Timing controller so on. For high-speed data transfer, supports MIPI DSI. The driver can be connected directly to the interface bus. It stores the compressed gray scale display data sent from the AP in its internal display GRAM and generates AMOLED driving signals independently of the AP. Partially stored initialization registers in the OTP are automatically loaded during display start period. This IC has the low current consumption, source driver circuit, high-efficiency power circuit. In addition, power can be controlled more finely using command control.

*MIPI: Mobile Industry Processor Interface, *DSI: Display Serial Interface, *AP: Application Processor, *SPR: Sub Pixel Rendering. *AMOLED: active-matrix organic light-emitting diode

2. Features

■ ICNA3512 supports the following key features:

■ Category: General

Items	Description
Display Type	<ul style="list-style-type: none"> WFHD+ Portrait
Display Resolution	<ul style="list-style-type: none"> 1200RGBG x 2950 with 1:1/1:2 MUX (Max. DSC 2-SS) 1280RGBG x 2800 with 1:1/1:2 MUX Horizontal Resolution: 720+4N~1280(Max) 720 ~ 1280 (SPR) x H-line with MUX 1:1 (2560 source channels) 720 ~ 1280 (SPR) x H-line with MUX 1:2 (1280 source channels) Vertical Resolution: 2N(Max:2800@1280H)
Sub Pixel Rendering	<ul style="list-style-type: none"> RGBG SPR GGRB SPR Delta RGB SPR
Color Depth	<ul style="list-style-type: none"> 24 or 30 bits
Color Mode	<ul style="list-style-type: none"> 16.7 M colors/1Billion color 8 or 10 colors
Frame Rate	<ul style="list-style-type: none"> Dynamic Frame Rate 144Hz @ Command mode (Max.) 144Hz @ Video mode (Max.) AOD(1~60Hz)
Display Operation Mode	<ul style="list-style-type: none"> Partial Mode Idle Mode AOD Mode Local High Brightness Mode (HBM)
Frame Memory	<ul style="list-style-type: none"> WFHD+ with 1/3 RAM Graphic RAM size: 28.672M-bits (1280 x 2800 x 24bit / 3)
Package	<ul style="list-style-type: none"> COP
Operating Temperature	<ul style="list-style-type: none"> -40°C ~ 85°C

■ Category: Interface

Items	Description
MIPI	<ul style="list-style-type: none"> MIPI DPHY 1-port, 4-lane, V1.1 / MIPI DSI: V1.2 for DPHY - MIPI Speed: 1.3Gbps/Lane MIPI CPHY 1-port, 3-trio / MIPI DSI-2: V1.0 for CPHY - MIPI Speed: 1.0Gsps/Trio
Compression	<ul style="list-style-type: none"> DSC V1.2a, Two Decoder - YCbCr Domain: One decoder only - RGB Domain: One or Two decoder Compression Ratio - 8BPC-8BPP: 16 / 48 bit (3:1 Compression, RGB) - 10BPC-8BPP: 16 / 60 bit (3.75:1 Compression, RGB) - 10BPC-10BPP : 20 / 60 bit (3:1 Compression, RGB) - 8BPC-12BPP : 24 / 48bit bit(2:1 Compression, RGB) - 10BPC-12BPP : 24 / 60bit bit(2.5:1 Compression, RGB) - 8BPC-6BPP: 12 / 32 bit (2.67:1 Compression, Native 422) - 8BPC-7BPP: 14 / 32 bit (2.29:1 Compression, Native 422) - 8BPC-8BPP: 16 / 32 bit (2:1 Compression, Native 422)

	<ul style="list-style-type: none"> - 8BPC-10BPP : 20 / 32 bit (1.6:1 Compression, Native 422) - 10BPC-7BPP: 14 / 40 bit (2.86:1 Compression, Native 422) - 10BPC-8BPP: 16 / 40 bit (2.5:1 Compression, Native 422) - 10BPC-10BPP: 20 / 40 bit (2:1 Compression, Native 422)
Flash I/F	<ul style="list-style-type: none"> • Serial peripheral interface (SPI) • Support several types of Flash Memory

■ Category: Self-Diagnostic

Items	Description
Panel Related	<ul style="list-style-type: none"> • Panel Crack Detection
IC Related	<ul style="list-style-type: none"> • Low Voltage Detection • SRAM CRC/ECC Comparison • Thermal Detection • UCS Checksum Error Check

■ Category: Display Quality Technology

Items	Description
Image Enhancement	<ul style="list-style-type: none"> • Scaling Up Function (HD to WFHD and FHD to WFHD) • Sharpness Enhancement • Contrast Optimization • High Dynamic Range • Color Gamut Mapping • Color Temperature Adjustment

■ Category: AMOLED Panel Control Technology

Items	Description
Panel Structure	<ul style="list-style-type: none"> • Sub Pixel Rendering <ul style="list-style-type: none"> → RGBG SPR → GGRB SPR → Delta RGB SPR • Notch, Round-Corner Compensation
Panel Compensation	<ul style="list-style-type: none"> • ELVDD Compensation • IR Drop Compensation (IRC) / Dynamic color control (DCC) • De-Mura/De-burn in Function
Power Saving	<ul style="list-style-type: none"> • Brightness Control • ACL/MCL • Always On Display (AOD) <ul style="list-style-type: none"> → Image Sticking Prevention → ELVDD, ELVSS are from the DDIC • Dynamic ELVSS

FPS Application	<ul style="list-style-type: none"> • Finger Print Sensor (FPS) function with Local High Brightness Mode (HBM)
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■ Category: AMOLED Panel Driving Control

Items	Description
GOA Timing	<ul style="list-style-type: none"> • 16 sets GOA control outputs each side • Support GOA pin swapping function • EM Duty Function
MUX	<ul style="list-style-type: none"> • 1:1 (No MUX) / 1:2(MUX)
Source	<ul style="list-style-type: none"> • 2560 channel outputs (Max)
Gamma	<ul style="list-style-type: none"> • RGB Separate Digital Gamma Structure
PMIC Control	<ul style="list-style-type: none"> • SWIRE, SWIRE2 for on Module DC/DC converter

■ Category: Supply Voltage Range

Items	Description
VDDI (I/O supply)	<ul style="list-style-type: none"> • 1.65V ~ 1.95V (Typ. 1.8V)
VCI (Analog supply)	<ul style="list-style-type: none"> • 2.65V ~ 3.6V (Typ. 3.0V)
AVDD (Source supply)	<ul style="list-style-type: none"> • 6.0V ~ 8.0V (Typ. 7.3V)
ELVDD	<ul style="list-style-type: none"> • 4.6V ~ 5.0V (Default: 4.6V @ 400 mA)
ELVSS	<ul style="list-style-type: none"> • -0.8V ~ -6.4V (Default: -5.4V@ 400 mA)
VDD (Logic supply)	<ul style="list-style-type: none"> • 1.05V ~ 1.25V (Typ. 1.15V)

■ Category: Output Voltage Range

Items	Description
VOUT2	<ul style="list-style-type: none"> • 7.0V ~ 15.0V (Typ. 8.0V, Step: 0.5V) • Step-up converter for VGH
VGH1	<ul style="list-style-type: none"> • 3.0V ~ 14.5V (Typ. 7.0V, Step: 0.1V) • The positive voltage for GOA driver
VGH2	<ul style="list-style-type: none"> • 3.0V ~ 14.5V (Typ. 7.0V, Step: 0.1V) • The positive voltage for GOA driver
VOUT4	<ul style="list-style-type: none"> • -2.0V ~ -7.0V (Typ. -4.0V, Step: 0.5V) • Step-up converter for VGL
VGL1	<ul style="list-style-type: none"> • -15.0V ~ -3.0V (Typ. -7.0V, Step: 0.1V) • The negative voltage for GOA driver
VGL2	<ul style="list-style-type: none"> • -14.5V ~ -2.5V (Typ. -7.0V, Step: 0.1V) • The negative voltage for GOA driver
VH_A	<ul style="list-style-type: none"> • 0.5V ~ 6.0V (Typ. 3.0V, Step: 0.1V) • The OLED pixel reference voltage
VL_A	<ul style="list-style-type: none"> • -6.0V ~ -0.5V (Typ. -3.0V, Step: 0.1V) • The OLED pixel reference voltage
VH_B	<ul style="list-style-type: none"> • 0.5V ~ 6.0V (Typ. 3.0V, Step: 0.1V) • The OLED pixel reference voltage
VL_B	<ul style="list-style-type: none"> • -6.0V ~ -0.5V (Typ. -3.0V, Step: 0.1V) • The OLED pixel reference voltage

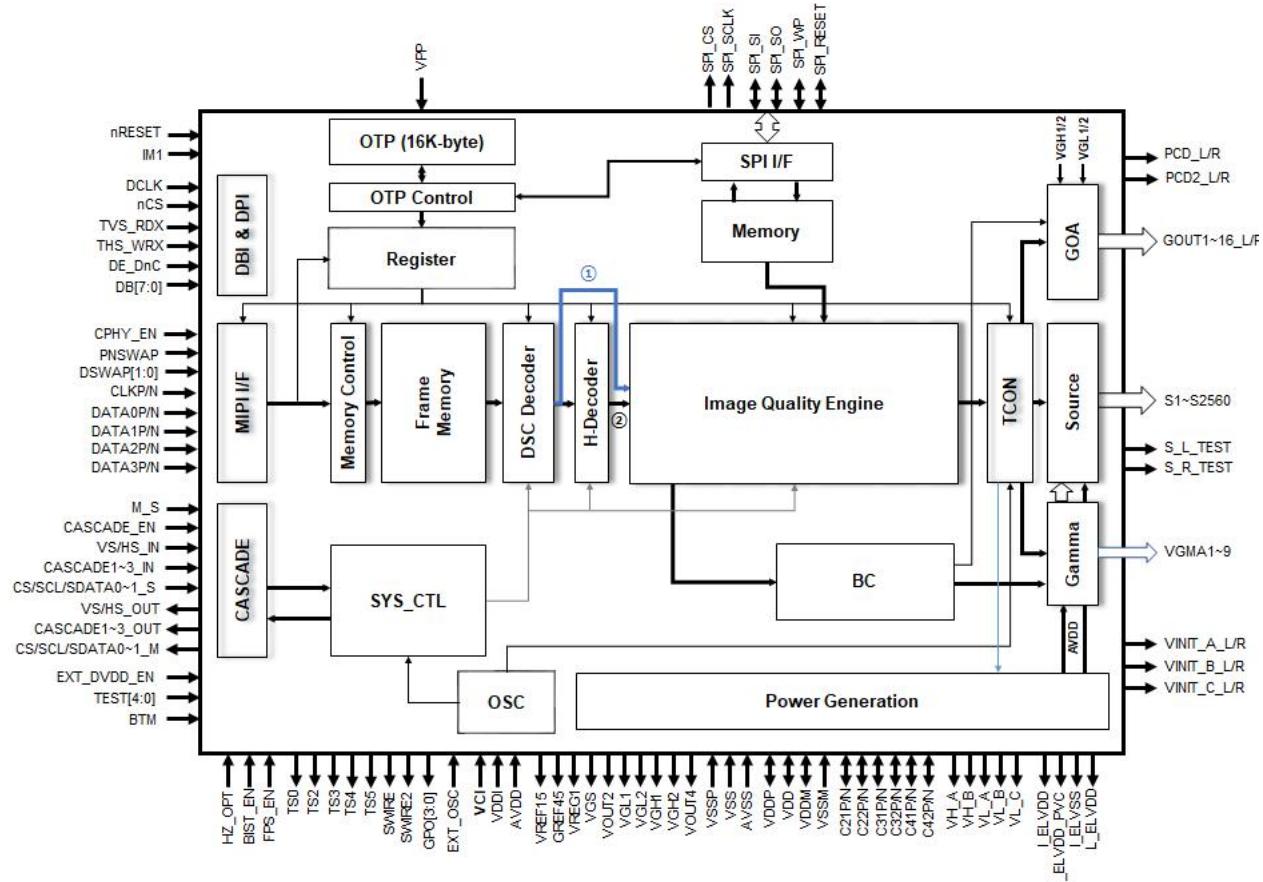
VL_C	<ul style="list-style-type: none"> -6.0V ~ -0.5V (Typ. -3.0V, Step: 0.1V) The OLED pixel reference voltage
VINIT_A	<ul style="list-style-type: none"> -6.0V ~ 6.0V (Typ. -3.0V, Step: 0.1V) The OLED pixel reference voltage
VINIT_B	<ul style="list-style-type: none"> -6.0V ~ 6.0V (Typ. -3.0V, Step: 0.1V) The OLED pixel reference voltage
VINIT_C	<ul style="list-style-type: none"> -6.0V ~ -0.5V (Typ. -3.0V, Step: 0.1V) The OLED pixel reference voltage
I_ELVDD	<ul style="list-style-type: none"> 2.6V ~ 5.7V (Typ. 4.6V, Step: 0.1V) The ELVDD voltage for AOD mode
I_ELVSS	<ul style="list-style-type: none"> -5.0V ~ -0.5V (Typ. -1.5V, Step: 0.1V) The ELVSS voltage for AOD mode
VREG1	<ul style="list-style-type: none"> 4.5V ~ 7.6V (Typ. 6.5V, Step: 0.02V) Regulator output voltage generated from AVDD for high voltage of gamma circuit.
VGS	<ul style="list-style-type: none"> 0.5V ~ 5.6V (Typ. 2.0V, Step: 0.02V) Regulator output voltage generated from AVDD for low voltage of gamma circuit.

■ Category: Non-Volatile Memory (NVM)

Items	Description
Size	<ul style="list-style-type: none"> 16K-byte One-Time Programmable (OTP) NVM
ID1	<ul style="list-style-type: none"> OTP 8 times
ID2, ID3	<ul style="list-style-type: none"> OTP 3 times
MIPI	<ul style="list-style-type: none"> OTP 1 times & Flash
TCON	<ul style="list-style-type: none"> OTP 1 times & Flash
DSC	<ul style="list-style-type: none"> OTP 1 times & Flash
DGM, PIC	<ul style="list-style-type: none"> OTP 1 times & Flash
BC (Band value)	<ul style="list-style-type: none"> Flash only
PWM	<ul style="list-style-type: none"> OTP 1 times & Flash
CASCADE	<ul style="list-style-type: none"> OTP 1 times & Flash
ODC, CTB	<ul style="list-style-type: none"> OTP 1 times & Flash
SPR	<ul style="list-style-type: none"> OTP 1 times & Flash
RN	<ul style="list-style-type: none"> OTP 1 times & Flash
POC	<ul style="list-style-type: none"> OTP 1 times & Flash
DEMURA	<ul style="list-style-type: none"> OTP 1 times & Flash
IE	<ul style="list-style-type: none"> OTP 1 times & Flash
BOIS_IP	<ul style="list-style-type: none"> OTP 1 times & Flash

3. Device Overview

3.1 Functional Block Diagram of the IC



4. Description of Pins

4.1 Pins for Power Supply

Symbol	I/O	Description
VDDI	P	<ul style="list-style-type: none"> Power supply to I/O 1.65 ~ 1.95V (Typ 1.8V) Connect a stabilizing capacitor
VCI	P	<ul style="list-style-type: none"> Power supply to analog power for the DDIC use 2.65 ~ 3.6V (Typ 3.0V) Connect a stabilizing capacitor
AVDD	P	<ul style="list-style-type: none"> Power supply to analog power for the DDIC use 6.0 ~ 8.0V (Typ 7.3V) Connect a stabilizing capacitor
VDD	P	<ul style="list-style-type: none"> Power supply to logic power 1.05 ~ 1.25V (Typ 1.15V)
VPP	P	<ul style="list-style-type: none"> Power supply for internal OTP programming 5.75 ~ 6.25V (Typ 6.0V) Leave it open when not used.
VSS	P	Ground for overall system except reference voltage generation block
AVSS	P	Ground for analog reference voltage generation block
VSSM	P	Ground for MIPI-PHY block reference voltage generation block
VSSP	P	Ground for OSC block

4.2 Pins for MIPI Interface

Symbol	I/O	Description
CLKP CLKN	I	<ul style="list-style-type: none"> DSI CLK+/- differential clock signals When IC enters to DSTB mode, please keep these pins to low Should be connected to VSSM when not used
DATA0P DATA0N	I/O	
DATA1P DATA1N	I/O	<ul style="list-style-type: none"> DSI D0~D3+/- differential data signals When IC enters to DSTB mode, please keep these pins to low Should be connected to VSSM when not used
DATA2P DATA2N	I/O	
DATA3P DATA3N	I/O	

4.3 Pins for SPI Interface

- These pins are used to read and write the Flash-Memory.

Symbol	I/O	Description
F_SPI_CS	O	<ul style="list-style-type: none"> • Chip Select • Leave it open when not used
F_SPI_SCLK	O	<ul style="list-style-type: none"> • A synchronous clock signal • Leave it open when not used
F_SPI_SI	I/O	<ul style="list-style-type: none"> • Serial Data Input • Leave it open when not used
F_SPI_SO	I/O	<ul style="list-style-type: none"> • Serial Data Output • Leave it open when not used
F_SPI_WP	I/O	<ul style="list-style-type: none"> • Write Protection (active low) • Leave it open when not used
F_SPI_RESET	I/O	<ul style="list-style-type: none"> • Reset • Leave it open when not used

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4.4 Pins for Interface Logic Control

Symbol	I/O	Description																																																																																																																																																																																																																																																																																																																																			
nRESET	I	<ul style="list-style-type: none"> This signal will reset the device and must be applied to properly initialize the chip. Signal is active low. There is no internal pull up resistor for this pin. 																																																																																																																																																																																																																																																																																																																																			
IM1	I	<ul style="list-style-type: none"> Interface Mode Selection <ul style="list-style-type: none"> 0 : MIPI I/F (Default) 1 : For Test 																																																																																																																																																																																																																																																																																																																																			
PSWAP	I	<ul style="list-style-type: none"> MIPI lane swap selection of Lane polarity <ul style="list-style-type: none"> 1 : P→P, N→N (Default) 0 : P→N, N→P 																																																																																																																																																																																																																																																																																																																																			
DSWAP [1:0]	I	<table border="1"> <thead> <tr> <th colspan="3">PIN option</th> <th colspan="9">IC PAD</th> </tr> <tr> <th>CPHY_EN</th> <th>PSWAP</th> <th>DSWAP [1:0]</th> <th>D3P (3+)</th> <th>D3N (3-)</th> <th>D0P (0+)</th> <th>D0N (0-)</th> <th>CP (C+)</th> <th>CN (C-)</th> <th>D1P (1+)</th> <th>D1N (1-)</th> <th>D2P (2+)</th> <th>D2N (2-)</th> </tr> </thead> <tbody> <tr> <td rowspan="4">0</td> <td rowspan="4">0</td> <td>00</td> <td>0-</td> <td>0+</td> <td>1-</td> <td>1+</td> <td rowspan="4">C-</td> <td rowspan="4">C+</td> <td>2-</td> <td>2+</td> <td>3-</td> <td>3+</td> </tr> <tr> <td>01</td> <td>2-</td> <td>2+</td> <td>1-</td> <td>1+</td> <td>0-</td> <td>0+</td> <td>3-</td> <td>3+</td> </tr> <tr> <td>10</td> <td>3-</td> <td>3+</td> <td>2-</td> <td>2+</td> <td>1-</td> <td>1+</td> <td>0-</td> <td>0+</td> </tr> <tr> <td>11</td> <td>3-</td> <td>3+</td> <td>0-</td> <td>0+</td> <td>1-</td> <td>1+</td> <td>2-</td> <td>2+</td> </tr> <tr> <td rowspan="4">0</td> <td rowspan="4">1</td> <td>00</td> <td>0+</td> <td>0-</td> <td>1+</td> <td>1-</td> <td rowspan="4">C+</td> <td rowspan="4">C-</td> <td>2+</td> <td>2-</td> <td>3+</td> <td>3-</td> </tr> <tr> <td>01</td> <td>2+</td> <td>2-</td> <td>1+</td> <td>1-</td> <td>0+</td> <td>0-</td> <td>3+</td> <td>3-</td> </tr> <tr> <td>10</td> <td>3+</td> <td>3-</td> <td>2+</td> <td>2-</td> <td>1+</td> <td>1-</td> <td>0+</td> <td>0-</td> </tr> <tr> <td>11</td> <td>3+</td> <td>3-</td> <td>0+</td> <td>0-</td> <td>1+</td> <td>1-</td> <td>2+</td> <td>2-</td> </tr> <tr> <td rowspan="4">1</td> <td rowspan="4">0</td> <td>00</td> <td>C1</td> <td>B1</td> <td>A1</td> <td>C2</td> <td>B2</td> <td>A2</td> <td>X</td> <td>C0</td> <td>B0</td> <td>A0</td> </tr> <tr> <td>01</td> <td>C0</td> <td>B0</td> <td>A0</td> <td>C2</td> <td>B2</td> <td>A2</td> <td>X</td> <td>C1</td> <td>B1</td> <td>A1</td> </tr> <tr> <td>10</td> <td>C2</td> <td>B2</td> <td>A2</td> <td>C1</td> <td>B1</td> <td>A1</td> <td>X</td> <td>C0</td> <td>B0</td> <td>A0</td> </tr> <tr> <td>11</td> <td>C0</td> <td>B0</td> <td>A0</td> <td>C1</td> <td>B1</td> <td>A1</td> <td>X</td> <td>C2</td> <td>B2</td> <td>A2</td> </tr> <tr> <td rowspan="4">1</td> <td rowspan="9">1</td> <td>00</td> <td>A1</td> <td>B1</td> <td>C1</td> <td>A2</td> <td>B2</td> <td>C2</td> <td>X</td> <td>A0</td> <td>B0</td> <td>C0</td> </tr> <tr> <td>01</td> <td>A0</td> <td>B0</td> <td>C0</td> <td>A2</td> <td>B2</td> <td>C2</td> <td>X</td> <td>A1</td> <td>B1</td> <td>C1</td> </tr> <tr> <td>10</td> <td>A2</td> <td>B2</td> <td>C2</td> <td>A1</td> <td>B1</td> <td>C1</td> <td>X</td> <td>A0</td> <td>B0</td> <td>C0</td> </tr> <tr> <td>11</td> <td>A0</td> <td>B0</td> <td>C0</td> <td>A1</td> <td>B1</td> <td>C1</td> <td>X</td> <td>A2</td> <td>B2</td> <td>C2</td> </tr> <tr> <td colspan="3">LANE_SEL[1:0]</td><td colspan="6">D-PHY</td><td colspan="5">C-PHY</td></tr> <tr> <td colspan="3">00</td><td colspan="6">CP/CN, D0N/D0P</td><td colspan="5">A0/B0/C0</td></tr> <tr> <td colspan="3">01</td><td colspan="6">CP/CN, D0N/D0P, D1N/D1P</td><td colspan="5">A0/B0/C0, A1/B1/C1</td></tr> <tr> <td colspan="3">10</td><td colspan="6">CP/CN, D0N/D0P, D1N/D1P, D2N/D2P</td><td colspan="5" rowspan="6">A0/B0/C0, A1/B1/C1, A2/B2/C2</td></tr> <tr> <td colspan="3">11</td><td colspan="11" rowspan="5">CP/CN, D0N/D0P, D1N/D1P, D2N/D2P, D3N/D3P</td></tr> <tr> <td>EXT_DVDD_EN</td><td>I</td><td colspan="12"> <ul style="list-style-type: none"> VDD Power Mode Selection <ul style="list-style-type: none"> 0 : Internal VDD mode (Default), 1 : External VDD mode </td></tr> <tr> <td>SWIRE2</td><td>O</td><td colspan="12"> <ul style="list-style-type: none"> Swire protocol setting pin of Power IC (ELVSS, ELVDD) Leave it open when not used </td></tr> <tr> <td>SWIRE</td><td>O</td><td colspan="12"> <ul style="list-style-type: none"> Power IC enable control pin (AVDD) Leave it open when not used </td></tr> <tr> <td>GPO[3:0]</td><td>O</td><td colspan="12"> <ul style="list-style-type: none"> Default setting: GPO[0]=Vsync; GPO[1]=Hsync; GPO[2]=TE; GPO[3]=Error Flag activated and selected by register command. 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*NOTE: "1" = VDDI level, "0" = VSS level.

4.5 Pins for Analog Output of OLED Display Driving

Symbol	I/O	Description
S<1> ~ S<2560>	O	<ul style="list-style-type: none"> • Source driver output pins
GOUT1_L ~ GOUT16_L	O	<ul style="list-style-type: none"> • Panel control pins from GOA driver
GOUT1_R ~ GOUT16_R	O	<ul style="list-style-type: none"> • Panel control pins from GOA driver
VINIT_A_L/R	O	<ul style="list-style-type: none"> • Initial voltage or reference voltage used for OLED panel. • This pad can be output VH_A or VL_A voltage. • If not used, please open these pins
VINIT_B_L/R	O	<ul style="list-style-type: none"> • Initial voltage or reference voltage used for OLED panel. • This pad can be output VH_B or VL_B voltage. • If not used, please open these pins
VINIT_C_L/R	O	<ul style="list-style-type: none"> • Initial voltage or reference voltage used for OLED panel. • This pad can be output VL_C voltage. • If not used, please open these pins
S_L/R_TEST	O	<ul style="list-style-type: none"> • Source output monitoring pad for test purpose, activated by command. • If not used, please open these pins

4.6 Pins for DC/DC Convert Pins

Symbol	I/O	Description
VGH1	O	<ul style="list-style-type: none"> • LDO output used for GOA • Connect a stabilizing capacitor
VGH2	O	<ul style="list-style-type: none"> • LDO output used for GOA • Connect a stabilizing capacitor
VDD	O	<ul style="list-style-type: none"> • LDO output used for logic circuit • Connect a stabilizing capacitor
VDDM	O	<ul style="list-style-type: none"> • LDO output used for MIPI block • Connect a stabilizing capacitor
VDDP	O	<ul style="list-style-type: none"> • LDO output used for OSC block • Connect a stabilizing capacitor
VH_A	O	<ul style="list-style-type: none"> • Internal regulator output for panel • Connect a stabilizing capacitor • If not used, please open these pins
VL_A	O	<ul style="list-style-type: none"> • Internal regulator output for panel • Connect a stabilizing capacitor • If not used, please open these pins
VH_B	O	<ul style="list-style-type: none"> • Internal regulator output for panel • Connect a stabilizing capacitor • If not used, please open these pins
VL_B	O	<ul style="list-style-type: none"> • Internal regulator output for panel • Connect a stabilizing capacitor • If not used, please open these pins
VL_C	O	<ul style="list-style-type: none"> • Internal regulator output for panel • Connect a stabilizing capacitor • If not used, please open these pins
VREG1	O	<ul style="list-style-type: none"> • LDO output used for source driver grayscale reference voltage. • Connect a stabilizing capacitor

VGS	O	<ul style="list-style-type: none"> LDO output used for source driver grayscale reference voltage. Connect a stabilizing capacitor
VREF15	O	<ul style="list-style-type: none"> LDO output for internal reference voltage Connect a stabilizing capacitor
GREF45	O	<ul style="list-style-type: none"> LDO output for internal reference voltage Connect a stabilizing capacitor
L_ELVDD	O	<ul style="list-style-type: none"> Internal regulator output for panel Connect a stabilizing capacitor
I_ELVDD	O	<ul style="list-style-type: none"> Internal regulator output for panel Connect a stabilizing capacitor
I_ELVSS	O	<ul style="list-style-type: none"> Internal regulator output for panel Connect a stabilizing capacitor
VGL1	O	<ul style="list-style-type: none"> Output voltage from step-up circuit which generate VGL1 Connect a stabilizing capacitor
VGL2	O	<ul style="list-style-type: none"> LDO output used for GOA Connect a stabilizing capacitor
VOUT2	O	<ul style="list-style-type: none"> Output voltage from step-up circuit which generate VOUT2 Connect a stabilizing capacitor
VOUT4	O	<ul style="list-style-type: none"> Output voltage from step-up circuit which generate VOUT4 Connect a stabilizing capacitor
C21P / C21N	O	<ul style="list-style-type: none"> Capacitor connection pins for the step-up circuit which generate VOUT2
C22P / C22N	O	
C31P / C31N	O	
C32P / C32N	O	<ul style="list-style-type: none"> Capacitor connection pins for the step-up circuit which generate VGL
C41P / C41N	O	
C42P / C42N	O	<ul style="list-style-type: none"> Capacitor connection pins for the step-up circuit which generate VOUT4

4.7 Test Pins

Symbol	I/O	Description
PCD_L PCD_R	O	<ul style="list-style-type: none"> • PCD pins for measuring panel resistor. • Leave them open when not used. • Connect a stabilizing capacitor.
PCD2_L PCD2_R	O	<ul style="list-style-type: none"> • PCD2 pins for measuring panel resistor. • Leave them open when not used.
TEST[4:0], TS0,2,5	I	<ul style="list-style-type: none"> • Test pins, not accessible to user. • Must be floating for normal using.
TS3,4	O	<ul style="list-style-type: none"> • Test pins, not accessible to user. • Must be floating for normal using.
EXT_OSC	I	<ul style="list-style-type: none"> • Test pins, not accessible to user. • Must be Connected to floating or VSS for normal using
DCLK	I	<ul style="list-style-type: none"> • Pixel-clock • Should be connected to floating when not used
DB[7:0]	I/O	<ul style="list-style-type: none"> • Bi-directional data bus for DBI interface and DPI interface • Used for DPI-I/F or DBI-I/F • Leave it open when not used
TVS_RDX	I	<ul style="list-style-type: none"> • Read strobe (active low) • Used for DBI-I/F • Should be connected to VDDI or floating when not used
THS_WRX	I	<ul style="list-style-type: none"> • Write strobe (active low) • Should be connected to VDDI or floating when not used
DnC	I	<ul style="list-style-type: none"> • Data(high) or command(low) select • Should be connected to VDDI or floating when not used
nCS	I	<ul style="list-style-type: none"> • Chip select (active low) • Should be connected to VDDI or floating when not used
BTM	I	<ul style="list-style-type: none"> • Test pins, not accessible to user. • Must be Connected to DVSS for normal using
HZ_OPT	I	<ul style="list-style-type: none"> • Input pin to select discharge function for AVDD, ELVDD and ELVSS. • HZ_OPT=0 Discharge to GND during Reset Low / DSTB • HZ_OPT=1 Hi-Z during Reset Low / DSTB
BIST_EN	I	<ul style="list-style-type: none"> • Input pin for free-run mode control, internal weakly pull to DVSS. - BIST_EN=0: normal operation. - BIST_EN=1: free-run mode. • Leave it open or connected to DVSS for normal operation.
FPS_EN	I	<ul style="list-style-type: none"> •FPS_EN=0, FPS mode disable. •FPS_EN=1, FPS mode enable. •If not used, can be floating or connected to DVSS
CPHY_EN	I	<ul style="list-style-type: none"> •Input pin to select used MIPI interface. -CPHY_EN=0 MIPI D_PHY -CPHY_EN=1 MIPI C_PHY
CASCADE_EN M_S	I	<ul style="list-style-type: none"> •Input pins for driver IC application -CASCADE_EN=0; M_S=0 Single chip -CASCADE_EN=1; M_S=0 Cascade (Slave) -CASCADE_EN=1; M_S=1 Cascade (master)
I_ELVDD_PVC	I	<ul style="list-style-type: none"> •Input Pin to track ELVDD variation. •Connect to mid-end ELVDD from Panel. •If no used, please connect to U_ELVDD
VS_OUT/IN, HS_OUT/IN CASCADEx_OUT/IN	I/O	<ul style="list-style-type: none"> •Clock link pins when use cascade function. Leave them open when not used •Connect VS_OUT / IN together. Connect HS_OUT / IN together. •Connect CASCADEx_OUT and CASCADEx_IN together.

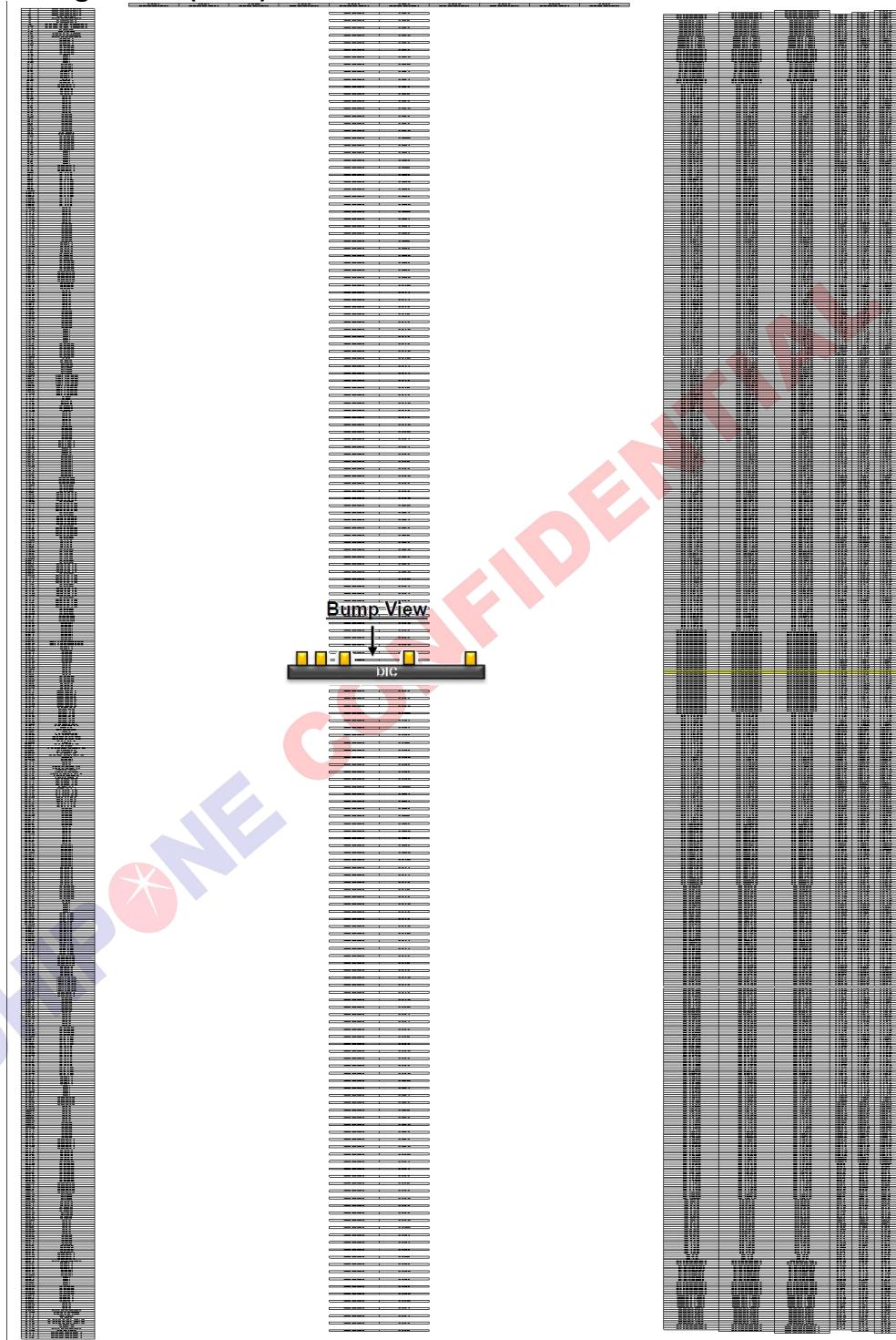
VGMA1~VGMA9		•Connect VGMAX of Master IC and Slave IC together.
CS_M/S, SCL_M/S, SDATA0_M/S, SDATA1_M/S	I/O	<ul style="list-style-type: none"> •Link pins when use cascade function. Leave them open when not used •Connect CS_M and CS_S together. Connect SCL_M and SCL_S together
TS7	O	• Dummy pin
VSSDUMMY	O	• Dummy pin
DUMMY_R1/R2	O	• SMT_L (Source output) and bonding res. for test pin
DUMMY_L3/L4	O	• SMT_R (Source output) and bonding res. for test pin
DUMMYO_R1/R2	O	• Dummy pin
DUMMYO_L3/L4	O	• Dummy pin
DUMMY_SL/SR	O	• Dummy pin
DUMMY	O	• Dummy pin

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5. PAD Specifications

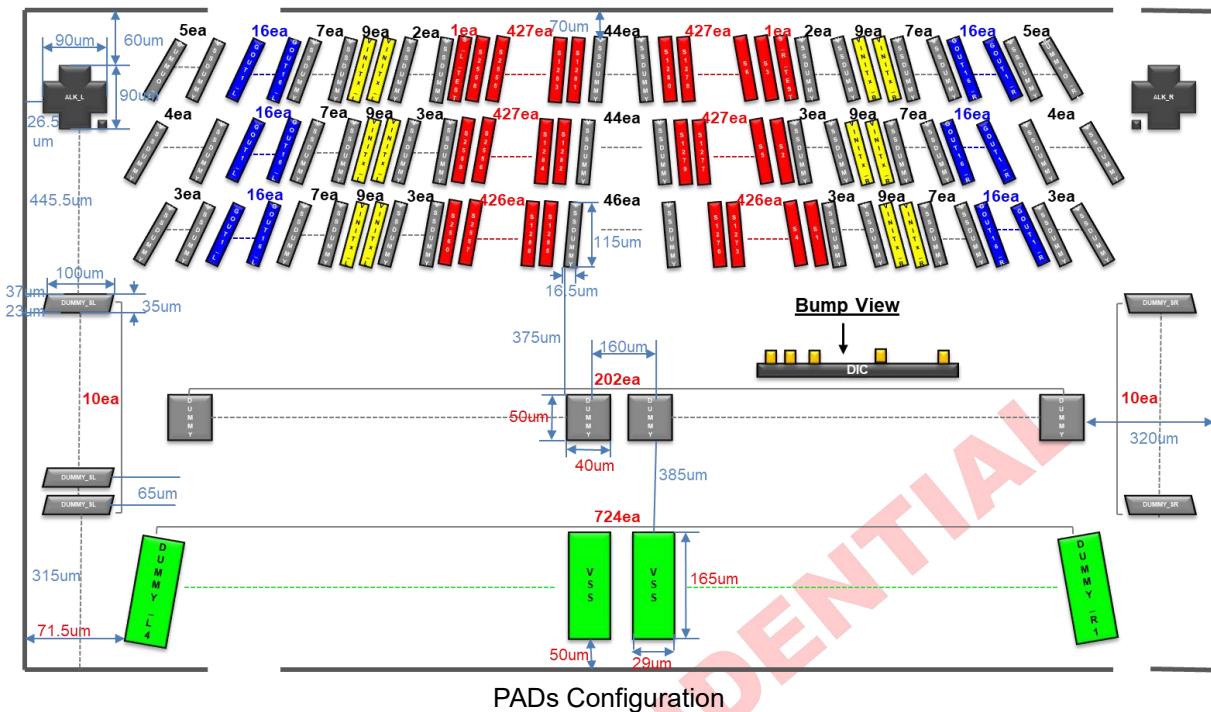
5.1 PAD Information

5.1.1 PAD Assignment (COP)



Pad Assignments

5.1.2 PAD Configuration(COP)



Refer to Section Pad Coordinates.

5.1.3 Bump Information

Bump Information

Item	Pad No.	Size		Unit
		X (Length)	Y (Width)	
Pad Pitch	Input side	29	165	μm
	Output side1	16.5	115	
	Output side2	16.5	115	
	Output side3	16.5	115	
	Short Side	100	35	
	Center Side	40	50	
Bump Pad Height	Height	12um		
	Tolerance in chip	±2um		
Bump Dimple Height	-	TBD		
Chip thickness	-	Based on customer's requirement		

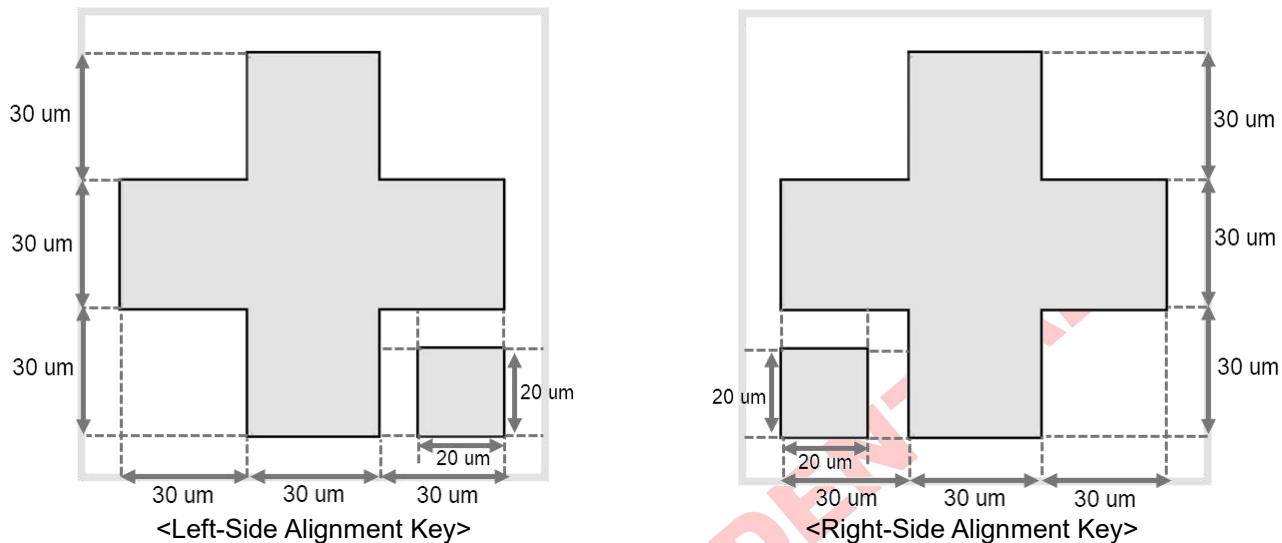
***NOTE:**

1. Dimension of bump pad size is based on bump TOP size.
2. Wafer thickness can be varied based on the customer's requirement.

5.1.4 Bump Dimension

*NOTE: To get more detailed information for ICNA3512 bump pads arrangement and dimensions, please refer to the bump layout file, "ICNA3512_COP_BUMP.DXF".

5.1.5 Alignment Key



Alignment Key Coordinates

Item	Coordinates		Unit
	X	Y	
Left-side alignment key (Top)	-16348.5	670.5	μm
Right-side alignment key (Top)	16348.5	670.5	

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

It defines the maximum operating conditions for the DDIC device. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage for I/O	VDDI ~ VSS	TBD	V
LDO Output	VDD ~ VSS	TBD	V
LDO Output	VDDM ~ VSS	TBD	V
LDO Output	VDDP ~ VSSP	TBD	V
LDO Output	VH_A/B ~ AVSS	TBD	V
LDO Output	AVSS ~ VL_A/B	TBD	V
LDO Output	AVSS ~ VL_C	TBD	V
Supply Voltage for Analog	VCI ~ AVSS	TBD	V
Supply Voltage for Analog	AVDD ~ AVSS	TBD	V
Step-up Circuit	VOUT2 ~ AVSS	TBD	V
LDO Output	VGH ~ AVSS	TBD	V
Regulator Output	I_ELVDD ~ AVSS	TBD	V
LDO Output	VREG1 ~ AVSS	TBD	V
LDO Output	VGS ~ AVSS	TBD	V
Step-up Circuit	AVSS ~ VOUT4	TBD	V
Regulator Output	AVSS ~ I_ELVSS	TBD	V
Output	AVSS ~ VINIT_C	TBD	V
Step-up Circuit	AVSS ~ VGL1	TBD	V
Restriction	VOUT2 ~ VGL1	TBD	V
	AVSS ~ VGL1	TBD	V
	VH_A/B ~ VL_A/B	TBD	V
Supply Voltage for OTP	VPP ~ VSS	TBD	V
MIPI Differential Input	CLKP/CLKN DATAnP/DATAnN ~ VSSM	-0.3 to + 1.8	V
Input Voltage Range	V _{in}	-0.3 to VDDI + 0.3	V
Output Voltage Range	V _o	-0.3 to VDDI + 0.3	V
Operating Temperature	T _{opr}	-40 to + 85	°C
Storage Temperature	T _{stg}	-55 to + 125	°C

***NOTE:**

1. Absolute maximum ratings are the limit value of operating. Beyond those ranges, the IC cannot guarantee the safety. Conditions outside the range listed in the above table may cause permanent damage to the device, may not be recovered.
2. Absolute voltages are referenced to ground.
3. DATAnP/DATAnN, n = 0, 1, 2 and 3.

***CAUTION:**

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

6.2 DC Electrical Characteristics

DC Characteristics for Power Supply Voltage						
Category	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage for I/O	VDDI	—	1.65	1.80	1.95	V
Supply Voltage for Analog	VCI	—	2.65	3.00	3.60	V
Supply Voltage for Analog	AVDD	—	6.00	7.30	8.00	V
Supply Voltage for OTP	VPP	—	5.75	6.0	6.25	V

*NOTE: $T_A = -40$ to 85°C

DC Characteristics for Generated Voltage						
Category	Symbol	Condition	MIN	TYP	MAX	Unit
LDO Output	VDD	-	1.05	1.15	1.25	V
LDO Output	VDDM	-	1.05	1.15	1.25	V
LDO Output	VDDP	-	1.05	1.15	1.25	V
LDO Output	VH_A/B	-	0.50	3.00	6.00	V
LDO Output	VL_A/B	-	-6.00	-3.00	-0.50	V
LDO Output	VL_C	-	-6.00	-3.00	-0.50	V
Step-up Circuit	VOUT2	-	7.50	8.00	15.00	V
Step-up Circuit	VGL1	-	-3.00	-7.00	-15.00	V
LDO Output	VGL2	-	-2.50	-6.50	-14.50	V
LDO Output	VGH1/2	-	3.00	7.00	14.50	V
Regulator Output	I(L)_ELVDD	-	2.60	4.60	5.70	V
LDO Output	VREG1	-	4.50	6.50	7.60	V
LDO Output	VGS	-	0.50	2.00	5.60	V
Step-up Circuit	VOUT4	-	-2.00	-4.00	-7.00	V
Regulator Output	I_ELVSS	-	-0.50	-1.50	-5.00	V
Regulator Output	VINIT_A/B	-	-6.00	-3.00	6.00	V
Regulator Output	VINIT_C	-	-0.50	-3.00	-6.00	V

*NOTE: $T_A = -40$ to 85°C

DC Characteristic for Interface Signals						
Category	Symbol	Condition	MIN	TYP	MAX	Unit
Logic High Level Input Voltage	V_{IH}	—	$0.8 \times VDDI$	—	VDDI	V
Logic Low Level Input Voltage	V_{IL}	—	VSS	—	$0.2 \times VDDI$	V
Logic High Level Output Voltage	V_{OH}	$I_{OUT} = -1\text{mA}$	$0.8 \times VDDI$	—	VDDI	V
Logic Low level Output Voltage	V_{OL}	$I_{OUT} = +1\text{mA}$	VSS	—	$0.2 \times VDDI$	V
Logic High Level Leakage	I_{IH}	$V_{IN} = VDDI$	—	—	1.00	μA
Logic Low Level Leakage	I_{IL}	$V_{IN} = VSS$	-1.00	—	—	μA

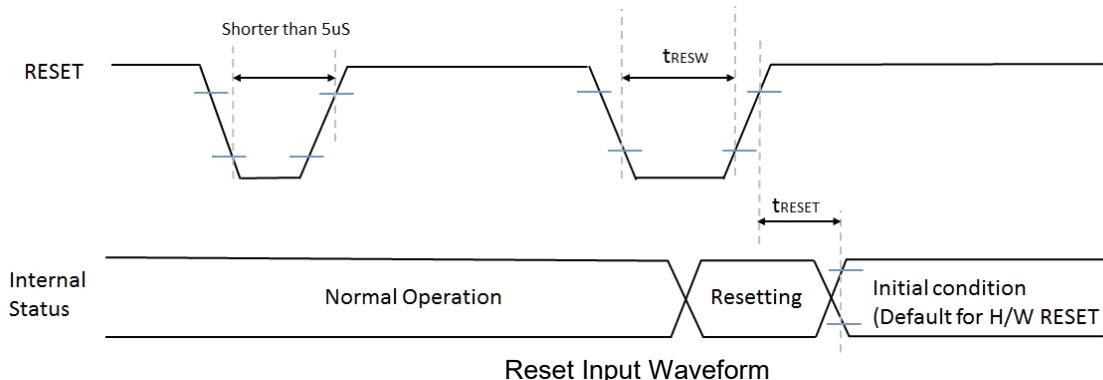
*NOTE: $T_A = -40$ to 85°C

DC Characteristic for Source Output						
Category	Symbol	Condition	MIN	TYP	MAX	Unit
Source Output Range	S<n>	—	0.70	—	7.60	V
Source Output Deviation: mean value (channel to channel)	V _{DEV,POS}	V _{SS} + 0.7 V < V _{SO} < AVDD – 0.5 V	—	—	TBD	mV

*NOTE: T_A = -40 to 85°C

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6.3 DC Characteristics for Reset



Reset Input Timing

Parameter	Symbol	Pin	Description	MIN	TYP	MAX	Unit
Reset low pulse width	t_{RESW}	nRESET		20	—	—	μs
Secure reset completion time	t_{RESET}	nRESET	Reset during Sleep In mode	—	—	5	ms
		nRESET	Reset during Sleep Out mode	—	—	120	ms
Reset un-reacted pulse width		nRESET		—	—	5	μs

***NOTE:**

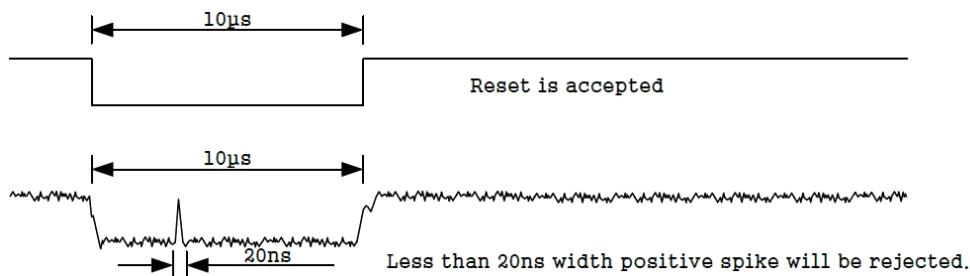
1. Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table as below.

RESET Pulse	
RESET Pulse	Action
Short than 5μs	Reset Rejected
Long than 20μs	Reset
Between 5μs and 20μs	Reset Start

2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

3. During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (t_{RESET}) within 5ms after a rising edge of RESET.

4. Spike Rejection also applies during a valid reset pulse as shown as below.



5. It is necessary to wait 5ms after releasing RESET before sending commands. Also Sleep Out command cannot be sent for 120m second.

6. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied. Internal PoR (Power-on Reset) circuit generates a reset signal within 1ms after VDDI and VCI rise up to 90% of their typical value. It is necessary to wait 5m second after Power-on reset before sending commands; this is to allow time for OTP loading.

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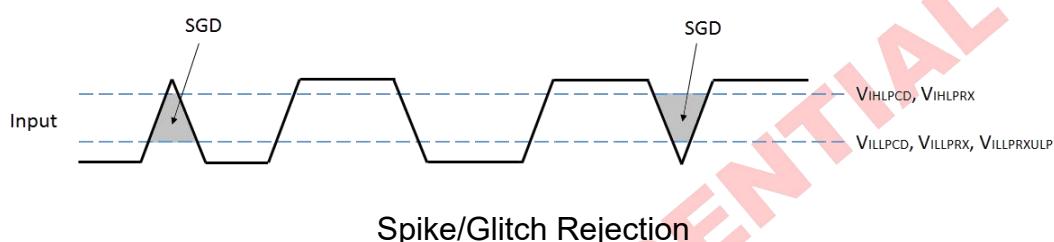
6.4 MIPI DSI Characteristics

6.4.1 DC Characteristics for MIPI DSI LP Mode

DC Characteristics for MIPI DSI LP Mode

Parameter	Symbol	Condition	Specification			Unit	Note
			MIN	TYP	MAX		
Logic high level input voltage	V_{IHLPCD}	LP-CD	450		1250	mV	
Logic Low level input voltage	V_{ILLPCD}	LP-CD			200	mV	
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK,D0)	740		1250	mV	
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK,D0)			550	mV	
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)			300	mV	
Logic high level input voltage	V_{OHLPTX}	LP-TX(D0)	1.1		1.25	V	
Logic Low level input voltage	V_{OLLPTX}	LP-TX(D0)	-50		50	mV	
Input pulse rejection	SGD	DSI-CLKP/N,DSI-DnP/N			300	Vps	1

*Note: Peak interference amplitude max. is 200mV, and interference frequency min. is 450MHz.



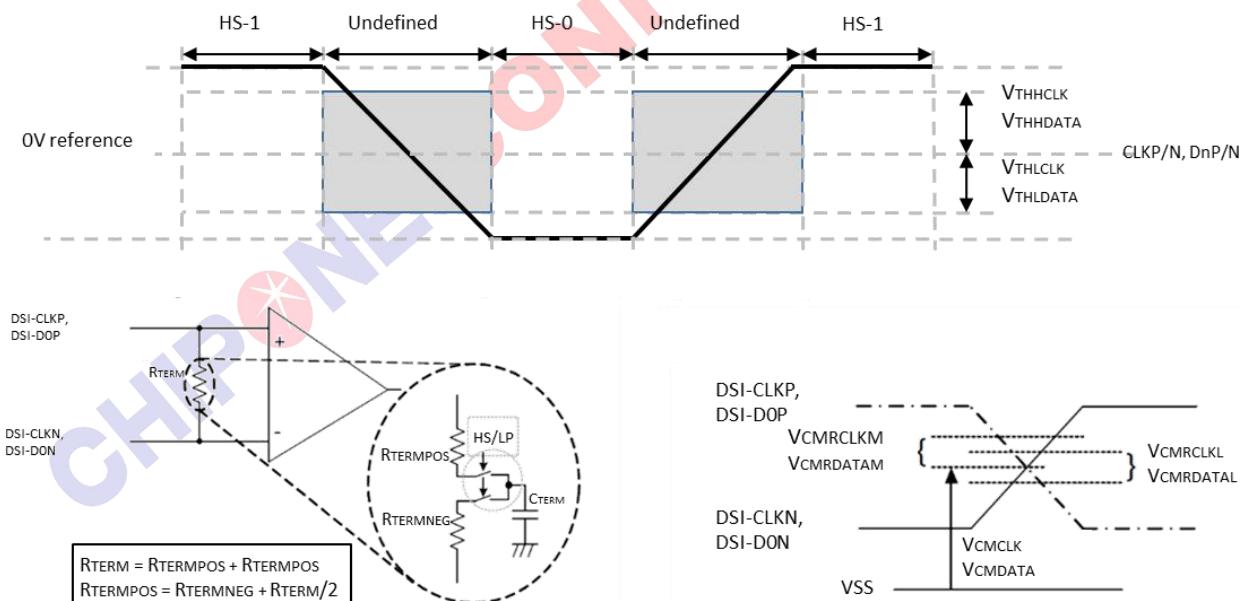
6.4.2 DC Characteristics for MIPI DSI HS Mode

DC Characteristics for MIPI DSI HS Mod

Parameter	Symbol	Condition	Specification			Unit	Note
			MIN	TYP	MAX		
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	CLKP/N, DnP/N	70		330	mV	1,2
Input voltage common mode variation ($\leq 450\text{MHz}$)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	CLKP/N, DnP/N	-50		50	mV	3
Input voltage common mode variation ($\geq 450\text{MHz}$)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	CLKP/N, DnP/N			100	mV	
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	CLKP/N, DnP/N	-70			mV	
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	CLKP/N, DnP/N			70	mV	
Single-ended input low voltage	V_{ILHS}	CLKP/N, DnP/N	-40			mV	2
Single-ended input high voltage	V_{IHHS}	CLKP/N, DnP/N			460	mV	2
Differential input termination resistor	R_{TERM}	CLKP/N, DnP/N	80	100	125	Ω	
Single-ended threshold voltage for termination enable	V_{TERM_EN}	CLKP/N, DnP/N			450	mV	
Termination capacitor	C_{TERM}	CLKP/N, DnP/N			60	pF	

*Note:

1. Includes 50mV (-50mV to 50mV) ground difference.
2. Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$.
3. Without 50mV (-50mV to 50mV) ground difference.
4. Dn = D0, D1, D2 and D3.

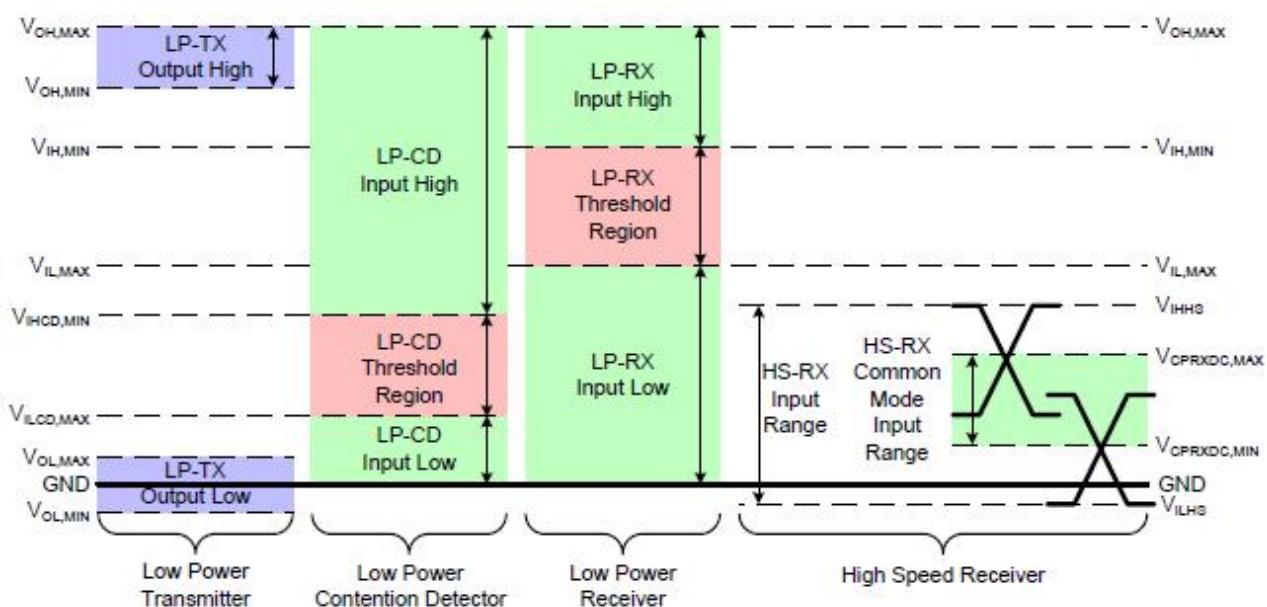


Differential voltage range, termination resistor and common mode voltage

6.4.3 DC Characteristics for C-PHY HS Mode

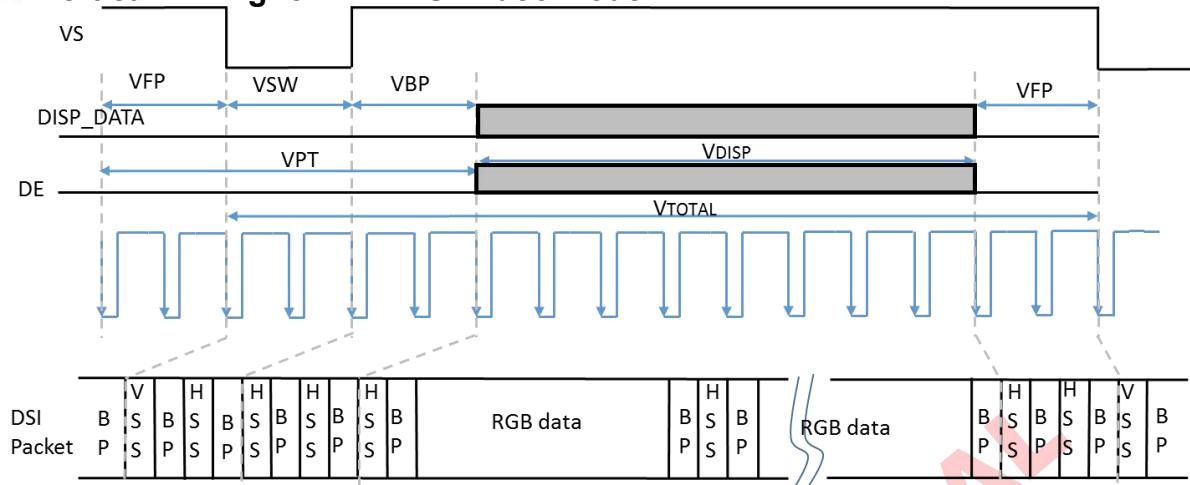
DC Characteristics for C-PHY HS Mode

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Single-end input high voltage	VIHHS	-	-	535	mV
Common mode voltage	VCMRXDC	95	-	390	mV
Differential input impedance	ZID_AB,ZID_BC,ZID_CA	80	100	120	Ω
Differential input high threshold	VIDTH	-	-	40	mV
Differential input low threshold	VIDTL	-40	-	-	mV
Single-end threshold for HS termination enable	VTERM-EN	-	-	450	mV



6.5 MIPI AC Timing Characteristics

6.5.1 Vertical Timing for MIPI DSI Video Mode

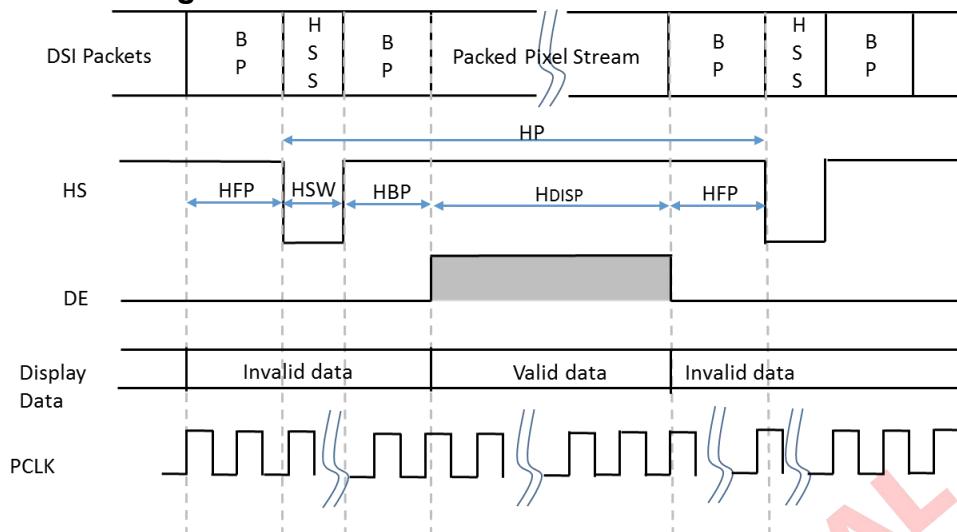


Vertical Timing for MIPI DSI Video Mode

Parameter	Symbol	Condition	Specification			Unit	Note
			MIN	TYP	MAX		
Vertical total	VTOTAL			2832		Line	
Vertical low pulse width	VSW			1		Line	1
Vertical front porch	VFP			16		Line	
Vertical back porch	VBP			15		Line	1
Vertical data start point		VSW+VBP		16		Line	1
Vertical blanking period	VPT	VSW+VBP+VFP		32		Line	
Vertical active area	VDISP			2800		Line	
Vertical frame rate	VFR			60		Hz	

*Note: The VSW and VBP pulse width are related to GOA timing. The GOA timing must be set at corresponding position for normal display.

6.5.2 Horizontal Timing for MIPI DSI Video Mode

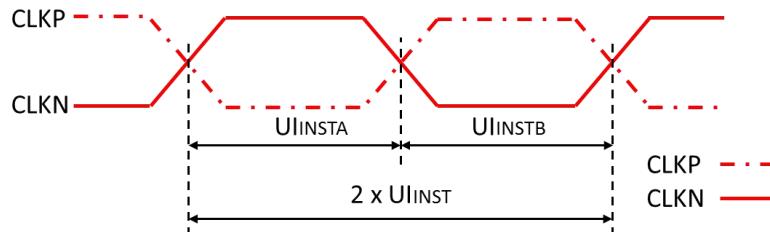


Horizontal Timing for MIPI DSI Video Mode

Parameter	Symbol	Condition	Specification			Unit	Note
			MIN	TYP	MAX		
HS low pulse width	HSW			TBD		nS	
Horizontal back porch	HBP			TBD		nS	
Horizontal front porch	HFP			TBD		nS	
Horizontal data start point		HSW+HBP		TBD		nS	
Horizontal blanking period	HBLK	HSW+HBP+HFP		TBD		nS	
Horizontal active area	HDISP			TBD		nS	

6.6 MIPI AC Characteristics

6.6.1 High-Speed Mode - Clock Timing

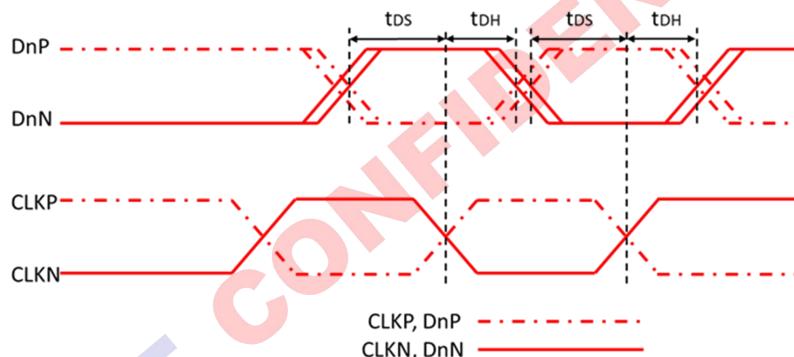


High-Speed Mode - Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Note
			MIN	TYP	MAX		
CLK P/N	$2 \times UI_{INST}$	Double UI instantaneous	1.54		25	nS	
CLK P/N	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	0.77		12.5	nS	1

*Note: UI = $UI_{INSTA} = UI_{INSTB}$.

6.6.2 High-Speed Mode - Clock / Data Timing

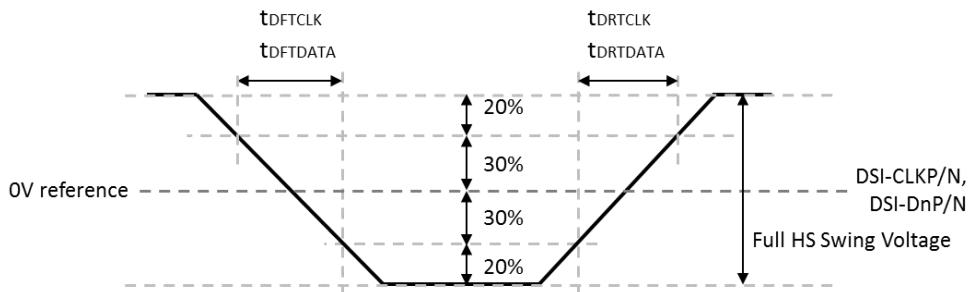


High-Speed Mode - Clock / Data Timing

Signal	Symbol	Parameter	Specification			Unit	Note
			MIN	TYP	MAX		
DnP/N	tds	Data to Clock Setup time	0.20*UI			UI	
	tDH	Clock to Data Hold time	0.20*UI			UI	

*Note: Dn = D0, D1, D2 and D3.

6.6.3 High-Speed Mode - Rising and Falling Timing



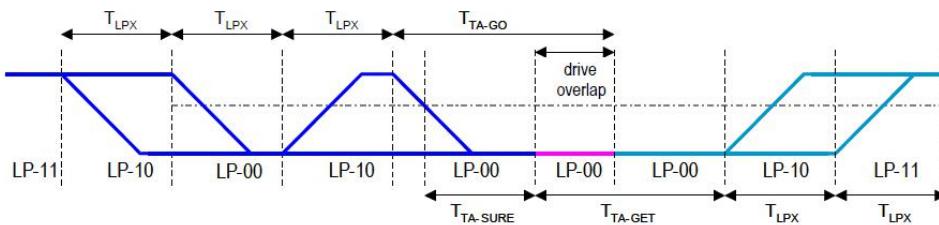
High-Speed Mode - Rising and Falling Timing

Parameter	Symbol	Conditions	Specification			Unit	Note
			MIN	TYP	MAX		
Differential Rise Time for Clock	tDRCLK	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	tDRDATA	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	tDFTCLK	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	tDFTDATA	DnP/N	150pS		0.3*UI		1,2,3

*Note:

1. DnP/N, n = 0, 1, 2 and 3.
2. The display module has to meet timing requirements, which are defined for the transmitter (AP) on MIPI D-PHY standard.
3. DSİ-CLKP = CLKP. DSİ-CLKN = CLKN.
4. DSİ-DnP = DnP, n = 0, 1, 2 and 3. DSİ-DnN = DnN, n = 0, 1, 2 and 3.

6.6.4 Low-Speed Mode - Bus Turn Around



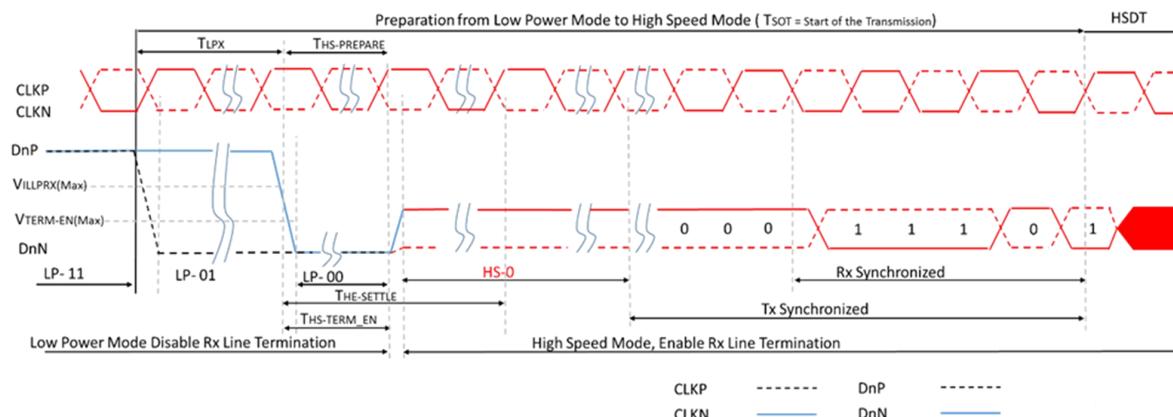
Bus Turn Around (BTA) Procedure

Low-Speed Mode - Bus Turn Around Timing

Signal	Symbol	Parameter	Specification			Unit	Note
			MIN	TYP	MAX		
D0P/N	T_{LPX}	Transmitted length of any Low-Power state period	50			nS	1
D0P/N	Ratio T_{LPX}	Ratio of $T_{LPX}(\text{MASTER})/T_{LPX}(\text{SLAVE})$ between Master and Slave side	2/3		3/2	-	1
D0P/N	T_{TA_SURE}	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		$2 * T_{LPX}$	nS	1
D0P/N	T_{TA_GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5 * T_{LPX}$			nS	1
D0P/N	T_{TA_GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4 * T_{LPX}$			nS	1

*Note: D0P = DS1-D0+, D0N = DS1-D0-.

6.6.5 Data Lanes from Low-Power Mode to High-Speed Mode

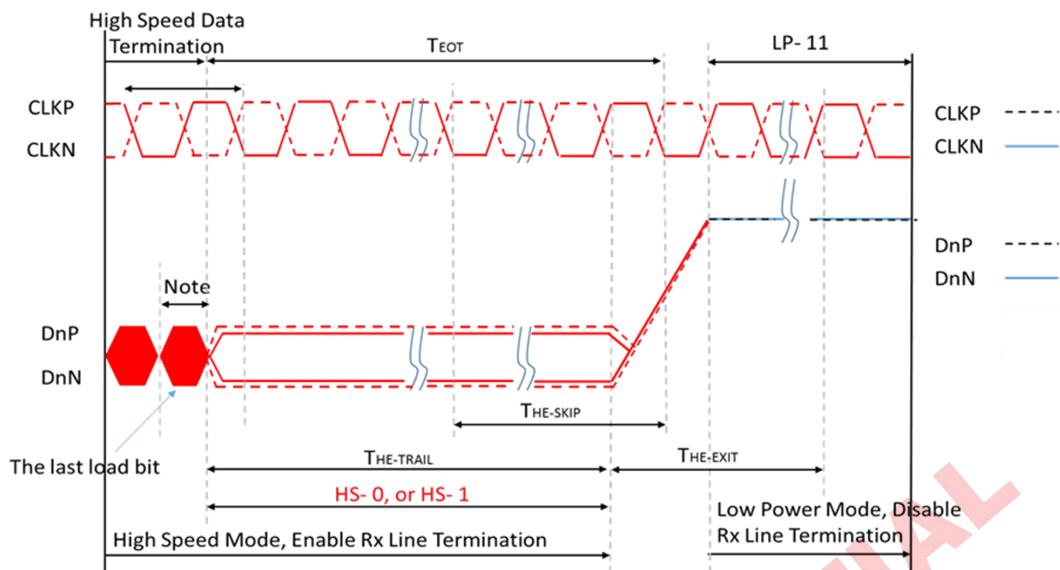


Data Lanes from Low-Power Mode to High-Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Note
			MIN	TYP	MAX		
DnP/N	T _{LPX}	Length of any Low Power State Period	50			nS	1
DnP/N	T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	T _{HS-TREM-EN}	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

*Note: DnP/N, n = 0, 1, 2 and 3.

6.6.6 Data Lanes from High-Speed Mode to Low-Power Mode



Note:

If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.

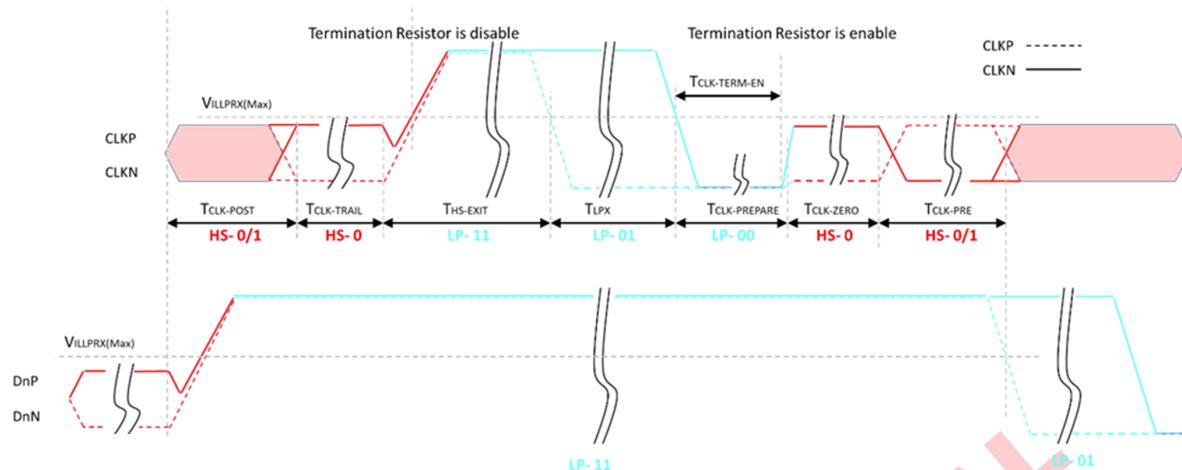
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0.

Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Note
			MIN	TYP	MAX		
DnP/N	T _{HS-SKIP}	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100			nS	1

*Note: DnP/N, n = 0, 1, 2 and 3.

6.6.7 DSI Clock Burst – High-Speed Mode to /from Low-Power Mode



DSI Clock Burst – High-Speed Mode to /from Low-Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Note
			MIN	TYP	MAX		
CLKP/N	T _{CLK-POST}	Time that the AP shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	TBD			nS	
CLKP/N	T _{CLK-TRAIL}	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CLKP/N	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100			nS	
CLKP/N	T _{CLK-PREPARE}	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CLKP/N	T _{CLK-TERM-EN}	Time-out at Clock Lane to enable HS termination			38	nS	
CLKP/N	T _{CLK-PREPARE+} T _{CLK-ZERO}	Minimum lead HS-0 drive period before starting Clock	300			nS	
CLKP/N	T _{CLK-PRE}	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8			UI	

*Note: DnP/N, n = 0, 1, 2 and 3.

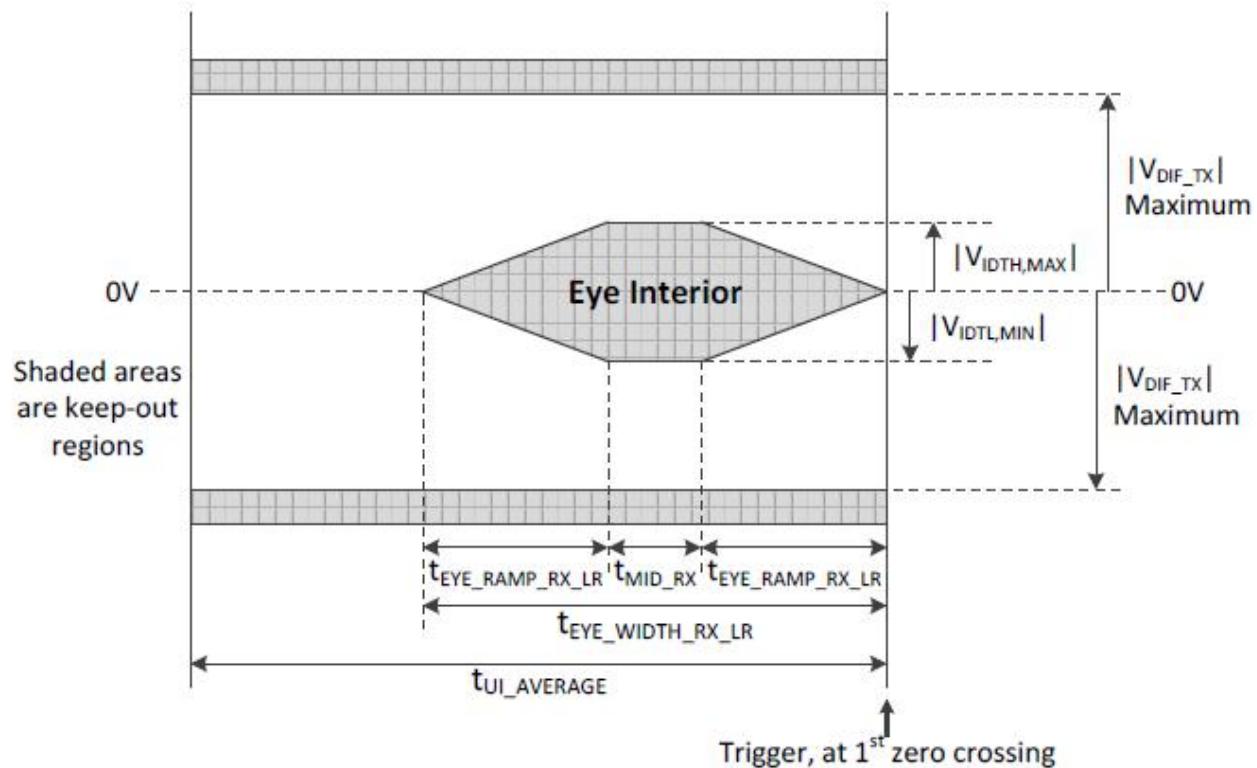
6.6.8 MIPI DSI2 Timing Characteristics

6.6.8.1 C-PHY High Speed Transmission

Symbol	Parameter	MIN	TYP	MAX	Unit
$t_{EYE_RAMP_RX_LR}$	Eye ramp time at the receive	0.25	-	-	UI
$t_{EYE_WIDTH_RX_LR}$	Eye width at the receive	0.5 (Note)	-	-	UI
U_{INST}	UI instantaneous	1	-	12.5	ns
$t_{UI_AVERAGE}$	UI average	-	U_{INST}	-	ns

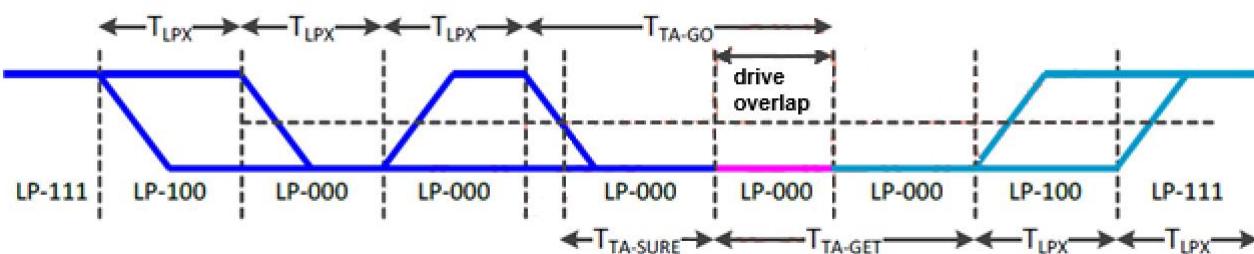
*Note : 1. $t_{EYE_WIDTH_RX_LR} = 2*t_{EYE_RAMP_RX_LR}+t_{MID_RX}$

2. $t_{MID_RX}=t_{UI_AVERAGE}-2500\text{ps}$, at $t_{UI_AVERAGE}>2.5\text{ns}\sim12.5\text{ns}$



6.6.8.2 C-PHY Low Power Mode

Symbol	Parameter	MIN	TYP	MAX	Unit
Turnaround Procedure					
T_{LPX}	Transmitted length of any Low-Power state period	50			ns
Ratio_ T_{LPX}	Ratio of $T_{LPX}(\text{MASTER})/T_{LPX}(\text{SLAVE})$ between Master and Slave side	2/3		3/2	
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		$2xT_{LPX}$	ns
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5xT_{LPX}$		ns
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4xT_{LPX}$		ns



6.6.8.3 C-PHY High Speed Transmission in Bursts

Symbol	Parameter	MIN	TYP	MAX	Unit
High Speed Data Transmission in Bursts					
t _{3-PREPARE}	Time that the transmitter drives the 3-wire LP-000 line state immediately before the start of the HS transmission	38	-	95	ns
t _{3-TERM-EN}	Time for the slave to enable the HS line termination, starting from the time point when the A, B and C wire cross V _{IL_MAX}	Note4	-	38	ns
t _{3-SETTLE}	Time interval during which the HS receiver should ignore any HS transitions on the lane, starting from the beginning of t _{3-PREPARE}	95	-	300	ns
t _{HS-EXIT}	Time that the transmitter drives LP-111 following a HS burst	100	-	-	ns
t _{LPX}	Length of any Low-Power state period	50	-	-	ns
t _{3-POST}	Time that the transmitter drives 4444444 after a HS burst	TBD	-	-	UI

*Note 1) The minimum value depends on the symbol rate.

Implementations should ensure proper operation for all the supported symbol rates.

*Note 2) UI means Unit Interval.

*Note 3) TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

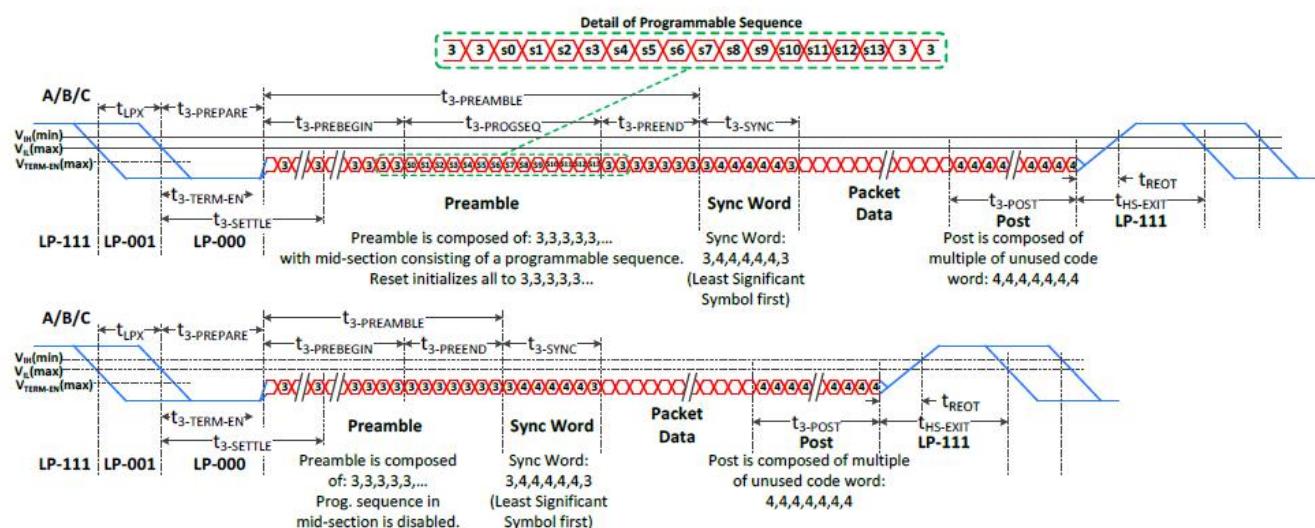
*Note 4) Receiver termination impedances shall not be enabled until the single-ended voltages on all of A, B and C fall below VTERM-EN .

t_{3-PREPARE} < t_{3-SETTLE} < t_{3-PREPARE} + t_{3-PREAMBLE}

t_{3-PREAMBLE} = t_{3-PREBEGIN} + t_{3-PROGSEQ} + t_{3-PREEND}

t_{3-PROGSEQ} = 14UI or 0UI

t_{3-SYNC} = 7UI



6.7 ESD Protection Level

ESD Protection Level

Model	JEDEC	Level
Human Body Mode (HBM)	JESD22-A114-F	$\geq \pm 3KV$
Charged Device Mode (CDM)	JESD22-C101-D	$\geq \pm 800V$
Latch-up		150mA or $1.5*VDD_{max}$
TLP		500V or 4A

6.8 Latch-Up Protection Level

The device will not latch up at trigger current level less than $\pm 150mA$. (EIA/JESD78C)

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7. Interface Description

7.1 Interface Mode Selection

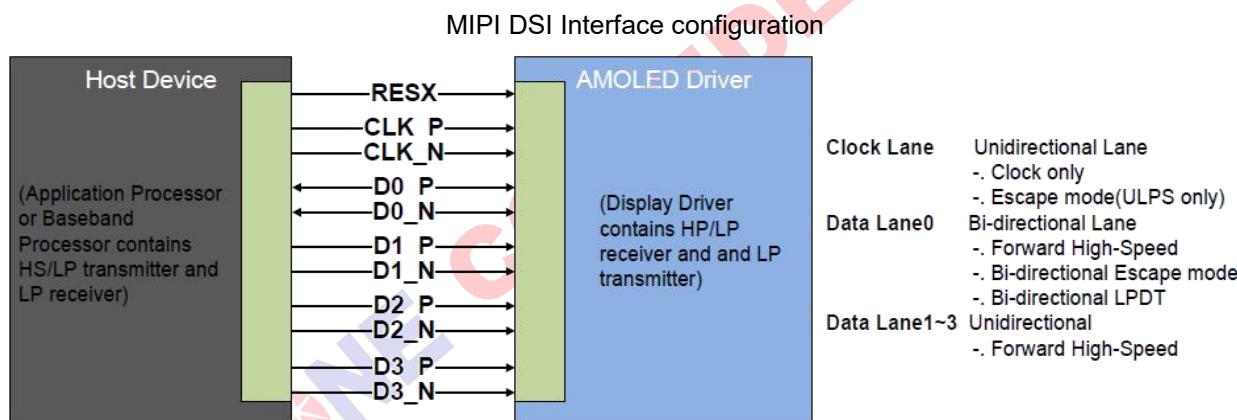
Following table shows the interface transfers instructions (include commands and parameters) and display data between the DDIC and the AP. This product supports the command transmission in MIPI mode through LPDT or HSDT.

Interface Mode Selection				
CPHY_EN	LANE_SEL[1:0]	Display Data transmitted by	Instruction transmitted by	Note
0	00	CP/CN, D0P/0N		
	01	CP/CN, D0P/D0N, D1P/D1N		-
	10	CP/CN, D0P/D0N, D1P/D1N, D2P/D2N		-
	11	CP/CN, D0P/D0N, D1P/D1N, D2P/D2N, D3P/D3N		Default
1	00	A0/B0/C0		-
	01	A0/B0/C0, A1/B1/C1		-
	1x	A0/B0/C0, A1/B1/C1, A2/B2/C2		Default

*Note: IM1 should be connect "0"

7.2 MIPI Display Serial Interface (DSI)

MIPI DSI standard defines protocols between a host processor and Client peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards. DSI specifies the interface between a host processor and a peripheral such as a display module. It builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DCS standards. The following figure shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface performs the same functions as interfaces based on similar parallel display interfaces. It sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals. From a system or software point of view, the serialization and deserialization operations should be transparent. The most visible, and unavoidable, consequence of transformation to serial data and back to parallel is increased latency for transactions that require a response from the peripheral. For example, reading a pixel from the frame buffer on a display module has a higher latency using DSI. Another fundamental difference is the host processor's inability during a read transaction to throttle the rate, or size, of returned data.



7.2.1 MIPI DSI Feature

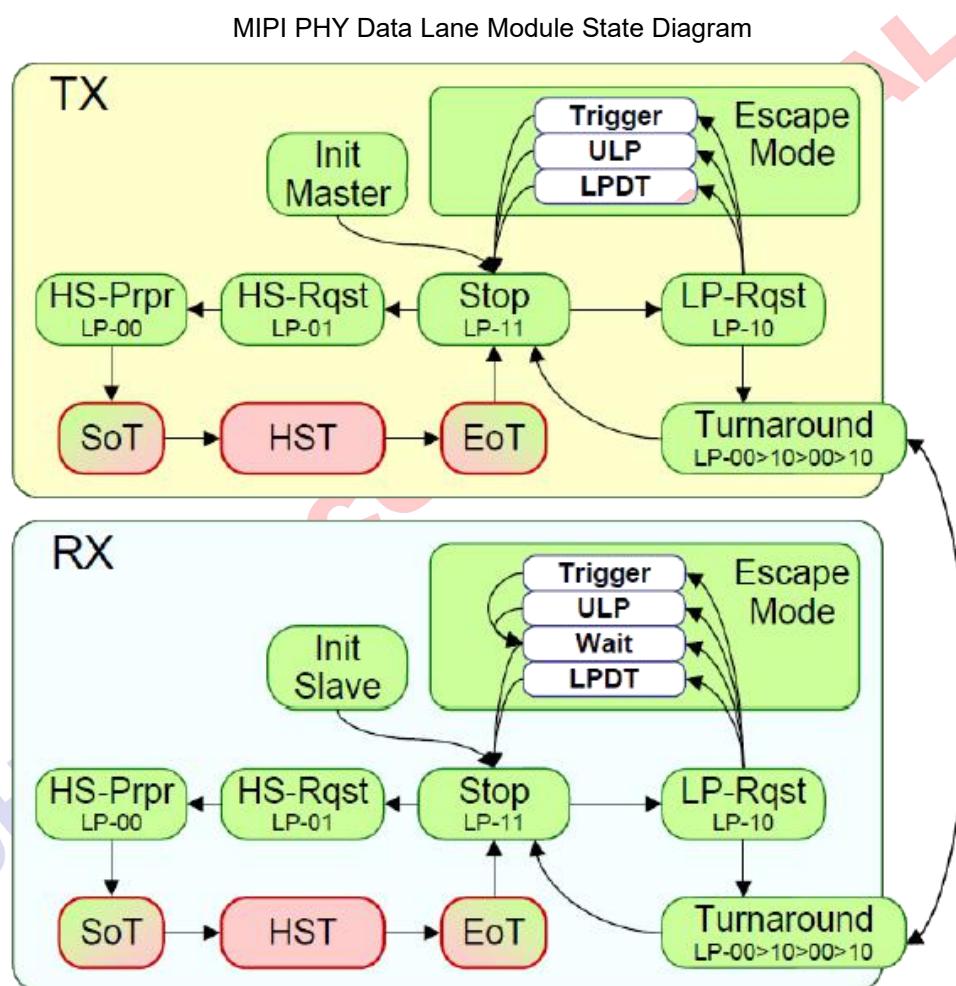
- 4 Data Lanes
- High Speed (HS) Transmission (Unidirectional)
- Low Power (LP) Transmission (Bidirectional)
- Command and Video modes are supported.
- Tearing effect (TE) signal is supported
- Diagnostic function – checksum and ECC error monitoring
- Functionality supported by Escape mode
- Packet-Based Protocol

7.2.2 MIPI DSI Physical Layer

The D-PHY provides a synchronous connection between master and slave. A practical PHY configuration consists of a clock signal and one or more data signals. The clock signal is unidirectional, originating at the master and terminating at the slave. The data signals can be either unidirectional or bi-directional, depending on the selected options. For half-duplex operation, the reverse direction bandwidth is one-fourth of the forward direction bandwidth. Token passing is used to control the communication direction of the link.

7.2.2.1 Global Operation Flow Diagram

The following figure shows the operational flow diagram for a Data Lane Module. Within both Tx and Rx four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround and Initialization.



7.2.2.2 Lane State Definition

The display module uses data and clock lane differential pairs for DSI. Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode. High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode. Different modes and protocols are used in each mode when transferring information from the AP to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined as below.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair define

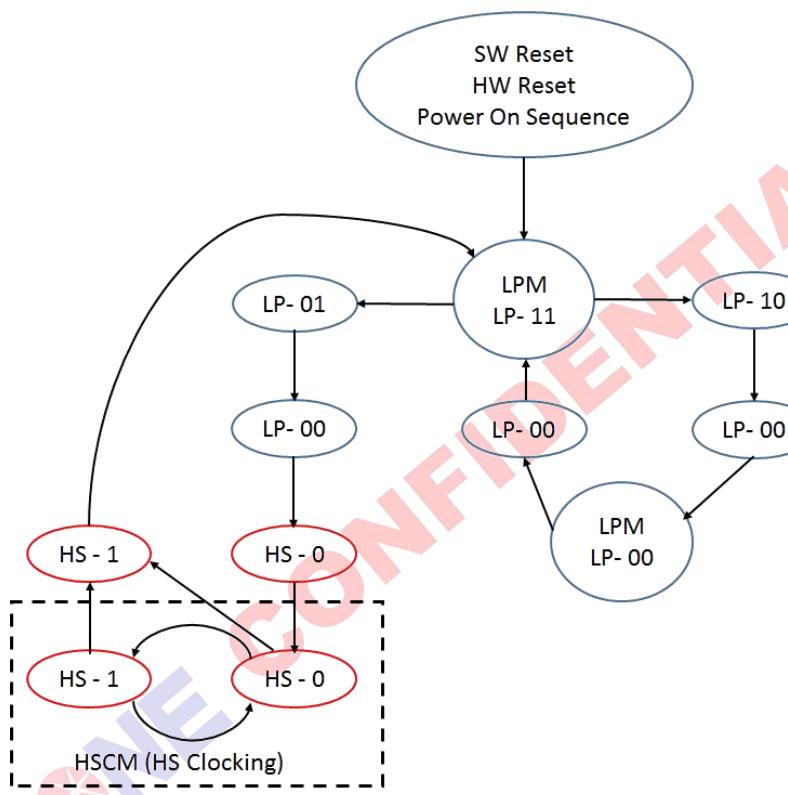
Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N		Burst Mode	Control Mode
HS-0	Low (HS)	High (HS)	Differential – 0	Note1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note1	Note1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

***Note:**

1. Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, then the lane pair will return to LP-11 of the Control Mode.
3. n = 0, 1, 2 and 3 (D1P/N, D2P/N and D3P/N lanes only for HS-0 and HS-1).

7.2.2.3 Clock Lane Module State

CLKP/N lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra-Low Power Mode (ULPM) and High Speed Clock Mode (HSCM). Clock lane is in the single ended mode (LP = Low Power) when entering or leaving Low Power Mode (LPM) or Ultra-Low Power Mode (ULPM). Clock lane is in the single ended mode (LP = Low Power) when entering in or leaving High Speed Clock Mode (HSCM). These entering and leaving protocols use Clock lane in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different Clock lane power modes is illustrated as below.

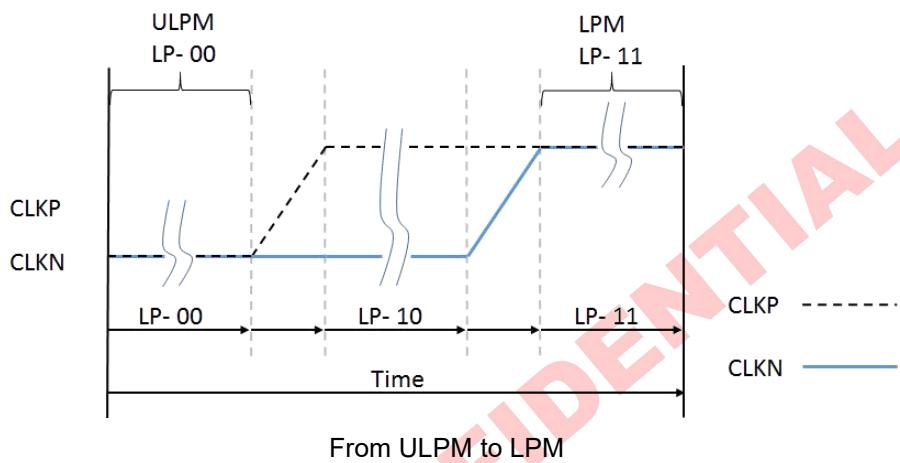


Clock Lane Module State Diagram

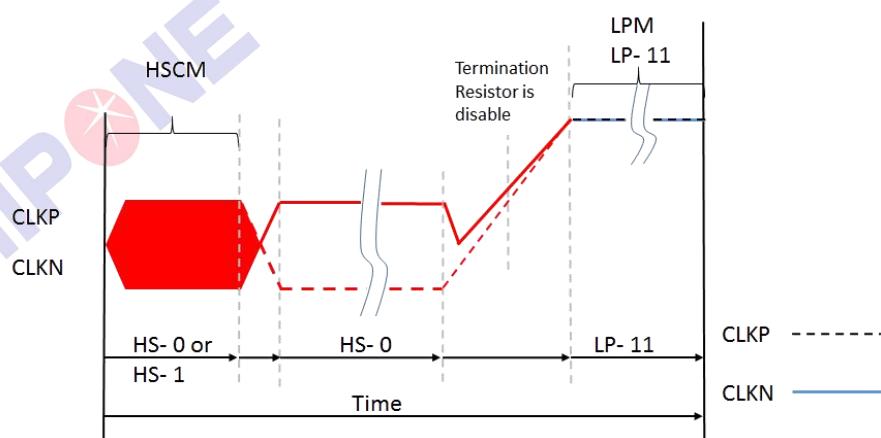
7.2.2.4 Low Power Mode (LPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence => LP-11.
- 2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM). This sequence is illustrated as below.

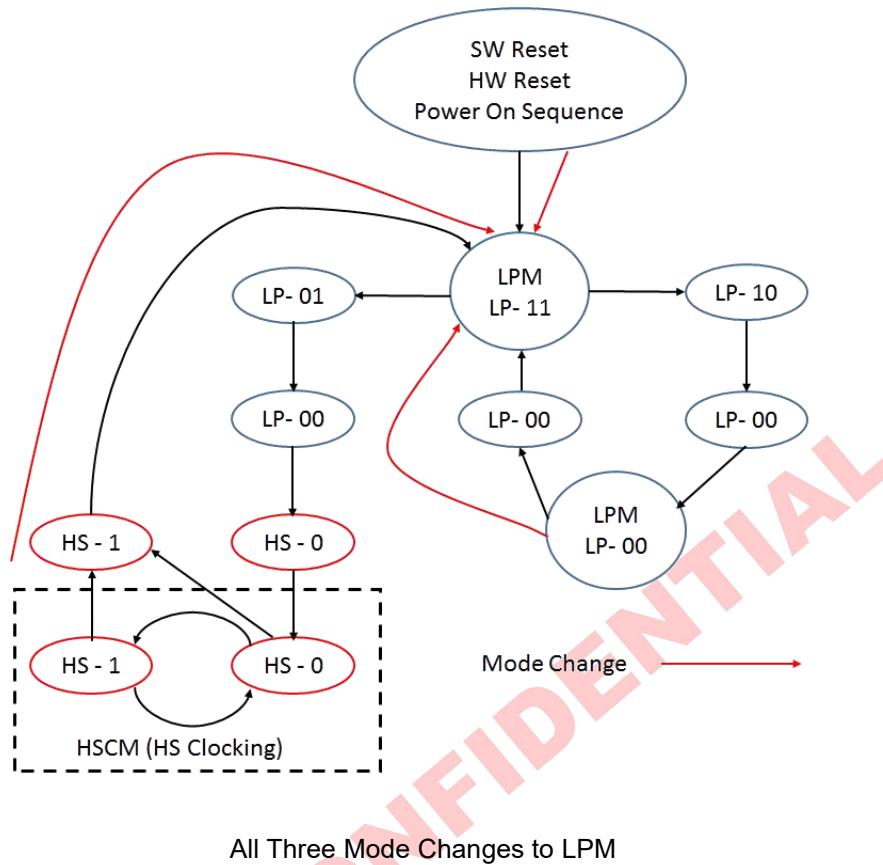


- 3) After CLKP/N lanes leave High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0=> LP-11 (LPM). This sequence is illustrated as below.



From High Speed Clock Mode (HSCM) to LPM

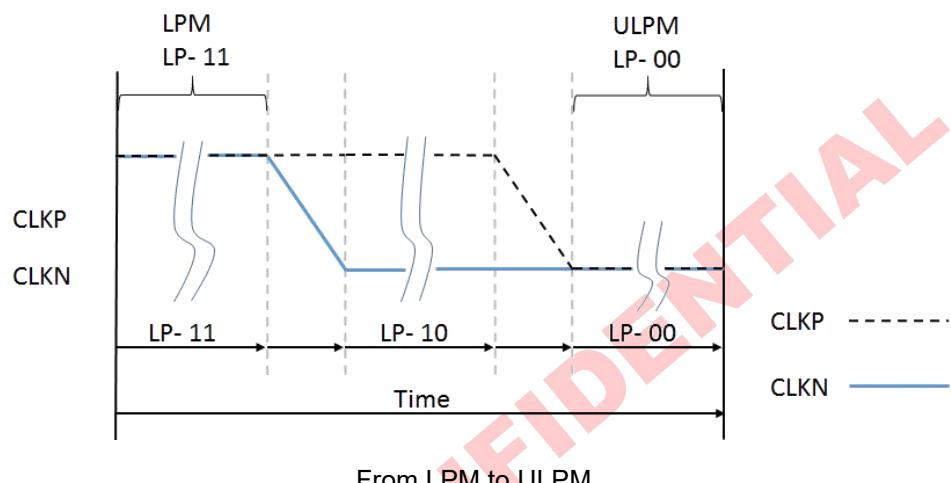
The changes of all the three modes are illustrated in the flow chart as below.



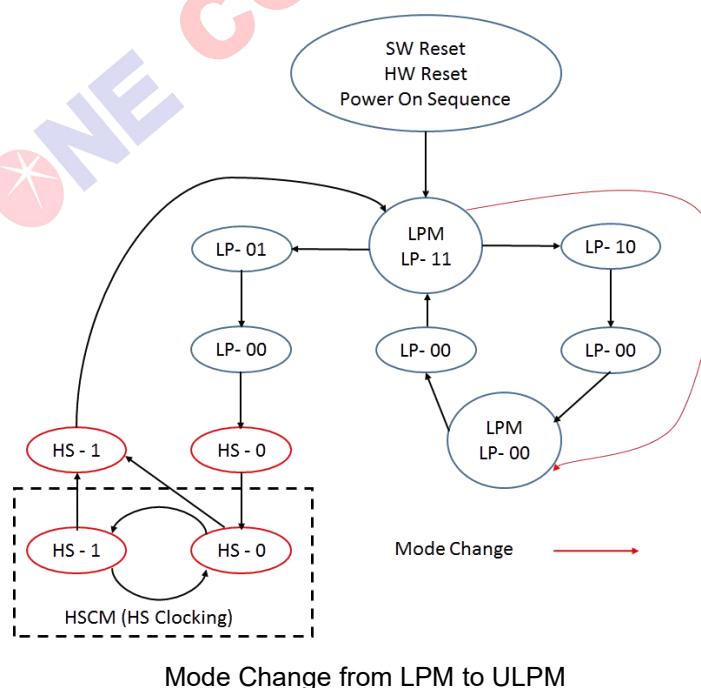
7.2.2.5 Ultra-Low Power Mode (ULPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence => LP-11.
 - 2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM).
- This sequence is illustrated as below.



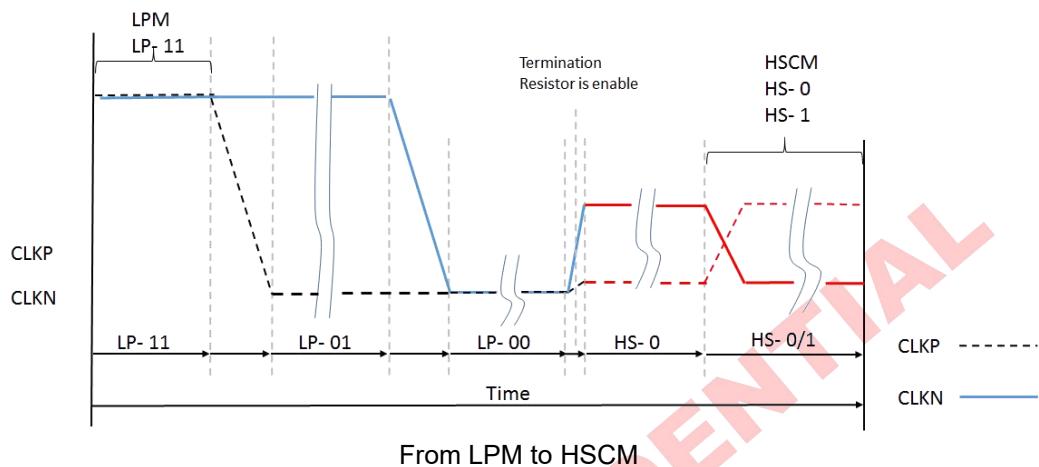
The mode change is also illustrated as below.



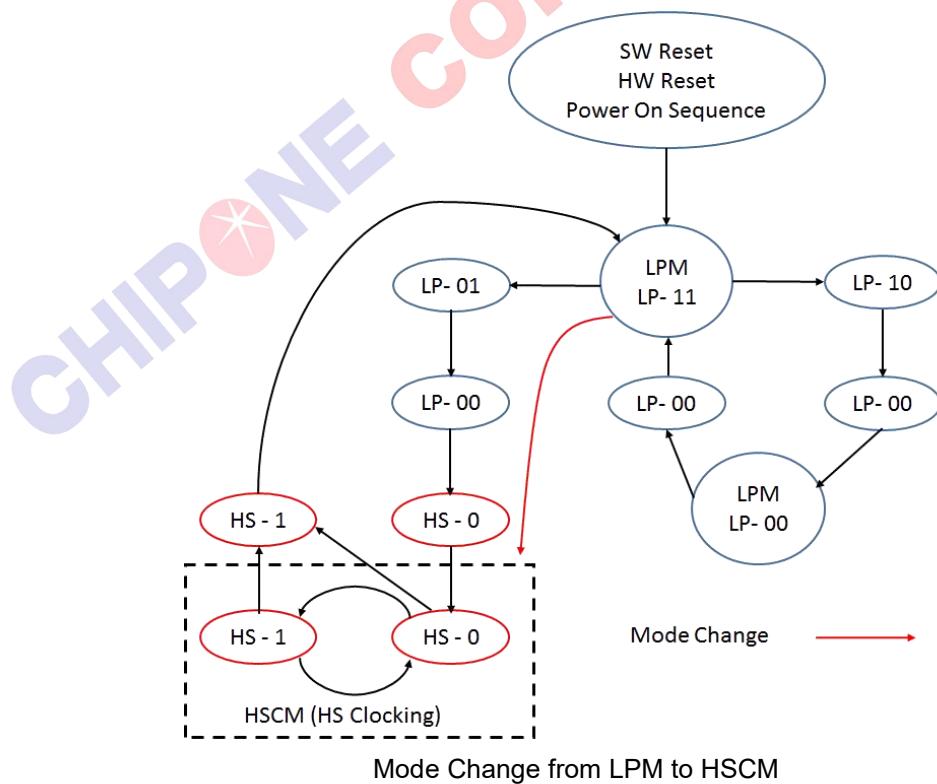
7.2.2.6 High-Speed Clock Mode (HSCM)

CLKP/N lanes can be driven to the High Speed Clock Mode (HSCM) when CLK lanes start to function between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM).

This sequence is illustrated as below.



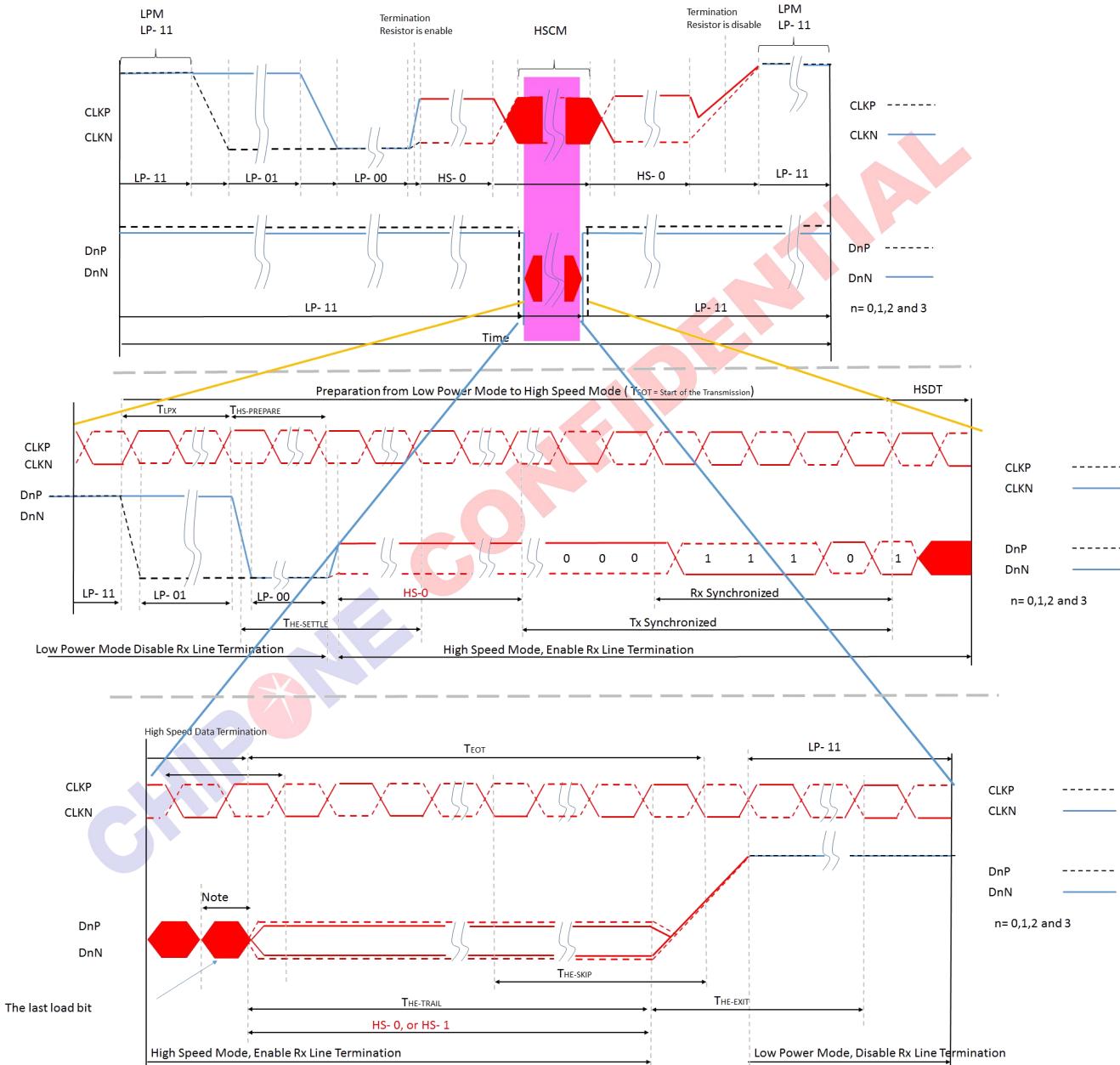
The mode change is also illustrated as below.



The high speed clock (CLKP/N) starts before high speed data is sent via data lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions.
- Start state is HS- 0.
- End state is HS- 0.



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

High Speed Clock Burst

7.2.2.7 Data Lane Module State

D0P/N, and D1P/N Data lanes can be driven into different modes:

- Escape Mode (Only D0P/N data lane is used).
- High- Speed Data Transmission (all data lanes are used).
- Bus Turnaround Request (Only D0P/N data lane are used).

These modes and their entering codes are defined in the following table.

Modes and entering code define

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP- 11→ LP- 10→ LP- 00 → LP- 01 → LP- 00	LP- 00→ LP- 10→ LP- 11 (Mark-1)
High- Speed Data Transmission	LP- 11→ LP- 01 → LP- 00 → HS- 0	(HS- 0 or HS- 1)→ LP11
Bus Turnaround Request	LP- 11→ LP- 10→ LP- 00 → LP- 10→ LP- 00	Hi- Z

7.2.2.8 Escape Modes

D0P/N data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode.

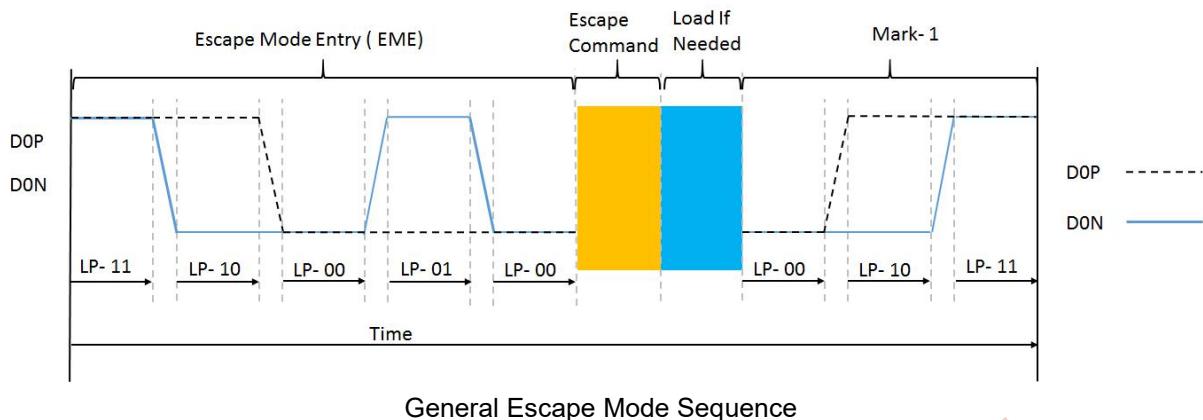
These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) from the AP to the display module.
- Drive data lanes to “Ultra-Low Power State” (ULPS).
- Indicate “Remote Application Reset” (RAR), which can reset DSI link block in the D-IC.
- Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the AP.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11.
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00.
- Escape Command (EC), which is coded, when one of the data lanes changes from low-to-high-to-low then this changed data lane presents the value of the current data bit (D0P = 1, D0N= 0). When DSI-D0 changes from low-to-high-to-low, the receiver will latch a data bit, which value is logical 0. The receiver will use this low-to-high-to-low transition as its internal clock.
- A load if it is needed.
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11.
- End: LP-11.

This basic construction is illustrated as below.



A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as shown in the following table.

An example of the Mode type Escape Command is „Ultra-Low Power Mode”, where the AP instructs the display module to enter its Ultra-Low Power Mode.

Escape commands are defined in the following table.

Escape commands define

Escape Command	Command Type Mode / Trigger	Entry command Pattern (First Bit → Last Bit Transmitted)	Dn	D0
Low- Power Data Transmission	Mode	1110 0001 bin		x
Ultra- Low Power Mode	Mode	0001 1110 bin	x	x
Underdefined- 1, Note1	Mode	1001 1111 bin		
Underdefined- 2, Note1	Mode	1101 1110 bin		
Remote Application Reset	Trigger	0110 0010 bin		
Acknowledge	Trigger	0010 0001 bin		x
UnKnow- 5, Note1	Trigger	1010 0000 bin		

***Note:**

1. This Escape command support is not implemented on the display module.
2. n=1, 2 and 3.
3. x= supported.

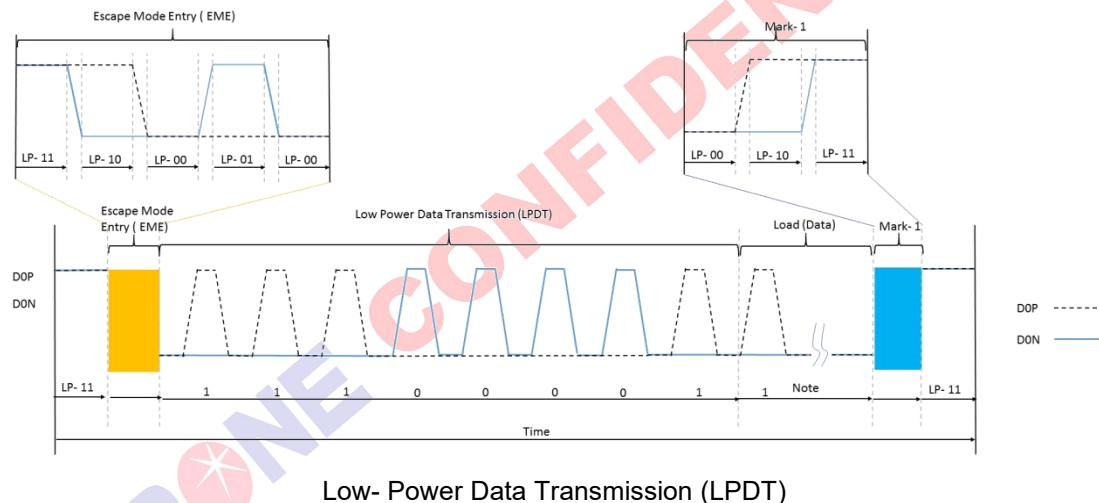
7.2.2.9 Low-Power Data Transmission (LPDT)

The AP can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module.

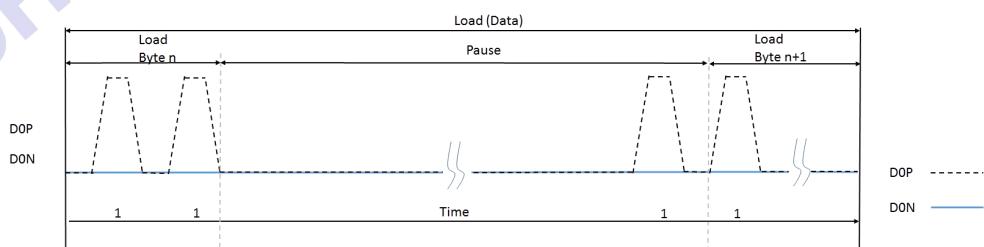
The display module also uses the same sequence when it sends data to the AP. The Low Power Data Transmission (LPDT) uses the following sequence:

- Start: LP-11.
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00.
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit).
- Load (Data).
- One or more bytes (one byte = 8 bit).
- Data lanes are in pause mode when data lanes are stopped (both lanes are low) between bytes.
- Mark-1: LP-00 => LP-10 => LP-11.
- End: LP-11.

This sequence is illustrated for reference purposes as below.



*Note: Load (Data) presents that the first bit is the logical 1 in this example.

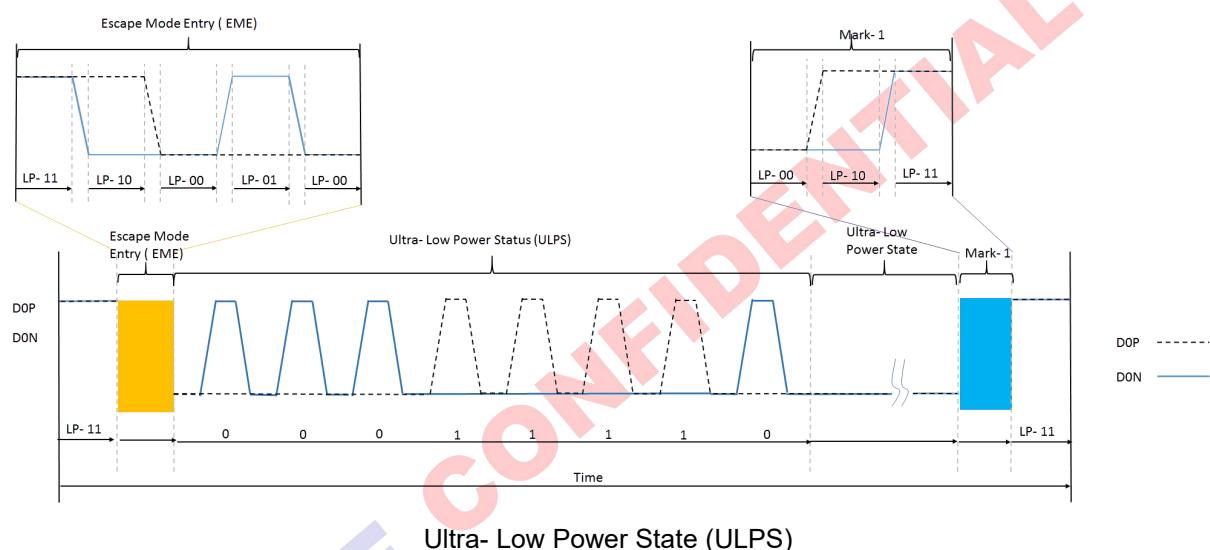


7.2.2.10 Ultra-Low Power State (ULPS)

The AP can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode. The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11.
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00.
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit).
- Ultra-Low Power State (ULPS) when the AP keeps data lanes low.
- Mark-1: LP-00 => LP-10 => LP-11.
- End: LP-11 (Next command must wait 100us after data lanes leave ULPS).

This sequence is illustrated for reference purposes as below.

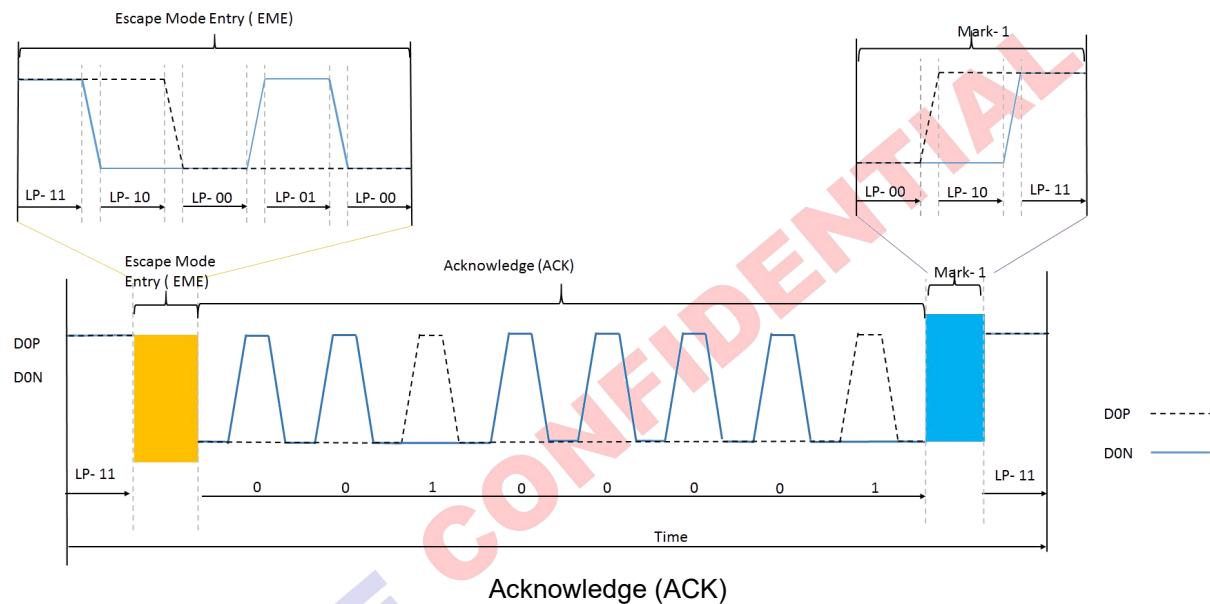


7.2.2.11 Acknowledge (ACK)

The display module can inform the AP an error is not recognized by Acknowledge (ACK). The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11.
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00.
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit).
- Mark-1: LP-00 => LP-10 => LP-11.
- End: LP-11.
-

This sequence is illustrated for reference purposes as below.

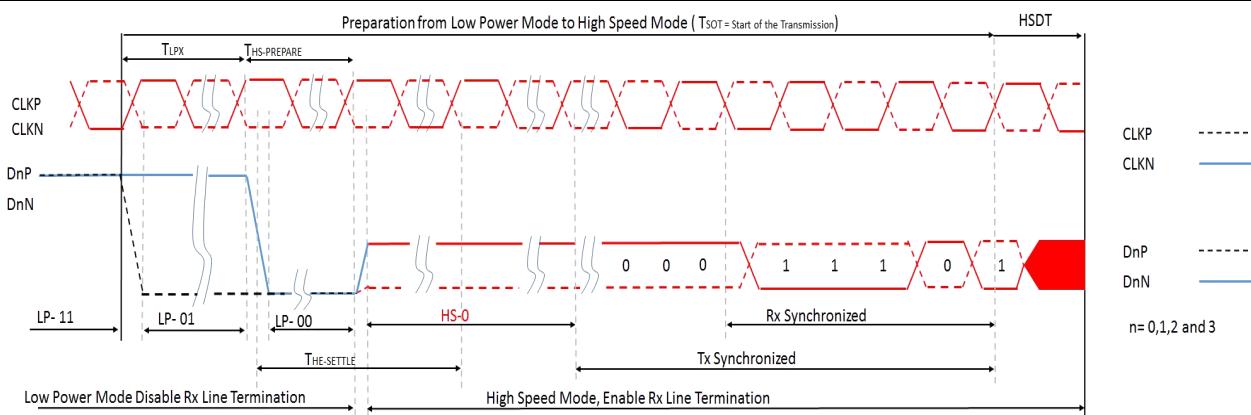


7.2.2.12 Entering High-Speed Data Transmission (TSOT of HSDT)

The display module enters High-Speed Data Transmission (HSDT) when Clock lane CLKP/N have already entered the High-Speed Clock Mode (HSCM) by the AP. See more information in the section “High-Speed Clock Mode (HSCM)”. Data lanes D0P/N and D1P/N of the display module enter the High-Speed Data Transmission (TSOT of HSDT) as follows:

- Start: LP-11.
- HS-Request: LP-01.
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable).
- Rx Synchronization: 011101 (Tx (= AP) Synchronization: 0001 1101).
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load.

The sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated as below.



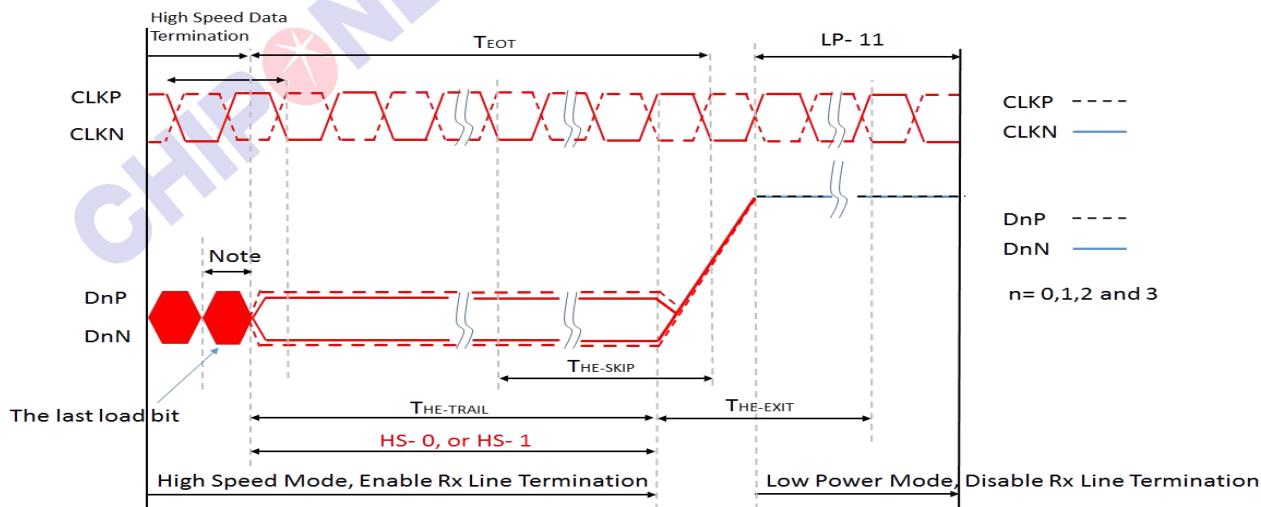
Entering High-Speed Data Transmission (TSOT of HSDT)

7.2.2.13 Leaving High-Speed Data Transmission (TEOP of HSDT)

The display module leaves the High-Speed Data Transmission (TEOT of HSDT) when Clock lane DSICLKPN are in the High-Speed Clock Mode (HSCM) by the AP, and this HSCM is kept until data lanes D0P/N and D1P/N are in the LP-11 mode. See more information in the section “High-Speed Clock Mode (HSCM)”. Data lanes D0P/N and D1P/N of the display module leave the High-Speed Data Transmission (TEOT of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT).
- Stops High-Speed Data Transmission.
- AP changes to HS-1, if the last load bit is HS-0.
- AP changes to HS-0, if the last load bit is HS-1.
- End: LP-11 (Rx: Lane Termination Disable).

The sequence of leaving High-Speed Data Transmission (TEOT of HSDT) is illustrated as below.



Note:

If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Leaving High-Speed Data Transmission (TEOT of HSDT)

7.2.3 MIPI DSI Protocol

7.2.3.1 Data Type (DT)

This Data Type (DT) also defines the used packet is a Short Packet (SPa) or a Long Packet (LPa). Data Types (DT) are different from the AP to the display module (or other devices) and vice versa. These Data Types (DT) are defined in the tables as below.

Data Types (DT) define List

Data Type (HEX)	Description	Packet Size
01h	Sync Event, V Sync Start	Short
11h	Sync Event, V Sync End	Short
21h	Sync Event, H Sync Start	Short
31h	Sync Event, H Sync End	Short
07h	Compression Mode Command	Short
08h	End of Transmission packet (EoTp)	Short
03h	Generic Short WRITE, no parameters	Short
13h	Generic Short WRITE, 1 parameter	Short
23h	Generic Short WRITE, 2 parameters	Short
04h	Generic READ, no parameters	Short
14h	Generic READ, 1 parameter	Short
24h	Generic READ, 2 parameters	Short
05h	DCS Short WRITE, no parameters	Short
15h	DCS Short WRITE, 1 parameter	Short
06h	DCS READ, no parameters	Short
37h	Set Maximum Return Packet Size	Short
09h	Null Packet, no data	Long
19h	Blanking Packet, no data	Long
29h	Generic Long Write	Long
39h	DCS Long Write/Write_LUT Command Packet	Long
0Ah	Picture Parameter Set	Long
0Bh	Compressed Pixel Stream	Long
0Ch	Loosely Packet Pixel Stream, 20-bit YCbCr, 4:2:2 Format	Long
2Ch	Packed Pixel Stream, 16-bit YCbCr, 4:2:2 Format	Long
3Eh	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h and XFh	DO NOT USE. All unspecified codes are reserved.	-

*Note:

1. This can be used when the AP wants to make sure that it is the end of the transmission in High Speed Data

Transferring (HSDT) mode.

2. This can be used when data lanes are to be kept in High Speed Data Transferring (HSDT) Mode.

Data Type (DT) from the Display Module (or Other Devices) to the AP.

Data Type (DT) from the Display Module (or Other Devices) to the AP

From the Display Module to the AP		
Hex	Description	Short / Long Packet
02h	Acknowledge with Error Report	SPa (Short Packet)
1Ch	DCS Read Long Response	LPa (Long Packet)
21h	DCS Read Short Response, 1 byte returned	SPa (Short Packet)
22h	DCS Read Short Response, 2 byte returned	SPa (Short Packet)
1Ah	Generic Read Long Response	LPa (Long Packet)
11h	Generic Read Short Response, 1 byte returned	SPa (Short Packet)
12h	Generic Read Short Response, 2 byte returned	SPa (Short Packet)

***Note:** The data type for Generic write/read: 1Ah, 11h, 12 will be disable (ignored packet) if bit DSIG is set to "0".

The receiver will ignore other Data Type (DT) if they are not defined on tables: "Data Type (DT) from the AP to the Display Module (or Other Devices)" or "Data Type (DT) from the Display Module (or Other Devices) to the AP".

7.2.3.2 Acknowledge with Error Report (AwER)

“Acknowledge with Error Report” (AwER), which is defined in Data Type (DT, 00 0010b), is always used in a Short Packet (SPa) from the display module to the AP. The Packet Data (PD) can include bits, which define the current error, when the corresponding bit is set to 1, as defined in the following table.

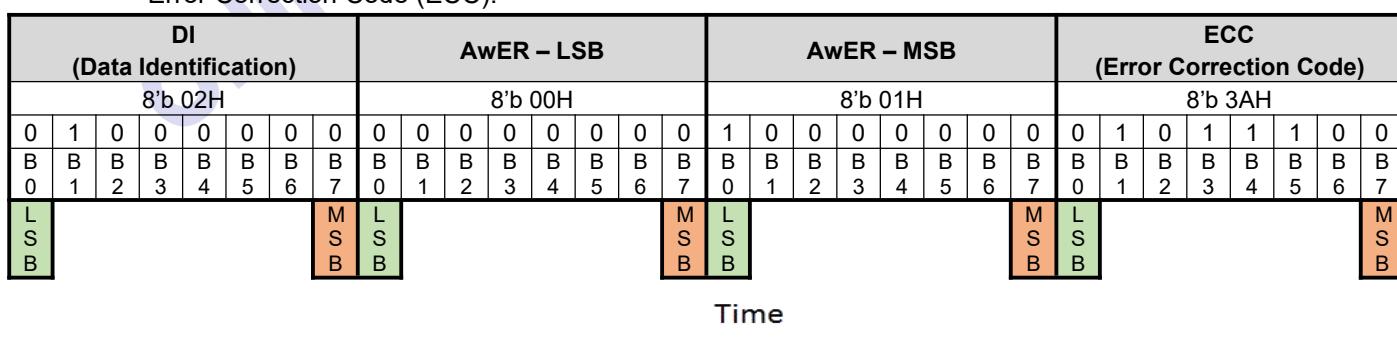
Acknowledge with Error Report

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long Packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages that have been received from the AP to the display module before the Bus Turnaround (BTA). The display module ignores the received packet which includes error or errors.

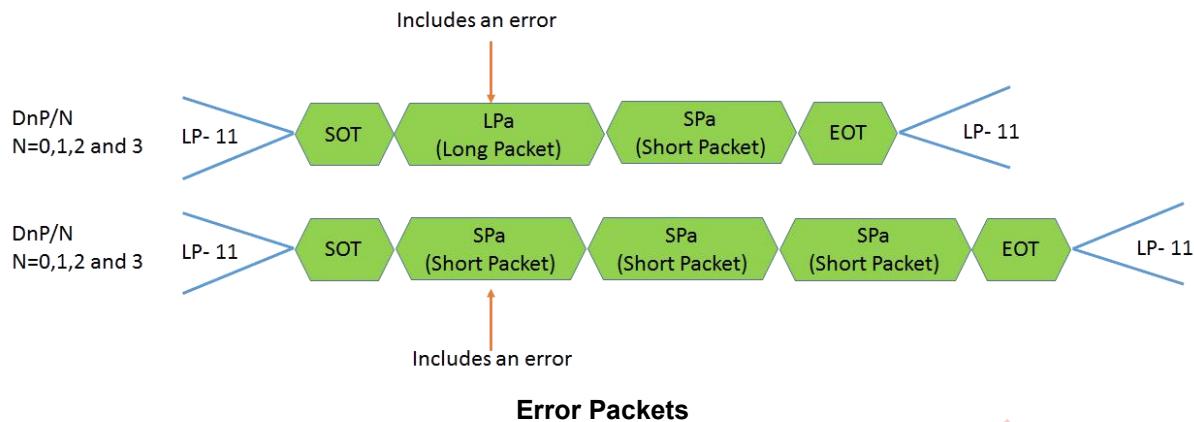
Acknowledge with Error Report (AwER) of a Short Packet (SPa) is defined as:

- Data Identification (DI):
 - - Virtual Channel (VC, DI [7...6]): 00b.
 - - Data Type (DT, DI [5...0]): 000010b.
- Packet Data (PD):
 - - Bit 8: ECC Error, single-bit (detected and corrected).
 - - AwER: 0100h.
- Error Correction Code (ECC).

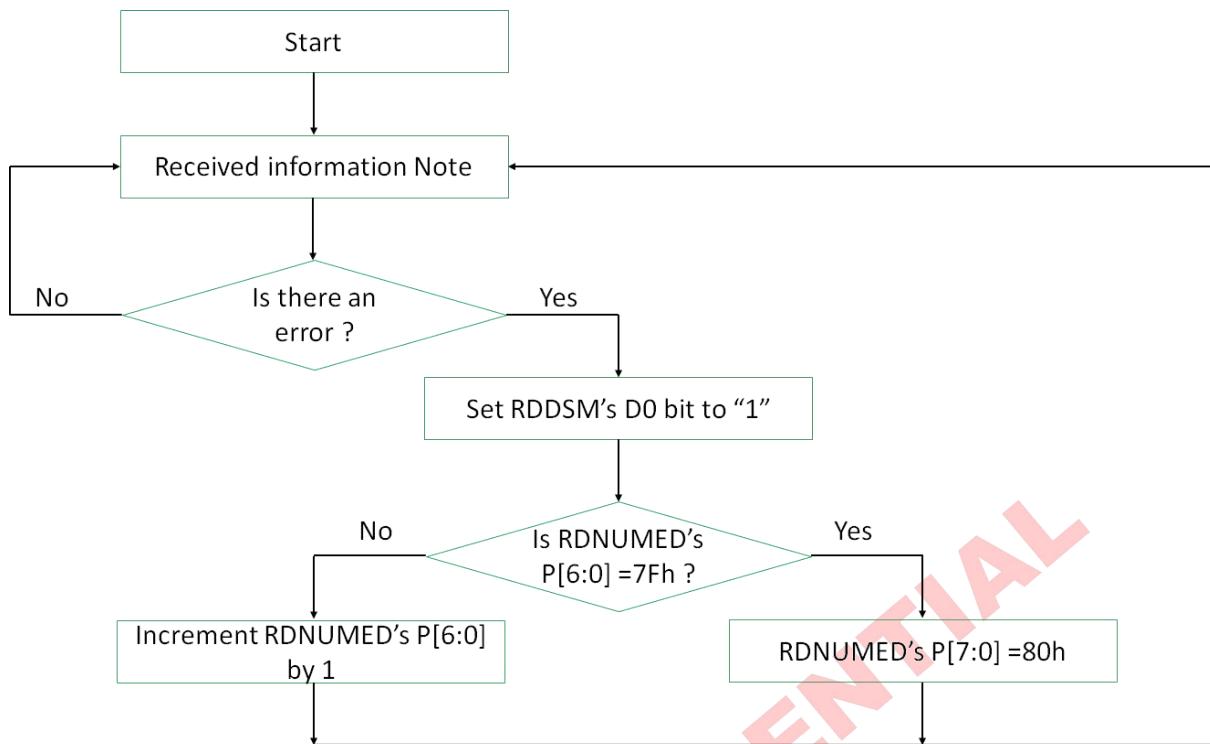


Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the AP before the AP performs the Bus Turnaround (BTA). Some examples are illustrated for reference purposes as below.



Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets can be detected by “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. The bit D0 of the “Read Display Signal Mode (0Eh)” command will be set to 1 if a received packet includes an error. The amount of packets, which include an **ECC** or **CRC** error, is calculated in the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h and set the bit D0 of the “Read Display Signal Mode (0Eh)” command to 0 after the AP has read the RDNUMED register from the display module. The functionality of the RDNUMED register is illustrated for reference purposes as below.



Flow Chart for Errors on DSI

***Note:**

1. This information can be Interface or Packet Level Communication, but it is always from the AP to the display module.
2. CRC or ECC error

7.2.4 Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

7.2.4.1 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, *Burst Mode* refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figure the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figure in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

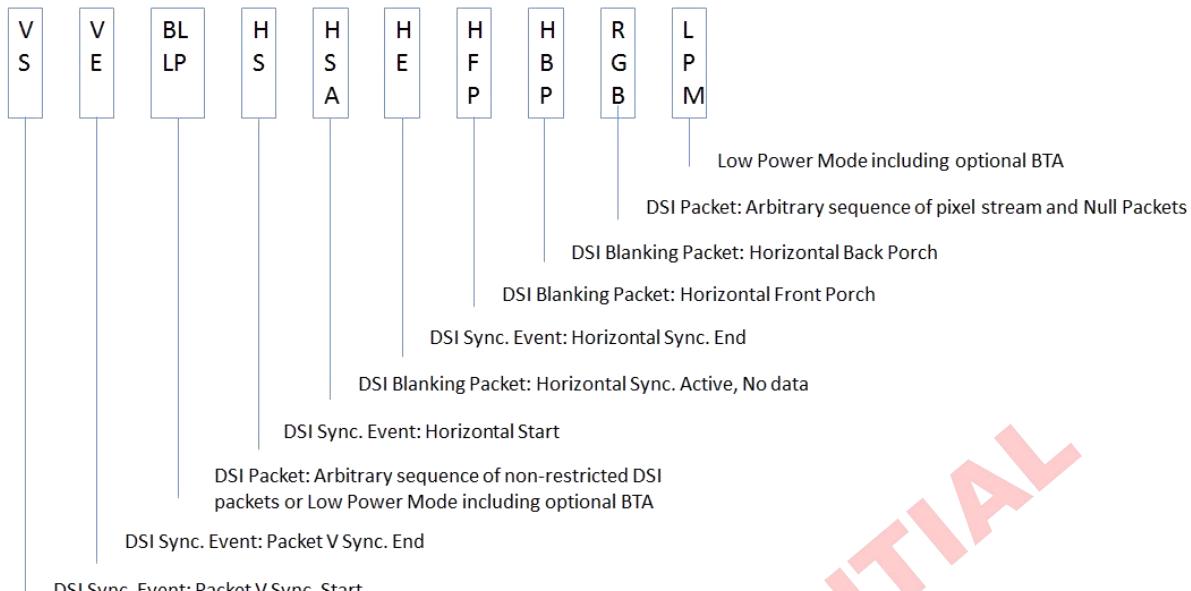
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX.
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode.
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode.
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode.
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel. Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figure in this section are defined in figure as below unless

otherwise specified.

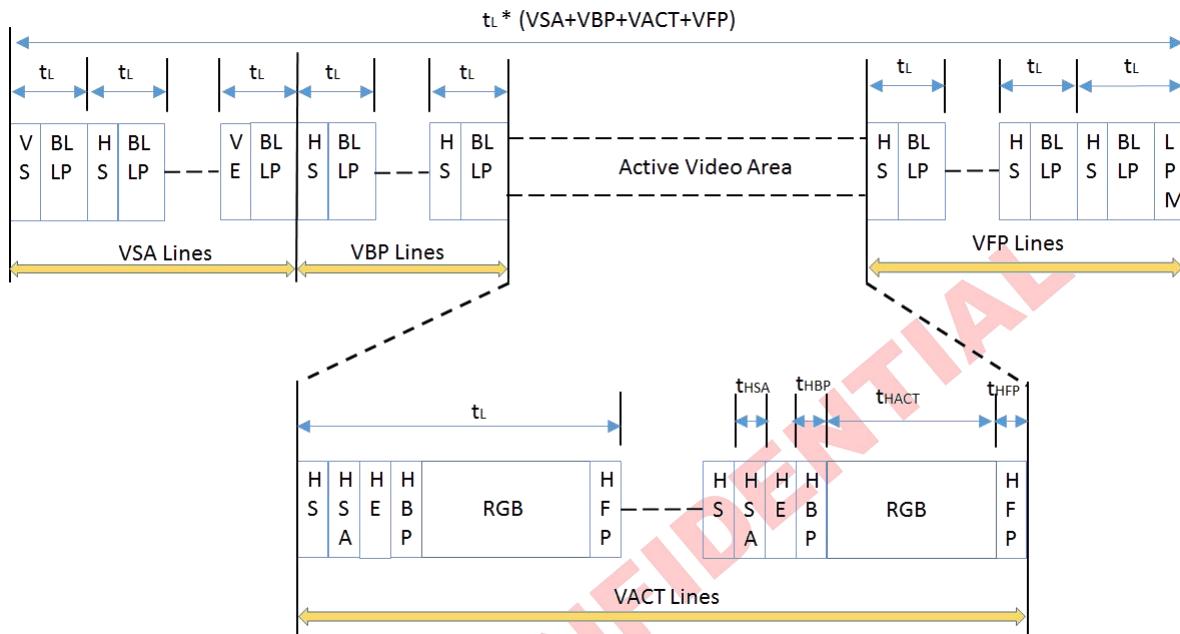


DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

7.2.4.2 Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in the figure as below.



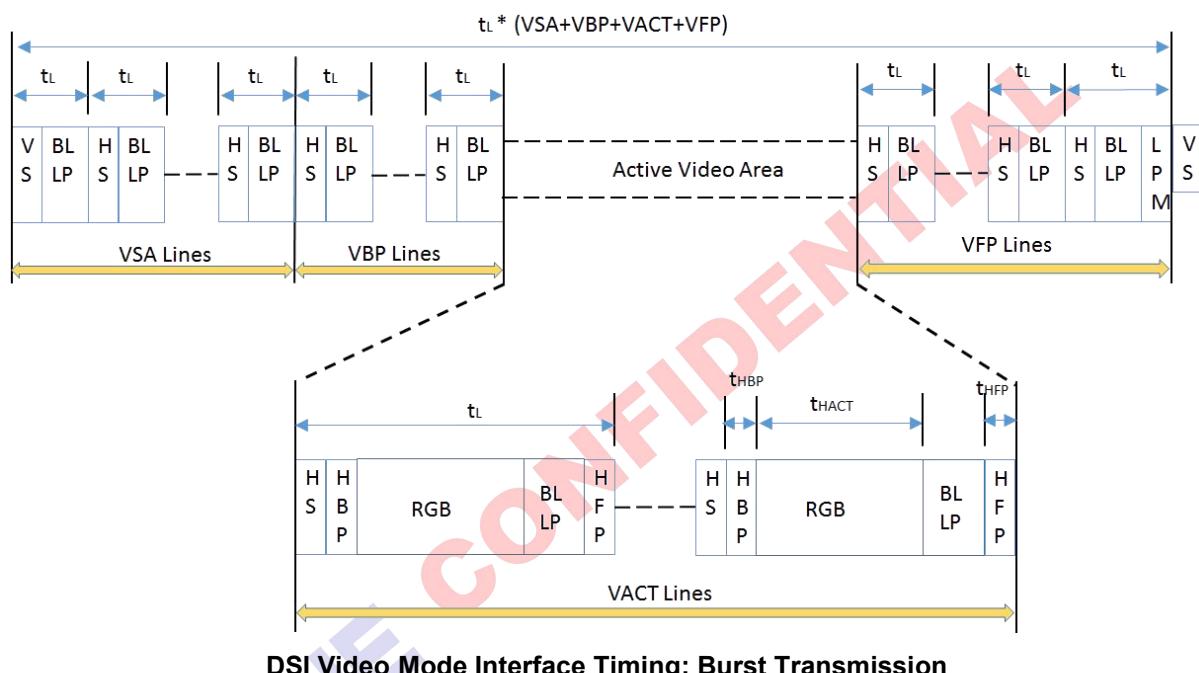
DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet.

Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

7.2.4.3 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in figure as below.



Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

7.2.5 Display Data Compression Mode

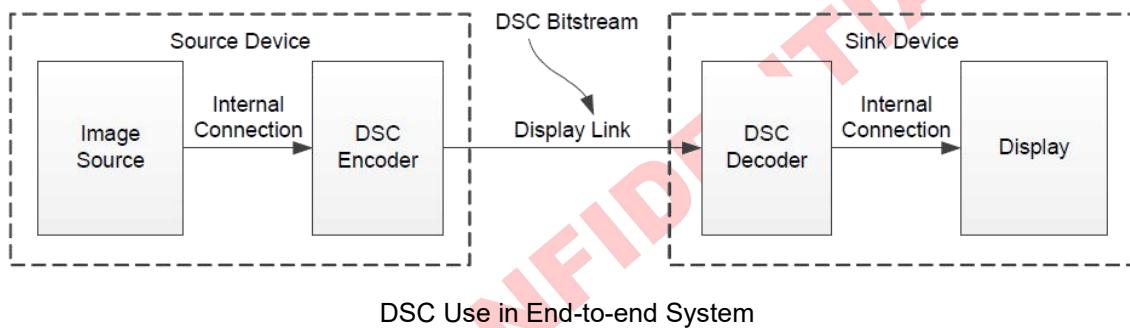
7.2.5.1 VESA Display Stream Compression (DSC)

The DSC Standard is a specification of the algorithms used for compressing and decompressing image display streams, including the specification of the syntax and semantics of the compressed video bitstream. DSC is designed for real-time systems, with real-time compression, transmission, decompression, and display.

The DSC algorithm is designed to enable low-cost hardware implementations of visually lossless video compression over display links. One of the main features is the ability to support of slices to enable partial update of compressed frame buffers, and for bounding the range of artifacts resulting from errors in the received bitstream.

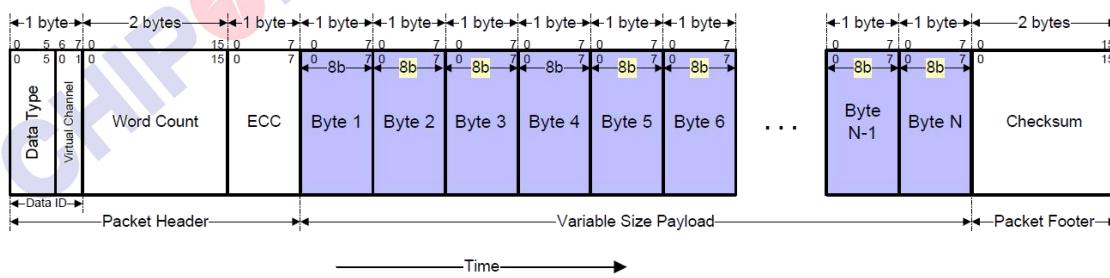
The standardization of DSC transmission has also been achieved to transfer compressed display data over MIPI Display Serial Interface (DSI).

*VESA: Video Electronics Standards Association



7.2.5.2 Compressed Pixel Stream

The Compressed Pixel Stream is a long packet, which is defined in Data Type (DT, 00 1011b), that carries compressed data to a Video Mode display module. This packet shall consist of a DI byte, a two-byte non-zero WC, an ECC byte, a payload containing WC bytes and a two-byte checksum, shown in the figure as below.



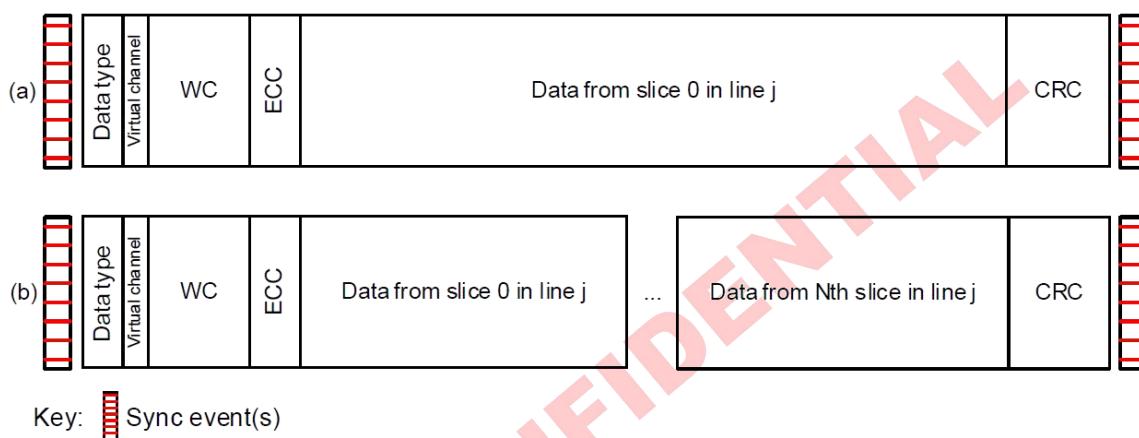
Compressed Pixel Stream Format, Long Packet

A compressed image is composed of data slices (a full slice usually ranges over several lines). The packet carries data from one or more compressed slice segments (called slice-widths) or chunks within one line time period. The specification of DSC Standard can limit the number of slice-widths of data carried in one line time.

The following two figures illustrate transporting a single slice-width of data or transporting multiple slice-widths of data in this packet. The slices have the same horizontal size that equates to the same packet size in a constant bit rate coding system. This behavior is defined by the coding system. For example, if the image is compressed to

have one slice-width of data horizontally, the following figure (a) shows the portion of slice 0 transported in line time period j is fully contained in one packet. In this case, the following figure 40 (a) is the only means to transport this portion of the slice-width of data. If the image is compressed to have more slices horizontally, the following figure (b) shows the Compressed Pixel Stream packet contains multiple slice-widths of data.

If the image is compressed to have more than one slice horizontally, an integral number of slice-widths of data may be carried by sequential Compressed Pixel Stream packets in one line time j. The following figure shows sequential packets that can contain slice-widths of data. This is one method that can segregate slice-widths when the receiver has multiple instantiations of decoders and this packet structure is used to identify slice-width boundaries.



One Line Containing One Packet with Data from One or More Compressed Slices

The Compressed Pixel Stream does not limit usage to any specific MIPI-compliant bitstream or standard. This packet shall only carry compressed image data with any pixel arrangement or component depth supported by the decoder.

7.2.5.3 Compression Mode Command

Some display stream compression parameters may be configured using the Compression Mode Command, which is a short packet consisting of a DI byte, a two-byte payload and an ECC byte. It is defined in Data Type (DT, 00 0111b).

This packet signals whether compression is enabled or disabled and the coding system used to create a bitstream that is carried by the Compressed Pixel Stream data type in Data Type (DT, 00 1011b).

Compression Mode Parameters

SP Byte	Bit Location	Bit Description and Assigned Values
Data 0	7:6	Reserved, bits equal 0
Data 0	5:4	PPS selector 00 = PPS Table 1 (or no tables stored, default reset value) 01 = PPS Table 2 10 = PPS Table 3 11 = PPS Table 4
Data 0	3	Reserved
Data 0	2:1	Reserved, bits equal 0
Data 0	0	0 = compression disabled (default) 1 = compression enabled
Data 1	7:0	Reserved, bits equal 0

***Note:** Applies to video mode or command mode. In command mode, all bits are readable and writable, except reserved bits that use a defined value or are disallowed.

The Command mode contains a two-bit PPS Selector that may be used to enable a pre-stored PPS Table for controlling the compression decoder parameters. The processor sends this data type to change the decoder parameters that shall take effect following the next vertical sync or internal vertical sync (if using command mode). The PPS Selector is an optional field; if no table is stored in the receiver, the selector shall be 00b.

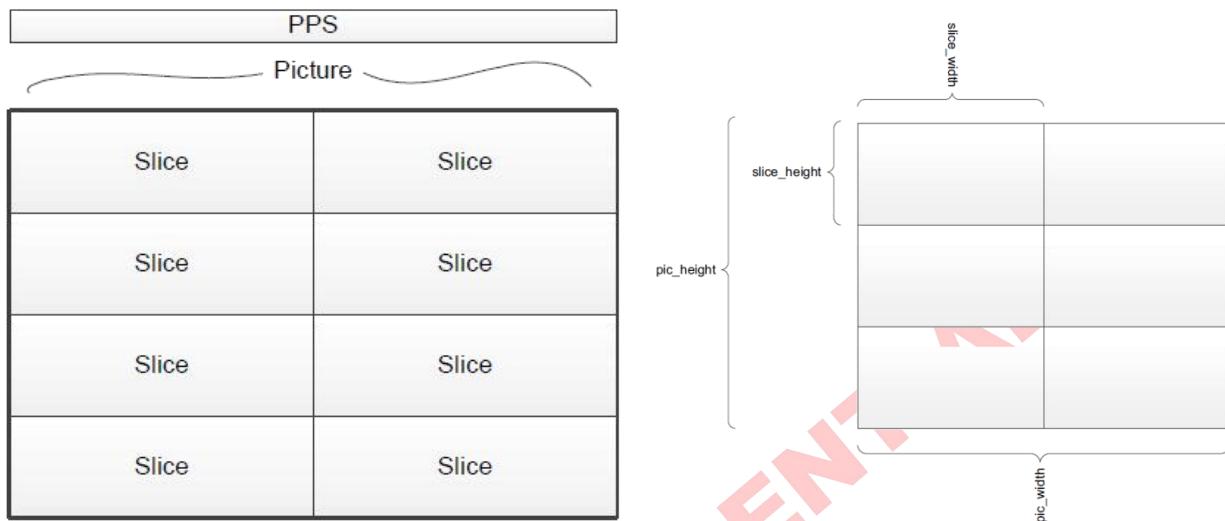
7.2.5.4 Picture Parameter Set

The Picture Parameter Set (PPS) data type, which is defined in Data Type (DT, 00 1010b), is a long packet used to transmit a pre-defined set of parameters that control a compression coding system. The packet shall consist of a DI byte, a two-byte, non-zero WC, an ECC byte, a payload containing WC bytes, and a two-byte checksum.

The size, content and timing context of this long packet is defined by the coding system designated in the Compression Mode data type, Data Type (DT, 00 0111b), and transported in the Compressed Image Format data type, Data Type (DT, 00 1011b). Using this long packet, for example, may replace adding header markers to a bitstream.

If the peripheral receiver supports multiple, stored PPS tables, the received new PPS data is stored in the table designated by the Compression Mode PPS Selector if the table is writable.

The PPS table is a pre-defined set of compression parameters. The DSC encoder and DSC decoder should be set up the same compression parameter configuration in order to encode and decode the bitstream correctly. The PPS table should be transmitted when the DDIC initialized or the input resolution changed or compression ratio changed and so on.

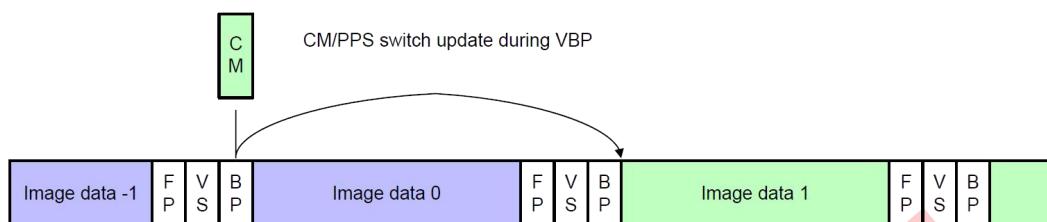
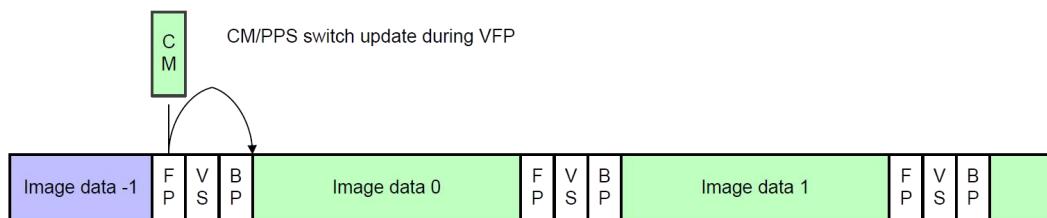


Relationship between Picture Parameter Set, Pictures, and Slices

***Note:**

1. Slice Height: The vertical frame dimension shall be evenly divisible by the number of lines per slice.
2. Partial Update: the minimum unit of partial update range is 1 slice. The detail addressing method, please refer the COSET (2Ah) and PASET (2Bh).

The PPS table change takes effect in a video mode peripheral that is processing a data stream after the next vertical sync, not within the same frame, as shown in the following figure. The PPS change takes effect in a command mode peripheral after the next signaled tearing effect, that is, either after a TE signal pulse or a TE Trigger Message.



PPS Update by Setting the Compression Mode Short Packet

***Note:**

VS = Vertical sync event

FP = Vertical front porch

BP = Vertical back porch

CM = Compression Mode short packet with PPS change

7.3 MIPI Display Serial Interface (DSI2)

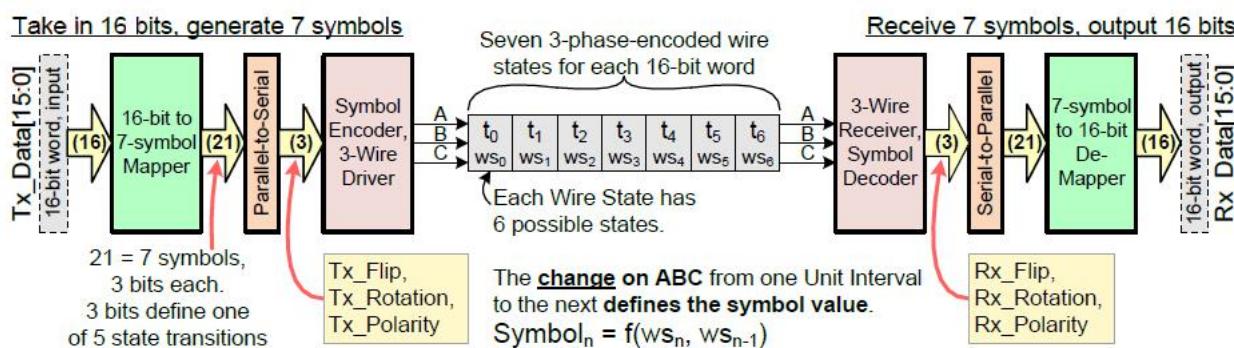
7.3.1 General Description for C-PHY

C-PHY describes a high-speed, rate-efficient PHY, especially suited for mobile applications where channel rate limitations are a factor. The needs of rate limited channels are accomplished through the use of 3-Phase symbol encoding technology delivering approximately 2.28 bits per symbol over a three-wire group of conductors. This C-PHY specification has been written primarily for the connection of cameras and displays to a host processor. Nevertheless, it can be applied to many other applications.

C-PHY has re-used many parts of the D-PHY standard. C-PHY was designed to coexist on the same IC pins as D-PHY so that dual-mode devices can be developed. C-PHY high-speed data coding differs substantially from the D-PHY clock-forwarding system, although the high-speed signal levels and terminations bear some similarity. The low-power mode of D-PHY is reused almost completely, and the transitions to and from the high-speed and low-power modes is very similar to the D-PHY standard.

The key characteristics of C-PHY coding are:

- ◆ Uses a group of three conductors rather than conventional pairs. The group of three wires is called a lane, and the individual lines of the lane are called: A, B and C. C-PHY does not have a separate clock lane.
- ◆ Within a three-wire lane, two of the three wires are driven to opposite levels; the third wire is terminated to a mid-level (at either one end or both ends), and the voltages at which the wires are driven changes at every symbol.
- ◆ Multiple bits are encoded into each symbol each, the data rate is ~2.28x the symbol rate. There is no additional overhead for line coding, such as 8b10b, which is not needed.
- ◆ Clock timing is encoded into each symbol. This is accomplished by requiring that the combination of voltages driven onto the wires must change at every symbol boundary. This simplifies clock recovery.
- ◆ C-PHY interface can co-exist on the same pins/pads as the D-PHY interface signals.

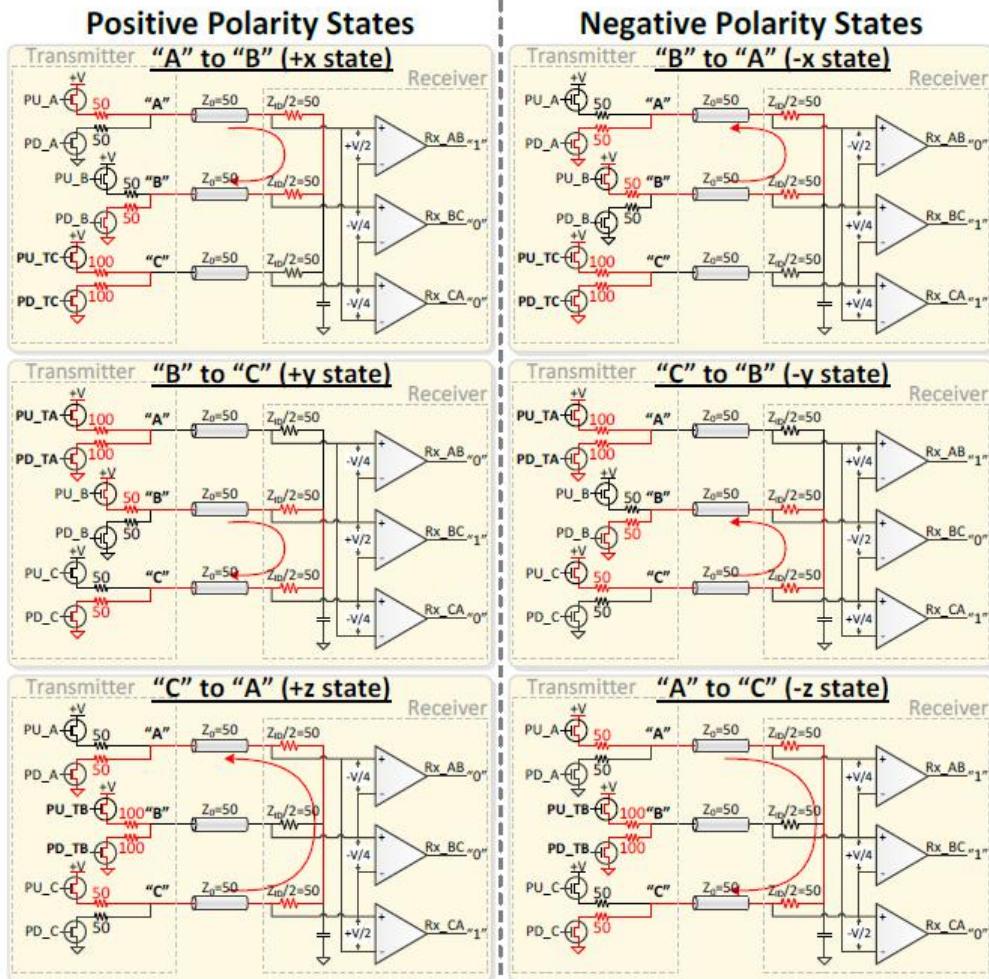


End-to-End Transmission of Data, 16-bit Word Conversion to Channel States

7.3.1.1 Lane Signaling States

The circuit examples below are simplified for the data encoding example; they are intended to illustrate the basic signaling states on the three-wire link. 6 driven states (called wire states) on a C-PHY lane are called: +x, -x, +y, -y, +z, and -z. Ex: the +x wire state is defined as A being driven high and B driven low, while the -x wire state is B driven high and A driven low.

The
and
voltage
C-PHY
defined



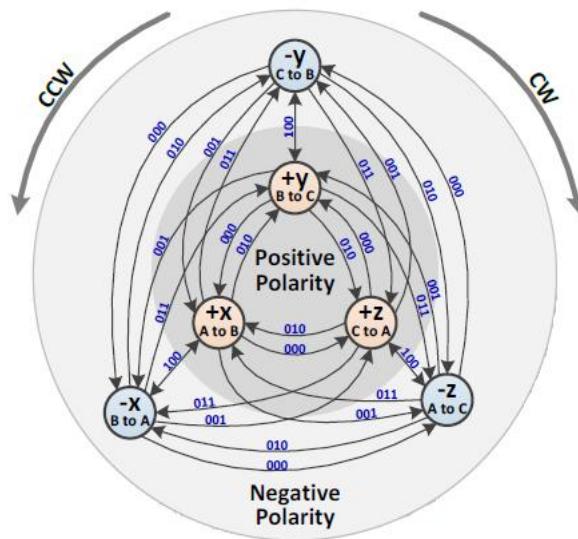
signal voltage
differential
for the six
wire states are
below:

Wire States	Wire Amplitude			Receiver Diff. Input Voltage			Receiver digital output		
	A	B	C	A-B	B-C	C-A	Rx_AB	Rx_BC	Rx_CA
+x	+x	+x	+x	+x	+x	+x	+x	+x	+x
$\frac{3}{4} V$	$\frac{3}{4} V$	$\frac{3}{4} V$	$\frac{3}{4} V$	$\frac{3}{4} V$	$\frac{3}{4} V$	$\frac{3}{4} V$	$\frac{3}{4} V$	$\frac{3}{4} V$	$\frac{3}{4} V$
$\frac{1}{4} V$	$\frac{1}{4} V$	$\frac{1}{4} V$	$\frac{1}{4} V$	$\frac{1}{4} V$	$\frac{1}{4} V$	$\frac{1}{4} V$	$\frac{1}{4} V$	$\frac{1}{4} V$	$\frac{1}{4} V$
$\frac{1}{2} V$	$\frac{1}{2} V$	$\frac{1}{2} V$	$\frac{1}{2} V$	$\frac{1}{2} V$	$\frac{1}{2} V$	$\frac{1}{2} V$	$\frac{1}{2} V$	$\frac{1}{2} V$	$\frac{1}{2} V$
$+\frac{1}{2} V$	$+\frac{1}{2} V$	$+\frac{1}{2} V$	$+\frac{1}{2} V$	$+\frac{1}{2} V$	$+\frac{1}{2} V$	$+\frac{1}{2} V$	$+\frac{1}{2} V$	$+\frac{1}{2} V$	$+\frac{1}{2} V$
$-\frac{1}{4} V$	$-\frac{1}{4} V$	$-\frac{1}{4} V$	$-\frac{1}{4} V$	$-\frac{1}{4} V$	$-\frac{1}{4} V$	$-\frac{1}{4} V$	$-\frac{1}{4} V$	$-\frac{1}{4} V$	$-\frac{1}{4} V$

7.3.1.2 Compressed Pixel Stream

With six possible wire states (as shown below Figure and above Table) there are always 5 possible transitions to the next wire state from any present wire state. The possible state transitions are illustrated in the

state diagram. The symbol value is defined by the change in wire state values from one unit interval to the next.



7.3.1.3 Symbol Encoding and Decoding

Each symbol shall be represented using a 3-bit number having one of five values: 000, 001, 010, 011 and 100.

The symbol values are based on the specific transitions between the wire states as below. These transitions are derived from the 3-bit symbol value where each bit defines a particular wire state change parameter: flip, rotate, and polarity. The flip, rotate and polarity bits affect the wire state as follows:

Five Possible Transitions from Previous State to Present State (Encoding)

Symbol Input Value	Previous Wire State, interval N-1						What Happens
	+x	-x	+y	-y	+z	-z	
000	+z	-z	+x	-x	+y	-y	Rotate CCW, polarity is Same
001	-z	+z	-x	+x	-y	+y	Rotate CCW, polarity is Opposite
010	+y	-y	+z	-z	+x	-x	Rotate CW, polarity is Same
011	-y	+y	-z	+z	-x	+x	Rotate CW, polarity is Opposite
1XX	-x	+x	-y	+y	-z	+z	Same phase, polarity is Opposite

*Notes:

1. Symbol Input value is: [Tx_Flip, Tx_Rotation, Tx_Polarity]
2. Values in the table show the Present Wire State transmitted during interval N, as a function of the Previous Wire State transmitted during interval N-1, and 3-bit Symbol Value.

Receive Transition Mapping (Decoding)

Present Wire State [Rx_AB, Rx_BC, Rx_CA]	Previous Wire State [prev_Rx_AB, prev_Rx_BC, prev_Rx_CA] (wire state received during interval N-1)

(received during interval N)	+x [100]	+x [100]	+x [100]	+x [100]	+x [100]	+x [100]
+x state [100]	N/A	1xx	000	001	010	011
-x state [011]	1xx	N/A	001	000	011	010
+y state [010]	010	011	n/a	1xx	000	001
-y state [101]	011	010	N/A	n/a	001	000
+z state [001]	000	001	010	011	N/A	1xx
-z state [110]	001	000	011	010	1xx	N/A
	symbol value above = [Rx_Flip, Rx_Rotation, Rx_Polarity]					

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7.3.2 Interface Level Communication for C-PHY

7.3.2.1 General

The display module uses data and clock lane differential pairs for DSI2 (DSI2-1M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disabled (A termination resistor of the receiver is disabled) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enabled) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below

State Code	Line Voltage Levels			High-Speed	Low-Power	
	A Line	B Line	C Line	Burst Mode	Control Mode	Escape Mode
HS_+X	HS High	HS Low	HS Mid	+x state	N/A, Note 1	N/A, Note 1
HS+-X	HS Low	HS High	HS Mid	-x state	N/A, Note 1	N/A, Note 1
HS_+Y	HS Mid	HS High	HS Low	+y state	N/A, Note 1	N/A, Note 1
HS_-Y	HS Mid	HS Low	HS High	-y state	N/A, Note 1	N/A, Note 1
HS_+Z	HS Low	HS Mid	HS High	+z state	N/A, Note 1	N/A, Note 1
HS_-Z	HS High	HS Mid	HS Low	-z state	N/A, Note 1	N/A, Note 1
LP-000	LP Low	LP Low	LP Low	N/A	Bridge	Space
LP-001	LP Low	LP Low	LP High	N/A	HS-Rqst	Mark-0

*Notes:

1. During high-speed transmission the low-power Receivers observe LP-000 on the lines.
2. If LP-111 occurs during escape mode the lane returns to Stop state (Control Mode LP-111)

7.3.2.2 DSI2-DATA Lanes

DSI2-An/Bn/Cn Data Lanes can be driven in different modes which are:

- Escape Mode (Only DSI2-D0 A/B/C data lanes is used)
- High-Speed Data Transmission (all data lanes are used)
- Bus Turnaround Request (Only DSI2-D0 A/B/C data lanes is used)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-111=>LP-100=>LP-000=>LP-001=>LP-000	LP-000=>LP-100=>LP-111 (Mark-1)
High-Speed Data Transmission	LP-111=>LP-001=>LP-000=>3333333	4444444 =>LP-111
Bus Turnaround Request	LP-111 >LP-100=>LP-000=>LP-100=>LP-000	High-Z

Escape Modes

Data lanes (DSI2-A0/B0/C0) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

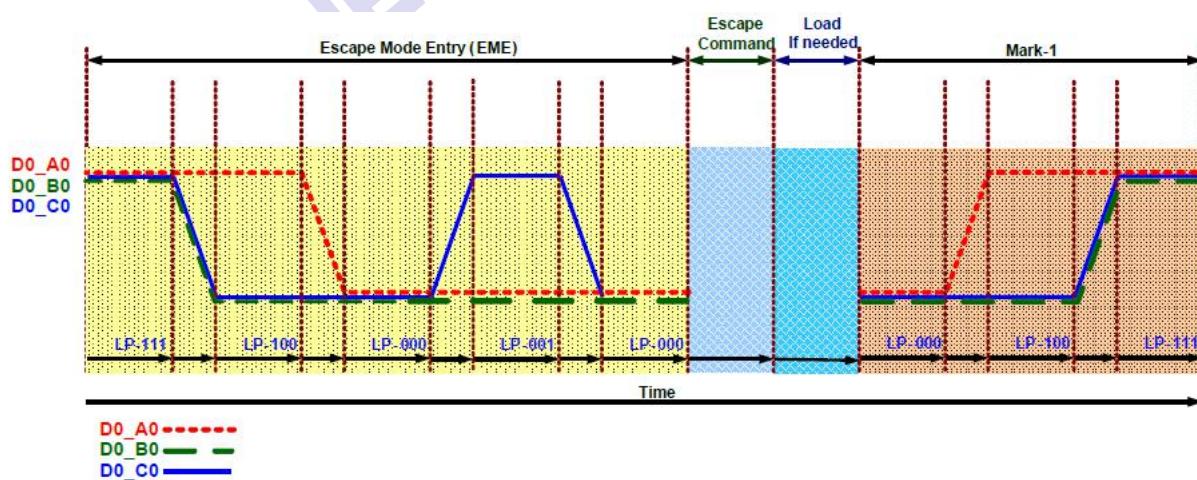
These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is reset the display module
- Indicate “Tearing Effect” (TE), which is used for a TE trigger event from the display module to the MCU
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

- Start: LP-111
- Escape Mode Entry (EME): LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI2-D0_A0 = 1, DSI2-D0_B0 = 0, DSI2-D0_C0 = 0) e.g. when DSI2-D0_C0 is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-000 =>LP-100 =>LP-111
- End: LP-111

This basic construction is illustrated below:



General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as shown in the following table.

An example of the Mode type Escape Command is „Ultra-Low Power Mode”, where the AP instructs the display module to enter its Ultra-Low Power Mode.

Escape commands are defined in the following table.

Escape commands define

Escape Command	Command Type Mode / Trigger	Entry command Pattern (First Bit→ Last Bit Transmitted)	Dn	D0
Low- Power Data Transmission	Mode	1110 0001 bin		x
Ultra- Low Power Mode	Mode	0001 1110 bin	x	x
Underdefined- 1, Note1	Mode	1001 1111 bin		
Underdefined- 2, Note1	Mode	1101 1110 bin		
Remote Application Reset	Trigger	0110 0010 bin		
Acknowledge	Trigger	0010 0001 bin		x
UnKnow- 5, Note1	Trigger	1010 0000 bin		

***Note:**

1. This Escape command support is not implemented on the display module.
2. n=1, 2 and 3.
3. x= supported.

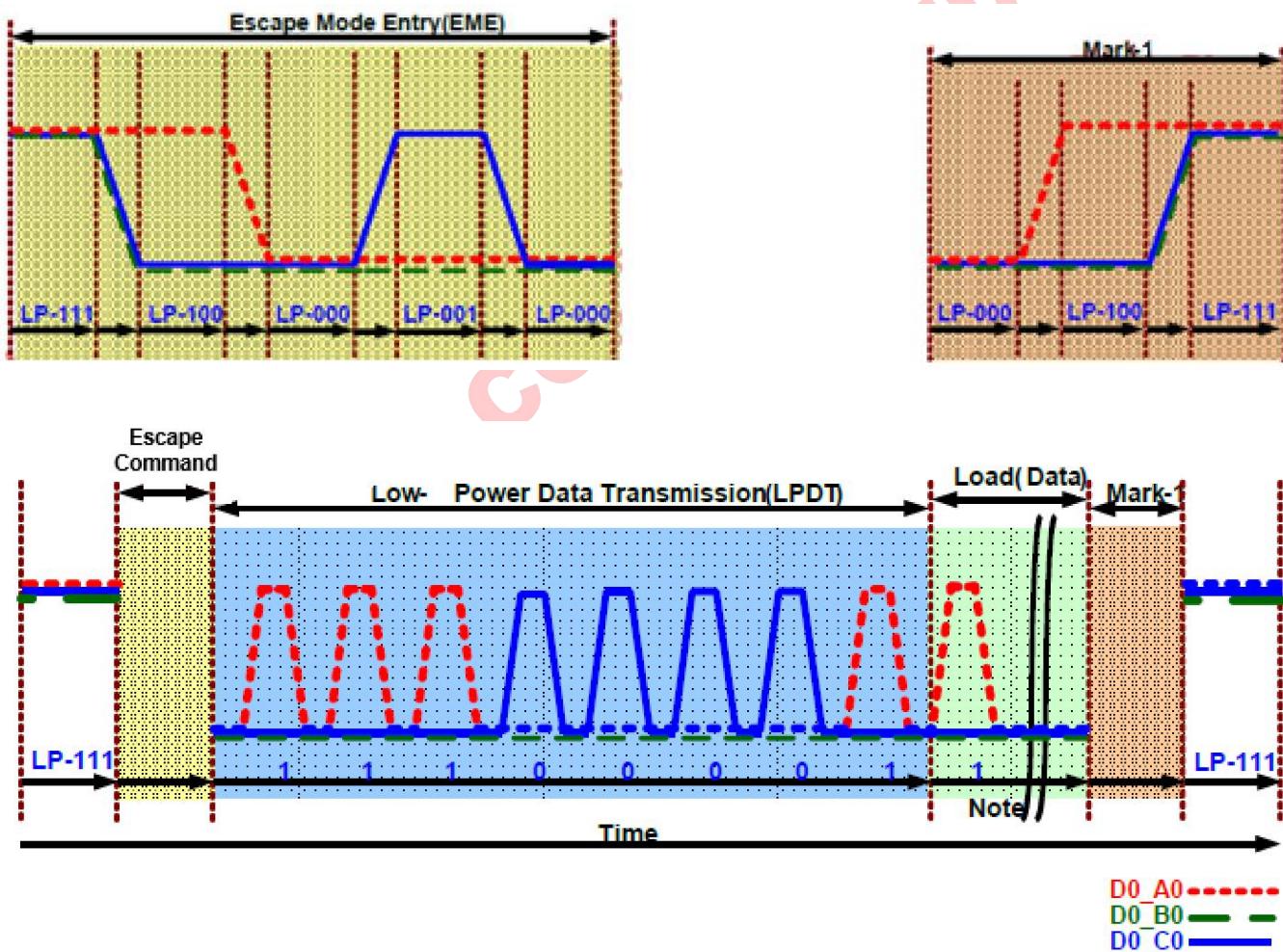
Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

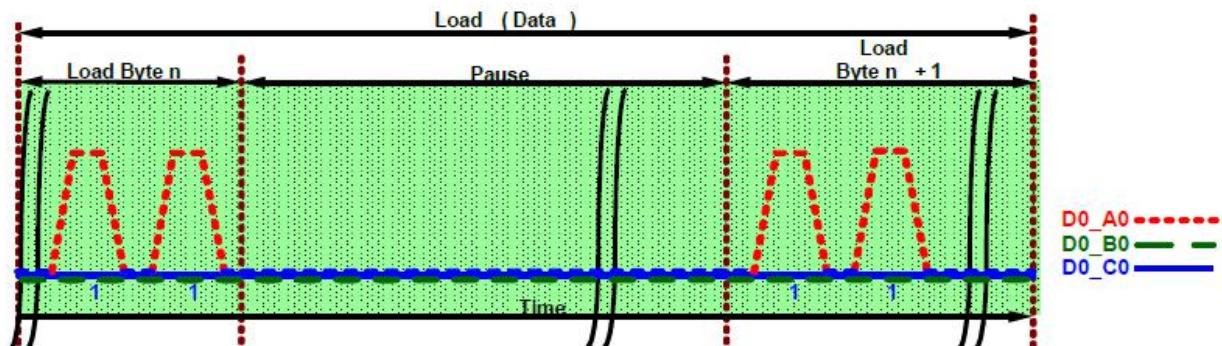
- Start: LP-111
- Escape Mode Entry (EME): LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
- One or more bytes (8 bit)
- Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-000 =>LP-100 =>LP-111
- End: LP-111

This sequence is illustrated for reference purposes below:



*Note: Load (Data) is presenting that the first bit is logic '1' in this example

Low-Power Data Transmission (LPDT)



Pause (Example)

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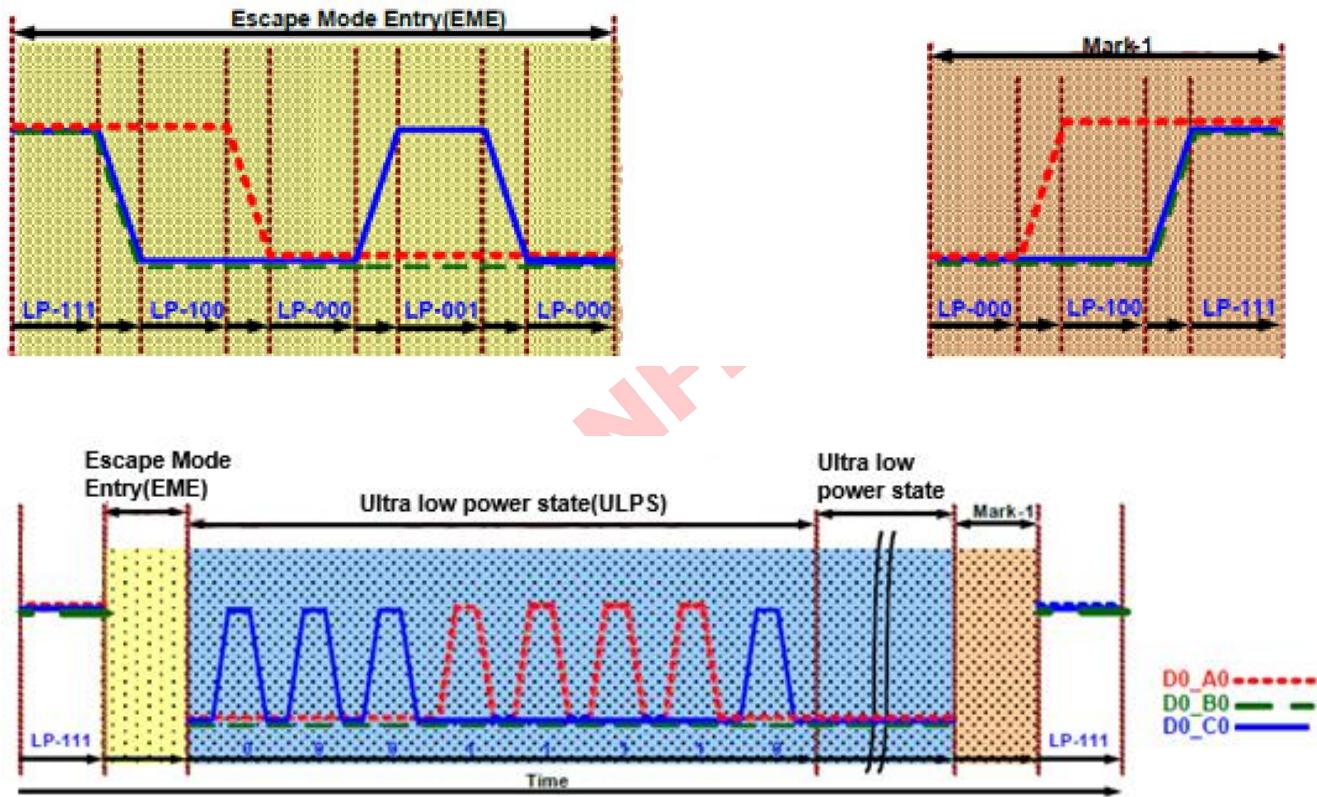
Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-111
- Escape Mode Entry (EME): LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-000 =>LP-100 =>LP-111
- End: LP-111

This sequence is illustrated for reference purposes below:



Ultra-Low Power State (ULPS)

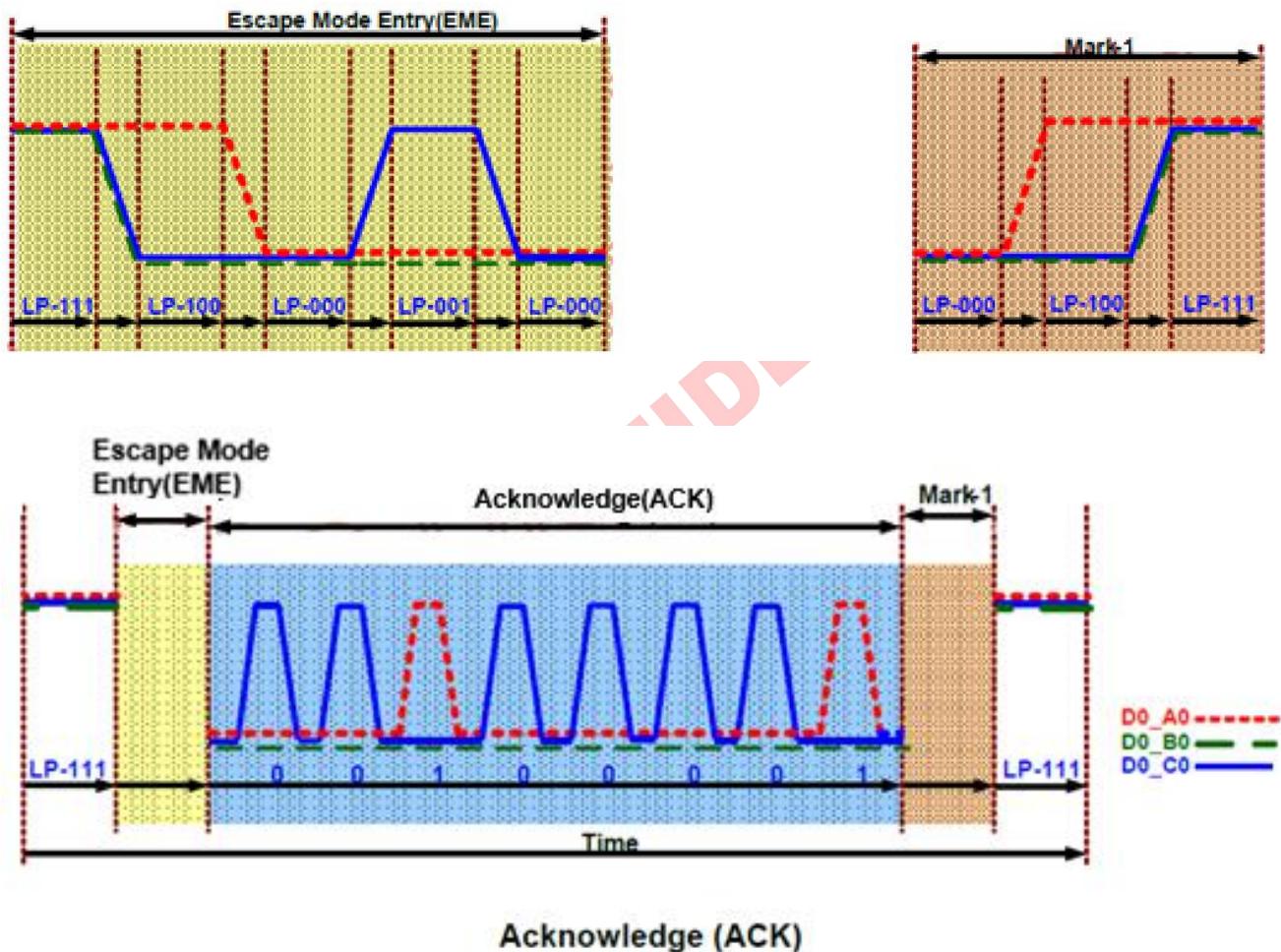
Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-111
- Escape Mode Entry (EME): LP-111 =>LP-100 =>LP-000 =>LP-001 =>LP-000
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-000 =>LP-100 =>LP-111
- End: LP-111

This sequence is illustrated for reference purposes below:



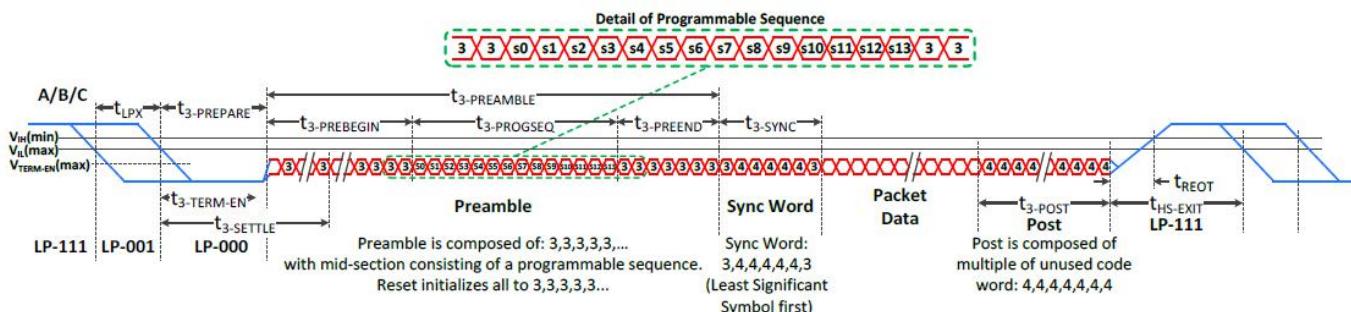
High Speed Data Transmission (HSDT)**Entering High-Speed Data Transmission (T_{SOT} of HSDT)**

The display module is entering High-Speed Data Transmission (HSDT) by the MCU.

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-111
- HS-Request: LP-001
- HS-Settle: LP-000 => 333333 (Rx: Lane Termination Enable)
- Rx Synchronization: 3444443 (Sync Word), Least Significant Symbol first
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below

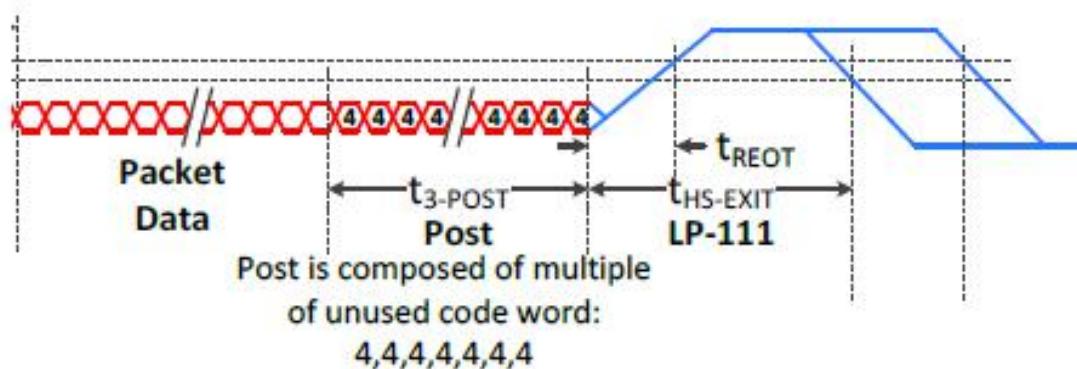
**Leaving High-Speed Data Transmission (T_{EOT} of HSDT)**

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) by the MCU and this HSCM is kept until data lanes are in LP-111 mode.

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- MCU changes to 4444444, Post is composed of multiple of unused code
- End: LP-111 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below



7.3.3 Packet Level Communication for C-PHY

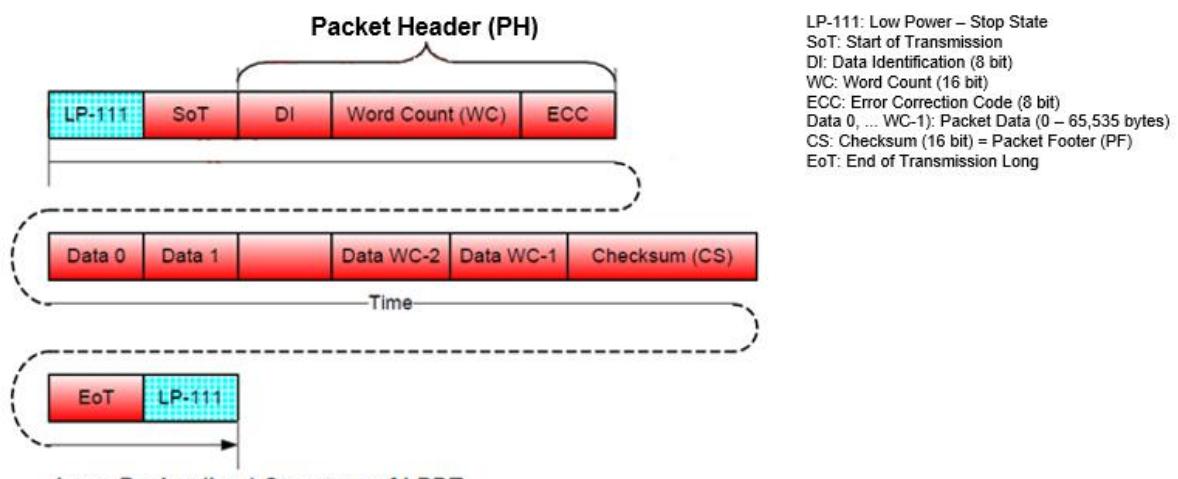
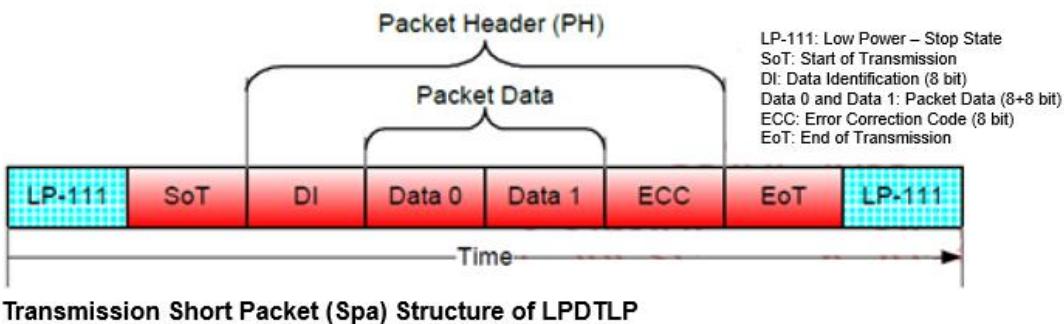
7.3.3.1 Short Packet (SPa) and Long Packet (LPa) Structure for C-PHY

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

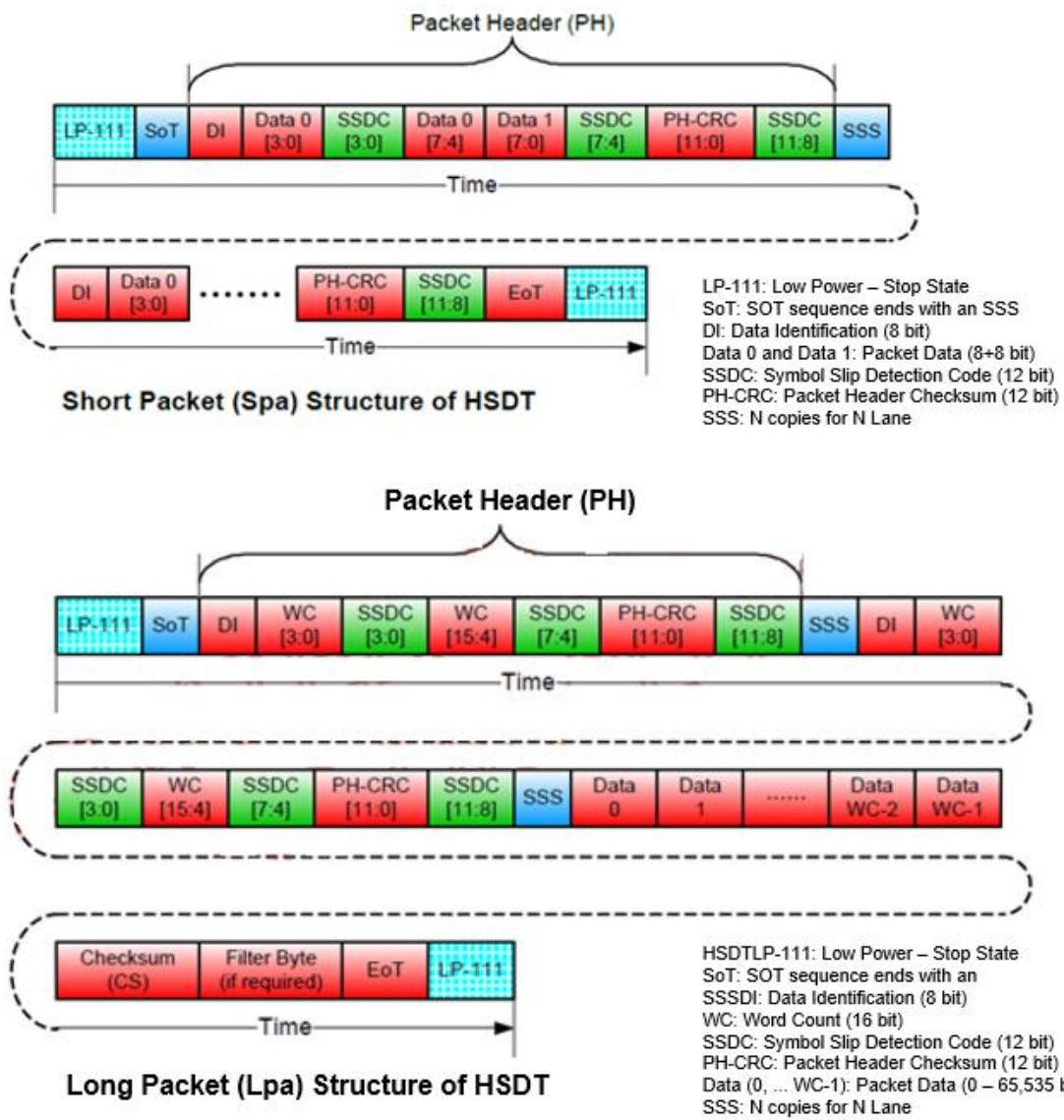
- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).



Note:
Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-111, SoT and EoT for each packet sending).
The other possibility is that there is not needed SoT, EoT and LP-111 between packets if packets have sent in multiple packet format e.g.

- * LP-111 => SoT => SPa => LPa => SPa => SPa => EoT => LP-111
- * LP-111 => SoT => SPa => SPa => SPa => EoT => LP-111
- * LP-111 => SoT => LPa => LPa => EoT => LP-111



8. Functional Description

8.1 Tearing Effect Information

The tearing effect output line supplies to the AP a panel synchronization signal. This signal can be enabled or disabled by the tearing effect line off & on commands. The mode of the tearing effect line is defined by the parameter of the tearing effect line on command.

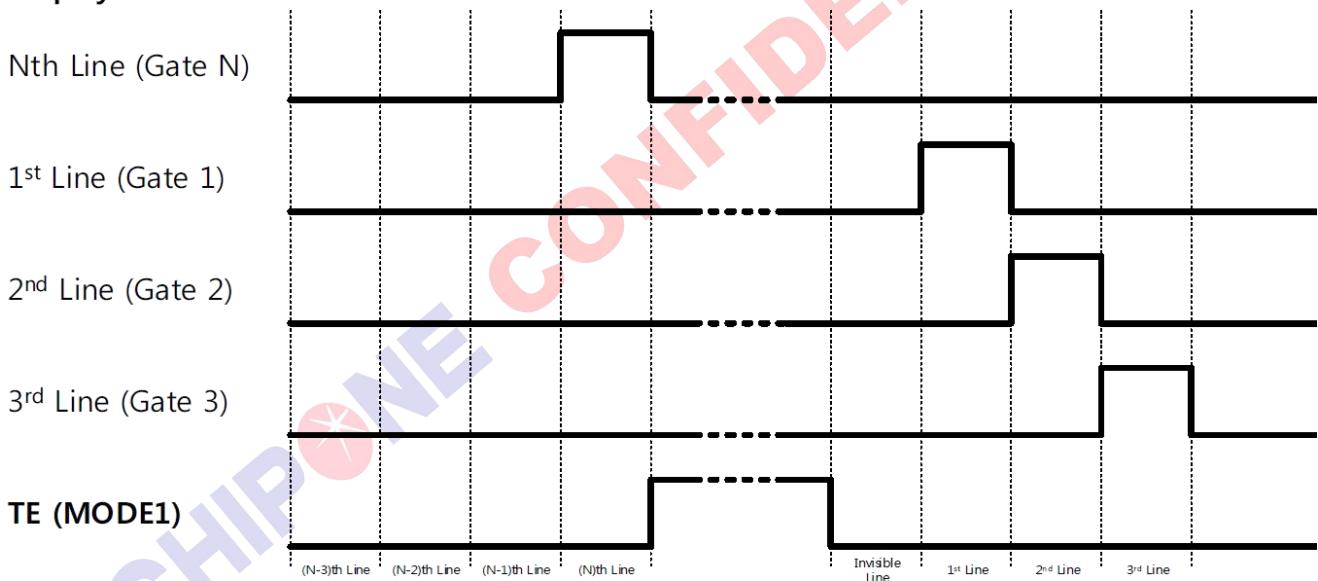
The setting of the tearing effect line is defined by the instructions of:

1. TEOFF (34h)
2. TEON (35h)
3. TESCAN (44h)

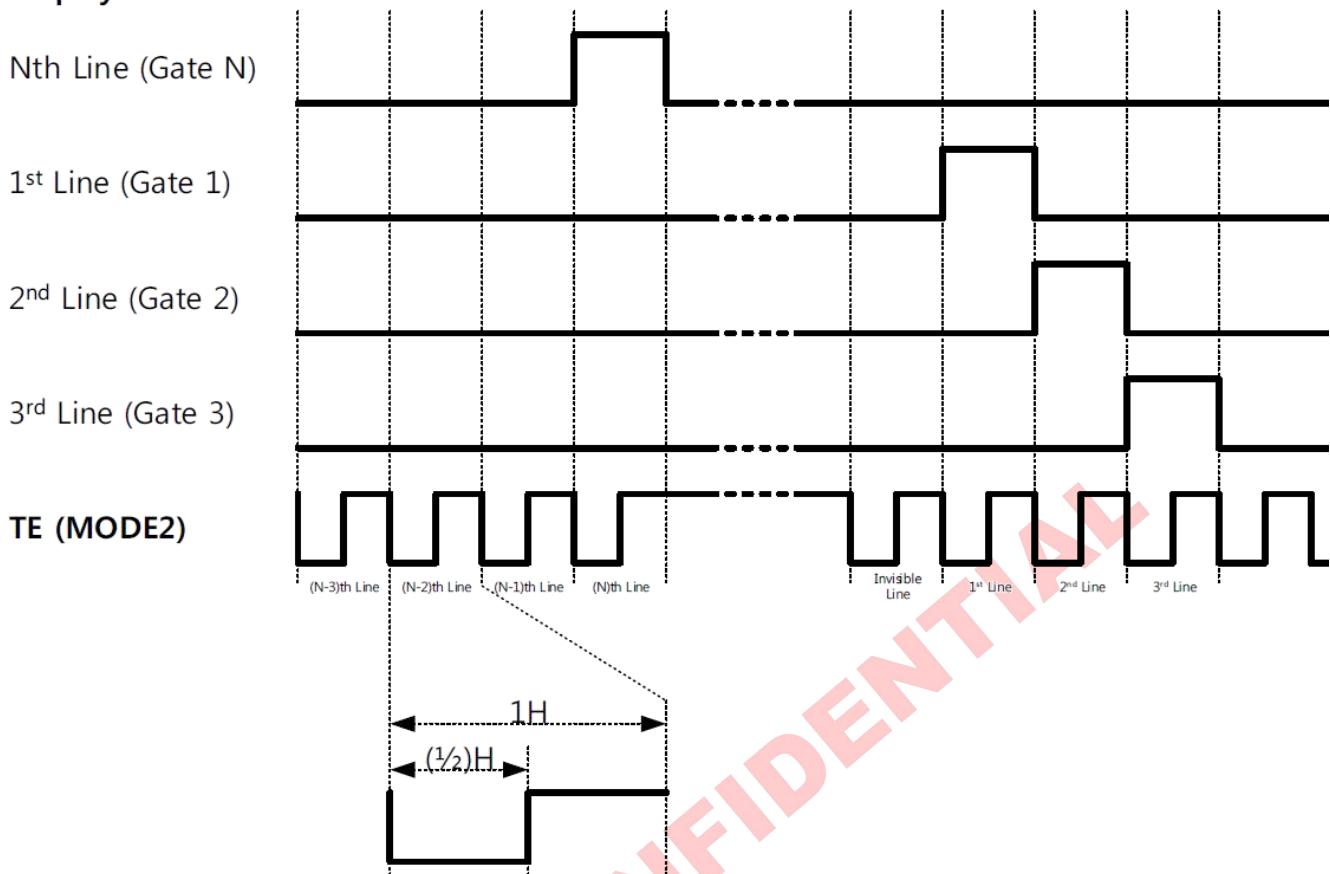
8.1.1 Tearing Effect Line Modes

[Mode 1]: the Tearing Effect Output signal consists of V-Sync and V-Blanking information only:

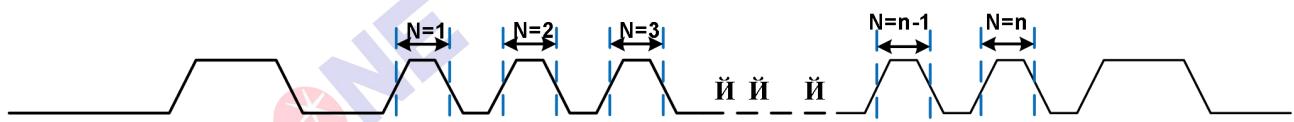
Display Gate Scan



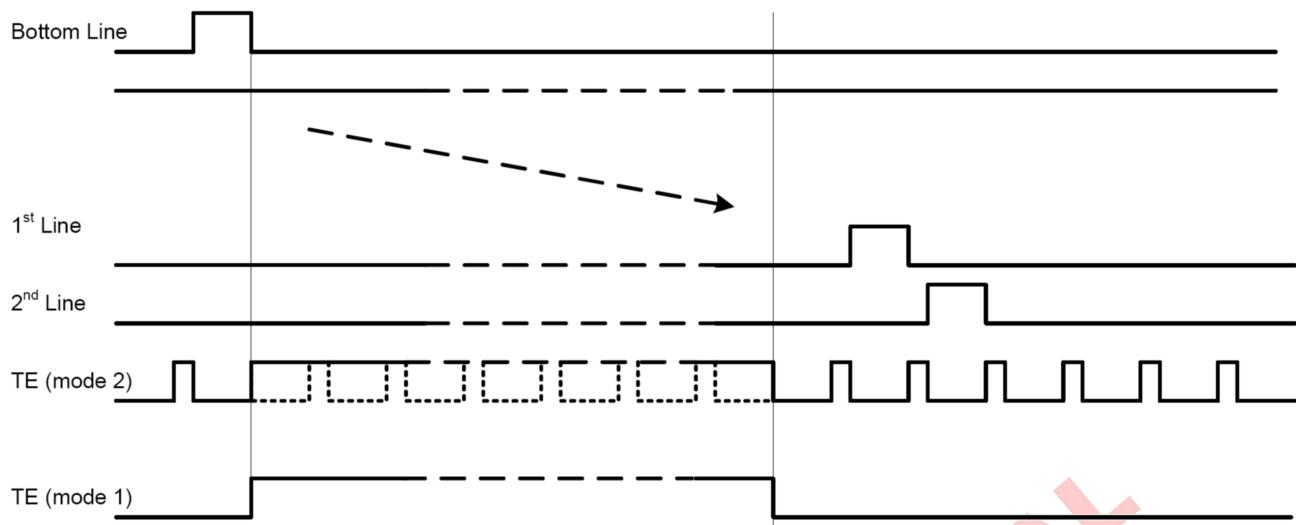
[Mode 2]: the tearing effect output signal consists of V-Blanking and H-Blanking which are included of V-sync and H-sync information:

Display Gate Scan

[Mode 3]: This mode turn on the tearing effect output signal when vertical scanning reaches line N. In the following figure, it shows that TE only output one line period pulse that can be selected by TESCAN (44h).

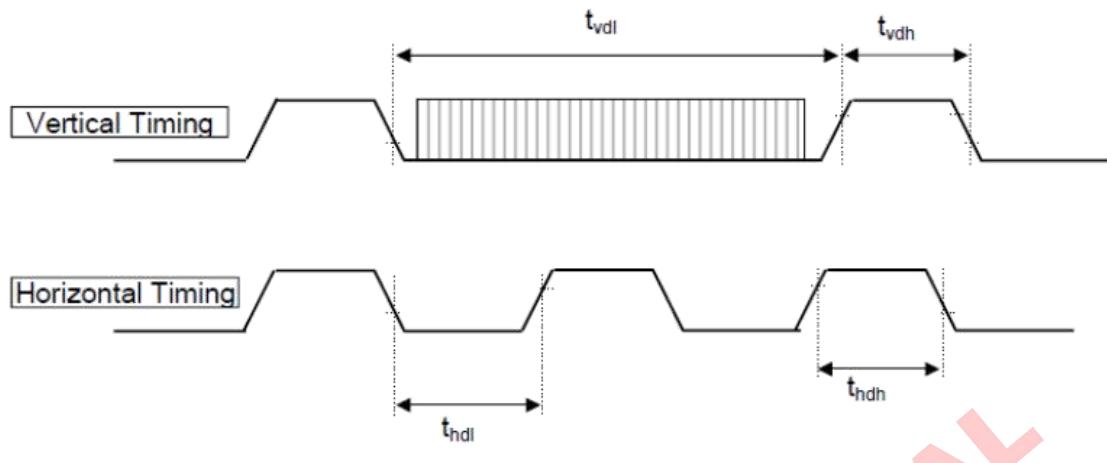


N = the N-th scanning line which set by register TESCAN (44h).



*NOTE: During sleep in mode, the tearing effect output signal is active low.

8.1.2 Tearing Effect Line Timing

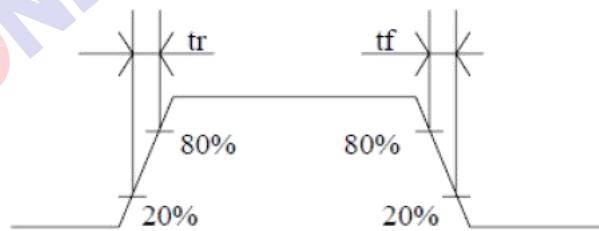


Tearing Effect Line Timing

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Vertical timing low duration	t_{vdl}	—	—	—	μs	
Vertical timing high duration	t_{vdh}	16	—	$VBP[11:0]+VFP[11:0]-1$	hsync	
Horizontal timing low duration	t_{hdl}	—	—	—	μs	
Horizontal timing high duration	t_{hdh}	—	—	1/2	hsync	
Rise time	Tr	—	—	25	ns	$C_{load} = 70\text{pF}$
Fall time	Tf	—	—	25	ns	

*Note:

1. The signal's rise and fall times (tf , tr) are stipulated to be equal to or less than 15 ns.
2. The signal's rise and fall times (tf , tr) are simulation result.



Rise and Fall Times

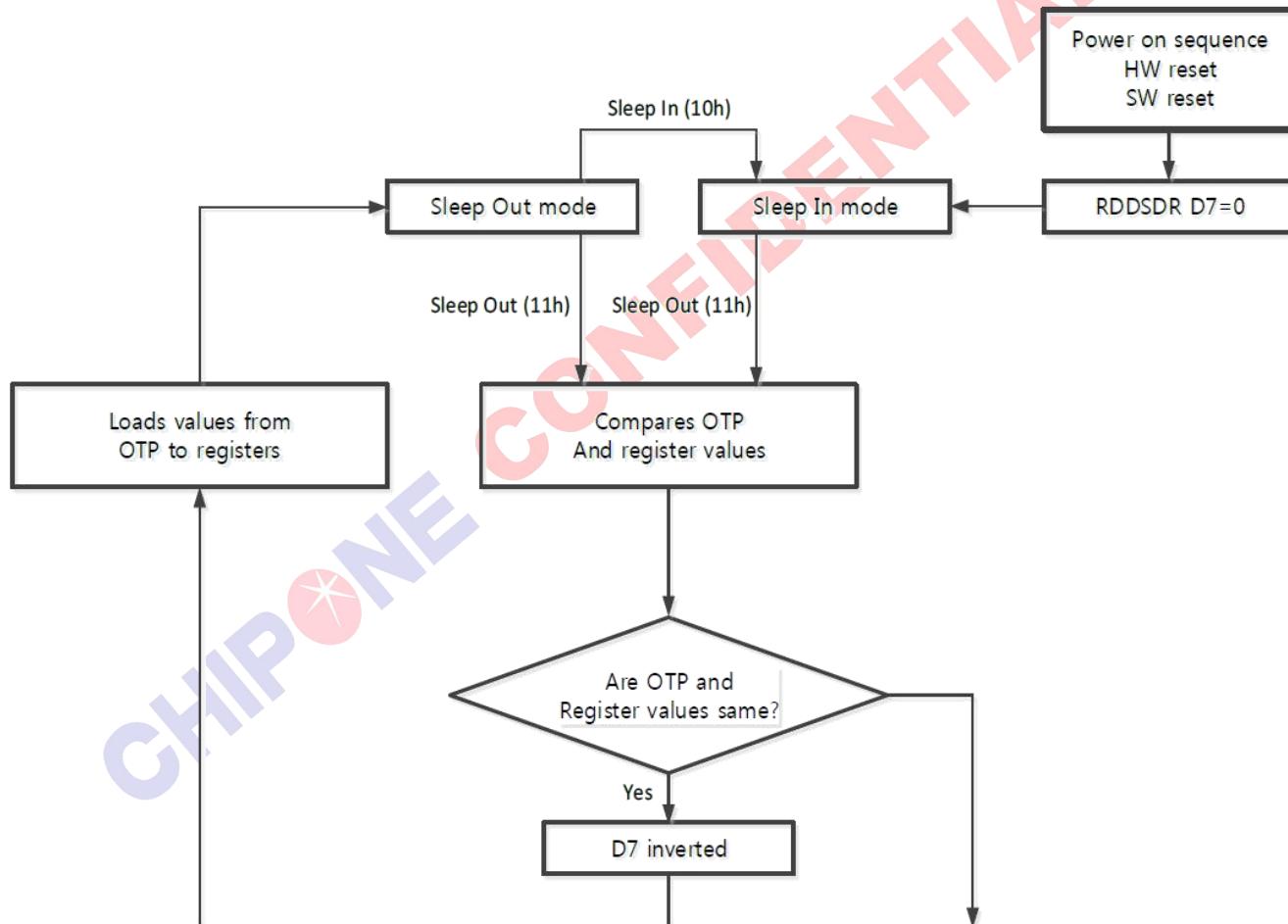
8.2 Sleep Out Command and Self-Diagnostic Functions

8.2.1 Register Loading Detection

Sleep out command is a trigger for an internal function of the display module which indicates, if the display module loading function of factory default values from OTP to registers of the display controller is working properly.

There are compared factory values of the OTP and register values of the display controller by the display controller (1st step: Compares register and OTP) values, 2nd step: Loads OTP value to register. If those both values (OTP and register values) are same, there is inverted (increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0FH)" (RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (not increased by 1).

The flow chart for this internal function is following.



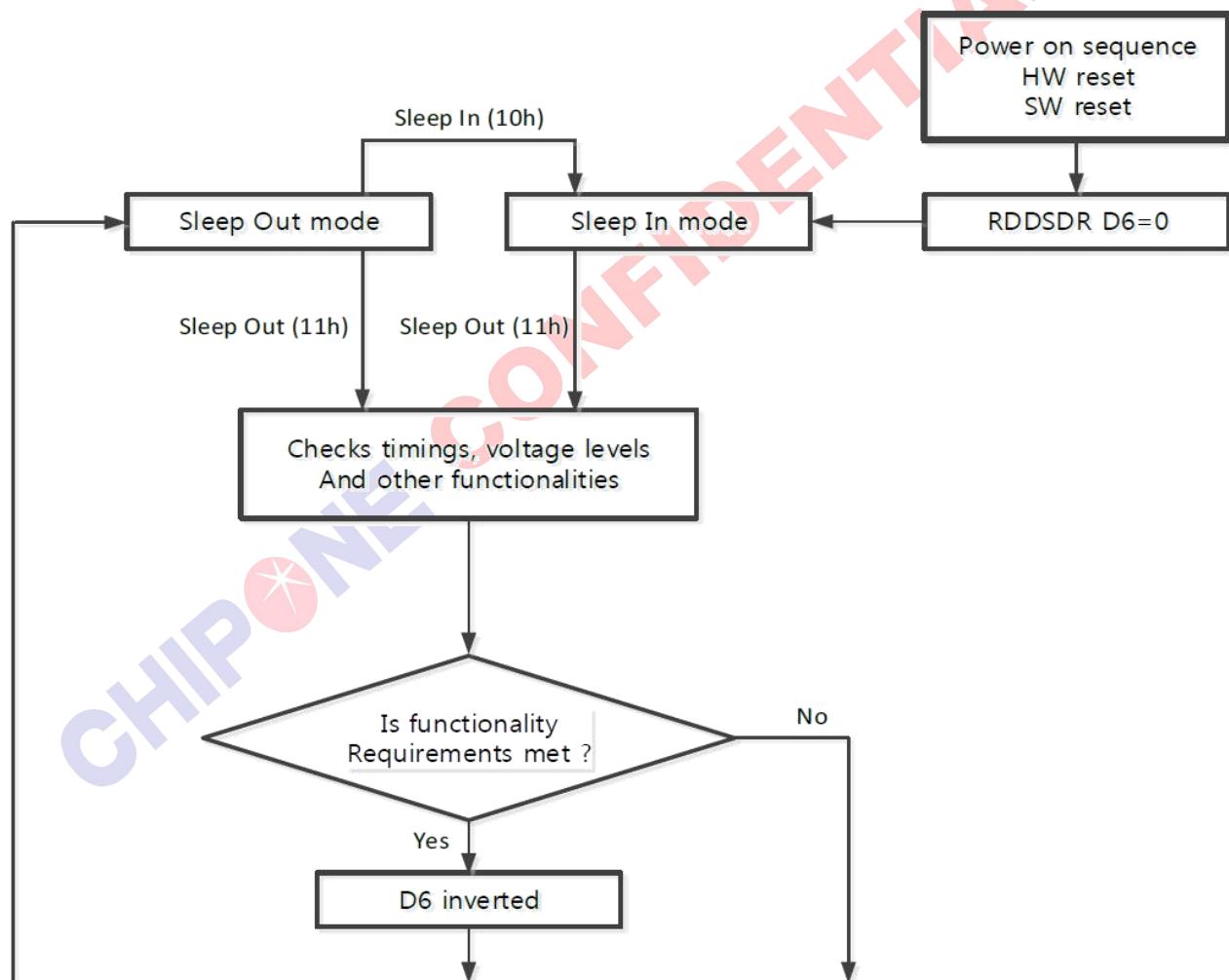
Flowchart of Register Loading Detection

8.2.2 Functionality Detection

Sleep out command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. Step up circuit voltage levels, timings, etc.) If functionality requirement is met, there is inverted (Increased by 1) a bit, which defined in command “Read Display Self-Diagnostic Result (0FH)” (RDDSDR) (the used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= Not increased by 1) and the used TE-line is set to low (registers, what are set by “Tearing Effect Line On (35H)” command, are keeping their current values) when it can only be reactivated “Tearing Effect Line On (35H)” command.

The flow chart for this internal function is following:

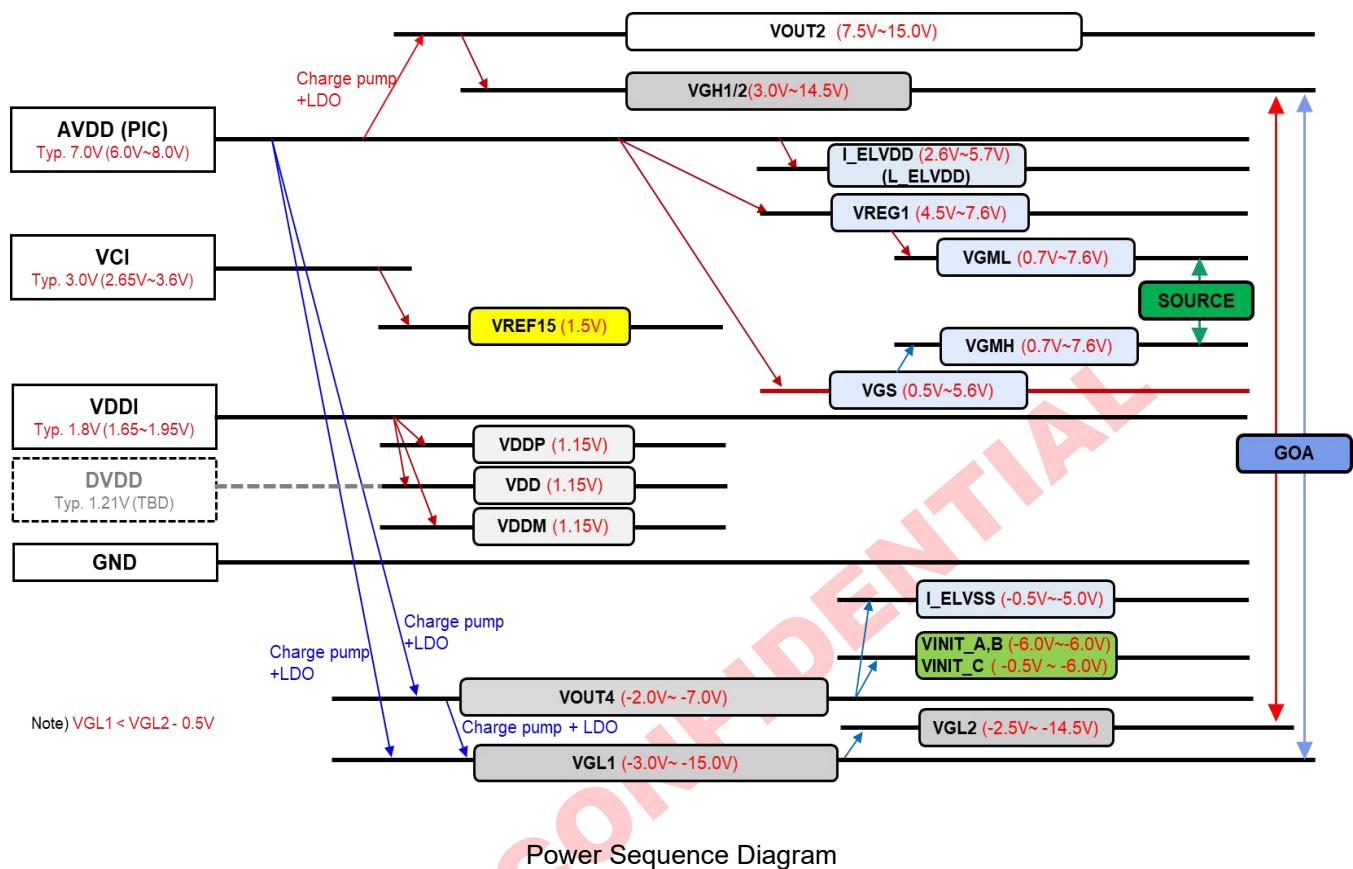


Flowchart of Functionality Detection

*NOTE: There is needed 120ms after sleep out command, when there is changing from sleep in mode to sleep out mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise there is 10ms delay for D6's value when Sleep out command is sent in Sleep out mode.

8.3 Power

8.3.1 Power Generation Diagram



***Note:**

1. VGL1 should be the lowest voltage in the chip.
2. VOUT2 should be the highest voltage in the chip
3. Source Output Range: 0.7V ~ 7.6V

8.3.2 Power ON Sequence

If nRESET line is held high or unstable by the host during power on, then a hardware reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

If nRESET line is held Low (and stable) by the host during Power On, then the nRESET must be held low for minimum 10μsec after both VCI and VDDI have been applied.

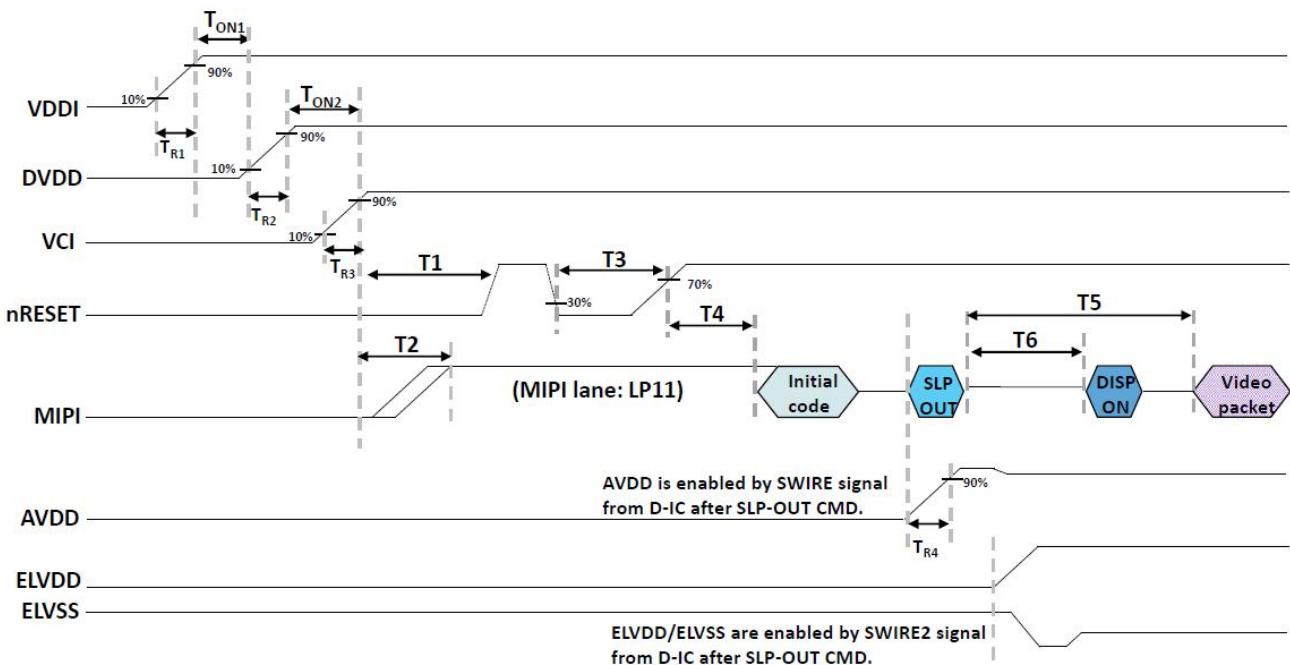
The power on sequence for different power input modes are shown as below.

Power ON Sequence Timing

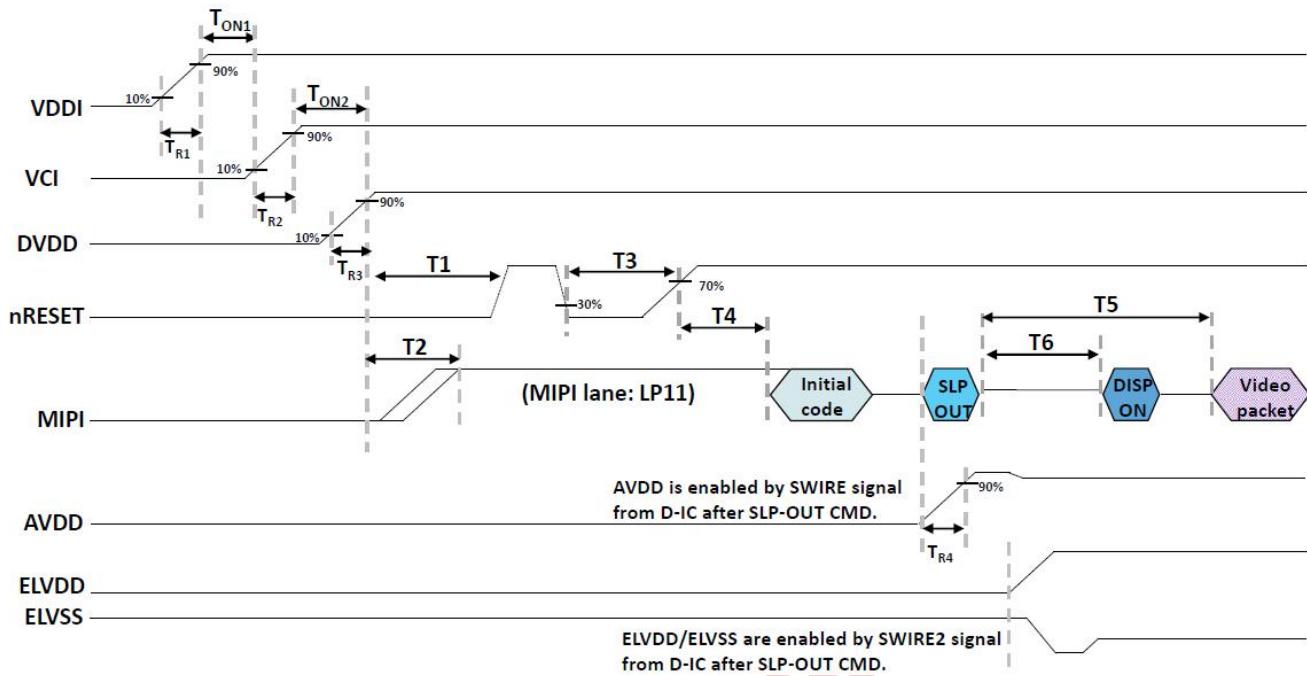
Symbol	Description	Value			Unit	Note
		Min.	Typ.	Max.		
T _{ON1}	VDDI on to DVDD on delay	>0	-	-	μs	
T _{ON2}	CASE1 : DVDD on to VCI on power delay time CASE2 : VCI on to DVDD on power delay time	>0	-	-	ms	
T ₁	CASE1 : VCI on to valid to nRESET high CASE2 : DVDD on to valid to nRESET high	10	-	-	ms	
T ₂	CASE1 : VCI to MIPI bus ready delay CASE2 : DVDD to MIPI bus ready delay	0	-	T ₁	ms	
T ₃	nRESET low period	50	-	-	us	
T ₄	nRESET high to OTP code re-load ready	15	-	-	ms	
T ₅	Sleep-out command received to video packet transmit delay.	80	-	-	ms	
T ₆	Sleep-out command received to display on command transmit delay	>0	-	-	μs	
T _{R1}	VDDI power rising time	0.3	-	2	ms	
T _{R2}	DVDD power rising time	0.3	-	2	ms	
T _{R3}	VCI power rising time	0.3	-	2	ms	
T _{R4}	AVDD power rising time	0.3	-	5	ms	

The Power on sequence is shown as below.

Power On Sequence for External DVDD_CASE1



Power On Sequence for External DVDD_CASE2



Power on sequence

*Note: Unless otherwise specified, timing herein shows cross point at 50% of signal/power level.

8.3.3 Power OFF Sequence

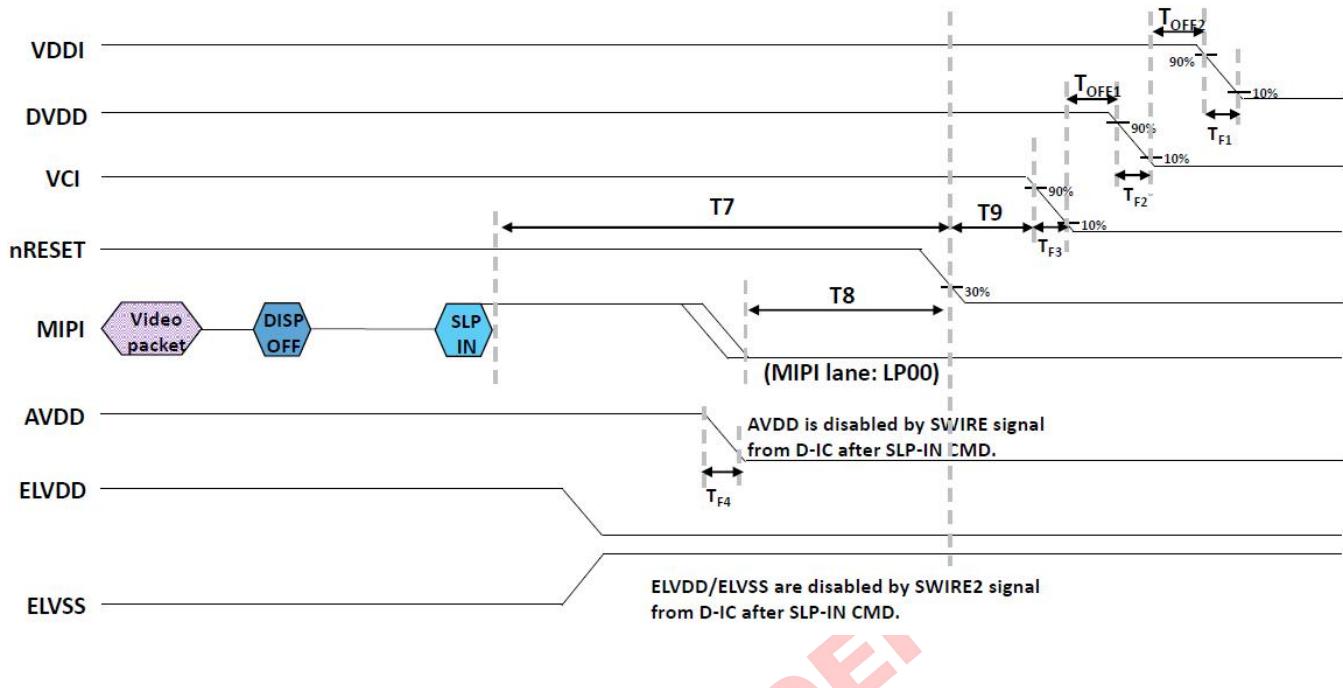
The power off sequence for different power input modes are shown as below.

Power OFF Sequence Timing

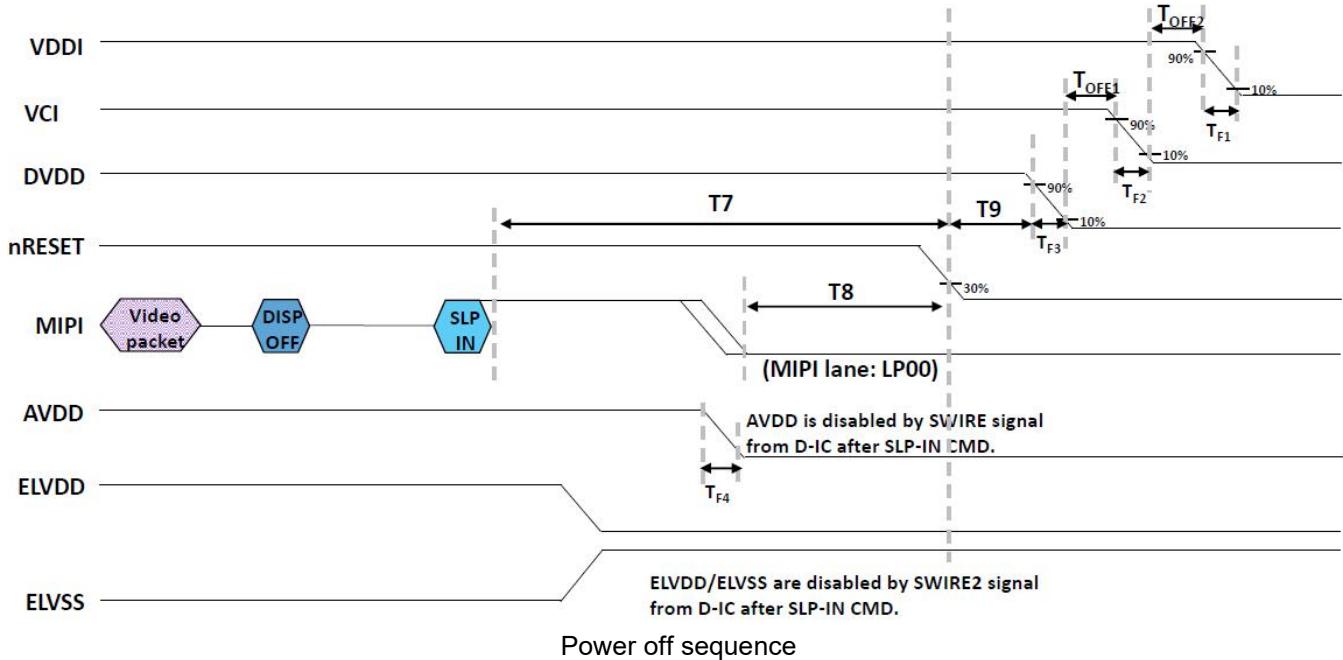
Symbol	Description	Value			Unit	Note
		Min.	Typ.	Max.		
T_{OFF1}	CASE1 : VCI off to DVDD off delay CASE2 : DVDD off to VCI off delay	>0	-	-	μs	
T_{OFF2}	CASE1 : DVDD off to VDDI off delay CASE2 : VCI off to VDDI off delay	>0	-	-	μs	
T_7	Sleep-in command received to valid to nRESET low	100	-	-	ms	
T_8	MIPI ultra low power mode to valid to nRESET low	0	-	-	μs	
T_9	nRESET low to VCI off delay	0	-	-	μs	
T_{F1}	VDDI power falling time	0.3	-	2	ms	
T_{F2}	DVDD power falling time	0.3	-	2	ms	
T_{F3}	VCI power falling time	0.3	-	2	ms	
T_{F4}	AVDD power falling time	0.3	-	5	ms	

The power off sequence is shown as below:

Power Off Sequence for External DVDD_CASE1



Power Off Sequence for External DVDD_CASE2



***Note:**

1. Unless otherwise specified, timing herein shows cross point at 50% of signal/power level.
2. Keep VGH is equal to or larger than VCI during power off sequence.

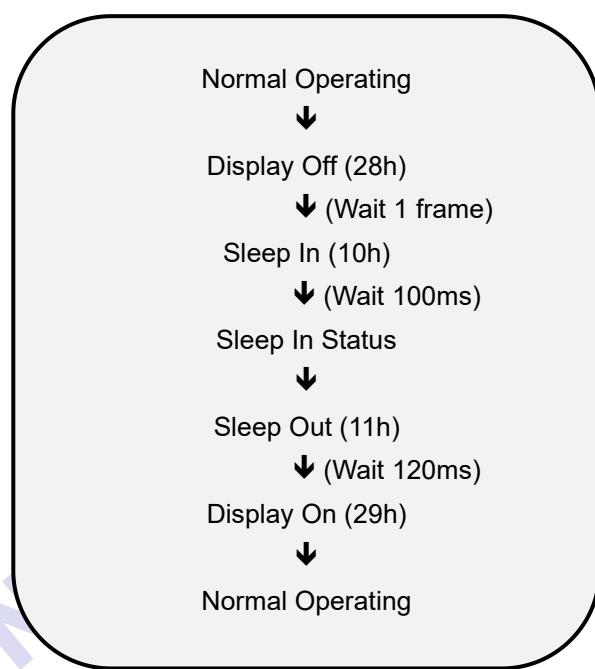
8.3.4 Abrupt Power Off

The abrupt power-off represents a situation where, for e.g. a battery is removed without the expected power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abrupt power-off, the display will go blank and there will not be any visible effects with 1 second on the display (Blank display) and remains blank until "Power-on Sequence" powers it up. Blank display means: For normally white panel, the blank display indicates white display. For normally black panel, the blank display indicates black display.

8.3.5 Sleep In/Out Flow

This DDIC supports sleep mode for low power consumption.

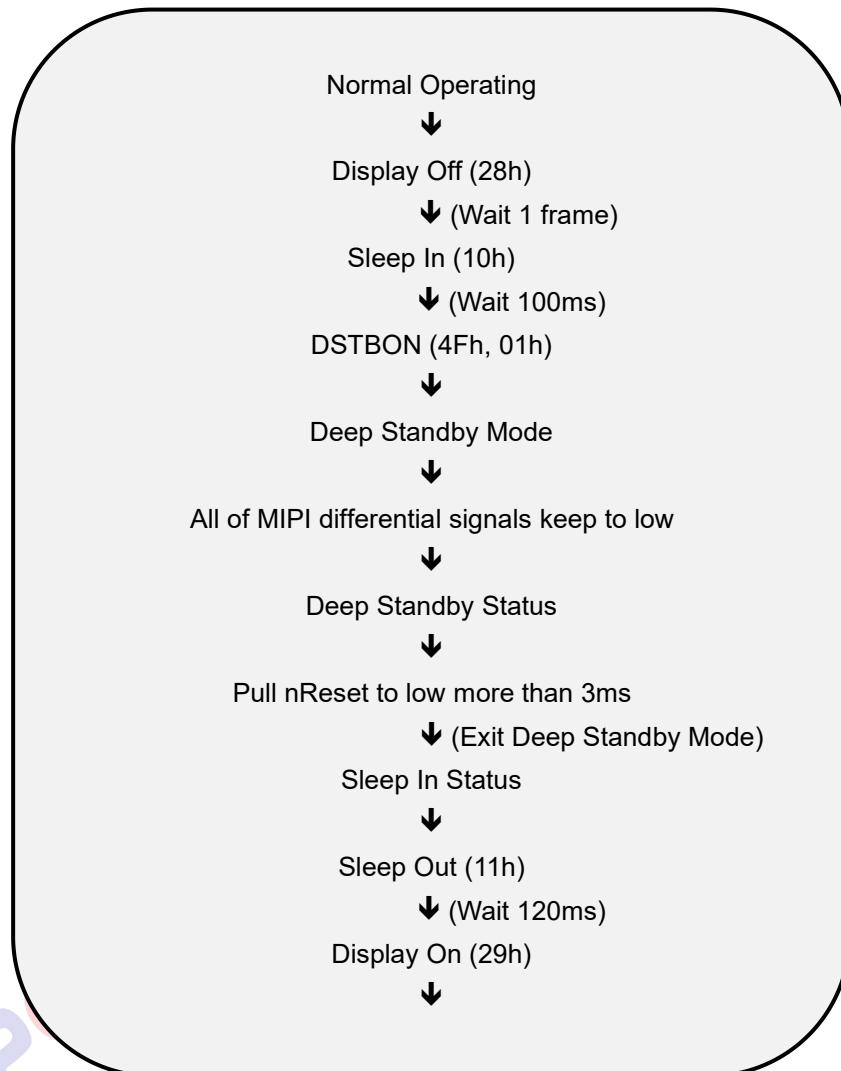
Flow chart of sleep mode



8.3.6 Deep Standby Flow

This DDIC supports deep standby mode for ultra-low power consumption.

Flow chart of deep standby mode



8.4 Source

8.4.1 Source Driver

The source driver circuit consists of 2560 drivers (S<1> to S<2560>). Display data is latched when 2560 channel data has arrived. Then the latched data enables the source drivers to output to expected voltage level. When less than 2560 sources are required, the unused source outputs should be left open and the available source outputs are presented as following table.

Connection between source outputs and AMOLED panel with SPR

Source Output	Panel Connection	Source Output	Panel Connection
Symbol	1280 x RGBG	Symbol	1080 x RGBG
VSSDUMMY...	Leave it open	VSSDUMMY...	Leave it open
S<1>	R1	S<1>	R1
S<2>	G1	S<2>	G1
S<3>	B2	S<3>	B2
S<4>	G2	S<4>	G2
S<5>	R3	S<5>	R3
S<6>	G3	S<6>	G3
...
S<1275>	B638	S<1075>	B538
S<1276>	G638	S<1076>	G538
S<1277>	R639	S<1077>	R539
S<1278>	G639	S<1078>	G539
S<1279>	B720	S<1079>	B540
S<1280>	G720	S<1080>	G540
VSSDUMMY...	Leave it open	VSSDUMMY...	Leave it open
S<1281>	R721	S<1481>	R541
S<1282>	G721	S<1482>	G541
S<1283>	B722	S<1483>	B542
S<1284>	G722	S<1484>	G542
S<1285>	R723	S<1485>	R543
S<1286>	G723	S<1486>	G543
...
S<2555>	B1278	S<2555>	B1078
S<2556>	G1278	S<2556>	G1078
S<2557>	R1279	S<2557>	R1079
S<2558>	G1279	S<2558>	G1079
S<2559>	B1280	S<2559>	B1080
S<2560>	G1280	S<2560>	G1080
VSSDUMMY...	Leave it open	VSSDUMMY...	Leave it open

*Note: Horizontal Resolution:720+4N RGBG

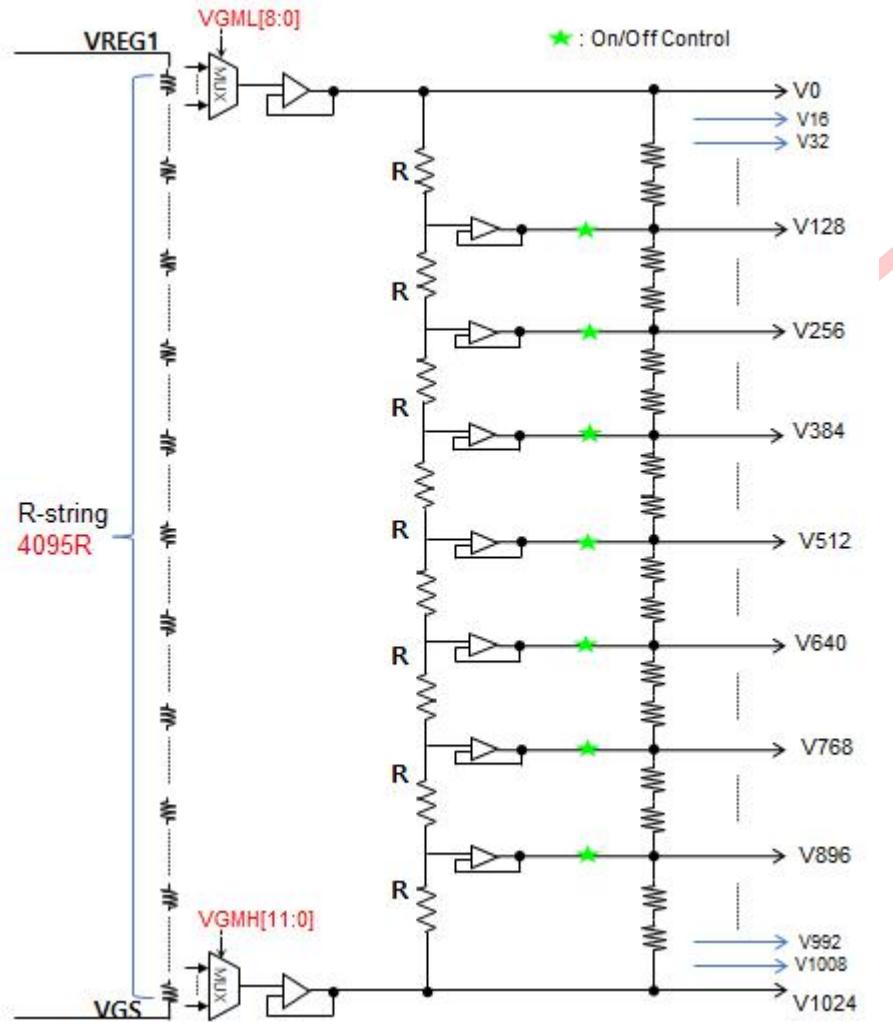
8.4.2 Gamma Adjustment Function

This DDIC provides the gamma adjustment function to display 16.7M colors simultaneously for each R/G/B color. The gamma adjustment executed by the high/mid/low level adjustment registers determines grayscale reference levels. Furthermore, you can adjust them to match AMOLED panel and a gamma for each R/G/B color, respectively.

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8.4.3 Structure of Grayscale Generator

The structure of grayscale generator is shown as below. This has totally 9 voltage taps. These 9 voltage levels (V0-V1023) between VREG1 and VGS are determined by the reference adjustment register, the amplitude adjustment register, the micro-adjustment register. These tap voltage levels make 1024 gray levels ranging from V0 to V1023 with the internal ladder resistor network.



Structure of Grayscale generator

8.5 One-Time Programmable (OTP) Control

This DDIC has an embedded OTP (One Time Programmable Device, EG0016K8TA04DDY03A) which is consist of one OTP IP (16K x 8bit) in eMemory Technology Inc. The EG0016K8TA04DDY03A is programmed by 1.1V, 3.3V power supply and 6V external VPP high voltage supply.

DC Specification

Operating Mode	Power Pin	Min.	Typ.	Max.	Unit
Read mode	VDD	0.99	1.1	1.21	V
	VDD2	2.3	3.3	4.8	V
	VPP	VDD2/VSS/Floating			
	VSS	0			V
Write mode	VDD	0.99	1.1	1.21	V
	VDD2	1.62	3.3	4.8	V
	VPP	5.75	6	6.25	V
	VSS	0			V

8.5.1 OTP Address Configuration

This DDIC's OTP control IP support auto write function from logic register to OTP cell. The number of auto write for each IP is different. Auto write time of each IP is supported 1 ~ 8 times.

Items	Description
Size	• 16K-byte One-Time Programmable (OTP) NVM
ID1	• OTP 8 times
ID2, ID3	• OTP 3 times
MIPI	• OTP 1 time & FLASH
TCON	• OTP 1time & FLASH
DSC	• OTP 1time & FLASH
DGM, PIC	• OTP 1time & FLASH
GAMMA	• Only FLASH
PWM, BC	• OTP 1 time & FLASH
CASCADE	• OTP 1 time & FLASH
ODC,CTB	• OTP 1 time & FLASH
SPR	• OTP 1 time & FLASH
RN	• OTP 1 time & FLASH
IE	• OTP 1 time & FLASH
DEMURA	• OTP 1 time & FLASH

*Note: Please refer the ICNA3512 Application Note of the OTP programming.

9. Command

9.1 List of User Command

Operational Code is abbreviated by OpCode, Read/Write/Command is abbreviated by RWC, and Number of Parameter bytes is abbreviated by Num. of Para.

List of User Command (Level-1)

OpCode (Hex)	Command	RWC	Num. of Para.	Description
00h	NOP	C	0	No Operation
01h	SWRESET	C	0	Software Reset
05h	RDNUMPE	R	1	Read Number of the Errors on Primary DSI
0Ah	RDDPM	R	1	Read Display Power Mode
0Bh	RDDMADCTL	R	1	Read Display Memory Access Control
0Dh	RDDIM	R	1	Read Display Image Mode
0Eh	RDDSM	R	1	Read Display Signal Mode
0Fh	RDDSDR	R	1	Read Display Self-Diagnostic Result
10h	SLPIN	C	0	Sleep In
11h	SLPOUT	C	0	Sleep Out
12h	PTLON	C	0	Partial Mode On
13h	NORON	C	0	Normal Mode On
20h	INVOFF	C	0	Display Inversion Off
21h	INVON	C	0	Display Inversion On
22h	ALLPOFF	C	0	All Pixel Off
23h	ALLPON	C	0	All Pixel On
28h	DISPOFF	C	0	Display Off
29h	DISPON	C	0	Display On
2Ah	COSET	W	4	Write Column Address Set
2Bh	PASET	W	4	Write Page Address Set
2Ch	RAMWR	W	Variable	Memory Write
30h	PTLAR	W	4	Write Partial Area Row Set
31h	PTLAC	W	4	Write Partial Area Column Set
32h	RTE	C	0	Request TE
34h	TEOFF	C	0	Tearing Effect Line Off
35h	TEON	W	1	Write Tearing Effect Line On
36h	MADCTL	W	1	Memory Data Access Control
38h	IDLEOFF	C	0	Idle Mode Off
39h	IDLEON	C	0	Idle Mode On
3Ch	RAMWRC	W	1	Memory Write Continue
40h	WRREGION	W	1	Write Multi Region Value

41h	RDREGION	R	1	Read Multi Region Value
42h	WRUPSCM	W	1	Write Scale-up Value
43h	RDUPSCM	R	1	Read Scale-up Value
44h	TESCAN	W	2	Write Tear Scanline
45h	RDTESCAN	R	3	Read Scanline
48h	WRDSIM	W	1	Write DSI MODE
49h	RDDSIM	R	1	Read DSI MODE
4Fh	DSTBON	W	1	Write Deep Standby On
51h	WRDISBV	W	5	Write Display Brightness
52h	RDDISBV	R	5	Read Display Brightness Value
53h	WRCTRL	W	1	Write Control Display
54h	RDCTRL	R	1	Read Control Display Value
55h	WRACL	W	2	Write ACL Value
56h	RDACL	R	2	Read ACL Value
57h	WRIE	W	1	Write IE Value
58h	RDIE	R	1	Read IE Value
59h	WRCM	W	1	Write CM Value
5Ah	RDCM	R	1	Read CM Value
5Dh	WRMCL	W	2	Write MCL Value
5Eh	RDMCL	R	2	Read MCL Value
63h	WRLTPOMD	W	1	Write LTPO Value
64h	RDLTPOMD	R	1	Read LTPO Value
65h	WRMANDLY	W	5	WR MAN Delay Value
66h	RDMANDLY	R	5	RD MAN Delay Value
68h	RDMANVTEO	R	2	RD MAN VTE Value
69h	WRMSYNC	W	1	Write MSYNC Value
6Ah	RDMSYNC	R	1	Read MSYNC Value
6Bh	WRQSYNC	W	1	Write QSYNC Value
6Ch	RDQSYNC	R	1	Read QSYNC Value
6Dh	WRQSYNCTO	W	4	Write QSYNC Timeout Value
6Eh	RDQSYNCTO	R	4	Read QSYNC Timeout Value
71h	WRTEMP	W	1	Write TEMP Value
72h	RDTEMP	R	1	Read TEMP Value
73h	RDWCX	R	1	Read W Coor. X
74h	RDWCY	R	1	Read W Coor. Y
76h	RDRCX	R	1	Read R Coor. X
77h	RDRCY	R	1	Read R Coor. Y
78h	RDGCX	R	1	Read G Coor. X
79h	RDGCY	R	1	Read G Coor. Y

7Bh	RDBCX	R	1	Read B Coor. X
7Ch	RDWBCY	R	1	Read B Coor. Y
80h	OSC CALIB	W	1	Write OSC Calibration Value
84h	RDBRL	R	1	Read BR Low Byte
85h	RDBRH	R	1	Read BR High Byte
8Fh	RDERRFLAG	R	1	Read Error Flag Status
90h	AODSET	W	1	Write AOD Value
91h	WRVR_CTRL	W	1	Write VR Value
92h	RDVR_CTRL	R	1	Read VR Value
93h	WRRNEN	W	1	Write RN Value
94h	RDRNEN	R	1	Read RN Value
95h	WTECC_WT	W	1	Write ECC Value
96h	RDECC_WT	R	1	Read ECC Value
97h	WRFPS	W	3	Write FPS Value
98h	RDFPS	R	3	Read FPS Value
99h	WRFPSOFFSET	W	4	Write FPS Offset Value
9Ah	RDFPSOFFSET	R	4	Read FPS Offset Value
9Bh	PARA_SEL	W	1	MCS Parameter Selection (Only Use Chipone)
9Ch	UCS LOCK	W	1	UCS Lock (Only Use Chipone)
9Dh	WRFPSCGAIN	W	4	Write FPS Gain Value
9Eh	RDFPSCGAIN	R	4	Read FPS Gain Value
9Fh	REG SEL	W	1	MCS Group Selection (Only Use Chipone)
A0h	RDDIC	R	27	Read DIC Info.
A1h	RDDDB	R	24	Read DDB Start
A2h	RDPPS	R	Variable	Read PPS
A8h	RDDDBC	R	Variable	Read DDB Continue
A9h	RDPPSC	R	Variable	Read Continue PPS
AAh	RDFCS	R	Variable	Read First Checksum
AFh	RDCCS	R	Variable	Read Continue Checksum
B1h	RDID_IPX	R	19	Read ID Value (Hidden)
DAh	RDID1	R	1	Read ID1
DBh	RDID2	R	1	Read ID2
DCh	RDID3	R	1	Read ID3
FDh	MCS LOCK	W	1	MCS Lock (Only Use Chipone)

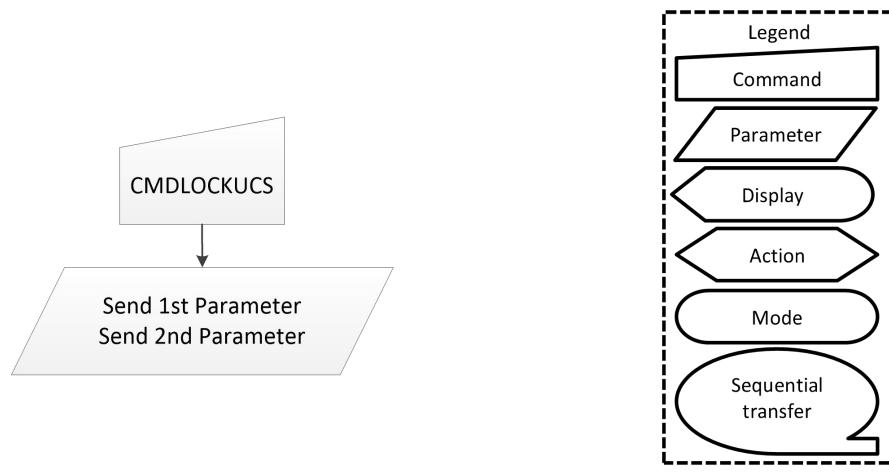
*Note: Parameters of the command are stored onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break.

9.2 User Command and Manufacture Command Access

9.2.1 (9Ch) CMDLOCKUCS: User Command Access

Command Set		CMDLOCKUCS								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
CMDLOCKUCS	W	1	0	0	1	1	1	0	0	9Ch
Parameter	1	UCS LOCK[7:0]								

NOTE: “-”Don’t care.

Description	This command is used to lock or unlock the User Command (Level-1) Sets.	
	Instruction	Parameter
	9Ch	UCS LOCK[7:0]
	9Ch	UCS LOCK[7:0]
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	PIN1: A5h, PIN2: A5h
	S/W Reset	PIN1: A5h, PIN2: A5h
	H/W Reset	PIN1: A5h, PIN2: A5h
Flow Chart		Legend Command Parameter Display Action Mode Sequential transfer

9.2.2 (FDh) CMDLOCKMCS: Manufacture Command Access

Command Set		CMDLOCKMCS									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
CMDLOCKMCS	W	1	1	1	1	1	1	0	1	FDh	
Parameter	1	MCS_LOCK[7:0]									

NOTE: “-”Don’t care.

Description	This command is used to lock or unlock the Manufacture Command (Level-2) Sets.			
	Instruction	Parameter	Value	Description
	FDh	MCS_LOCK[7:0]	5Ah, 5Ah	Lock Disable
Restriction	-			
Register Availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	
Default	Status		Default Value	
	Power On Sequence		PIN1: 5Ah, PIN2: 5Ah	
	S/W Reset		PIN1: 5Ah, PIN2: 5Ah	
	H/W Reset		PIN1: 5Ah, PIN2: 5Ah	
Flow Chart				

9.3 Description of User Command

9.3.1 (00h) NOP: No Operation

Command Set		NOP								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
NOP	C	0	0	0	0	0	0	0	0	00h
Parameter	-	No Parameter								

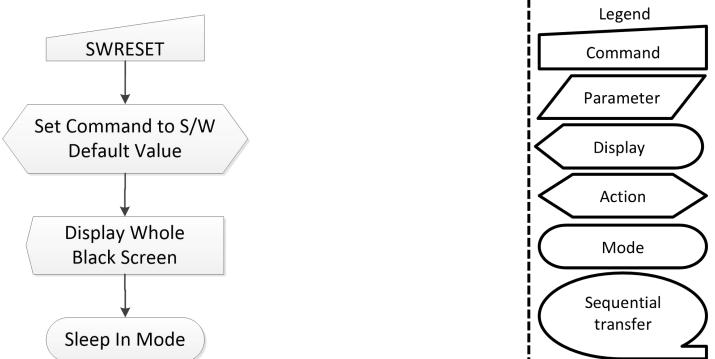
NOTE: “-”Don’t care.

Description	This command is an empty command. It does not have any effect on the display module.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>NA</td> </tr> <tr> <td>S/W Reset</td> <td>NA</td> </tr> <tr> <td>H/W Reset</td> <td>NA</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	NA	S/W Reset	NA	H/W Reset	NA				
Status	Default Value													
Power On Sequence	NA													
S/W Reset	NA													
H/W Reset	NA													
Flow Chart	 <pre> graph TD NOP[NOP] --> NonAction{Non-Action} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.2 (01h) SWRESET: Software Reset

Command Set		SWRESET								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
SWRESET	C	0	0	0	0	0	0	0	1	01h
Parameter	-	No Parameter								

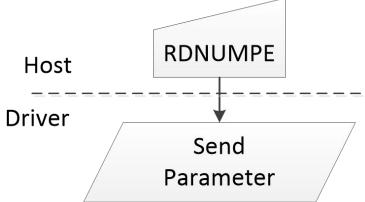
NOTE: “-”Don’t care.

Description	When the software reset command is written, it causes a software reset. It resets the commands and parameters to their S/W reset default values. (See default tables in each command description)													
Restriction	<p>It will be necessary to wait 5m second before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5m second in sleep in status.</p> <p>If software reset is applied during sleep out mode, it will be necessary to wait 120m second before sending sleep out command.</p> <p>Software reset command cannot be sent during sleep out sequence.</p>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													
Flow Chart	 <pre> graph TD SWRESET([SWRESET]) --> Set[Set Command to S/W Default Value] Set --> Display[Display Whole Black Screen] Display --> Sleep[Sleep In Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.3 (05h) RDNUMPE: Read Number of the Errors on Primary DSI

Command Set		RDNUMPE									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDNUMPE	R	0	0	0	0	0	1	0	1	05h	
Parameter	1	NUMED[7:0]									

NOTE: “-”Don’t care.

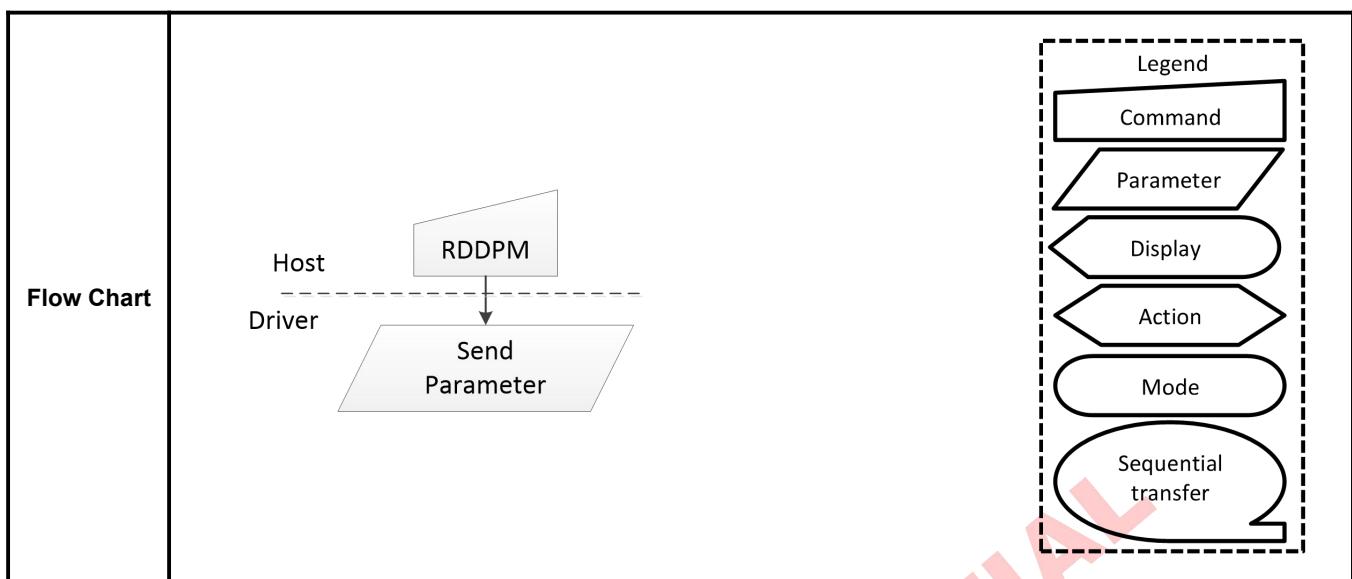
Description	This command returns the number of corrupted packets previously received on the DSI link. For each parameter, NUMED[7] is set to ‘1’ if there is overflow with NUMED[6:0] bits.													
Restriction	Only ECC single-bit errors, ECC multi-bit errors and Checksum errors are included in the error counter functionality.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host[Host] -- RDNUMPE --> Driver[Driver] Driver -- "Send Parameter" --> Send[Send Parameter] </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.4 (0Ah) RDDPM: Read Display Power Mode

Command Set		RDDPM									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDDPM	R	0	0	0	0	1	0	1	0	0Ah	
Parameter	1	BVST	IDLEON	PTLON	SLPOUT	NORON	DISPON	0	0	08h	

NOTE: “-”Don’t care.

	This command indicates the current status of the display as described in the table below:												
Description	Bit	Description											
	D7	Booster Voltage Status “1” = Booster on, “0” = Booster off											
	D6	Idle Mode On/Off “1” = Idle Mode On, “0” = Idle Mode Off											
	D5	Partial Mode On/Off “1” = Partial Mode On, “0” = Partial Mode Off											
	D4	Sleep In/Out “1” = Sleep Out, “0” = Sleep In											
	D3	Display Normal Mode On/Off “1” = Normal Display On, “0” = Normal Display Off											
	D2	Display On/Off “1” = Display On, “0” = Display Off											
	D1	Not Used “0”											
Restriction	D7 bit, Booster Voltage Status, keeps “1” after booster is normally enabled in spite of going back to sleep status. This bit is only initialized by reset.												
	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>98h</td> </tr> <tr> <td>S/W Reset</td> <td>08h</td> </tr> <tr> <td>H/W Reset</td> <td>08h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	98h	S/W Reset	08h	H/W Reset	08h			
Status	Default Value												
Power On Sequence	98h												
S/W Reset	08h												
H/W Reset	08h												

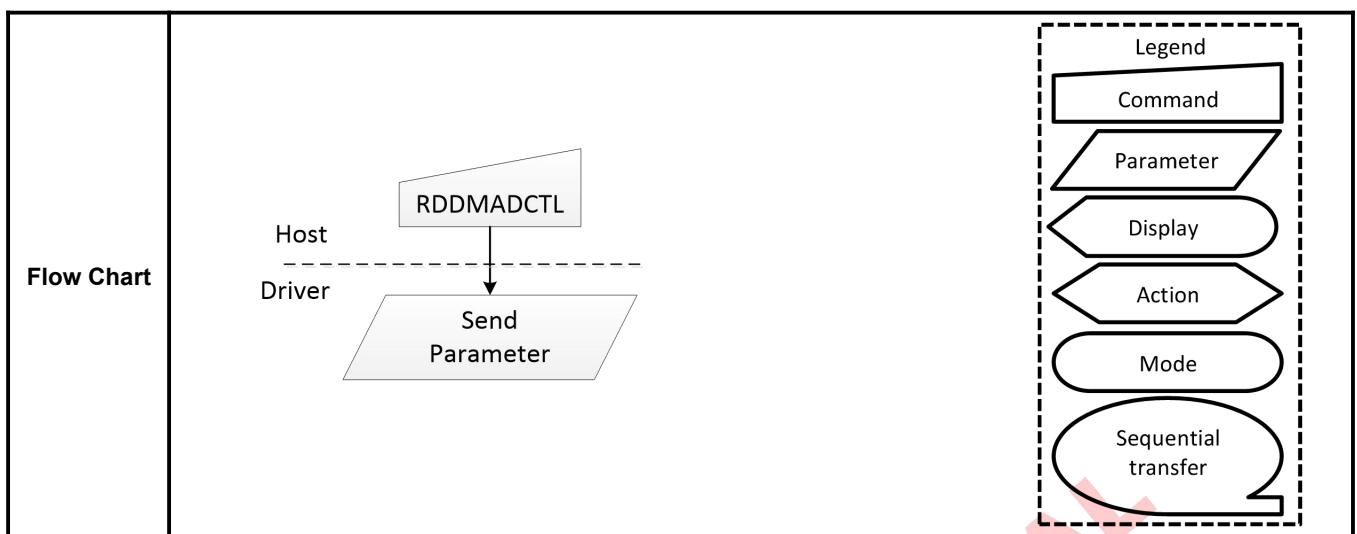


9.3.5 (0Bh) RDDMADCTL: Read Display Memory Access Control

Command Set		RDDMADCTL									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDDMADCTL	R	0	0	0	0	1	0	1	1	0Bh	
Parameter	1	0	0	0	0	0	0	FH	0	00h	

NOTE: “-”Don’t care.

Description	This command indicates the current status of the display as described in the table below:													
	Bit	Description												
	D7	Not Used												
	D6	Not Used												
	D5	Not Used												
	D4	Not Used												
	D3	Not Used												
	D2	Not Used												
	D1	FH												
	D0	Not Used												
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

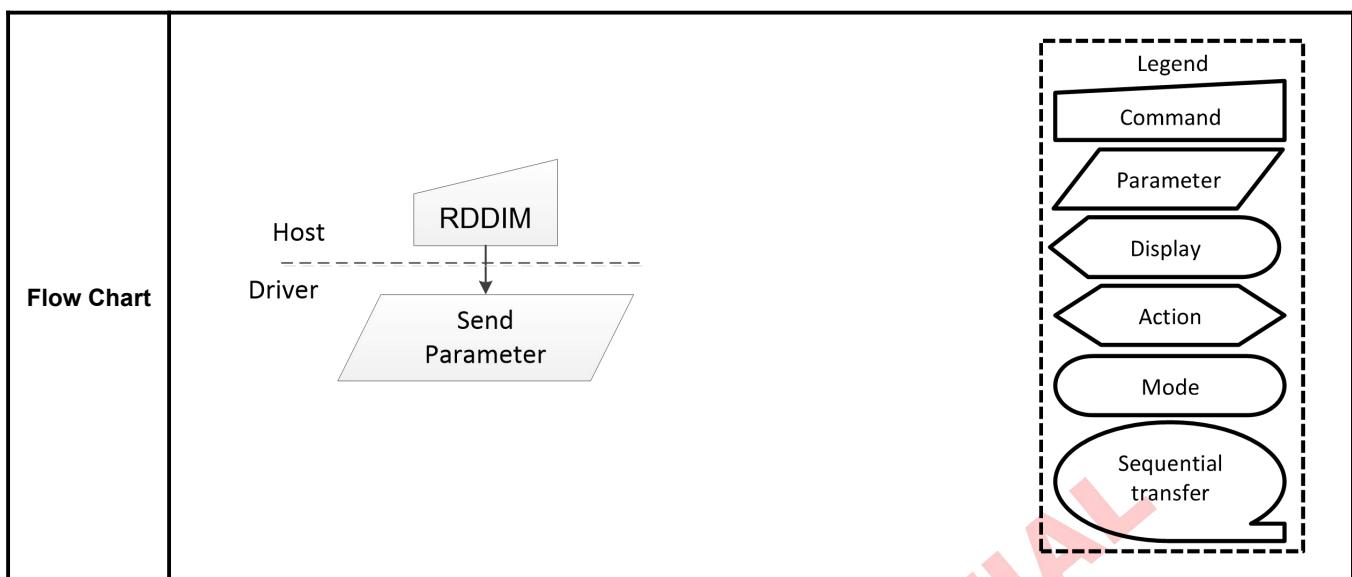


9.3.6 (0Dh) RDDIM: Read Display Image Mode

Command Set		RDDIM								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDDIM	R	0	0	0	0	1	1	0	1	0Dh
Parameter	1	0	0	0	ALLPON	ALLPOFF	0	0	0	00h

NOTE: “-”Don’t care.

Description	This command indicates the current status of the display as described in the table below:													
	Bit	Description												
	D7	Not Used												
	D6	Not Used												
	D5	Not Used												
	D4	All Pixels On												
	D3	All Pixels Off												
	D2	Not Used												
	D1	Not Used												
	D0	Not Used												
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

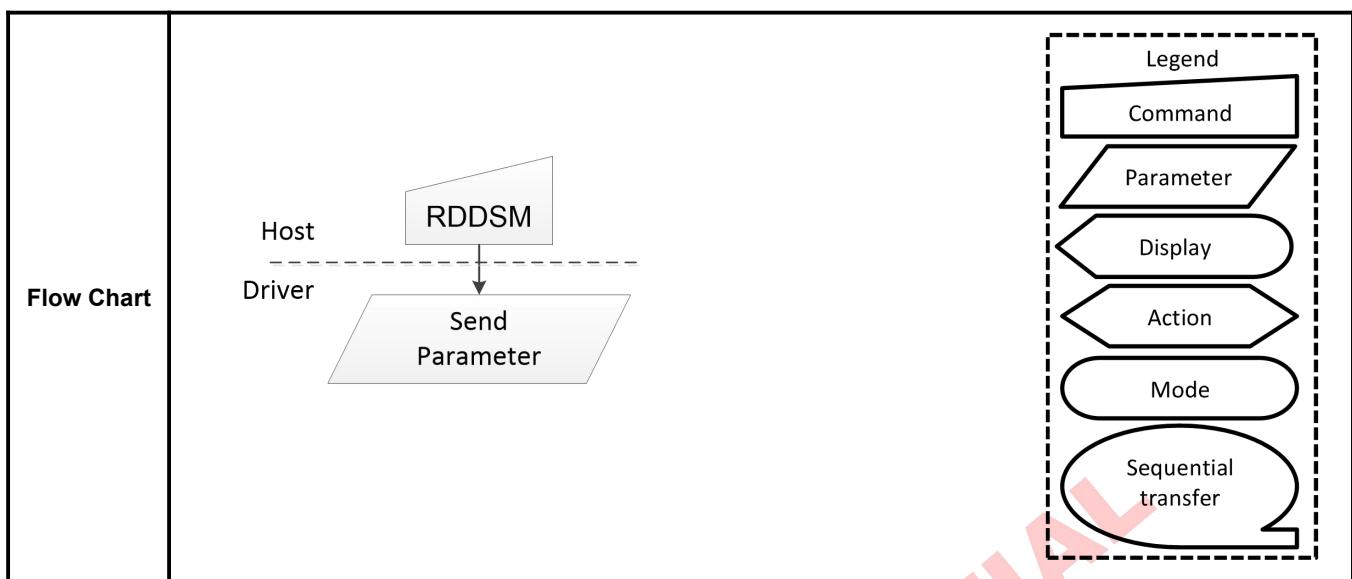


9.3.7 (0Eh) RDDSM: Read Display Signal Mode

Command Set		RDDSM									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDDSM	R	0	0	0	0	1	1	1	0	0Eh	
Parameter	1	0	0	0	0	0	0	0	DSIE	00h	

NOTE: “-”Don’t care.

Description	This command indicates the current status of the display as described in the table below:													
	Bit	Description												
	D7	Not Used												
	D6	Not Used												
	D5	Not Used												
	D4	Not Used												
	D3	Not Used												
	D2	Not Used												
	D1	Not Used												
	D0	Error on DSI “1” = Error, “0” = No Error												
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

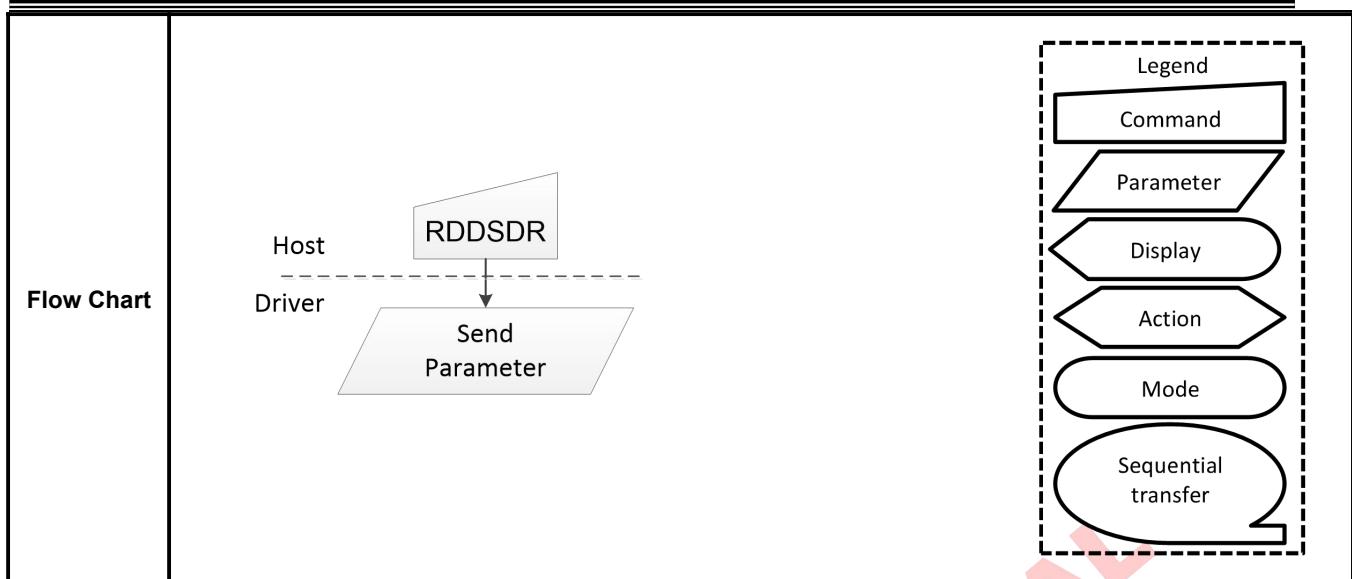


9.3.8 (0Fh) RDDSDR: Read Display Self-Diagnostic Result

Command Set		RDDSDR								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDDSDR	R	0	0	0	0	1	1	1	1	0Fh
Parameter	1	RLDT	FNDT	0	0	0	0	0	CKSUM	00h

NOTE: “-”Don’t care.

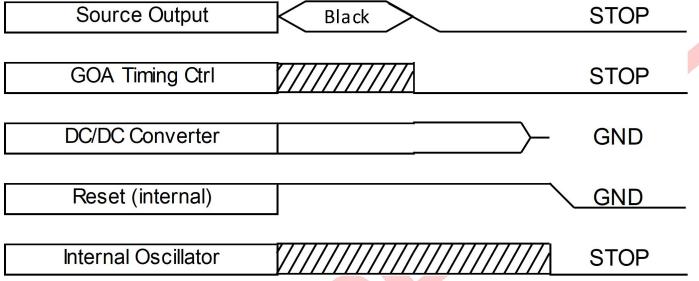
Description	This command indicates the status of the display self-diagnostic results after Sleep Out – command														
	Bit	Description	Value												
	D7	Register Loading Detection	“0” = OTP & Register are not same “1” = OTP & Register are same												
	D6	Functionality Detection	“0” = Booster voltage levels, timing is not met “1” = Booster voltage levels, timing is met												
	D5	Not Used	“0”												
	D4	Not Used	“0”												
	D3	Not Used	“0”												
	D2	Not Used	“0”												
	D1	Not Used	“0”												
	D0	Checksums comparison	“0” = Checksums are same “1” = Checksums are not same												
Restriction	-														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>			Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value														
Power On Sequence	00h														
S/W Reset	00h														
H/W Reset	00h														

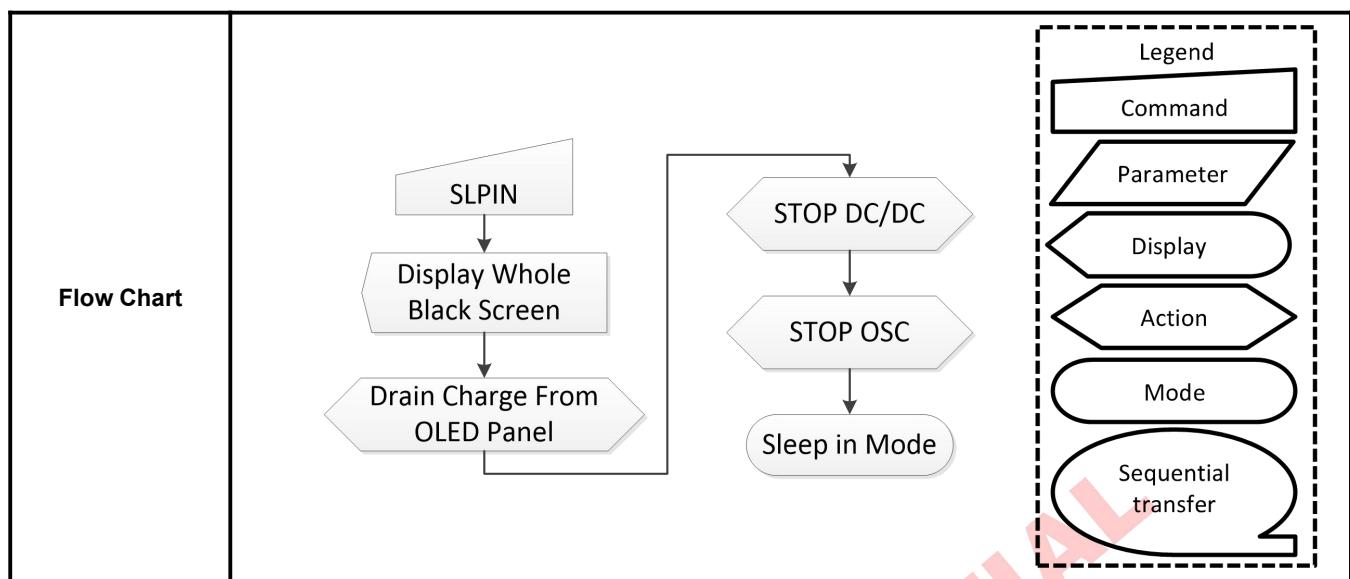


9.3.9 (10h) SLPIN: Sleep In

Command Set		SLPIN									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
SLPIN	C	0	0	0	1	0	0	0	0	10h	
Parameter	-	No Parameter									

NOTE: “-”“Don’t care.

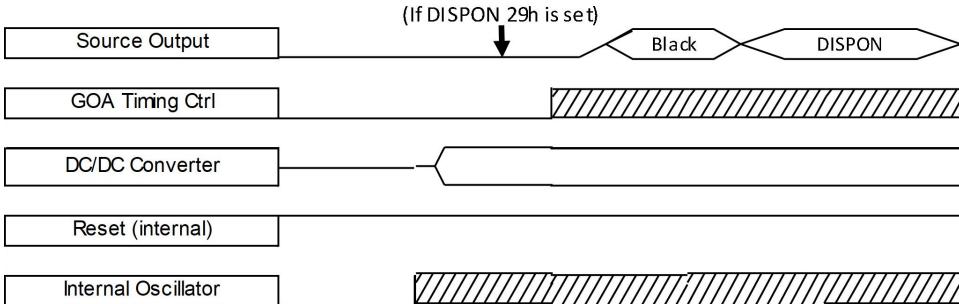
Description	<p>This command causes the AMOLED module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped. The control Interface such as registers is still working and keeps its values.</p> 												
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by “SLPOUT (11h)”. It will be necessary to wait 5m second before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120m second after sending sleep out command (When in sleep in mode) before sleep in command can be sent.</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode				
Status	Default Value												
Power On Sequence	Sleep In Mode												
S/W Reset	Sleep In Mode												
H/W Reset	Sleep In Mode												

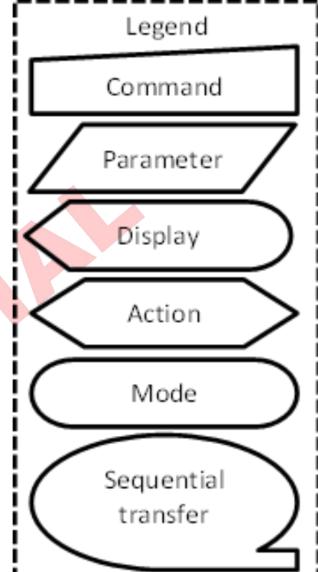


9.3.10 (11h) SLPOUT: Sleep Out

Command Set		SLPOUT								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
SLPOUT	C	0	0	0	1	0	0	0	1	11h
Parameter	-	No Parameter								

NOTE: “-”Don’t care.

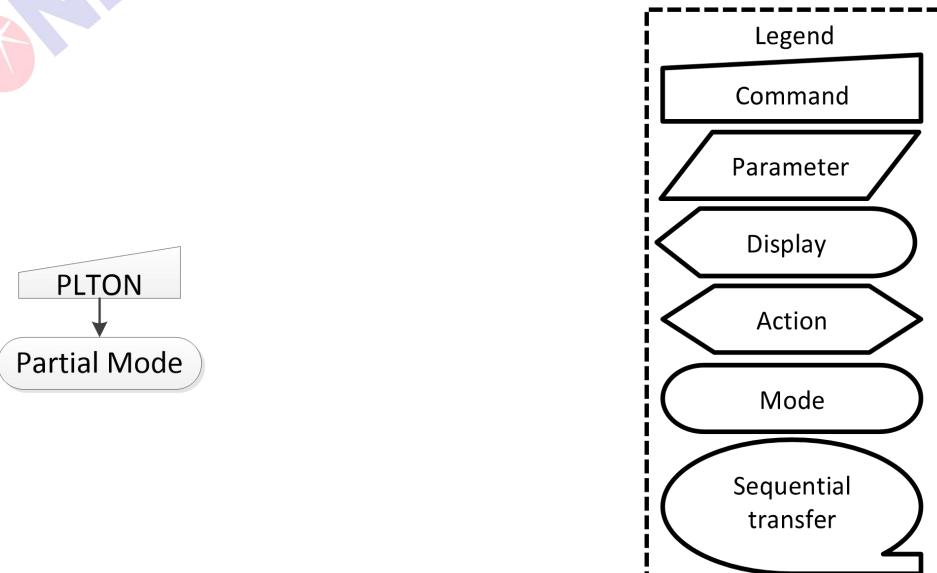
Description	<p>This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</p> 												
Restriction	<p>This command has no effect when AMOLED module is already in sleep out mode. Sleep out mode can only be exit by the sleep in command (10h). It will be necessary to wait 5m second before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. This DDIC loads all default values of extended and test command to the registers during this 5m second and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when it is already sleep out mode. This DDIC is doing self-diagnostic functions during this 5m second. It will be necessary to wait 120m second after sending sleep in command (when in sleep out mode) before sleep out command can be sent.</p>												
Register Availability	<table border="1" data-bbox="446 1545 1367 1821"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

Default	Status	Default Value
	Power On Sequence	Sleep In Mode
	S/W Reset	Sleep In Mode
	H/W Reset	Sleep In Mode
Flow Chart	<pre>graph TD; S1[SLPOUT] --> S2{OSC Enable}; S2 --> S3{DC/DC Enable};</pre>	<pre>graph TD; S1[Charge Offset Voltage for OLED Panel] --> S2{Display Whole Black Screen}; S2 --> S3[Sleep Out Mode];</pre>
		

9.3.11 (12h) PTION: Partial Mode On

Command Set		PTION									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
PTION	C	0	0	0	1	0	0	1	0	12h	
Parameter	-	No Parameter									

NOTE: “-”Don’t care.

Description	This command turns on partial mode. The partial mode window is described by the partial area command (30h). To leave partial mode, the normal display mode command (13h) should be written.													
Restriction	This command has no effect on when Partial Display mode is active.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal display mode on</td> </tr> <tr> <td>S/W Reset</td> <td>Normal display mode on</td> </tr> <tr> <td>H/W Reset</td> <td>Normal display mode on</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Normal display mode on	S/W Reset	Normal display mode on	H/W Reset	Normal display mode on				
Status	Default Value													
Power On Sequence	Normal display mode on													
S/W Reset	Normal display mode on													
H/W Reset	Normal display mode on													
Flow Chart	 <pre> graph TD PLTON[PLTON] --> PartialMode([Partial Mode]) subgraph Legend [Legend] direction TB L1[Command] L2[Parameter] L3[Display] L4[Action] L5[Mode] L6[Sequential transfer] end </pre>													

9.3.12 (13h) NORON: Normal Mode On

Command Set		NORON								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
NORON	C	0	0	0	1	0	0	1	1	13h
Parameter	-	No Parameter								

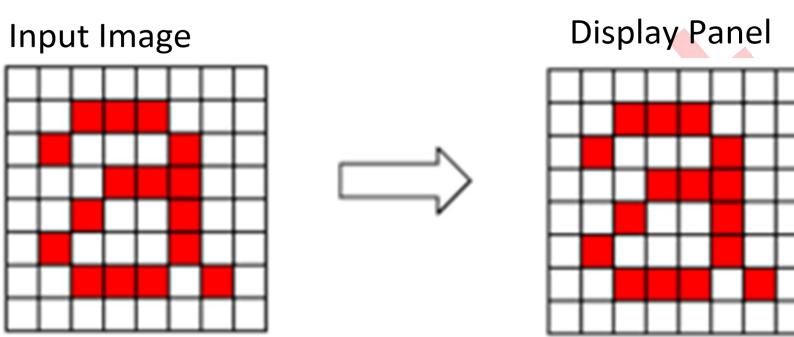
NOTE: “-”Don’t care.

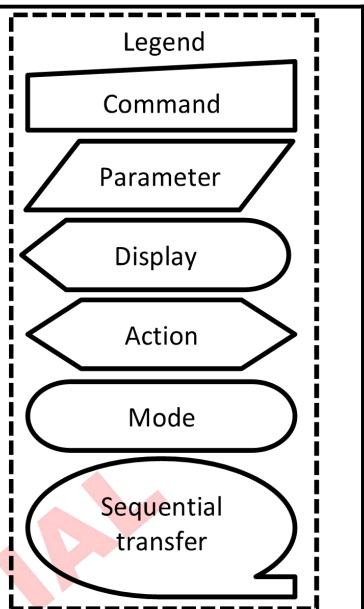
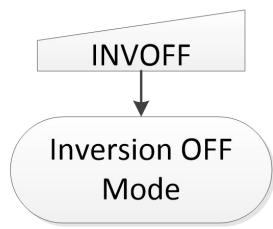
Description	This command returns the display to normal mode. To leave partial mode or all pixel on/off mode, the normal display mode command (13h) should be written.													
Restriction	This command has no effect on when Normal Display mode is active.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal display mode on</td> </tr> <tr> <td>S/W Reset</td> <td>Normal display mode on</td> </tr> <tr> <td>H/W Reset</td> <td>Normal display mode on</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Normal display mode on	S/W Reset	Normal display mode on	H/W Reset	Normal display mode on				
Status	Default Value													
Power On Sequence	Normal display mode on													
S/W Reset	Normal display mode on													
H/W Reset	Normal display mode on													
Flow Chart	<pre> graph TD NORON[NORON] --> NormalDisplayMode((Normal Display Mode)) </pre> <p>The flowchart shows a rectangular box labeled "NORON" with a downward-pointing arrow. This arrow points to an oval labeled "Normal Display Mode". To the right of the flowchart is a legend enclosed in a dashed box:</p> <ul style="list-style-type: none"> Legend Command Parameter Display Action Mode Sequential transfer 													

9.3.13 (20h) INVOFF: Display Inversion Off

Command Set		INVOFF								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
INVOFF	C	0	0	1	0	0	0	0	0	20h
Parameter	-	No Parameter								

NOTE: “-”Don’t care.

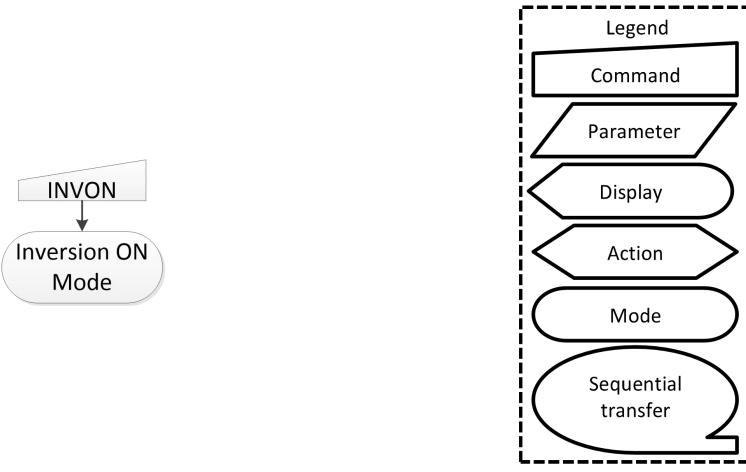
Description	<p>This command is used to recover from display inversion mode. This command makes no change of contents of frame memory, also output is not changed. This command does not change any other status.</p> <div style="text-align: center; margin-top: 20px;">  </div>												
Restriction	This command has no effect when module is already the display image.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d3d3d3;">Status</th> <th style="background-color: #d3d3d3;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d3d3d3;">Status</th> <th style="background-color: #d3d3d3;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off				
Status	Default Value												
Power On Sequence	Display Inversion off												
S/W Reset	Display Inversion off												
H/W Reset	Display Inversion off												

Flow Chart

9.3.14 (21h) INVON: Display Inversion On

Command Set		INVON								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
INVON	C	0	0	1	0	0	0	0	1	21h
Parameter	-	No Parameter								

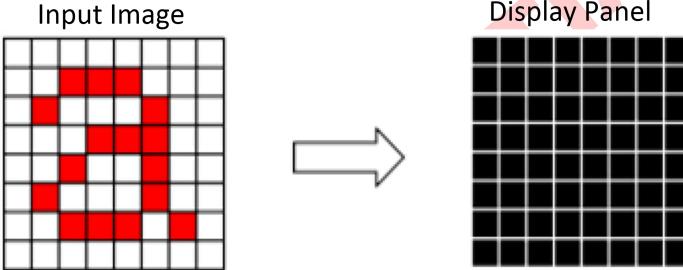
NOTE: “-”Don’t care.

Description	This command is used to enter display inversion mode. This command makes no change of contents of frame memory, but changes output. Ex) 00_00_00 -> FF_FF_FF This command does not change any other status. To exit from display inversion on, the display inversion off command (20h) should be written.													
Restriction	This command has no effect when module is already inverting the display image.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off				
Status	Default Value													
Power On Sequence	Display Inversion off													
S/W Reset	Display Inversion off													
H/W Reset	Display Inversion off													
Flow Chart	 <pre> graph TD INVON[INVON] --> InversionONMode((Inversion ON Mode)) style InversionONMode fill:none,stroke:none </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

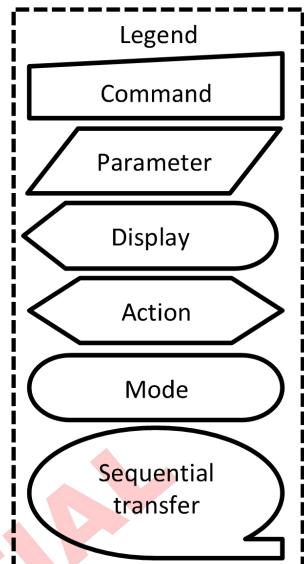
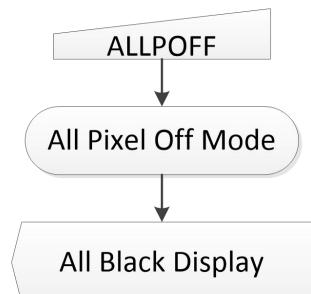
9.3.15 (22h) ALLPOFF: All Pixel Off

Command Set		ALLPOFF									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
ALLPOFF	C	0	0	1	0	0	0	1	0	22h	
Parameter	-	No Parameter									

NOTE: “-”Don’t care.

Description	<p>This command turns the display panel black in sleep out mode and a status of the display on/off register can be "on" or "off".</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>All pixel on, normal display mode on commands are used to leave this mode. The display panel is showing the content of the frame memory after normal display on command.</p> <div style="text-align: center; margin-top: 20px;">  </div>												
Restriction	This command has no effect when module is already in all pixel off mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>All Pixel Off</td></tr> <tr> <td>S/W Reset</td><td>All Pixel Off</td></tr> <tr> <td>H/W Reset</td><td>All Pixel Off</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	All Pixel Off	S/W Reset	All Pixel Off	H/W Reset	All Pixel Off				
Status	Default Value												
Power On Sequence	All Pixel Off												
S/W Reset	All Pixel Off												
H/W Reset	All Pixel Off												

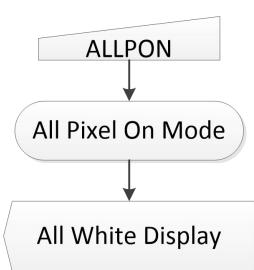
Flow Chart



9.3.16 (23h) ALLPON: All Pixel On

Command Set		ALLPON									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
ALLPON	C	0	0	1	0	0	0	1	1	23h	
Parameter	-	No Parameter									

NOTE: “-”Don’t care.

Description	This command turns the display panel white in sleep out mode and a status of the display on/off register can be "on" or "off". This command does not change any other status. "All Pixels Off" or "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode.													
Restriction	This command has no effect when module is already in all pixel on mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>All Pixel Off</td> </tr> <tr> <td>S/W Reset</td> <td>All Pixel Off</td> </tr> <tr> <td>H/W Reset</td> <td>All Pixel Off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	All Pixel Off	S/W Reset	All Pixel Off	H/W Reset	All Pixel Off				
Status	Default Value													
Power On Sequence	All Pixel Off													
S/W Reset	All Pixel Off													
H/W Reset	All Pixel Off													
Flow Chart	 <pre> graph TD ALLPON[ALLPON] --> APOM[All Pixel On Mode] APOM --> AW[All White Display] </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.17 (28h) DISPOFF: Display Off

Command Set		DISPOFF								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
DISPOFF	C	0	0	1	0	1	0	0	0	28h
Parameter	-	No Parameter								

NOTE: “-”Don’t care.

Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output is disabled and blank page inserted. This command does not change any other status. There will be no abnormal visible effect on the display.													
Restriction	This command has no effect when module is already in display off mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value													
Power On Sequence	Display Off													
S/W Reset	Display Off													
H/W Reset	Display Off													
Flow Chart	<pre> graph TD A[DISPOFF] --> B([Display Off Mode]) B --> C[All Black Display] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.18 (29h) DISPON: Display On

Command Set		DISPON									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
DISPON	C	0	0	1	0	1	0	0	1	29h	
Parameter	-	No Parameter									

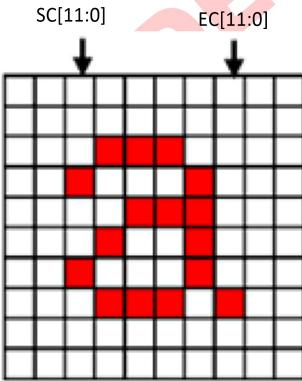
NOTE: “-”Don’t care.

Description	This command causes the display module to start displaying the image data on the display device. This command does not change any other status.													
Restriction	This command has no effect when module is already in display on mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value													
Power On Sequence	Display Off													
S/W Reset	Display Off													
H/W Reset	Display Off													
Flow Chart	 <pre> graph TD A[DISPON] --> B([Display On Mode]) style A fill:#fff,stroke:#000,stroke-width:1px style B fill:#fff,stroke:#000,stroke-width:1px </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.19 (2Ah) COSET: Write Column Address Set

Command Set		COSET								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
COSET	W	0	0	1	0	1	0	1	0	2Ah
Parameter	1	0	0	0	0	SC[11:8]				00h
Parameter	2	SC[7:0]						00h		
Parameter	3	0	0	0	0	EC[11:8]				05h
Parameter	4	EC[7:0]						9Fh		

NOTE: “-”Don’t care.

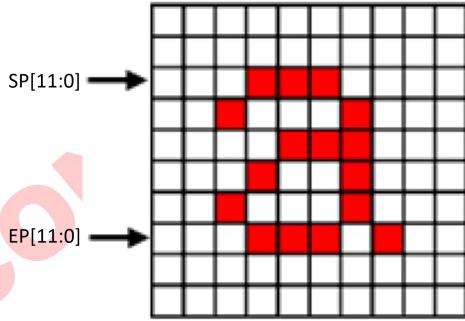
Description	<p>This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands.</p> <p>This command makes No Change on the other driver status.</p> <p>The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes.</p> <p>Each value represents one column line in the Frame Memory.</p> <p>MIPI Packet size to transfer should be transferred by the value of CASET.</p> 
Restriction	<ol style="list-style-type: none"> 1. SC[11:0] always must be equal to or less than EC[11:0]. 2. SC[11:0] should be multiple of slice width. 3. EC[11:0] should be multiple of slice width - 1. 4. Window size should be multiple of slice width.

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	SC[11:0]: 000h, EC[11:0]:59Fh
	S/W Reset	SC[11:0]: 000h, EC[11:0]:59Fh
	H/W Reset	SC[11:0]: 000h, EC[11:0]:59Fh
Flow Chart	<pre> graph TD CASET[CASET] --> SC[SC[11:0] EC[11:0]] SC --> PASET[PASET] PASET --> SP[SP[11:0] EP[11:0]] </pre>	<pre> graph TD RAMWR[RAMWR] --> CompData[Compressed Image Data] CompData --> AnyCommand[Any Command] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

9.3.20 (2Bh) PASET: Write Page Address Set

Command Set		PASET									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
PASET	W	0	0	1	0	1	0	1	1	2Bh	
Parameter	1	0	0	FMEM_WT _MASK_M	FMEM_WT _MASK_S	SP[11:8]				00h	
Parameter	2	SP[7:0]						00h			
Parameter	3	0	0	0	0	EP[11:8]				0Bh	
Parameter	4	EP[7:0]						8Fh			

NOTE: “-”Don’t care.

Description	<p>This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command.</p> <p>This command makes No Change on the other driver status.</p> <p>The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.</p> <p>Each value represents one column line in the Frame Memory.</p>  <p>FMEM_WT_MASK_M: Write control for master IC's frame memory in CASCADE mode</p> <ul style="list-style-type: none"> - 0h : No masking - 1h : Write masking <p>FMEM_WT_MASK_S: Write control for slave IC's frame memory in CASCADE mode</p> <ul style="list-style-type: none"> - 0h : No masking - 1h : Write masking
	<p>1. SP[11:0] always must be equal to or less than EP[11:0].</p> <p>2. SP[11:0] should be multiple of slice height.</p> <p>3. EP[11:0] should be multiple of slice height - 1.</p> <p>4. Window size should be multiple of slice height.</p>

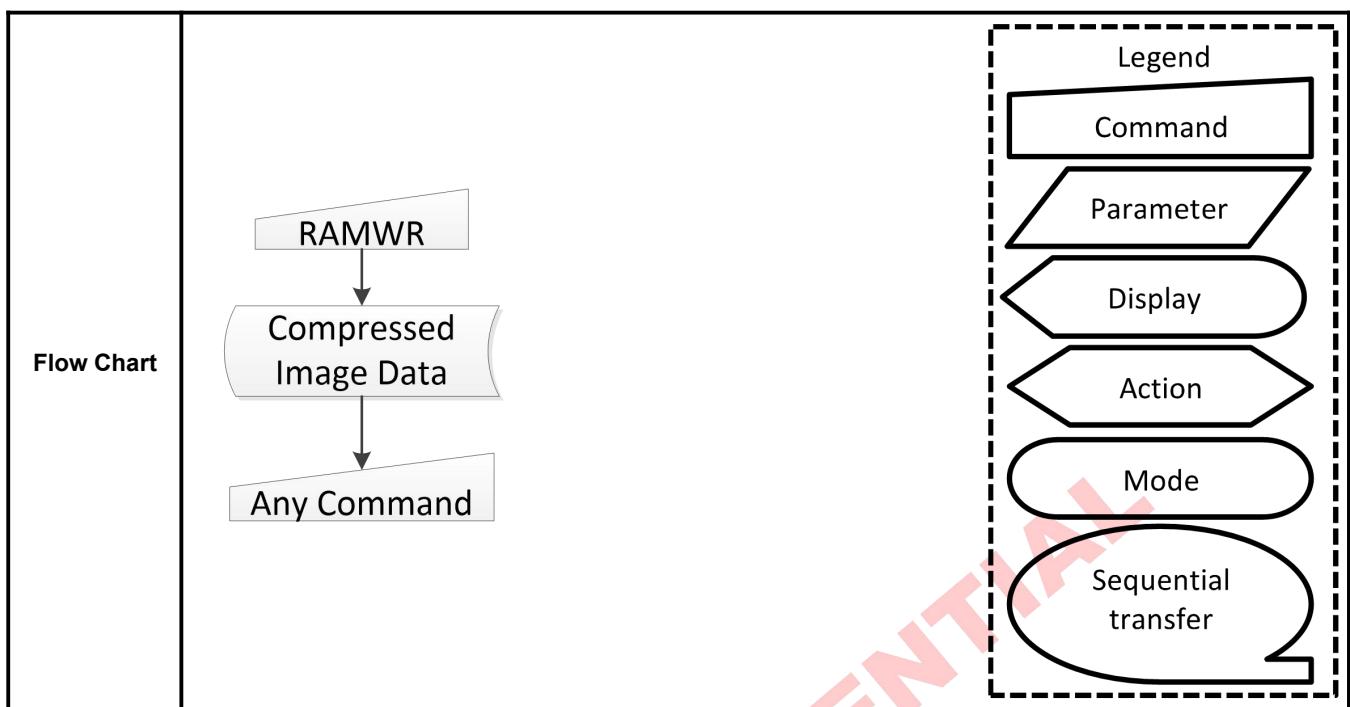
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	SP[11:0]: 000h, EP[11:0]:B8Fh
	S/W Reset	SP[11:0]: 000h, EP[11:0]:B8Fh
	H/W Reset	SP[11:0]: 000h, EP[11:0]:B8Fh
Flow Chart	<pre> graph TD CASET[CASET] --> SC[SC[11:0] EC[11:0]] SC --> PASET[PASET] PASET --> SP[SP[11:0] EP[11:0]] </pre>	<pre> graph TD RAMWR[RAMWR] --> CID[Compressed Image Data] CID --> AC[Any Command] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

9.3.21 (2Ch) RAMWR: Memory Write

Command Set		RAMWR									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RAMWR	W	0	0	1	0	1	1	0	0	2Ch	
Parameter	1	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	variable	
Parameter	
Parameter	N	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	variable	

NOTE: “-“Don’t care.

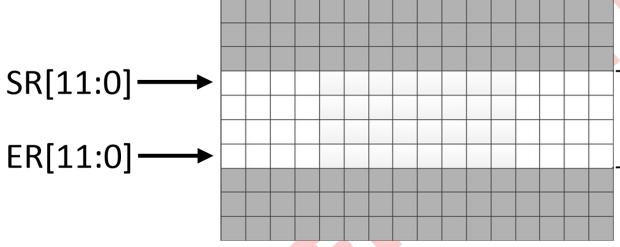
Description	This command is used to transfer data from host processor to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.													
Restriction	There are some restrictions on the command. No access to the frame memory in Sleep In mode. The total number of parameters sent by 2Ch and 3Ch is determined by memory window area. User will send parameters according to memory window area set by 2Ah, 2Bh.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is set randomly</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is set randomly	H/W Reset	Contents of memory is set randomly				
Status	Default Value													
Power On Sequence	Contents of memory is set randomly													
S/W Reset	Contents of memory is set randomly													
H/W Reset	Contents of memory is set randomly													

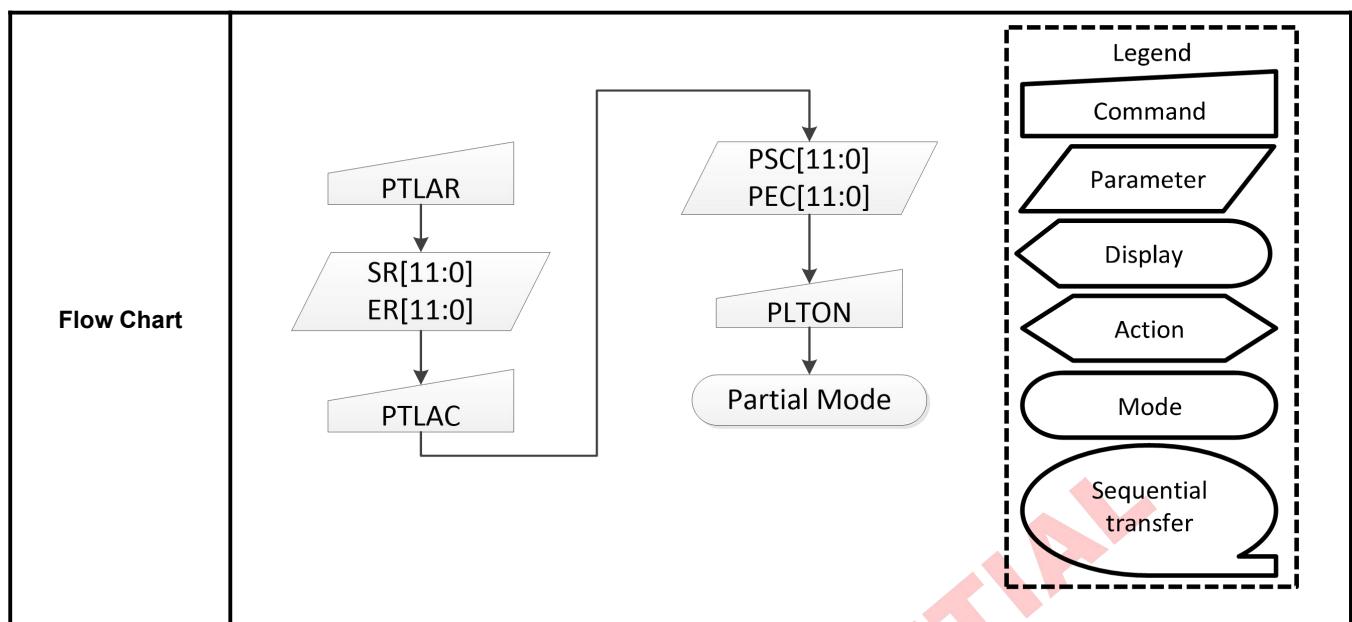


9.3.22 (30h) PTLAR: Write Partial Area Raw Set

Command Set		PTLAR									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
PTLAR	W	0	0	1	1	0	0	0	0	30h	
Parameter	1	0	0	0	0	SR[11:8]				00h	
Parameter	2	SR[7:0]						00h			
Parameter	3	0	0	0	0	ER[11:8]				0Bh	
Parameter	4	ER[7:0]						8Fh			

NOTE: “-”Don’t care.

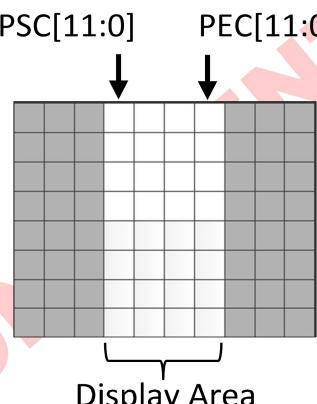
Description	This command defines the partial mode’s display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second defines the End Row(ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. 												
Restriction	SR[11:0] and ER[11:0] cannot exceed the last vertical line number.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SR[11:0]: 000h, ER[11:0]:B8Fh</td> </tr> <tr> <td>S/W Reset</td> <td>SR[11:0]: 000h, ER[11:0]:B8Fh</td> </tr> <tr> <td>H/W Reset</td> <td>SR[11:0]: 000h, ER[11:0]:B8Fh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	SR[11:0]: 000h, ER[11:0]:B8Fh	S/W Reset	SR[11:0]: 000h, ER[11:0]:B8Fh	H/W Reset	SR[11:0]: 000h, ER[11:0]:B8Fh				
Status	Default Value												
Power On Sequence	SR[11:0]: 000h, ER[11:0]:B8Fh												
S/W Reset	SR[11:0]: 000h, ER[11:0]:B8Fh												
H/W Reset	SR[11:0]: 000h, ER[11:0]:B8Fh												



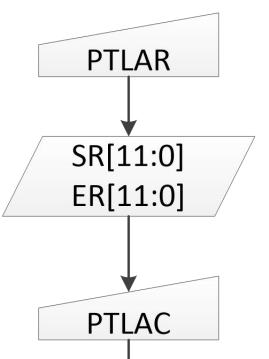
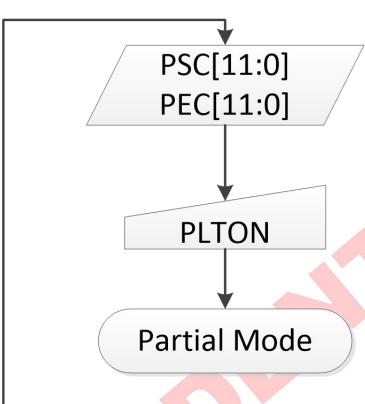
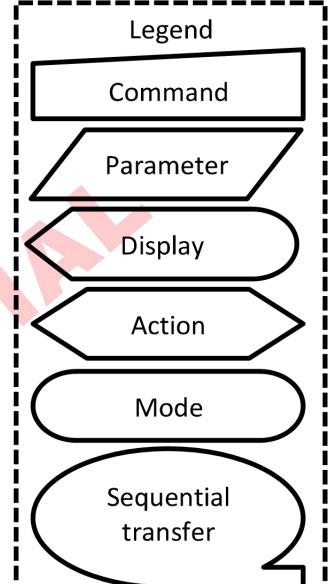
9.3.23 (31h) PTLAC: Write Partial Area Column Set

Command Set		PTLAC									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
PTLAC	W	0	0	1	1	0	0	0	1	31h	
Parameter	1	0	0	0	0	PSC[11:8]				00h	
Parameter	2	PSC[7:0]						PEC[11:8]			00h
Parameter	3	0	0	0	0	PEC[11:8]				05h	
Parameter	4	PEC[7:0]						Display Area			9Fh

NOTE: “-”Don’t care.

Description	<p>This command defines the partial mode’s display area. There are two parameters associated with this command, the first defines the Start Column (PSC) and the second defines the End Column (PEC), as illustrated in the figures below. PSC and PEC refer to the Source Column Pointer.</p> 												
Restriction	PSC[15:0] and PEC[15:0] cannot exceed the last column number.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

Default	Status	Default Value
	Power On Sequence	PSC[11:0]: 000h, PEC[11:0]:59Fh
	S/W Reset	PSC[11:0]: 000h, PEC[11:0]:59Fh
	H/W Reset	PSC[11:0]: 000h, PEC[11:0]:59Fh

Flow Chart		
		

9.3.24 (32h) RTE : Request TE

Command Set		RTE								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RTE	C	0	0	1	1	0	0	1	0	32h
Parameter	-	No Parameter								

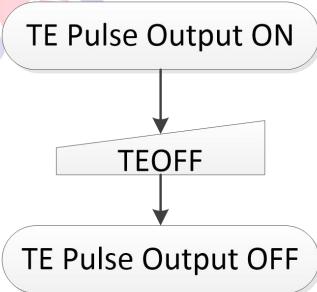
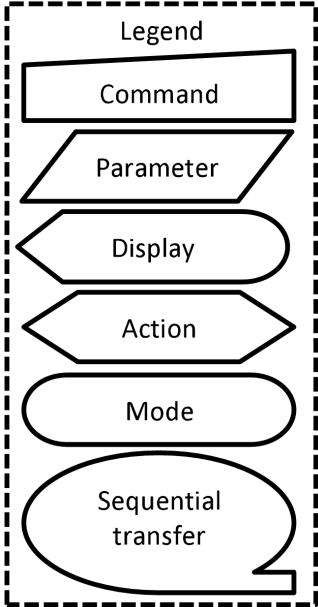
NOTE: “-”Don’t care.

Description	This command is a new command for MSYNC to notice DDIC from AP. This command does not change any other status.													
Restriction	This command has no effect when module is already in display on mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value													
Power On Sequence	Display Off													
S/W Reset	Display Off													
H/W Reset	Display Off													
Flow Chart	<pre> graph TD RTE[RTE] --> RequestTE([Request TE]) subgraph Legend [Legend] Command[Command] Parameter[Parameter] Display[Display] Action[Action] Mode[Mode] SequentialTransfer[Sequential transfer] end </pre>													

9.3.25 (34h) TEOFF: Tearing Effect Line Off

Command Set		TEOFF								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
TEOFF	C	0	0	1	1	0	1	0	0	34h
Parameter	-	No Parameter								

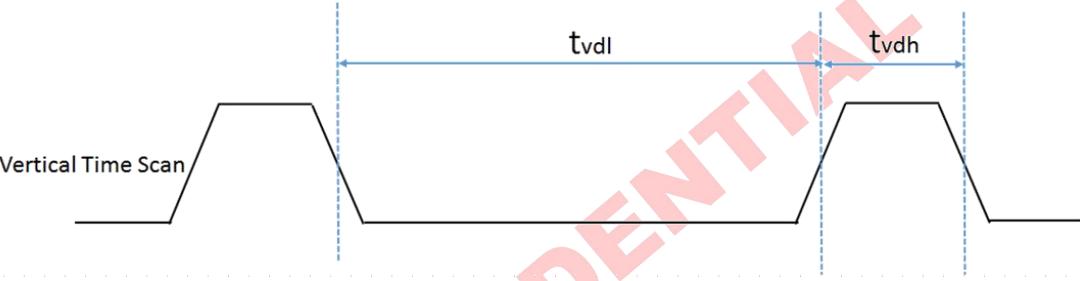
NOTE: “-”Don’t care.

Description	This command is used to turn OFF the Tearing Effect output signal from the TE signal line.													
Restriction	This command has no effect when Tearing Effect output is already OFF.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>S/W Reset</td> <td>OFF</td> </tr> <tr> <td>H/W Reset</td> <td>OFF</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	OFF	S/W Reset	OFF	H/W Reset	OFF				
Status	Default Value													
Power On Sequence	OFF													
S/W Reset	OFF													
H/W Reset	OFF													
Flow Chart	 <pre> graph TD A([TE Pulse Output ON]) --> B[/TEOFF/] B --> C([TE Pulse Output OFF]) </pre>	 <pre> graph LR Legend[Legend] --- Command[Command] Legend --- Parameter[Parameter] Legend --- Display[Display] Legend --- Action[Action] Legend --- Mode[Mode] Legend --- Sequential[Sequential transfer] </pre>												

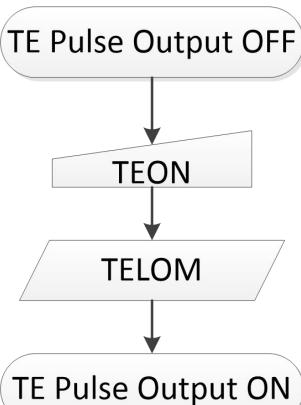
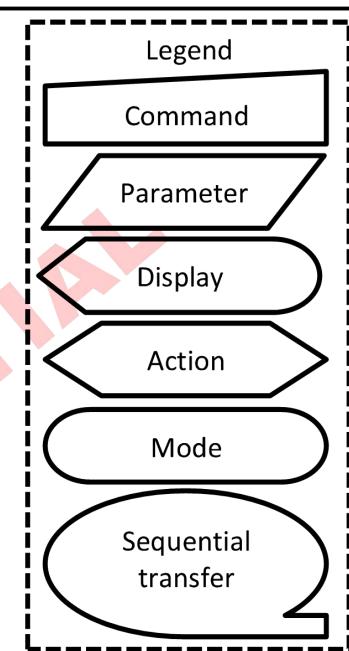
9.3.26 (35h) TEON: Write Tearing Effect Line On

Command Set		TEON								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
TEON	W	0	0	1	1	0	1	0	1	35h
Parameter	1	0	0	0	0	0	0	0	TELOM	00h

NOTE: “-”Don’t care.

Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.</p> <p>When TELOM = “0”: The Tearing Effect Output line consists of V-Blanking information only.</p> 												
	<p>When TELOM = “1”: The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.</p> 												
	<p>*Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p>												
Restriction	This command has no effect when Tearing Effect output is already ON.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

	Status	Default Value
Default	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

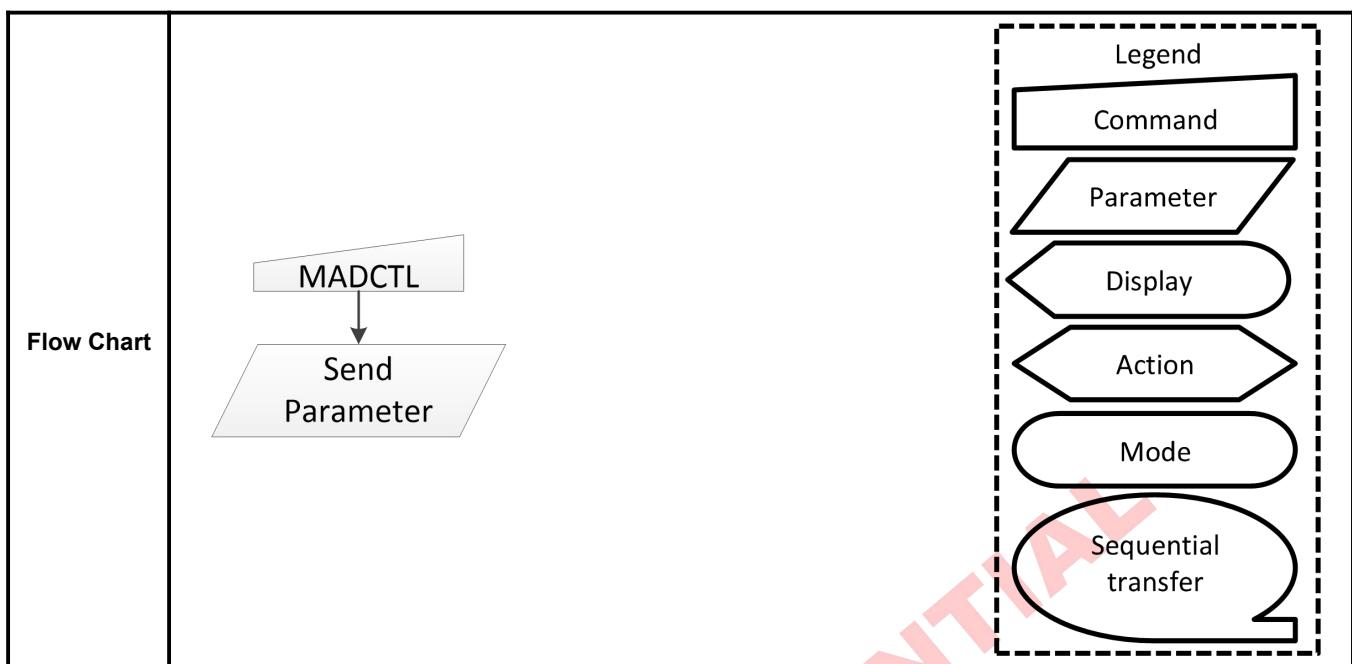
Flow Chart		

9.3.27 (36h) MADCTL: Memory Data Access Control

Command Set		MADCTL									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
MADCTL	W	0	0	1	1	0	1	1	0	36h	
Parameter	1	0	0	0	0	0	0	FH	0	00h	

NOTE: “-”Don’t care.

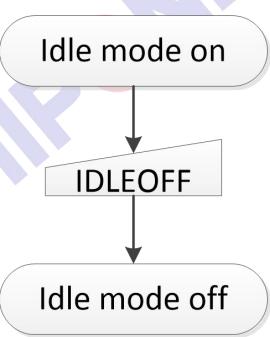
Description	This command defines scanning direction of display image. This command makes no change on the other driver status. MADCTL field is described in the table below:	
	Bit	Description
	D7	Not Used
	D6	Not Used
	D5	Not Used
	D4	Not Used
	D3	Not Used
	D2	Not Used
	D1	FH
	D0	Not Used
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h



9.3.28 (38h) IDLEOFF: Idle Mode Off

Command Set		IDLEOFF									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
IDLEOFF	C	0	0	1	1	1	0	0	0	38h	
Parameter	-	No Parameter									

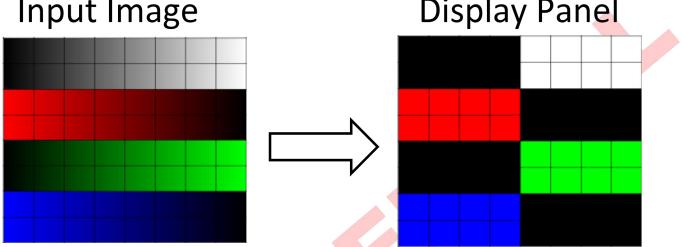
NOTE: “-”Don’t care.

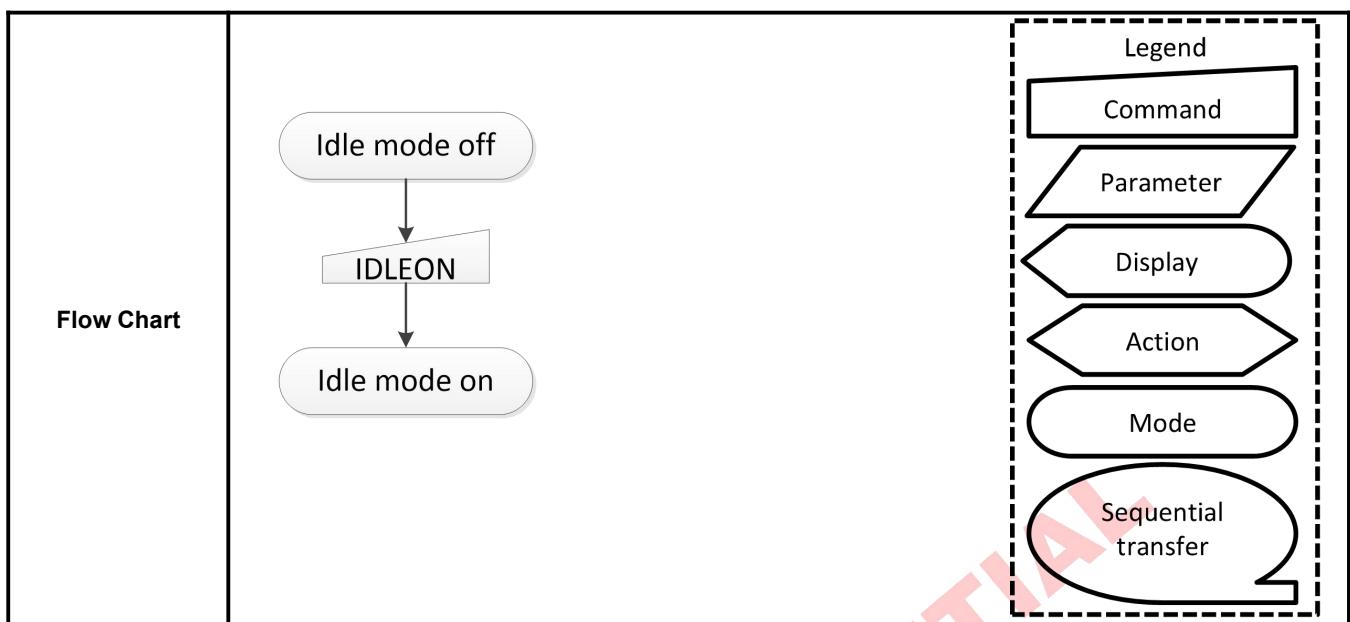
Description	This command is used to recover from Idle mode on.													
Restriction	This command has no effect when module is already in Idle Off mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle mode Off</td> </tr> <tr> <td>S/W Reset</td> <td>Idle mode Off</td> </tr> <tr> <td>H/W Reset</td> <td>Idle mode Off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Idle mode Off	S/W Reset	Idle mode Off	H/W Reset	Idle mode Off				
Status	Default Value													
Power On Sequence	Idle mode Off													
S/W Reset	Idle mode Off													
H/W Reset	Idle mode Off													
Flow Chart	 <pre> graph TD A([Idle mode on]) --> B[/IDLEOFF/] B --> C([Idle mode off]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.29 (39h) IDLEON: Idle Mode On

Command Set		IDLEON									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
IDLEON	C	0	0	1	1	1	0	0	1	39h	
Parameter	-	No Parameter									

NOTE: “-”Don’t care.

Description	<p>This command causes the display module to enter Idle Mode. In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the Input Image.</p> 												
Restriction	This command has no effect when module is already in idle on mode.												
Register Availability	<table border="1" data-bbox="446 1102 1367 1388"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" data-bbox="446 1439 1367 1641"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle mode Off</td> </tr> <tr> <td>S/W Reset</td> <td>Idle mode Off</td> </tr> <tr> <td>H/W Reset</td> <td>Idle mode Off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Idle mode Off	S/W Reset	Idle mode Off	H/W Reset	Idle mode Off				
Status	Default Value												
Power On Sequence	Idle mode Off												
S/W Reset	Idle mode Off												
H/W Reset	Idle mode Off												

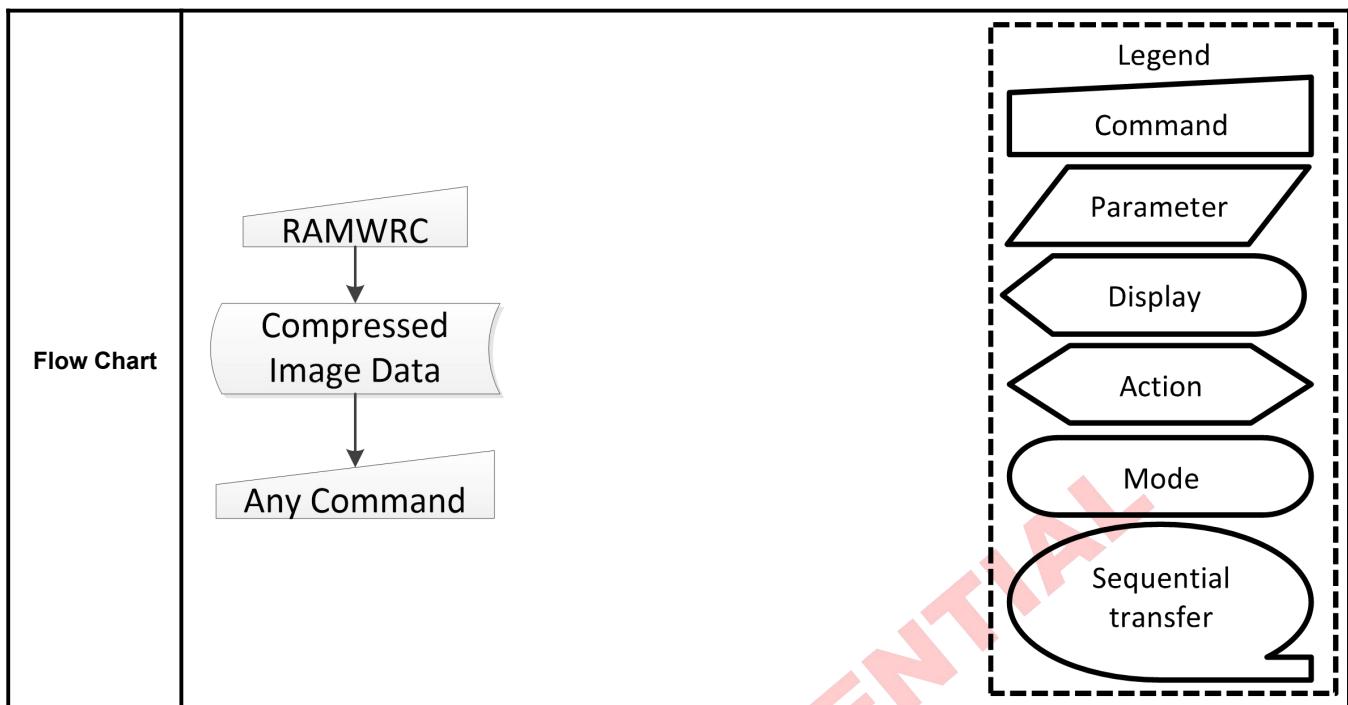


9.3.30 (3Ch) RAMWRC: Memory Write Continue

Command Set		RAMWRC									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RAMWRC	W	0	0	1	1	1	1	0	0	3Ch	
Parameter	1	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	variable	

NOTE: “-”Don’t care.

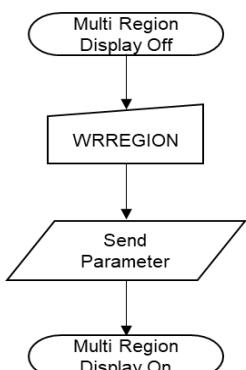
Description	This command is used to transfer data from host processor to frame memory. If there is wanted to continue memory write after "Memory Write (2Ch)" command. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are not reset to the Start Column/Start Page positions as it has been done on "Memory Write (2Ch)" command.													
Restriction	There are some restrictions on the command. No access to the frame memory in Sleep In mode. The total number of parameters sent by 2Ch and 3Ch is determined by memory window area. User will send parameters according to memory window area set by 2Ah, 2Bh.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is set randomly</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is set randomly	H/W Reset	Contents of memory is set randomly				
Status	Default Value													
Power On Sequence	Contents of memory is set randomly													
S/W Reset	Contents of memory is set randomly													
H/W Reset	Contents of memory is set randomly													



9.3.31 (40h) WRREGION: Write MULTI REGION Value

Command Set		WRREGION								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRREGION	W	0	1	0	0	0	0	0	0	40h
Parameter	1	0	0	0	0	0	0	MULTI_PRS[1:0]	03h	

NOTE: “-”Don’t care.

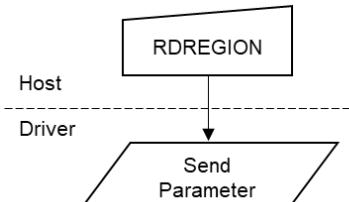
Description	This command causes the DDIC to enter MULTI REGION Mode.	
	MULTI_PRS[1:0]:	Description
	2'b00	Setting Disabled
	2'b01	Only A display On
	2'b10	Only B display On
	2'b11	A+B display On
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
Power On Sequence	Contents of memory is set randomly	
S/W Reset	Contents of memory is set randomly	
H/W Reset	Contents of memory is set randomly	
Flow Chart	 <pre> graph TD A([Multi Region Display Off]) --> B[WRREGION] B --> C{Send Parameter} C --> D([Multi Region Display On]) </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

9.3.32 (41h) RDREGION: Read MULTI REGION Value

Command Set	RDREGION
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Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDREGION	R	0	1	0	0	0	0	0	1	41h
Parameter	1	0	0	0	0	0	0	MULTI_PRS[1:0]	03h	

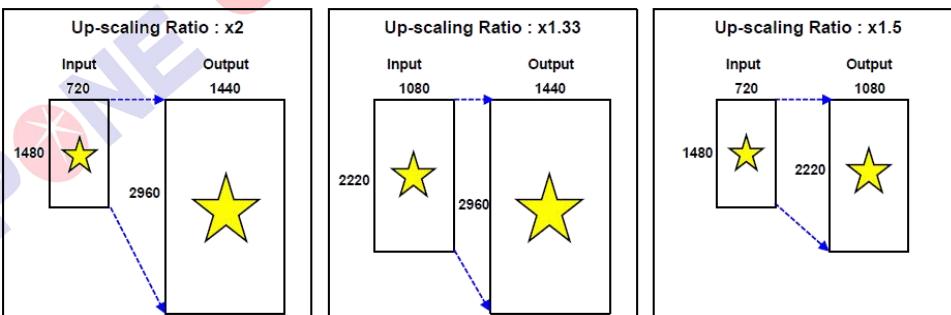
NOTE: “-”Don’t care.

Description	<table border="1"> <tr> <td>MULTI_PRS[1:0]:</td><td>Description</td></tr> <tr> <td>2'b00</td><td>Setting Disabled</td></tr> <tr> <td>2'b01</td><td>Only A display On</td></tr> <tr> <td>2'b10</td><td>Only B display On</td></tr> <tr> <td>2'b11</td><td>A+B display On</td></tr> </table>		MULTI_PRS[1:0]:	Description	2'b00	Setting Disabled	2'b01	Only A display On	2'b10	Only B display On	2'b11	A+B display On	This command causes the DDIC to enter MULTI REGION Mode.
MULTI_PRS[1:0]:	Description												
2'b00	Setting Disabled												
2'b01	Only A display On												
2'b10	Only B display On												
2'b11	A+B display On												
Restriction													
Register Availability <table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default <table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is set randomly</td> </tr> </table>		Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is set randomly	H/W Reset	Contents of memory is set randomly				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Contents of memory is set randomly												
H/W Reset	Contents of memory is set randomly												
Flow Chart  <pre> graph TD RDREGION[RDREGION] --> Host SP[/Send Parameter/] SP --> Driver RDREGION </pre>		<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

9.3.33 (42h) WRUPSCM: Write Scale-up Value

Command Set		WRUPSCM								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRUPSCM	W	0	1	0	0	0	0	1	0	42h
Parameter	1	0	0	0	SCALER_EN	0	0	SCALER_MODE[1:0]		00h

NOTE: “-”Don’t care.

Description	<p>This command causes the DDIC to enter Up-Scaling Mode. This function converts image from a lower resolution to a higher resolution.</p> <p>It can support three kinds of up-scaling ratio : x2, x1.5, x1.33</p> <p>SCALER_EN:</p> <ul style="list-style-type: none"> - “0” = Turn off Up-Scaling Mode. - “1” = Turn on Up-Scaling Mode. <p>SCALER_MODE[1:0]:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">SCALER_MODE[1:0]:</th><th style="text-align: left;">Description</th></tr> </thead> <tbody> <tr> <td>2'b00</td><td>up-scaling ratio x1.33</td></tr> <tr> <td>2'b01</td><td>up-scaling ratio x2</td></tr> <tr> <td>2'b10</td><td>up-scaling ratio x1.5</td></tr> <tr> <td>2'b11</td><td>Reserved</td></tr> </tbody> </table> <p>Some examples of up-scaling application resolution:</p> 		SCALER_MODE[1:0]:	Description	2'b00	up-scaling ratio x1.33	2'b01	up-scaling ratio x2	2'b10	up-scaling ratio x1.5	2'b11	Reserved
SCALER_MODE[1:0]:	Description											
2'b00	up-scaling ratio x1.33											
2'b01	up-scaling ratio x2											
2'b10	up-scaling ratio x1.5											
2'b11	Reserved											
Restriction	Scaling-Up function is only available in command mode.											

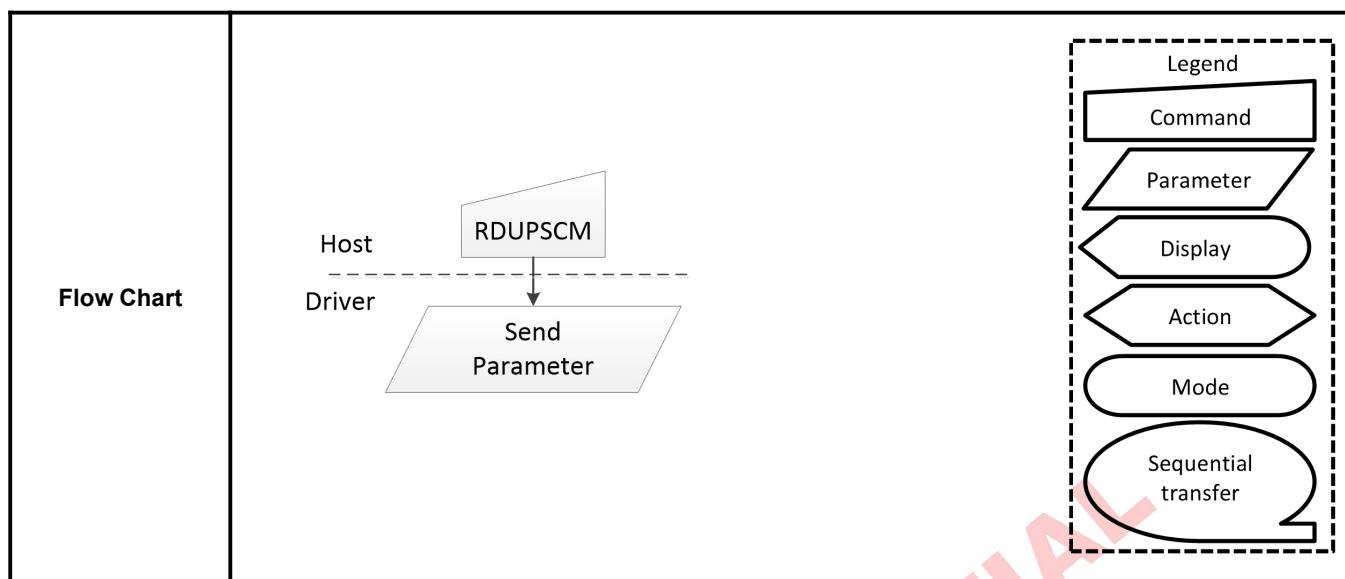
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	<pre> graph TD WRUPSCM[WRUPSCM] --> SCALER[SCALER_EN = 1 & SCALER_MODE[1:0]] SCALER --> ScalingUpMode{Scaling-Up Mode} ScalingUpMode --> RAMWR[RAMWR & RAMWRC] </pre>	<pre> graph TD CompImage[Compressed Image Data] --> DispImage[Display Scaling-Up Image] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

9.3.34 (43h) RDUPSCM: Read Scale-up Value

Command Set		RDUPSCM								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDUPSCM	R	0	1	0	0	0	0	1	1	43h
Parameter	1	0	0	0	SCALER_EN	0	0	SCALER_MODE[1:0]		00h

NOTE: “-”Don’t care.

Description	This command indicates the Up-Scaling Mode status of the display as described as below:													
	SCALER_EN: - “0” = Turn off Up-Scaling Mode. - “1” = Turn on Up-Scaling Mode.													
SCALER_MODE[1:0]:														
<table border="1"> <thead> <tr> <th>SCALER_MODE[1:0]:</th><th>Description</th></tr> </thead> <tbody> <tr> <td>2'b00</td><td>up-scaling ratio x2</td></tr> <tr> <td>2'b01</td><td>up-scaling ratio x1.5</td></tr> <tr> <td>2'b10</td><td>up-scaling ratio x1.33</td></tr> <tr> <td>2'b11</td><td>Reserved</td></tr> </tbody> </table>		SCALER_MODE[1:0]:	Description	2'b00	up-scaling ratio x2	2'b01	up-scaling ratio x1.5	2'b10	up-scaling ratio x1.33	2'b11	Reserved			
SCALER_MODE[1:0]:	Description													
2'b00	up-scaling ratio x2													
2'b01	up-scaling ratio x1.5													
2'b10	up-scaling ratio x1.33													
2'b11	Reserved													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
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	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													
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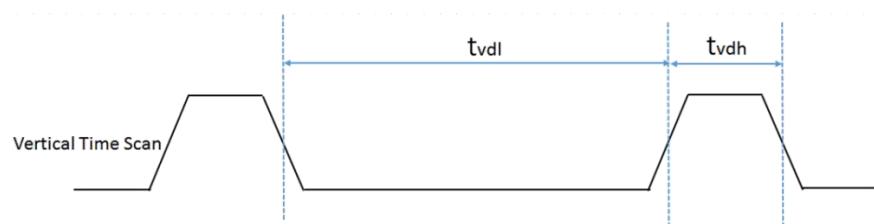
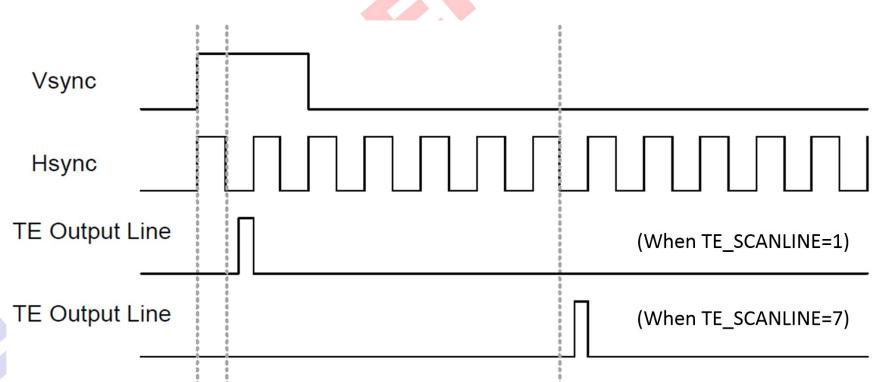


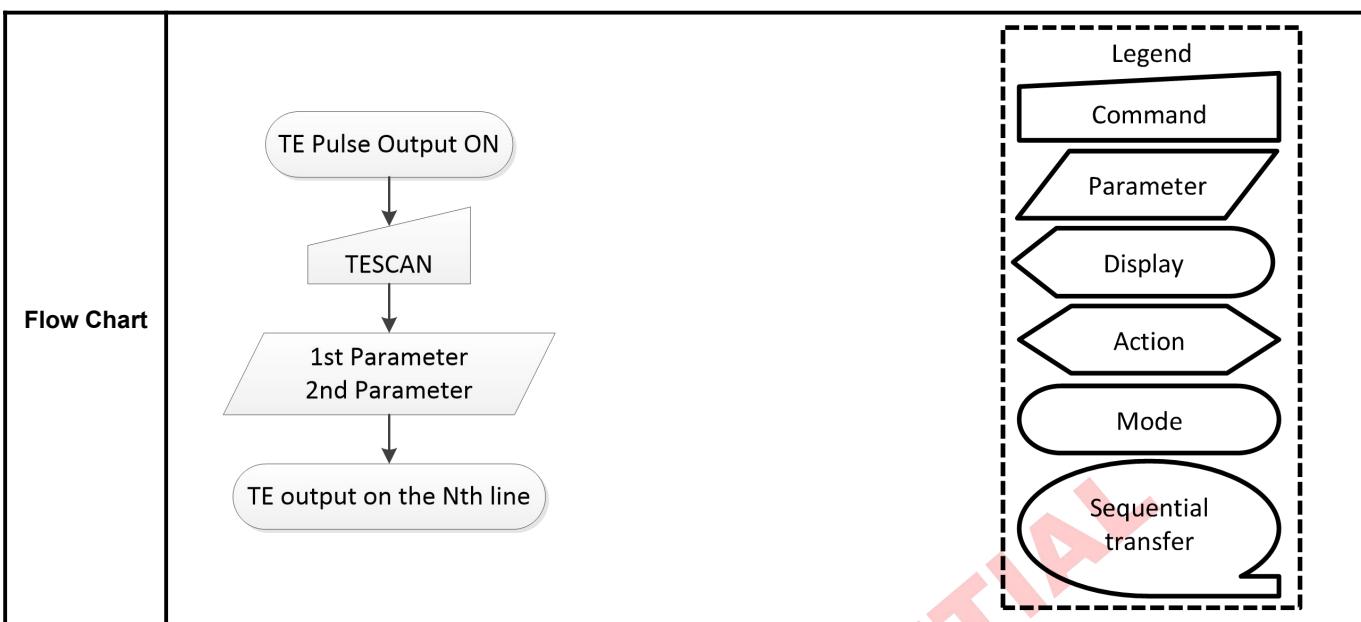
9.3.35 (44h) TESCAN: Write Tear Scanline

Command Set		TESCAN									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
TESCAN	W	0	1	0	0	0	1	0	0	44h	
Parameter	1	TE_SCANLINE[15:8]									
Parameter	2	TE_SCANLINE[7:0]									

NOTE: “-”Don’t care.

Description	<p>This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line TE_SCANLINE.</p> <p>When TE_SCANLINE =1, Tearing Effect output line is on at the first line of VSYNC.</p> <p>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p> <p>Note that TESCAN with TE_SCANLINE = 0 is equivalent to TEON with TELOM = 0.</p> <p>This command takes effect on the frame following the current frame. Therefore, if the Tear Effect (TE) output is already ON, the TE output shall continue to operate as programmed by the previous TEON, or TESCAN, command until the end of the frame.</p>													
Restriction	TE_SCANLINE[15:0] always must be less than VBP + VFP + VSYNC + VACT.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value													
Power On Sequence	000h													
S/W Reset	000h													
H/W Reset	000h													

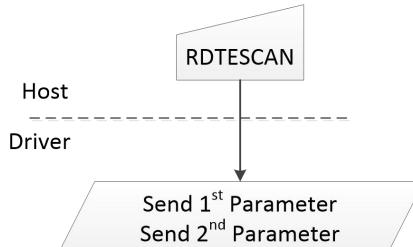
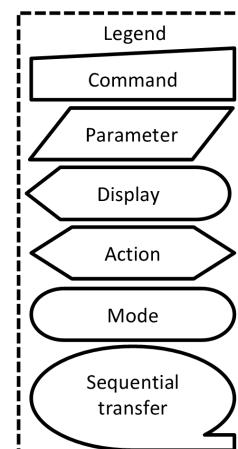
	TEON	TESCAN	TE Pulse Output
Description	TELOM	TE_SCANLINE	The Tearing Effect Output line consists of V-blanking information only.
	0	0	 <p>Vertical Time Scan</p>
	0	$\neq 0$	<p>The Tearing Effect Output Line consists of Nth line information</p> 
	1	X	<p>The Tearing Effect Output Line consists of both V-Blanking and H- Blanking information.</p> 



9.3.36 (45h) RDTESCAN: Read Scanline

Command Set		RDTESCAN									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDTESCAN	R	0	1	0	0	0	1	0	1	45h	
Parameter	1	0	0	0	0	0	0	SCANLINE[17:16]		00h	
Parameter	2	SCANLINE[15:8]						00h			
Parameter	3	SCANLINE[7:0]						00h			

NOTE: “-”“Don’t care.

Description	This command returns the current scan line, N, used to update the display module. The total number of scan lines on display is defined as VBP + VFP + VSYNC + VACT. The first scan line is defined as the first line of V Sync and is denoted as Line 0. When in Sleep in mode, the returned value is undefined.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Status	Default Value													
Power On Sequence	000h													
S/W Reset	000h													
H/W Reset	000h													
Flow Chart	 <pre> graph TD Host -- RDTESCAN --> Driver Driver -- "Send 1st Parameter" --> Param1 Driver -- "Send 2nd Parameter" --> Param2 </pre>	 <pre> graph LR subgraph Legend L1[Command] L2[Parameter] L3[Display] L4[Action] L5[Mode] L6[Sequential transfer] end </pre>												

9.3.37 (48h) WRDSIM: Write DSI MODE

Command Set		WRDSIM								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRDSIM	W	0	1	0	0	1	0	0	0	48h
Parameter	1	0	0	HFR_MODE[1:0]		0	0	DSI_MODE[1:0]		00h

NOTE: “-”Don’t care.

Description	<p>This command is used to select display operation mode. Power, GOA and Source timing can be set in 60Hz and 90Hz mode separately. When display operation mode is changed, please follow display mode change sequence.</p> <table border="1"> <tr> <td>DSI_MODE[1:0]</td><td>Display operation mode</td><td>Mode</td><td>HFR_MODE[1:0]</td><td>Display Refresh Rate</td></tr> <tr> <td>2'b00</td><td>Command Mode</td><td>Through GRAM</td><td>2'b00</td><td>Normal Mode</td></tr> <tr> <td>2'b01</td><td>Reserved</td><td>Reserved</td><td>2'b01</td><td>HF1 Mode</td></tr> <tr> <td>2'b10</td><td rowspan="2">Video Mode</td><td>Through GRAM</td><td>2'b10</td><td>HF2 Mode</td></tr> <tr> <td>2'b11</td><td>Bypass GRAM</td><td>2'b11</td><td>HF3 Mode</td></tr> </table>						DSI_MODE[1:0]	Display operation mode	Mode	HFR_MODE[1:0]	Display Refresh Rate	2'b00	Command Mode	Through GRAM	2'b00	Normal Mode	2'b01	Reserved	Reserved	2'b01	HF1 Mode	2'b10	Video Mode	Through GRAM	2'b10	HF2 Mode	2'b11	Bypass GRAM	2'b11	HF3 Mode		
DSI_MODE[1:0]	Display operation mode	Mode	HFR_MODE[1:0]	Display Refresh Rate																												
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2'b01	Reserved	Reserved	2'b01	HF1 Mode																												
2'b10	Video Mode	Through GRAM	2'b10	HF2 Mode																												
2'b11		Bypass GRAM	2'b11	HF3 Mode																												
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<table border="1"> <tr> <td>WRDSIM</td> <td>HFR_MODE[1:0] & DSI_MODE[1:0]</td> <td>New Control Value</td> <td>Legend</td> </tr> <tr> <td>↓</td> <td>↓</td> <td>↓</td> <td>Command</td> </tr> <tr> <td></td> <td></td> <td></td> <td>Parameter</td> </tr> <tr> <td></td> <td></td> <td></td> <td>Display</td> </tr> <tr> <td></td> <td></td> <td></td> <td>Action</td> </tr> <tr> <td></td> <td></td> <td></td> <td>Mode</td> </tr> <tr> <td></td> <td></td> <td></td> <td>Sequential transfer</td> </tr> </table>					WRDSIM	HFR_MODE[1:0] & DSI_MODE[1:0]	New Control Value	Legend	↓	↓	↓	Command				Parameter				Display				Action				Mode				Sequential transfer
WRDSIM	HFR_MODE[1:0] & DSI_MODE[1:0]	New Control Value	Legend																													
↓	↓	↓	Command																													
			Parameter																													
			Display																													
			Action																													
			Mode																													
			Sequential transfer																													

9.3.38 (49h) RDDSIM: Read DS1 MODE

Command Set		RDDSIM								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDDSIM	R	0	1	0	0	1	0	0	1	49h
Parameter	1	0	0	HFR_MODE[1:0]		0	0	DSI_MODE[1:0]		00h

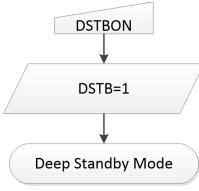
NOTE: “-”Don’t care.

Description	This command returns the status of display operation mode.																									
	<table border="1"> <thead> <tr> <th>DSI_MODE[1:0]</th> <th>Display operation mode</th> <th>Mode</th> <th>HFR_MODE[1:0]</th> <th>Display Refresh Rate</th> </tr> </thead> <tbody> <tr> <td>2'b00</td> <td>Command Mode</td> <td>Through GRAM</td> <td>2'b00</td> <td>Normal Mode</td> </tr> <tr> <td>2'b01</td> <td>Reserved</td> <td>Reserved</td> <td>2'b01</td> <td>HF1 Mode</td> </tr> <tr> <td>2'b10</td> <td rowspan="2">Video Mode</td> <td>Through GRAM</td> <td>2'b10</td> <td>HF2 Mode</td> </tr> <tr> <td>2'b11</td> <td>Bypass GRAM</td> <td>2'b11</td> <td>HF3 Mode</td> </tr> </tbody> </table>		DSI_MODE[1:0]	Display operation mode	Mode	HFR_MODE[1:0]	Display Refresh Rate	2'b00	Command Mode	Through GRAM	2'b00	Normal Mode	2'b01	Reserved	Reserved	2'b01	HF1 Mode	2'b10	Video Mode	Through GRAM	2'b10	HF2 Mode	2'b11	Bypass GRAM	2'b11	HF3 Mode
DSI_MODE[1:0]	Display operation mode	Mode	HFR_MODE[1:0]	Display Refresh Rate																						
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2'b10	Video Mode	Through GRAM	2'b10	HF2 Mode																						
2'b11		Bypass GRAM	2'b11	HF3 Mode																						
Restriction	-																									
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Flow Chart	 <pre> graph TD Host[Host] -- RDDSIM --> Driver[Driver] Driver -- "Send Parameter" --> Param[/] style Param fill:none,stroke:none subgraph Legend [Legend] direction TB C[Command] --- P[Parameter] D[Display] --- A[Action] M[Mode] --- ST[Sequential transfer] end </pre>																									

9.3.39 (4Fh) DSTBON: Write Deep Standby On

Command Set		DSTBON									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
DSTBON	W	0	1	0	0	1	1	1	1	4Fh	
Parameter	1	0	0	0	0	0	0	0	DSTB	00h	

NOTE: “-”Don’t care.

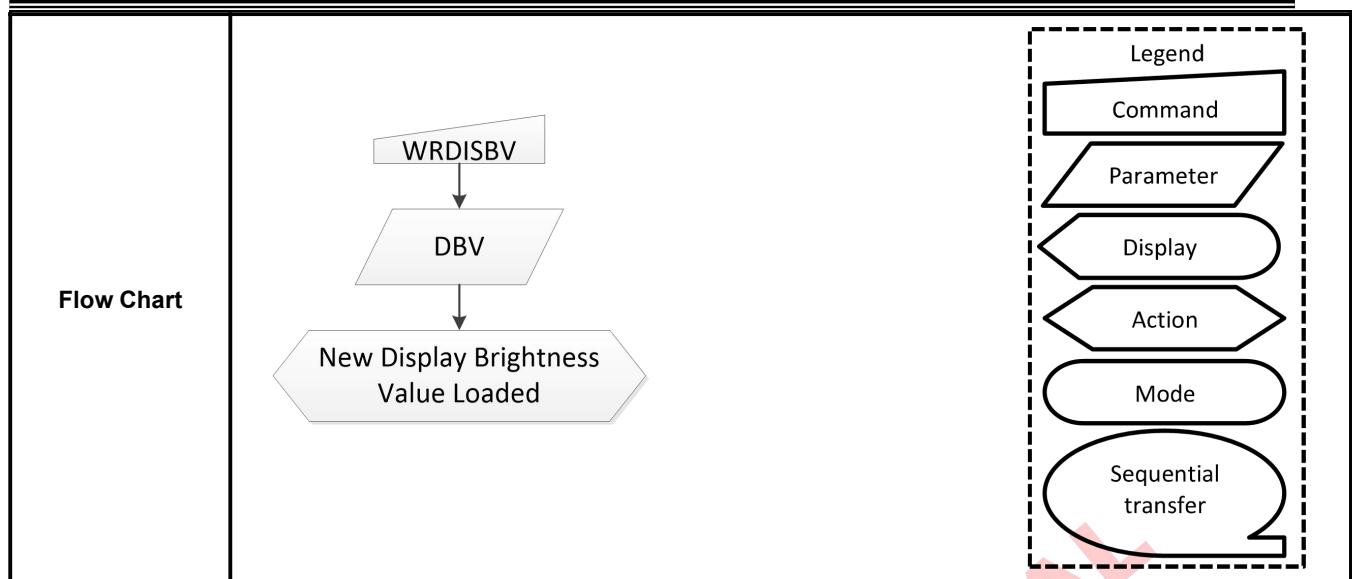
Description	This command is used to enter deep standby mode. DSTB=“1”, enter deep standby mode. *Notes: 1. To exit Deep Standby Mode, set RESX low pulse more than 3m second to pin nRESET. 2. If user wants to enter DSTB mode from Normal Display directly, it should enter sleep-in & display-off mode first, and wait 2 frames or more time for completing power-down sequence, and then execute this command to enter DSTB mode.													
Restriction	This command is only valid sleep mode.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	No	Normal Mode On, Idle Mode On, Sleep Out	No	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
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Status	Default Value													
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H/W Reset	00h													
Flow Chart	 <pre> graph TD DSTBON[DSTBON] --> DSTB1{DSTB=1} DSTB1 --> DSTBON[Deep Standby Mode] </pre> <p>Legend: Command (rectangle) Parameter (trapezoid) Display (diamond) Action (triangle) Mode (oval) Sequential transfer (rounded rectangle) </p>													

9.3.40 (51h) WRDISBV: Write Display Brightness

Command Set		WRDISBV									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
WRDISBV	W	0	1	0	1	0	0	0	1	51h	
Parameter	1	DBV1[7:0]									
Parameter	2	0	0	0	0	0	0	DBV1[12:8]			00h
Parameter	3	DBV2[7:0]									
Parameter	4	0	0	0	0	0	0	DBV2[12:8]			00h
Parameter	5	ELVSS_OFF _EN	ELVSS_OFF _SIGN	ELVSS_OFF_DBV[5:0]							

NOTE: “-”Don’t care.

Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 0000h value means the lowest brightness and 1FFFh value means the highest brightness. DBV1[12:0] : Brightness control for A area DBV2[12:0] : Brightness control for B area ELVSS_OFF_EN: Control On/Off for ELVSS offset value ELVSS_OFF_SIGN: Control sign bit for ELVSS offset value ELVSS_OFF_DBV[5:0]: Control for ELVSS offset value												
Restriction	-												
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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S/W Reset	000h												
H/W Reset	000h												

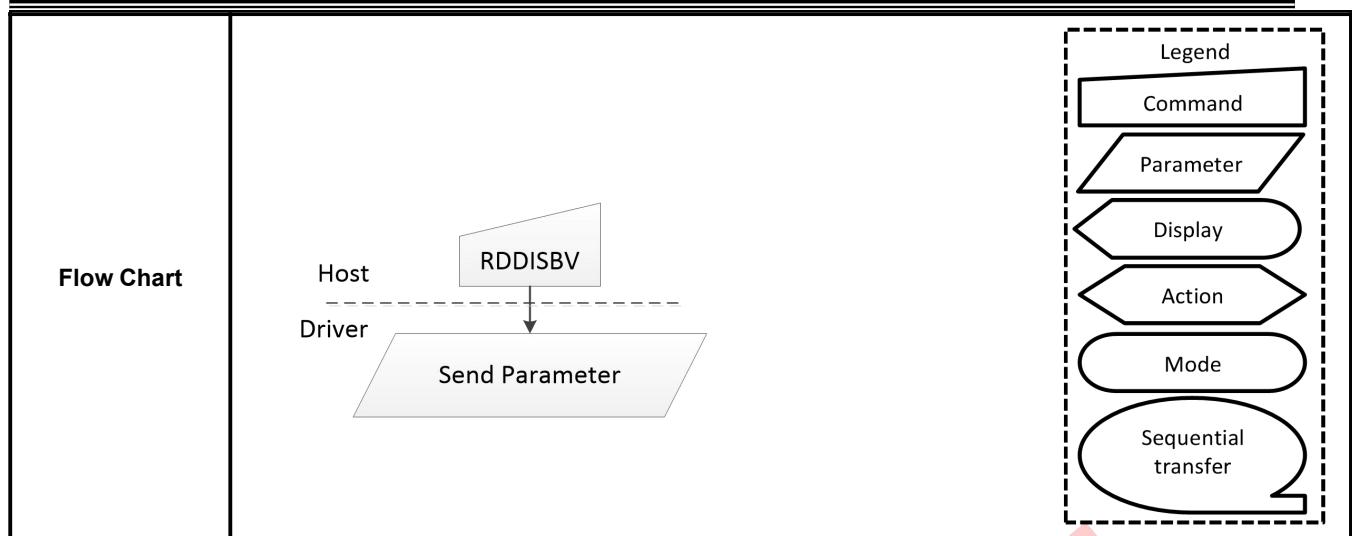


9.3.41 (52h) RDDISBV: Read Display Brightness Value

Command Set		RDDISBV								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDDISBV	R	0	1	0	1	0	0	1	0	52h
Parameter	1	DBV1[7:0]								
Parameter	2	0	0	0	0	0	0	DBV1[12:8]		00h
Parameter	3	DBV2[7:0]								
Parameter	4	0	0	0	0	0	0	DBV2[12:8]		00h
Parameter	5	ELVSS_OFF _EN	ELVSS_OFF _SIGN	ELVSS_OFF_DBV[5:0]						00h

NOTE: “-”Don’t care.

Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 0000h value means the lowest brightness and 1FFFh value means the highest brightness. DBV1[12:0] : Brightness control for A area DBV2[12:0] : Brightness control for B area ELVSS_OFF_EN: Control On/Off for ELVSS offset value ELVSS_OFF_SIGN: Control sign bit for ELVSS offset value ELVSS_OFF_DBV[5:0]: Control for ELVSS offset value												
Restriction	-												
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>000h</td> </tr> <tr> <td>S/W Reset</td> <td>000h</td> </tr> <tr> <td>H/W Reset</td> <td>000h</td> </tr> </table>	Status	Default Value	Power On Sequence	000h	S/W Reset	000h	H/W Reset	000h				
Status	Default Value												
Power On Sequence	000h												
S/W Reset	000h												
H/W Reset	000h												



9.3.42 (53h) WRCTRL: Write Control Display

Command Set		WRCTRL								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRCTRL	W	0	1	0	1	0	0	1	1	53h
Parameter	1	HBM_MODE[1:0]	BCTL	0	BC_DIM_EN	BC_DC_EN	0	HBM_EN	00h	

NOTE: “-”Don’t care.

Description	This command is used to control OLED brightness.						
	HBM_MODE[1:0]: Select the high brightness threshold						
	HBM_MODE[1:0]	HBM Area Luminance control (in HBM mode)					
	2'h0	Max gamma threshold is normal area					
	2'h1	Max gamma threshold is HBM3 area					
	2'h2	Max gamma threshold is HBM2 area					
	2'h3	Max gamma threshold is HBM1 area					
	BCTL: Brightness On/Off control						
	<table border="1"> <tr> <th>BCTL</th><th>Description</th></tr> <tr> <td>0</td><td>Off</td></tr> <tr> <td>1</td><td>On</td></tr> </table>		BCTL	Description	0	Off	1
BCTL	Description						
0	Off						
1	On						
BC_DIM_EN: Brightness control with dimming effect							
<table border="1"> <tr> <th>BC_DIM_EN</th><th>Description</th></tr> <tr> <td>0</td><td>Display Dimming is off</td></tr> <tr> <td>1</td><td>Display Dimming is on</td></tr> </table>		BC_DIM_EN	Description	0	Display Dimming is off	1	Display Dimming is on
BC_DIM_EN	Description						
0	Display Dimming is off						
1	Display Dimming is on						
HBM_EN: High Brightness Mode control							
<table border="1"> <tr> <th>HBM_EN</th><th>Description</th></tr> <tr> <td>0</td><td>HBM Off</td></tr> <tr> <td>1</td><td>HBM On</td></tr> </table>		HBM_EN	Description	0	HBM Off	1	HBM On
HBM_EN	Description						
0	HBM Off						
1	HBM On						
BC_DC_EN : Control On/Off for DC mode (When HW_ENs is 1)							
<table border="1"> <tr> <th>BC_DC_EN</th><th>Description</th></tr> <tr> <td>0</td><td>DC Off</td></tr> <tr> <td>1</td><td>DC On</td></tr> </table>		BC_DC_EN	Description	0	DC Off	1	DC On
BC_DC_EN	Description						
0	DC Off						
1	DC On						
Restriction	-						

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	<pre> graph TD WRCTRL[WRCTRL] --> HBM_MODE[HBM_MODE[1:0], BCTL, BC_DIM_EN, HBM_EN] HBM_MODE --> NCV[New Control Value] </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

9.3.43 (54h) RDCTRL: Read Control Value Display

Command Set		RDCTRL								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDCTRL	R	0	1	0	1	0	1	0	0	54h
Parameter	1	HBM_MODE[1:0]	BCTL	0	BC_DIM_EN	BC_DC_EN	0	HBM_EN	00h	

NOTE: “-”Don’t care.

Description	This command is used to read the setting status of OLED brightness control.						
	HBM_MODE[1:0]: Select the high brightness threshold						
	HBM_MODE[1:0]	HBM Area Luminance control (in HBM mode)					
	2'h0	Max gamma threshold is normal area					
	2'h1	Max gamma threshold is HBM3 area					
	2'h2	Max gamma threshold is HBM2 area					
	2'h3	Max gamma threshold is HBM1 area					
	BCTL: Brightness control						
	<table border="1"> <thead> <tr> <th>BCTL</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Off</td></tr> <tr> <td>1</td><td>On</td></tr> </tbody> </table>		BCTL	Description	0	Off	1
BCTL	Description						
0	Off						
1	On						
BC_DIM_EN: Brightness control with dimming effect							
<table border="1"> <thead> <tr> <th>BC_DIM_EN</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Display Dimming is off</td></tr> <tr> <td>1</td><td>Display Dimming is on</td></tr> </tbody> </table>		BC_DIM_EN	Description	0	Display Dimming is off	1	Display Dimming is on
BC_DIM_EN	Description						
0	Display Dimming is off						
1	Display Dimming is on						
HBM_EN: High Brightness Mode control							
<table border="1"> <thead> <tr> <th>HBM_EN</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>HBM Off</td></tr> <tr> <td>1</td><td>HBM On</td></tr> </tbody> </table>		HBM_EN	Description	0	HBM Off	1	HBM On
HBM_EN	Description						
0	HBM Off						
1	HBM On						
BC_DC_EN : Control On/Off for DC mode (When HW_ENs is 1)							
<table border="1"> <thead> <tr> <th>BC_DC_EN</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>DC Off</td></tr> <tr> <td>1</td><td>DC On</td></tr> </tbody> </table>		BC_DC_EN	Description	0	DC Off	1	DC On
BC_DC_EN	Description						
0	DC Off						
1	DC On						
Restriction	-						

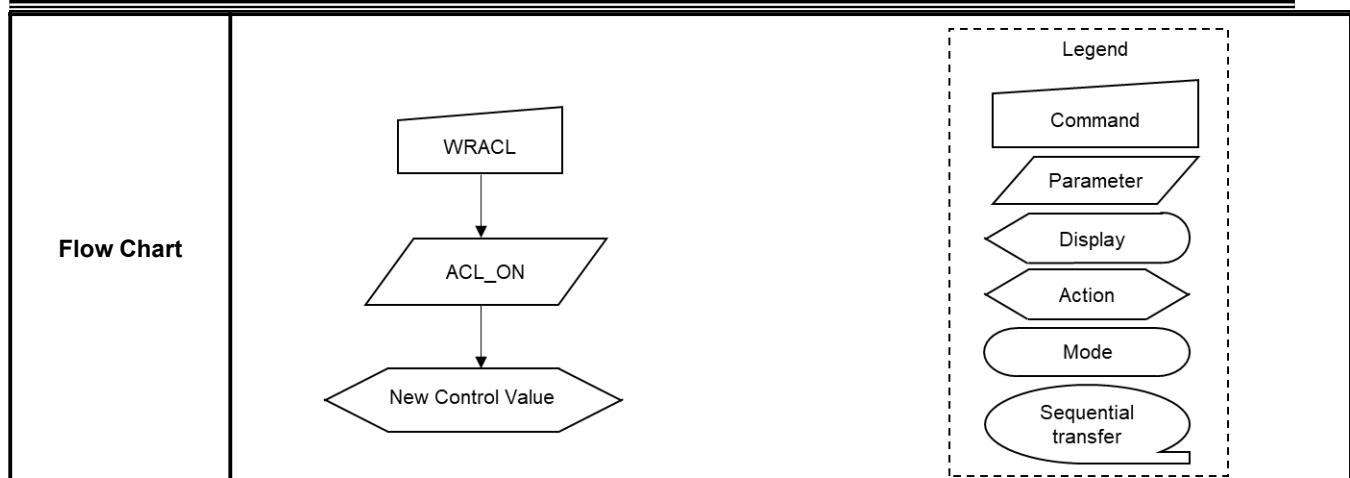
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	<pre> graph TD Host[Host] --> RDCTRL[RDCTRL] RDCTRL --> Driver[Driver] subgraph Legend [Legend] direction TB C[Command] P[Parameter] D[Display] A[Action] M[Mode] ST[Sequential transfer] end </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

9.3.44 (55h) WRACL: Write ACL Value

Command Set		WRACL									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
WRICL	W	0	1	0	1	0	1	0	1	55h	
Parameter	1	ACL_CMD[9:8]		0	0	0	0	ACL[1:0]		00h	
Parameter	2	ACL_CMD[7:0]								00h	

NOTE: “-”Don’t care.

Description	This command is used to adjust Automatic Current Limit (ACL) for power saving.													
	ACL_CMD[9:0]: AL value that receives command from AP.													
	ACL[1:0] : Control for ACL mode													
	<table border="1"> <thead> <tr> <th>ACL[1:0]</th><th>Description</th></tr> </thead> <tbody> <tr> <td>2'h0</td><td>ACL Off</td></tr> <tr> <td>2'h1</td><td>ACL Rate1</td></tr> <tr> <td>2'h2</td><td>ACL Rate2</td></tr> <tr> <td>2'h3</td><td>ACL Rate3</td></tr> </tbody> </table>		ACL[1:0]	Description	2'h0	ACL Off	2'h1	ACL Rate1	2'h2	ACL Rate2	2'h3	ACL Rate3		
ACL[1:0]	Description													
2'h0	ACL Off													
2'h1	ACL Rate1													
2'h2	ACL Rate2													
2'h3	ACL Rate3													
Restriction														
-														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>00h</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													



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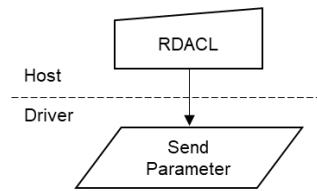
9.3.45 (56h) RDACL: Read ACL Value

Command Set		RDACL								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDICL	R	0	1	0	1	0	1	1	0	56h
Parameter	1	ACL_CMD[9:8]		0	0	0	0	ACL[1:0]		00h
Parameter	2	ACL_CMD[7:0]							00h	

NOTE: “-”Don’t care.

Description	This command is used to read the status of Automatic Current Limit (ACL) for power saving.													
	ACL_CMD[9:0]: AL value that receives command from AP.													
	ACL[1:0] : Control for ACL mode													
	<table border="1"> <thead> <tr> <th>ACL[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>ACL Off</td> </tr> <tr> <td>2'h1</td> <td>ACL Rate1</td> </tr> <tr> <td>2'h2</td> <td>ACL Rate2</td> </tr> <tr> <td>2'h3</td> <td>ACL Rate3</td> </tr> </tbody> </table>		ACL[1:0]	Description	2'h0	ACL Off	2'h1	ACL Rate1	2'h2	ACL Rate2	2'h3	ACL Rate3		
ACL[1:0]	Description													
2'h0	ACL Off													
2'h1	ACL Rate1													
2'h2	ACL Rate2													
2'h3	ACL Rate3													
Restriction														
-														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

low Chart



Legend

Command

Parameter

Display

Action

Mode

Sequential transfer

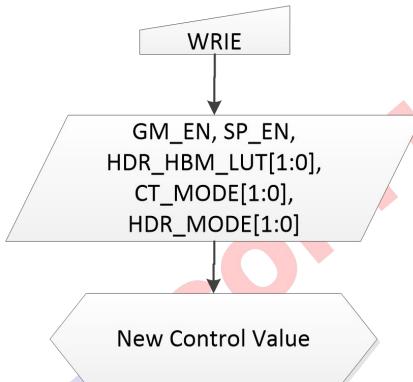
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9.3.46 (57h) WRIE: Write IE Value

Command Set		WRIE									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
WRIE	W	0	1	0	1	0	1	1	1	57h	
Parameter	1	CE_ON	0	0	PAPERMODE_ON	HDR_ON	ENSUN_ON	EDGE_ON	CONST_ON	00h	

NOTE: “-”Don’t care.

Description	This command is used to control Image Enhancement function.	
	CE_ON : CE On/Off Control	
	CE_ON	Description
	0	Off
	1	On
	PAPERMODE_ON : E-PAPER MODE On/Off Control	
	PAPERMODE_ON	Description
	0	Off
	1	On
	HDR_ON: HDR On/Off Control	
	HDR_ON	Description
	0	Off
	1	On
	ENSUN_ON: SLR(Sun Light Readable) On/Off Control	
	ENSUN_ON	Description
	0	Off
	1	On
	EDGE_ON: Sharpness On/Off Control	
	EDGE_ON	Description
	0	Off
	1	On
	CONST_ON: Contrast On/Off Control	
	CONT_ON	Description
	0	Off
	1	On
Restriction	-	

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	 <p>The flowchart illustrates the write operation. It starts with a rectangular input 'WRIE' pointing to a trapezoidal node containing five control bits: GM_EN, SP_EN, HDR_HBM_LUT[1:0], CT_MODE[1:0], and HDR_MODE[1:0]. An arrow from this node points down to a hexagonal output 'New Control Value'.</p>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

9.3.47 (58h) RDIE: Read IE Value

Command Set		RDIE									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDIE	R	0	1	0	1	1	0	0	0	58h	
Parameter	1	CE_ON	0	0	PAPERMODE_ON	HDR_ON	ENSUN_ON	EDGE_ON	CONST_ON	00h	

NOTE: “-”Don’t care.

Description	This command is used to read the status of Image Enhancement Function.	
	CE_ON : CE On/Off Control	
	CE_ON	Description
	0	Off
	1	On
	PAPERMODE_ON : E-PAPER MODE On/Off Control	
	PAPERMODE_ON	Description
	0	Off
	1	On
Restriction	HDR_ON: HDR On/Off Control	
	HDR_ON	Description
	0	Off
	1	On
	ENSUN_ON: SLR(Sun Light Readable) On/Off Control	
	ENSUN_ON	Description
	0	Off
	1	On
Restriction	EDGE_ON: Sharpness On/Off Control	
	EDGE_ON	Description
	0	Off
	1	On
	CONST_ON: Contrast On/Off Control	
	CONT_ON	Description
	0	Off
	1	On

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	<pre> graph TD Host[Host] -- RDIE --> Driver[Driver] Driver -- Send Parameter --> SendParameter[/Send Parameter/] </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

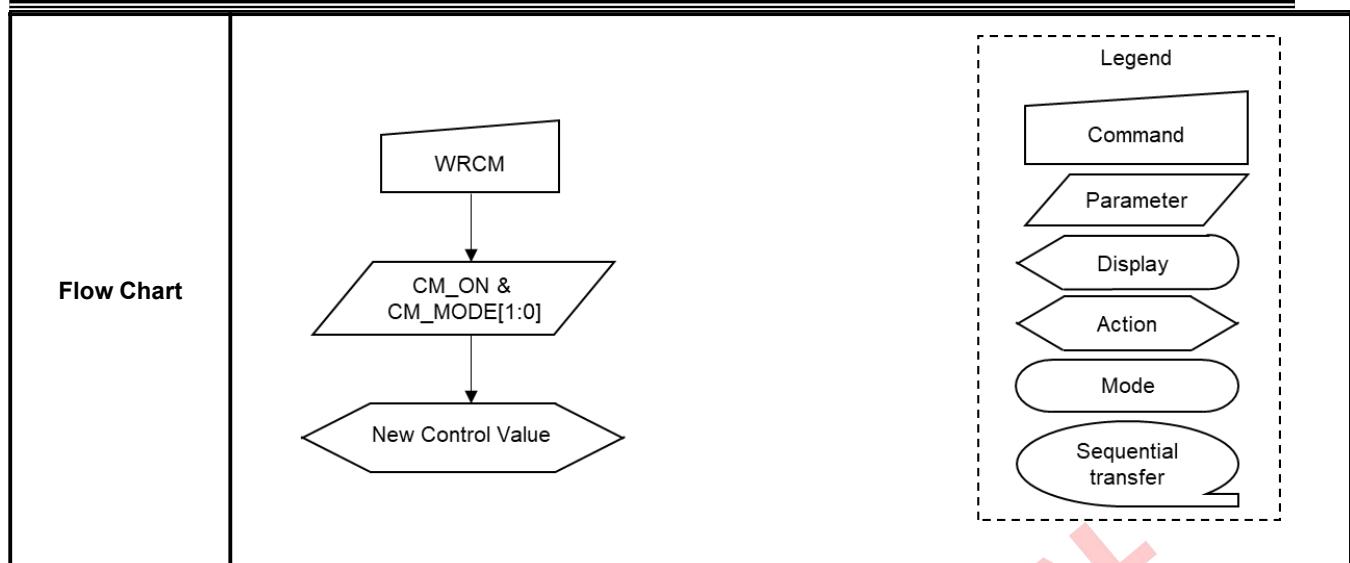
9.3.48 (59h) WRCM: Write CM Value

Command Set		WRCM									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
WRCM	W	0	1	0	1	1	0	0	1	59h	
Parameter	1	0	0	0	CM_ON	0	0	CM_MODE[1:0]	00h		

NOTE: “-”Don’t care.

Description	This command is used to control Color Management function.										
	CM_ON: Color Management On/Off Control										
<table border="1"> <tr> <th>CM_N</th> <th>Description</th> </tr> <tr> <td>0</td> <td>Off</td> </tr> <tr> <td>1</td> <td>On</td> </tr> </table>		CM_N	Description	0	Off	1	On				
CM_N	Description										
0	Off										
1	On										
CM_MODE[1:0]: Color Management Mode Control											
<table border="1"> <tr> <th>CM_MODE[1:0]</th> <th>Description</th> </tr> <tr> <td>2'h0</td> <td>Mode 0</td> </tr> <tr> <td>2'h1</td> <td>Mode 1</td> </tr> <tr> <td>2'h2</td> <td>Mode 2</td> </tr> <tr> <td>2'h3</td> <td>Mode 3</td> </tr> </table>		CM_MODE[1:0]	Description	2'h0	Mode 0	2'h1	Mode 1	2'h2	Mode 2	2'h3	Mode 3
CM_MODE[1:0]	Description										
2'h0	Mode 0										
2'h1	Mode 1										
2'h2	Mode 2										
2'h3	Mode 3										
Restriction	-										

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h



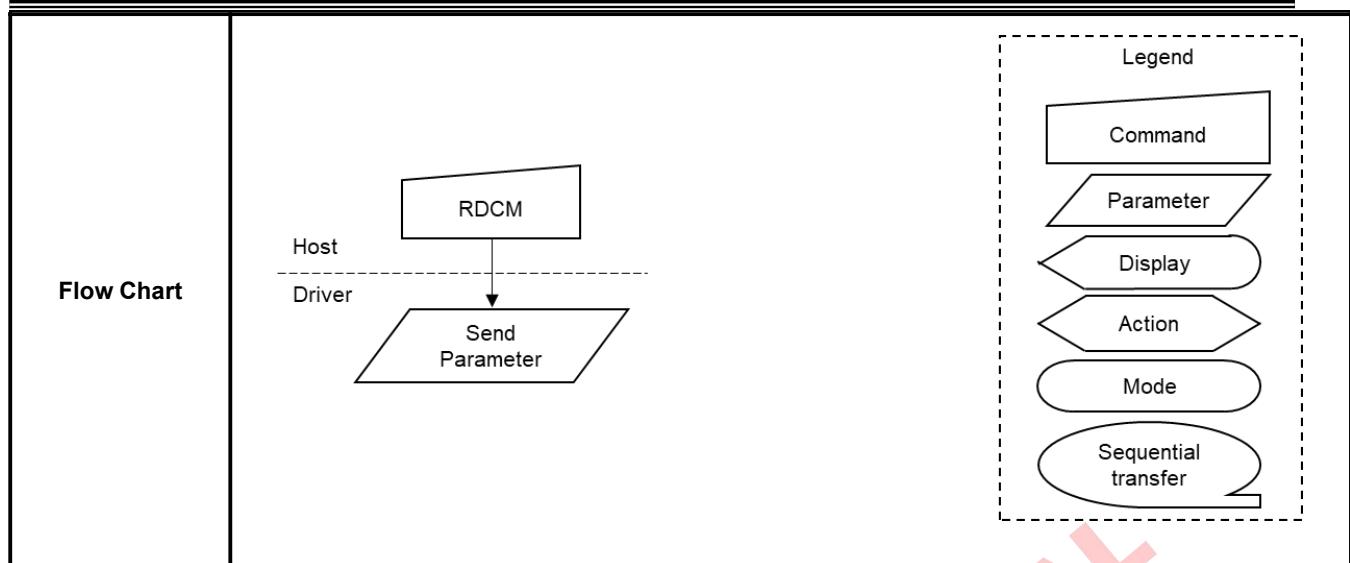
9.3.49 (5Ah) RDCM: Read CM Value

Command Set		RDCM									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDCM	R	0	1	0	1	1	0	1	0	5Ah	
Parameter	1	0	0	0	CM_ON	0	0	CM_MODE[1:0]	00h		

NOTE: “-”Don’t care.

Description	This command is used to control Color Management function.	
	CM_ON: Color Management On/Off Control	
	CM_ON	Description
		0 Off
		1 On
CM_MODE[1:0]: Color Management Mode Control		
		CM_MODE[1:0] Description
		2'h0 Mode 0
		2'h1 Mode 1
		2'h2 Mode 2
		2'h3 Mode 3
Restriction	-	

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
		Sleep In
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

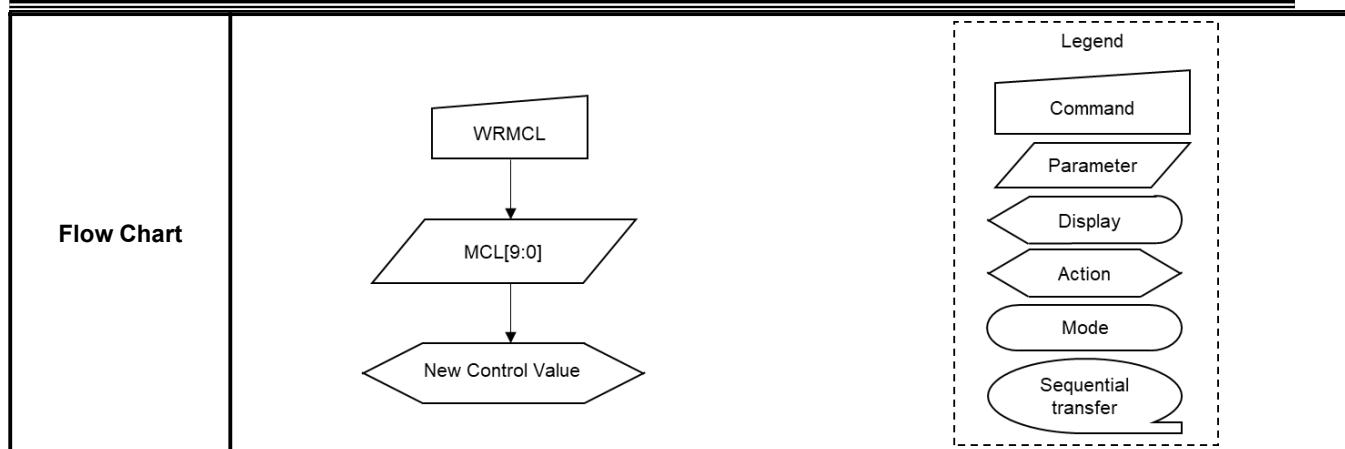


9.3.50 (5Dh) WRMCL: Write MCL Value

Command Set		WRMCL									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
WRMCL	W	0	1	0	1	1	1	0	1	5Dh	
Parameter	1	0	0	0	0	0	0	MCL[9:8]		00h	
Parameter	2	MCL[7:0]								00h	

NOTE: “-”Don’t care.

Description	This command is used to adjust Max Current Limit (MCL) for power saving. MCL[9:0]: Control for MCL Command from HOST												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												



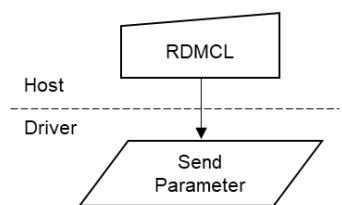
9.3.51 (5Eh) RDMCL: Read MCL Value

Command Set		RDMCL									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDMCL	R	0	1	0	1	1	1	1	0	5Eh	
Parameter	1	0	0	0	0	0	0	MCL[9:8]		00h	
Parameter	2	MCL[7:0]									

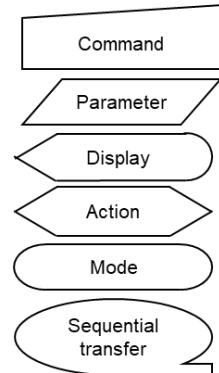
NOTE: “-”Don’t care.

Description	This command is used to adjust Max Current Limit (MCL) for power saving. MCL[9:0]: Control for MCL Command from HOST												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

Flow Chart



Legend

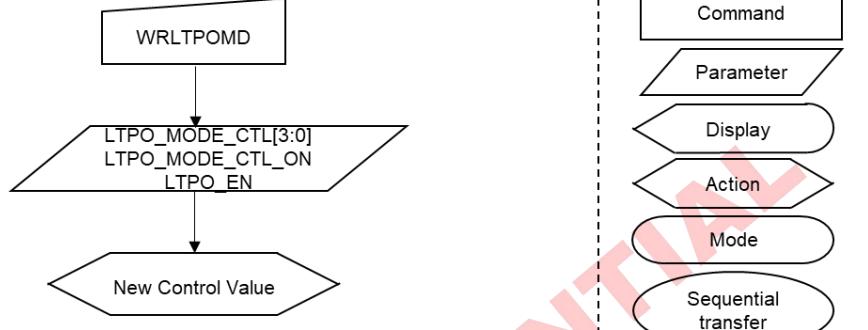


9.3.52 (63h) WRLTPOMD : Write LTPO Value

Command Set		WRLTPOMD								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRMCL	W	0	1	1	0	0	0	1	1	63h
Parameter	1	LTPO_MODE_CTL[3:0]				0	0	LTPO_MODE_CTL_O N	LTPO_EN	00h

NOTE: “-”Don’t care.

Description	This command is used to control LTPO function.	
	LTPO_MODE_CTL[3:0]: LTPO Mode Control	
	LTPO_MODE_CTL[3:0]	Description
	4'h0	Mode 1
Description	4'h1	Mode 2
	4'h2	Mode 3
	4'h3	Mode 4
	4'hE	Mode 15
Description	4'hF	Mode 16
	LTPO_MODE_CTL_ON: LTPO Mode Control On/Off Control	
	LTPO_MODE_CTL_ON	Description
	0	Off
Description	1	On
	LTPO_EN: LTPO On/Off Control	
	LTPO_EN	Description
	0	Off
Restriction	-	
	Register Availability	
	Status	
	Normal Mode On, Idle Mode Off, Sleep Out	
	Yes	
Register Availability	Normal Mode On, Idle Mode On, Sleep Out	
	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	
	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	
Register Availability	Sleep In	
	Yes	

Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></tbody></table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value								
Power On Sequence	00h								
S/W Reset	00h								
H/W Reset	00h								
Flow Chart	 <p>The flowchart illustrates the process of setting control values. It begins with a rectangular box labeled "WRLTPOMD". An arrow points down to a trapezoidal box containing three items: "LTPO_MODE_CTL[3:0]", "LTPO_MODE_CTL_ON", and "LTPO_EN". Another arrow points down to a diamond-shaped box labeled "New Control Value". To the right of the flowchart is a legend enclosed in a dashed box, defining the symbols used:</p> <table border="1"><thead><tr><th>Legend</th></tr></thead><tbody><tr><td>Command</td></tr><tr><td>Parameter</td></tr><tr><td>Display</td></tr><tr><td>Action</td></tr><tr><td>Mode</td></tr><tr><td>Sequential transfer</td></tr></tbody></table>	Legend	Command	Parameter	Display	Action	Mode	Sequential transfer	
Legend									
Command									
Parameter									
Display									
Action									
Mode									
Sequential transfer									

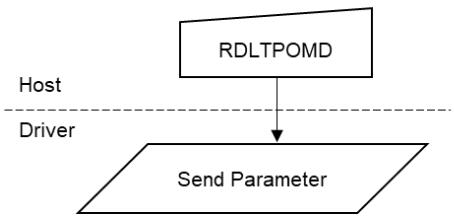
9.3.53 (64h) RDLTPOMD : Read LTPO Value

Command Set		WRLTPOMD								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRMCL	R	0	1	1	0	0	1	0	0	64h
Parameter	1	LTPO_MODE_CTL[3:0]			0	0	LTPO_MODE_CTL_ON		LTPO_EN	00h

NOTE: “-”Don’t care.

Description	This command is used to control LTPO function.	
	LTPO_MODE_CTL[3:0]: LTPO Mode Control	
	LTPO_MODE_CTL[3:0]	Description
	4'h0	Mode 1
Description	4'h1	Mode 2
	4'h2	Mode 3
	4'h3	Mode 4
	4'hE	Mode 15
Description	4'hF	Mode 16
	LTPO_MODE_CTL_ON: LTPO Mode Control On/Off Control	
	LTPO_MODE_CTL_ON	Description
	0	Off
Description	1	On
	LTPO_EN: LTPO On/Off Control	
	LTPO_EN	Description
	0	Off
Restriction	-	
	Register Availability	
	Status	
	Normal Mode On, Idle Mode Off, Sleep Out	
	Yes	
Register Availability	Normal Mode On, Idle Mode On, Sleep Out	
	Partial Mode On, Idle Mode Off, Sleep Out	
	Partial Mode On, Idle Mode On, Sleep Out	
	Sleep In	
	Yes	

Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

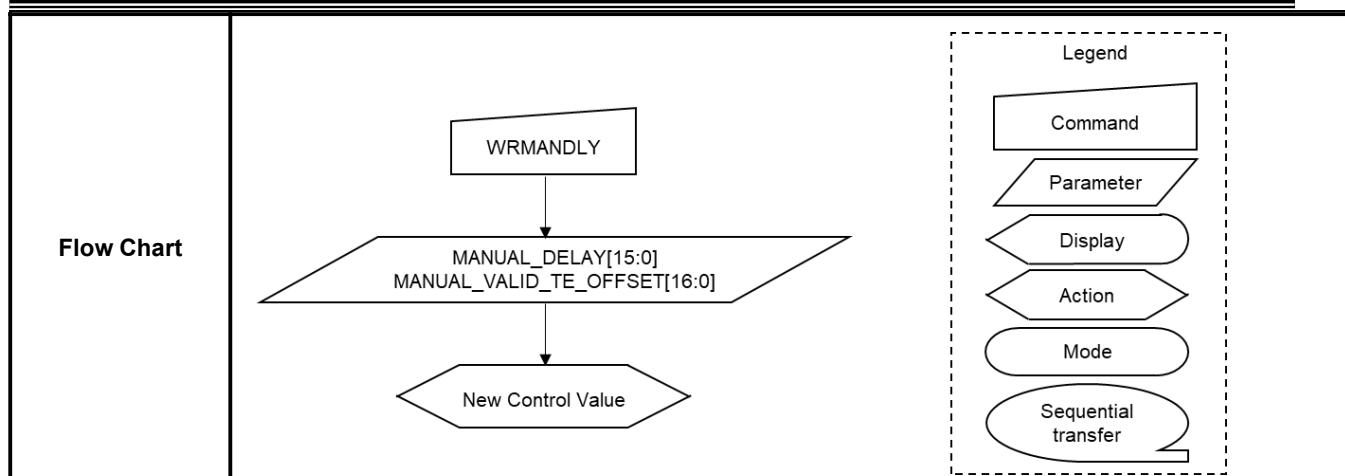
Flow Chart		Legend			
		Command	Parameter	Display	Action

9.3.54 (65h) WRMANDLY : Write Manual Delay Value

Command Set		WRMANDLY								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRMCL	W	0	1	1	0	0	1	0	1	65h
Parameter	1	MANUAL_DELAY[7:0]								
Parameter	2	MANUAL_DELAY[15:8]								
Parameter	3	MANUAL_VALID_TE_OFFSET[7:0]								
Parameter	4	MANUAL_VALID_TE_OFFSET[15:8]								
Parameter	5	0	0	0	0	0	0	0	MANUAL_VALID_TE_OFFSET[16]	00h

NOTE: “-”Don’t care.

Description	This command is used to control MSYNC function. MANUAL_DELAY[15:0] : Manual AFP set by AP when manual delay mode is enabled. MANUAL_VALID_TE_OFFSET[16:0] : Manual Valid TE Offset set by AP when manual delay mode is enabled.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

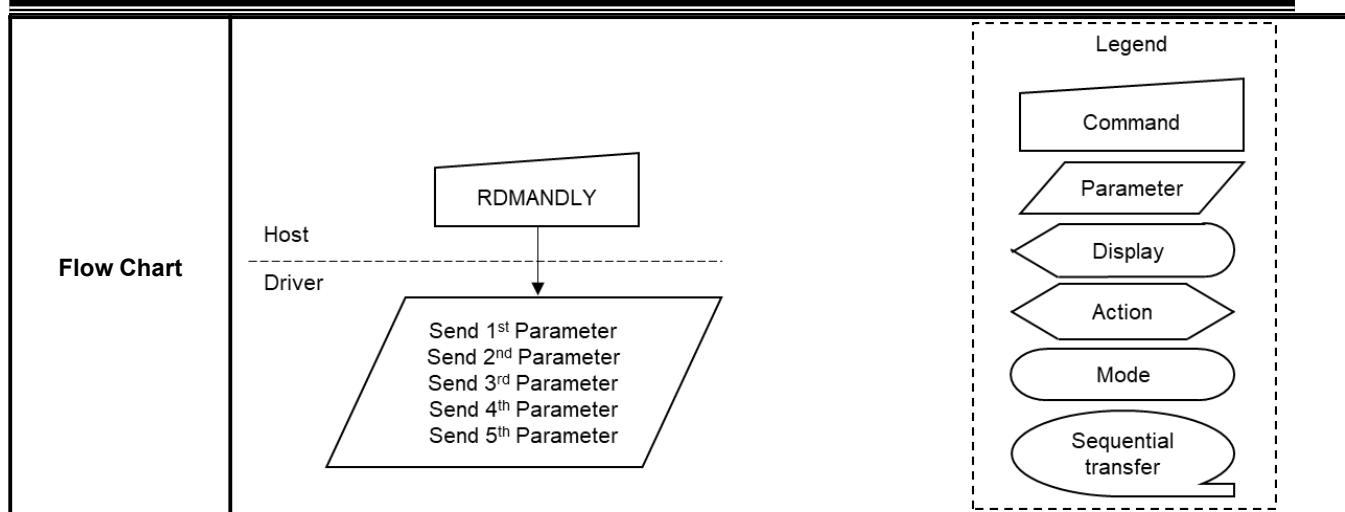


9.3.55 (66h) RDMANDLY : Read Manual Delay Value

Command Set		WRMANDLY								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRMCL	R	0	1	1	0	0	1	1	0	66h
Parameter	1	MANUAL_DELAY[7:0]								
Parameter	2	MANUAL_DELAY[15:8]								
Parameter	3	MANUAL_VALID_TE_OFFSET[7:0]								
Parameter	4	MANUAL_VALID_TE_OFFSET[15:8]								
Parameter	5	0	0	0	0	0	0	0	MANUAL_VALID_TE_OFFSET[16]	00h

NOTE: “-”Don’t care.

Description	This command is used to control MSYNC function. MANUAL_DELAY[15:0] : Manual AFP set by AP when manual delay mode is enabled. MANUAL_VALID_TE_OFFSET[16:0] : Manual Valid TE Offset set by AP when manual delay mode is enabled.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

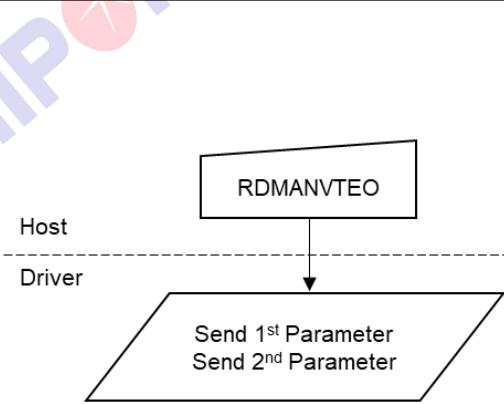


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9.3.56 (68h) RDMANVTEO : Read Manual VTEO Value

Command Set		WRMANDLY									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
WRMCL	R	0	1	1	0	1	0	0	0	68h	
Parameter	1	VALID_TE_OFFSET[7:0]								00h	
Parameter	2	VALID_TE_OFFSET[15:8]								00h	

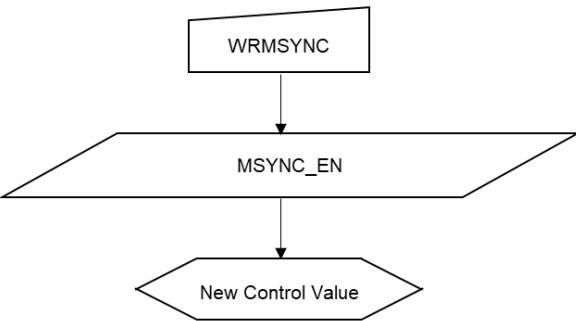
NOTE: “-”Don’t care.

Description	This command is used to control MSYNC function. RDMANVTEO[15:0] : DDIC Internal Valid Offset Counter when manual delay mode is enabled.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host[Host] --> RDMANVTEO[RDMANVTEO] RDMANVTEO --> Send1[Send 1st Parameter] RDMANVTEO --> Send2[Send 2nd Parameter] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.57 (69h) WRMSYNC : Write MSYNC Value

Command Set		WRMANDLY								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRMCL	W	0	1	1	0	1	0	0	1	69h
Parameter	1	0	0	0	0	0	0	0	MSYNC_EN	00h

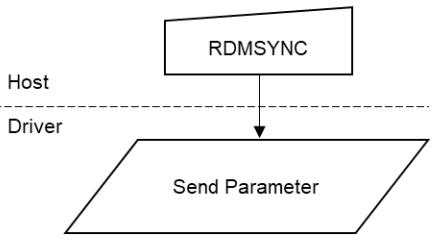
NOTE: “-”Don’t care.

Description	<p>This command is used to control MSYNC function.</p> <p>MSYNC_EN: Msync On/Off Control</p> <table border="1" data-bbox="362 669 941 804"> <thead> <tr> <th>MSYNC_EN</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Off</td></tr> <tr> <td>1</td><td>On</td></tr> </tbody> </table>		MSYNC_EN	Description	0	Off	1	On						
MSYNC_EN	Description													
0	Off													
1	On													
Restriction	-													
Register Availability	<table border="1" data-bbox="446 889 1367 1174"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1" data-bbox="446 1242 1367 1432"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD WRMSYNC[WRMSYNC] --> MSYNC_EN{MSYNC_EN} MSYNC_EN --> NCV{New Control Value} </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.58 (6Ah) RDMSYNC : Read MSYNC Value

Command Set		WRMANDLY								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRMCL	R	0	1	1	0	1	0	1	0	6Ah
Parameter	1	0	0	0	0	0	0	0	MSYNC_EN	00h

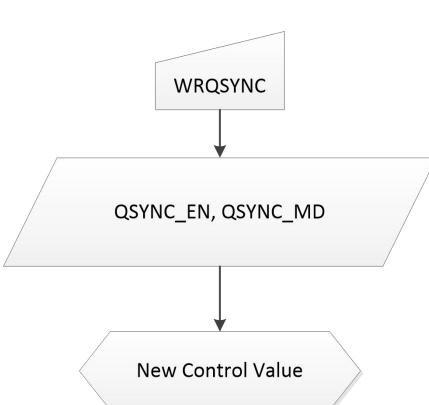
NOTE: “-”Don’t care.

Description	<p>This command is used to control MSYNC function.</p> <p>MSYNC_EN: Msync On/Off Control</p> <table border="1" data-bbox="362 669 941 804"> <thead> <tr> <th>MSYNC_EN</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Off</td></tr> <tr> <td>1</td><td>On</td></tr> </tbody> </table>		MSYNC_EN	Description	0	Off	1	On						
MSYNC_EN	Description													
0	Off													
1	On													
Restriction	-													
Register Availability	<table border="1" data-bbox="446 889 1367 1174"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1" data-bbox="446 1242 1367 1432"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host[Host] -- RDMSYNC --> Driver[Driver] Driver -- "Send Parameter" --> Send[Send Parameter] </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.59 (6Bh) WRQSYNC: Write QSYNC Value

Command Set		WRQSYNC								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRQSYNC	W	0	1	1	0	1	0	1	1	6Bh
Parameter	1	0	0	0	0	0	0	0	QSYNC_EN	00h

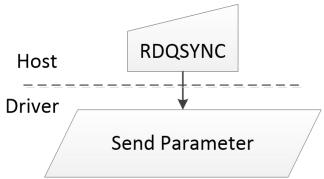
NOTE: “-”Don’t care.

Description	This command is used to control QSYNC function. QSYNC_EN: Qsync or Pixel Sync On/Off Control													
	<table border="1"> <thead> <tr> <th>QSYNC_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Off</td> </tr> <tr> <td>1</td> <td>On</td> </tr> </tbody> </table>		QSYNC_EN	Description	0	Off	1	On						
QSYNC_EN	Description													
0	Off													
1	On													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD WRQSYNC[WRQSYNC] --> QSyncEN[QSYNC_EN, QSYNC_MD] QSyncEN --> NewControlValue[New Control Value] </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.60 (6Ch) RDQSYNC: Read QSYNC Value

Command Set		RDQSYNC								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDQSYNC	R	0	1	1	0	1	1	0	0	6Ch
Parameter	1	0	0	0	0	0	0	0	QSYNC_EN	00h

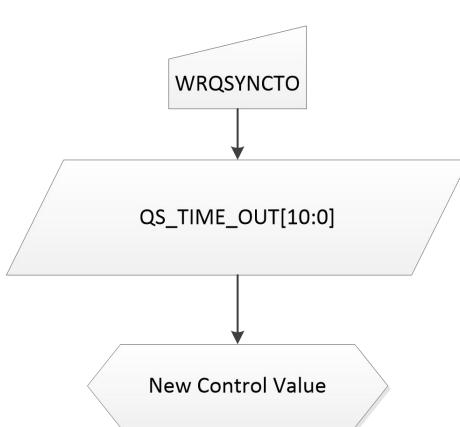
NOTE: “-”Don’t care.

Description	This command is used to read the status of QSYNC function. QSYNC_EN: Qsync or Pixel Sync On/Off Control													
	<table border="1"> <thead> <tr> <th>QSYNC_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Off</td> </tr> <tr> <td>1</td> <td>On</td> </tr> </tbody> </table>		QSYNC_EN	Description	0	Off	1	On						
QSYNC_EN	Description													
0	Off													
1	On													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host -- RDQSYNC --> Driver Driver -- Send Parameter --> None </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.61 (6Dh) WRQSYNCTO: Write QSYNC Timeout Value

Command Set		WRQSYNCTO									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
WRQSYNCTO	W	0	1	1	0	1	1	0	1	6Dh	
Parameter	1	QS_TIME_OUT[15:8]									
Parameter	2	QS_TIME_OUT[7:0]									
Parameter	3	TE_EXT_TIME_OUT[15:8]									
Parameter	4	TE_EXT_TIME_OUT[7:0]									

NOTE: “-”Don’t care.

Description	This command is used to control QSYNC function. QS_TIME_OUT[15:0]: Qsync Time Out Value TE_EXT_TIME_OUT[15:0]: TE Extension Time Out Value													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD WRQSYNCTO[WRQSYNCTO] --> QS[QS_TIME_OUT[10:0]] QS --> NCV[New Control Value] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.62 (6Eh) RDQSYNCTO: Read QSYNC Timeout Value

Command Set		RDQSYNCTO								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDQSYNCTO	R	0	1	1	0	1	1	1	0	6Eh
Parameter	1	QS_TIME_OUT[15:8]								
Parameter	2	QS_TIME_OUT[7:0]								
Parameter	3	TE_EXT_TIME_OUT[15:8]								
Parameter	4	TE_EXT_TIME_OUT[7:0]								

NOTE: “-”Don’t care.

Description	This command is used to read the status of QSYNC function. QS_TIME_OUT[15:0]: Qsync Time Out Value TE_EXT_TIME_OUT[15:0]: TE Extension Time Out Value													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value													
Power On Sequence	000h													
S/W Reset	000h													
H/W Reset	000h													
Flow Chart	<pre> graph TD Host -- RDQSYNCTO --> Driver subgraph Legend [Legend] direction TB R[Command] --- D[Parameter] D --- T1[Display] T1 --- T2[Action] T2 --- M[Mode] M --- ST[Sequential transfer] end subgraph RDQSYNCTO [RDQSYNCTO] direction TB R --- P1{Send 1st Parameter} P1 --- P2{Send 2nd Parameter} end </pre>													

9.3.63 (71h) WRTEMP: Write TEMP Value

Command Set	WRTEMP
-------------	--------

Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRTEMP	W	0	1	1	1	0	0	0	1	71h
Parameter	1					TEMP[7:0]				00h

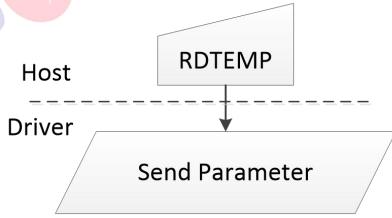
NOTE: “-”Don’t care.

Description	This command is used to control temperature function. TEMP[7:0]: Temperature Data from HOST													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	<pre> graph TD WRTEMP[WRTEMP] --> TEMP[TEMP[7:0]] TEMP --> NCV[New Control Value] </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.64 (72h) RDTEMP: Read TEMP Value

Command Set		RDTEMP									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDTEMP	R	0	1	1	1	0	0	1	0	72h	
Parameter	1	TEMP[7:0]									

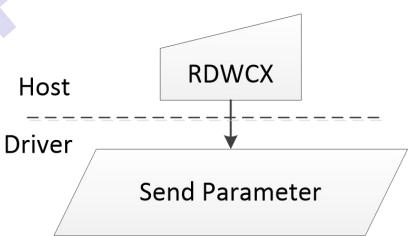
NOTE: “-”Don’t care.

Description	This command is used to control temperature function. TEMP[7:0]: Temperature Data from HOST													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host[Host] -- RDTEMP --> Driver[Driver] Driver -- Send Parameter --> SendParameter[/Send Parameter/] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.65 (73h) RDWCX: Read W Coor. X

Command Set		RDWCX									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDWCX	R	0	1	1	1	0	0	1	1	73h	
Parameter	1	READ_W_X[7:0]									

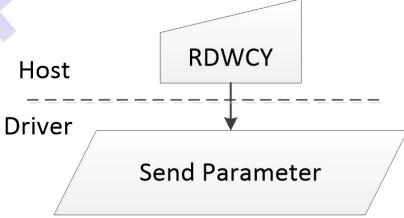
NOTE: “-”Don’t care.

Description	This command is used to read the status. READ_W_X[7:0]: WX bits (WX[7:0]) of white color characteristics													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host -- RDWCX --> Driver Driver -- "Send Parameter" --> null </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.66 (74h) RDWCY: Read W Coor. Y

Command Set		RDWCY									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDWCY	R	0	1	1	1	0	1	0	0	74h	
Parameter	1	READ_W_Y[7:0]									

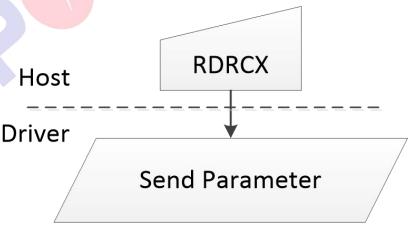
NOTE: “-”Don’t care.

Description	This command is used to read the status. READ_W_Y[7:0]: WY bits (WY[7:0]) of white color characteristics													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host -- RDWCY --> Driver Driver -- "Send Parameter" --> None </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.67 (76h) RDRCX: Read R Coor. X

Command Set		RDRCX								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDRCX	R	0	1	1	1	0	1	1	0	76h
Parameter	1	READ_R_X[7:0]								

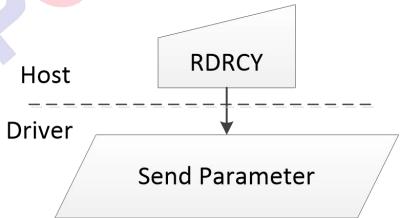
NOTE: “-”Don’t care.

Description	This command is used to read the status. READ_R_X[7:0]: RX bits (RX[7:0]) of Red color characteristics.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host -- RDRCX --> Driver Driver -- Send Parameter --> None </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.68 (77h) RDRCY: Read R Coor. Y

Command Set		RDRCY									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDRCY	R	0	1	1	1	0	1	1	1	77h	
Parameter	1	READ_R_Y[7:0]									

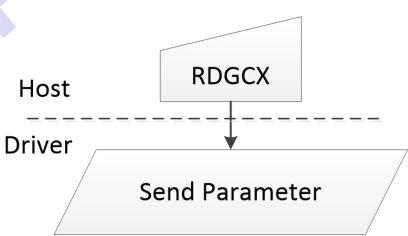
NOTE: “-”Don’t care.

Description	This command is used to read the status. READ_R_Y[7:0]: RY bits (RY[7:0]) of Red color characteristics.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host -- RDRCY --> Driver Driver -- "Send Parameter" --> None </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.69 (78h) RDGCX: Read G Coor. X

Command Set		RDGCX								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDGCX	R	0	1	1	1	1	0	0	0	78h
Parameter	1	READ_G_X[7:0]								

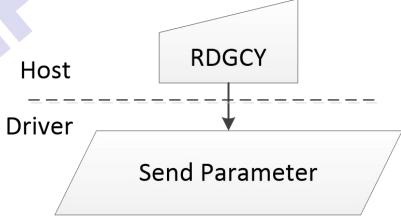
NOTE: “-”Don’t care.

Description	This command is used to read the status. READ_G_X[7:0]: GX bits (GX[7:0]) of Green color characteristics													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host[Host] -- RDGCX --> Driver[Driver] Driver -- "Send Parameter" --> SendParam[/Send Parameter/] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.70 (79h) RDGCY: Read G Coor. Y

Command Set		RDGCY									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDGCY	R	0	1	1	1	1	0	0	1	79h	
Parameter	1	READ_G_Y[7:0]									

NOTE: “-”Don’t care.

Description	This command is used to read the status. READ_G_Y[7:0]: GY bits (GY[7:0]) of Green color characteristics													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host -- RDGCY --> Driver Driver -- Send Parameter --> None </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.71 (7Bh) RDBCX: Read B Coor. X

Command Set		RDBCX								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDBCX	R	0	1	1	1	1	0	1	1	7Bh
Parameter	1	READ_B_X[7:0]								

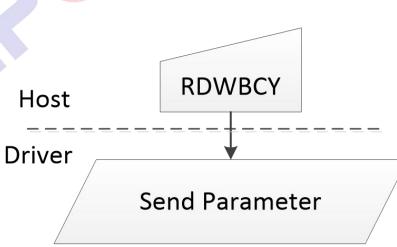
NOTE: “-”Don’t care.

Description	This command is used to read the status. READ_B_X[7:0]: BX bits (BX[7:0]) of Blue color characteristics.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	<pre> graph TD Host[Host] --> RDBCX[RDBCX] RDBCX --> SendParam[Send Parameter] subgraph Legend [Legend] direction TB L1[Command] L2[Parameter] L3[Display] L4[Action] L5[Mode] L6[Sequential transfer] end </pre> <p>The flowchart illustrates the communication between the Host and the Driver. The Host initiates the process by sending the RDBCX command to the Driver. The Driver then performs the action of sending a parameter. A legend on the right side defines the symbols used in the flowchart: a rectangle for Command, a trapezoid for Parameter, a parallelogram for Display, a diamond for Action, an oval for Mode, and an ellipse for Sequential transfer.</p>													

9.3.72 (7Ch) RDWBCY: Read B Coor. Y

Command Set		RDWBCY								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDWBCY	R	0	1	1	1	1	1	0	0	7Ch
Parameter	1	READ_B_Y[7:0]								

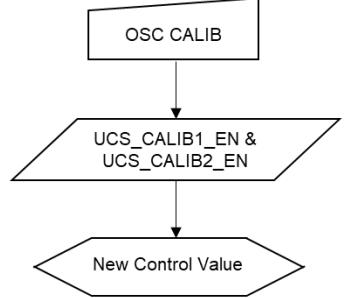
NOTE: “-”Don’t care.

Description	This command is used to read the status. READ_B_Y[7:0]: BY bits (BY[7:0]) of Blue color characteristics													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host -- RDWBCY --> Driver Driver -- "Send Parameter" --> None </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.73 (80h) OSC CALIB: OSC Calibration Control

Command Set		OSC CALIB								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
OSC CALIB	W	1	0	0	0	0	0	0	0	80h
Parameter	1	0	CALIB_TARG_SEL[2:0]			0	0	UCS_CALIB2_EN	UCS_CALIB1_EN	00h

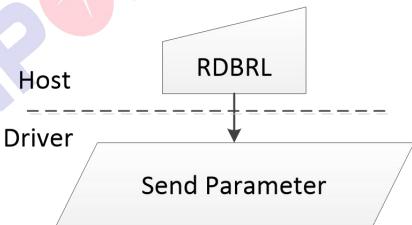
NOTE: “-”Don’t care.

Description	<p>This command is used to write for OSC Calibration 1/2 Control.</p> <p>CALIB_TARG_SEL[2:0] : Calibration Target Selection Control.</p> <p>UCS_CALIB1_EN : OSC128 Calibration1 Enable/Disable Control</p> <p>UCS_CALIB2_EN : OSC155 Calibration2 Enable/Disable Control</p>													
Restriction	-													
Register Availability	<table border="1" data-bbox="446 970 1367 1260"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1" data-bbox="446 1327 1367 1529"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD A[OSC CALIB] --> B{UCS_CALIB1_EN & UCS_CALIB2_EN} B --> C{New Control Value} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.74 (84h) RDBRL: Read BR Low Byte

Command Set		RDBRL									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDBRL	R	1	0	0	0	0	1	0	0	84h	
Parameter	1	READ_BR[7:0]									

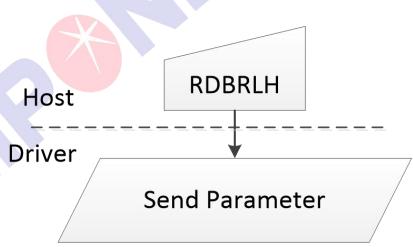
NOTE: “-”Don’t care.

Description	This command is used to read the status.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host --> RDBRL[RDBRL] RDBRL --> SendParameter[Send Parameter] subgraph Legend [Legend] direction TB L1[Command] L2[Parameter] L3[Display] L4[Action] L5[Mode] L6[Sequential transfer] end </pre>													

9.3.75 (85h) RDBRH: Read BR High Byte

Command Set		RDBRH									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDBRH	R	1	0	0	0	0	1	0	1	85h	
Parameter	1	READ_BR[15:8]									

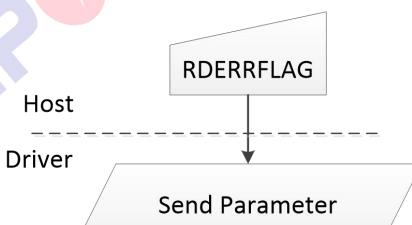
NOTE: “-”Don’t care.

Description	This command is used to read the status.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
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Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host[Host] --> RDBRLH[RDBRLH] RDBRLH --> SendParameter[Send Parameter] SendParameter --> Driver[Driver] </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.76 (8Fh) RDERRFLAG: Read Error Flag Status

Command Set		RDERRFLAG									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDERRFLAG	R	1	0	0	0	1	1	1	1	8Fh	
Parameter	1	READ_ERR_FLAG[7:0]									00h

NOTE: “-”Don’t care.

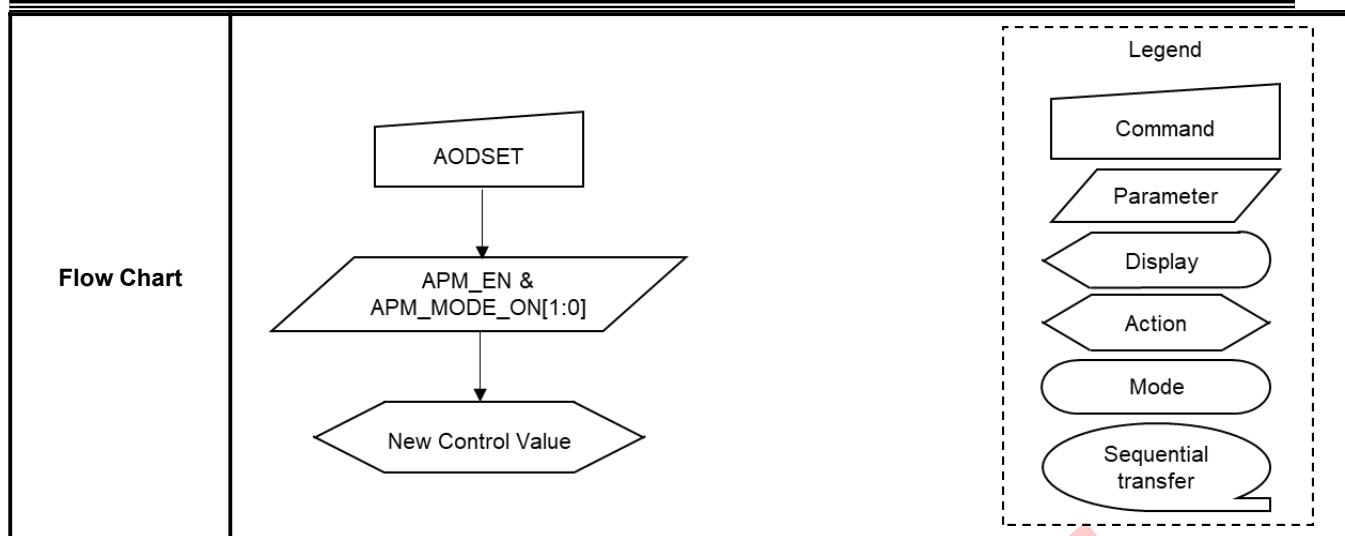
Description	This command is used to read the status. READ_ERR_FLAG[7:0]: Error Flag Information													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host[Host] -- RDERRFLAG --> Driver[Driver] Driver -- Send Parameter --> Param[/Send Parameter/] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.77 (90h) AODSET: Write AOD Value

Command Set		AODSET								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
AODSET	W	1	0	0	1	0	0	0	0	90h
Parameter	1	APM_EN	0	0	0	0	0	0	AOD_MODE_ON	00h

NOTE: “-”Don’t care.

Description	This command is used to control AOD Mode function.													
	APM_EN: Auto Pixel Moving On/Off Control													
	APM_EN	Description												
	0	Off												
	1	On												
Restriction	AOD_MODE_ON: AOD Mode On/Off Control													
	0	AOD MODE OFF												
	1	AOD MODE ON												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													



9.3.78 (91h) WRVR_CTRL: Write VR Value

Command Set		WRVR_CTRL								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRVR_CTRL	W	1	0	0	1	0	0	0	1	91h
Parameter	1	0	0	0	0	0	0	0	VR_EN	00h

NOTE: “-”Don’t care.

Description	This command is used to control VR function.													
	VR_EN: VR Mode On/Off Control													
	<table border="1"> <thead> <tr> <th>VR_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Off</td> </tr> <tr> <td>1</td> <td>On</td> </tr> </tbody> </table>		VR_EN	Description	0	Off	1	On						
VR_EN	Description													
0	Off													
1	On													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	<pre> graph TD WRVR_CTRL[WRVR_CTRL] --> VR_EN{VR_EN} VR_EN --> NewValue{New Control Value} </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.79 (92h) RDVR_CTRL: Read VR Value

Command Set		RDVR_CTRL								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDVR_CTRL	R	1	0	0	1	0	0	1	0	92h
Parameter	1	0	0	0	0	0	0	0	VR_EN	00h

NOTE: “-”Don’t care.

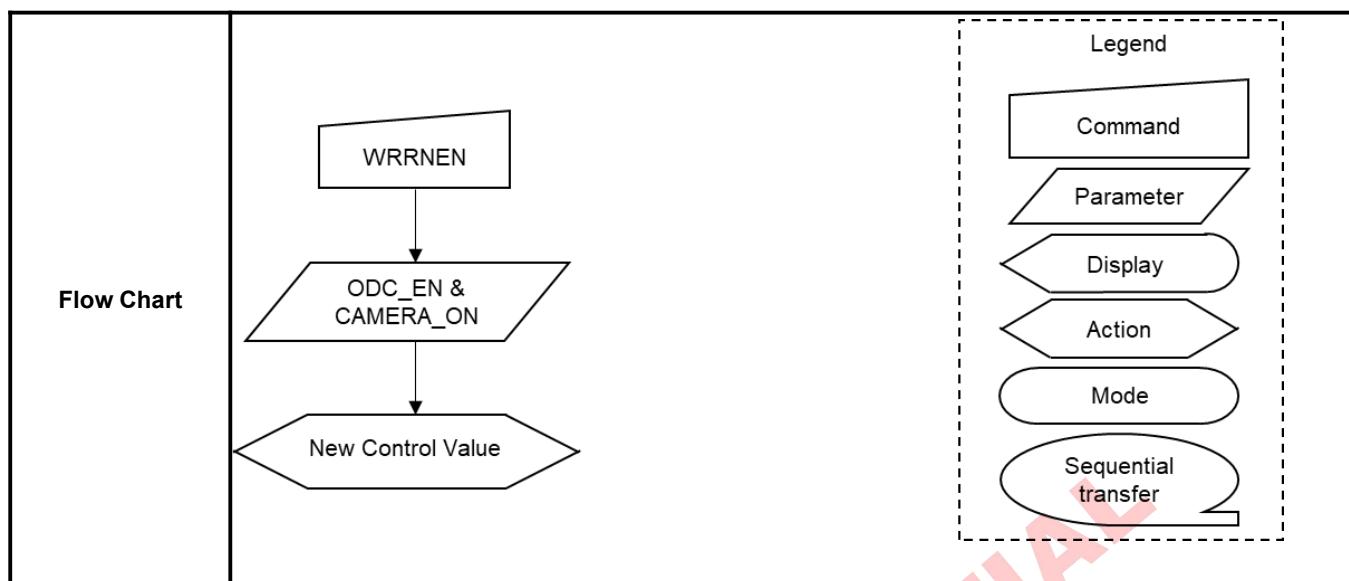
Description	This command is used to control VR function. VR_EN: VR Mode On/Off Control													
	<table border="1"> <thead> <tr> <th>VR_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Off</td> </tr> <tr> <td>1</td> <td>On</td> </tr> </tbody> </table>		VR_EN	Description	0	Off	1	On						
VR_EN	Description													
0	Off													
1	On													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	<pre> graph TD Host -- RDVR_CTRL --> Driver Driver -- "Send Parameter" --> SendParameter[/Send Parameter/] </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.80 (93h) WRRNEN: Write RN Value

Command Set		WRRNEN								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRRNEN	W	1	0	0	1	0	0	1	1	93h
Parameter		1	0	0	0	ODC_EN	0	0	CAMERA_ON	00h

NOTE: “-”Don’t care.

Description	ODC_EN: ODC On/Off Control													
	ODC_EN	Description												
	0	Off												
	1	On												
Restriction	CAMERA_ON: Camera on/off Control													
	CAMERA_ON	Description												
	0	Off												
	1	On												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													



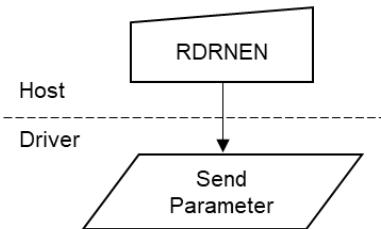
9.3.81 (94h) RDRNEN: Read RN Value

Command Set		RDRNEN									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDRNEN	R	1	0	0	1	0	1	0	0	94h	
Parameter	1	0	0	0	ODC_EN	0	0	0	CAMERA_ON	00h	

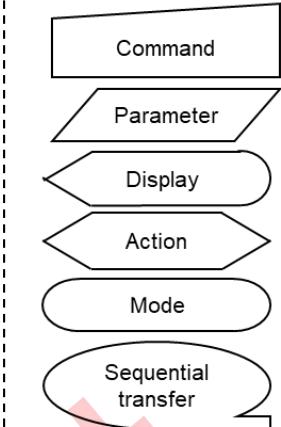
NOTE: “-”Don’t care.

Description	ODC_EN: ODC On/Off Control													
	ODC_EN	Description												
	0	Off												
	1	On												
Restriction	CAMERA_ON: Camera on/off Control													
	CAMERA_ON	Description												
	0	Off												
	1	On												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

Flow Chart



Legend



9.3.82 (95h) WTECC_WT: Write ECC Value

Command Set		WTECC_WT									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
WTECC_WT	W	1	0	0	1	0	1	0	1	95h	
Parameter	1	0	0	0	0	0	0	0	ECC_WT	00h	

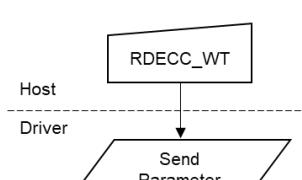
NOTE: “-”Don’t care.

Description	This command is used to control OTP. ECC_WT : OTP Auto Write Start signal for ECC registers													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	<pre> graph TD A[WTECC_WT] --> B[ECC_WT] B --> C[New Control Value] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.83 (96h) RDECC_WT: Read ECC Value

Command Set		RDECC_WT									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDECC_WT	R	1	0	0	1	0	1	1	0	96h	
Parameter	1	0	0	0	0	0	0	0	ECC_WT	00h	

NOTE: “-”Don’t care.

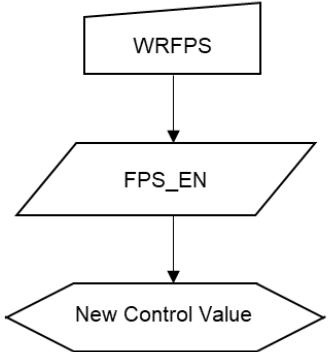
Description	This command is used to control OTP. ECC_WT : ECC_WT : OTP Auto Write Start signal for ECC registers													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host[Host] --> RDECC_WT[RDECC_WT] RDECC_WT --> SendParam[/Send Parameter/] subgraph Legend [Legend] Command[Command] Parameter[Parameter] Display[Display] Action[Action] Mode[Mode] Sequential[Sequential transfer] end </pre>													

9.3.84 (97h) WRFPS: Write FPS

Command Set		WRFPS								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRFPS	W	1	0	0	1	0	1	1	1	97h
Parameter	1	0	0	0	0	0	0	0	FPS_EN	00h
Parameter	2	FPS_GAIN_CTRL_EN	0	0	0	FPS_GAIN[11:8]				00h
Parameter	3	FPS_GAIN[7:0]								00h

NOTE: “-”Don’t care.

Description	This command is used to control FPS function.													
	FPS_EN : FPS Mode On/Off Control													
	<table border="1"> <thead> <tr> <th>FPS_EN</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Off</td></tr> <tr> <td>1</td><td>On</td></tr> </tbody> </table>		FPS_EN	Description	0	Off	1	On						
FPS_EN	Description													
0	Off													
1	On													
	FPS_GAIN_CTRL_EN : Alpha Gain On/Off Control													
	<table border="1"> <thead> <tr> <th>FPS_GAIN_CTRL_EN</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Off</td></tr> <tr> <td>1</td><td>On</td></tr> </tbody> </table>		FPS_GAIN_CTRL_EN	Description	0	Off	1	On						
FPS_GAIN_CTRL_EN	Description													
0	Off													
1	On													
	FPS_GAIN[11:0] : Alpha Gain value control													
	$\frac{\text{Input Image} \times \text{FPS_GAIN}[11:0]}{4096}, 0 < \text{FPS_GAIN}[11:0] \leq 4095$													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													

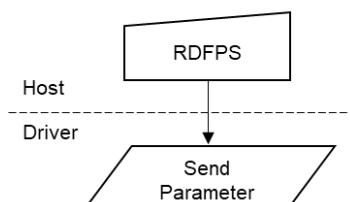
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></tbody></table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value								
Power On Sequence	00h								
S/W Reset	00h								
H/W Reset	00h								
Flow Chart	 <pre>graph TD; A[WRFPS] --> B{FPS_EN}; B --> C{New Control Value}</pre> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer								

9.3.85 (98h) RDPFS: Read FPS

Command Set		RDFPS									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDFPS	R	1	0	0	1	1	0	0	0	98h	
Parameter	1	0	0	0	0	0	0	0	FPS_EN	00h	
Parameter	2	FPS_GAIN_CTRL_EN	0	0	0	FPS_GAIN[11:8]				00h	
Parameter	3	FPS_GAIN[7:0]								00h	

NOTE: “-”Don’t care.

Description	This command is used to control FPS function.													
	FPS_EN: FPS Mode On/Off Control													
	<table border="1"> <thead> <tr> <th>FPS_EN</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Off</td></tr> <tr> <td>1</td><td>On</td></tr> </tbody> </table>		FPS_EN	Description	0	Off	1	On						
FPS_EN	Description													
0	Off													
1	On													
FPS_GAIN_CTRL_EN : Alpha Gain On/Off Control														
Restriction	<table border="1"> <thead> <tr> <th>FPS_GAIN_CTRL_EN</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>Off</td></tr> <tr> <td>1</td><td>On</td></tr> </tbody> </table>		FPS_GAIN_CTRL_EN	Description	0	Off	1	On						
FPS_GAIN_CTRL_EN	Description													
0	Off													
1	On													
FPS_GAIN[11:0] : Alpha Gain value control														
$\frac{\text{Input Image} \times \text{FPS_GAIN}[11:0]}{4096}, 0 < \text{FPS_GAIN}[11:0] \leq 4095$														
-														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													

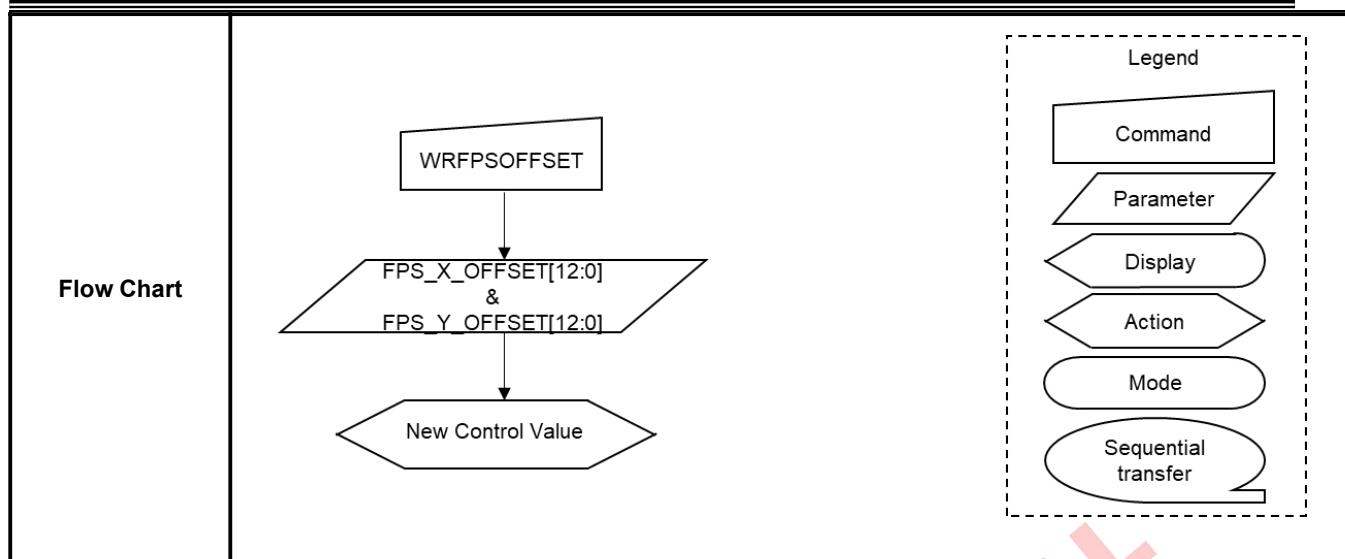
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></tbody></table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value								
Power On Sequence	00h								
S/W Reset	00h								
H/W Reset	00h								
Flow Chart	 <p>The flowchart illustrates the communication process. It starts with a rectangular box labeled "RDFPS" at the top, with an arrow pointing down to a trapezoidal box labeled "Send Parameter". The "Host" is positioned above the "RDFPS" box, and the "Driver" is positioned below the "Send Parameter" box, separated by a dashed horizontal line.</p> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer								

9.3.86 (99h) WRFPSOFFSET: Write FPS Offset Value

Command Set		WRFPSOFFSET								
Inst / Para	W /R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
WRFPSOFFSET	W	1	0	0	1	1	0	0	1	99h
Parameter	1	0	0	0	FPS_X_OFFSET[12:8]					00h
Parameter	2	FPS_X_OFFSET[7:0]							00h	
Parameter	3	0	0	0	FPS_Y_OFFSET[12:8]					00h
Parameter	4	FPS_Y_OFFSET[7:0]							00h	

NOTE: “-”Don’t care.

Description	This command is used to control FPS function. FPS_X/Y_OFFSET : FPS X position offset FPS_X/Y_OFFSET[12] is sign bit If FPS_X/Y_OFFSET[12] = 0, FPS Circle x position is FPS_X_POS + FPS_X_OFFSET[11:0] If FPS_X/Y_OFFSET[12] = 1, FPS Circle x position is FPS_X_POS - FPS_X_OFFSET[11:0]													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value				
Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													

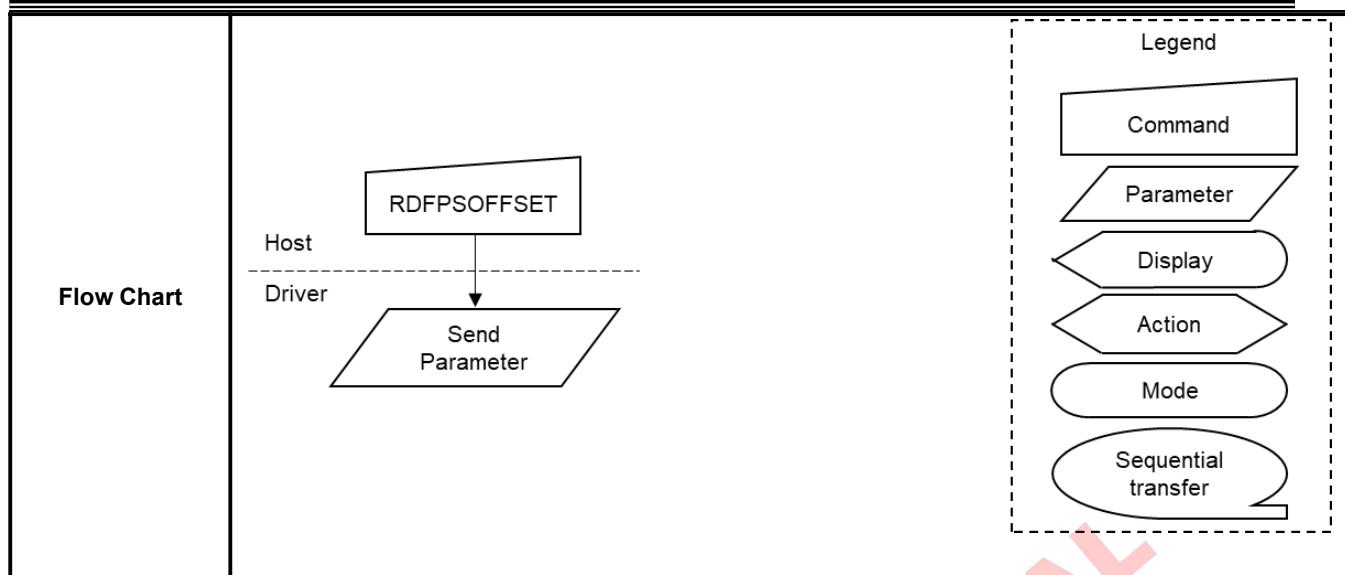


9.3.87 (9Ah) RDFPSOFFSET: Read FPS Offset Value

Command Set		RDFPSOFFSET								
Inst / Para	W /R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDFPSOFFSET	R	1	0	0	1	1	0	1	0	9Ah
Parameter	1	0	0	0	FPS_X_OFFSET[12:8]					00h
Parameter	2	FPS_X_OFFSET[7:0]							00h	
Parameter	3	0	0	0	FPS_Y_OFFSET[12:8]					00h
Parameter	4	FPS_Y_OFFSET[7:0]							00h	

NOTE: “-”Don’t care.

Description	This command is used to control FPS function. FPS_X/Y_OFFSET : FPS X position offset FPS_X/Y_OFFSET[12] is sign bit If FPS_X/Y_OFFSET[12] = 0, FPS Circle x position is FPS_X_POS + FPS_X_OFFSET[11:0] If FPS_X/Y_OFFSET[12] = 1, FPS Circle x position is FPS_X_POS - FPS_X_OFFSET[11:0]													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value				
Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													

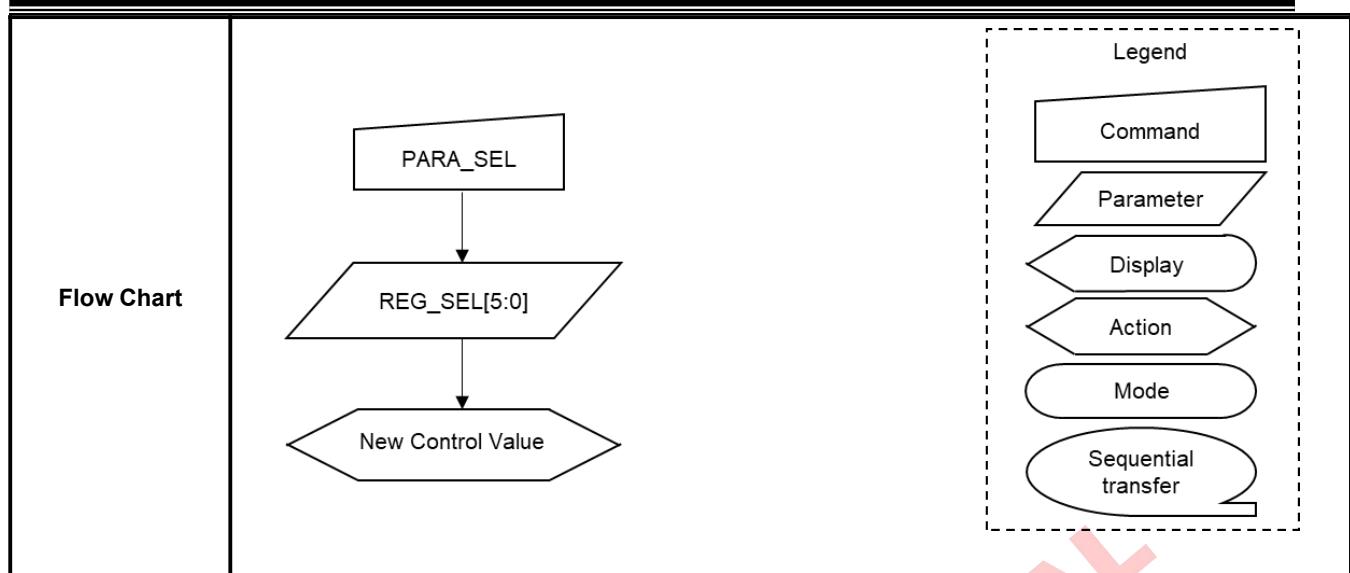


9.3.88 (9Bh) PARA_SEL: MCS Parameter Value

Command Set		PARA_SEL									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
PARA_SEL	W	1	0	0	1	1	0	1	1	9Bh	
Parameter	1	0	0	REG_SEL[5:0]						00h	

NOTE: “-”Don’t care.

Description	This command is used to control Register Parameter Selection													
	REG_SEL[5:0]	Description												
	00h	1'st Parameter												
	01h	2'nd Parameter												
	02h	3'rd Parameter												
	03h	4'th Parameter												
	04h	5'th Parameter												
	05h	6'th Parameter												
	06h	7'th Parameter												
	07h	8'th Parameter												
	08h	9'th Parameter												
	09h	10'th Parameter												
	0Ah	11'th Parameter												
	0Bh	12'th Parameter												
	0Ch	13'th Parameter												
												
	3Fh	64'th Parameter												
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value				
Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													

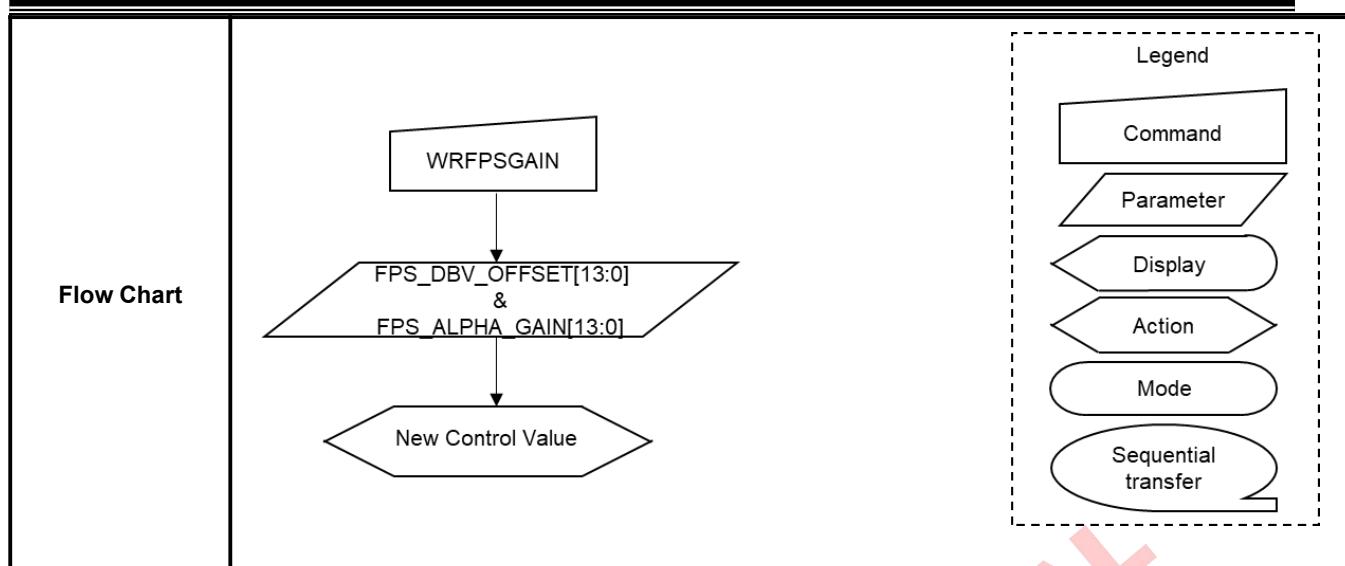


9.3.89 (9Dh) WRFPSEGAIN: Write FPS Gain Value

Command Set		WRFPSEGAIN									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
WRFPSEGAIN	W	1	0	0	1	1	1	0	1	9Dh	
Parameter	1	0	0	FPS_DBV_OFFSET[13:8]						00h	
Parameter	2	FPS_DBV_OFFSET[7:0]								00h	
Parameter	3	0	0	FPS_ALPHA_GAIN[13:8]						20h	
Parameter	4	FPS_ALPHA_GAIN[7:0]								00h	

NOTE: “-”Don’t care.

Description	This command is used to control FPS function. FPS_DBV_OFFSET : DBV Offset when FPS turn on FPS_DBV_OFFSET[13] is sign bit If FPS_DBV_OFFSET[13] = 0, DBV = DBV – FPS_DBV_OFFSET[12:0] If FPS_DBV_OFFSET[13] = 1, DBV = DBV + FPS_DBV_OFFSET[12:0] FPS_ALPHA_GAIN : DBV Gain when FPS turn on FPS1_GAIN(DGM Block) = FPS1_GAIN(BC Block) * FPS_ALPHA_GAIN												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value				
Status	Default Value												
Power On Sequence	OTP Value												
S/W Reset	OTP Value												
H/W Reset	OTP Value												

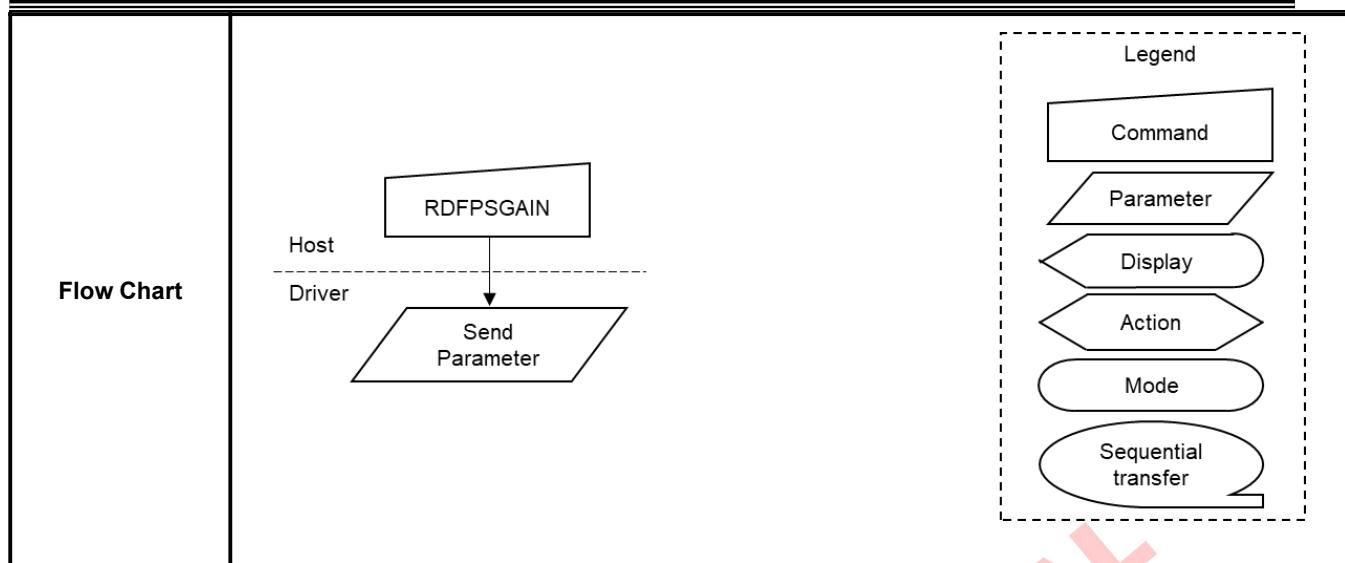


9.3.90 (9Eh) RDFPSGAIN: Read FPS Gain Value

Command Set		RDFPSGAIN									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDFPSGAIN	R	1	0	0	1	1	1	1	0	9Eh	
Parameter	1	0	0	FPS_DBV_OFFSET[13:8]						00h	
Parameter	2	FPS_DBV_OFFSET[7:0]									
Parameter	3	0	0	FPS_ALPHA_GAIN[13:8]						20h	
Parameter	4	FPS_ALPHA_GAIN[7:0]									

NOTE: “-”Don’t care.

Description	This command is used to control FPS function. FPS_DBV_OFFSET : DBV Offset when FPS turn on FPS_DBV_OFFSET[13] is sign bit If FPS_DBV_OFFSET[13] = 0, DBV = DBV – FPS_DBV_OFFSET[12:0] If FPS_DBV_OFFSET[13] = 1, DBV = DBV + FPS_DBV_OFFSET[12:0] FPS_ALPHA_GAIN : DBV Gain when FPS turn on FPS1_GAIN(DGM Block) = FPS1_GAIN(BC Block) * FPS_ALPHA_GAIN												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value				
Status	Default Value												
Power On Sequence	OTP Value												
S/W Reset	OTP Value												
H/W Reset	OTP Value												

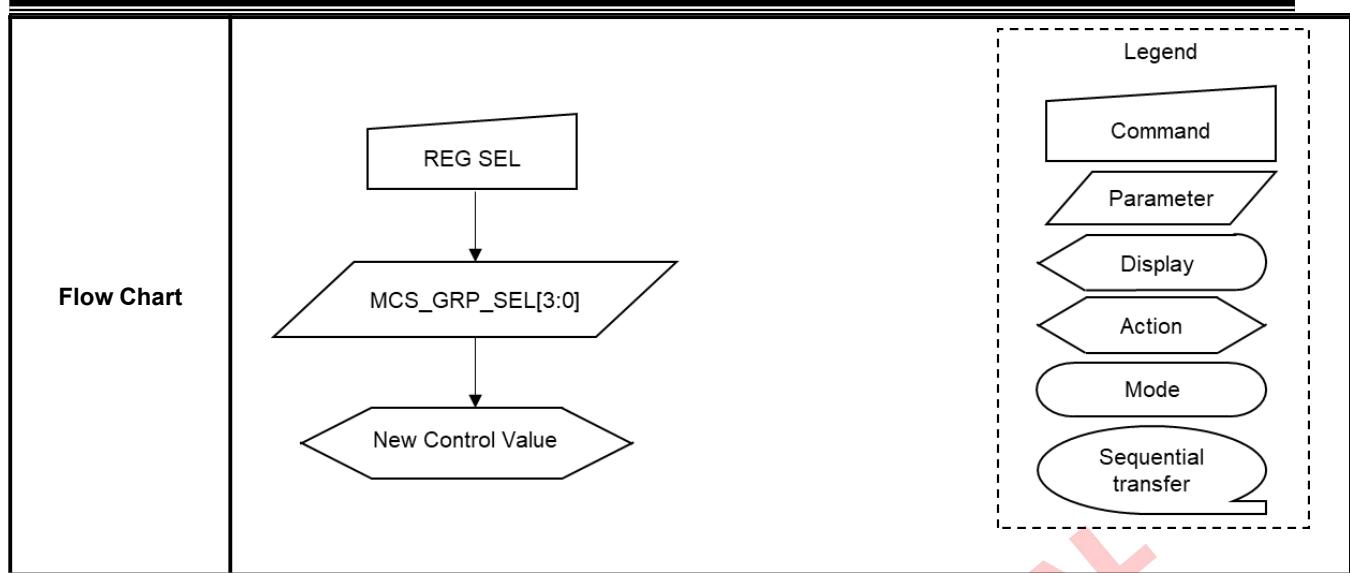


9.3.91 (9Fh) REG SEL: MCS Group Selection

Command Set		REG SEL									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
REG SEL	W	1	0	0	1	1	1	1	1	9Fh	
Parameter	1	0	0	0	0	MCS_GRP_SEL[3:0]				00h	

NOTE: “-”Don’t care.

Description	This command is used to control Register Group Selection	
	MCS_GRP_SEL[3:0]	Description
	0h	Disable MCS Group Selection
	1h	Register Group 1
	2h	Register Group 2
	3h	Register Group 3
	4h	Register Group 4
	5h	Register Group 5
	6h	Register Group 6
	7h	Register Group 7
	8h	Register Group 8
	9h	Register Group 9
	Ah	Register Group A
	Bh	Register Group B
	Ch	Register Group C
	Dh	Register Group D
	Eh	Register Group E
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	OTP Value
	S/W Reset	OTP Value
	H/W Reset	OTP Value

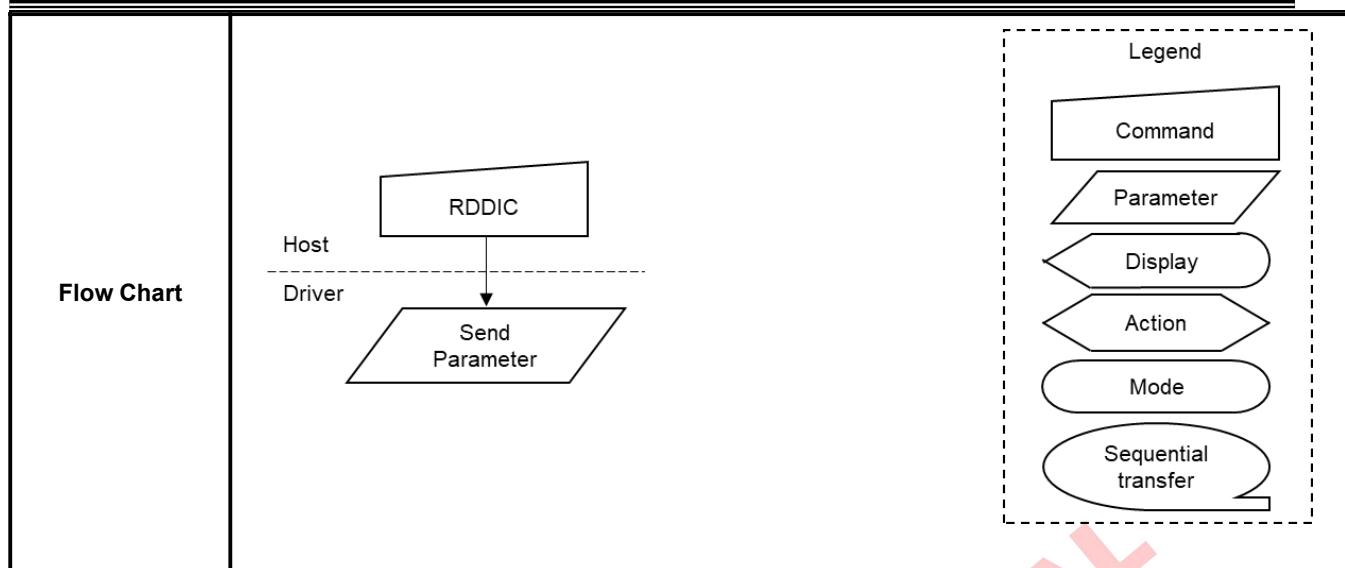


9.3.92 (A0h) RDDIC: Read DIC

Command Set		RDDIC									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDDIC	R	1	0	1	0	0	0	0	0	A0h	
Parameter	1	0	0	1	1	0	1	0	1	35h	
Parameter	2	0	0	0	1	0	0	1	0	12h	
Parameter	3	REV_ID[7:0]								00h	
Parameter	4	LOT_ID1[7:0]								00h	
Parameter	Nth	LOT_IDn[7:0]								00h	
Parameter	27	LOT_ID24[7:0]								00h	

NOTE: “-”Don’t care.

Description														
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value				
Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													



9.3.93 (A1h) RDDDB: Read DDB Start

Command Set		RDDDB									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDDDB	R	1	0	1	0	0	0	0	1	A1h	
Parameter	1	IDX1[7:0]								OTP	
Parameter	Nth	IDXn[7:0]								OTP	
Parameter	24	IDX24[7:0]								OTP	

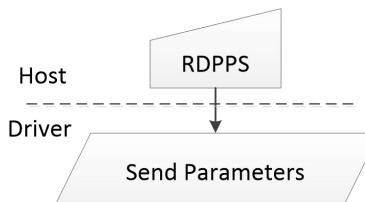
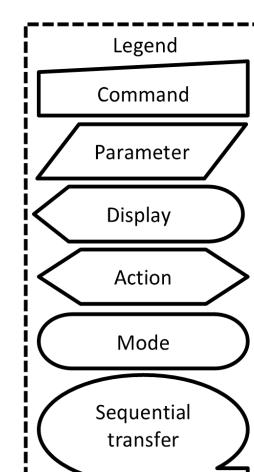
NOTE: ““Don’t care.

Description	This command returns supplier identification and display module model/revision information. NOTE: This information is not the same RDID1(DAh) : Read ID1, RDID2(DBh) : Read ID2 and RDID3(DCh) : Read ID3 commands are returning. This read sequence can be interrupted by any command and it can be continued by “RDDDBC (A8h)” when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS → 1st parameter has been sent → 2nd Parameter has been sent → interrupt → RDDDBC → 3rd parameter of the RDDDBS has been sent.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													
Flow Chart	<p>The flowchart illustrates the communication sequence between the Host and the Driver. The Host initiates the process by sending an RDDDB command to the Driver. The Driver then responds by sending parameters. A legend on the right side of the diagram provides a key for the symbols used in the flowchart:</p> <ul style="list-style-type: none"> Command: Represented by a square symbol. Parameter: Represented by a triangle symbol. Display: Represented by a diamond symbol. Action: Represented by a hexagon symbol. Mode: Represented by an oval symbol. Sequential transfer: Represented by a circle symbol. 													

9.3.94 (A2h) RDPPS: Read PPS

Command Set		RDPPS								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDPPS	R	1	0	1	0	0	0	1	0	A2h
Parameter	1	PPS1[7:0]								OTP
Parameter	Nth	PPSN[7:0]								OTP
Parameter	128	PPS128[7:0]								OTP

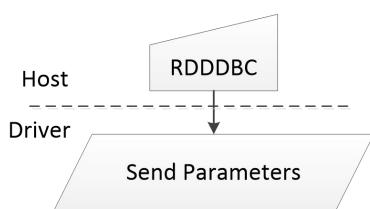
NOTE: “—”“Don’t care.

Description	This command returns DSC PPS (picture parameter set) table data. There's 4 table for PPS set. if host want to read specific table's PPS data, host should set PPSSEL(compress mode command packet. MIPI DSI Data type 0x07 0x01) table value first.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value				
Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													
Flow Chart	 <pre> graph TD Host[Host] -- RDPPS --> Driver[Driver] Driver -- "Send Parameters" --> Send[Send Parameters] </pre>	 <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.95 (A8h) RDDDBC: Read DDB Continue

Command Set		RDDDBC								
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX
RDDDBC	R	1	0	1	0	1	0	0	0	A8h
Parameter	1	IDX1[7:0]							OTP	
Parameter	Nth	IDXn[7:0]							OTP	
Parameter	128	IDX128[7:0]							OTP	

NOTE: “—”Don’t care.

Description	This command returns supplier's identification and display module model/revision information from the point where RDDDBS command was interrupt by another command e.g. RDDDBS was interrupted after 2nd parameter. The first parameter, what RDDDBC is returning is 3rd parameter.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													
Flow Chart	 <pre> graph TD Host[Host] -- "RDDDBC" --> Driver[Driver] Driver -- "Send Parameters" --> Send[Send Parameters] </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.96 (A9h) RDPPSC: Read Continue PPS

Command Set		RDPPSC									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDPPSC	R	1	0	1	0	1	0	0	1	A9h	
Parameter	1	PPS1[7:0]								OTP	
Parameter	Nth	PPSn[7:0]								OTP	
Parameter	128	PPS128[7:0]								OTP	

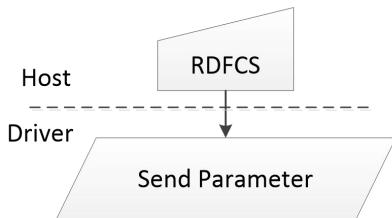
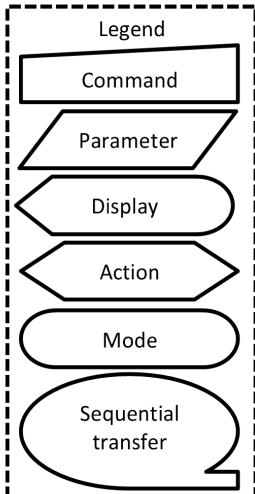
NOTE: ““Don’t care.

Description	<p>This command returns DSC PPS (picture parameter set) table data.</p> <p>There's 4 table for PPS set. if host want to read specific table's PPS data, host should set PPSSEL(compress mode command packet. MIPI DSI Data type 0x07 0x01) table value first.</p> <p>This command returns DSC PPS (picture parameter set) table data from the point where RDPPS command was interrupt by another command e.g. RDPPS was interrupted after 2nd parameter. The first parameter, what RDPPSC is returning is 3rd parameter.</p>													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													
Flow Chart	 <pre> graph TD Host -- RDPPSC --> Driver Driver -- Send Parameters --> None </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.97 (AAh) RDFCS: Read First Checksum

Command Set		RDFCS									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDFCS	R	1	0	1	0	1	0	1	0	AAh	
Parameter	1	FCS[7:0]									

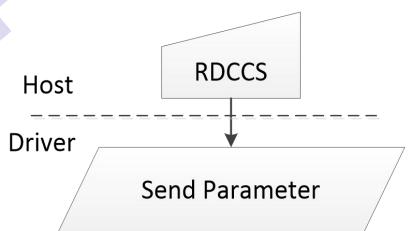
NOTE: “-”Don’t care.

Description	This command returns the first checksum what has been calculated from “User Command Set” area registers (not included “Manufacture Command Set”) after the write access to those registers has been done.													
Restriction	It will be necessary to wait 150ms after there is the last write access on “User Command Set” area registers before there can read this checksum value.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host[Host] --> RDFCS[RDFCS] RDFCS --> SendParam[Send Parameter] SendParam --> Driver[Driver] </pre>	 <pre> graph LR subgraph Legend [Legend] direction TB L1[Command] --- R1[] L2[Parameter] --- R2[] L3[Display] --- R3[] L4[Action] --- R4[] L5[Mode] --- R5[] L6[Sequential transfer] --- R6[] end </pre>												

9.3.98 (AFh) RDCCS: Read Continue Checksum

Command Set		RDCCS									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDCCS	R	1	0	1	0	1	1	1	1	AFh	
Parameter	1	CCS[7:0]									00h

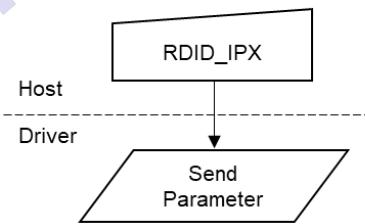
NOTE: “-”Don’t care.

Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from some “User Command Set” area registers after the write access to those registers has been done.													
Restriction	It will be necessary to wait 300ms after there is the last write access on “User Command Set” area registers before there can read this checksum value.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Sleep In	Yes													
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													
Flow Chart	 <pre> graph TD Host[Host] -- RDCCS --> Driver[Driver] Driver -- "Send Parameter" --> SendParam[/Send Parameter/] </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.99 (B1h) RDID_UDI: Read ID_UDI - Please do not open to BOE.

Command Set		RDID_IPX									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDID_IPX	R	1	0	1	1	0	0	0	1	B1h	
Parameter	1	UDI1[7:0]								00h	
Parameter	Nth	UDIn[7:0]								00h	
Parameter	19	UDI19[7:0]								00h	

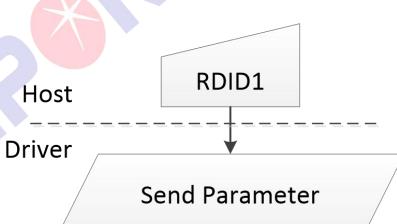
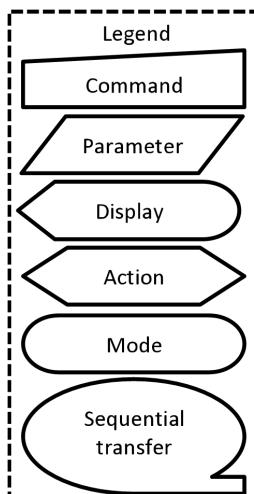
NOTE: “-”Don’t care.

Description	This read byte identifies a User Defined Information.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value				
Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													
Flow Chart	 <pre> graph TD Host -- RDID_IPX --> Driver Driver -- "Send Parameter" --> None </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.100 (DAh) RDID1: Read ID1

Command Set		RDID1									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDID1	R	1	1	0	1	1	0	1	0	DAh	
Parameter	1	DM_ID1[7:0]									

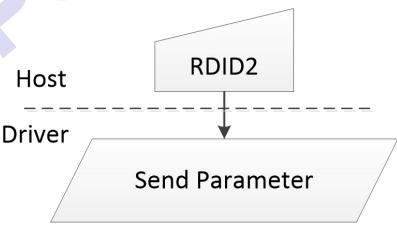
NOTE: “-”Don’t care.

Description	This read byte identifies the OLED module's manufacturer.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value				
Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													
Flow Chart	 <pre> graph TD Host -- RDID1 --> Driver Driver -- "Send Parameter" --> Output </pre>	 <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

9.3.101 (DBh) RDID2: Read ID2

Command Set		RDID2									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDID2	R	1	1	0	1	1	0	1	1	DBh	
Parameter	1	DM_ID2[7:0]									

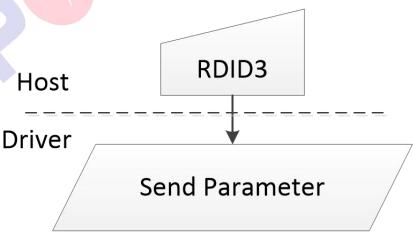
NOTE: “-”Don’t care.

Description	This read byte is used to track the OLED module/driver version. It is defined by internal and changes each time a revision is made to the display, material or construction specifications.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OTP Value</td> </tr> <tr> <td>S/W Reset</td> <td>OTP Value</td> </tr> <tr> <td>H/W Reset</td> <td>OTP Value</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	OTP Value	S/W Reset	OTP Value	H/W Reset	OTP Value				
Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													
Flow Chart	 <pre> graph TD Host[Host] -- RDID2 --> Driver[Driver] Driver -- "Send Parameter" --> Send[Send Parameter] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

9.3.102 (DCh) RDID3: Read ID3

Command Set		RDID3									
Inst / Para	W/R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	HEX	
RDID3	R	1	1	0	1	1	1	0	0	DCh	
Parameter	1	DM_ID3[7:0]									

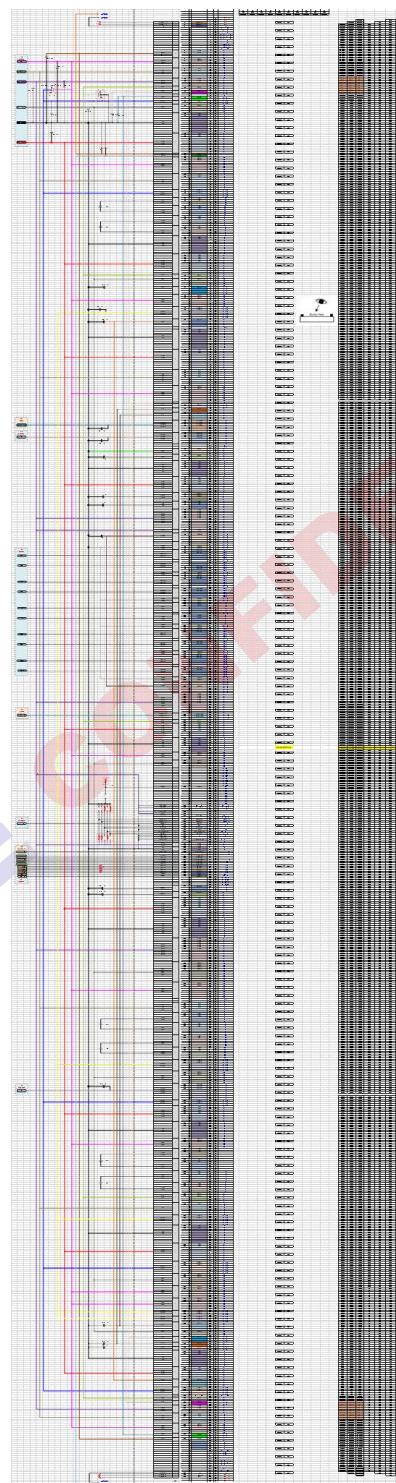
NOTE: “-”Don’t care.

Description	This read byte identifies the OLED module/driver. It is specified by end customer and for this display module project.													
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	OTP Value													
S/W Reset	OTP Value													
H/W Reset	OTP Value													
Flow Chart	 <pre> graph TD Host[Host] -- RDID3 --> Driver[Driver] Driver -- "Send Parameter" --> SendParam[/Send Parameter/] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

10. Appendix

10.1 Application Circuit

A typical application circuit is shown in following figure.



10.2 Configuration of External Components

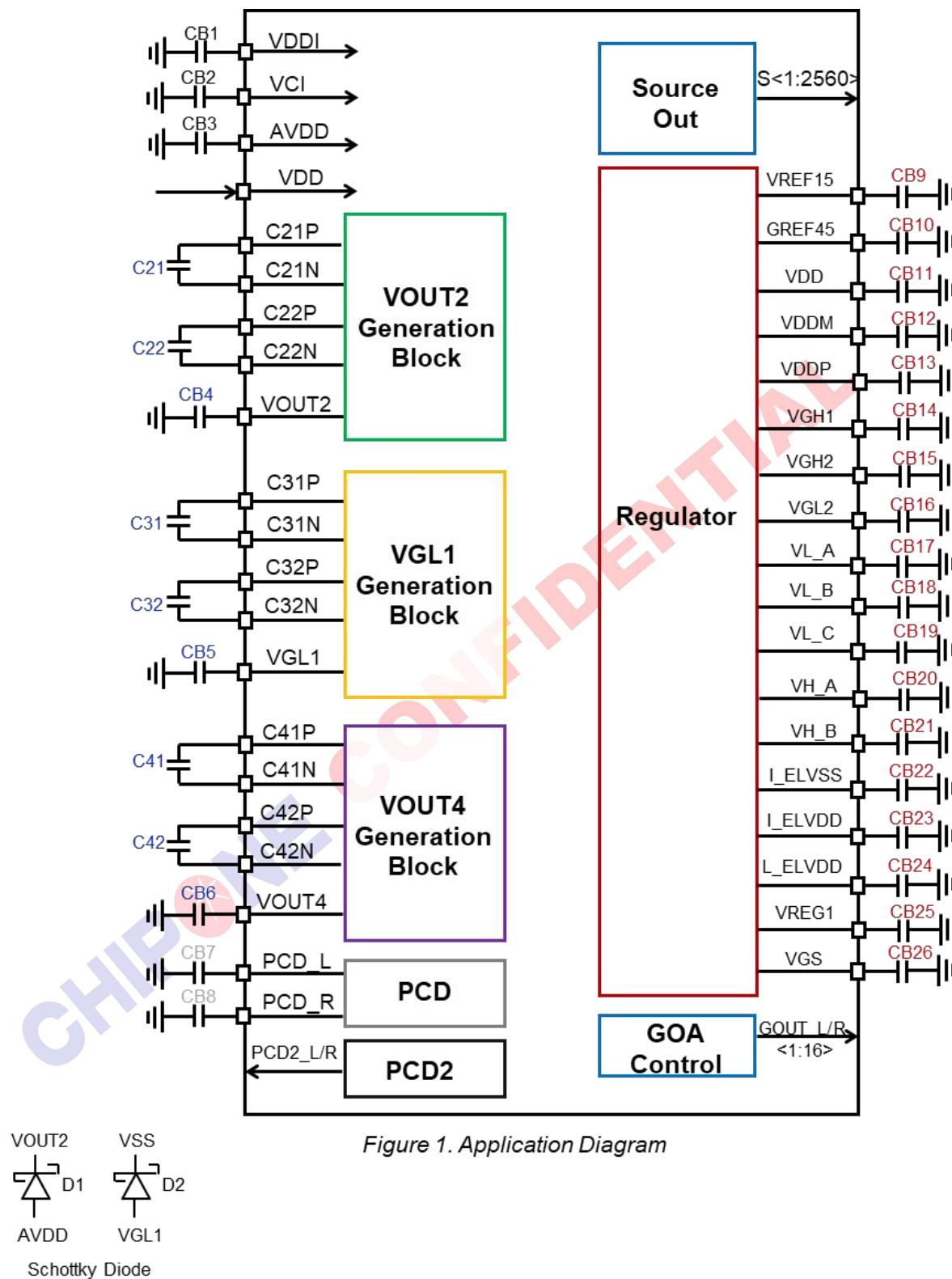


Figure 1. Application Diagram

10.3 Specifications of External Components

The following tables show the specifications of external element connected to the ICNA3512'S power Supply circuit. e position.

Table1 Capacitor

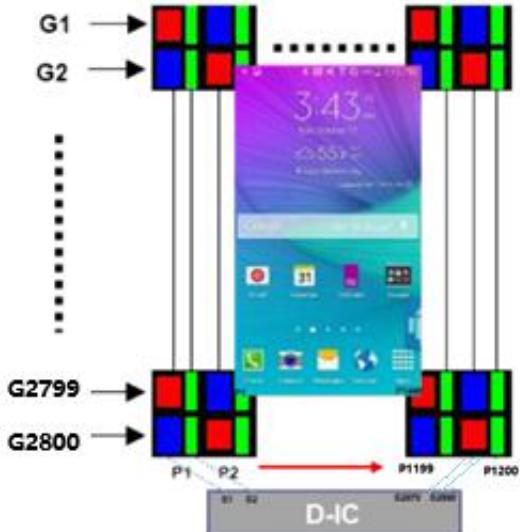
Component Number	Recommended Voltage	Capacity	Tolerance
CB7, CB8 (option)	6V	10.0nF	±10%
CB12, CB13	6V		
CB25, CB26	10V	1.0µF	±10%
C21, C22, C31, C32, C41, C42	25V		
CB9	6V		
CB6, CB10, CB17, CB18, CB19, CB20, CB21, CB22, CB23, CB24	10V	2.2µF	±10%
CB4, CB5, CB14, CB15, CB16	25V		
CB1, CB2, CB11	6V		
CB3	10V	4.7µF	±10%

Table2 of Schottky Diode

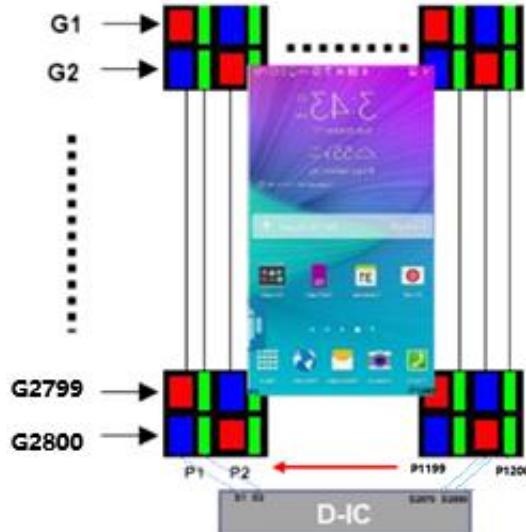
Component Number	Schottky Diode
D1, D2	VF < 0.4V / 100mA at 25°C, VR > 10V

10.4 Display Module Position

The position of an AMOLED panel with SPR is always at top as below. When MADCTL's (36h) parameter is 00h and the arrangement of sub pixel rendering is RGBG, the DDIC can support many kinds of connection between the DDIC's source outputs and AMOLED panel with SPR.



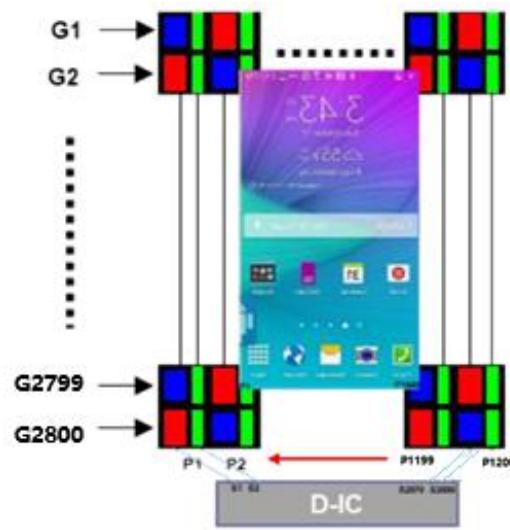
[Case 1]: SW_MODE = 00, SDIR = 0



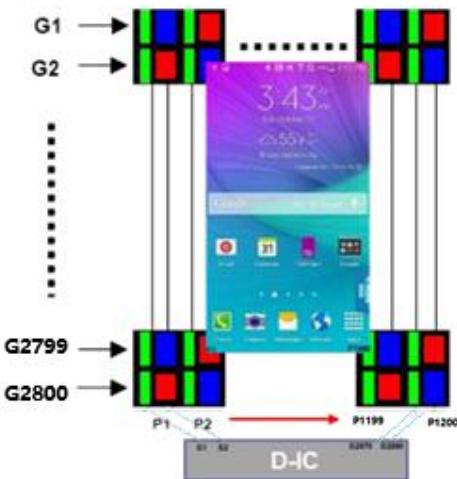
[Case 2]: SW_MODE = 00, SDIR = 1



[Case 3]: SW_MODE = 01, SDIR = 0



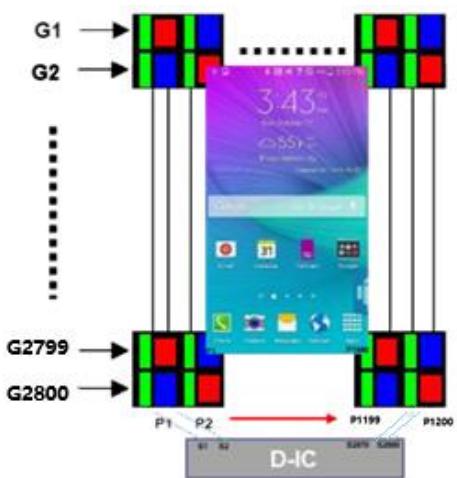
[Case 4]: SW_MODE = 01, SDIR = 1



[Case 5]: SW_MODE = 11, SDIR = 0



[Case 6]: SW_MODE = 11, SDIR = 1



[Case 7]: SW_MODE = 10, SDIR = 0



[Case 8]: SW_MODE = 10, SDIR = 1

10.5 Pad Coordinates

Pad List:

Pad no.	Pad Name	Center Coordinate	
		X	Y
1	DUMMY_L4	-16300.78	-622.5
2	DUMMY_L3	-16255.6875	-622.5
3	DUMMY_L3	-16210.595	-622.5
4	DUMMY_L3	-16165.505	-622.5
5	PCD2_L	-16120.4125	-622.5
6	VSSDUMMY	-16075.32	-622.5
7	VS_OUT	-16030.2275	-622.5
8	HS_OUT	-15985.135	-622.5
9	CASCADE3_OUT	-15940.045	-622.5
10	CASCADE2_OUT	-15894.9525	-622.5
11	CASCADE1_OUT	-15849.86	-622.5
12	CS_M	-15804.7675	-622.5
13	SCL_M	-15759.675	-622.5
14	SDATA1_M	-15714.5825	-622.5
15	SDATA0_M	-15669.4925	-622.5
16	VSSDUMMY	-15624.4	-622.5
17	VGH1	-15579.3075	-622.5
18	VGH1	-15534.215	-622.5
19	VGH1	-15489.1225	-622.5
20	VGH1	-15444.03	-622.5
21	AVDD	-15398.94	-622.5
22	AVDD	-15353.8475	-622.5
23	AVDD	-15308.755	-622.5
24	AVDD	-15263.6625	-622.5
25	AVDD	-15218.57	-622.5
26	VCI	-15173.4775	-622.5
27	VCI	-15128.3875	-622.5
28	VCI	-15083.295	-622.5
29	VCI	-15038.2025	-622.5
30	VCI	-14993.11	-622.5
31	VDDI	-14948.0175	-622.5
32	VDDI	-14902.9275	-622.5
33	VDDI	-14857.835	-622.5
34	VDDI	-14812.7425	-622.5

35	VGL1	-14767.65	-622.5
36	VGL1	-14722.5575	-622.5
37	VGL2	-14677.465	-622.5
38	VGL2	-14632.375	-622.5
39	TS1	-14587.2825	-622.5
40	VGH2	-14542.19	-622.5
41	VGH2	-14497.0975	-622.5
42	VOUT2	-14452.005	-622.5
43	VOUT2	-14406.9125	-622.5
44	AVSS	-14361.8225	-622.5
45	AVSS	-14316.73	-622.5
46	AVSS	-14271.6375	-622.5
47	AVSS	-14226.545	-622.5
48	VSS	-14181.4525	-622.5
49	VSS	-14136.3625	-622.5
50	VSS	-14091.27	-622.5
51	VSS	-14046.1775	-622.5
52	VSS	-14001.085	-622.5
53	VSS	-13955.9925	-622.5
54	VSS	-13910.9	-622.5
55	VSS	-13865.81	-622.5
56	VSS	-13820.7175	-622.5
57	VSS	-13775.625	-622.5
58	VDD	-13730.5325	-622.5
59	VDD	-13685.44	-622.5
60	VDD	-13640.3475	-622.5
61	VDD	-13595.2575	-622.5
62	VDD	-13550.165	-622.5
63	VDD	-13505.0725	-622.5
64	VDD	-13459.98	-622.5
65	VDD	-13414.8875	-622.5
66	VDD	-13369.7975	-622.5
67	VDD	-13324.705	-622.5
68	PCD_L	-13279.6125	-622.5
69	PCD_R	-13234.52	-622.5
70	AVDD	-13189.4275	-622.5
71	AVDD	-13144.335	-622.5

72	AVDD	-13099.245	-622.5		112	VSS	-11295.5625	-622.5
73	AVDD	-13054.1525	-622.5		113	VSS	-11250.47	-622.5
74	AVDD	-13009.06	-622.5		114	VSS	-11205.3775	-622.5
75	AVDD	-12963.9675	-622.5		115	VSS	-11160.285	-622.5
76	AVDD	-12918.875	-622.5		116	VSS	-11115.1925	-622.5
77	AVDD	-12873.7825	-622.5		117	VSS	-11070.1	-622.5
78	VCI	-12828.6925	-622.5		118	VDD	-11025.01	-622.5
79	VCI	-12783.6	-622.5		119	VDD	-10979.9175	-622.5
80	VCI	-12738.5075	-622.5		120	VDD	-10934.825	-622.5
81	VCI	-12693.415	-622.5		121	VDD	-10889.7325	-622.5
82	VCI	-12648.3225	-622.5		122	VDD	-10844.64	-622.5
83	VCI	-12603.23	-622.5		123	VDD	-10799.5475	-622.5
84	VCI	-12558.14	-622.5		124	VDD	-10754.4575	-622.5
85	VCI	-12513.0475	-622.5		125	VDD	-10709.365	-622.5
86	VOUT2	-12467.955	-622.5		126	VDD	-10664.2725	-622.5
87	VOUT2	-12422.8625	-622.5		127	VDD	-10619.18	-622.5
88	VOUT2	-12377.77	-622.5		128	VGL1	-10574.0875	-622.5
89	VOUT2	-12332.68	-622.5		129	VGL1	-10528.9975	-622.5
90	C22P	-12287.5875	-622.5		130	AVSS	-10483.905	-622.5
91	C22P	-12242.495	-622.5		131	AVSS	-10438.8125	-622.5
92	C22P	-12197.4025	-622.5		132	AVSS	-10393.72	-622.5
93	C22P	-12152.31	-622.5		133	AVSS	-10348.6275	-622.5
94	C22N	-12107.2175	-622.5		134	VH_A	-10303.535	-622.5
95	C22N	-12062.1275	-622.5		135	VH_A	-10258.445	-622.5
96	C22N	-12017.035	-622.5		136	VH_A	-10213.3525	-622.5
97	C22N	-11971.9425	-622.5		137	VH_A	-10168.26	-622.5
98	C22N	-11926.85	-622.5		138	AVDD	-10123.1675	-622.5
99	C21N	-11881.7575	-622.5		139	AVDD	-10078.075	-622.5
100	C21N	-11836.665	-622.5		140	AVDD	-10032.9825	-622.5
101	C21N	-11791.575	-622.5		141	AVDD	-9987.8925	-622.5
102	C21N	-11746.4825	-622.5		142	AVDD	-9942.8	-622.5
103	C21N	-11701.39	-622.5		143	AVDD	-9897.7075	-622.5
104	C21P	-11656.2975	-622.5		144	VOUT4	-9852.615	-622.5
105	C21P	-11611.205	-622.5		145	VOUT4	-9807.5225	-622.5
106	C21P	-11566.115	-622.5		146	VOUT4	-9762.4325	-622.5
107	C21P	-11521.0225	-622.5		147	VOUT4	-9717.34	-622.5
108	C21P	-11475.93	-622.5		148	VOUT4	-9672.2475	-622.5
109	VSS	-11430.8375	-622.5		149	VOUT4	-9627.155	-622.5
110	VSS	-11385.745	-622.5		150	VH_B	-9582.0625	-622.5
111	VSS	-11340.6525	-622.5		151	VH_B	-9536.97	-622.5

152	VH_B	-9491.88	-622.5
153	VH_B	-9446.7875	-622.5
154	TS2	-9401.695	-622.5
155	VSS	-9356.6025	-622.5
156	VSS	-9311.51	-622.5
157	VSS	-9266.4175	-622.5
158	VSS	-9221.3275	-622.5
159	VSS	-9176.235	-622.5
160	VSS	-9131.1425	-622.5
161	VSS	-9086.05	-622.5
162	VSS	-9040.9575	-622.5
163	VSS	-8995.8675	-622.5
164	VSS	-8950.775	-622.5
165	VDD	-8905.6825	-622.5
166	VDD	-8860.59	-622.5
167	VDD	-8815.4975	-622.5
168	VDD	-8770.405	-622.5
169	VDD	-8725.315	-622.5
170	VDD	-8680.2225	-622.5
171	VDD	-8635.13	-622.5
172	VDD	-8590.0375	-622.5
173	VDD	-8544.945	-622.5
174	VDD	-8499.8525	-622.5
175	VCI	-8454.7625	-622.5
176	VCI	-8409.67	-622.5
177	VCI	-8364.5775	-622.5
178	VCI	-8319.485	-622.5
179	VCI	-8274.3925	-622.5
180	VCI	-8229.3	-622.5
181	VCI	-8184.21	-622.5
182	VCI	-8139.1175	-622.5
183	AVDD	-8094.025	-622.5
184	AVDD	-8048.9325	-622.5
185	AVDD	-8003.84	-622.5
186	AVDD	-7958.75	-622.5
187	AVDD	-7913.6575	-622.5
188	AVDD	-7868.565	-622.5
189	AVDD	-7823.4725	-622.5
190	AVDD	-7778.38	-622.5
191	TS3	-7733.2875	-622.5
192	VL_A	-7688.1975	-622.5
193	VL_A	-7643.105	-622.5
194	VL_B	-7598.0125	-622.5
195	VL_B	-7552.92	-622.5
196	VL_C	-7507.8275	-622.5
197	VL_C	-7462.735	-622.5
198	VL_C	-7417.645	-622.5
199	VL_C	-7372.5525	-622.5
200	L_ELVDD	-7327.46	-622.5
201	L_ELVDD	-7282.3675	-622.5
202	L_ELVDD	-7237.275	-622.5
203	L_ELVDD	-7192.185	-622.5
204	L_ELVDD	-7147.0925	-622.5
205	L_ELVDD	-7102	-622.5
206	I_ELVDD	-7056.9075	-622.5
207	I_ELVDD	-7011.815	-622.5
208	I_ELVDD	-6966.7225	-622.5
209	I_ELVDD	-6921.6325	-622.5
210	I_ELVDD	-6876.54	-622.5
211	I_ELVDD	-6831.4475	-622.5
212	TS0	-6786.355	-622.5
213	TS4	-6741.2625	-622.5
214	VSSP	-6696.17	-622.5
215	VSSP	-6651.08	-622.5
216	VSSP	-6605.9875	-622.5
217	VDDP	-6560.895	-622.5
218	VDDP	-6515.8025	-622.5
219	VDDP	-6470.71	-622.5
220	VSS	-6425.62	-622.5
221	VSS	-6380.5275	-622.5
222	VSS	-6335.435	-622.5
223	VSS	-6290.3425	-622.5
224	VSS	-6245.25	-622.5
225	VSS	-6200.1575	-622.5
226	VSS	-6155.0675	-622.5
227	VSS	-6109.975	-622.5
228	VDD	-6064.8825	-622.5
229	VDD	-6019.79	-622.5
230	VDD	-5974.6975	-622.5
231	VDD	-5929.605	-622.5

232	VDD	-5884.5115	-622.5		272	DATA3N	-4080.8325	-622.5
233	VDD	-5839.4225	-622.5		273	DATA3N	-4035.74	-622.5
234	VDD	-5794.33	-622.5		274	DATA3N	-3990.6475	-622.5
235	VDD	-5749.2375	-622.5		275	VSSM	-3945.555	-622.5
236	VREG1	-5704.145	-622.5		276	VSSM	-3900.4625	-622.5
237	VREG1	-5659.0525	-622.5		277	DATAOP	-3855.3725	-622.5
238	VREG1	-5613.9625	-622.5		278	DATAOP	-3810.28	-622.5
239	VREG1	-5568.87	-622.5		279	DATAOP	-3765.1875	-622.5
240	VGS	-5523.7775	-622.5		280	DATAOP	-3720.095	-622.5
241	VGS	-5478.685	-622.5		281	DATAOP	-3675.0025	-622.5
242	VGS	-5433.5925	-622.5		282	VSSM	-3629.91	-622.5
243	VGS	-5388.5025	-622.5		283	DATA0N	-3584.82	-622.5
244	VDDI	-5343.41	-622.5		284	DATA0N	-3539.7275	-622.5
245	VDDI	-5298.3175	-622.5		285	DATA0N	-3494.635	-622.5
246	VDDI	-5253.225	-622.5		286	DATA0N	-3449.5425	-622.5
247	VDDI	-5208.1325	-622.5		287	DATA0N	-3404.45	-622.5
248	VDDI	-5163.04	-622.5		288	VSSM	-3359.3575	-622.5
249	VDDI	-5117.95	-622.5		289	VSSM	-3314.2675	-622.5
250	VDDI	-5072.8575	-622.5		290	CLKP	-3269.175	-622.5
251	VDDI	-5027.765	-622.5		291	CLKP	-3224.0825	-622.5
252	VDDI	-4982.6725	-622.5		292	CLKP	-3178.99	-622.5
253	VDDI	-4937.58	-622.5		293	CLKP	-3133.8975	-622.5
254	VDDI	-4892.4875	-622.5		294	CLKP	-3088.805	-622.5
255	VDDI	-4847.3975	-622.5		295	VSSM	-3043.715	-622.5
256	VDDM	-4802.305	-622.5		296	CLKN	-2998.6225	-622.5
257	VDDM	-4757.2125	-622.5		297	CLKN	-2953.53	-622.5
258	VDDM	-4712.12	-622.5		298	CLKN	-2908.4375	-622.5
259	VDDM	-4667.0275	-622.5		299	CLKN	-2863.345	-622.5
260	VSSM	-4621.9375	-622.5		300	CLKN	-2818.255	-622.5
261	VSSM	-4576.845	-622.5		301	VSSM	-2773.1625	-622.5
262	VSSM	-4531.7525	-622.5		302	VSSM	-2728.07	-622.5
263	VSSM	-4486.66	-622.5		303	DATA1P	-2682.9775	-622.5
264	DATA3P	-4441.5675	-622.5		304	DATA1P	-2637.885	-622.5
265	DATA3P	-4396.475	-622.5		305	DATA1P	-2592.7925	-622.5
266	DATA3P	-4351.385	-622.5		306	DATA1P	-2547.7025	-622.5
267	DATA3P	-4306.2925	-622.5		307	DATA1P	-2502.61	-622.5
268	DATA3P	-4261.2	-622.5		308	VSSM	-2457.5175	-622.5
269	VSSM	-4216.1075	-622.5		309	DATA1N	-2412.425	-622.5
270	DATA3N	-4171.015	-622.5		310	DATA1N	-2367.3325	-622.5
271	DATA3N	-4125.9225	-622.5		311	DATA1N	-2322.24	-622.5

312	DATA1N	-2277.15	-622.5		352	VDD	-473.4675	-622.5
313	DATA1N	-2232.0575	-622.5		353	VDD	-428.375	-622.5
314	VSSM	-2186.965	-622.5		354	VDD	-383.2825	-622.5
315	VSSM	-2141.8725	-622.5		355	VDD	-338.19	-622.5
316	DATA2P	-2096.78	-622.5		356	VDD	-293.0975	-622.5
317	DATA2P	-2051.69	-622.5		357	VSS	-248.0075	-622.5
318	DATA2P	-2006.5975	-622.5		358	VSS	-202.915	-622.5
319	DATA2P	-1961.505	-622.5		359	VSS	-157.8225	-622.5
320	DATA2P	-1916.4125	-622.5		360	VSS	-112.73	-622.5
321	VSSM	-1871.32	-622.5		361	VSS	-67.6375	-622.5
322	DATA2N	-1826.2275	-622.5		362	VSS	-22.545	-622.5
323	DATA2N	-1781.1375	-622.5		363	VSS	22.545	-622.5
324	DATA2N	-1736.045	-622.5		364	AVDD	67.6375	-622.5
325	DATA2N	-1690.9525	-622.5		365	AVDD	112.73	-622.5
326	DATA2N	-1645.86	-622.5		366	AVDD	157.8225	-622.5
327	VSSM	-1600.7675	-622.5		367	AVDD	202.915	-622.5
328	VSSM	-1555.675	-622.5		368	AVSS	248.0075	-622.5
329	VSSM	-1510.585	-622.5		369	AVSS	293.0975	-622.5
330	VSSM	-1465.4925	-622.5		370	AVSS	338.19	-622.5
331	VDDM	-1420.4	-622.5		371	AVSS	383.2825	-622.5
332	VDDM	-1375.3075	-622.5		372	VGMA1	428.375	-622.5
333	VDDM	-1330.215	-622.5		373	VGMA2	473.4675	-622.5
334	VDDM	-1285.125	-622.5		374	VGMA3	518.5575	-622.5
335	VDDI	-1240.0325	-622.5		375	VGMA4	563.65	-622.5
336	VDDI	-1194.94	-622.5		376	VGMA5	608.7425	-622.5
337	VDDI	-1149.8475	-622.5		377	VGMA6	653.835	-622.5
338	VDDI	-1104.755	-622.5		378	VGMA7	698.9275	-622.5
339	VDDI	-1059.6625	-622.5		379	VGMA8	744.02	-622.5
340	VDDI	-1014.5725	-622.5		380	VGMA9	789.11	-622.5
341	VDDI	-969.48	-622.5		381	PSWAP	834.2025	-622.5
342	VDDI	-924.3875	-622.5		382	DB<0>	879.295	-622.5
343	VDDI	-879.295	-622.5		383	DB<1>	924.3875	-622.5
344	VDDI	-834.2025	-622.5		384	DB<2>	969.48	-622.5
345	I_ELVDD_PVC	-789.11	-622.5		385	DB<3>	1014.5725	-622.5
346	I_ELVDD_PVC	-744.02	-622.5		386	DB<4>	1059.6625	-622.5
347	I_ELVDD_PVC	-698.9275	-622.5		387	DB<5>	1104.755	-622.5
348	VGL1	-653.835	-622.5		388	DB<6>	1149.8475	-622.5
349	VGL1	-608.7425	-622.5		389	DB<7>	1194.94	-622.5
350	VDD	-563.65	-622.5		390	TVS_RDX	1240.0325	-622.5
351	VDD	-518.5575	-622.5		391	THS_WRX	1285.125	-622.5

392	DCLK	1330.215	-622.5		432	GREF45	3133.8975	-622.5
393	DE_DnC	1375.3075	-622.5		433	VREF15	3178.99	-622.5
394	nCS	1420.4	-622.5		434	VREF15	3224.0825	-622.5
395	EXT_OSC	1465.4925	-622.5		435	VREF15	3269.175	-622.5
396	TEST<0>	1510.585	-622.5		436	VDD	3314.2675	-622.5
397	DSWAP<0>	1555.675	-622.5		437	VDD	3359.3575	-622.5
398	DSWAP<1>	1600.7675	-622.5		438	VDD	3404.45	-622.5
399	nRESET	1645.86	-622.5		439	VDD	3449.5425	-622.5
400	IM1	1690.9525	-622.5		440	VDD	3494.635	-622.5
401	CPHY_EN	1736.045	-622.5		441	VDD	3539.7275	-622.5
402	BTM	1781.1375	-622.5		442	VDD	3584.82	-622.5
403	EXT_DVDD_EN	1826.2275	-622.5		443	VDD	3629.91	-622.5
404	HZ_OPT	1871.32	-622.5		444	VDD	3675.0025	-622.5
405	BIST_EN	1916.4125	-622.5		445	VDD	3720.095	-622.5
406	FPS_EN	1961.505	-622.5		446	VSS	3765.1875	-622.5
407	CASCADE_EN	2006.5975	-622.5		447	VSS	3810.28	-622.5
408	M_S	2051.69	-622.5		448	VSS	3855.3725	-622.5
409	VDDI	2096.78	-622.5		449	VSS	3900.4625	-622.5
410	VDDI	2141.8725	-622.5		450	VSS	3945.555	-622.5
411	VSS	2186.965	-622.5		451	VSS	3990.6475	-622.5
412	VSS	2232.0575	-622.5		452	VSS	4035.74	-622.5
413	F_SPI_SCLK	2277.15	-622.5		453	VSS	4080.8325	-622.5
414	F_SPI_SCLK	2322.24	-622.5		454	VSS	4125.9225	-622.5
415	F_SPI_SI	2367.3325	-622.5		455	VSS	4171.015	-622.5
416	F_SPI_SO	2412.425	-622.5		456	VDDI	4216.1075	-622.5
417	F_SPI_RESET	2457.5175	-622.5		457	VDDI	4261.2	-622.5
418	F_SPI_WP	2502.61	-622.5		458	VDDI	4306.2925	-622.5
419	F_SPI_CS	2547.7025	-622.5		459	VDDI	4351.385	-622.5
420	GPO<0>	2592.7925	-622.5		460	VDDI	4396.475	-622.5
421	GPO<1>	2637.885	-622.5		461	VDDI	4441.5675	-622.5
422	GPO<2>	2682.9775	-622.5		462	VDDI	4486.66	-622.5
423	GPO<3>	2728.07	-622.5		463	VDDI	4531.7525	-622.5
424	SWIRE	2773.1625	-622.5		464	VDDI	4576.845	-622.5
425	SWIRE2	2818.255	-622.5		465	VDDI	4621.9375	-622.5
426	TEST<1>	2863.345	-622.5		466	VDDI	4667.0275	-622.5
427	TEST<2>	2908.4375	-622.5		467	VDDI	4712.12	-622.5
428	TEST<3>	2953.53	-622.5		468	AVSS	4757.2125	-622.5
429	TEST<4>	2998.6225	-622.5		469	AVSS	4802.305	-622.5
430	GREF45	3043.715	-622.5		470	AVSS	4847.3975	-622.5
431	GREF45	3088.805	-622.5		471	AVSS	4892.4875	-622.5

472	AVSS	4937.58	-622.5		512	C42N	6741.2625	-622.5
473	AVSS	4982.6725	-622.5		513	C42N	6786.355	-622.5
474	AVSS	5027.765	-622.5		514	C42N	6831.4475	-622.5
475	AVSS	5072.8575	-622.5		515	C42N	6876.54	-622.5
476	AVSS	5117.95	-622.5		516	VOUT4	6921.6325	-622.5
477	AVSS	5163.04	-622.5		517	VOUT4	6966.7225	-622.5
478	AVDD	5208.1325	-622.5		518	VOUT4	7011.815	-622.5
479	AVDD	5253.225	-622.5		519	VOUT4	7056.9075	-622.5
480	AVDD	5298.3175	-622.5		520	VOUT4	7102	-622.5
481	AVDD	5343.41	-622.5		521	VOUT4	7147.0925	-622.5
482	AVDD	5388.5025	-622.5		522	AVSS	7192.185	-622.5
483	AVDD	5433.5925	-622.5		523	AVSS	7237.275	-622.5
484	AVDD	5478.685	-622.5		524	AVSS	7282.3675	-622.5
485	AVDD	5523.7775	-622.5		525	AVSS	7327.46	-622.5
486	TS7	5568.87	-622.5		526	AVSS	7372.5525	-622.5
487	TS5	5613.9625	-622.5		527	AVSS	7417.645	-622.5
488	VCI	5659.0525	-622.5		528	I_ELVSS	7462.735	-622.5
489	VCI	5704.145	-622.5		529	I_ELVSS	7507.8275	-622.5
490	VCI	5749.2375	-622.5		530	I_ELVSS	7552.92	-622.5
491	VCI	5794.33	-622.5		531	I_ELVSS	7598.0125	-622.5
492	VCI	5839.4225	-622.5		532	I_ELVSS	7643.105	-622.5
493	C41N	5884.515	-622.5		533	I_ELVSS	7688.1975	-622.5
494	C41N	5929.605	-622.5		534	I_ELVSS	7733.2875	-622.5
495	C41N	5974.6975	-622.5		535	I_ELVSS	7778.38	-622.5
496	C41N	6019.79	-622.5		536	VOUT2	7823.4725	-622.5
497	C41N	6064.8825	-622.5		537	VOUT2	7868.565	-622.5
498	C41P	6109.975	-622.5		538	VOUT2	7913.6575	-622.5
499	C41P	6155.0675	-622.5		539	VDD	7958.75	-622.5
500	C41P	6200.1575	-622.5		540	VDD	8003.84	-622.5
501	C41P	6245.25	-622.5		541	VDD	8048.9325	-622.5
502	C41P	6290.3425	-622.5		542	VDD	8094.025	-622.5
503	C41P	6335.435	-622.5		543	VDD	8139.1175	-622.5
504	C42P	6380.5275	-622.5		544	VDD	8184.21	-622.5
505	C42P	6425.62	-622.5		545	VDD	8229.3	-622.5
506	C42P	6470.71	-622.5		546	VDD	8274.3925	-622.5
507	C42P	6515.8025	-622.5		547	VSS	8319.485	-622.5
508	C42P	6560.895	-622.5		548	VSS	8364.5775	-622.5
509	C42P	6605.9875	-622.5		549	VSS	8409.67	-622.5
510	C42N	6651.08	-622.5		550	VSS	8454.7625	-622.5
511	C42N	6696.17	-622.5		551	VSS	8499.8525	-622.5

552	VSS	8544.945	-622.5		592	VCI	10348.6275	-622.5
553	VSS	8590.0375	-622.5		593	VOUT4	10393.72	-622.5
554	VSS	8635.13	-622.5		594	VOUT4	10438.8125	-622.5
555	AVDD	8680.2225	-622.5		595	VOUT4	10483.905	-622.5
556	AVDD	8725.315	-622.5		596	VOUT4	10528.9975	-622.5
557	AVDD	8770.405	-622.5		597	VOUT4	10574.0875	-622.5
558	AVDD	8815.4975	-622.5		598	VSS	10619.18	-622.5
559	AVDD	8860.59	-622.5		599	VSS	10664.2725	-622.5
560	C31N	8905.6825	-622.5		600	VSS	10709.365	-622.5
561	C31N	8950.775	-622.5		601	VSS	10754.4575	-622.5
562	C31N	8995.8675	-622.5		602	VSS	10799.5475	-622.5
563	C31N	9040.9575	-622.5		603	VSS	10844.64	-622.5
564	C31N	9086.05	-622.5		604	VSS	10889.7325	-622.5
565	C31P	9131.1425	-622.5		605	VSS	10934.825	-622.5
566	C31P	9176.235	-622.5		606	VSS	10979.9175	-622.5
567	C31P	9221.3275	-622.5		607	VDD	11025.01	-622.5
568	C31P	9266.4175	-622.5		608	VDD	11070.1	-622.5
569	C31P	9311.51	-622.5		609	VDD	11115.1925	-622.5
570	C31P	9356.6025	-622.5		610	VDD	11160.285	-622.5
571	C32P	9401.695	-622.5		611	VDD	11205.3775	-622.5
572	C32P	9446.7875	-622.5		612	VDD	11250.47	-622.5
573	C32P	9491.88	-622.5		613	VDD	11295.5625	-622.5
574	C32P	9536.97	-622.5		614	VDD	11340.6525	-622.5
575	C32P	9582.0625	-622.5		615	VDD	11385.745	-622.5
576	C32P	9627.155	-622.5		616	VOUT2	11430.8375	-622.5
577	C32N	9672.2475	-622.5		617	VOUT2	11475.93	-622.5
578	C32N	9717.34	-622.5		618	VOUT2	11521.0225	-622.5
579	C32N	9762.4325	-622.5		619	VOUT2	11566.115	-622.5
580	C32N	9807.5225	-622.5		620	VOUT2	11611.205	-622.5
581	C32N	9852.615	-622.5		621	VOUT2	11656.2975	-622.5
582	VGL1	9897.7075	-622.5		622	AVSS	11701.39	-622.5
583	VGL1	9942.8	-622.5		623	AVSS	11746.4825	-622.5
584	VGL1	9987.8925	-622.5		624	AVSS	11791.575	-622.5
585	VGL1	10032.9825	-622.5		625	AVSS	11836.665	-622.5
586	VGL1	10078.075	-622.5		626	AVSS	11881.7575	-622.5
587	VCI	10123.1675	-622.5		627	AVSS	11926.85	-622.5
588	VCI	10168.26	-622.5		628	AVDD	11971.9425	-622.5
589	VCI	10213.3525	-622.5		629	AVDD	12017.035	-622.5
590	VCI	10258.445	-622.5		630	AVDD	12062.1275	-622.5
591	VCI	10303.535	-622.5		631	AVDD	12107.2175	-622.5

632	AVDD	12152.31	-622.5		672	VDD	13955.9925	-622.5
633	AVDD	12197.4025	-622.5		673	VDD	14001.085	-622.5
634	AVDD	12242.495	-622.5		674	VH_B	14046.1775	-622.5
635	AVDD	12287.5875	-622.5		675	VH_B	14091.27	-622.5
636	AVDD	12332.68	-622.5		676	VH_B	14136.3625	-622.5
637	AVDD	12377.77	-622.5		677	VH_B	14181.4525	-622.5
638	AVDD	12422.8625	-622.5		678	VOUT2	14226.545	-622.5
639	AVDD	12467.955	-622.5		679	VOUT2	14271.6375	-622.5
640	VOUT4	12513.0475	-622.5		680	VOUT2	14316.73	-622.5
641	VOUT4	12558.14	-622.5		681	VOUT2	14361.8225	-622.5
642	VOUT4	12603.23	-622.5		682	VSSDUMMY	14406.9125	-622.5
643	VOUT4	12648.3225	-622.5		683	VGL1	14452.005	-622.5
644	VOUT4	12693.415	-622.5		684	VGL1	14497.0975	-622.5
645	VOUT4	12738.5075	-622.5		685	VGL2	14542.19	-622.5
646	VL_C	12783.6	-622.5		686	VGL2	14587.2825	-622.5
647	VL_C	12828.6925	-622.5		687	VDDI	14632.375	-622.5
648	VL_C	12873.7825	-622.5		688	VDDI	14677.465	-622.5
649	VL_C	12918.875	-622.5		689	VDDI	14722.5575	-622.5
650	AVSS	12963.9675	-622.5		690	VDDI	14767.65	-622.5
651	AVSS	13009.06	-622.5		691	VCI	14812.7425	-622.5
652	AVSS	13054.1525	-622.5		692	VCI	14857.835	-622.5
653	VH_A	13099.245	-622.5		693	VCI	14902.9275	-622.5
654	VH_A	13144.335	-622.5		694	VCI	14948.0175	-622.5
655	VH_A	13189.4275	-622.5		695	VCI	14993.11	-622.5
656	VL_B	13234.52	-622.5		696	AVDD	15038.2025	-622.5
657	VL_B	13279.6125	-622.5		697	AVDD	15083.295	-622.5
658	VL_A	13324.705	-622.5		698	AVDD	15128.3875	-622.5
659	VL_A	13369.7975	-622.5		699	AVDD	15173.4775	-622.5
660	VSS	13414.8875	-622.5		700	AVDD	15218.57	-622.5
661	VSS	13459.98	-622.5		701	VGH2	15263.6625	-622.5
662	VSS	13505.0725	-622.5		702	VGH2	15308.755	-622.5
663	VSS	13550.165	-622.5		703	VGH1	15353.8475	-622.5
664	VSS	13595.2575	-622.5		704	VGH1	15398.94	-622.5
665	VSS	13640.3475	-622.5		705	VPP	15444.03	-622.5
666	VSS	13685.44	-622.5		706	VPP	15489.1225	-622.5
667	VSS	13730.5325	-622.5		707	VPP	15534.215	-622.5
668	VDD	13775.625	-622.5		708	VPP	15579.3075	-622.5
669	VDD	13820.7175	-622.5		709	VSSDUMMY	15624.4	-622.5
670	VDD	13865.81	-622.5		710	SDATA0_S	15669.4925	-622.5
671	VDD	13910.9	-622.5		711	SDATA1_S	15714.5825	-622.5

712	SCL_S	15759.675	-622.5
713	CS_S	15804.7675	-622.5
714	CASCADE1_IN	15849.86	-622.5
715	CASCADE2_IN	15894.9525	-622.5
716	CASCADE3_IN	15940.045	-622.5
717	HS_IN	15985.135	-622.5
718	VS_IN	16030.2275	-622.5
719	VSSDUMMY	16075.32	-622.5
720	PCD2_R	16120.4125	-622.5
721	DUMMY_R2	16165.505	-622.5
722	DUMMY_R2	16210.595	-622.5
723	DUMMY_R2	16255.6875	-622.5
724	DUMMY_R1	16300.78	-622.5
725	DUMMYO_R1	16246.285	647.5
726	VSSDUMMY	16277.4525	487.5
727	DUMMYO_R1	16213.0275	647.5
728	VSSDUMMY	16308.355	327.5
729	VSSDUMMY	16244.06	487.5
730	DUMMYO_R1	16179.77	647.5
731	VSSDUMMY	16274.8325	327.5
732	VSSDUMMY	16210.6725	487.5
733	DUMMYO_R2	16146.5125	647.5
734	VSSDUMMY	16241.31	327.5
735	VSSDUMMY	16177.285	487.5
736	VSSDUMMY	16113.255	647.5
737	GOUT1_R	16207.7875	327.5
738	GOUT1_R	16143.8925	487.5
739	GOUT1_R	16079.9975	647.5
740	GOUT2_R	16174.265	327.5
741	GOUT2_R	16110.505	487.5
742	GOUT2_R	16046.74	647.5
743	GOUT3_R	16140.7475	327.5
744	GOUT3_R	16077.1125	487.5
745	GOUT3_R	16013.4825	647.5
746	GOUT4_R	16107.225	327.5
747	GOUT4_R	16043.725	487.5
748	GOUT4_R	15980.225	647.5
749	GOUT5_R	16073.7025	327.5
750	GOUT5_R	16010.3325	487.5
751	GOUT5_R	15946.9675	647.5

752	GOUT6_R	16040.18	327.5
753	GOUT6_R	15976.945	487.5
754	GOUT6_R	15913.71	647.5
755	GOUT7_R	16006.6575	327.5
756	GOUT7_R	15943.5575	487.5
757	GOUT7_R	15880.4525	647.5
758	GOUT8_R	15973.135	327.5
759	GOUT8_R	15910.165	487.5
760	GOUT8_R	15847.195	647.5
761	GOUT9_R	15939.6125	327.5
762	GOUT9_R	15876.7775	487.5
763	GOUT9_R	15813.9375	647.5
764	GOUT10_R	15906.095	327.5
765	GOUT10_R	15843.385	487.5
766	GOUT10_R	15780.68	647.5
767	GOUT11_R	15872.5725	327.5
768	GOUT11_R	15809.9975	487.5
769	GOUT11_R	15747.4225	647.5
770	GOUT12_R	15839.05	327.5
771	GOUT12_R	15776.605	487.5
772	GOUT12_R	15714.165	647.5
773	GOUT13_R	15805.5275	327.5
774	GOUT13_R	15743.2175	487.5
775	GOUT13_R	15680.9075	647.5
776	GOUT14_R	15772.005	327.5
777	GOUT14_R	15709.83	487.5
778	GOUT14_R	15647.65	647.5
779	GOUT15_R	15738.4825	327.5
780	GOUT15_R	15676.4375	487.5
781	GOUT15_R	15614.3925	647.5
782	GOUT16_R	15704.96	327.5
783	GOUT16_R	15643.05	487.5
784	GOUT16_R	15581.135	647.5
785	VSSDUMMY	15671.4425	327.5
786	VSSDUMMY	15609.6575	487.5
787	VSSDUMMY	15547.8775	647.5
788	VSSDUMMY	15637.92	327.5
789	VSSDUMMY	15576.27	487.5
790	VSSDUMMY	15514.62	647.5
791	VSSDUMMY	15604.3975	327.5

792	VSSDUMMY	15542.8775	487.5
793	VSSDUMMY	15481.3625	647.5
794	VSSDUMMY	15570.875	327.5
795	VSSDUMMY	15509.49	487.5
796	VSSDUMMY	15448.105	647.5
797	VSSDUMMY	15537.3525	327.5
798	VSSDUMMY	15476.1025	487.5
799	VSSDUMMY	15414.8475	647.5
800	VSSDUMMY	15503.83	327.5
801	VSSDUMMY	15442.71	487.5
802	VSSDUMMY	15381.59	647.5
803	VSSDUMMY	15470.3075	327.5
804	VSSDUMMY	15409.3225	487.5
805	VSSDUMMY	15348.3325	647.5
806	VINIT_B_R	15436.7875	327.5
807	VINIT_B_R	15375.93	487.5
808	VINIT_B_R	15315.075	647.5
809	VINIT_B_R	15403.2675	327.5
810	VINIT_B_R	15342.5425	487.5
811	VINIT_B_R	15281.8175	647.5
812	VINIT_B_R	15369.745	327.5
813	VINIT_B_R	15309.15	487.5
814	VINIT_B_R	15248.56	647.5
815	VINIT_C_R	15336.2225	327.5
816	VINIT_C_R	15275.7625	487.5
817	VINIT_C_R	15215.3025	647.5
818	VINIT_C_R	15302.7	327.5
819	VINIT_C_R	15242.375	487.5
820	VINIT_C_R	15182.045	647.5
821	VINIT_C_R	15269.1775	327.5
822	VINIT_C_R	15208.9825	487.5
823	VINIT_C_R	15148.7875	647.5
824	VINIT_A_R	15235.655	327.5
825	VINIT_A_R	15175.595	487.5
826	VINIT_A_R	15115.53	647.5
827	VINIT_A_R	15202.135	327.5
828	VINIT_A_R	15142.2025	487.5
829	VINIT_A_R	15082.2725	647.5
830	VINIT_A_R	15168.615	327.5
831	VINIT_A_R	15108.815	487.5

832	VINIT_A_R	15049.015	647.5
833	VSSDUMMY	15135.0925	327.5
834	VSSDUMMY	15075.4225	487.5
835	VSSDUMMY	15015.7575	647.5
836	VSSDUMMY	15101.57	327.5
837	VSSDUMMY	15042.035	487.5
838	VSSDUMMY	14982.5	647.5
839	VSSDUMMY	15068.0475	327.5
840	VSSDUMMY	15008.6475	487.5
841	S_R_TEST	14949.2425	647.5
842	S<1>	15034.525	327.5
843	S<2>	14975.255	487.5
844	S<3>	14915.985	647.5
845	S<4>	15001.0025	327.5
846	S<5>	14941.8675	487.5
847	S<6>	14882.7275	647.5
848	S<7>	14967.4825	327.5
849	S<8>	14908.475	487.5
850	S<9>	14849.47	647.5
851	S<10>	14933.9625	327.5
852	S<11>	14875.0875	487.5
853	S<12>	14816.2125	647.5
854	S<13>	14900.44	327.5
855	S<14>	14841.695	487.5
856	S<15>	14782.955	647.5
857	S<16>	14866.9175	327.5
858	S<17>	14808.3075	487.5
859	S<18>	14749.6975	647.5
860	S<19>	14833.395	327.5
861	S<20>	14774.9175	487.5
862	S<21>	14716.44	647.5
863	S<22>	14799.8725	327.5
864	S<23>	14741.5275	487.5
865	S<24>	14683.1825	647.5
866	S<25>	14766.35	327.5
867	S<26>	14708.14	487.5
868	S<27>	14649.925	647.5
869	S<28>	14732.83	327.5
870	S<29>	14674.7475	487.5
871	S<30>	14616.6675	647.5

872	S<31>	14699.31	327.5
873	S<32>	14641.36	487.5
874	S<33>	14583.41	647.5
875	S<34>	14665.7875	327.5
876	S<35>	14607.97	487.5
877	S<36>	14550.1525	647.5
878	S<37>	14632.265	327.5
879	S<38>	14574.58	487.5
880	S<39>	14516.895	647.5
881	S<40>	14598.7425	327.5
882	S<41>	14541.19	487.5
883	S<42>	14483.6375	647.5
884	S<43>	14565.22	327.5
885	S<44>	14507.8	487.5
886	S<45>	14450.38	647.5
887	S<46>	14531.6975	327.5
888	S<47>	14474.4125	487.5
889	S<48>	14417.1225	647.5
890	S<49>	14498.1775	327.5
891	S<50>	14441.02	487.5
892	S<51>	14383.865	647.5
893	S<52>	14464.6575	327.5
894	S<53>	14407.6325	487.5
895	S<54>	14350.6075	647.5
896	S<55>	14431.135	327.5
897	S<56>	14374.2425	487.5
898	S<57>	14317.35	647.5
899	S<58>	14397.6125	327.5
900	S<59>	14340.8525	487.5
901	S<60>	14284.0925	647.5
902	S<61>	14364.09	327.5
903	S<62>	14307.4625	487.5
904	S<63>	14250.835	647.5
905	S<64>	14330.5675	327.5
906	S<65>	14274.0725	487.5
907	S<66>	14217.5775	647.5
908	S<67>	14297.045	327.5
909	S<68>	14240.685	487.5
910	S<69>	14184.32	647.5
911	S<70>	14263.525	327.5

912	S<71>	14207.2925	487.5
913	S<72>	14151.0625	647.5
914	S<73>	14230.0025	327.5
915	S<74>	14173.905	487.5
916	S<75>	14117.805	647.5
917	S<76>	14196.4825	327.5
918	S<77>	14140.515	487.5
919	S<78>	14084.5475	647.5
920	S<79>	14162.96	327.5
921	S<80>	14107.125	487.5
922	S<81>	14051.29	647.5
923	S<82>	14129.4375	327.5
924	S<83>	14073.735	487.5
925	S<84>	14018.0325	647.5
926	S<85>	14095.915	327.5
927	S<86>	14040.345	487.5
928	S<87>	13984.775	647.5
929	S<88>	14062.3925	327.5
930	S<89>	14006.9575	487.5
931	S<90>	13951.5175	647.5
932	S<91>	14028.8725	327.5
933	S<92>	13973.565	487.5
934	S<93>	13918.26	647.5
935	S<94>	13995.35	327.5
936	S<95>	13940.1775	487.5
937	S<96>	13885.0025	647.5
938	S<97>	13961.83	327.5
939	S<98>	13906.7875	487.5
940	S<99>	13851.745	647.5
941	S<100>	13928.3075	327.5
942	S<101>	13873.3975	487.5
943	S<102>	13818.4875	647.5
944	S<103>	13894.785	327.5
945	S<104>	13840.0075	487.5
946	S<105>	13785.23	647.5
947	S<106>	13861.2625	327.5
948	S<107>	13806.6175	487.5
949	S<108>	13751.9725	647.5
950	S<109>	13827.74	327.5
951	S<110>	13773.23	487.5

952	S<111>	13718.715	647.5
953	S<112>	13794.22	327.5
954	S<113>	13739.8375	487.5
955	S<114>	13685.4575	647.5
956	S<115>	13760.6975	327.5
957	S<116>	13706.45	487.5
958	S<117>	13652.2	647.5
959	S<118>	13727.1775	327.5
960	S<119>	13673.06	487.5
961	S<120>	13618.9425	647.5
962	S<121>	13693.655	327.5
963	S<122>	13639.67	487.5
964	S<123>	13585.685	647.5
965	S<124>	13660.1325	327.5
966	S<125>	13606.28	487.5
967	S<126>	13552.4275	647.5
968	S<127>	13626.61	327.5
969	S<128>	13572.89	487.5
970	S<129>	13519.17	647.5
971	S<130>	13593.0875	327.5
972	S<131>	13539.5025	487.5
973	S<132>	13485.9125	647.5
974	S<133>	13559.5675	327.5
975	S<134>	13506.11	487.5
976	S<135>	13452.655	647.5
977	S<136>	13526.045	327.5
978	S<137>	13472.7225	487.5
979	S<138>	13419.3975	647.5
980	S<139>	13492.525	327.5
981	S<140>	13439.3325	487.5
982	S<141>	13386.14	647.5
983	S<142>	13459.0025	327.5
984	S<143>	13405.9425	487.5
985	S<144>	13352.8825	647.5
986	S<145>	13425.48	327.5
987	S<146>	13372.5525	487.5
988	S<147>	13319.625	647.5
989	S<148>	13391.9575	327.5
990	S<149>	13339.1625	487.5
991	S<150>	13286.3675	647.5

992	S<151>	13358.435	327.5
993	S<152>	13305.775	487.5
994	S<153>	13253.11	647.5
995	S<154>	13324.915	327.5
996	S<155>	13272.3825	487.5
997	S<156>	13219.8525	647.5
998	S<157>	13291.3925	327.5
999	S<158>	13238.995	487.5
1000	S<159>	13186.595	647.5
1001	S<160>	13257.8725	327.5
1002	S<161>	13205.605	487.5
1003	S<162>	13153.3375	647.5
1004	S<163>	13224.35	327.5
1005	S<164>	13172.215	487.5
1006	S<165>	13120.08	647.5
1007	S<166>	13190.8275	327.5
1008	S<167>	13138.825	487.5
1009	S<168>	13086.8225	647.5
1010	S<169>	13157.305	327.5
1011	S<170>	13105.435	487.5
1012	S<171>	13053.565	647.5
1013	S<172>	13123.7825	327.5
1014	S<173>	13072.0475	487.5
1015	S<174>	13020.3075	647.5
1016	S<175>	13090.2625	327.5
1017	S<176>	13038.655	487.5
1018	S<177>	12987.05	647.5
1019	S<178>	13056.74	327.5
1020	S<179>	13005.2675	487.5
1021	S<180>	12953.7925	647.5
1022	S<181>	13023.22	327.5
1023	S<182>	12971.8775	487.5
1024	S<183>	12920.535	647.5
1025	S<184>	12989.6975	327.5
1026	S<185>	12938.4875	487.5
1027	S<186>	12887.2775	647.5
1028	S<187>	12956.175	327.5
1029	S<188>	12905.0975	487.5
1030	S<189>	12854.02	647.5
1031	S<190>	12922.6525	327.5

1032	S<191>	12871.7075	487.5
1033	S<192>	12820.7625	647.5
1034	S<193>	12889.13	327.5
1035	S<194>	12838.32	487.5
1036	S<195>	12787.505	647.5
1037	S<196>	12855.61	327.5
1038	S<197>	12804.9275	487.5
1039	S<198>	12754.2475	647.5
1040	S<199>	12822.0875	327.5
1041	S<200>	12771.54	487.5
1042	S<201>	12720.99	647.5
1043	S<202>	12788.565	327.5
1044	S<203>	12738.15	487.5
1045	S<204>	12687.7325	647.5
1046	S<205>	12755.045	327.5
1047	S<206>	12704.76	487.5
1048	S<207>	12654.475	647.5
1049	S<208>	12721.5225	327.5
1050	S<209>	12671.37	487.5
1051	S<210>	12621.2175	647.5
1052	S<211>	12688	327.5
1053	S<212>	12637.98	487.5
1054	S<213>	12587.96	647.5
1055	S<214>	12654.4775	327.5
1056	S<215>	12604.5925	487.5
1057	S<216>	12554.7025	647.5
1058	S<217>	12620.9575	327.5
1059	S<218>	12571.2	487.5
1060	S<219>	12521.445	647.5
1061	S<220>	12587.435	327.5
1062	S<221>	12537.8125	487.5
1063	S<222>	12488.1875	647.5
1064	S<223>	12553.9125	327.5
1065	S<224>	12504.4225	487.5
1066	S<225>	12454.93	647.5
1067	S<226>	12520.3925	327.5
1068	S<227>	12471.0325	487.5
1069	S<228>	12421.6725	647.5
1070	S<229>	12486.87	327.5
1071	S<230>	12437.6425	487.5

1072	S<231>	12388.415	647.5
1073	S<232>	12453.3475	327.5
1074	S<233>	12404.2525	487.5
1075	S<234>	12355.1575	647.5
1076	S<235>	12419.825	327.5
1077	S<236>	12370.865	487.5
1078	S<237>	12321.9	647.5
1079	S<238>	12386.305	327.5
1080	S<239>	12337.4725	487.5
1081	S<240>	12288.6425	647.5
1082	S<241>	12352.7825	327.5
1083	S<242>	12304.085	487.5
1084	S<243>	12255.385	647.5
1085	S<244>	12319.26	327.5
1086	S<245>	12270.695	487.5
1087	S<246>	12222.1275	647.5
1088	S<247>	12285.74	327.5
1089	S<248>	12237.305	487.5
1090	S<249>	12188.87	647.5
1091	S<250>	12252.2175	327.5
1092	S<251>	12203.915	487.5
1093	S<252>	12155.6125	647.5
1094	S<253>	12218.695	327.5
1095	S<254>	12170.525	487.5
1096	S<255>	12122.355	647.5
1097	S<256>	12185.1725	327.5
1098	S<257>	12137.135	487.5
1099	S<258>	12089.0975	647.5
1100	S<259>	12151.6525	327.5
1101	S<260>	12103.745	487.5
1102	S<261>	12055.84	647.5
1103	S<262>	12118.13	327.5
1104	S<263>	12070.3575	487.5
1105	S<264>	12022.5825	647.5
1106	S<265>	12084.6075	327.5
1107	S<266>	12036.9675	487.5
1108	S<267>	11989.325	647.5
1109	S<268>	12051.0875	327.5
1110	S<269>	12003.5775	487.5
1111	S<270>	11956.0675	647.5

1112	S<271>	12017.565	327.5
1113	S<272>	11970.1875	487.5
1114	S<273>	11922.81	647.5
1115	S<274>	11984.0425	327.5
1116	S<275>	11936.7975	487.5
1117	S<276>	11889.5525	647.5
1118	S<277>	11950.52	327.5
1119	S<278>	11903.4075	487.5
1120	S<279>	11856.295	647.5
1121	S<280>	11916.9975	327.5
1122	S<281>	11870.0175	487.5
1123	S<282>	11823.0375	647.5
1124	S<283>	11883.4775	327.5
1125	S<284>	11836.63	487.5
1126	S<285>	11789.78	647.5
1127	S<286>	11849.955	327.5
1128	S<287>	11803.24	487.5
1129	S<288>	11756.5225	647.5
1130	S<289>	11816.435	327.5
1131	S<290>	11769.85	487.5
1132	S<291>	11723.265	647.5
1133	S<292>	11782.9125	327.5
1134	S<293>	11736.46	487.5
1135	S<294>	11690.0075	647.5
1136	S<295>	11749.39	327.5
1137	S<296>	11703.07	487.5
1138	S<297>	11656.75	647.5
1139	S<298>	11715.8675	327.5
1140	S<299>	11669.68	487.5
1141	S<300>	11623.4925	647.5
1142	S<301>	11682.345	327.5
1143	S<302>	11636.29	487.5
1144	S<303>	11590.235	647.5
1145	S<304>	11648.825	327.5
1146	S<305>	11602.9025	487.5
1147	S<306>	11556.9775	647.5
1148	S<307>	11615.3025	327.5
1149	S<308>	11569.5125	487.5
1150	S<309>	11523.72	647.5
1151	S<310>	11581.78	327.5

1152	S<311>	11536.1225	487.5
1153	S<312>	11490.4625	647.5
1154	S<313>	11548.26	327.5
1155	S<314>	11502.7325	487.5
1156	S<315>	11457.205	647.5
1157	S<316>	11514.7375	327.5
1158	S<317>	11469.3425	487.5
1159	S<318>	11423.9475	647.5
1160	S<319>	11481.215	327.5
1161	S<320>	11435.9525	487.5
1162	S<321>	11390.69	647.5
1163	S<322>	11447.6925	327.5
1164	S<323>	11402.5625	487.5
1165	S<324>	11357.4325	647.5
1166	S<325>	11414.1725	327.5
1167	S<326>	11369.175	487.5
1168	S<327>	11324.175	647.5
1169	S<328>	11380.65	327.5
1170	S<329>	11335.785	487.5
1171	S<330>	11290.9175	647.5
1172	S<331>	11347.1275	327.5
1173	S<332>	11302.395	487.5
1174	S<333>	11257.66	647.5
1175	S<334>	11313.6075	327.5
1176	S<335>	11269.005	487.5
1177	S<336>	11224.4025	647.5
1178	S<337>	11280.085	327.5
1179	S<338>	11235.615	487.5
1180	S<339>	11191.145	647.5
1181	S<340>	11246.5625	327.5
1182	S<341>	11202.225	487.5
1183	S<342>	11157.8875	647.5
1184	S<343>	11213.04	327.5
1185	S<344>	11168.835	487.5
1186	S<345>	11124.63	647.5
1187	S<346>	11179.52	327.5
1188	S<347>	11135.4475	487.5
1189	S<348>	11091.3725	647.5
1190	S<349>	11145.9975	327.5
1191	S<350>	11102.0575	487.5

1192	S<351>	11058.115	647.5
1193	S<352>	11112.475	327.5
1194	S<353>	11068.6675	487.5
1195	S<354>	11024.8575	647.5
1196	S<355>	11078.955	327.5
1197	S<356>	11035.2775	487.5
1198	S<357>	10991.6	647.5
1199	S<358>	11045.4325	327.5
1200	S<359>	11001.8875	487.5
1201	S<360>	10958.3425	647.5
1202	S<361>	11011.91	327.5
1203	S<362>	10968.4975	487.5
1204	S<363>	10925.085	647.5
1205	S<364>	10978.3875	327.5
1206	S<365>	10935.1075	487.5
1207	S<366>	10891.8275	647.5
1208	S<367>	10944.8675	327.5
1209	S<368>	10901.72	487.5
1210	S<369>	10858.57	647.5
1211	S<370>	10911.345	327.5
1212	S<371>	10868.33	487.5
1213	S<372>	10825.3125	647.5
1214	S<373>	10877.8225	327.5
1215	S<374>	10834.94	487.5
1216	S<375>	10792.0575	647.5
1217	S<376>	10844.3025	327.5
1218	S<377>	10801.55	487.5
1219	S<378>	10758.8	647.5
1220	S<379>	10810.78	327.5
1221	S<380>	10768.16	487.5
1222	S<381>	10725.5425	647.5
1223	S<382>	10777.2575	327.5
1224	S<383>	10734.77	487.5
1225	S<384>	10692.285	647.5
1226	S<385>	10743.735	327.5
1227	S<386>	10701.38	487.5
1228	S<387>	10659.0275	647.5
1229	S<388>	10710.215	327.5
1230	S<389>	10667.9925	487.5
1231	S<390>	10625.77	647.5

1232	S<391>	10676.6925	327.5
1233	S<392>	10634.6025	487.5
1234	S<393>	10592.5125	647.5
1235	S<394>	10643.17	327.5
1236	S<395>	10601.2125	487.5
1237	S<396>	10559.255	647.5
1238	S<397>	10609.65	327.5
1239	S<398>	10567.8225	487.5
1240	S<399>	10525.9975	647.5
1241	S<400>	10576.1275	327.5
1242	S<401>	10534.4325	487.5
1243	S<402>	10492.74	647.5
1244	S<403>	10542.605	327.5
1245	S<404>	10501.0425	487.5
1246	S<405>	10459.4825	647.5
1247	S<406>	10509.0825	327.5
1248	S<407>	10467.6525	487.5
1249	S<408>	10426.225	647.5
1250	S<409>	10475.5625	327.5
1251	S<410>	10434.265	487.5
1252	S<411>	10392.9675	647.5
1253	S<412>	10442.04	327.5
1254	S<413>	10400.875	487.5
1255	S<414>	10359.71	647.5
1256	S<415>	10408.5175	327.5
1257	S<416>	10367.485	487.5
1258	S<417>	10326.4525	647.5
1259	S<418>	10374.995	327.5
1260	S<419>	10334.095	487.5
1261	S<420>	10293.195	647.5
1262	S<421>	10341.475	327.5
1263	S<422>	10300.705	487.5
1264	S<423>	10259.9375	647.5
1265	S<424>	10307.9525	327.5
1266	S<425>	10267.315	487.5
1267	S<426>	10226.68	647.5
1268	S<427>	10274.43	327.5
1269	S<428>	10233.9275	487.5
1270	S<429>	10193.4225	647.5
1271	S<430>	10240.91	327.5

1272	S<431>	10200.5375	487.5
1273	S<432>	10160.165	647.5
1274	S<433>	10207.3875	327.5
1275	S<434>	10167.1475	487.5
1276	S<435>	10126.9075	647.5
1277	S<436>	10173.865	327.5
1278	S<437>	10133.7575	487.5
1279	S<438>	10093.65	647.5
1280	S<439>	10140.3425	327.5
1281	S<440>	10100.3675	487.5
1282	S<441>	10060.3925	647.5
1283	S<442>	10106.8225	327.5
1284	S<443>	10066.9775	487.5
1285	S<444>	10027.135	647.5
1286	S<445>	10073.3	327.5
1287	S<446>	10033.5875	487.5
1288	S<447>	9993.8775	647.5
1289	S<448>	10039.7775	327.5
1290	S<449>	10000.2	487.5
1291	S<450>	9960.62	647.5
1292	S<451>	10006.2575	327.5
1293	S<452>	9966.81	487.5
1294	S<453>	9927.3625	647.5
1295	S<454>	9972.735	327.5
1296	S<455>	9933.42	487.5
1297	S<456>	9894.105	647.5
1298	S<457>	9939.2125	327.5
1299	S<458>	9900.03	487.5
1300	S<459>	9860.8475	647.5
1301	S<460>	9905.69	327.5
1302	S<461>	9866.64	487.5
1303	S<462>	9827.59	647.5
1304	S<463>	9872.17	327.5
1305	S<464>	9833.25	487.5
1306	S<465>	9794.3325	647.5
1307	S<466>	9838.6475	327.5
1308	S<467>	9799.86	487.5
1309	S<468>	9761.075	647.5
1310	S<469>	9805.125	327.5
1311	S<470>	9766.4725	487.5

1312	S<471>	9727.8175	647.5
1313	S<472>	9771.605	327.5
1314	S<473>	9733.08	487.5
1315	S<474>	9694.56	647.5
1316	S<475>	9738.0825	327.5
1317	S<476>	9699.6925	487.5
1318	S<477>	9661.3025	647.5
1319	S<478>	9704.56	327.5
1320	S<479>	9666.3025	487.5
1321	S<480>	9628.045	647.5
1322	S<481>	9671.0375	327.5
1323	S<482>	9632.9125	487.5
1324	S<483>	9594.7875	647.5
1325	S<484>	9637.5175	327.5
1326	S<485>	9599.5225	487.5
1327	S<486>	9561.53	647.5
1328	S<487>	9603.995	327.5
1329	S<488>	9566.1325	487.5
1330	S<489>	9528.2725	647.5
1331	S<490>	9570.4725	327.5
1332	S<491>	9532.745	487.5
1333	S<492>	9495.015	647.5
1334	S<493>	9536.9525	327.5
1335	S<494>	9499.3525	487.5
1336	S<495>	9461.7575	647.5
1337	S<496>	9503.43	327.5
1338	S<497>	9465.965	487.5
1339	S<498>	9428.5	647.5
1340	S<499>	9469.9075	327.5
1341	S<500>	9432.575	487.5
1342	S<501>	9395.2425	647.5
1343	S<502>	9436.385	327.5
1344	S<503>	9399.185	487.5
1345	S<504>	9361.985	647.5
1346	S<505>	9402.865	327.5
1347	S<506>	9365.795	487.5
1348	S<507>	9328.7275	647.5
1349	S<508>	9369.3425	327.5
1350	S<509>	9332.405	487.5
1351	S<510>	9295.47	647.5

1352	S<511>	9335.82	327.5
1353	S<512>	9299.0175	487.5
1354	S<513>	9262.2125	647.5
1355	S<514>	9302.3	327.5
1356	S<515>	9265.625	487.5
1357	S<516>	9228.955	647.5
1358	S<517>	9268.7775	327.5
1359	S<518>	9232.2375	487.5
1360	S<519>	9195.6975	647.5
1361	S<520>	9235.255	327.5
1362	S<521>	9198.8475	487.5
1363	S<522>	9162.44	647.5
1364	S<523>	9201.7325	327.5
1365	S<524>	9165.4575	487.5
1366	S<525>	9129.1825	647.5
1367	S<526>	9168.21	327.5
1368	S<527>	9132.0675	487.5
1369	S<528>	9095.925	647.5
1370	S<529>	9134.69	327.5
1371	S<530>	9098.6775	487.5
1372	S<531>	9062.6675	647.5
1373	S<532>	9101.1675	327.5
1374	S<533>	9065.29	487.5
1375	S<534>	9029.41	647.5
1376	S<535>	9067.6475	327.5
1377	S<536>	9031.8975	487.5
1378	S<537>	8996.1525	647.5
1379	S<538>	9034.125	327.5
1380	S<539>	8998.51	487.5
1381	S<540>	8962.895	647.5
1382	S<541>	9000.6025	327.5
1383	S<542>	8965.12	487.5
1384	S<543>	8929.6375	647.5
1385	S<544>	8967.08	327.5
1386	S<545>	8931.73	487.5
1387	S<546>	8896.38	647.5
1388	S<547>	8933.5575	327.5
1389	S<548>	8898.34	487.5
1390	S<549>	8863.1225	647.5
1391	S<550>	8900.0375	327.5

1392	S<551>	8864.95	487.5
1393	S<552>	8829.865	647.5
1394	S<553>	8866.515	327.5
1395	S<554>	8831.5625	487.5
1396	S<555>	8796.6075	647.5
1397	S<556>	8832.995	327.5
1398	S<557>	8798.17	487.5
1399	S<558>	8763.35	647.5
1400	S<559>	8799.4725	327.5
1401	S<560>	8764.7825	487.5
1402	S<561>	8730.0925	647.5
1403	S<562>	8765.95	327.5
1404	S<563>	8731.3925	487.5
1405	S<564>	8696.835	647.5
1406	S<565>	8732.4275	327.5
1407	S<566>	8698.0025	487.5
1408	S<567>	8663.5775	647.5
1409	S<568>	8698.905	327.5
1410	S<569>	8664.6125	487.5
1411	S<570>	8630.32	647.5
1412	S<571>	8665.385	327.5
1413	S<572>	8631.2225	487.5
1414	S<573>	8597.0625	647.5
1415	S<574>	8631.8625	327.5
1416	S<575>	8597.835	487.5
1417	S<576>	8563.805	647.5
1418	S<577>	8598.3425	327.5
1419	S<578>	8564.4425	487.5
1420	S<579>	8530.5475	647.5
1421	S<580>	8564.82	327.5
1422	S<581>	8531.055	487.5
1423	S<582>	8497.29	647.5
1424	S<583>	8531.2975	327.5
1425	S<584>	8497.665	487.5
1426	S<585>	8464.0325	647.5
1427	S<586>	8497.775	327.5
1428	S<587>	8464.275	487.5
1429	S<588>	8430.775	647.5
1430	S<589>	8464.2525	327.5
1431	S<590>	8430.885	487.5

1432	S<591>	8397.5175	647.5
1433	S<592>	8430.7325	327.5
1434	S<593>	8397.495	487.5
1435	S<594>	8364.26	647.5
1436	S<595>	8397.21	327.5
1437	S<596>	8364.1075	487.5
1438	S<597>	8331.0025	647.5
1439	S<598>	8363.69	327.5
1440	S<599>	8330.715	487.5
1441	S<600>	8297.745	647.5
1442	S<601>	8330.1675	327.5
1443	S<602>	8297.3275	487.5
1444	S<603>	8264.4875	647.5
1445	S<604>	8296.645	327.5
1446	S<605>	8263.9375	487.5
1447	S<606>	8231.23	647.5
1448	S<607>	8263.1225	327.5
1449	S<608>	8230.5475	487.5
1450	S<609>	8197.9725	647.5
1451	S<610>	8229.6	327.5
1452	S<611>	8197.1575	487.5
1453	S<612>	8164.715	647.5
1454	S<613>	8196.08	327.5
1455	S<614>	8163.7675	487.5
1456	S<615>	8131.4575	647.5
1457	S<616>	8162.5575	327.5
1458	S<617>	8130.38	487.5
1459	S<618>	8098.2	647.5
1460	S<619>	8129.0375	327.5
1461	S<620>	8096.9875	487.5
1462	S<621>	8064.9425	647.5
1463	S<622>	8095.515	327.5
1464	S<623>	8063.6	487.5
1465	S<624>	8031.685	647.5
1466	S<625>	8061.9925	327.5
1467	S<626>	8030.21	487.5
1468	S<627>	7998.4275	647.5
1469	S<628>	8028.47	327.5
1470	S<629>	7996.82	487.5
1471	S<630>	7965.17	647.5

1472	S<631>	7994.9475	327.5
1473	S<632>	7963.43	487.5
1474	S<633>	7931.9125	647.5
1475	S<634>	7961.425	327.5
1476	S<635>	7930.04	487.5
1477	S<636>	7898.655	647.5
1478	S<637>	7927.905	327.5
1479	S<638>	7896.6525	487.5
1480	S<639>	7865.3975	647.5
1481	S<640>	7894.385	327.5
1482	S<641>	7863.26	487.5
1483	S<642>	7832.14	647.5
1484	S<643>	7860.8625	327.5
1485	S<644>	7829.8725	487.5
1486	S<645>	7798.8825	647.5
1487	S<646>	7827.34	327.5
1488	S<647>	7796.4825	487.5
1489	S<648>	7765.625	647.5
1490	S<649>	7793.8175	327.5
1491	S<650>	7763.0925	487.5
1492	S<651>	7732.3675	647.5
1493	S<652>	7760.295	327.5
1494	S<653>	7729.7025	487.5
1495	S<654>	7699.11	647.5
1496	S<655>	7726.7725	327.5
1497	S<656>	7696.3125	487.5
1498	S<657>	7665.8525	647.5
1499	S<658>	7693.2525	327.5
1500	S<659>	7662.925	487.5
1501	S<660>	7632.595	647.5
1502	S<661>	7659.7325	327.5
1503	S<662>	7629.5325	487.5
1504	S<663>	7599.3375	647.5
1505	S<664>	7626.21	327.5
1506	S<665>	7596.145	487.5
1507	S<666>	7566.08	647.5
1508	S<667>	7592.6875	327.5
1509	S<668>	7562.755	487.5
1510	S<669>	7532.8225	647.5
1511	S<670>	7559.165	327.5

1512	S<671>	7529.365	487.5
1513	S<672>	7499.565	647.5
1514	S<673>	7525.6425	327.5
1515	S<674>	7495.975	487.5
1516	S<675>	7466.3075	647.5
1517	S<676>	7492.12	327.5
1518	S<677>	7462.585	487.5
1519	S<678>	7433.05	647.5
1520	S<679>	7458.6	327.5
1521	S<680>	7429.1975	487.5
1522	S<681>	7399.7925	647.5
1523	S<682>	7425.08	327.5
1524	S<683>	7395.805	487.5
1525	S<684>	7366.535	647.5
1526	S<685>	7391.5575	327.5
1527	S<686>	7362.4175	487.5
1528	S<687>	7333.2775	647.5
1529	S<688>	7358.035	327.5
1530	S<689>	7329.025	487.5
1531	S<690>	7300.02	647.5
1532	S<691>	7324.5125	327.5
1533	S<692>	7295.6375	487.5
1534	S<693>	7266.7625	647.5
1535	S<694>	7290.99	327.5
1536	S<695>	7262.2475	487.5
1537	S<696>	7233.505	647.5
1538	S<697>	7257.4675	327.5
1539	S<698>	7228.8575	487.5
1540	S<699>	7200.2475	647.5
1541	S<700>	7223.9475	327.5
1542	S<701>	7195.47	487.5
1543	S<702>	7166.99	647.5
1544	S<703>	7190.4275	327.5
1545	S<704>	7162.0775	487.5
1546	S<705>	7133.7325	647.5
1547	S<706>	7156.905	327.5
1548	S<707>	7128.69	487.5
1549	S<708>	7100.475	647.5
1550	S<709>	7123.3825	327.5
1551	S<710>	7095.2975	487.5

1552	S<711>	7067.2175	647.5
1553	S<712>	7089.86	327.5
1554	S<713>	7061.91	487.5
1555	S<714>	7033.96	647.5
1556	S<715>	7056.3375	327.5
1557	S<716>	7028.52	487.5
1558	S<717>	7000.7025	647.5
1559	S<718>	7022.815	327.5
1560	S<719>	6995.13	487.5
1561	S<720>	6967.445	647.5
1562	S<721>	6989.295	327.5
1563	S<722>	6961.7425	487.5
1564	S<723>	6934.1875	647.5
1565	S<724>	6955.775	327.5
1566	S<725>	6928.35	487.5
1567	S<726>	6900.93	647.5
1568	S<727>	6922.2525	327.5
1569	S<728>	6894.9625	487.5
1570	S<729>	6867.6725	647.5
1571	S<730>	6888.73	327.5
1572	S<731>	6861.57	487.5
1573	S<732>	6834.415	647.5
1574	S<733>	6855.2075	327.5
1575	S<734>	6828.1825	487.5
1576	S<735>	6801.1575	647.5
1577	S<736>	6821.685	327.5
1578	S<737>	6794.7925	487.5
1579	S<738>	6767.9	647.5
1580	S<739>	6788.1625	327.5
1581	S<740>	6761.4025	487.5
1582	S<741>	6734.6425	647.5
1583	S<742>	6754.64	327.5
1584	S<743>	6728.015	487.5
1585	S<744>	6701.385	647.5
1586	S<745>	6721.1225	327.5
1587	S<746>	6694.6225	487.5
1588	S<747>	6668.1275	647.5
1589	S<748>	6687.6	327.5
1590	S<749>	6661.235	487.5
1591	S<750>	6634.87	647.5

1592	S<751>	6654.0775	327.5
1593	S<752>	6627.8425	487.5
1594	S<753>	6601.6125	647.5
1595	S<754>	6620.555	327.5
1596	S<755>	6594.455	487.5
1597	S<756>	6568.355	647.5
1598	S<757>	6587.0325	327.5
1599	S<758>	6561.065	487.5
1600	S<759>	6535.0975	647.5
1601	S<760>	6553.51	327.5
1602	S<761>	6527.675	487.5
1603	S<762>	6501.84	647.5
1604	S<763>	6519.9875	327.5
1605	S<764>	6494.2875	487.5
1606	S<765>	6468.5825	647.5
1607	S<766>	6486.47	327.5
1608	S<767>	6460.895	487.5
1609	S<768>	6435.325	647.5
1610	S<769>	6452.9475	327.5
1611	S<770>	6427.5075	487.5
1612	S<771>	6402.0675	647.5
1613	S<772>	6419.425	327.5
1614	S<773>	6394.115	487.5
1615	S<774>	6368.81	647.5
1616	S<775>	6385.9025	327.5
1617	S<776>	6360.7275	487.5
1618	S<777>	6335.5525	647.5
1619	S<778>	6352.38	327.5
1620	S<779>	6327.3375	487.5
1621	S<780>	6302.295	647.5
1622	S<781>	6318.8575	327.5
1623	S<782>	6293.9475	487.5
1624	S<783>	6269.0375	647.5
1625	S<784>	6285.335	327.5
1626	S<785>	6260.56	487.5
1627	S<786>	6235.78	647.5
1628	S<787>	6251.8175	327.5
1629	S<788>	6227.1675	487.5
1630	S<789>	6202.5225	647.5
1631	S<790>	6218.295	327.5

1632	S<791>	6193.78	487.5
1633	S<792>	6169.265	647.5
1634	S<793>	6184.7725	327.5
1635	S<794>	6160.3875	487.5
1636	S<795>	6136.0075	647.5
1637	S<796>	6151.25	327.5
1638	S<797>	6127	487.5
1639	S<798>	6102.75	647.5
1640	S<799>	6117.7275	327.5
1641	S<800>	6093.6125	487.5
1642	S<801>	6069.4925	647.5
1643	S<802>	6084.205	327.5
1644	S<803>	6060.22	487.5
1645	S<804>	6036.235	647.5
1646	S<805>	6050.6825	327.5
1647	S<806>	6026.8325	487.5
1648	S<807>	6002.9775	647.5
1649	S<808>	6017.1625	327.5
1650	S<809>	5993.44	487.5
1651	S<810>	5969.72	647.5
1652	S<811>	5983.6425	327.5
1653	S<812>	5960.0525	487.5
1654	S<813>	5936.4625	647.5
1655	S<814>	5950.12	327.5
1656	S<815>	5926.66	487.5
1657	S<816>	5903.205	647.5
1658	S<817>	5916.5975	327.5
1659	S<818>	5893.2725	487.5
1660	S<819>	5869.9475	647.5
1661	S<820>	5883.075	327.5
1662	S<821>	5859.885	487.5
1663	S<822>	5836.69	647.5
1664	S<823>	5849.5525	327.5
1665	S<824>	5826.4925	487.5
1666	S<825>	5803.4325	647.5
1667	S<826>	5816.03	327.5
1668	S<827>	5793.105	487.5
1669	S<828>	5770.175	647.5
1670	S<829>	5782.51	327.5
1671	S<830>	5759.7125	487.5

1672	S<831>	5736.9175	647.5
1673	S<832>	5748.99	327.5
1674	S<833>	5726.325	487.5
1675	S<834>	5703.66	647.5
1676	S<835>	5715.4675	327.5
1677	S<836>	5692.9325	487.5
1678	S<837>	5670.4025	647.5
1679	S<838>	5681.945	327.5
1680	S<839>	5659.545	487.5
1681	S<840>	5637.145	647.5
1682	S<841>	5648.4225	327.5
1683	S<842>	5626.1575	487.5
1684	S<843>	5603.8875	647.5
1685	S<844>	5614.9	327.5
1686	S<845>	5592.765	487.5
1687	S<846>	5570.63	647.5
1688	S<847>	5581.3775	327.5
1689	S<848>	5559.3775	487.5
1690	S<849>	5537.3725	647.5
1691	S<850>	5547.855	327.5
1692	S<851>	5525.985	487.5
1693	S<852>	5504.115	647.5
1694	S<853>	5514.3375	327.5
1695	S<854>	5492.5975	487.5
1696	S<855>	5470.8575	647.5
1697	S<856>	5480.815	327.5
1698	S<857>	5459.205	487.5
1699	S<858>	5437.6	647.5
1700	S<859>	5447.2925	327.5
1701	S<860>	5425.8175	487.5
1702	S<861>	5404.3425	647.5
1703	S<862>	5413.77	327.5
1704	S<863>	5392.43	487.5
1705	S<864>	5371.085	647.5
1706	S<865>	5380.2475	327.5
1707	S<866>	5359.0375	487.5
1708	S<867>	5337.8275	647.5
1709	S<868>	5346.725	327.5
1710	S<869>	5325.65	487.5
1711	S<870>	5304.57	647.5

1712	S<871>	5313.2025	327.5
1713	S<872>	5292.2575	487.5
1714	S<873>	5271.3125	647.5
1715	S<874>	5279.685	327.5
1716	S<875>	5258.87	487.5
1717	S<876>	5238.055	647.5
1718	S<877>	5246.1625	327.5
1719	S<878>	5225.4775	487.5
1720	S<879>	5204.7975	647.5
1721	S<880>	5212.64	327.5
1722	S<881>	5192.09	487.5
1723	S<882>	5171.54	647.5
1724	S<883>	5179.1175	327.5
1725	S<884>	5158.7025	487.5
1726	S<885>	5138.2825	647.5
1727	S<886>	5145.595	327.5
1728	S<887>	5125.31	487.5
1729	S<888>	5105.025	647.5
1730	S<889>	5112.0725	327.5
1731	S<890>	5091.9225	487.5
1732	S<891>	5071.7675	647.5
1733	S<892>	5078.55	327.5
1734	S<893>	5058.53	487.5
1735	S<894>	5038.51	647.5
1736	S<895>	5045.0325	327.5
1737	S<896>	5025.1425	487.5
1738	S<897>	5005.2525	647.5
1739	S<898>	5011.51	327.5
1740	S<899>	4991.75	487.5
1741	S<900>	4971.995	647.5
1742	S<901>	4977.9875	327.5
1743	S<902>	4958.3625	487.5
1744	S<903>	4938.7375	647.5
1745	S<904>	4944.465	327.5
1746	S<905>	4924.9725	487.5
1747	S<906>	4905.48	647.5
1748	S<907>	4910.9425	327.5
1749	S<908>	4891.5825	487.5
1750	S<909>	4872.2225	647.5
1751	S<910>	4877.42	327.5

1752	S<911>	4858.195	487.5
1753	S<912>	4838.965	647.5
1754	S<913>	4843.8975	327.5
1755	S<914>	4824.8025	487.5
1756	S<915>	4805.7075	647.5
1757	S<916>	4810.38	327.5
1758	S<917>	4791.415	487.5
1759	S<918>	4772.45	647.5
1760	S<919>	4776.8575	327.5
1761	S<920>	4758.0225	487.5
1762	S<921>	4739.1925	647.5
1763	S<922>	4743.335	327.5
1764	S<923>	4724.635	487.5
1765	S<924>	4705.935	647.5
1766	S<925>	4709.8125	327.5
1767	S<926>	4691.245	487.5
1768	S<927>	4672.6775	647.5
1769	S<928>	4676.29	327.5
1770	S<929>	4657.855	487.5
1771	S<930>	4639.42	647.5
1772	S<931>	4642.7675	327.5
1773	S<932>	4624.4675	487.5
1774	S<933>	4606.1625	647.5
1775	S<934>	4609.245	327.5
1776	S<935>	4591.075	487.5
1777	S<936>	4572.905	647.5
1778	S<937>	4575.7275	327.5
1779	S<938>	4557.6875	487.5
1780	S<939>	4539.6475	647.5
1781	S<940>	4542.205	327.5
1782	S<941>	4524.295	487.5
1783	S<942>	4506.39	647.5
1784	S<943>	4508.6825	327.5
1785	S<944>	4490.9075	487.5
1786	S<945>	4473.1325	647.5
1787	S<946>	4475.16	327.5
1788	S<947>	4457.5175	487.5
1789	S<948>	4439.875	647.5
1790	S<949>	4441.6375	327.5
1791	S<950>	4424.1275	487.5

1792	S<951>	4406.6175	647.5
1793	S<952>	4408.115	327.5
1794	S<953>	4390.74	487.5
1795	S<954>	4373.36	647.5
1796	S<955>	4374.5925	327.5
1797	S<956>	4357.3475	487.5
1798	S<957>	4340.1025	647.5
1799	S<958>	4341.075	327.5
1800	S<959>	4323.96	487.5
1801	S<960>	4306.845	647.5
1802	S<961>	4307.5525	327.5
1803	S<962>	4290.5675	487.5
1804	S<963>	4273.5875	647.5
1805	S<964>	4274.03	327.5
1806	S<965>	4257.18	487.5
1807	S<966>	4240.33	647.5
1808	S<967>	4240.5075	327.5
1809	S<968>	4223.79	487.5
1810	S<969>	4207.0725	647.5
1811	S<970>	4206.985	327.5
1812	S<971>	4190.4	487.5
1813	S<972>	4173.815	647.5
1814	S<973>	4173.4625	327.5
1815	S<974>	4157.0125	487.5
1816	S<975>	4140.5575	647.5
1817	S<976>	4139.94	327.5
1818	S<977>	4123.62	487.5
1819	S<978>	4107.3	647.5
1820	S<979>	4106.42	327.5
1821	S<980>	4090.2325	487.5
1822	S<981>	4074.0425	647.5
1823	S<982>	4072.9	327.5
1824	S<983>	4056.84	487.5
1825	S<984>	4040.785	647.5
1826	S<985>	4039.3775	327.5
1827	S<986>	4023.4525	487.5
1828	S<987>	4007.5275	647.5
1829	S<988>	4005.855	327.5
1830	S<989>	3990.0625	487.5
1831	S<990>	3974.27	647.5

1832	S<991>	3972.3325	327.5
1833	S<992>	3956.6725	487.5
1834	S<993>	3941.0125	647.5
1835	S<994>	3938.81	327.5
1836	S<995>	3923.285	487.5
1837	S<996>	3907.755	647.5
1838	S<997>	3905.2875	327.5
1839	S<998>	3889.8925	487.5
1840	S<999>	3874.4975	647.5
1841	S<1000>	3871.7675	327.5
1842	S<1001>	3856.505	487.5
1843	S<1002>	3841.24	647.5
1844	S<1003>	3838.2475	327.5
1845	S<1004>	3823.1125	487.5
1846	S<1005>	3807.9825	647.5
1847	S<1006>	3804.725	327.5
1848	S<1007>	3789.725	487.5
1849	S<1008>	3774.725	647.5
1850	S<1009>	3771.2025	327.5
1851	S<1010>	3756.335	487.5
1852	S<1011>	3741.4675	647.5
1853	S<1012>	3737.68	327.5
1854	S<1013>	3722.945	487.5
1855	S<1014>	3708.21	647.5
1856	S<1015>	3704.1575	327.5
1857	S<1016>	3689.5575	487.5
1858	S<1017>	3674.9525	647.5
1859	S<1018>	3670.635	327.5
1860	S<1019>	3656.165	487.5
1861	S<1020>	3641.695	647.5
1862	S<1021>	3637.115	327.5
1863	S<1022>	3622.7775	487.5
1864	S<1023>	3608.4375	647.5
1865	S<1024>	3603.595	327.5
1866	S<1025>	3589.385	487.5
1867	S<1026>	3575.18	647.5
1868	S<1027>	3570.0725	327.5
1869	S<1028>	3555.9975	487.5
1870	S<1029>	3541.9225	647.5
1871	S<1030>	3536.55	327.5

1872	S<1031>	3522.6075	487.5
1873	S<1032>	3508.665	647.5
1874	S<1033>	3503.0275	327.5
1875	S<1034>	3489.2175	487.5
1876	S<1035>	3475.4075	647.5
1877	S<1036>	3469.505	327.5
1878	S<1037>	3455.83	487.5
1879	S<1038>	3442.15	647.5
1880	S<1039>	3435.9825	327.5
1881	S<1040>	3422.4375	487.5
1882	S<1041>	3408.8925	647.5
1883	S<1042>	3402.4625	327.5
1884	S<1043>	3389.05	487.5
1885	S<1044>	3375.635	647.5
1886	S<1045>	3368.9425	327.5
1887	S<1046>	3355.6575	487.5
1888	S<1047>	3342.3775	647.5
1889	S<1048>	3335.42	327.5
1890	S<1049>	3322.27	487.5
1891	S<1050>	3309.12	647.5
1892	S<1051>	3301.8975	327.5
1893	S<1052>	3288.88	487.5
1894	S<1053>	3275.8625	647.5
1895	S<1054>	3268.375	327.5
1896	S<1055>	3255.49	487.5
1897	S<1056>	3242.605	647.5
1898	S<1057>	3234.8525	327.5
1899	S<1058>	3222.1025	487.5
1900	S<1059>	3209.3475	647.5
1901	S<1060>	3201.33	327.5
1902	S<1061>	3188.71	487.5
1903	S<1062>	3176.09	647.5
1904	S<1063>	3167.81	327.5
1905	S<1064>	3155.3225	487.5
1906	S<1065>	3142.8325	647.5
1907	S<1066>	3134.29	327.5
1908	S<1067>	3121.93	487.5
1909	S<1068>	3109.575	647.5
1910	S<1069>	3100.7675	327.5
1911	S<1070>	3088.5425	487.5

1912	S<1071>	3076.3175	647.5
1913	S<1072>	3067.245	327.5
1914	S<1073>	3055.1525	487.5
1915	S<1074>	3043.06	647.5
1916	S<1075>	3033.7225	327.5
1917	S<1076>	3021.7625	487.5
1918	S<1077>	3009.8025	647.5
1919	S<1078>	3000.2	327.5
1920	S<1079>	2988.375	487.5
1921	S<1080>	2976.545	647.5
1922	S<1081>	2966.6775	327.5
1923	S<1082>	2954.9825	487.5
1924	S<1083>	2943.2875	647.5
1925	S<1084>	2933.1575	327.5
1926	S<1085>	2921.595	487.5
1927	S<1086>	2910.03	647.5
1928	S<1087>	2899.635	327.5
1929	S<1088>	2888.2025	487.5
1930	S<1089>	2876.7725	647.5
1931	S<1090>	2866.115	327.5
1932	S<1091>	2854.815	487.5
1933	S<1092>	2843.515	647.5
1934	S<1093>	2832.5925	327.5
1935	S<1094>	2821.425	487.5
1936	S<1095>	2810.2575	647.5
1937	S<1096>	2799.07	327.5
1938	S<1097>	2788.035	487.5
1939	S<1098>	2777	647.5
1940	S<1099>	2765.5475	327.5
1941	S<1100>	2754.6475	487.5
1942	S<1101>	2743.7425	647.5
1943	S<1102>	2732.025	327.5
1944	S<1103>	2721.255	487.5
1945	S<1104>	2710.485	647.5
1946	S<1105>	2698.505	327.5
1947	S<1106>	2687.8675	487.5
1948	S<1107>	2677.2275	647.5
1949	S<1108>	2664.9825	327.5
1950	S<1109>	2654.475	487.5
1951	S<1110>	2643.97	647.5

1952	S<1111>	2631.4625	327.5
1953	S<1112>	2621.0875	487.5
1954	S<1113>	2610.7125	647.5
1955	S<1114>	2597.94	327.5
1956	S<1115>	2587.6975	487.5
1957	S<1116>	2577.455	647.5
1958	S<1117>	2564.4175	327.5
1959	S<1118>	2554.3075	487.5
1960	S<1119>	2544.1975	647.5
1961	S<1120>	2530.895	327.5
1962	S<1121>	2520.92	487.5
1963	S<1122>	2510.94	647.5
1964	S<1123>	2497.3725	327.5
1965	S<1124>	2487.5275	487.5
1966	S<1125>	2477.6825	647.5
1967	S<1126>	2463.8525	327.5
1968	S<1127>	2454.14	487.5
1969	S<1128>	2444.425	647.5
1970	S<1129>	2430.33	327.5
1971	S<1130>	2420.7475	487.5
1972	S<1131>	2411.1675	647.5
1973	S<1132>	2396.81	327.5
1974	S<1133>	2387.36	487.5
1975	S<1134>	2377.91	647.5
1976	S<1135>	2363.2875	327.5
1977	S<1136>	2353.97	487.5
1978	S<1137>	2344.6525	647.5
1979	S<1138>	2329.765	327.5
1980	S<1139>	2320.58	487.5
1981	S<1140>	2311.395	647.5
1982	S<1141>	2296.2425	327.5
1983	S<1142>	2287.19	487.5
1984	S<1143>	2278.1375	647.5
1985	S<1144>	2262.72	327.5
1986	S<1145>	2253.8	487.5
1987	S<1146>	2244.88	647.5
1988	S<1147>	2229.2	327.5
1989	S<1148>	2220.4125	487.5
1990	S<1149>	2211.6225	647.5
1991	S<1150>	2195.6775	327.5

1992	S<1151>	2187.02	487.5
1993	S<1152>	2178.365	647.5
1994	S<1153>	2162.1575	327.5
1995	S<1154>	2153.6325	487.5
1996	S<1155>	2145.1075	647.5
1997	S<1156>	2128.635	327.5
1998	S<1157>	2120.2425	487.5
1999	S<1158>	2111.85	647.5
2000	S<1159>	2095.1125	327.5
2001	S<1160>	2086.8525	487.5
2002	S<1161>	2078.5925	647.5
2003	S<1162>	2061.59	327.5
2004	S<1163>	2053.4625	487.5
2005	S<1164>	2045.335	647.5
2006	S<1165>	2028.0675	327.5
2007	S<1166>	2020.0725	487.5
2008	S<1167>	2012.0775	647.5
2009	S<1168>	1994.5475	327.5
2010	S<1169>	1986.685	487.5
2011	S<1170>	1978.82	647.5
2012	S<1171>	1961.025	327.5
2013	S<1172>	1953.295	487.5
2014	S<1173>	1945.5625	647.5
2015	S<1174>	1927.505	327.5
2016	S<1175>	1919.905	487.5
2017	S<1176>	1912.305	647.5
2018	S<1177>	1893.9825	327.5
2019	S<1178>	1886.515	487.5
2020	S<1179>	1879.0475	647.5
2021	S<1180>	1860.46	327.5
2022	S<1181>	1853.125	487.5
2023	S<1182>	1845.79	647.5
2024	S<1183>	1826.9375	327.5
2025	S<1184>	1819.735	487.5
2026	S<1185>	1812.5325	647.5
2027	S<1186>	1793.415	327.5
2028	S<1187>	1786.345	487.5
2029	S<1188>	1779.275	647.5
2030	S<1189>	1759.895	327.5
2031	S<1190>	1752.9575	487.5

2032	S<1191>	1746.0175	647.5
2033	S<1192>	1726.3725	327.5
2034	S<1193>	1719.5675	487.5
2035	S<1194>	1712.76	647.5
2036	S<1195>	1692.85	327.5
2037	S<1196>	1686.1775	487.5
2038	S<1197>	1679.5025	647.5
2039	S<1198>	1659.33	327.5
2040	S<1199>	1652.7875	487.5
2041	S<1200>	1646.245	647.5
2042	S<1201>	1625.8075	327.5
2043	S<1202>	1619.3975	487.5
2044	S<1203>	1612.9875	647.5
2045	S<1204>	1592.285	327.5
2046	S<1205>	1586.0075	487.5
2047	S<1206>	1579.73	647.5
2048	S<1207>	1558.7625	327.5
2049	S<1208>	1552.6175	487.5
2050	S<1209>	1546.4725	647.5
2051	S<1210>	1525.2425	327.5
2052	S<1211>	1519.23	487.5
2053	S<1212>	1513.215	647.5
2054	S<1213>	1491.72	327.5
2055	S<1214>	1485.84	487.5
2056	S<1215>	1479.9575	647.5
2057	S<1216>	1458.1975	327.5
2058	S<1217>	1452.45	487.5
2059	S<1218>	1446.7	647.5
2060	S<1219>	1424.6775	327.5
2061	S<1220>	1419.06	487.5
2062	S<1221>	1413.4425	647.5
2063	S<1222>	1391.155	327.5
2064	S<1223>	1385.67	487.5
2065	S<1224>	1380.185	647.5
2066	S<1225>	1357.6325	327.5
2067	S<1226>	1352.28	487.5
2068	S<1227>	1346.9275	647.5
2069	S<1228>	1324.11	327.5
2070	S<1229>	1318.89	487.5
2071	S<1230>	1313.67	647.5

2072	S<1231>	1290.59	327.5
2073	S<1232>	1285.5025	487.5
2074	S<1233>	1280.4125	647.5
2075	S<1234>	1257.0675	327.5
2076	S<1235>	1252.1125	487.5
2077	S<1236>	1247.155	647.5
2078	S<1237>	1223.545	327.5
2079	S<1238>	1218.7225	487.5
2080	S<1239>	1213.8975	647.5
2081	S<1240>	1190.025	327.5
2082	S<1241>	1185.3325	487.5
2083	S<1242>	1180.64	647.5
2084	S<1243>	1156.5025	327.5
2085	S<1244>	1151.9425	487.5
2086	S<1245>	1147.3825	647.5
2087	S<1246>	1122.98	327.5
2088	S<1247>	1118.5525	487.5
2089	S<1248>	1114.125	647.5
2090	S<1249>	1089.4575	327.5
2091	S<1250>	1085.1625	487.5
2092	S<1251>	1080.8675	647.5
2093	S<1252>	1055.9375	327.5
2094	S<1253>	1051.775	487.5
2095	S<1254>	1047.61	647.5
2096	S<1255>	1022.415	327.5
2097	S<1256>	1018.385	487.5
2098	S<1257>	1014.3525	647.5
2099	S<1258>	988.8925	327.5
2100	S<1259>	984.995	487.5
2101	S<1260>	981.095	647.5
2102	S<1261>	955.3725	327.5
2103	S<1262>	951.605	487.5
2104	S<1263>	947.8375	647.5
2105	S<1264>	921.85	327.5
2106	S<1265>	918.215	487.5
2107	S<1266>	914.58	647.5
2108	S<1267>	888.3275	327.5
2109	S<1268>	884.825	487.5
2110	S<1269>	881.3225	647.5
2111	S<1270>	854.805	327.5

2112	S<1271>	851.435	487.5
2113	S<1272>	848.065	647.5
2114	S<1273>	821.285	327.5
2115	S<1274>	818.0475	487.5
2116	S<1275>	814.8075	647.5
2117	S<1276>	787.7625	327.5
2118	S<1277>	784.6575	487.5
2119	S<1278>	781.55	647.5
2120	VSSDUMMY	754.24	327.5
2121	S<1279>	751.2675	487.5
2122	S<1280>	748.2925	647.5
2123	VSSDUMMY	720.72	327.5
2124	VSSDUMMY	717.8775	487.5
2125	VSSDUMMY	715.035	647.5
2126	VSSDUMMY	687.1975	327.5
2127	VSSDUMMY	684.4875	487.5
2128	VSSDUMMY	681.7775	647.5
2129	VSSDUMMY	653.675	327.5
2130	VSSDUMMY	651.0975	487.5
2131	VSSDUMMY	648.52	647.5
2132	VSSDUMMY	620.1525	327.5
2133	VSSDUMMY	617.7075	487.5
2134	VSSDUMMY	615.2625	647.5
2135	VSSDUMMY	586.6325	327.5
2136	VSSDUMMY	584.32	487.5
2137	VSSDUMMY	582.005	647.5
2138	VSSDUMMY	553.11	327.5
2139	VSSDUMMY	550.93	487.5
2140	VSSDUMMY	548.7475	647.5
2141	VSSDUMMY	519.5875	327.5
2142	VSSDUMMY	517.54	487.5
2143	VSSDUMMY	515.49	647.5
2144	VSSDUMMY	486.065	327.5
2145	VSSDUMMY	484.15	487.5
2146	VSSDUMMY	482.2325	647.5
2147	VSSDUMMY	452.545	327.5
2148	VSSDUMMY	450.76	487.5
2149	VSSDUMMY	448.975	647.5
2150	VSSDUMMY	419.0225	327.5
2151	VSSDUMMY	417.37	487.5

2152	VSSDUMMY	415.7175	647.5
2153	VSSDUMMY	385.5	327.5
2154	VSSDUMMY	383.98	487.5
2155	VSSDUMMY	382.46	647.5
2156	VSSDUMMY	351.98	327.5
2157	VSSDUMMY	350.5925	487.5
2158	VSSDUMMY	349.2025	647.5
2159	VSSDUMMY	318.4575	327.5
2160	VSSDUMMY	317.2025	487.5
2161	VSSDUMMY	315.945	647.5
2162	VSSDUMMY	284.935	327.5
2163	VSSDUMMY	283.8125	487.5
2164	VSSDUMMY	282.6875	647.5
2165	VSSDUMMY	251.4125	327.5
2166	VSSDUMMY	250.4225	487.5
2167	VSSDUMMY	249.43	647.5
2168	VSSDUMMY	217.8925	327.5
2169	VSSDUMMY	217.0325	487.5
2170	VSSDUMMY	216.1725	647.5
2171	VSSDUMMY	184.37	327.5
2172	VSSDUMMY	183.6425	487.5
2173	VSSDUMMY	182.915	647.5
2174	VSSDUMMY	150.8475	327.5
2175	VSSDUMMY	150.2525	487.5
2176	VSSDUMMY	149.6575	647.5
2177	VSSDUMMY	117.3275	327.5
2178	VSSDUMMY	116.865	487.5
2179	VSSDUMMY	116.4	647.5
2180	VSSDUMMY	83.805	327.5
2181	VSSDUMMY	83.475	487.5
2182	VSSDUMMY	83.1425	647.5
2183	VSSDUMMY	50.2825	327.5
2184	VSSDUMMY	50.085	487.5
2185	VSSDUMMY	49.885	647.5
2186	VSSDUMMY	16.76	327.5
2187	VSSDUMMY	16.695	487.5
2188	VSSDUMMY	16.6275	647.5
2189	VSSDUMMY	-16.6275	647.5
2190	VSSDUMMY	-16.695	487.5
2191	VSSDUMMY	-16.76	327.5

2192	VSSDUMMY	-49.885	647.5
2193	VSSDUMMY	-50.085	487.5
2194	VSSDUMMY	-50.2825	327.5
2195	VSSDUMMY	-83.1425	647.5
2196	VSSDUMMY	-83.475	487.5
2197	VSSDUMMY	-83.805	327.5
2198	VSSDUMMY	-116.4	647.5
2199	VSSDUMMY	-116.865	487.5
2200	VSSDUMMY	-117.3275	327.5
2201	VSSDUMMY	-149.6575	647.5
2202	VSSDUMMY	-150.2525	487.5
2203	VSSDUMMY	-150.8475	327.5
2204	VSSDUMMY	-182.915	647.5
2205	VSSDUMMY	-183.6425	487.5
2206	VSSDUMMY	-184.37	327.5
2207	VSSDUMMY	-216.1725	647.5
2208	VSSDUMMY	-217.0325	487.5
2209	VSSDUMMY	-217.8925	327.5
2210	VSSDUMMY	-249.43	647.5
2211	VSSDUMMY	-250.4225	487.5
2212	VSSDUMMY	-251.4125	327.5
2213	VSSDUMMY	-282.6875	647.5
2214	VSSDUMMY	-283.8125	487.5
2215	VSSDUMMY	-284.935	327.5
2216	VSSDUMMY	-315.945	647.5
2217	VSSDUMMY	-317.2025	487.5
2218	VSSDUMMY	-318.4575	327.5
2219	VSSDUMMY	-349.2025	647.5
2220	VSSDUMMY	-350.5925	487.5
2221	VSSDUMMY	-351.98	327.5
2222	VSSDUMMY	-382.46	647.5
2223	VSSDUMMY	-383.98	487.5
2224	VSSDUMMY	-385.5	327.5
2225	VSSDUMMY	-415.7175	647.5
2226	VSSDUMMY	-417.37	487.5
2227	VSSDUMMY	-419.0225	327.5
2228	VSSDUMMY	-448.975	647.5
2229	VSSDUMMY	-450.76	487.5
2230	VSSDUMMY	-452.545	327.5
2231	VSSDUMMY	-482.2325	647.5

2232	VSSDUMMY	-484.15	487.5
2233	VSSDUMMY	-486.065	327.5
2234	VSSDUMMY	-515.49	647.5
2235	VSSDUMMY	-517.54	487.5
2236	VSSDUMMY	-519.5875	327.5
2237	VSSDUMMY	-548.7475	647.5
2238	VSSDUMMY	-550.93	487.5
2239	VSSDUMMY	-553.11	327.5
2240	VSSDUMMY	-582.005	647.5
2241	VSSDUMMY	-584.32	487.5
2242	VSSDUMMY	-586.6325	327.5
2243	VSSDUMMY	-615.2625	647.5
2244	VSSDUMMY	-617.7075	487.5
2245	VSSDUMMY	-620.1525	327.5
2246	VSSDUMMY	-648.52	647.5
2247	VSSDUMMY	-651.0975	487.5
2248	VSSDUMMY	-653.675	327.5
2249	VSSDUMMY	-681.7775	647.5
2250	VSSDUMMY	-684.4875	487.5
2251	VSSDUMMY	-687.1975	327.5
2252	VSSDUMMY	-715.035	647.5
2253	VSSDUMMY	-717.8775	487.5
2254	VSSDUMMY	-720.72	327.5
2255	S<1281>	-748.2925	647.5
2256	S<1282>	-751.2675	487.5
2257	VSSDUMMY	-754.24	327.5
2258	S<1283>	-781.55	647.5
2259	S<1284>	-784.6575	487.5
2260	S<1285>	-787.7625	327.5
2261	S<1286>	-814.8075	647.5
2262	S<1287>	-818.0475	487.5
2263	S<1288>	-821.285	327.5
2264	S<1289>	-848.065	647.5
2265	S<1290>	-851.435	487.5
2266	S<1291>	-854.805	327.5
2267	S<1292>	-881.3225	647.5
2268	S<1293>	-884.825	487.5
2269	S<1294>	-888.3275	327.5
2270	S<1295>	-914.58	647.5
2271	S<1296>	-918.215	487.5

2272	S<1297>	-921.85	327.5
2273	S<1298>	-947.8375	647.5
2274	S<1299>	-951.605	487.5
2275	S<1300>	-955.3725	327.5
2276	S<1301>	-981.095	647.5
2277	S<1302>	-984.995	487.5
2278	S<1303>	-988.8925	327.5
2279	S<1304>	-1014.3525	647.5
2280	S<1305>	-1018.385	487.5
2281	S<1306>	-1022.415	327.5
2282	S<1307>	-1047.61	647.5
2283	S<1308>	-1051.775	487.5
2284	S<1309>	-1055.9375	327.5
2285	S<1310>	-1080.8675	647.5
2286	S<1311>	-1085.1625	487.5
2287	S<1312>	-1089.4575	327.5
2288	S<1313>	-1114.125	647.5
2289	S<1314>	-1118.5525	487.5
2290	S<1315>	-1122.98	327.5
2291	S<1316>	-1147.3825	647.5
2292	S<1317>	-1151.9425	487.5
2293	S<1318>	-1156.5025	327.5
2294	S<1319>	-1180.64	647.5
2295	S<1320>	-1185.3325	487.5
2296	S<1321>	-1190.025	327.5
2297	S<1322>	-1213.8975	647.5
2298	S<1323>	-1218.7225	487.5
2299	S<1324>	-1223.545	327.5
2300	S<1325>	-1247.155	647.5
2301	S<1326>	-1252.1125	487.5
2302	S<1327>	-1257.0675	327.5
2303	S<1328>	-1280.4125	647.5
2304	S<1329>	-1285.5025	487.5
2305	S<1330>	-1290.59	327.5
2306	S<1331>	-1313.67	647.5
2307	S<1332>	-1318.89	487.5
2308	S<1333>	-1324.11	327.5
2309	S<1334>	-1346.9275	647.5
2310	S<1335>	-1352.28	487.5
2311	S<1336>	-1357.6325	327.5

2312	S<1337>	-1380.185	647.5
2313	S<1338>	-1385.67	487.5
2314	S<1339>	-1391.155	327.5
2315	S<1340>	-1413.4425	647.5
2316	S<1341>	-1419.06	487.5
2317	S<1342>	-1424.6775	327.5
2318	S<1343>	-1446.7	647.5
2319	S<1344>	-1452.45	487.5
2320	S<1345>	-1458.1975	327.5
2321	S<1346>	-1479.9575	647.5
2322	S<1347>	-1485.84	487.5
2323	S<1348>	-1491.72	327.5
2324	S<1349>	-1513.215	647.5
2325	S<1350>	-1519.23	487.5
2326	S<1351>	-1525.2425	327.5
2327	S<1352>	-1546.4725	647.5
2328	S<1353>	-1552.6175	487.5
2329	S<1354>	-1558.7625	327.5
2330	S<1355>	-1579.73	647.5
2331	S<1356>	-1586.0075	487.5
2332	S<1357>	-1592.285	327.5
2333	S<1358>	-1612.9875	647.5
2334	S<1359>	-1619.3975	487.5
2335	S<1360>	-1625.8075	327.5
2336	S<1361>	-1646.245	647.5
2337	S<1362>	-1652.7875	487.5
2338	S<1363>	-1659.33	327.5
2339	S<1364>	-1679.5025	647.5
2340	S<1365>	-1686.1775	487.5
2341	S<1366>	-1692.85	327.5
2342	S<1367>	-1712.76	647.5
2343	S<1368>	-1719.5675	487.5
2344	S<1369>	-1726.3725	327.5
2345	S<1370>	-1746.0175	647.5
2346	S<1371>	-1752.9575	487.5
2347	S<1372>	-1759.895	327.5
2348	S<1373>	-1779.275	647.5
2349	S<1374>	-1786.345	487.5
2350	S<1375>	-1793.415	327.5
2351	S<1376>	-1812.5325	647.5

2352	S<1377>	-1819.735	487.5
2353	S<1378>	-1826.9375	327.5
2354	S<1379>	-1845.79	647.5
2355	S<1380>	-1853.125	487.5
2356	S<1381>	-1860.46	327.5
2357	S<1382>	-1879.0475	647.5
2358	S<1383>	-1886.515	487.5
2359	S<1384>	-1893.9825	327.5
2360	S<1385>	-1912.305	647.5
2361	S<1386>	-1919.905	487.5
2362	S<1387>	-1927.505	327.5
2363	S<1388>	-1945.5625	647.5
2364	S<1389>	-1953.295	487.5
2365	S<1390>	-1961.025	327.5
2366	S<1391>	-1978.82	647.5
2367	S<1392>	-1986.685	487.5
2368	S<1393>	-1994.5475	327.5
2369	S<1394>	-2012.0775	647.5
2370	S<1395>	-2020.0725	487.5
2371	S<1396>	-2028.0675	327.5
2372	S<1397>	-2045.335	647.5
2373	S<1398>	-2053.4625	487.5
2374	S<1399>	-2061.59	327.5
2375	S<1400>	-2078.5925	647.5
2376	S<1401>	-2086.8525	487.5
2377	S<1402>	-2095.1125	327.5
2378	S<1403>	-2111.85	647.5
2379	S<1404>	-2120.2425	487.5
2380	S<1405>	-2128.635	327.5
2381	S<1406>	-2145.1075	647.5
2382	S<1407>	-2153.6325	487.5
2383	S<1408>	-2162.1575	327.5
2384	S<1409>	-2178.365	647.5
2385	S<1410>	-2187.02	487.5
2386	S<1411>	-2195.6775	327.5
2387	S<1412>	-2211.6225	647.5
2388	S<1413>	-2220.4125	487.5
2389	S<1414>	-2229.2	327.5
2390	S<1415>	-2244.88	647.5
2391	S<1416>	-2253.8	487.5

2392	S<1417>	-2262.72	327.5
2393	S<1418>	-2278.1375	647.5
2394	S<1419>	-2287.19	487.5
2395	S<1420>	-2296.2425	327.5
2396	S<1421>	-2311.395	647.5
2397	S<1422>	-2320.58	487.5
2398	S<1423>	-2329.765	327.5
2399	S<1424>	-2344.6525	647.5
2400	S<1425>	-2353.97	487.5
2401	S<1426>	-2363.2875	327.5
2402	S<1427>	-2377.91	647.5
2403	S<1428>	-2387.36	487.5
2404	S<1429>	-2396.81	327.5
2405	S<1430>	-2411.1675	647.5
2406	S<1431>	-2420.7475	487.5
2407	S<1432>	-2430.33	327.5
2408	S<1433>	-2444.425	647.5
2409	S<1434>	-2454.14	487.5
2410	S<1435>	-2463.8525	327.5
2411	S<1436>	-2477.6825	647.5
2412	S<1437>	-2487.5275	487.5
2413	S<1438>	-2497.3725	327.5
2414	S<1439>	-2510.94	647.5
2415	S<1440>	-2520.92	487.5
2416	S<1441>	-2530.895	327.5
2417	S<1442>	-2544.1975	647.5
2418	S<1443>	-2554.3075	487.5
2419	S<1444>	-2564.4175	327.5
2420	S<1445>	-2577.455	647.5
2421	S<1446>	-2587.6975	487.5
2422	S<1447>	-2597.94	327.5
2423	S<1448>	-2610.7125	647.5
2424	S<1449>	-2621.0875	487.5
2425	S<1450>	-2631.4625	327.5
2426	S<1451>	-2643.97	647.5
2427	S<1452>	-2654.475	487.5
2428	S<1453>	-2664.9825	327.5
2429	S<1454>	-2677.2275	647.5
2430	S<1455>	-2687.8675	487.5
2431	S<1456>	-2698.505	327.5

2432	S<1457>	-2710.485	647.5
2433	S<1458>	-2721.255	487.5
2434	S<1459>	-2732.025	327.5
2435	S<1460>	-2743.7425	647.5
2436	S<1461>	-2754.6475	487.5
2437	S<1462>	-2765.5475	327.5
2438	S<1463>	-2777	647.5
2439	S<1464>	-2788.035	487.5
2440	S<1465>	-2799.07	327.5
2441	S<1466>	-2810.2575	647.5
2442	S<1467>	-2821.425	487.5
2443	S<1468>	-2832.5925	327.5
2444	S<1469>	-2843.515	647.5
2445	S<1470>	-2854.815	487.5
2446	S<1471>	-2866.115	327.5
2447	S<1472>	-2876.7725	647.5
2448	S<1473>	-2888.2025	487.5
2449	S<1474>	-2899.635	327.5
2450	S<1475>	-2910.03	647.5
2451	S<1476>	-2921.595	487.5
2452	S<1477>	-2933.1575	327.5
2453	S<1478>	-2943.2875	647.5
2454	S<1479>	-2954.9825	487.5
2455	S<1480>	-2966.6775	327.5
2456	S<1481>	-2976.545	647.5
2457	S<1482>	-2988.375	487.5
2458	S<1483>	-3000.2	327.5
2459	S<1484>	-3009.8025	647.5
2460	S<1485>	-3021.7625	487.5
2461	S<1486>	-3033.7225	327.5
2462	S<1487>	-3043.06	647.5
2463	S<1488>	-3055.1525	487.5
2464	S<1489>	-3067.245	327.5
2465	S<1490>	-3076.3175	647.5
2466	S<1491>	-3088.5425	487.5
2467	S<1492>	-3100.7675	327.5
2468	S<1493>	-3109.575	647.5
2469	S<1494>	-3121.93	487.5
2470	S<1495>	-3134.29	327.5
2471	S<1496>	-3142.8325	647.5

2472	S<1497>	-3155.3225	487.5
2473	S<1498>	-3167.81	327.5
2474	S<1499>	-3176.09	647.5
2475	S<1500>	-3188.71	487.5
2476	S<1501>	-3201.33	327.5
2477	S<1502>	-3209.3475	647.5
2478	S<1503>	-3222.1025	487.5
2479	S<1504>	-3234.8525	327.5
2480	S<1505>	-3242.605	647.5
2481	S<1506>	-3255.49	487.5
2482	S<1507>	-3268.375	327.5
2483	S<1508>	-3275.8625	647.5
2484	S<1509>	-3288.88	487.5
2485	S<1510>	-3301.8975	327.5
2486	S<1511>	-3309.12	647.5
2487	S<1512>	-3322.27	487.5
2488	S<1513>	-3335.42	327.5
2489	S<1514>	-3342.3775	647.5
2490	S<1515>	-3355.6575	487.5
2491	S<1516>	-3368.9425	327.5
2492	S<1517>	-3375.635	647.5
2493	S<1518>	-3389.05	487.5
2494	S<1519>	-3402.4625	327.5
2495	S<1520>	-3408.8925	647.5
2496	S<1521>	-3422.4375	487.5
2497	S<1522>	-3435.9825	327.5
2498	S<1523>	-3442.15	647.5
2499	S<1524>	-3455.83	487.5
2500	S<1525>	-3469.505	327.5
2501	S<1526>	-3475.4075	647.5
2502	S<1527>	-3489.2175	487.5
2503	S<1528>	-3503.0275	327.5
2504	S<1529>	-3508.665	647.5
2505	S<1530>	-3522.6075	487.5
2506	S<1531>	-3536.55	327.5
2507	S<1532>	-3541.9225	647.5
2508	S<1533>	-3555.9975	487.5
2509	S<1534>	-3570.0725	327.5
2510	S<1535>	-3575.18	647.5
2511	S<1536>	-3589.385	487.5

2512	S<1537>	-3603.595	327.5
2513	S<1538>	-3608.4375	647.5
2514	S<1539>	-3622.7775	487.5
2515	S<1540>	-3637.115	327.5
2516	S<1541>	-3641.695	647.5
2517	S<1542>	-3656.165	487.5
2518	S<1543>	-3670.635	327.5
2519	S<1544>	-3674.9525	647.5
2520	S<1545>	-3689.5575	487.5
2521	S<1546>	-3704.1575	327.5
2522	S<1547>	-3708.21	647.5
2523	S<1548>	-3722.945	487.5
2524	S<1549>	-3737.68	327.5
2525	S<1550>	-3741.4675	647.5
2526	S<1551>	-3756.335	487.5
2527	S<1552>	-3771.2025	327.5
2528	S<1553>	-3774.725	647.5
2529	S<1554>	-3789.725	487.5
2530	S<1555>	-3804.725	327.5
2531	S<1556>	-3807.9825	647.5
2532	S<1557>	-3823.1125	487.5
2533	S<1558>	-3838.2475	327.5
2534	S<1559>	-3841.24	647.5
2535	S<1560>	-3856.505	487.5
2536	S<1561>	-3871.7675	327.5
2537	S<1562>	-3874.4975	647.5
2538	S<1563>	-3889.8925	487.5
2539	S<1564>	-3905.2875	327.5
2540	S<1565>	-3907.755	647.5
2541	S<1566>	-3923.285	487.5
2542	S<1567>	-3938.81	327.5
2543	S<1568>	-3941.0125	647.5
2544	S<1569>	-3956.6725	487.5
2545	S<1570>	-3972.3325	327.5
2546	S<1571>	-3974.27	647.5
2547	S<1572>	-3990.0625	487.5
2548	S<1573>	-4005.855	327.5
2549	S<1574>	-4007.5275	647.5
2550	S<1575>	-4023.4525	487.5
2551	S<1576>	-4039.3775	327.5

2552	S<1577>	-4040.785	647.5
2553	S<1578>	-4056.84	487.5
2554	S<1579>	-4072.9	327.5
2555	S<1580>	-4074.0425	647.5
2556	S<1581>	-4090.2325	487.5
2557	S<1582>	-4106.42	327.5
2558	S<1583>	-4107.3	647.5
2559	S<1584>	-4123.62	487.5
2560	S<1585>	-4139.94	327.5
2561	S<1586>	-4140.5575	647.5
2562	S<1587>	-4157.0125	487.5
2563	S<1588>	-4173.4625	327.5
2564	S<1589>	-4173.815	647.5
2565	S<1590>	-4190.4	487.5
2566	S<1591>	-4206.985	327.5
2567	S<1592>	-4207.0725	647.5
2568	S<1593>	-4223.79	487.5
2569	S<1594>	-4240.5075	327.5
2570	S<1595>	-4240.33	647.5
2571	S<1596>	-4257.18	487.5
2572	S<1597>	-4274.03	327.5
2573	S<1598>	-4273.5875	647.5
2574	S<1599>	-4290.5675	487.5
2575	S<1600>	-4307.5525	327.5
2576	S<1601>	-4306.845	647.5
2577	S<1602>	-4323.96	487.5
2578	S<1603>	-4341.075	327.5
2579	S<1604>	-4340.1025	647.5
2580	S<1605>	-4357.3475	487.5
2581	S<1606>	-4374.5925	327.5
2582	S<1607>	-4373.36	647.5
2583	S<1608>	-4390.74	487.5
2584	S<1609>	-4408.115	327.5
2585	S<1610>	-4406.6175	647.5
2586	S<1611>	-4424.1275	487.5
2587	S<1612>	-4441.6375	327.5
2588	S<1613>	-4439.875	647.5
2589	S<1614>	-4457.5175	487.5
2590	S<1615>	-4475.16	327.5
2591	S<1616>	-4473.1325	647.5

2592	S<1617>	-4490.9075	487.5
2593	S<1618>	-4508.6825	327.5
2594	S<1619>	-4506.39	647.5
2595	S<1620>	-4524.295	487.5
2596	S<1621>	-4542.205	327.5
2597	S<1622>	-4539.6475	647.5
2598	S<1623>	-4557.6875	487.5
2599	S<1624>	-4575.7275	327.5
2600	S<1625>	-4572.905	647.5
2601	S<1626>	-4591.075	487.5
2602	S<1627>	-4609.245	327.5
2603	S<1628>	-4606.1625	647.5
2604	S<1629>	-4624.4675	487.5
2605	S<1630>	-4642.7675	327.5
2606	S<1631>	-4639.42	647.5
2607	S<1632>	-4657.855	487.5
2608	S<1633>	-4676.29	327.5
2609	S<1634>	-4672.6775	647.5
2610	S<1635>	-4691.245	487.5
2611	S<1636>	-4709.8125	327.5
2612	S<1637>	-4705.935	647.5
2613	S<1638>	-4724.635	487.5
2614	S<1639>	-4743.335	327.5
2615	S<1640>	-4739.1925	647.5
2616	S<1641>	-4758.0225	487.5
2617	S<1642>	-4776.8575	327.5
2618	S<1643>	-4772.45	647.5
2619	S<1644>	-4791.415	487.5
2620	S<1645>	-4810.38	327.5
2621	S<1646>	-4805.7075	647.5
2622	S<1647>	-4824.8025	487.5
2623	S<1648>	-4843.8975	327.5
2624	S<1649>	-4838.965	647.5
2625	S<1650>	-4858.195	487.5
2626	S<1651>	-4877.42	327.5
2627	S<1652>	-4872.2225	647.5
2628	S<1653>	-4891.5825	487.5
2629	S<1654>	-4910.9425	327.5
2630	S<1655>	-4905.48	647.5
2631	S<1656>	-4924.9725	487.5

2632	S<1657>	-4944.465	327.5
2633	S<1658>	-4938.7375	647.5
2634	S<1659>	-4958.3625	487.5
2635	S<1660>	-4977.9875	327.5
2636	S<1661>	-4971.995	647.5
2637	S<1662>	-4991.75	487.5
2638	S<1663>	-5011.51	327.5
2639	S<1664>	-5005.2525	647.5
2640	S<1665>	-5025.1425	487.5
2641	S<1666>	-5045.0325	327.5
2642	S<1667>	-5038.51	647.5
2643	S<1668>	-5058.53	487.5
2644	S<1669>	-5078.55	327.5
2645	S<1670>	-5071.7675	647.5
2646	S<1671>	-5091.9225	487.5
2647	S<1672>	-5112.0725	327.5
2648	S<1673>	-5105.025	647.5
2649	S<1674>	-5125.31	487.5
2650	S<1675>	-5145.595	327.5
2651	S<1676>	-5138.2825	647.5
2652	S<1677>	-5158.7025	487.5
2653	S<1678>	-5179.1175	327.5
2654	S<1679>	-5171.54	647.5
2655	S<1680>	-5192.09	487.5
2656	S<1681>	-5212.64	327.5
2657	S<1682>	-5204.7975	647.5
2658	S<1683>	-5225.4775	487.5
2659	S<1684>	-5246.1625	327.5
2660	S<1685>	-5238.055	647.5
2661	S<1686>	-5258.87	487.5
2662	S<1687>	-5279.685	327.5
2663	S<1688>	-5271.3125	647.5
2664	S<1689>	-5292.2575	487.5
2665	S<1690>	-5313.2025	327.5
2666	S<1691>	-5304.57	647.5
2667	S<1692>	-5325.65	487.5
2668	S<1693>	-5346.725	327.5
2669	S<1694>	-5337.8275	647.5
2670	S<1695>	-5359.0375	487.5
2671	S<1696>	-5380.2475	327.5

2672	S<1697>	-5371.085	647.5
2673	S<1698>	-5392.43	487.5
2674	S<1699>	-5413.77	327.5
2675	S<1700>	-5404.3425	647.5
2676	S<1701>	-5425.8175	487.5
2677	S<1702>	-5447.2925	327.5
2678	S<1703>	-5437.6	647.5
2679	S<1704>	-5459.205	487.5
2680	S<1705>	-5480.815	327.5
2681	S<1706>	-5470.8575	647.5
2682	S<1707>	-5492.5975	487.5
2683	S<1708>	-5514.3375	327.5
2684	S<1709>	-5504.115	647.5
2685	S<1710>	-5525.985	487.5
2686	S<1711>	-5547.855	327.5
2687	S<1712>	-5537.3725	647.5
2688	S<1713>	-5559.3775	487.5
2689	S<1714>	-5581.3775	327.5
2690	S<1715>	-5570.63	647.5
2691	S<1716>	-5592.765	487.5
2692	S<1717>	-5614.9	327.5
2693	S<1718>	-5603.8875	647.5
2694	S<1719>	-5626.1575	487.5
2695	S<1720>	-5648.4225	327.5
2696	S<1721>	-5637.145	647.5
2697	S<1722>	-5659.545	487.5
2698	S<1723>	-5681.945	327.5
2699	S<1724>	-5670.4025	647.5
2700	S<1725>	-5692.9325	487.5
2701	S<1726>	-5715.4675	327.5
2702	S<1727>	-5703.66	647.5
2703	S<1728>	-5726.325	487.5
2704	S<1729>	-5748.99	327.5
2705	S<1730>	-5736.9175	647.5
2706	S<1731>	-5759.7125	487.5
2707	S<1732>	-5782.51	327.5
2708	S<1733>	-5770.175	647.5
2709	S<1734>	-5793.105	487.5
2710	S<1735>	-5816.03	327.5
2711	S<1736>	-5803.4325	647.5

2712	S<1737>	-5826.4925	487.5
2713	S<1738>	-5849.5525	327.5
2714	S<1739>	-5836.69	647.5
2715	S<1740>	-5859.885	487.5
2716	S<1741>	-5883.075	327.5
2717	S<1742>	-5869.9475	647.5
2718	S<1743>	-5893.2725	487.5
2719	S<1744>	-5916.5975	327.5
2720	S<1745>	-5903.205	647.5
2721	S<1746>	-5926.66	487.5
2722	S<1747>	-5950.12	327.5
2723	S<1748>	-5936.4625	647.5
2724	S<1749>	-5960.0525	487.5
2725	S<1750>	-5983.6425	327.5
2726	S<1751>	-5969.72	647.5
2727	S<1752>	-5993.44	487.5
2728	S<1753>	-6017.1625	327.5
2729	S<1754>	-6002.9775	647.5
2730	S<1755>	-6026.8325	487.5
2731	S<1756>	-6050.6825	327.5
2732	S<1757>	-6036.235	647.5
2733	S<1758>	-6060.22	487.5
2734	S<1759>	-6084.205	327.5
2735	S<1760>	-6069.4925	647.5
2736	S<1761>	-6093.6125	487.5
2737	S<1762>	-6117.7275	327.5
2738	S<1763>	-6102.75	647.5
2739	S<1764>	-6127	487.5
2740	S<1765>	-6151.25	327.5
2741	S<1766>	-6136.0075	647.5
2742	S<1767>	-6160.3875	487.5
2743	S<1768>	-6184.7725	327.5
2744	S<1769>	-6169.265	647.5
2745	S<1770>	-6193.78	487.5
2746	S<1771>	-6218.295	327.5
2747	S<1772>	-6202.5225	647.5
2748	S<1773>	-6227.1675	487.5
2749	S<1774>	-6251.8175	327.5
2750	S<1775>	-6235.78	647.5
2751	S<1776>	-6260.56	487.5

2752	S<1777>	-6285.335	327.5
2753	S<1778>	-6269.0375	647.5
2754	S<1779>	-6293.9475	487.5
2755	S<1780>	-6318.8575	327.5
2756	S<1781>	-6302.295	647.5
2757	S<1782>	-6327.3375	487.5
2758	S<1783>	-6352.38	327.5
2759	S<1784>	-6335.5525	647.5
2760	S<1785>	-6360.7275	487.5
2761	S<1786>	-6385.9025	327.5
2762	S<1787>	-6368.81	647.5
2763	S<1788>	-6394.115	487.5
2764	S<1789>	-6419.425	327.5
2765	S<1790>	-6402.0675	647.5
2766	S<1791>	-6427.5075	487.5
2767	S<1792>	-6452.9475	327.5
2768	S<1793>	-6435.325	647.5
2769	S<1794>	-6460.895	487.5
2770	S<1795>	-6486.47	327.5
2771	S<1796>	-6468.5825	647.5
2772	S<1797>	-6494.2875	487.5
2773	S<1798>	-6519.9875	327.5
2774	S<1799>	-6501.84	647.5
2775	S<1800>	-6527.675	487.5
2776	S<1801>	-6553.51	327.5
2777	S<1802>	-6535.0975	647.5
2778	S<1803>	-6561.065	487.5
2779	S<1804>	-6587.0325	327.5
2780	S<1805>	-6568.355	647.5
2781	S<1806>	-6594.455	487.5
2782	S<1807>	-6620.555	327.5
2783	S<1808>	-6601.6125	647.5
2784	S<1809>	-6627.8425	487.5
2785	S<1810>	-6654.0775	327.5
2786	S<1811>	-6634.87	647.5
2787	S<1812>	-6661.235	487.5
2788	S<1813>	-6687.6	327.5
2789	S<1814>	-6668.1275	647.5
2790	S<1815>	-6694.6225	487.5
2791	S<1816>	-6721.1225	327.5

2792	S<1817>	-6701.385	647.5
2793	S<1818>	-6728.015	487.5
2794	S<1819>	-6754.64	327.5
2795	S<1820>	-6734.6425	647.5
2796	S<1821>	-6761.4025	487.5
2797	S<1822>	-6788.1625	327.5
2798	S<1823>	-6767.9	647.5
2799	S<1824>	-6794.7925	487.5
2800	S<1825>	-6821.685	327.5
2801	S<1826>	-6801.1575	647.5
2802	S<1827>	-6828.1825	487.5
2803	S<1828>	-6855.2075	327.5
2804	S<1829>	-6834.415	647.5
2805	S<1830>	-6861.57	487.5
2806	S<1831>	-6888.73	327.5
2807	S<1832>	-6867.6725	647.5
2808	S<1833>	-6894.9625	487.5
2809	S<1834>	-6922.2525	327.5
2810	S<1835>	-6900.93	647.5
2811	S<1836>	-6928.35	487.5
2812	S<1837>	-6955.775	327.5
2813	S<1838>	-6934.1875	647.5
2814	S<1839>	-6961.7425	487.5
2815	S<1840>	-6989.295	327.5
2816	S<1841>	-6967.445	647.5
2817	S<1842>	-6995.13	487.5
2818	S<1843>	-7022.815	327.5
2819	S<1844>	-7000.7025	647.5
2820	S<1845>	-7028.52	487.5
2821	S<1846>	-7056.3375	327.5
2822	S<1847>	-7033.96	647.5
2823	S<1848>	-7061.91	487.5
2824	S<1849>	-7089.86	327.5
2825	S<1850>	-7067.2175	647.5
2826	S<1851>	-7095.2975	487.5
2827	S<1852>	-7123.3825	327.5
2828	S<1853>	-7100.475	647.5
2829	S<1854>	-7128.69	487.5
2830	S<1855>	-7156.905	327.5
2831	S<1856>	-7133.7325	647.5

2832	S<1857>	-7162.0775	487.5
2833	S<1858>	-7190.4275	327.5
2834	S<1859>	-7166.99	647.5
2835	S<1860>	-7195.47	487.5
2836	S<1861>	-7223.9475	327.5
2837	S<1862>	-7200.2475	647.5
2838	S<1863>	-7228.8575	487.5
2839	S<1864>	-7257.4675	327.5
2840	S<1865>	-7233.505	647.5
2841	S<1866>	-7262.2475	487.5
2842	S<1867>	-7290.99	327.5
2843	S<1868>	-7266.7625	647.5
2844	S<1869>	-7295.6375	487.5
2845	S<1870>	-7324.5125	327.5
2846	S<1871>	-7300.02	647.5
2847	S<1872>	-7329.025	487.5
2848	S<1873>	-7358.035	327.5
2849	S<1874>	-7333.2775	647.5
2850	S<1875>	-7362.4175	487.5
2851	S<1876>	-7391.5575	327.5
2852	S<1877>	-7366.535	647.5
2853	S<1878>	-7395.805	487.5
2854	S<1879>	-7425.08	327.5
2855	S<1880>	-7399.7925	647.5
2856	S<1881>	-7429.1975	487.5
2857	S<1882>	-7458.6	327.5
2858	S<1883>	-7433.05	647.5
2859	S<1884>	-7462.585	487.5
2860	S<1885>	-7492.12	327.5
2861	S<1886>	-7466.3075	647.5
2862	S<1887>	-7495.975	487.5
2863	S<1888>	-7525.6425	327.5
2864	S<1889>	-7499.565	647.5
2865	S<1890>	-7529.365	487.5
2866	S<1891>	-7559.165	327.5
2867	S<1892>	-7532.8225	647.5
2868	S<1893>	-7562.755	487.5
2869	S<1894>	-7592.6875	327.5
2870	S<1895>	-7566.08	647.5
2871	S<1896>	-7596.145	487.5

2872	S<1897>	-7626.21	327.5
2873	S<1898>	-7599.3375	647.5
2874	S<1899>	-7629.5325	487.5
2875	S<1900>	-7659.7325	327.5
2876	S<1901>	-7632.595	647.5
2877	S<1902>	-7662.925	487.5
2878	S<1903>	-7693.2525	327.5
2879	S<1904>	-7665.8525	647.5
2880	S<1905>	-7696.3125	487.5
2881	S<1906>	-7726.7725	327.5
2882	S<1907>	-7699.11	647.5
2883	S<1908>	-7729.7025	487.5
2884	S<1909>	-7760.295	327.5
2885	S<1910>	-7732.3675	647.5
2886	S<1911>	-7763.0925	487.5
2887	S<1912>	-7793.8175	327.5
2888	S<1913>	-7765.625	647.5
2889	S<1914>	-7796.4825	487.5
2890	S<1915>	-7827.34	327.5
2891	S<1916>	-7798.8825	647.5
2892	S<1917>	-7829.8725	487.5
2893	S<1918>	-7860.8625	327.5
2894	S<1919>	-7832.14	647.5
2895	S<1920>	-7863.26	487.5
2896	S<1921>	-7894.385	327.5
2897	S<1922>	-7865.3975	647.5
2898	S<1923>	-7896.6525	487.5
2899	S<1924>	-7927.905	327.5
2900	S<1925>	-7898.655	647.5
2901	S<1926>	-7930.04	487.5
2902	S<1927>	-7961.425	327.5
2903	S<1928>	-7931.9125	647.5
2904	S<1929>	-7963.43	487.5
2905	S<1930>	-7994.9475	327.5
2906	S<1931>	-7965.17	647.5
2907	S<1932>	-7996.82	487.5
2908	S<1933>	-8028.47	327.5
2909	S<1934>	-7998.4275	647.5
2910	S<1935>	-8030.21	487.5
2911	S<1936>	-8061.9925	327.5

2912	S<1937>	-8031.685	647.5
2913	S<1938>	-8063.6	487.5
2914	S<1939>	-8095.515	327.5
2915	S<1940>	-8064.9425	647.5
2916	S<1941>	-8096.9875	487.5
2917	S<1942>	-8129.0375	327.5
2918	S<1943>	-8098.2	647.5
2919	S<1944>	-8130.38	487.5
2920	S<1945>	-8162.5575	327.5
2921	S<1946>	-8131.4575	647.5
2922	S<1947>	-8163.7675	487.5
2923	S<1948>	-8196.08	327.5
2924	S<1949>	-8164.715	647.5
2925	S<1950>	-8197.1575	487.5
2926	S<1951>	-8229.6	327.5
2927	S<1952>	-8197.9725	647.5
2928	S<1953>	-8230.5475	487.5
2929	S<1954>	-8263.1225	327.5
2930	S<1955>	-8231.23	647.5
2931	S<1956>	-8263.9375	487.5
2932	S<1957>	-8296.645	327.5
2933	S<1958>	-8264.4875	647.5
2934	S<1959>	-8297.3275	487.5
2935	S<1960>	-8330.1675	327.5
2936	S<1961>	-8297.745	647.5
2937	S<1962>	-8330.715	487.5
2938	S<1963>	-8363.69	327.5
2939	S<1964>	-8331.0025	647.5
2940	S<1965>	-8364.1075	487.5
2941	S<1966>	-8397.21	327.5
2942	S<1967>	-8364.26	647.5
2943	S<1968>	-8397.495	487.5
2944	S<1969>	-8430.7325	327.5
2945	S<1970>	-8397.5175	647.5
2946	S<1971>	-8430.885	487.5
2947	S<1972>	-8464.2525	327.5
2948	S<1973>	-8430.775	647.5
2949	S<1974>	-8464.275	487.5
2950	S<1975>	-8497.775	327.5
2951	S<1976>	-8464.0325	647.5

2952	S<1977>	-8497.665	487.5
2953	S<1978>	-8531.2975	327.5
2954	S<1979>	-8497.29	647.5
2955	S<1980>	-8531.055	487.5
2956	S<1981>	-8564.82	327.5
2957	S<1982>	-8530.5475	647.5
2958	S<1983>	-8564.4425	487.5
2959	S<1984>	-8598.3425	327.5
2960	S<1985>	-8563.805	647.5
2961	S<1986>	-8597.835	487.5
2962	S<1987>	-8631.8625	327.5
2963	S<1988>	-8597.0625	647.5
2964	S<1989>	-8631.2225	487.5
2965	S<1990>	-8665.385	327.5
2966	S<1991>	-8630.32	647.5
2967	S<1992>	-8664.6125	487.5
2968	S<1993>	-8698.905	327.5
2969	S<1994>	-8663.5775	647.5
2970	S<1995>	-8698.0025	487.5
2971	S<1996>	-8732.4275	327.5
2972	S<1997>	-8696.835	647.5
2973	S<1998>	-8731.3925	487.5
2974	S<1999>	-8765.95	327.5
2975	S<2000>	-8730.0925	647.5
2976	S<2001>	-8764.7825	487.5
2977	S<2002>	-8799.4725	327.5
2978	S<2003>	-8763.35	647.5
2979	S<2004>	-8798.17	487.5
2980	S<2005>	-8832.995	327.5
2981	S<2006>	-8796.6075	647.5
2982	S<2007>	-8831.5625	487.5
2983	S<2008>	-8866.515	327.5
2984	S<2009>	-8829.865	647.5
2985	S<2010>	-8864.95	487.5
2986	S<2011>	-8900.0375	327.5
2987	S<2012>	-8863.1225	647.5
2988	S<2013>	-8898.34	487.5
2989	S<2014>	-8933.5575	327.5
2990	S<2015>	-8896.38	647.5
2991	S<2016>	-8931.73	487.5

2992	S<2017>	-8967.08	327.5
2993	S<2018>	-8929.6375	647.5
2994	S<2019>	-8965.12	487.5
2995	S<2020>	-9000.6025	327.5
2996	S<2021>	-8962.895	647.5
2997	S<2022>	-8998.51	487.5
2998	S<2023>	-9034.125	327.5
2999	S<2024>	-8996.1525	647.5
3000	S<2025>	-9031.8975	487.5
3001	S<2026>	-9067.6475	327.5
3002	S<2027>	-9029.41	647.5
3003	S<2028>	-9065.29	487.5
3004	S<2029>	-9101.1675	327.5
3005	S<2030>	-9062.6675	647.5
3006	S<2031>	-9098.6775	487.5
3007	S<2032>	-9134.69	327.5
3008	S<2033>	-9095.925	647.5
3009	S<2034>	-9132.0675	487.5
3010	S<2035>	-9168.21	327.5
3011	S<2036>	-9129.1825	647.5
3012	S<2037>	-9165.4575	487.5
3013	S<2038>	-9201.7325	327.5
3014	S<2039>	-9162.44	647.5
3015	S<2040>	-9198.8475	487.5
3016	S<2041>	-9235.255	327.5
3017	S<2042>	-9195.6975	647.5
3018	S<2043>	-9232.2375	487.5
3019	S<2044>	-9268.7775	327.5
3020	S<2045>	-9228.955	647.5
3021	S<2046>	-9265.625	487.5
3022	S<2047>	-9302.3	327.5
3023	S<2048>	-9262.2125	647.5
3024	S<2049>	-9299.0175	487.5
3025	S<2050>	-9335.82	327.5
3026	S<2051>	-9295.47	647.5
3027	S<2052>	-9332.405	487.5
3028	S<2053>	-9369.3425	327.5
3029	S<2054>	-9328.7275	647.5
3030	S<2055>	-9365.795	487.5
3031	S<2056>	-9402.865	327.5

3032	S<2057>	-9361.985	647.5
3033	S<2058>	-9399.185	487.5
3034	S<2059>	-9436.385	327.5
3035	S<2060>	-9395.2425	647.5
3036	S<2061>	-9432.575	487.5
3037	S<2062>	-9469.9075	327.5
3038	S<2063>	-9428.5	647.5
3039	S<2064>	-9465.965	487.5
3040	S<2065>	-9503.43	327.5
3041	S<2066>	-9461.7575	647.5
3042	S<2067>	-9499.3525	487.5
3043	S<2068>	-9536.9525	327.5
3044	S<2069>	-9495.015	647.5
3045	S<2070>	-9532.745	487.5
3046	S<2071>	-9570.4725	327.5
3047	S<2072>	-9528.2725	647.5
3048	S<2073>	-9566.1325	487.5
3049	S<2074>	-9603.995	327.5
3050	S<2075>	-9561.53	647.5
3051	S<2076>	-9599.5225	487.5
3052	S<2077>	-9637.5175	327.5
3053	S<2078>	-9594.7875	647.5
3054	S<2079>	-9632.9125	487.5
3055	S<2080>	-9671.0375	327.5
3056	S<2081>	-9628.045	647.5
3057	S<2082>	-9666.3025	487.5
3058	S<2083>	-9704.56	327.5
3059	S<2084>	-9661.3025	647.5
3060	S<2085>	-9699.6925	487.5
3061	S<2086>	-9738.0825	327.5
3062	S<2087>	-9694.56	647.5
3063	S<2088>	-9733.08	487.5
3064	S<2089>	-9771.605	327.5
3065	S<2090>	-9727.8175	647.5
3066	S<2091>	-9766.4725	487.5
3067	S<2092>	-9805.125	327.5
3068	S<2093>	-9761.075	647.5
3069	S<2094>	-9799.86	487.5
3070	S<2095>	-9838.6475	327.5
3071	S<2096>	-9794.3325	647.5

3072	S<2097>	-9833.25	487.5
3073	S<2098>	-9872.17	327.5
3074	S<2099>	-9827.59	647.5
3075	S<2100>	-9866.64	487.5
3076	S<2101>	-9905.69	327.5
3077	S<2102>	-9860.8475	647.5
3078	S<2103>	-9900.03	487.5
3079	S<2104>	-9939.2125	327.5
3080	S<2105>	-9894.105	647.5
3081	S<2106>	-9933.42	487.5
3082	S<2107>	-9972.735	327.5
3083	S<2108>	-9927.3625	647.5
3084	S<2109>	-9966.81	487.5
3085	S<2110>	-10006.2575	327.5
3086	S<2111>	-9960.62	647.5
3087	S<2112>	-10000.2	487.5
3088	S<2113>	-10039.7775	327.5
3089	S<2114>	-9993.8775	647.5
3090	S<2115>	-10033.5875	487.5
3091	S<2116>	-10073.3	327.5
3092	S<2117>	-10027.135	647.5
3093	S<2118>	-10066.9775	487.5
3094	S<2119>	-10106.8225	327.5
3095	S<2120>	-10060.3925	647.5
3096	S<2121>	-10100.3675	487.5
3097	S<2122>	-10140.3425	327.5
3098	S<2123>	-10093.65	647.5
3099	S<2124>	-10133.7575	487.5
3100	S<2125>	-10173.865	327.5
3101	S<2126>	-10126.9075	647.5
3102	S<2127>	-10167.1475	487.5
3103	S<2128>	-10207.3875	327.5
3104	S<2129>	-10160.165	647.5
3105	S<2130>	-10200.5375	487.5
3106	S<2131>	-10240.91	327.5
3107	S<2132>	-10193.4225	647.5
3108	S<2133>	-10233.9275	487.5
3109	S<2134>	-10274.43	327.5
3110	S<2135>	-10226.68	647.5
3111	S<2136>	-10267.315	487.5

3112	S<2137>	-10307.9525	327.5
3113	S<2138>	-10259.9375	647.5
3114	S<2139>	-10300.705	487.5
3115	S<2140>	-10341.475	327.5
3116	S<2141>	-10293.195	647.5
3117	S<2142>	-10334.095	487.5
3118	S<2143>	-10374.995	327.5
3119	S<2144>	-10326.4525	647.5
3120	S<2145>	-10367.485	487.5
3121	S<2146>	-10408.5175	327.5
3122	S<2147>	-10359.71	647.5
3123	S<2148>	-10400.875	487.5
3124	S<2149>	-10442.04	327.5
3125	S<2150>	-10392.9675	647.5
3126	S<2151>	-10434.265	487.5
3127	S<2152>	-10475.5625	327.5
3128	S<2153>	-10426.225	647.5
3129	S<2154>	-10467.6525	487.5
3130	S<2155>	-10509.0825	327.5
3131	S<2156>	-10459.4825	647.5
3132	S<2157>	-10501.0425	487.5
3133	S<2158>	-10542.605	327.5
3134	S<2159>	-10492.74	647.5
3135	S<2160>	-10534.4325	487.5
3136	S<2161>	-10576.1275	327.5
3137	S<2162>	-10525.9975	647.5
3138	S<2163>	-10567.8225	487.5
3139	S<2164>	-10609.65	327.5
3140	S<2165>	-10559.255	647.5
3141	S<2166>	-10601.2125	487.5
3142	S<2167>	-10643.17	327.5
3143	S<2168>	-10592.5125	647.5
3144	S<2169>	-10634.6025	487.5
3145	S<2170>	-10676.6925	327.5
3146	S<2171>	-10625.77	647.5
3147	S<2172>	-10667.9925	487.5
3148	S<2173>	-10710.215	327.5
3149	S<2174>	-10659.0275	647.5
3150	S<2175>	-10701.38	487.5
3151	S<2176>	-10743.735	327.5

3152	S<2177>	-10692.285	647.5
3153	S<2178>	-10734.77	487.5
3154	S<2179>	-10777.2575	327.5
3155	S<2180>	-10725.5425	647.5
3156	S<2181>	-10768.16	487.5
3157	S<2182>	-10810.78	327.5
3158	S<2183>	-10758.8	647.5
3159	S<2184>	-10801.55	487.5
3160	S<2185>	-10844.3025	327.5
3161	S<2186>	-10792.0575	647.5
3162	S<2187>	-10834.94	487.5
3163	S<2188>	-10877.8225	327.5
3164	S<2189>	-10825.3125	647.5
3165	S<2190>	-10868.33	487.5
3166	S<2191>	-10911.345	327.5
3167	S<2192>	-10858.57	647.5
3168	S<2193>	-10901.72	487.5
3169	S<2194>	-10944.8675	327.5
3170	S<2195>	-10891.8275	647.5
3171	S<2196>	-10935.1075	487.5
3172	S<2197>	-10978.3875	327.5
3173	S<2198>	-10925.085	647.5
3174	S<2199>	-10968.4975	487.5
3175	S<2200>	-11011.91	327.5
3176	S<2201>	-10958.3425	647.5
3177	S<2202>	-11001.8875	487.5
3178	S<2203>	-11045.4325	327.5
3179	S<2204>	-10991.6	647.5
3180	S<2205>	-11035.2775	487.5
3181	S<2206>	-11078.955	327.5
3182	S<2207>	-11024.8575	647.5
3183	S<2208>	-11068.6675	487.5
3184	S<2209>	-11112.475	327.5
3185	S<2210>	-11058.115	647.5
3186	S<2211>	-11102.0575	487.5
3187	S<2212>	-11145.9975	327.5
3188	S<2213>	-11091.3725	647.5
3189	S<2214>	-11135.4475	487.5
3190	S<2215>	-11179.52	327.5
3191	S<2216>	-11124.63	647.5

3192	S<2217>	-11168.835	487.5
3193	S<2218>	-11213.04	327.5
3194	S<2219>	-11157.8875	647.5
3195	S<2220>	-11202.225	487.5
3196	S<2221>	-11246.5625	327.5
3197	S<2222>	-11191.145	647.5
3198	S<2223>	-11235.615	487.5
3199	S<2224>	-11280.085	327.5
3200	S<2225>	-11224.4025	647.5
3201	S<2226>	-11269.005	487.5
3202	S<2227>	-11313.6075	327.5
3203	S<2228>	-11257.66	647.5
3204	S<2229>	-11302.395	487.5
3205	S<2230>	-11347.1275	327.5
3206	S<2231>	-11290.9175	647.5
3207	S<2232>	-11335.785	487.5
3208	S<2233>	-11380.65	327.5
3209	S<2234>	-11324.175	647.5
3210	S<2235>	-11369.175	487.5
3211	S<2236>	-11414.1725	327.5
3212	S<2237>	-11357.4325	647.5
3213	S<2238>	-11402.5625	487.5
3214	S<2239>	-11447.6925	327.5
3215	S<2240>	-11390.69	647.5
3216	S<2241>	-11435.9525	487.5
3217	S<2242>	-11481.215	327.5
3218	S<2243>	-11423.9475	647.5
3219	S<2244>	-11469.3425	487.5
3220	S<2245>	-11514.7375	327.5
3221	S<2246>	-11457.205	647.5
3222	S<2247>	-11502.7325	487.5
3223	S<2248>	-11548.26	327.5
3224	S<2249>	-11490.4625	647.5
3225	S<2250>	-11536.1225	487.5
3226	S<2251>	-11581.78	327.5
3227	S<2252>	-11523.72	647.5
3228	S<2253>	-11569.5125	487.5
3229	S<2254>	-11615.3025	327.5
3230	S<2255>	-11556.9775	647.5
3231	S<2256>	-11602.9025	487.5

3232	S<2257>	-11648.825	327.5
3233	S<2258>	-11590.235	647.5
3234	S<2259>	-11636.29	487.5
3235	S<2260>	-11682.345	327.5
3236	S<2261>	-11623.4925	647.5
3237	S<2262>	-11669.68	487.5
3238	S<2263>	-11715.8675	327.5
3239	S<2264>	-11656.75	647.5
3240	S<2265>	-11703.07	487.5
3241	S<2266>	-11749.39	327.5
3242	S<2267>	-11690.0075	647.5
3243	S<2268>	-11736.46	487.5
3244	S<2269>	-11782.9125	327.5
3245	S<2270>	-11723.265	647.5
3246	S<2271>	-11769.85	487.5
3247	S<2272>	-11816.435	327.5
3248	S<2273>	-11756.5225	647.5
3249	S<2274>	-11803.24	487.5
3250	S<2275>	-11849.955	327.5
3251	S<2276>	-11789.78	647.5
3252	S<2277>	-11836.63	487.5
3253	S<2278>	-11883.4775	327.5
3254	S<2279>	-11823.0375	647.5
3255	S<2280>	-11870.0175	487.5
3256	S<2281>	-11916.9975	327.5
3257	S<2282>	-11856.295	647.5
3258	S<2283>	-11903.4075	487.5
3259	S<2284>	-11950.52	327.5
3260	S<2285>	-11889.5525	647.5
3261	S<2286>	-11936.7975	487.5
3262	S<2287>	-11984.0425	327.5
3263	S<2288>	-11922.81	647.5
3264	S<2289>	-11970.1875	487.5
3265	S<2290>	-12017.565	327.5
3266	S<2291>	-11956.0675	647.5
3267	S<2292>	-12003.5775	487.5
3268	S<2293>	-12051.0875	327.5
3269	S<2294>	-11989.325	647.5
3270	S<2295>	-12036.9675	487.5
3271	S<2296>	-12084.6075	327.5

3272	S<2297>	-12022.5825	647.5
3273	S<2298>	-12070.3575	487.5
3274	S<2299>	-12118.13	327.5
3275	S<2300>	-12055.84	647.5
3276	S<2301>	-12103.745	487.5
3277	S<2302>	-12151.6525	327.5
3278	S<2303>	-12089.0975	647.5
3279	S<2304>	-12137.135	487.5
3280	S<2305>	-12185.1725	327.5
3281	S<2306>	-12122.355	647.5
3282	S<2307>	-12170.525	487.5
3283	S<2308>	-12218.695	327.5
3284	S<2309>	-12155.6125	647.5
3285	S<2310>	-12203.915	487.5
3286	S<2311>	-12252.2175	327.5
3287	S<2312>	-12188.87	647.5
3288	S<2313>	-12237.305	487.5
3289	S<2314>	-12285.74	327.5
3290	S<2315>	-12222.1275	647.5
3291	S<2316>	-12270.695	487.5
3292	S<2317>	-12319.26	327.5
3293	S<2318>	-12255.385	647.5
3294	S<2319>	-12304.085	487.5
3295	S<2320>	-12352.7825	327.5
3296	S<2321>	-12288.6425	647.5
3297	S<2322>	-12337.4725	487.5
3298	S<2323>	-12386.305	327.5
3299	S<2324>	-12321.9	647.5
3300	S<2325>	-12370.865	487.5
3301	S<2326>	-12419.825	327.5
3302	S<2327>	-12355.1575	647.5
3303	S<2328>	-12404.2525	487.5
3304	S<2329>	-12453.3475	327.5
3305	S<2330>	-12388.415	647.5
3306	S<2331>	-12437.6425	487.5
3307	S<2332>	-12486.87	327.5
3308	S<2333>	-12421.6725	647.5
3309	S<2334>	-12471.0325	487.5
3310	S<2335>	-12520.3925	327.5
3311	S<2336>	-12454.93	647.5

3312	S<2337>	-12504.4225	487.5
3313	S<2338>	-12553.9125	327.5
3314	S<2339>	-12488.1875	647.5
3315	S<2340>	-12537.8125	487.5
3316	S<2341>	-12587.435	327.5
3317	S<2342>	-12521.445	647.5
3318	S<2343>	-12571.2	487.5
3319	S<2344>	-12620.9575	327.5
3320	S<2345>	-12554.7025	647.5
3321	S<2346>	-12604.5925	487.5
3322	S<2347>	-12654.4775	327.5
3323	S<2348>	-12587.96	647.5
3324	S<2349>	-12637.98	487.5
3325	S<2350>	-12688	327.5
3326	S<2351>	-12621.2175	647.5
3327	S<2352>	-12671.37	487.5
3328	S<2353>	-12721.5225	327.5
3329	S<2354>	-12654.475	647.5
3330	S<2355>	-12704.76	487.5
3331	S<2356>	-12755.045	327.5
3332	S<2357>	-12687.7325	647.5
3333	S<2358>	-12738.15	487.5
3334	S<2359>	-12788.565	327.5
3335	S<2360>	-12720.99	647.5
3336	S<2361>	-12771.54	487.5
3337	S<2362>	-12822.0875	327.5
3338	S<2363>	-12754.2475	647.5
3339	S<2364>	-12804.9275	487.5
3340	S<2365>	-12855.61	327.5
3341	S<2366>	-12787.505	647.5
3342	S<2367>	-12838.32	487.5
3343	S<2368>	-12889.13	327.5
3344	S<2369>	-12820.7625	647.5
3345	S<2370>	-12871.7075	487.5
3346	S<2371>	-12922.6525	327.5
3347	S<2372>	-12854.02	647.5
3348	S<2373>	-12905.0975	487.5
3349	S<2374>	-12956.175	327.5
3350	S<2375>	-12887.2775	647.5
3351	S<2376>	-12938.4875	487.5

3352	S<2377>	-12989.6975	327.5
3353	S<2378>	-12920.535	647.5
3354	S<2379>	-12971.8775	487.5
3355	S<2380>	-13023.22	327.5
3356	S<2381>	-12953.7925	647.5
3357	S<2382>	-13005.2675	487.5
3358	S<2383>	-13056.74	327.5
3359	S<2384>	-12987.05	647.5
3360	S<2385>	-13038.655	487.5
3361	S<2386>	-13090.2625	327.5
3362	S<2387>	-13020.3075	647.5
3363	S<2388>	-13072.0475	487.5
3364	S<2389>	-13123.7825	327.5
3365	S<2390>	-13053.565	647.5
3366	S<2391>	-13105.435	487.5
3367	S<2392>	-13157.305	327.5
3368	S<2393>	-13086.8225	647.5
3369	S<2394>	-13138.825	487.5
3370	S<2395>	-13190.8275	327.5
3371	S<2396>	-13120.08	647.5
3372	S<2397>	-13172.215	487.5
3373	S<2398>	-13224.35	327.5
3374	S<2399>	-13153.3375	647.5
3375	S<2400>	-13205.605	487.5
3376	S<2401>	-13257.8725	327.5
3377	S<2402>	-13186.595	647.5
3378	S<2403>	-13238.995	487.5
3379	S<2404>	-13291.3925	327.5
3380	S<2405>	-13219.8525	647.5
3381	S<2406>	-13272.3825	487.5
3382	S<2407>	-13324.915	327.5
3383	S<2408>	-13253.11	647.5
3384	S<2409>	-13305.775	487.5
3385	S<2410>	-13358.435	327.5
3386	S<2411>	-13286.3675	647.5
3387	S<2412>	-13339.1625	487.5
3388	S<2413>	-13391.9575	327.5
3389	S<2414>	-13319.625	647.5
3390	S<2415>	-13372.5525	487.5
3391	S<2416>	-13425.48	327.5

3392	S<2417>	-13352.8825	647.5
3393	S<2418>	-13405.9425	487.5
3394	S<2419>	-13459.0025	327.5
3395	S<2420>	-13386.14	647.5
3396	S<2421>	-13439.3325	487.5
3397	S<2422>	-13492.525	327.5
3398	S<2423>	-13419.3975	647.5
3399	S<2424>	-13472.7225	487.5
3400	S<2425>	-13526.045	327.5
3401	S<2426>	-13452.655	647.5
3402	S<2427>	-13506.11	487.5
3403	S<2428>	-13559.5675	327.5
3404	S<2429>	-13485.9125	647.5
3405	S<2430>	-13539.5025	487.5
3406	S<2431>	-13593.0875	327.5
3407	S<2432>	-13519.17	647.5
3408	S<2433>	-13572.89	487.5
3409	S<2434>	-13626.61	327.5
3410	S<2435>	-13552.4275	647.5
3411	S<2436>	-13606.28	487.5
3412	S<2437>	-13660.1325	327.5
3413	S<2438>	-13585.685	647.5
3414	S<2439>	-13639.67	487.5
3415	S<2440>	-13693.655	327.5
3416	S<2441>	-13618.9425	647.5
3417	S<2442>	-13673.06	487.5
3418	S<2443>	-13727.1775	327.5
3419	S<2444>	-13652.2	647.5
3420	S<2445>	-13706.45	487.5
3421	S<2446>	-13760.6975	327.5
3422	S<2447>	-13685.4575	647.5
3423	S<2448>	-13739.8375	487.5
3424	S<2449>	-13794.22	327.5
3425	S<2450>	-13718.715	647.5
3426	S<2451>	-13773.23	487.5
3427	S<2452>	-13827.74	327.5
3428	S<2453>	-13751.9725	647.5
3429	S<2454>	-13806.6175	487.5
3430	S<2455>	-13861.2625	327.5
3431	S<2456>	-13785.23	647.5

3432	S<2457>	-13840.0075	487.5
3433	S<2458>	-13894.785	327.5
3434	S<2459>	-13818.4875	647.5
3435	S<2460>	-13873.3975	487.5
3436	S<2461>	-13928.3075	327.5
3437	S<2462>	-13851.745	647.5
3438	S<2463>	-13906.7875	487.5
3439	S<2464>	-13961.83	327.5
3440	S<2465>	-13885.0025	647.5
3441	S<2466>	-13940.1775	487.5
3442	S<2467>	-13995.35	327.5
3443	S<2468>	-13918.26	647.5
3444	S<2469>	-13973.565	487.5
3445	S<2470>	-14028.8725	327.5
3446	S<2471>	-13951.5175	647.5
3447	S<2472>	-14006.9575	487.5
3448	S<2473>	-14062.3925	327.5
3449	S<2474>	-13984.775	647.5
3450	S<2475>	-14040.345	487.5
3451	S<2476>	-14095.915	327.5
3452	S<2477>	-14018.0325	647.5
3453	S<2478>	-14073.735	487.5
3454	S<2479>	-14129.4375	327.5
3455	S<2480>	-14051.29	647.5
3456	S<2481>	-14107.125	487.5
3457	S<2482>	-14162.96	327.5
3458	S<2483>	-14084.5475	647.5
3459	S<2484>	-14140.515	487.5
3460	S<2485>	-14196.4825	327.5
3461	S<2486>	-14117.805	647.5
3462	S<2487>	-14173.905	487.5
3463	S<2488>	-14230.0025	327.5
3464	S<2489>	-14151.0625	647.5
3465	S<2490>	-14207.2925	487.5
3466	S<2491>	-14263.525	327.5
3467	S<2492>	-14184.32	647.5
3468	S<2493>	-14240.685	487.5
3469	S<2494>	-14297.045	327.5
3470	S<2495>	-14217.5775	647.5
3471	S<2496>	-14274.0725	487.5

3472	S<2497>	-14330.5675	327.5
3473	S<2498>	-14250.835	647.5
3474	S<2499>	-14307.4625	487.5
3475	S<2500>	-14364.09	327.5
3476	S<2501>	-14284.0925	647.5
3477	S<2502>	-14340.8525	487.5
3478	S<2503>	-14397.6125	327.5
3479	S<2504>	-14317.35	647.5
3480	S<2505>	-14374.2425	487.5
3481	S<2506>	-14431.135	327.5
3482	S<2507>	-14350.6075	647.5
3483	S<2508>	-14407.6325	487.5
3484	S<2509>	-14464.6575	327.5
3485	S<2510>	-14383.865	647.5
3486	S<2511>	-14441.02	487.5
3487	S<2512>	-14498.1775	327.5
3488	S<2513>	-14417.1225	647.5
3489	S<2514>	-14474.4125	487.5
3490	S<2515>	-14531.6975	327.5
3491	S<2516>	-14450.38	647.5
3492	S<2517>	-14507.8	487.5
3493	S<2518>	-14565.22	327.5
3494	S<2519>	-14483.6375	647.5
3495	S<2520>	-14541.19	487.5
3496	S<2521>	-14598.7425	327.5
3497	S<2522>	-14516.895	647.5
3498	S<2523>	-14574.58	487.5
3499	S<2524>	-14632.265	327.5
3500	S<2525>	-14550.1525	647.5
3501	S<2526>	-14607.97	487.5
3502	S<2527>	-14665.7875	327.5
3503	S<2528>	-14583.41	647.5
3504	S<2529>	-14641.36	487.5
3505	S<2530>	-14699.31	327.5
3506	S<2531>	-14616.6675	647.5
3507	S<2532>	-14674.7475	487.5
3508	S<2533>	-14732.83	327.5
3509	S<2534>	-14649.925	647.5
3510	S<2535>	-14708.14	487.5
3511	S<2536>	-14766.35	327.5

3512	S<2537>	-14683.1825	647.5
3513	S<2538>	-14741.5275	487.5
3514	S<2539>	-14799.8725	327.5
3515	S<2540>	-14716.44	647.5
3516	S<2541>	-14774.9175	487.5
3517	S<2542>	-14833.395	327.5
3518	S<2543>	-14749.6975	647.5
3519	S<2544>	-14808.3075	487.5
3520	S<2545>	-14866.9175	327.5
3521	S<2546>	-14782.955	647.5
3522	S<2547>	-14841.695	487.5
3523	S<2548>	-14900.44	327.5
3524	S<2549>	-14816.2125	647.5
3525	S<2550>	-14875.0875	487.5
3526	S<2551>	-14933.9625	327.5
3527	S<2552>	-14849.47	647.5
3528	S<2553>	-14908.475	487.5
3529	S<2554>	-14967.4825	327.5
3530	S<2555>	-14882.7275	647.5
3531	S<2556>	-14941.8675	487.5
3532	S<2557>	-15001.0025	327.5
3533	S<2558>	-14915.985	647.5
3534	S<2559>	-14975.255	487.5
3535	S<2560>	-15034.525	327.5
3536	S_L_TEST	-14949.2425	647.5
3537	VSSDUMMY	-15008.6475	487.5
3538	VSSDUMMY	-15068.0475	327.5
3539	VSSDUMMY	-14982.5	647.5
3540	VSSDUMMY	-15042.035	487.5
3541	VSSDUMMY	-15101.57	327.5
3542	VSSDUMMY	-15015.7575	647.5
3543	VSSDUMMY	-15075.4225	487.5
3544	VSSDUMMY	-15135.0925	327.5
3545	VNIT_A_L	-15049.015	647.5
3546	VNIT_A_L	-15108.815	487.5
3547	VNIT_A_L	-15168.615	327.5
3548	VNIT_A_L	-15082.2725	647.5
3549	VNIT_A_L	-15142.2025	487.5
3550	VNIT_A_L	-15202.135	327.5
3551	VNIT_A_L	-15115.53	647.5

3552	VNIT_A_L	-15175.595	487.5
3553	VNIT_A_L	-15235.655	327.5
3554	VINIT_C_L	-15148.7875	647.5
3555	VINIT_C_L	-15208.9825	487.5
3556	VINIT_C_L	-15269.1775	327.5
3557	VINIT_C_L	-15182.045	647.5
3558	VINIT_C_L	-15242.375	487.5
3559	VINIT_C_L	-15302.7	327.5
3560	VINIT_C_L	-15215.3025	647.5
3561	VINIT_C_L	-15275.7625	487.5
3562	VINIT_C_L	-15336.2225	327.5
3563	VINIT_B_L	-15248.56	647.5
3564	VINIT_B_L	-15309.15	487.5
3565	VINIT_B_L	-15369.745	327.5
3566	VINIT_B_L	-15281.8175	647.5
3567	VINIT_B_L	-15342.5425	487.5
3568	VINIT_B_L	-15403.2675	327.5
3569	VINIT_B_L	-15315.075	647.5
3570	VINIT_B_L	-15375.93	487.5
3571	VINIT_B_L	-15436.7875	327.5
3572	VSSDUMMY	-15348.3325	647.5
3573	VSSDUMMY	-15409.3225	487.5
3574	VSSDUMMY	-15470.3075	327.5
3575	VSSDUMMY	-15381.59	647.5
3576	VSSDUMMY	-15442.71	487.5
3577	VSSDUMMY	-15503.83	327.5
3578	VSSDUMMY	-15414.8475	647.5
3579	VSSDUMMY	-15476.1025	487.5
3580	VSSDUMMY	-15537.3525	327.5
3581	VSSDUMMY	-15448.105	647.5
3582	VSSDUMMY	-15509.49	487.5
3583	VSSDUMMY	-15570.875	327.5
3584	VSSDUMMY	-15481.3625	647.5
3585	VSSDUMMY	-15542.8775	487.5
3586	VSSDUMMY	-15604.3975	327.5
3587	VSSDUMMY	-15514.62	647.5
3588	VSSDUMMY	-15576.27	487.5
3589	VSSDUMMY	-15637.92	327.5
3590	VSSDUMMY	-15547.8775	647.5
3591	VSSDUMMY	-15609.6575	487.5

3592	VSSDUMMY	-15671.4425	327.5
3593	GOUT16_L	-15581.135	647.5
3594	GOUT16_L	-15643.05	487.5
3595	GOUT16_L	-15704.96	327.5
3596	GOUT15_L	-15614.3925	647.5
3597	GOUT15_L	-15676.4375	487.5
3598	GOUT15_L	-15738.4825	327.5
3599	GOUT14_L	-15647.65	647.5
3600	GOUT14_L	-15709.83	487.5
3601	GOUT14_L	-15772.005	327.5
3602	GOUT13_L	-15680.9075	647.5
3603	GOUT13_L	-15743.2175	487.5
3604	GOUT13_L	-15805.5275	327.5
3605	GOUT12_L	-15714.165	647.5
3606	GOUT12_L	-15776.605	487.5
3607	GOUT12_L	-15839.05	327.5
3608	GOUT11_L	-15747.4225	647.5
3609	GOUT11_L	-15809.9975	487.5
3610	GOUT11_L	-15872.5725	327.5
3611	GOUT10_L	-15780.68	647.5
3612	GOUT10_L	-15843.385	487.5
3613	GOUT10_L	-15906.095	327.5
3614	GOUT9_L	-15813.9375	647.5
3615	GOUT9_L	-15876.7775	487.5
3616	GOUT9_L	-15939.6125	327.5
3617	GOUT8_L	-15847.195	647.5
3618	GOUT8_L	-15910.165	487.5
3619	GOUT8_L	-15973.135	327.5
3620	GOUT7_L	-15880.4525	647.5
3621	GOUT7_L	-15943.5575	487.5
3622	GOUT7_L	-16006.6575	327.5
3623	GOUT6_L	-15913.71	647.5
3624	GOUT6_L	-15976.945	487.5
3625	GOUT6_L	-16040.18	327.5
3626	GOUT5_L	-15946.9675	647.5
3627	GOUT5_L	-16010.3325	487.5
3628	GOUT5_L	-16073.7025	327.5
3629	GOUT4_L	-15980.225	647.5
3630	GOUT4_L	-16043.725	487.5
3631	GOUT4_L	-16107.225	327.5

3632	GOUT3_L	-16013.4825	647.5
3633	GOUT3_L	-16077.1125	487.5
3634	GOUT3_L	-16140.7475	327.5
3635	GOUT2_L	-16046.74	647.5
3636	GOUT2_L	-16110.505	487.5
3637	GOUT2_L	-16174.265	327.5
3638	GOUT1_L	-16079.9975	647.5
3639	GOUT1_L	-16143.8925	487.5
3640	GOUT1_L	-16207.7875	327.5
3641	VSSDUMMY	-16113.255	647.5
3642	VSSDUMMY	-16177.285	487.5
3643	VSSDUMMY	-16241.31	327.5
3644	DUMMYO_L3	-16146.5125	647.5
3645	VSSDUMMY	-16210.6725	487.5
3646	VSSDUMMY	-16274.8325	327.5
3647	DUMMYO_L4	-16179.77	647.5
3648	VSSDUMMY	-16244.06	487.5
3649	VSSDUMMY	-16308.355	327.5
3650	DUMMYO_L4	-16213.0275	647.5
3651	VSSDUMMY	-16277.4525	487.5
3652	DUMMYO_L4	-16246.285	647.5
3653	DUMMY_SL	-16340	162.5
3654	DUMMY_SL	-16340	97.5
3655	DUMMY_SL	-16340	32.5
3656	DUMMY_SL	-16340	-32.5
3657	DUMMY_SL	-16340	-97.5
3658	DUMMY_SL	-16340	-162.5
3659	DUMMY_SL	-16340	-227.5
3660	DUMMY_SL	-16340	-292.5
3661	DUMMY_SL	-16340	-357.5
3662	DUMMY_SL	-16340	-422.5
3663	DUMMY_SR	16340	162.5
3664	DUMMY_SR	16340	97.5
3665	DUMMY_SR	16340	32.5
3666	DUMMY_SR	16340	-32.5
3667	DUMMY_SR	16340	-97.5
3668	DUMMY_SR	16340	-162.5
3669	DUMMY_SR	16340	-227.5
3670	DUMMY_SR	16340	-292.5
3671	DUMMY_SR	16340	-357.5

3672	DUMMY_SR	16340	-422.5
3673	DUMMY	-16080	-130
3674	DUMMY	-15920	-130
3675	DUMMY	-15760	-130
3676	DUMMY	-15600	-130
3677	DUMMY	-15440	-130
3678	DUMMY	-15280	-130
3679	DUMMY	-15120	-130
3680	DUMMY	-14960	-130
3681	DUMMY	-14800	-130
3682	DUMMY	-14640	-130
3683	DUMMY	-14480	-130
3684	DUMMY	-14320	-130
3685	DUMMY	-14160	-130
3686	DUMMY	-14000	-130
3687	DUMMY	-13840	-130
3688	DUMMY	-13680	-130
3689	DUMMY	-13520	-130
3690	DUMMY	-13360	-130
3691	DUMMY	-13200	-130
3692	DUMMY	-13040	-130
3693	DUMMY	-12880	-130
3694	DUMMY	-12720	-130
3695	DUMMY	-12560	-130
3696	DUMMY	-12400	-130
3697	DUMMY	-12240	-130
3698	DUMMY	-12080	-130
3699	DUMMY	-11920	-130
3700	DUMMY	-11760	-130
3701	DUMMY	-11600	-130
3702	DUMMY	-11440	-130
3703	DUMMY	-11280	-130
3704	DUMMY	-11120	-130
3705	DUMMY	-10960	-130
3706	DUMMY	-10800	-130
3707	DUMMY	-10640	-130
3708	DUMMY	-10480	-130
3709	DUMMY	-10320	-130
3710	DUMMY	-10160	-130
3711	DUMMY	-10000	-130

3712	DUMMY	-9840	-130
3713	DUMMY	-9680	-130
3714	DUMMY	-9520	-130
3715	DUMMY	-9360	-130
3716	DUMMY	-9200	-130
3717	DUMMY	-9040	-130
3718	DUMMY	-8880	-130
3719	DUMMY	-8720	-130
3720	DUMMY	-8560	-130
3721	DUMMY	-8400	-130
3722	DUMMY	-8240	-130
3723	DUMMY	-8080	-130
3724	DUMMY	-7920	-130
3725	DUMMY	-7760	-130
3726	DUMMY	-7600	-130
3727	DUMMY	-7440	-130
3728	DUMMY	-7280	-130
3729	DUMMY	-7120	-130
3730	DUMMY	-6960	-130
3731	DUMMY	-6800	-130
3732	DUMMY	-6640	-130
3733	DUMMY	-6480	-130
3734	DUMMY	-6320	-130
3735	DUMMY	-6160	-130
3736	DUMMY	-6000	-130
3737	DUMMY	-5840	-130
3738	DUMMY	-5680	-130
3739	DUMMY	-5520	-130
3740	DUMMY	-5360	-130
3741	DUMMY	-5200	-130
3742	DUMMY	-5040	-130
3743	DUMMY	-4880	-130
3744	DUMMY	-4720	-130
3745	DUMMY	-4560	-130
3746	DUMMY	-4400	-130
3747	DUMMY	-4240	-130
3748	DUMMY	-4080	-130
3749	DUMMY	-3920	-130
3750	DUMMY	-3760	-130
3751	DUMMY	-3600	-130

3752	DUMMY	-3440	-130
3753	DUMMY	-3280	-130
3754	DUMMY	-3120	-130
3755	DUMMY	-2960	-130
3756	DUMMY	-2800	-130
3757	DUMMY	-2640	-130
3758	DUMMY	-2480	-130
3759	DUMMY	-2320	-130
3760	DUMMY	-2160	-130
3761	DUMMY	-2000	-130
3762	DUMMY	-1840	-130
3763	DUMMY	-1680	-130
3764	DUMMY	-1520	-130
3765	DUMMY	-1360	-130
3766	DUMMY	-1200	-130
3767	DUMMY	-1040	-130
3768	DUMMY	-880	-130
3769	DUMMY	-720	-130
3770	DUMMY	-560	-130
3771	DUMMY	-400	-130
3772	DUMMY	-240	-130
3773	DUMMY	-80	-130
3774	DUMMY	80	-130
3775	DUMMY	240	-130
3776	DUMMY	400	-130
3777	DUMMY	560	-130
3778	DUMMY	720	-130
3779	DUMMY	880	-130
3780	DUMMY	1040	-130
3781	DUMMY	1200	-130
3782	DUMMY	1360	-130
3783	DUMMY	1520	-130
3784	DUMMY	1680	-130
3785	DUMMY	1840	-130
3786	DUMMY	2000	-130
3787	DUMMY	2160	-130
3788	DUMMY	2320	-130
3789	DUMMY	2480	-130
3790	DUMMY	2640	-130
3791	DUMMY	2800	-130

3792	DUMMY	2960	-130
3793	DUMMY	3120	-130
3794	DUMMY	3280	-130
3795	DUMMY	3440	-130
3796	DUMMY	3600	-130
3797	DUMMY	3760	-130
3798	DUMMY	3920	-130
3799	DUMMY	4080	-130
3800	DUMMY	4240	-130
3801	DUMMY	4400	-130
3802	DUMMY	4560	-130
3803	DUMMY	4720	-130
3804	DUMMY	4880	-130
3805	DUMMY	5040	-130
3806	DUMMY	5200	-130
3807	DUMMY	5360	-130
3808	DUMMY	5520	-130
3809	DUMMY	5680	-130
3810	DUMMY	5840	-130
3811	DUMMY	6000	-130
3812	DUMMY	6160	-130
3813	DUMMY	6320	-130
3814	DUMMY	6480	-130
3815	DUMMY	6640	-130
3816	DUMMY	6800	-130
3817	DUMMY	6960	-130
3818	DUMMY	7120	-130
3819	DUMMY	7280	-130
3820	DUMMY	7440	-130
3821	DUMMY	7600	-130
3822	DUMMY	7760	-130
3823	DUMMY	7920	-130
3824	DUMMY	8080	-130
3825	DUMMY	8240	-130
3826	DUMMY	8400	-130
3827	DUMMY	8560	-130
3828	DUMMY	8720	-130
3829	DUMMY	8880	-130
3830	DUMMY	9040	-130
3831	DUMMY	9200	-130

3832	DUMMY	9360	-130
3833	DUMMY	9520	-130
3834	DUMMY	9680	-130
3835	DUMMY	9840	-130
3836	DUMMY	10000	-130
3837	DUMMY	10160	-130
3838	DUMMY	10320	-130
3839	DUMMY	10480	-130
3840	DUMMY	10640	-130
3841	DUMMY	10800	-130
3842	DUMMY	10960	-130
3843	DUMMY	11120	-130
3844	DUMMY	11280	-130
3845	DUMMY	11440	-130
3846	DUMMY	11600	-130
3847	DUMMY	11760	-130
3848	DUMMY	11920	-130
3849	DUMMY	12080	-130
3850	DUMMY	12240	-130
3851	DUMMY	12400	-130
3852	DUMMY	12560	-130
3853	DUMMY	12720	-130

3854	DUMMY	12880	-130
3855	DUMMY	13040	-130
3856	DUMMY	13200	-130
3857	DUMMY	13360	-130
3858	DUMMY	13520	-130
3859	DUMMY	13680	-130
3860	DUMMY	13840	-130
3861	DUMMY	14000	-130
3862	DUMMY	14160	-130
3863	DUMMY	14320	-130
3864	DUMMY	14480	-130
3865	DUMMY	14640	-130
3866	DUMMY	14800	-130
3867	DUMMY	14960	-130
3868	DUMMY	15120	-130
3869	DUMMY	15280	-130
3870	DUMMY	15440	-130
3871	DUMMY	15600	-130
3872	DUMMY	15760	-130
3873	DUMMY	15920	-130
3874	DUMMY	16080	-130

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