

iMX6 Rex Module

Variant: Variant name not interpreted

**7. 6. 2013
V1I1**

PRELIMINARY

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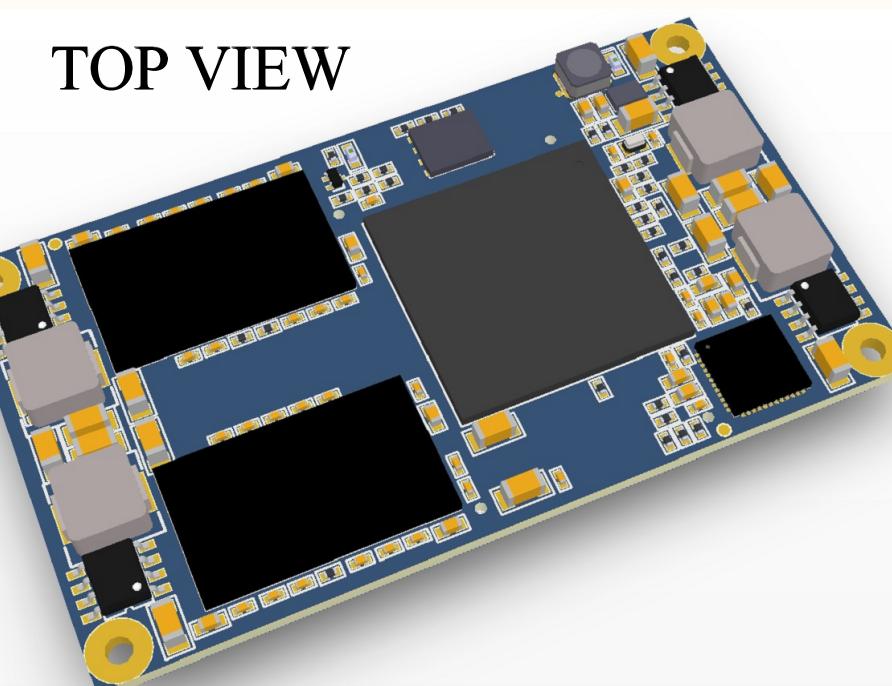
DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

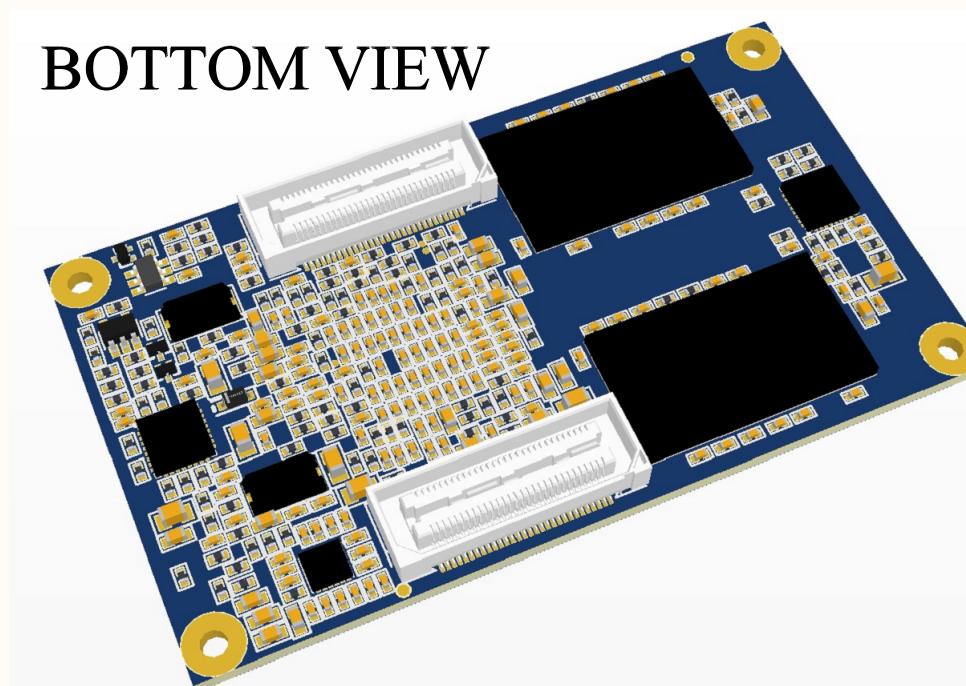
DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.



TOP VIEW



BOTTOM VIEW

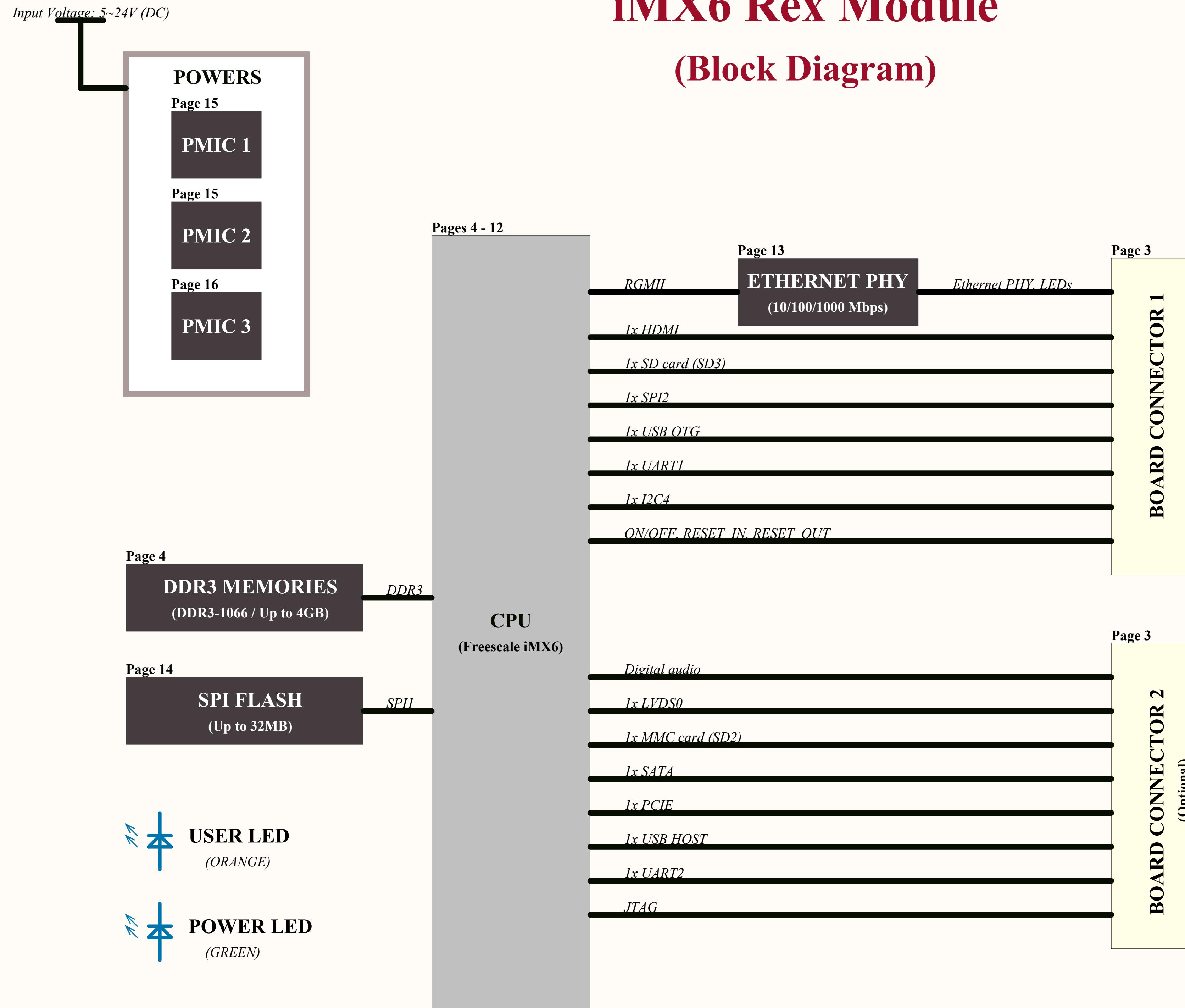


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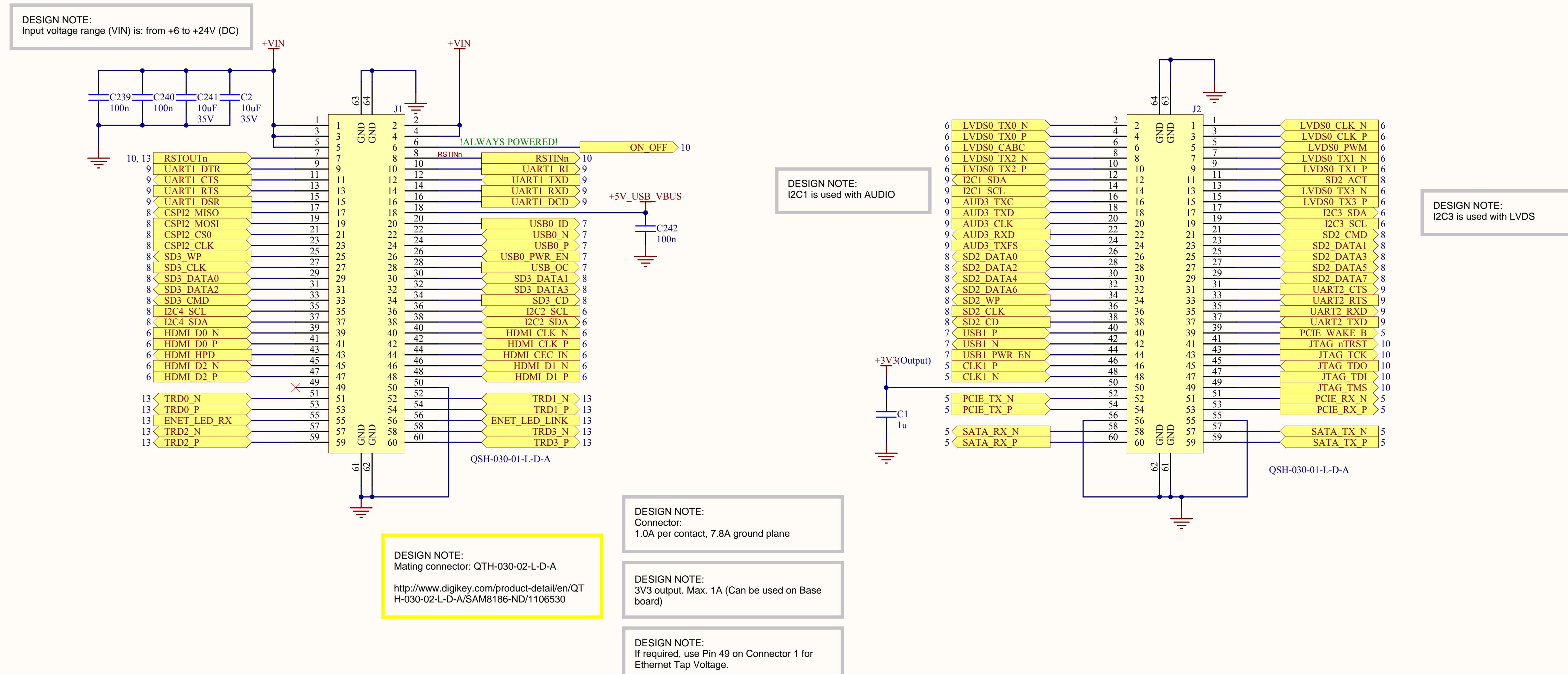
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iMX6 Rex Module

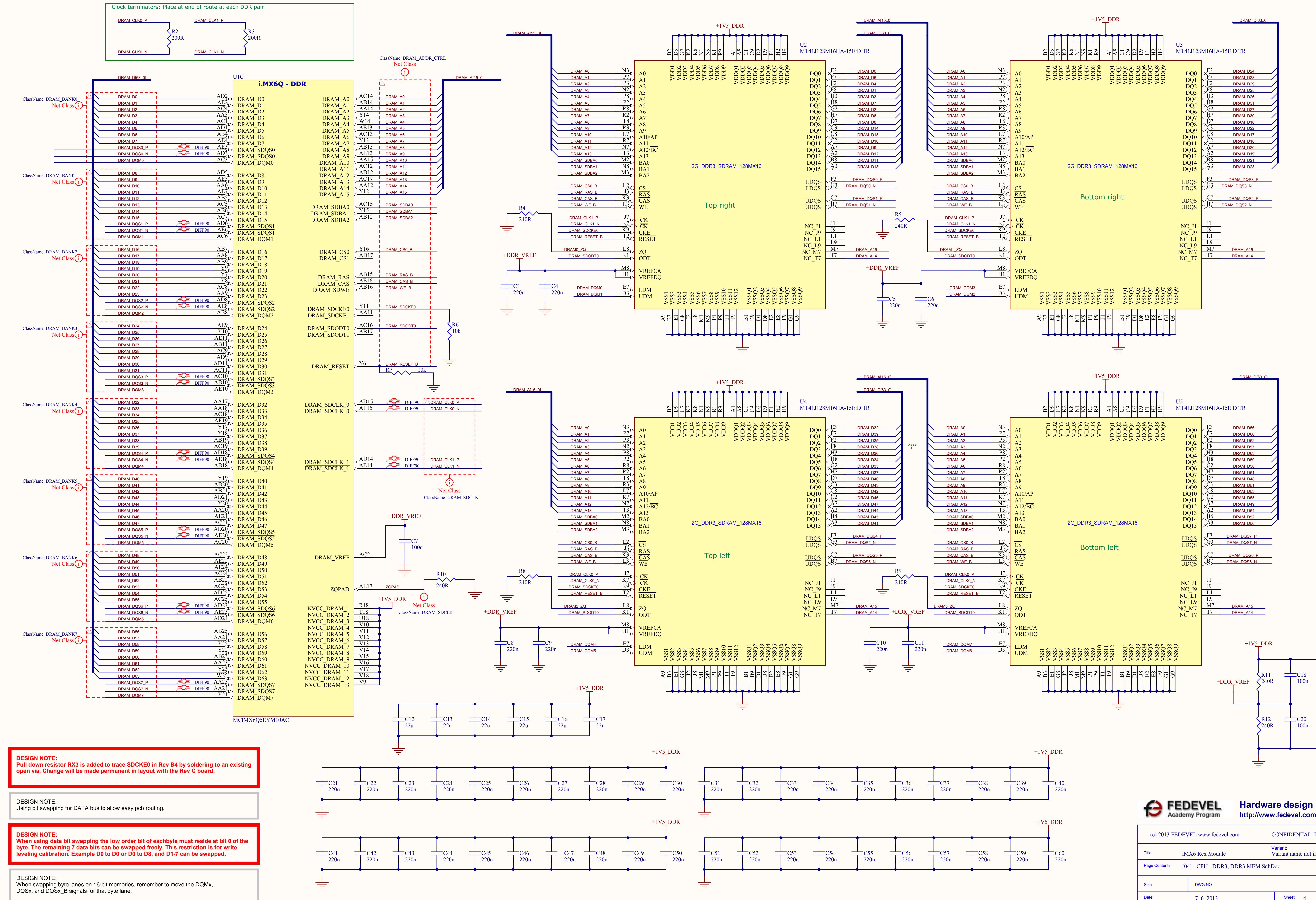
(Block Diagram)



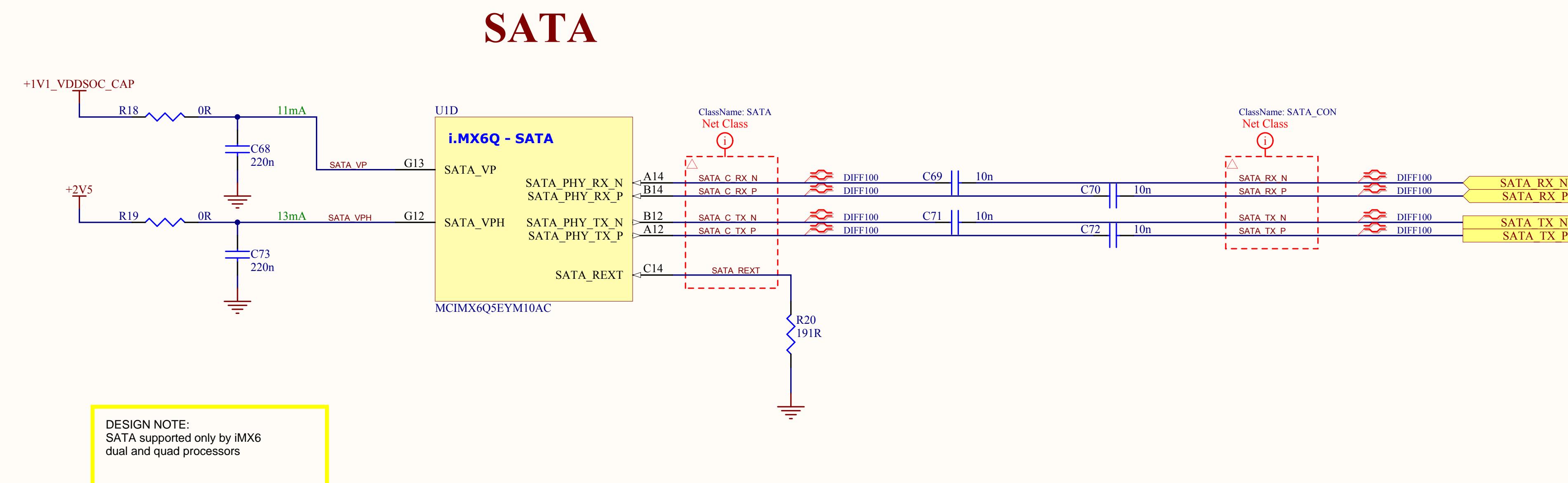
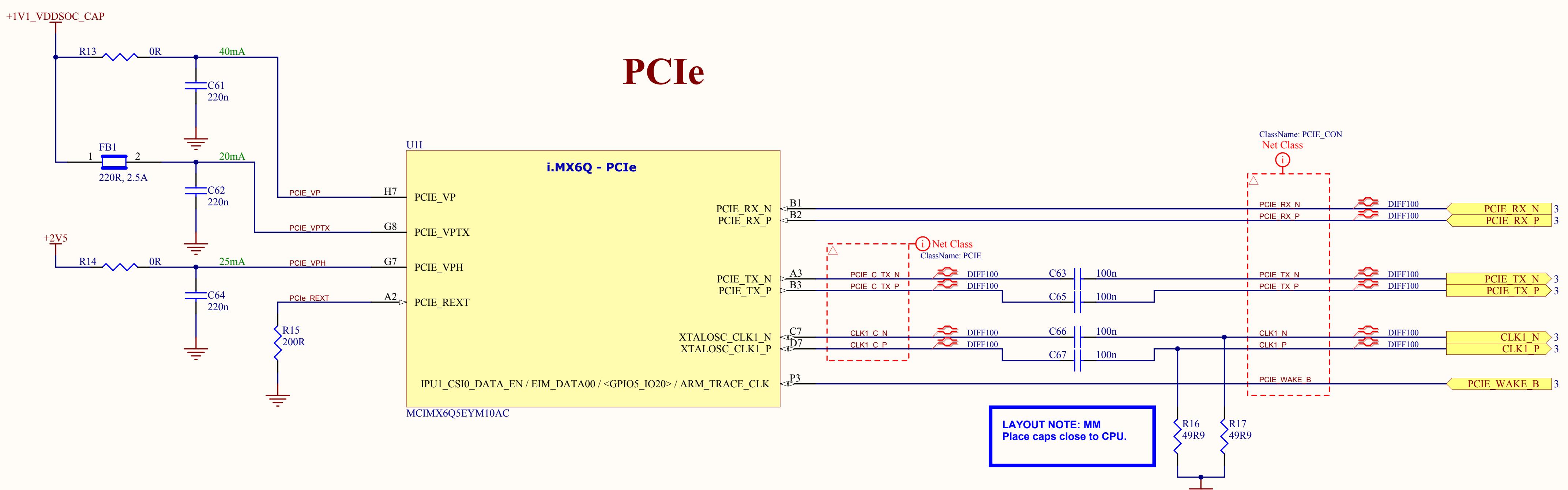
CONNECTORS



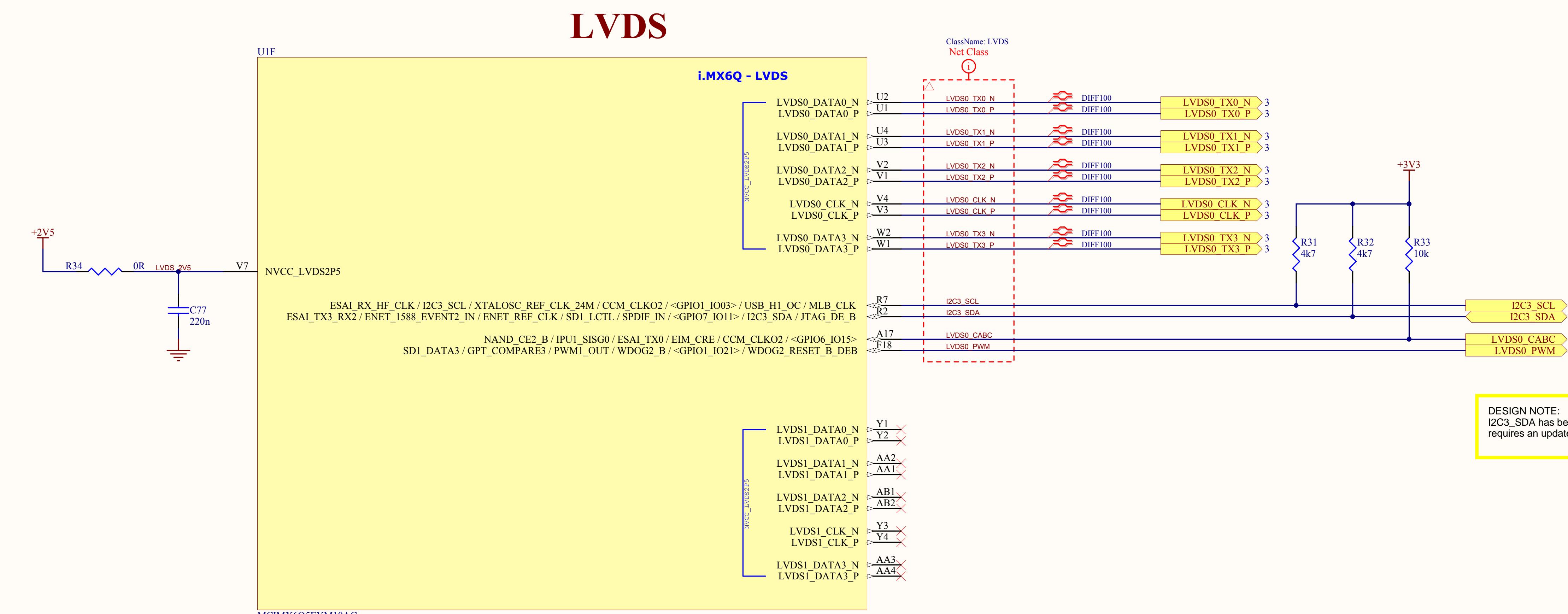
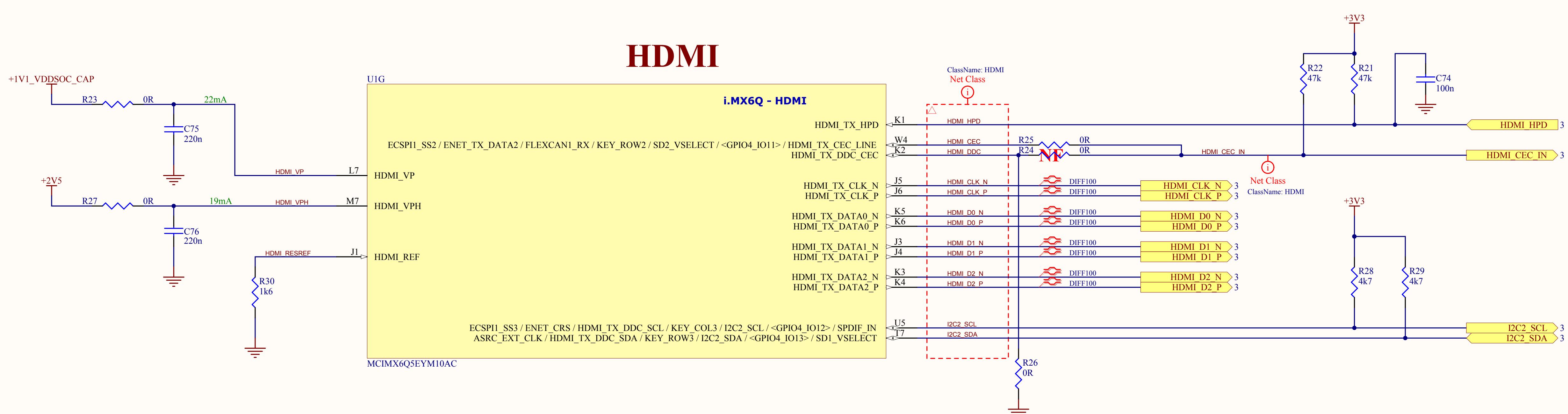
CPU - DDR3, DDR3 MEM



CPU - SATA, PCIe

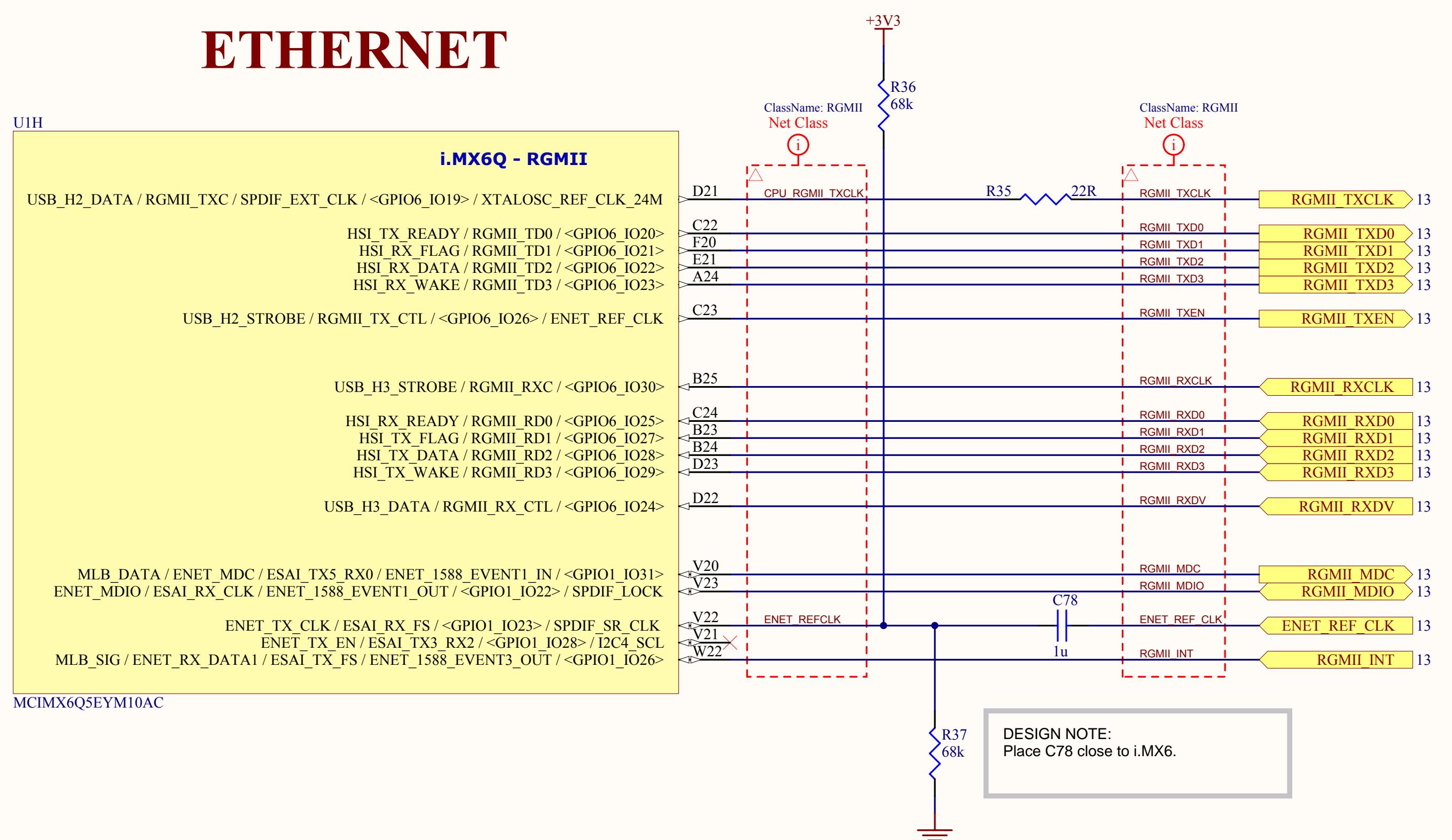


CPU - HDMI, LVDS

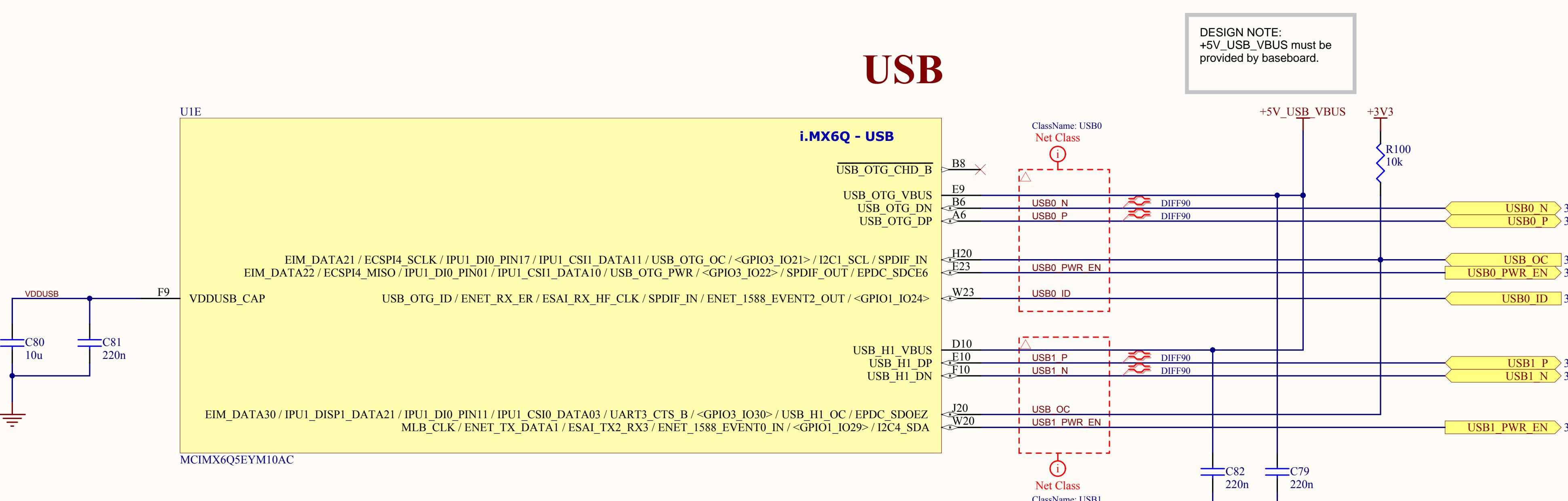


CPU - USB, ETHERNET

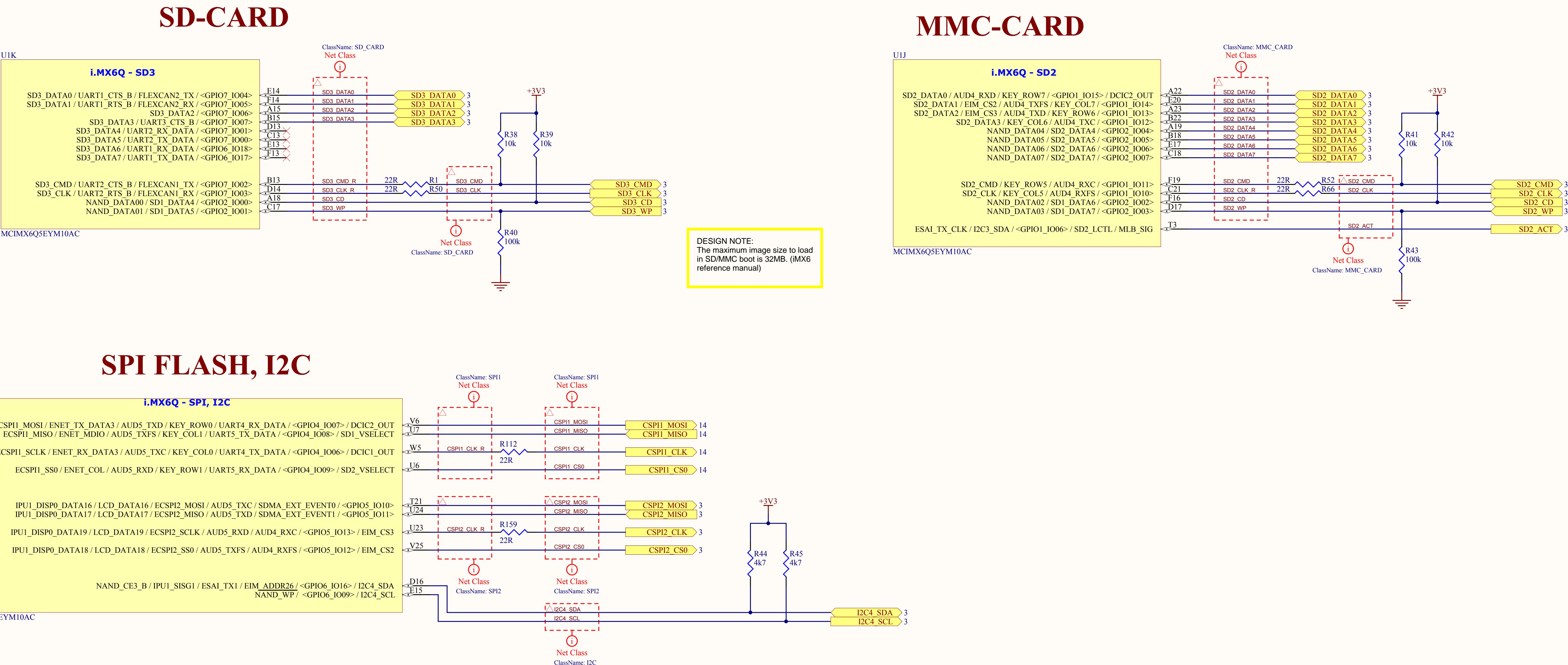
ETHERNET



USB



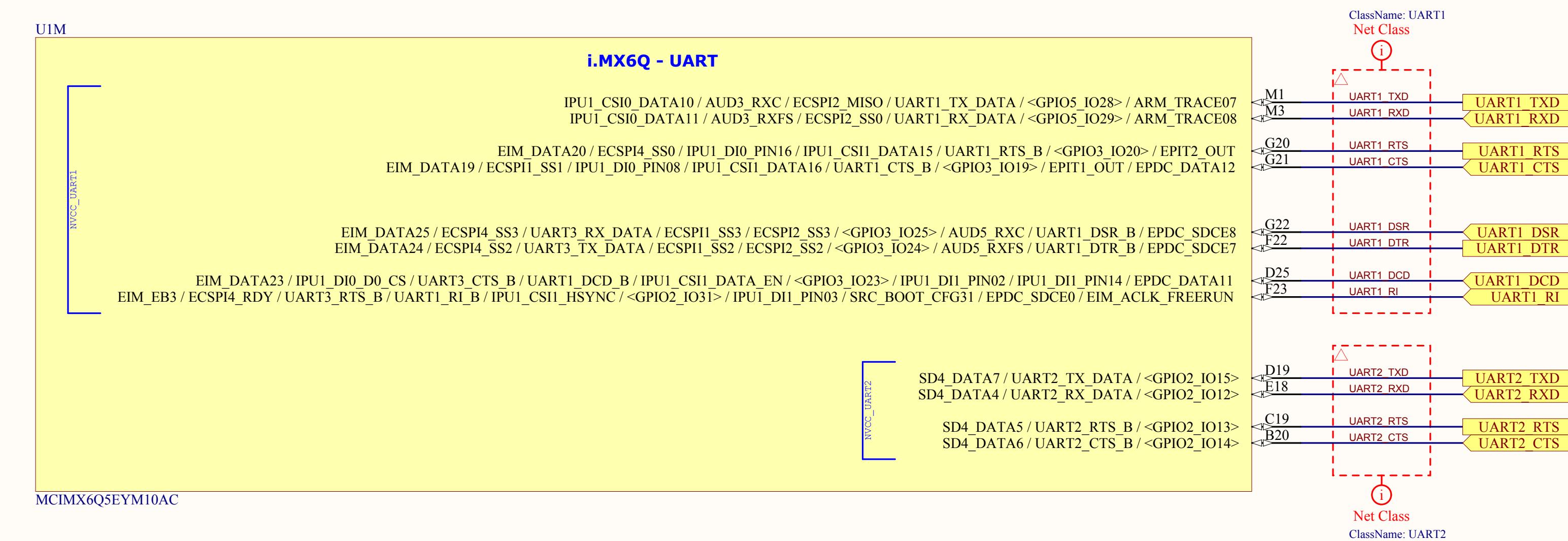
CPU - SPI, I2C, SD, MMC



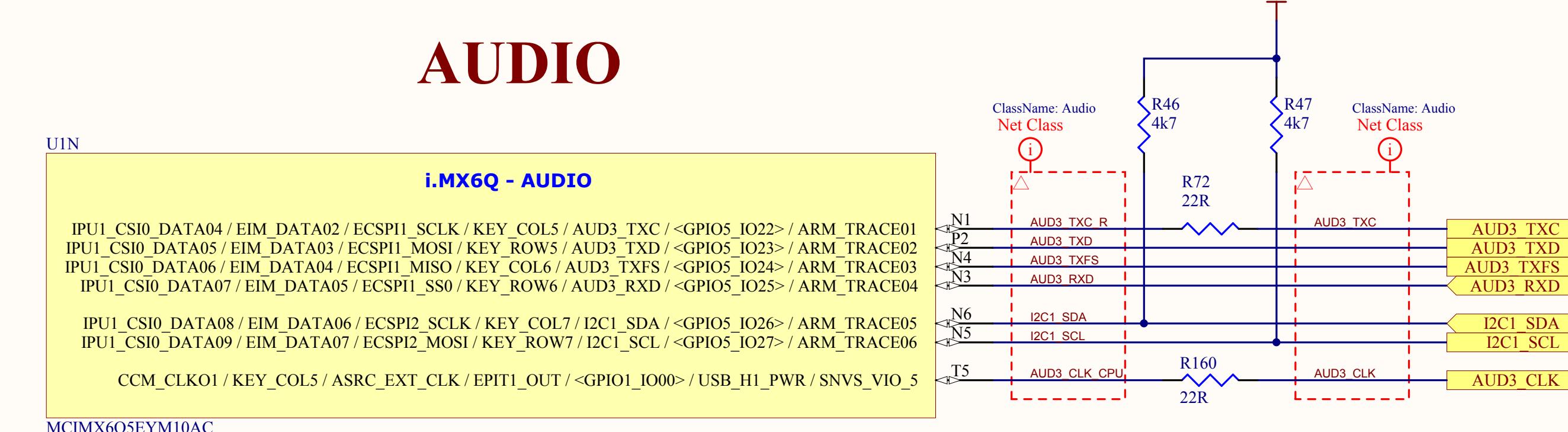
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CPU - UART, AUDIO

UART

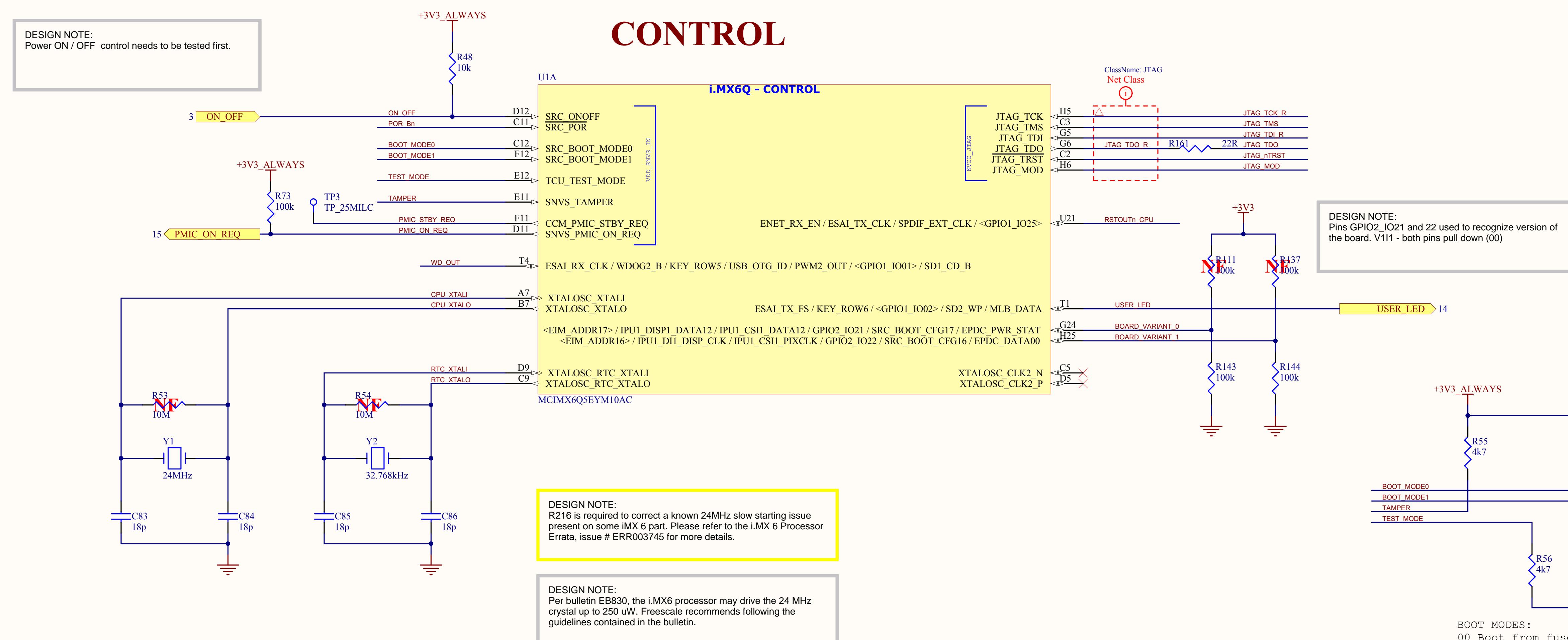


AUDIO



CPU - JTAG, CONTROL

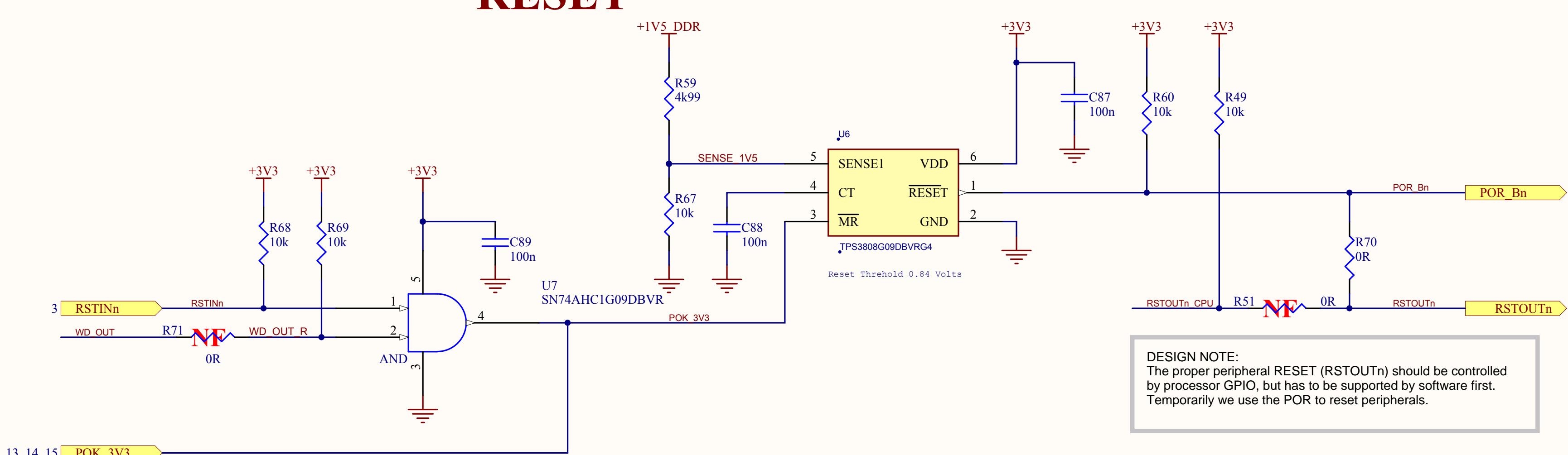
CONTROL



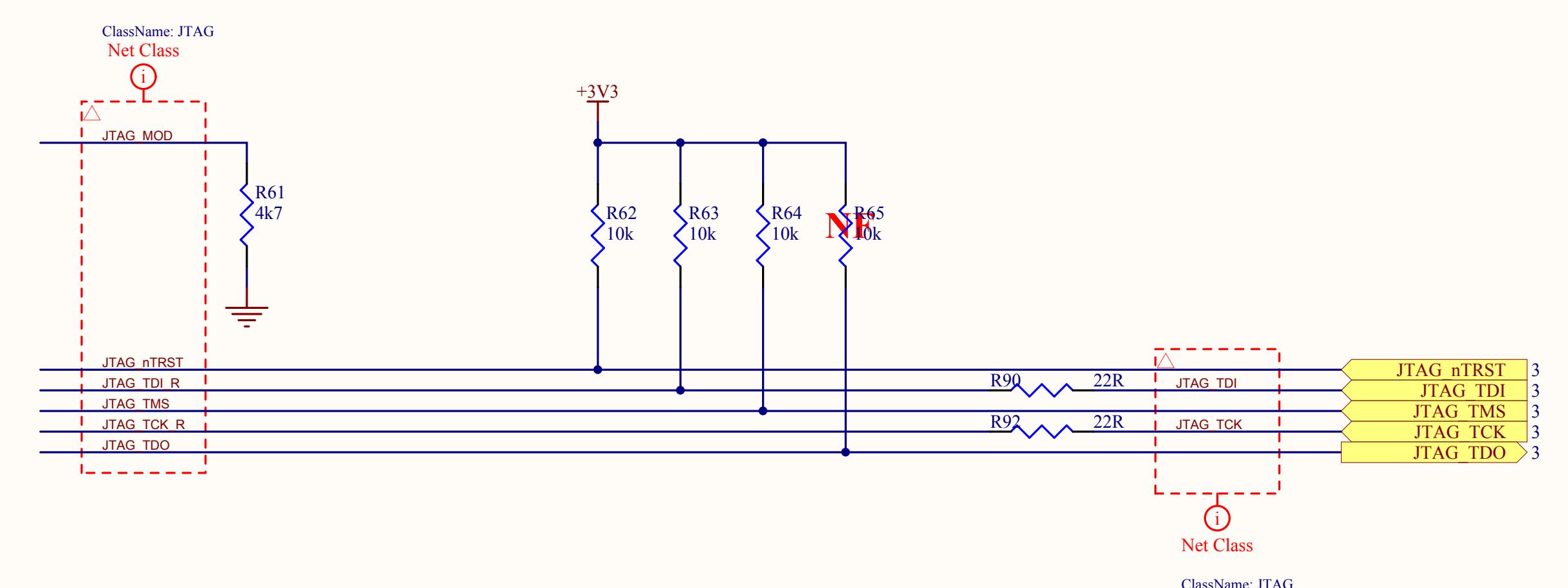
BOOT MODES:
00 Boot from fuses
01 Serial downloader
10 Boot from board settings
11 Reserved

DESIGN NOTE:
Default boot mode: 00 (eFuses).
Tamper won't be used. Test mode only for factory use.

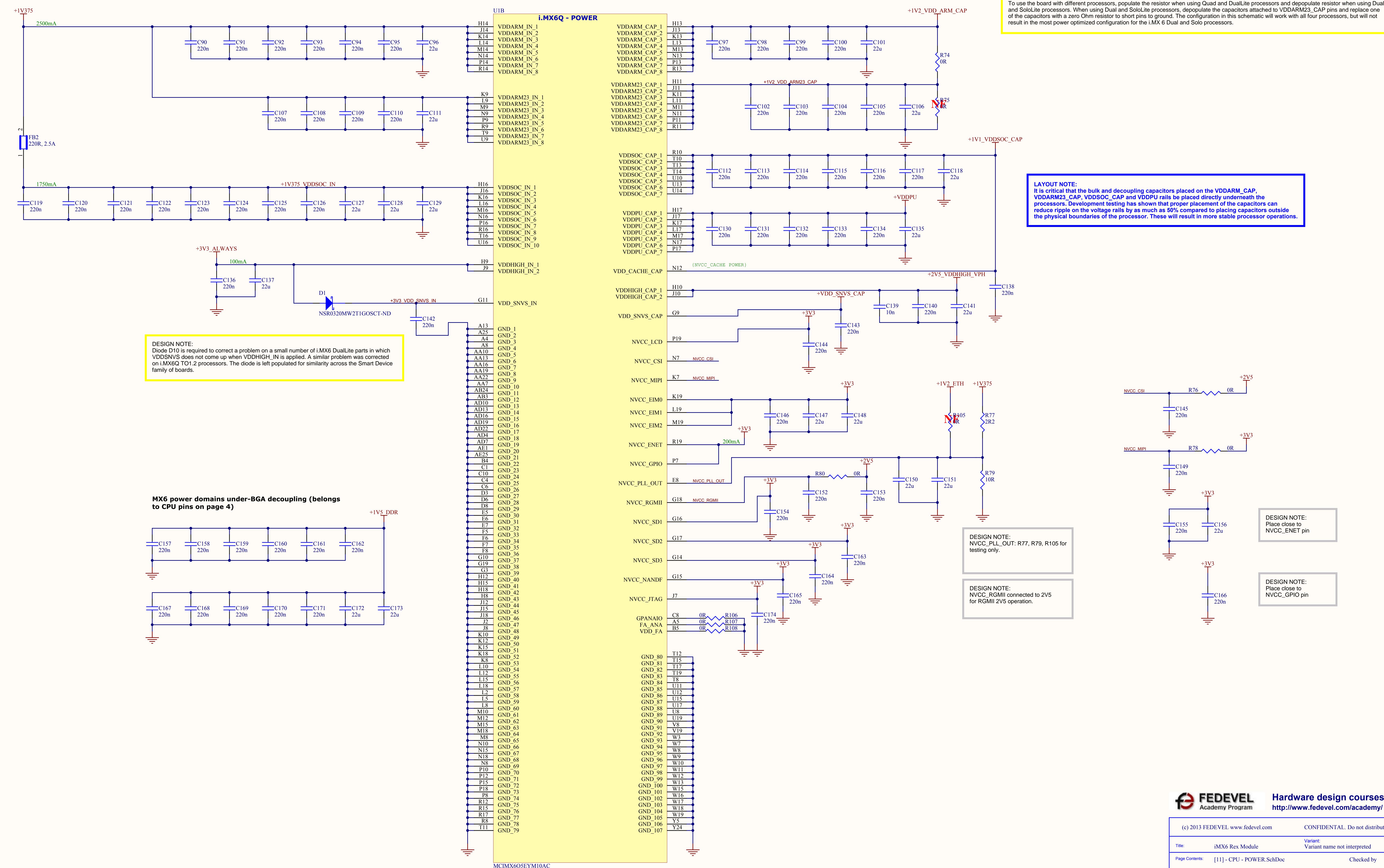
RESET



JTAG



CPU - POWER

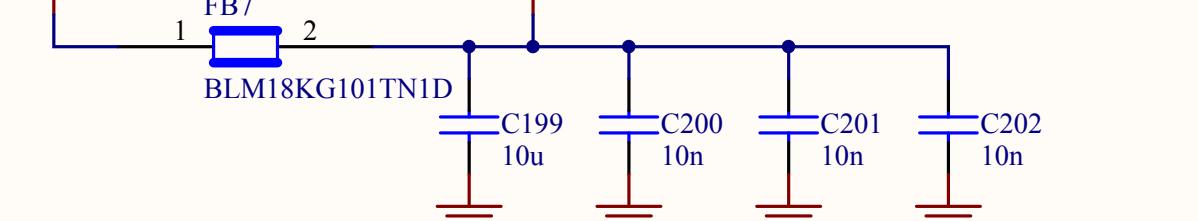
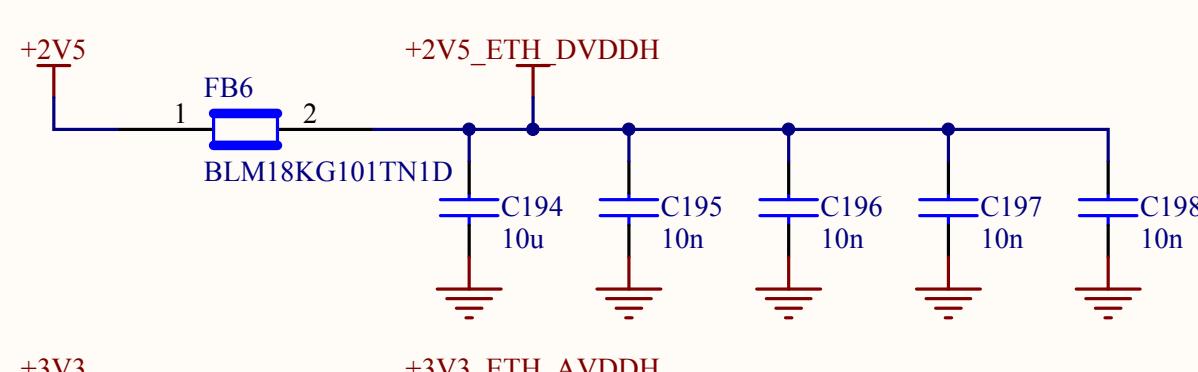
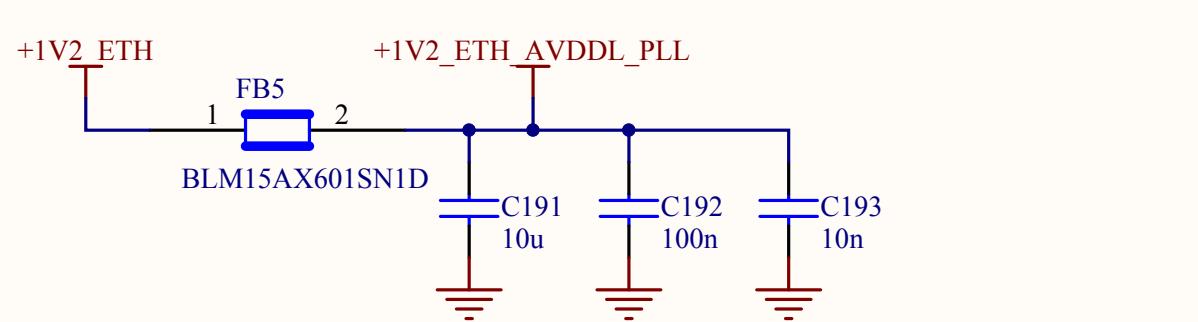
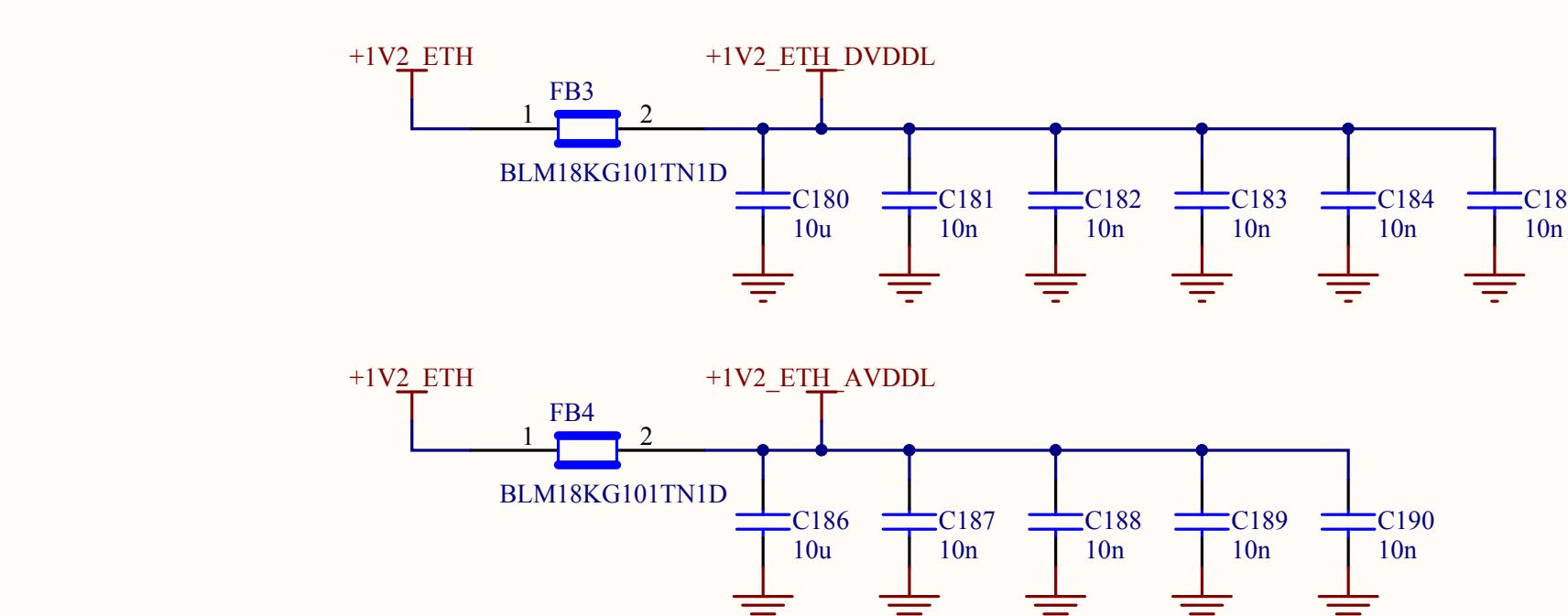
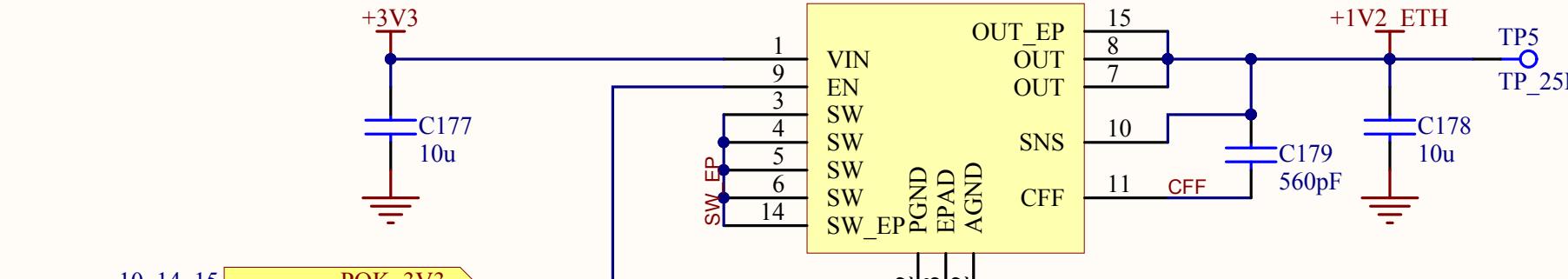
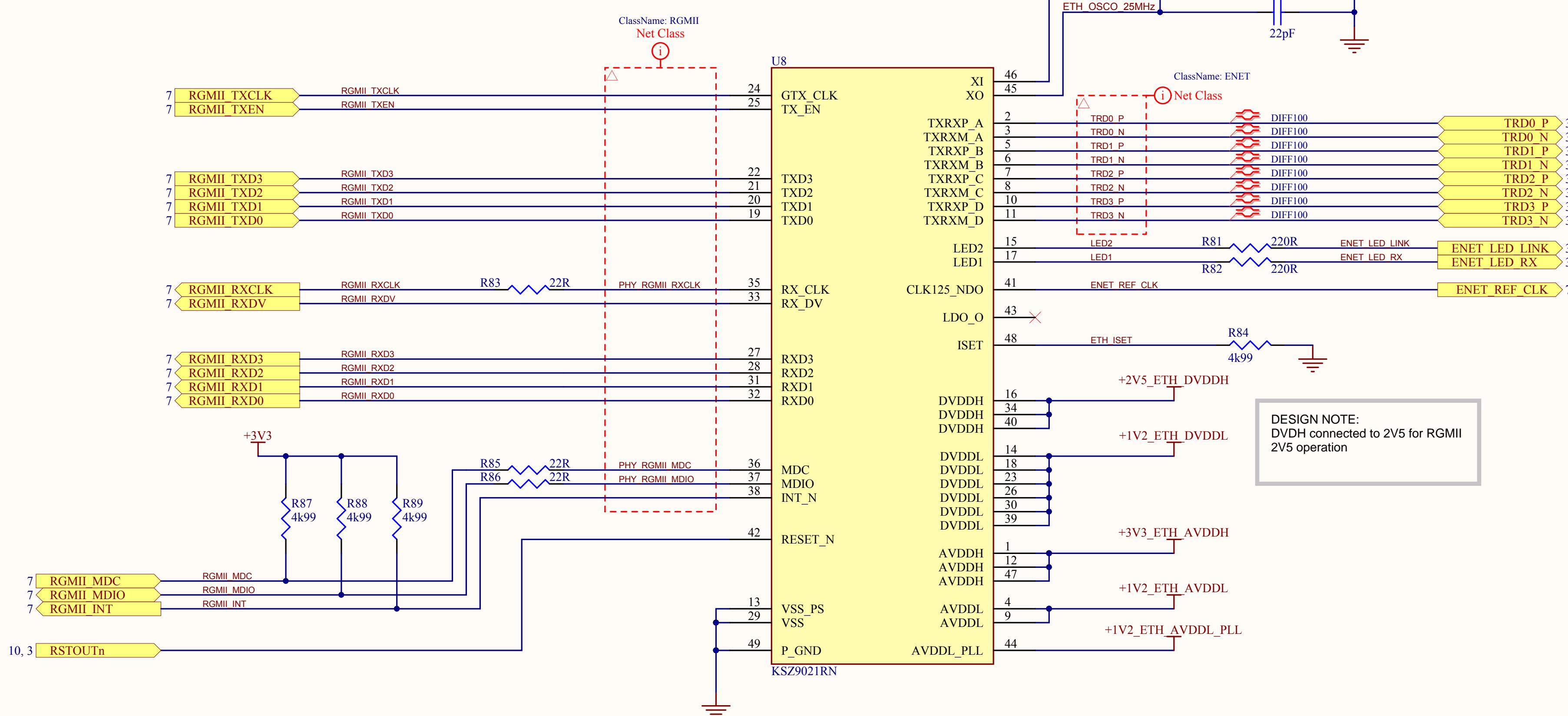


CPU - UNUSED PINS

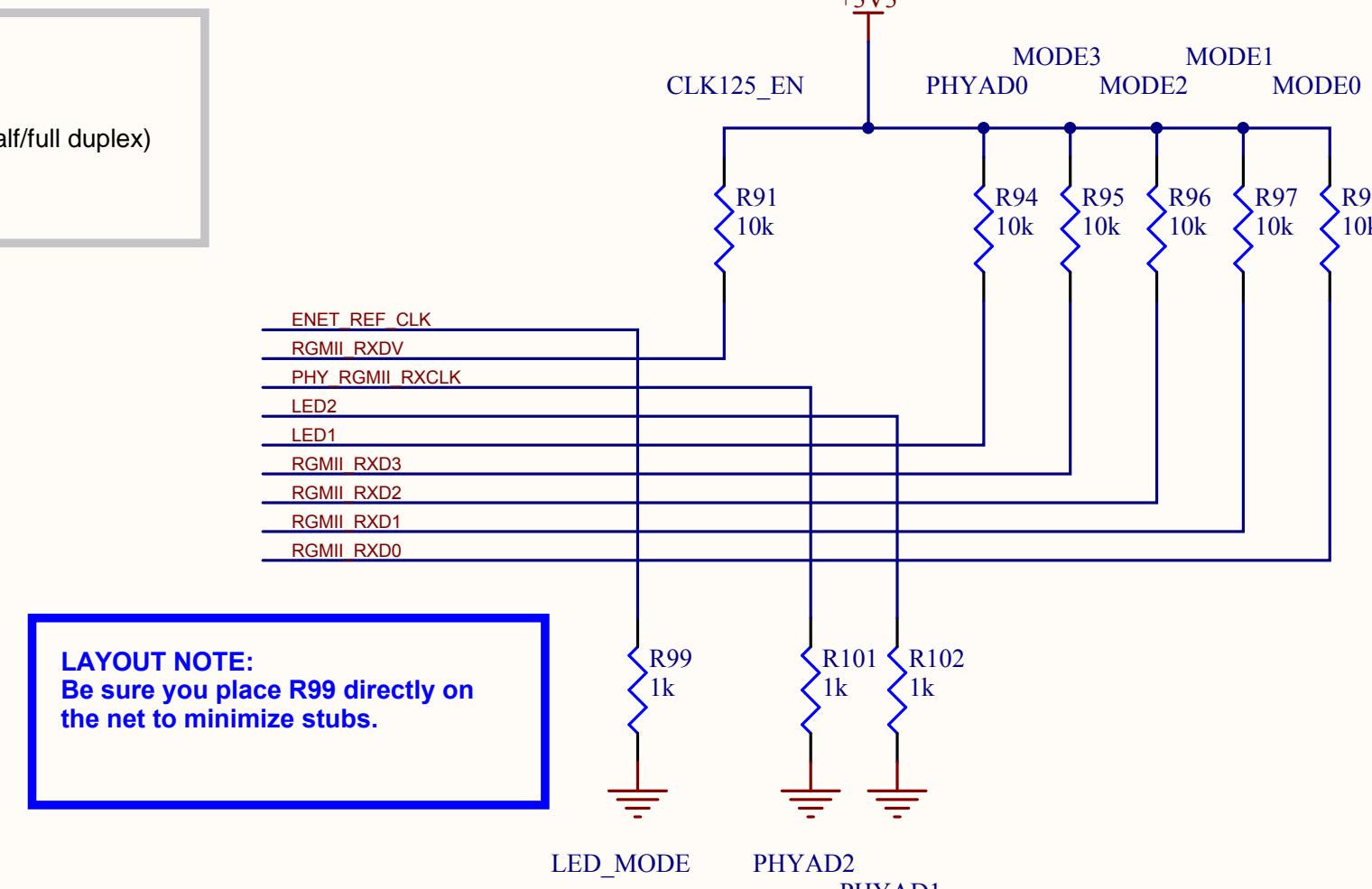


ETHERNET PHY

A

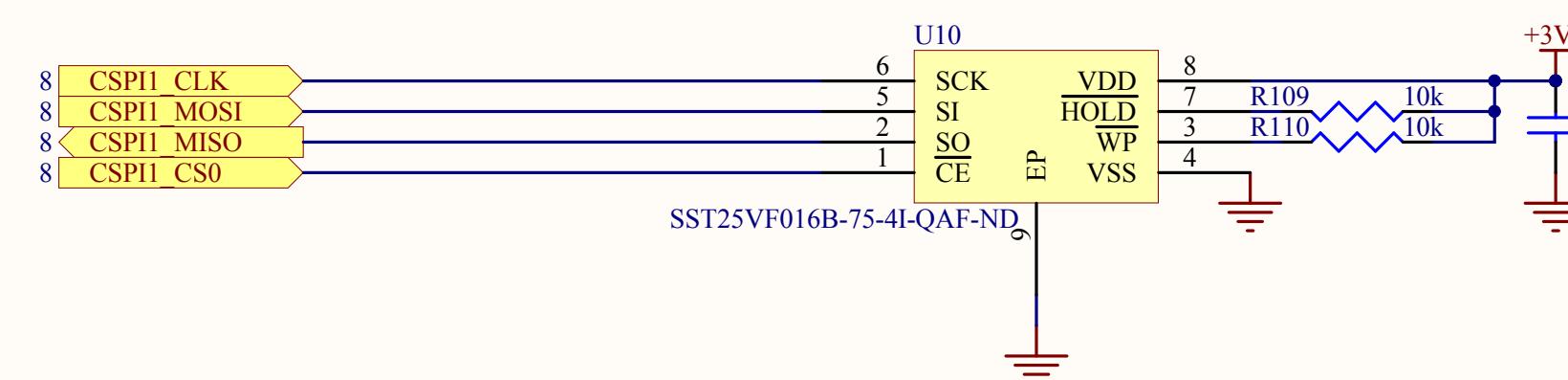


DESIGN NOTE:
Default Ethernet strapping options:
PHYAD2=0 - PHY address 0x1
MODE=0 - RGMII mode (10/100/1000 half/full duplex)
CLK125_EN: ref. clock enable
LED_MODE: tri-color dual mode

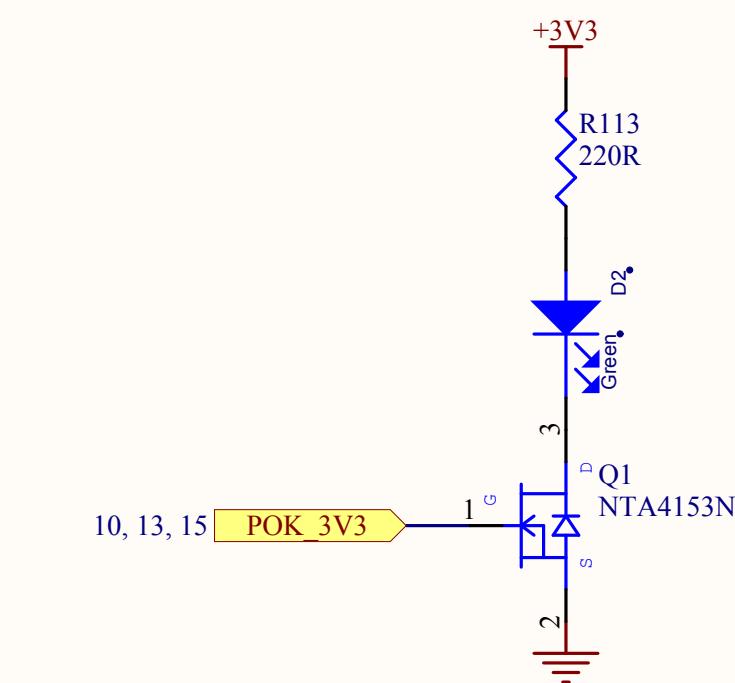


SPI FLASH, LED

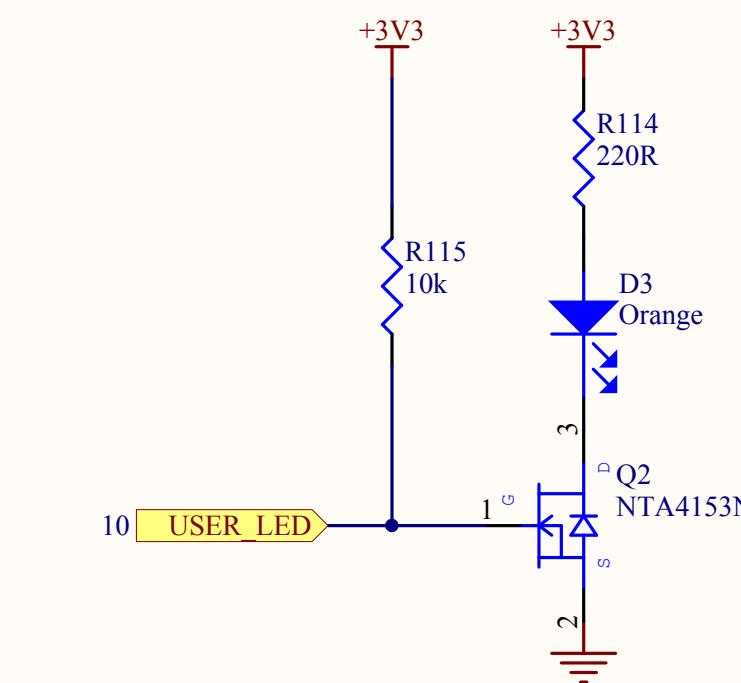
SPI NOR FLASH



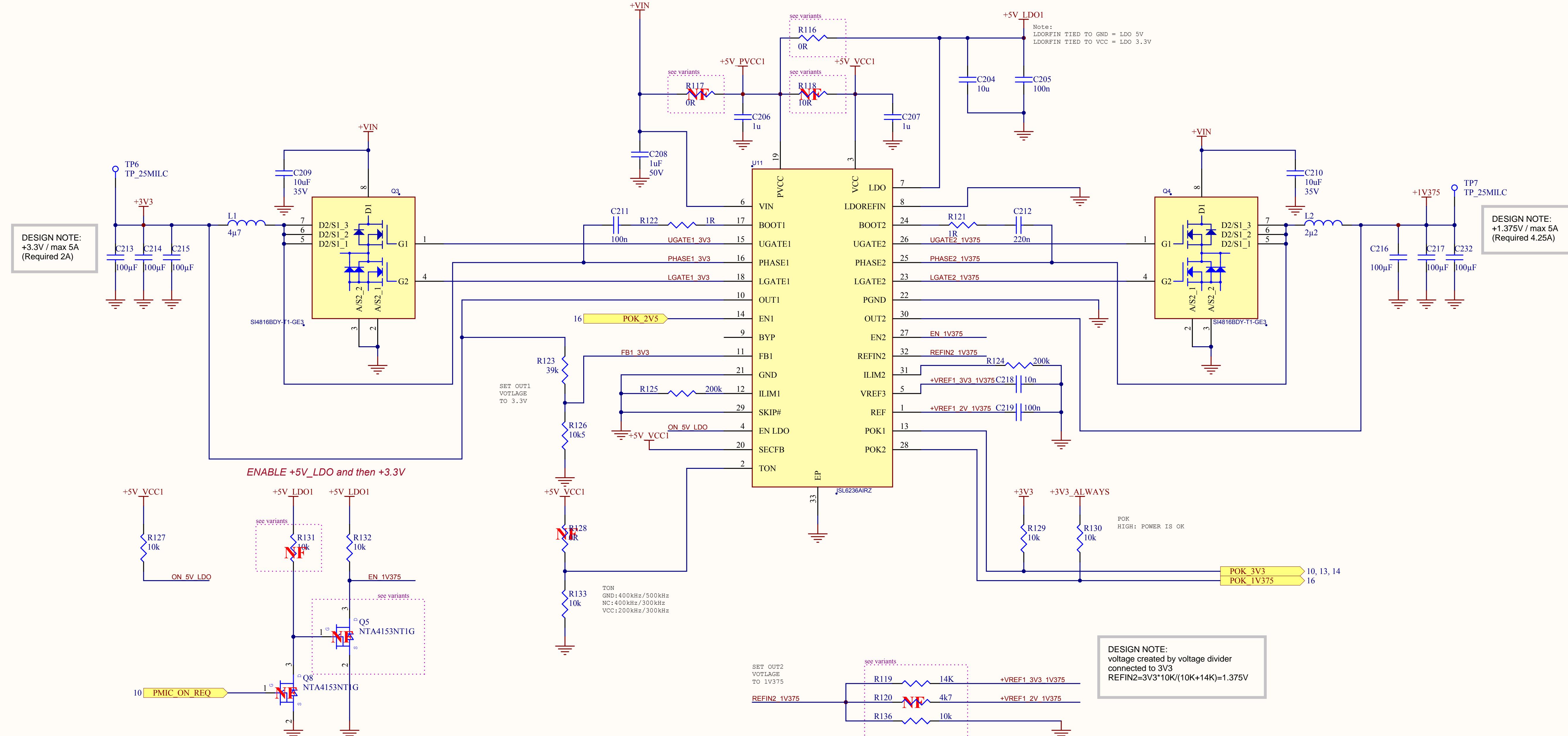
POWER LED



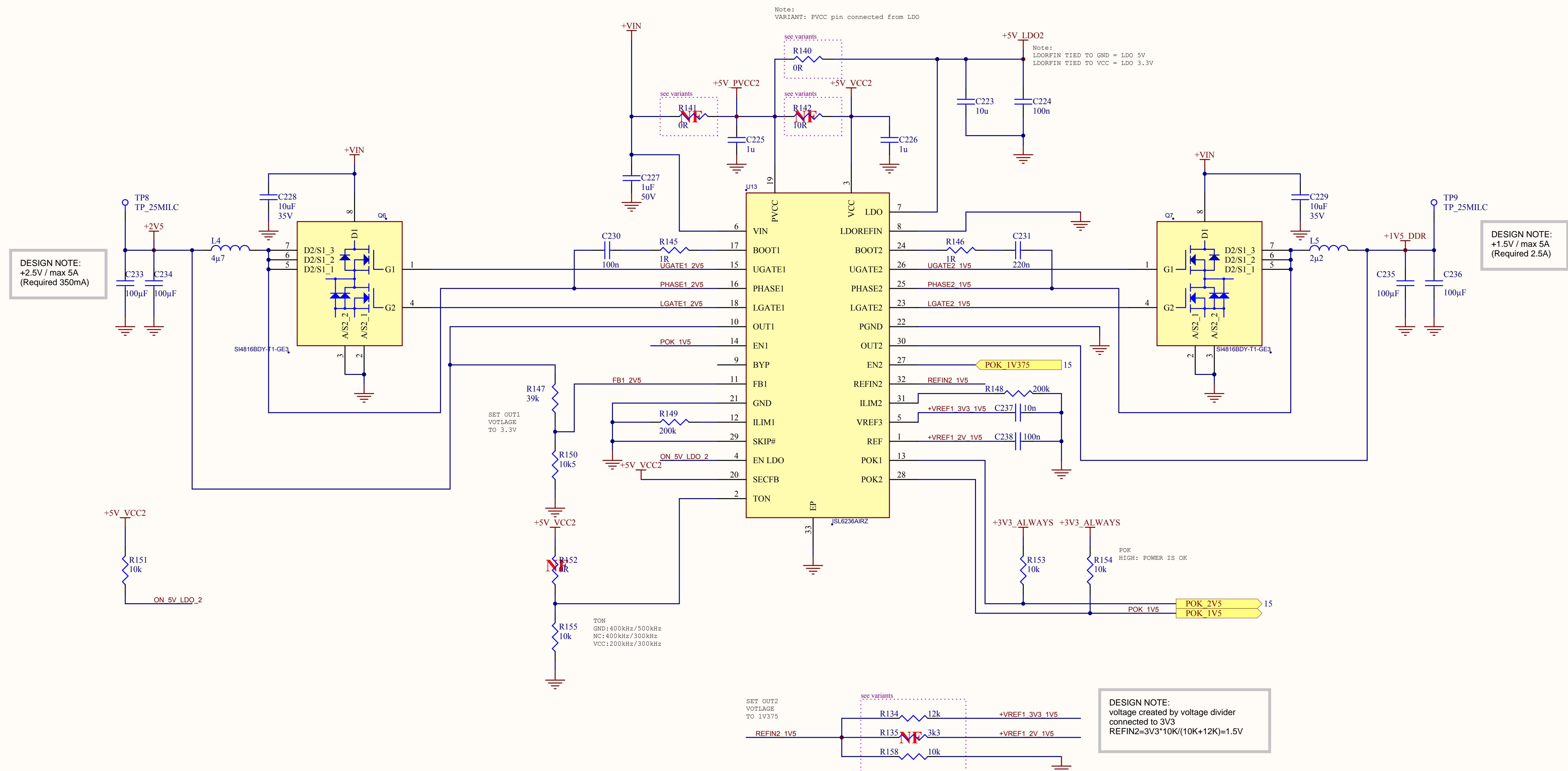
USER DEFINED LED



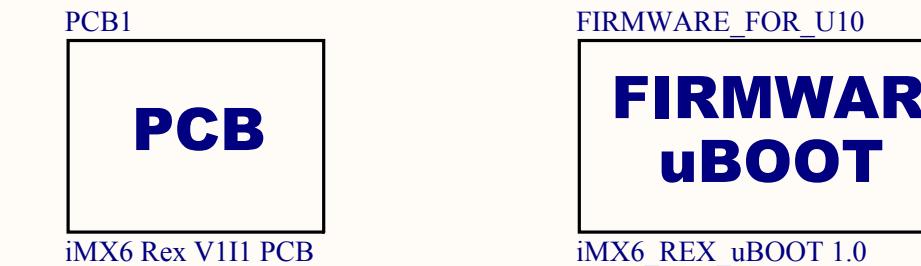
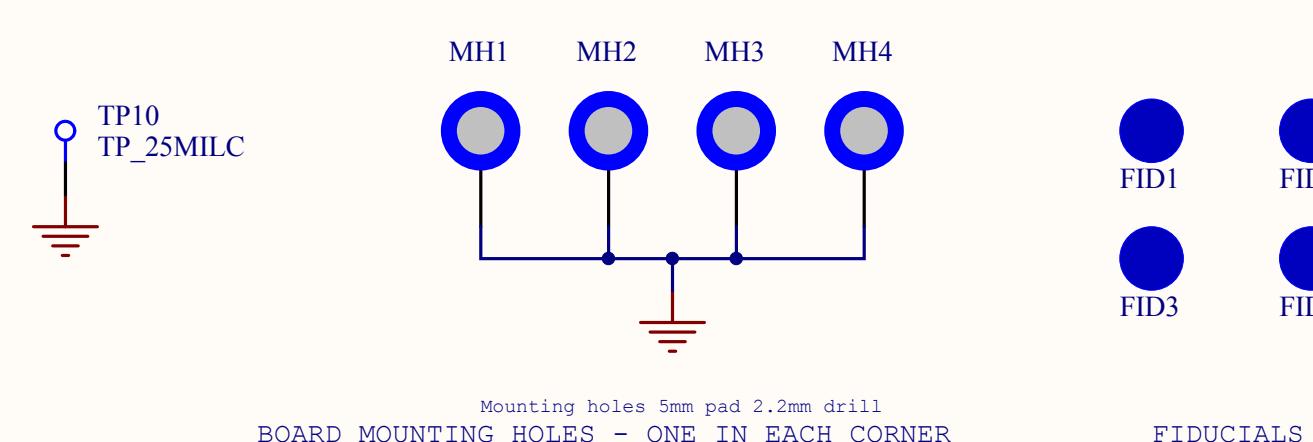
POWER +3.3V, +1.375V CON



POWER +2.5V, +1.5V CON

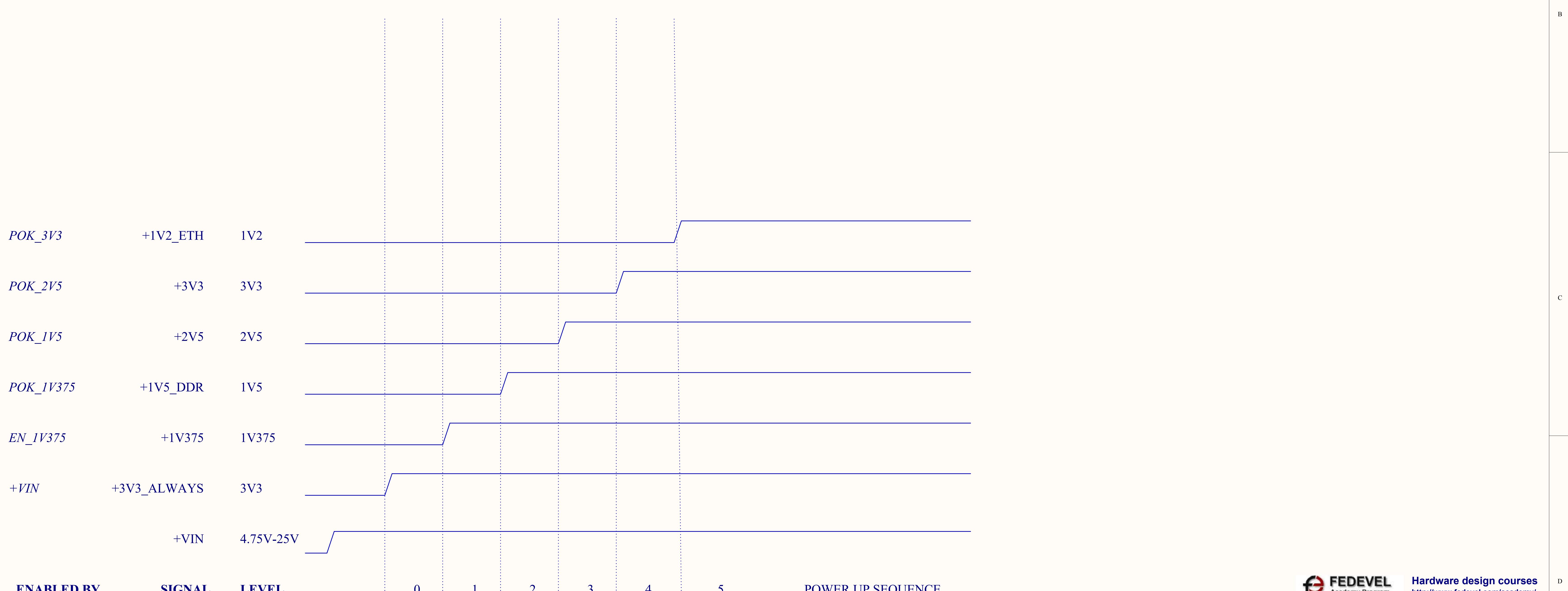


MECHANICAL



CPU - POWER SEQUENCING

+USB_VBUS	5V		
+DDR_VREF	0V75	+1V5_DDR	ref. for DDR memories, gen. with volt. divider
+1V2_VDD_ARM_CAP	1V2	iMX	cpu, core caps
+1V1_VDDSOC_CAP	1V1	iMX	core caps, cpu-sata, cpu-pcie, cpu-hdmi
OTHER USED SIGNAL	LEVEL	GEN BY	SUPPLIED FROM SIGNAL



ENABLED BY	SIGNAL	LEVEL
		0 1 2 3 4 5
		POWER UP SEQUENCE

DOC: REVISION HISTORY

A 05.06.2013 ADDED THE FOURTH LVDS DIFFERENTIAL PAIR DATA SIGNAL (LVDS0_TX3)

- signals LVDS0_TX3_P and LVDS0_TX3_N added to the second connector (J2)
- some signal on connector J2 has been moved to another position
- from second connector (J2) removed one +3V3 supply (one still remains connected)

B 07.06.2013 ADDED PULL-UP AND PULL-DOWN TO DEFINE BOARD VARIANT

- GPIO2_IO21 (pad G24) and GPIO2_IO22 (pad H25) moved from Unused to Control block and connected to pull-up and pull-down resistor



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CLOCKS (CPU & PCI)

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[01] - COVER PAGE.SchDoc

[02] - BLOCK DIAGRAM.SchDoc
[02] - BLOCK DIAGRAM.SchDoc

[03] - CONNECTORS.SchDoc
[03] - CONNECTORS.SchDoc

[04] - CPU - DDR3, DDR3 MEM.SchDoc
[04] - CPU - DDR3, DDR3 MEM.SchDoc

[05] - CPU - PCIE, SATA.SchDoc
[05] - CPU - PCIE, SATA.SchDoc

[06] - CPU - HDMI, LVDS.SchDoc
[06] - CPU - HDMI, LVDS.SchDoc

[07] - CPU - USB, ETHERNET.SchDoc
[07] - CPU - USB, ETHERNET.SchDoc

[08] - CPU - SPI, I2C, SD, MMC.SchDoc
[08] - CPU - SPI, I2C, SD, MMC.SchDoc

TEMPLATE NOTES

Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Company, Project and Version Revision

Mark Not Fitted Components as **NF**

Net Class Example



Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Title

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

[09] - CPU - UART, AUDIO.SchDoc
[09] - CPU - UART, AUDIO.SchDoc

[10] - CPU - JTAG, CONTROL.SchDoc
[10] - CPU - JTAG, CONTROL.SchDoc

[11] - CPU - POWER.SchDoc
[11] - CPU - POWER.SchDoc

[12] - CPU - UNUSED.SchDoc
[12] - CPU - UNUSED.SchDoc

[13] - ETHERNET PHY.SchDoc
[13] - ETHERNET PHY.SchDoc

[14] - SPI FLASH, LEDS.SchDoc
[14] - SPI FLASH, LEDS.SchDoc

[15] - PWR 3V3, 1V375.SchDoc
[15] - PWR 3V3, 1V375.SchDoc

[16] - PWR 2V5, 1V5.SchDoc
[16] - PWR 2V5, 1V5.SchDoc

[17] - MECH.SchDoc
[17] - MECH.SchDoc

[18] - POWER SEQUENCING.SchDoc
[18] - POWER SEQUENCING.SchDoc

[19] - DOC REVISION HISTORY.SchDoc
[19] - DOC REVISION HISTORY.SchDoc



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