IBIS Models User Guide

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1.0 Introduction

The Cyclone IV IBIS models model the operation of the I/O buffers in typical process, voltage, and temperature conditions. The IBIS file has been tested and verified using commercial tools.

This document explains how to use Cyclone IV IBIS models in simulations and contains a list of all IBIS models that Cyclone IV device supports.

For proper termination scheme, please refer to "*Chapter 6. I/O Features in Cyclone IV Devices*", Termination Scheme for I/O Standards section for the recommended and proper termination scheme of Cyclone IV Device Handbook. The handbook can be downloaded at:

http://www.altera.com/literature/hb/cyclone-iv/cyclone4-handbook.pdf

2.0 IBIS File Instruction

2.1 IBIS Specification

The IBIS model is currently using IBIS Specification v4.1. There are additional keywords that are supported in v4.1 but not in v3.2 and previous version. Users are advised to download the latest Visual IBIS Editor, version 4.0 Build 162 from Mentor Graphics in order to view and enabled the additional keywords from IBIS Specification v4.1. This is to prevent any error which might prompt from the IBIS checker on the updated keywords which are available in IBIS Specification v4.1 but not backward compatibility.

2.2 Package Modeling

The package resistance, inductance and capacitance (RLC) values that are currently defined under [Package] section in the IBIS file contain the lumped RLC value for 4CGX15_F169 package. For other package model values, please refer to the cyclone4_rlc.xls excel sheet which contains all the supported packages for Cyclone IV device. The excel sheet can be obtained from the following link:

http://www.altera.com/support/software/download/ibis/ibs-ibis_index.jsp

The IBIS file contains multiple models. Please refer to section 3.0 below for details on the model naming conventions.

3.0 Naming Nomenclature

3.1 All models except for Configuration Pins (refer Section 3.2)

All models follow the following naming method:

<I/O Standard>_<I/O>_<Features>

where,

<I/O Standard> refers to:

ttl33 - 3.3V LVTTL

ttl30 - 3.0V LVTTL

ttl25 - 2.5V LVTTL

ttl18 - 1.8V LVTTL

cmos33 - 3.3V LVCMOS

cmos30 - 3.0V LVCMOS

cmos15 - 1.5V LVCMOS

cmos12 - 1.2V LVCMOS

pci30 - 3.0V PCI

pcix30 - 3.0V PCI-X

hstl18c1 - 1.8V HSTL Class I

hstl15c1 - 1.5V HSTL Class I

hstl12c1 - 1.2V HSTL Class I

hstl18c2 - 1.8V HSTL Class II

hstl15c2 - 1.5V HSTL Class II

hstl12c2 - 1.2V HSTL Class II

sstl2c1 - 2.5V SSTL Class I

sstl18c1 - 1.8V SSTL Class I

sstl2c2 - 2.5V SSTL Class II

sstl18c2 - 1.8V SSTL Class II

dhstl18c1 - Differential 1.8V HSTL Class I

dhstl15c1 - Differential 1.5V HSTL Class I

dhstl12c1 - Differential 1.2V HSTL Class I

dhstl18c2 - Differential 1.8V HSTL Class II

dhstl15c2 - Differential 1.5V HSTL Class II

dhstl12c2 - Differential 1.2V HSTL Class II

dsstl2c1 - Differential 2.5V SSTL Class I

dsstl18c1 - Differential 1.8V SSTL Class I

dsstl2c2 - Differential 2.5V SSTL Class II

dsstl18c2 - Differential 1.8V SSTL Class II

lvds25 - 2.5V LVDS

mlvds25 - 2.5V mini-LVDS

ppds25 - 2.5V PPDS

rsds25 - 2.5V RSDS

lvpecl25 - 2.5V LVPECL

<I/O> refers to:

Top & Bottom I/O Bank (Begins with Letter 'c'):

cio - Column I/O

cin - Column input

co - Column output

ciop - Non-inverting pin, for differential I/O

cion - Inverting pin, for differential I/O

cop - Non-inverting pin, for differential driver

con - Inverting pin, for differential driver

cinp - Non-inverting pin, for differential receiver

cinn - Inverting pin, for differential receiver

Left & Right I/O Bank (Begins with Letter 'r'):

rio - Row I/O

rin - Row input

r**d**io - Row I/O, **DIFFIO pin** (Optional Pin Function)

r**d**in - Row input, **DIFFIO pin** (Optional Pin Function)

riop - Non-inverting pin, for differential I/O

rion - Inverting pin, for differential I/O

ro - Row Output

rop - Non-inverting pin, for differential driver

ron - Inverting pin, for differential driver

rinp - Non-inverting pin, for differential receiver

rinn - Inverting pin, for differential receiver

rdinp - Non-inverting pin, for differential receiver

rdinn - Inverting pin, for differential receiver

<Features> refers to:

s - Slow Slew Rate

m - Medium Slew Rate

f - Fast Slew Rate

p - PCI-clamp enabled

d8 - 8mA Drive Strength

r25 - 25ohm On-Chip Termination without Calibration

r50c - 50ohm On-Chip Termination with Calibration

on - Dedicated LVDS model with Pre-emphasis ON

off - Dedicated LVDS model with Pre-emphasis OFF

e3r - Non-dedicated LVDS/mini-LVDS/PPDS/RSDS with 3 external resistors

e1r - Non-dedicated RSDS with 1 external resistor

Example: sstl2c1_rio_d8f refers to

Cyclone IV, 2.5V SSTL Class I Row I/O model with 8ma drive strength for fast slew rate

3.2 Configuration Pins Naming Nomenclature

All models follow the following naming method:

<Voltage Standard>_<I/O>_<Config_pin>

Where,

<Voltage Standard> refers to:

3p3 - 3.3V

3p0 - 3.0V

2p5 - 2.5V

1p8 - 1.8V

1p5 - 1.5V

1p2 - 1.2V

<I/O> refers to:

io - I/O

o - Output

in - Input

<Config_pin> refers to:

condone - conf_done pin

nstatus - nstatus pin

dclk - dclk pin

tdo - JTAG tdo pin

nceo - nceo pin

flsh_nce_ncso - flash_nce pin & active-low output control signal

nreset - active-low reset output

navd - active-low address valid output

nwe - active-low write enable

noe - active-low output enable

asdo - active serial data output

data[15:0] - data pin

padd[23:0] - parallel address pin

init_done - init_done pin

crcerror - pin indicating the error detection circuitry has detected errors

Example: 3p0_io_nstatus refers to

Cyclone IV, 3.0V, nstatus configuration pin

4.0 List of Cyclone IV IBIS Models

4.1 1.2-V

cmos12_cin
cmos12_cio_d2
cmos12_cio_d4
cmos12_cio_d6
cmos12_cio_d8s
cmos12_cio_d10s
cmos12_cio_d12s
cmos12_cio_d8m
cmos12_cio_d10m
cmos12_cio_d12m
cmos12_cio_d8f
cmos12_cio_d10f
cmos12_cio_d12f
cmos12_cio_r50
cmos12_cio_r25
cmos12_cio_r50c
cmos12_cio_r25c

cmos12_rin
cmos12_rio_d2
cmos12_rio_d4
cmos12_rio_d6
cmos12_rio_d8s
cmos12_rio_d10s
cmos12_rio_d8m
cmos12_rio_d10m
cmos12_rio_d8f
cmos12_rio_d10f
cmos12_rio_r50
cmos12_rio_r50c

cmos12_rdin
cmos12_rdio_d2
cmos12_rdio_d4
cmos12_rdio_d6
cmos12_rido_d8s
cmos12_rdio_d10s
cmos12_rdio_d8m
cmos12_rdio_d10m
cmos12_rdio_d8f
cmos12_rdio_d10f
cmos12_rdio_r50
cmos12_rdio_r50c
1p2_tdo

4.2 1.5-V

cmos15_cin
cmos15_cio_d2
cmos15_cio_d4
cmos15_cio_d6
cmos15_cio_d8s
cmos15_cio_d10s
cmos15_cio_d12s
cmos15_cio_d16s
cmos15_cio_d8m
cmos15_cio_d10m
cmos15_cio_d12m
cmos15_cio_d16m
cmos15_cio_d8f
cmos15_cio_d10f
cmos15_cio_d12f
cmos15_cio_d16f
cmos15_cio_r50
cmos15_cio_r25
cmos15_cio_r50c
cmos15_cio_r25c

cmos15_rin
cmos15_rio_d2
cmos15_rio_d4
cmos15_rio_d6
cmos15_rio_d8s
cmos15_rio_d10s
cmos15_rio_d12s
cmos15_rio_d16s
cmos15_rio_d8m
cmos15_rio_d10m
cmos15_rio_d12m
cmos15_rio_d16m
cmos15_rio_d8f
cmos15_rio_d10f
cmos15_rio_d12f
cmos15_rio_d16f
cmos15_rio_r50
cmos15_rio_r25
cmos15_rio_r50c
cmos15_rio_r25c

cmos15_rdin
cmos15_rdio_d2
cmos15_rdio_d4
cmos15_rdio_d6
cmos15_rdio_d6
cmos15_rdio_d8s
cmos15_rdio_d10s
cmos15_rdio_d12s
cmos15_rdio_d16s
cmos15_rdio_d8m
cmos15_rdio_d10m
cmos15_rdio_d12m
cmos15_rdio_d16m
cmos15_rdio_d8f
cmos15_rdio_d10f
cmos15_rdio_d12f
cmos15_rdio_d16f
cmos15_rdio_r50
cmos15_rdio_r25
cmos15_rdio_r50c
cmos15_rdio_r25c
1p5_tdo

4.2 1.8-V

ttl18_cin
ttl18_cio_d2
ttl18_cio_d4
ttl18_cio_d6
ttl18_cio_d8s
ttl18_cio_d10s
ttl18_cio_d12s
ttl18_cio_d16s
ttl18_cio_d8m
ttl18_cio_d10m
ttl18_cio_d12m
ttl18_cio_d16m
ttl18_cio_d8f
ttl18_cio_d10f
ttl18_cio_d12f
ttl18_cio_d16f
ttl18_cio_r50
ttl18_cio_r25
ttl18_cio_r50c
ttl18_cio_r25c

ttl18_rin
ttl18_rio_d2
ttl18_rio_d4
ttl18_rio_d6
ttl18_rio_d8s
ttl18_rio_d10s
ttl18_rio_d12s
ttl18_rio_d16s
ttl18_rio_d8m
ttl18_rio_d10m
ttl18_rio_d12m
ttl18_rio_d16m
ttl18_rio_d8f
ttl18_rio_d10f
ttl18_rio_d12f
ttl18_rio_d16f
ttl18_rio_r50
ttl18_rio_r25
ttl18_rio_r50c
ttl18_rio_r25c

ttl18_rdin
ttl18_rdio_d2
ttl18_rdio_d4
ttl18_rdio_d6
ttl18_rdio_d8s
ttl18_rdio_d10s
ttl18_rdio_d12s
ttl18_rdio_d16s
ttl18_rdio_d8m
ttl18_rdio_d10m
ttl18_rdio_d12m
ttl18_rdio_d16m
ttl18_rdio_d8f
ttl18_rdio_d10f
ttl18_rdio_d12f
ttl18_rdio_d16f
ttl18_rdio_r50
ttl18_rdio_r25
ttl18_rdio_r50c
ttl18_rdio_r25c

1p8_condone
1p8_dclk
1p8_nceo
1p8_nstatus
1p8_tdo
1p8_rio_flsh_nce_ncso

1p8_rio_nreset
1p8_rio_navd
1p8_rio_nwe
1p8_rio_noe
1p8_rio_asdo_data1
1p8_rio_data0

1p8_cio_data[15:2]
1p8_cio_padd[19:0]
1p8_rio_padd[23:20]
1p8_ro_initdone
1p8_ro_crcerror

4.3 2.5-V

ttl25_cin
ttl25_cio_d4
ttl25_cio_d8s
ttl25_cio_d12s
ttl25_cio_d16s
ttl25_cio_d8m
ttl25_cio_d12m
ttl25_cio_d16m
ttl25_cio_d8f
ttl25_cio_d12f
ttl25_cio_d16f
ttl25_cin_p
ttl25_cio_d4p
ttl25_cio_d8p
ttl25_cio_d12p
ttl25_cio_d16p
ttl25_cio_r50
ttl25_cio_r25
ttl25_cio_r50c

ttl25_cio_r25c
ttl25_cio_r50p

ttl25_rin
ttl25_rio_d4
ttl25_rio_d8s
ttl25_rio_d12s
ttl25_rio_d16s
ttl25_rio_d8m
ttl25_rio_d12m
ttl25_rio_d16m
ttl25_rio_d8f
ttl25_rio_d12f
ttl25_rio_d16f
ttl25_rin_p
ttl25_rio_d4p
ttl25_rio_d8p
ttl25_rio_d12p
ttl25_rio_d16p
ttl25_rio_r50
ttl25_rio_r25
ttl25_rio_r50c

ttl25_rio_r25c
ttl25_rio_r50p

ttl25_rdin
ttl25_rdio_d4
ttl25_rdio_d8s
ttl25_rdio_d12s
ttl25_rdio_d16s
ttl25_rdio_d8m
ttl25_rdio_d12m
ttl25_rdio_d16m
ttl25_rdio_d8f
ttl25_rdio_d12f
ttl25_rdio_d16f
ttl25_rdin_p
ttl25_rdio_d4p
ttl25_rdio_d8p
ttl25_rdio_d12p
ttl25_rdio_d16p
ttl25_rdio_r50
ttl25_rdio_r25
ttl25_rdio_r50c
ttl25_rdio_r25c
ttl25_rdio_r50p

2p5_condone
2p5_dclk
2p5_nceo
2p5_nstatus
2p5_tdo
2p5_rio_flsh_nce_ncso
2p5_rio_nreset
2p5_rio_navd
2p5_rio_nwe
2p5_rio_noe
2p5_rio_asdo_data1
2p5_rio_data0
2p5_cio_data[15:2]
2p5_cio_padd[19:0]
2p5_rio_padd[23:20
2p5_ro_initdone
2p5_ro_crcerror

4.4 3.0-V LVTTL

ttl30_cin
ttl30_cio_d4
ttl30_cio_d8s
ttl30_cio_d12s
ttl30_cio_d16s
ttl30_cio_d8m
ttl30_cio_d12m
ttl30_cio_d16m
ttl30_cio_d8f
ttl30_cio_d12f
ttl30_cio_d16f
ttl30_cio_r50
ttl30_cio_r25
ttl30_cio_r50c
ttl30_cio_r25c
ttl30_cin_p
ttl30_cio_d4p
ttl30_cio_d8p
ttl30_cio_d12p
ttl30_cio_d16p
ttl30_rin
ttl30_rio_d4
ttl30_rio_d8s
ttl30_rio_d12s
ttl30_rio_d16s
ttl30_rio_d8m
ttl30_rio_d12m
ttl30_rio_d16m
ttl30_rio_d8f
ttl30_rio_d12f

ttl30_rio_d16f
ttl30_rio_r50
ttl30_rio_r25
ttl30_rio_r50c
ttl30_rio_r25c
ttl30_rin_p
ttl30_rio_d4p
ttl30_rio_d8p
ttl30_rio_d12p
ttl30_rio_d16p

ttl30_rdin
ttl30_rdio_d4
ttl30_rdio_d8s
ttl30_rdio_d12s
ttl30_rdio_d16s
ttl30_rdio_d8m
ttl30_rdio_d12m
ttl30_rdio_d16m
ttl30_rdio_d8f
ttl30_rdio_d12f
ttl30_rdio_d16f
ttl30_rdio_r50
ttl30_rdio_r25
ttl30_rdio_r50c
ttl30_rdio_r25c
ttl30_rdin_p
ttl30_rdio_d4p
ttl30_rdio_d8p
ttl30_rdio_d12p
ttl30_rdio_d16p

3p0_condone
3p0_dclk
3p0_nceo
3p0_nstatus
3p0_tdo
3p0_rio_flsh_nce_ncso

3p0_rio_nreset
3p0_rio_navd
3p0_rio_nwe
3p0_rio_noe
3p0_rio_asdo_data1
3p0_rio_data0

3p0_cio_data[15:2]
3p0_cio_padd[19:0]
3p0_rio_padd[23:20]
3p0_ro_crcerror
3p0_ro_initdone

4.5 3.3-V LVTTL

ttl33_cin
ttl33_cio_d4
ttl33_cio_d8
ttl33_cin_p
ttl33_cio_d4p
ttl33_cio_d8p
ttl30_cio_r50p

ttl33_rin
ttl33_rio_d4
ttl33_rio_d8
ttl33_rin_p
ttl33_rio_d4p
ttl33_rio_d8p
ttl30_rio_r50p

ttl33_rdin
ttl33_rdio_d4
ttl33_rdio_d8
ttl33_rdin_p
ttl33_rdio_d4p
ttl33_rdio_d8p
ttl30_rdio_r50p

3p3_condone
3p3_dclk
3p3_nceo
3p3_nstatus
3p3_tdo
3p3_rio_flsh_nce_ncso

3p3_rio_ncso
3p3_rio_nreset
3p3_rio_navd
3p3_rio_nwe
3p3_rio_noe

3p3_rio_asdo_data1
3p3_rio_data0
3p3_cio_data[15:2]
3p3_cio_padd[19:0]
3p3_rio_padd[23:20]
3p3_ro_crcerror
3p3_ro_initdone

4.6 3.0-V CMOS

cmos30_cin
cmos30_cio_d4

cmos30_cio_d8s
cmos30_cio_d8s

cmos30_cio_d16s
cmos30_cio_d8m

cmos30_cio_d12m
cmos30_cio_d16m
cmos30_cio_d8f
cmos30_cio_d12f
cmos30_cio_d16f
cmos30_cio_r50
cmos30_cio_r25
cmos30_cio_r50c
cmos30_cio_r25c
cmos30_cin_p
cmos30_cio_d4p
cmos30_cio_d8p
cmos30_cio_d12p
cmos30_cio_d16p
cmos30_cio_r50p

cmos30_rin
cmos30_rio_d4
cmos30_rio_d8s
cmos30_rio_d12s
cmos30_rio_d16s
cmos30_rio_d8m
cmos30_rio_d12m
cmos30_rio_d16m
cmos30_rio_d8f
cmos30_rio_d12f
cmos30_rio_d16f
cmos30_rio_r50
cmos30_rio_r25
cmos30_rio_r50c
cmos30_rio_r25c
cmos30_rin_p
cmos30_rio_d4p
cmos30_rio_d8p
cmos30_rio_d12p
cmos30_rio_d16p
cmos30_rio_r50p

cmos30_rdin
cmos30_rdio_d4
cmos30_rdio_d8s
cmos30_rdio_d12s
cmos30_rdio_d16s
cmos30_rdio_d8m
cmos30_rdio_d12m
cmos30_rdio_d16m
cmos30_rdio_d8f
cmos30_rdio_d12f
cmos30_rdio_d16f
cmos30_rdio_r50
cmos30_rdio_r25
cmos30_rdio_r50c
cmos30_rdio_r25c
cmos30_rdin_p
cmos30_rdio_d4p
cmos30_rdio_d8p
cmos30_rdio_d12p
cmos30_rdio_d16p
cmos30_rdio_r50p

4.7 3.3-V CMOS

cmos33_cin
cmos33_cio_d2
cmos33_cin_p
cmos33_cio_d2p

cmos33_rin
cmos33_rio_d2
cmos33_rin_p
cmos33_rio_d2p

cmos33_rdin
cmos33_rdio_d2
cmos33_rdin_p
cmos33_rdio_d2p

4.8 3.0-V PCI

pci30_cin
pci30_c

pci30_rin
pci30_r

pci30_rdin
pci30_rdio

4.9 3.0-V PCI-X

pcix30_cin
pcix30_c

pcix30_rin
pcix30_r

pcix30_rdin
pcix30_rdio

4.10 1.2-V HSTL

hstl12_cin
hstl12c1_cio_d8s
hstl12c1_cio_d10s
hstl12c1_cio_d12s
hstl12c2_cio_d14s

hstl12c1_cio_d8m
hstl12c1_cio_d10m
hstl12c1_cio_d12m
hstl12c2_cio_d14m
hstl12c1_cio_d8f

hstl12c1_cio_d10f
hstl12c1_cio_d12f
hstl12c2_cio_d14f
hstl12c1_cio_r50
hstl12c2_cio_r25

hstl12c1_cio_r50c	hstl12_rin	hstl12_rdin
hstl12c2_cio_r25c	hstl12c1_rio_d8s	hstl12c1_rdio_d8s
	hstl12c1_rio_d10s	hstl12c1_rdio_d10s
	hstl12c1_rio_d8m	hstl12c1_rdio_d8m
	hstl12c1_rio_d10m	hstl12c1_rdio_d10m
	hstl12c1_rio_d8f	hstl12c1_rdio_d8f
	hstl12c1_rio_d10f	hstl12c1_rdio_d10f
	hstl12c1_rio_r50	hstl12c1_rdio_r50
	hstl12c1_rio_r50c	hstl12c1_rdio_r50c

4.11 1.5-V HSTL

hstl15_cin	hstl15_rin	hstl15_rdin
hstl15c1_cio_d8s	hstl15c1_rio_d8s	hstl15c1_rdio_d8s
hstl15c1_cio_d10s	hstl15c1_rio_d10s	hstl15c1_rdio_d10s
hstl15c1_cio_d12s	hstl15c1_rio_d12s	hstl15c1_rdio_d12s
hstl15c1_cio_d8m	hstl15c1_rio_d8m	hstl15c1_rdio_d8m
hstl15c1_cio_d10m	hstl15c1_rio_d10m	hstl15c1_rdio_d10m
hstl15c1_cio_d12m	hstl15c1_rio_d12m	hstl15c1_rdio_d12m
hstl15c1_cio_d8f	hstl15c1_rio_d8f	hstl15c1_rdio_d8f
hstl15c1_cio_d10f	hstl15c1_rio_d10f	hstl15c1_rdio_d10f
hstl15c1_cio_d12f	hstl15c1_rio_d12f	hstl15c1_rdio_d12f
hstl15c1_cio_r50	hstl15c2_rio_d16s	hstl15c2_rdio_d16s
hstl15c2_cio_r25	hstl15c2_rio_d16m	hstl15c2_rdio_d16m
hstl15c1_cio_r50c	hstl15c2_rio_d16f	hstl15c2_rdio_d16f
hstl15c2_cio_r25c	hstl15c1_rio_r50	hstl15c1_rdio_r50
hstl15c2_cio_d16s	hstl15c2_rio_r25	hstl15c2_rdio_r25
hstl15c2_cio_d16m	hstl15c1_rio_r50c	hstl15c1_rdio_r50c
hstl15c2_cio_d16f	hstl15c2_rio_r25c	hstl15c2_rdio_r25c

4.12 1.8-V HSTL

hstl18_cin	hstl18_rin	hstl18_rdin
hstl18c1_cio_d8s	hstl18c1_rio_d8s	hstl18c1_rdio_d8s
hstl18c1_cio_d10s	hstl18c1_rio_d10s	hstl18c1_rdio_d10s
hstl18c1_cio_d12s	hstl18c1_rio_d12s	hstl18c1_rdio_d12s
hstl18c1_cio_d8m	hstl18c1_rio_d8m	hstl18c1_rdio_d8m
hstl18c1_cio_d10m	hstl18c1_rio_d10m	hstl18c1_rdio_d10m
hstl18c1_cio_d12m	hstl18c1_rio_d12m	hstl18c1_rdio_d12m
hstl18c1_cio_d8f	hstl18c1_rio_d8f	hstl18c1_rdio_d8f
hstl18c1_cio_d10f	hstl18c1_rio_d10f	hstl18c1_rdio_d10f
hstl18c1_cio_d12f	hstl18c1_rio_d12f	hstl18c1_rdio_d12f
hstl18c1_cio_r50	hstl18c2_rio_d16s	hstl18c2_rdio_d16s
hstl18c2_cio_r25	hstl18c2_rio_d16m	hstl18c2_rdio_d16m
hstl18c1_cio_r50c	hstl18c2_rio_d16f	hstl18c2_rdio_d16f
hstl18c2_cio_r25c	hstl18c1_rio_r50	hstl18c1_rdio_r50
hstl18c2_cio_d16s	hstl18c2_rio_r25	hstl18c2_rdio_r25
hstl18c2_cio_d16m	hstl18c1_rio_r50c	hstl18c1_rdio_r50c
hstl18c2_cio_d16f	hstl18c2_rio_r25c	hstl18c2_rdio_r25c

4.13 1.8-V SSTL

sstl18_cin	sstl18_rin	sstl18_rdin
sstl18c1_cio_d8s	sstl18c1_rio_d8s	sstl18c1_rdio_d8s
sstl18c1_cio_d10s	sstl18c1_rio_d10s	sstl18c1_rdio_d10s
sstl18c1_cio_d12s	sstl18c1_rio_d12s	sstl18c1_rdio_d12s
sstl18c1_cio_d8m	sstl18c1_rio_d8m	sstl18c1_rdio_d8m
sstl18c1_cio_d10m	sstl18c1_rio_d10m	sstl18c1_rdio_d10m
sstl18c1_cio_d12m	sstl18c1_rio_d12m	sstl18c1_rdio_d12m
sstl18c1_cio_d8f	sstl18c1_rio_d8f	sstl18c1_rdio_d8f
sstl18c1_cio_d10f	sstl18c1_rio_d10f	sstl18c1_rdio_d10f
sstl18c1_cio_d12f	sstl18c1_rio_d12f	sstl18c1_rdio_d12f
sstl18c2_cio_d12s	sstl18c2_rio_d12s	sstl18c2_rdio_d12s
sstl18c2_cio_d16s	sstl18c2_rio_d16s	sstl18c2_rdio_d16s
sstl18c2_cio_d12m	sstl18c2_rio_d12m	sstl18c2_rdio_d12m
sstl18c2_cio_d16m	sstl18c2_rio_d16m	sstl18c2_rdio_d16m
sstl18c2_cio_d12f	sstl18c2_rio_d12f	sstl18c2_rdio_d12f
sstl18c2_cio_d16f	sstl18c2_rio_d16f	sstl18c2_rdio_d16f
sstl18c1_cio_r50	sstl18c1_rio_r50	sstl18c1_rdio_r50
sstl18c2_cio_r25	sstl18c2_rio_r25	sstl18c2_rdio_r25
sstl18c1_cio_r50c	sstl18c1_rio_r50c	sstl18c1_rdio_r50c
sstl18c2_cio_r25c	sstl18c2_rio_r25c	sstl18c2_rdio_r25c

4.14 2.5-V SSTL

sstl2_cin	sstl2_rin	sstl2_rdin
sstl2c1_cio_d8s	sstl2c1_rio_d8s	sstl2c1_rdio_d8s
sstl2c1_cio_d12s	sstl2c1_rio_d12s	sstl2c1_rdio_d12s
sstl2c1_cio_d8m	sstl2c1_rio_d8m	sstl2c1_rdio_d8m
sstl2c1_cio_d12m	sstl2c1_rio_d12m	sstl2c1_rdio_d12m
sstl2c1_cio_d8f	sstl2c1_rio_d8f	sstl2c1_rdio_d8f
sstl2c1_cio_d8f	sstl2c1_rio_d12f	sstl2c1_rdio_d12f
sstl2c1_cio_r50	sstl2c1_rio_r50	sstl2c1_rdio_r50
sstl2c2_cio_r25	sstl2c2_rio_r25	sstl2c2_rdio_r25
sstl2c1_cio_r50c	sstl2c1_rio_r50c	sstl2c1_rdio_r50c
sstl2c2_cio_r25c	sstl2c2_rio_r25c	sstl2c2_rdio_r25c
sstl2c2_cio_d16s	sstl2c2_rio_d16s	sstl2c2_rdio_d16s
sstl2c2_cio_d16m	sstl2c2_rio_d16m	sstl2c2_rdio_d16m
sstl2c2_cio_d16f	sstl2c2_rio_d16f	sstl2c2_rdio_d16f

4.14 Differential 1.2-V HSTL

dhstl12_cin	dhstl12c1_cio_d8f	dhstl12_rdin
dhstl12c1_cio_d8s	dhstl12c1_cio_d10f	
dhstl12c1_cio_d10s	dhstl12c1_cio_d12f	
dhstl12c1_cio_d12s	dhstl12c1_cio_r50	
dhstl12c1_cio_d8m	dhstl12c1_cio_r50c	
dhstl12c1_cio_d10m		
dhstl12c1_cio_d12m		

4.15 Differential 1.5-V HSTL

dhstl15_cin
dhstl15_rdin
dhstl15c1_cio_d8s
dhstl15c1_cio_d10s
dhstl15c1_cio_d12s
dhstl15c1_cio_d8m
dhstl15c1_cio_d10m
dhstl15c1_cio_d12m
dhstl15c1_cio_d8f
dhstl15c1_cio_d10f
dhstl15c1_cio_d12f
dhstl15c1_cio_r50
dhstl15c1_cio_r50c

4.16 Differential 1.8-V HSTL

dhstl18_cin
dhstl18_rdin
dhstl18c1_cio_d8s
dhstl18c1_cio_d10s
dhstl18c1_cio_d12s
dhstl18c1_cio_d8m
dhstl18c1_cio_d10m
dhstl18c1_cio_d12m
dhstl18c1_cio_d8f
dhstl18c1_cio_d10f
dhstl18c1_cio_d12f
dhstl18c1_cio_r50
dhstl18c1_cio_r50c

4.17 Differential 1.8-V SSTL

dsstl18_cin
dsstl18_rdin
dsstl18c1_cio_d8s
dsstl18c1_cio_d10s
dsstl18c1_cio_d12s
dsstl18c1_cio_d8m
dsstl18c1_cio_d10m
dsstl18c1_cio_d12m
dsstl18c1_cio_d8f
dsstl18c1_cio_d10f
dsstl18c1_cio_d12f
dsstl18c1_cio_r50
dsstl18c1_cio_r50c

4.18 Differential 2.5-V SSTL

dsstl2_cin
dsstl2c1_cio_d8s
dsstl2c1_cio_d12s
dsstl2c1_cio_d8m
dsstl2c1_cio_d12m
dsstl2c1_cio_d8f
dsstl2c1_cio_d12f
dsstl2c1_cio_r50
dsstl2c2_cio_r25
dsstl2c1_cio_r50c
dsstl2c2_cio_r25c
dsstl2c2_cio_d16s
dsstl2c2_cio_d16m
dsstl2c2_cio_d16f
dsstl2_rdin
dsstl2c1_rdio_d8s
dsstl2c1_rdio_d12s
dsstl2c1_rdio_d8m
dsstl2c1_rdio_d12m
dsstl2c1_rdio_d8f
dsstl2c1_rdio_d12f

dsstl2c1_rdio_r50
dsstl2c2_rdio_r25
dsstl2c1_rdio_r50c
dsstl2c2_rdio_r25c
dsstl2c2_rdio_d16s
dsstl2c2_rdio_d16m
dsstl2c2_rdio_d16f

4.19 2.5V LVDS

lvds25_co_e3r
lvds25_cin
lvds25_rin
lvds25_ro_on
lvds25_ro_off
lvds25_ro_e3r

4.20 2.5V Mini-LVDS

mlvds25_co_e3r
mlvds25_ro_on
mlvds25_ro_off
mlvds25_ro_e3r

4.21 2.5V PPDS

ppds25_co_e3r
ppds25_ro_on
ppds25_ro_off
ppds25_ro_e3r

4.22 2.5V RSDS

rsds25_co_e3r
rsds25_co_e1r
rsds25_ro_on
rsds25_ro_off
rsds25_ro_e3r
rsds25_ro_e1r

4.23 2.5V LVPECL

lvpecl25_cin
lvpecl25_rdin

5.0 Cyclone IV IBIS File Revision History

File rev 2.0

Date release: July 2010

- Release for the following models:

  Top & Bottom I/O bank

  - 1.2V LVCMOS Input
  - 1.2V LVCMOS 2mA, 4mA, 6mA, 8mA, 10mA & 12mA I/O
  - 1.2V LVCMOS 25 Ohm & 50 Ohm Series OCT without Calibration I/O
  - 1.2V LVCMOS 25 Ohm & 50 Ohm Series OCT with Calibration I/O
  - 1.5V LVCMOS Input
  - 1.5V LVCMOS 2mA, 4mA, 6mA, 8mA, 10mA, 12mA & 16mA I/O
  - 1.5V LVCMOS 25 Ohm & 50 Ohm Series OCT without Calibration I/O
  - 1.5V LVCMOS 25 Ohm & 50 Ohm Series OCT with Calibration I/O
  - 1.8V LVTTL Input
  - 1.8V LVTTL 2mA, 4mA, 6mA, 8mA, 10mA ,12mA & 16mA I/O
  - 1.8V LVTTL 25 Ohm & 50 Ohm Series OCT without Calibration I/O
  - 1.8V LVTTL 25 Ohm & 50 Ohm Series OCT with Calibration I/O
  - 2.5V LVTTL Input
  - 2.5V LVTTL 4mA, 8mA, 12mA & 16mA I/O
  - 2.5V LVTTL 25 Ohm & 50 Ohm Series OCT without Calibration I/O
  - 2.5V LVTTL 25 Ohm & 50 Ohm Series OCT with Calibration I/O
  - 2.5V LVTTL with PCI diode enabled Input
  - 2.5V LVTTL 4mA, 8mA, 12mA & 16mA with PCI diode enabled I/O
  - 3.0V LVTTL Input
  - 3.0V LVTTL 4mA, 8mA, 12mA & 16mA I/O
  - 3.0V LVTTL 25 Ohm & 50 Ohm Series OCT without Calibration I/O
  - 3.0V LVTTL 25 Ohm & 50 Ohm Series OCT with Calibration I/O
  - 3.0V LVTTL with PCI diode enabled Input
  - 3.0V LVTTL 4mA, 8mA, 12mA & 16mA with PCI diode enabled I/O
  - 3.3V LVTTL Input
  - 3.3V LVTTL 4mA & 8mA I/O
  - 3.3V LVTTL with PCI diode enabled Input
  - 3.3V LVTTL 4mA & 8mA with PCI diode enabled I/O
  - 3.0V LVCMOS Input
  - 3.0V LVCMOS 4mA, 8mA, 12mA & 16mA I/O
  - 3.0V LVCMOS 25 Ohm & 50 Ohm Series OCT without Calibration I/O
  - 3.0V LVCMOS 25 Ohm & 50 Ohm Series OCT with Calibration I/O
  - 3.0V LVCMOS with PCI diode enabled Input
  - 3.0V LVCMOS 4mA, 8mA, 12mA & 16mA with PCI diode enabled I/O
  - 3.3V LVCMOS Input
  - 3.3V LVCMOS 2mA I/O
  - 3.3V LVCMOS with PCI diode enabled Input
  - 3.3V LVCMOS 2mA with PCI diode enabled I/O
  - 3.0V PCI Input
  - 3.0V PCI I/O
  - 3.0V PCI-X Input
  - 3.0V PCI-X I/O
  - 1.2V HSTL Input
  - 1.2V HSTL Class I 8mA, 10mA & 12mA I/O
  - 1.2V HSTL Class II 14mA I/O
  - 1.2V HSTL Class I 50-Ohms Series OCT With Calibration I/O
  - 1.2V HSTL Class II 25-Ohms Series OCT With Calibration I/O
  - 1.5V HSTL Input
  - 1.5V HSTL Class I 8mA, 10mA & 12mA I/O
  - 1.5V HSTL Class II 16mA I/O
  - 1.5V HSTL Class I 50-Ohms Series OCT With Calibration I/O
  - 1.5V HSTL Class II 25-Ohms Series OCT With Calibration I/O
  - 1.8V HSTL Input
  - 1.8V HSTL Class I 8mA, 10mA & 12mA I/O
  - 1.8V HSTL Class II 16mA I/O
  - 1.8V HSTL Class I 50-Ohms Series OCT With Calibration I/O
  - 1.8V HSTL Class II 25-Ohms Series OCT With Calibration I/O
  - 1.8V SSTL Input
  - 1.8V SSTL Class I 8mA, 10mA & 12mA I/O

- 1.8V SSTL Class II 12mA & 16mA I/O
- 1.8V SSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.8V SSTL Class II 25-Ohms Series OCT With Calibration I/O
- 2.5V SSTL Input
- 2.5V SSTL Class I 8mA & 12mA I/O
- 2.5V SSTL Class II 16mA I/O
- 2.5V SSTL Class I 50-Ohms Series OCT With Calibration I/O
- 2.5V SSTL Class II 25-Ohms Series OCT With Calibration I/O
- 1.2V Differential HSTL Input
- 1.2V Differential HSTL Class I 8mA, 10mA & 12mA I/O
- 1.2V Differential HSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.5V Differential HSTL Input
- 1.5V Differential HSTL Class I 8mA, 10mA & 12mA I/O
- 1.5V Differential HSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.8V Differential HSTL Input
- 1.8V Differential HSTL Class I 8mA, 10mA & 12mA I/O
- 1.8V Differential HSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.8V Differential SSTL Input
- 1.8V Differential SSTL Class I 8mA, 10mA & 12mA I/O
- 1.8V Differential SSTL Class I 50-Ohms Series OCT With Calibration I/O
- 2.5V Differential SSTL Input
- 2.5V Differential SSTL Class I 8mA & 12mA I/O
- 2.5V Differential SSTL Class II 16mA I/O
- 2.5V Differential SSTL Class I 50-Ohms Series OCT With Calibration I/O
- 2.5V Differential SSTL Class II 25-Ohms Series OCT With Calibration I/O
- 2.5V LVPECL Input
- 2.5V LVDS Input
- 2.5V LVDS Output
- 2.5V mini-LVDS Output
- 2.5V PPDS Output
- 2.5V RSDS Output

Left & Right I/O Bank

- 1.2V LVCMOS Input
- 1.2V LVCMOS 2mA, 4mA, 6mA, 8mA & 10mA I/O
- 1.2V LVCMOS 50 Ohm Series OCT without Calibration I/O
- 1.2V LVCMOS 50 Ohm Series OCT with Calibration I/O
- 1.5V LVCMOS Input
- 1.5V LVCMOS 2mA, 4mA, 6mA, 8mA, 10mA, 12mA & 16mA I/O
- 1.5V LVCMOS 25 Ohm & 50 Ohm Series OCT without Calibration I/O
- 1.5V LVCMOS 25 Ohm & 50 Ohm Series OCT with Calibration I/O
- 1.8V LVTTL Input
- 1.8V LVTTL 2mA, 4mA, 6mA, 8mA, 10mA ,12mA & 16mA I/O
- 1.8V LVTTL 25 Ohm & 50 Ohm Series OCT without Calibration I/O
- 1.8V LVTTL 25 Ohm & 50 Ohm Series OCT with Calibration I/O
- 2.5V LVTTL Input
- 2.5V LVTTL 4mA, 8mA, 12mA & 16mA I/O
- 2.5V LVTTL 25 Ohm & 50 Ohm Series OCT without Calibration I/O
- 2.5V LVTTL 25 Ohm & 50 Ohm Series OCT with Calibration I/O
- 2.5V LVTTL PCI diode enabled Input
- 2.5V LVTTL 4mA, 8mA, 12mA & 16mA with PCI diode enabled I/O
- 3.0V LVTTL Input
- 3.0V LVTTL 4mA, 8mA, 12mA & 16mA I/O
- 3.0V LVTTL 25 Ohm & 50 Ohm Series OCT without Calibration I/O
- 3.0V LVTTL 25 Ohm & 50 Ohm Series OCT with Calibration I/O
- 3.0V LVTTL with PCI diode enabled Input
- 3.0V LVTTL 4mA, 8mA, 12mA & 16mA with PCI diode enabled I/O
- 3.3V LVTTL Input
- 3.3V LVTTL 4mA & 8mA I/O
- 3.3V LVTTL with PCI diode enabled Input
- 3.3V LVTTL 4mA & 8mA with PCI diode enabled I/O
- 3.0V LVCMOS Input
- 3.0V LVCMOS 4mA, 8mA, 12mA & 16mA I/O
- 3.0V LVCMOS 25 Ohm & 50 Ohm Series OCT without Calibration I/O
- 3.0V LVCMOS 25 Ohm & 50 Ohm Series OCT with Calibration I/O
- 3.0V LVCMOS with PCI diode enabled Input
- 3.0V LVCMOS 4mA, 8mA, 12mA & 16mA with PCI diode enabled I/O
- 3.3V LVCMOS Input
- 3.3V LVCMOS 2mA I/O
- 3.3V LVCMOS with PCI diode enabled Input

- 3.3V LVCMOS 2mA with PCI diode enabled I/O
- 3.0V PCI Input
- 3.0V PCI I/O
- 3.0V PCI-X Input
- 3.0V PCI-X I/O
- 1.2V HSTL Input
- 1.2V HSTL Class I 8mA & 10mA I/O
- 1.2V HSTL Class II 14mA I/O
- 1.2V HSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 1.2V HSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.5V HSTL Input
- 1.5V HSTL Class I 8mA, 10mA & 12mA I/O
- 1.5V HSTL Class II 16mA I/O
- 1.5V HSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 1.5V HSTL Class II 25-Ohms Series OCT Without Calibration I/O
- 1.5V HSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.5V HSTL Class II 25-Ohms Series OCT With Calibration I/O
- 1.8V HSTL Input
- 1.8V HSTL Class I 8mA, 10mA & 12mA I/O
- 1.8V HSTL Class II 16mA I/O
- 1.8V HSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 1.8V HSTL Class II 25-Ohms Series OCT Without Calibration I/O
- 1.8V HSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.8V HSTL Class II 25-Ohms Series OCT With Calibration I/O
- 1.8V SSTL Input
- 1.8V SSTL Class I 8mA, 10mA & 12mA I/O
- 1.8V SSTL Class II 12mA & 16mA I/O
- 1.8V SSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 1.8V SSTL Class II 25-Ohms Series OCT Without Calibration I/O
- 1.8V SSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.8V SSTL Class II 25-Ohms Series OCT With Calibration I/O
- 2.5V SSTL Input
- 2.5V SSTL Class I 8mA & 12mA I/O
- 2.5V SSTL Class II 16mA I/O
- 2.5V SSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 2.5V SSTL Class II 25-Ohms Series OCT Without Calibration I/O
- 2.5V SSTL Class I 50-Ohms Series OCT With Calibration I/O
- 2.5V SSTL Class II 25-Ohms Series OCT With Calibration I/O
- 2.5V LVDS Input
- 2.5V LVDS Output
- 2.5V mini-LVDS Output
- 2.5V PPDS Output
- 2.5V RSDS Output

Left & Right I/O Bank with DIFFIO pin as optional pin function

- 1.2V LVCMOS Input
- 1.2V LVCMOS 2mA, 4mA, 6mA, 8mA & 10mA I/O
- 1.2V LVCMOS 50 Ohm Series OCT without Calibration I/O
- 1.2V LVCMOS 50 Ohm Series OCT with Calibration I/O
- 1.5V LVCMOS Input
- 1.5V LVCMOS 2mA, 4mA, 6mA, 8mA, 10mA, 12mA & 16mA I/O
- 1.5V LVCMOS 25 Ohm & 50 Ohm Series OCT without Calibration I/O
- 1.5V LVCMOS 25 Ohm & 50 Ohm Series OCT with Calibration I/O
- 1.8V LVTTL Input
- 1.8V LVTTL 2mA, 4mA, 6mA, 8mA, 10mA ,12mA & 16mA I/O
- 1.8V LVTTL 25 Ohm & 50 Ohm Series OCT without Calibration I/O
- 1.8V LVTTL 25 Ohm & 50 Ohm Series OCT with Calibration I/O
- 2.5V LVTTL Input
- 2.5V LVTTL 4mA, 8mA, 12mA & 16mA I/O
- 2.5V LVTTL 25 Ohm & 50 Ohm Series OCT without Calibration I/O
- 2.5V LVTTL 25 Ohm & 50 Ohm Series OCT with Calibration I/O
- 2.5V LVTTL PCI diode enabled Input
- 2.5V LVTTL 4mA, 8mA, 12mA & 16mA with PCI diode enabled I/O
- 3.0V LVTTL Input
- 3.0V LVTTL 4mA, 8mA, 12mA & 16mA I/O
- 3.0V LVTTL 25 Ohm & 50 Ohm Series OCT without Calibration I/O
- 3.0V LVTTL 25 Ohm & 50 Ohm Series OCT with Calibration I/O
- 3.0V LVTTL with PCI diode enabled Input
- 3.0V LVTTL 4mA, 8mA, 12mA & 16mA with PCI diode enabled I/O
- 3.3V LVTTL Input

- 3.3V LVTTL 4mA & 8mA I/O
- 3.3V LVTTL with PCI diode enabled Input
- 3.3V LVTTL 4mA & 8mA with PCI diode enabled I/O
- 3.0V LVCMOS Input
- 3.0V LVCMOS 4mA, 8mA, 12mA & 16mA I/O
- 3.0V LVCMOS 25 Ohm & 50 Ohm Series OCT without Calibration I/O
- 3.0V LVCMOS 25 Ohm & 50 Ohm Series OCT with Calibration I/O
- 3.0V LVCMOS with PCI diode enabled Input
- 3.0V LVCMOS 4mA, 8mA, 12mA & 16mA with PCI diode enabled I/O
- 3.3V LVCMOS Input
- 3.3V LVCMOS 2mA I/O
- 3.3V LVCMOS with PCI diode enabled Input
- 3.3V LVCMOS 2mA with PCI diode enabled I/O
- 3.0V PCI Input
- 3.0V PCI I/O
- 3.0V PCI-X Input
- 3.0V PCI-X I/O
- 1.2V HSTL Input
- 1.2V HSTL Class I 8mA & 10mA I/O
- 1.2V HSTL Class II 14mA I/O
- 1.2V HSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 1.2V HSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.5V HSTL Input
- 1.5V HSTL Class I 8mA, 10mA & 12mA I/O
- 1.5V HSTL Class II 16mA I/O
- 1.5V HSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 1.5V HSTL Class II 25-Ohms Series OCT Without Calibration I/O
- 1.5V HSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.5V HSTL Class II 25-Ohms Series OCT With Calibration I/O
- 1.8V HSTL Input
- 1.8V HSTL Class I 8mA, 10mA & 12mA I/O
- 1.8V HSTL Class II 16mA I/O
- 1.8V HSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 1.8V HSTL Class II 25-Ohms Series OCT Without Calibration I/O
- 1.8V HSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.8V HSTL Class II 25-Ohms Series OCT With Calibration I/O
- 1.8V SSTL Input
- 1.8V SSTL Class I 8mA, 10mA & 12mA I/O
- 1.8V SSTL Class II 12mA & 16mA I/O
- 1.8V SSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 1.8V SSTL Class II 25-Ohms Series OCT Without Calibration I/O
- 1.8V SSTL Class I 50-Ohms Series OCT With Calibration I/O
- 1.8V SSTL Class II 25-Ohms Series OCT With Calibration I/O
- 2.5V SSTL Input
- 2.5V SSTL Class I 8mA & 12mA I/O
- 2.5V SSTL Class II 16mA I/O
- 2.5V SSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 2.5V SSTL Class II 25-Ohms Series OCT Without Calibration I/O
- 2.5V SSTL Class I 50-Ohms Series OCT With Calibration I/O
- 2.5V SSTL Class II 25-Ohms Series OCT With Calibration I/O
- 1.2V Differential HSTL Input
- 1.5V Differential HSTL Input
- 1.8V Differential HSTL Input
- 1.8V Differential SSTL Input
- 2.5V Differential SSTL Input
- 2.5V Differential SSTL Class I 8mA & 12mA I/O
- 2.5V Differential SSTL Class II 16mA I/O
- 2.5V Differential SSTL Class I 50-Ohms Series OCT Without Calibration I/O
- 2.5V Differential SSTL Class II 25-Ohms Series OCT Without Calibration I/O
- 2.5V Differential SSTL Class I 50-Ohms Series OCT With Calibration I/O
- 2.5V Differential SSTL Class II 25-Ohms Series OCT With Calibration I/O
- 2.5V LVPECL Input
- 2.5V LVDS Input
- 2.5V LVDS Output
- 2.5V mini-LVDS Output
- 2.5V PPDS Output
- 2.5V RSDS Output

- For more information on the updated IBIS models, please refer to the IBIS file under 'Revision History' section

6.0 Cyclone IV IBIS Model User Guide Revision History

File rev 1.0

Date release: July 2010

- Initial release of Cyclone IV IBIS Models User Guide.