

iMX6 Rex Module

Variant: Variant name not interpreted

5. 9. 2013
V1I1

CHECKED

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DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

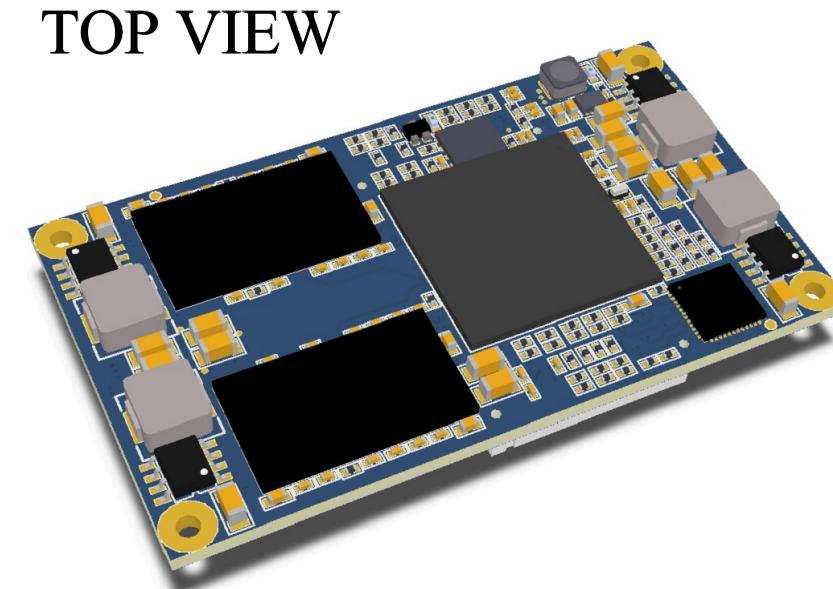
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for debug notes.

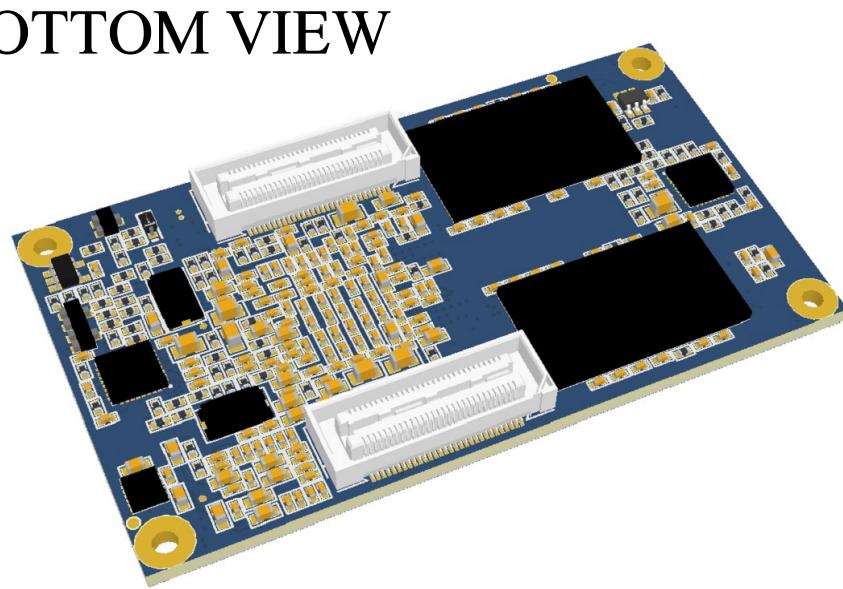
DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

TOP VIEW



BOTTOM VIEW

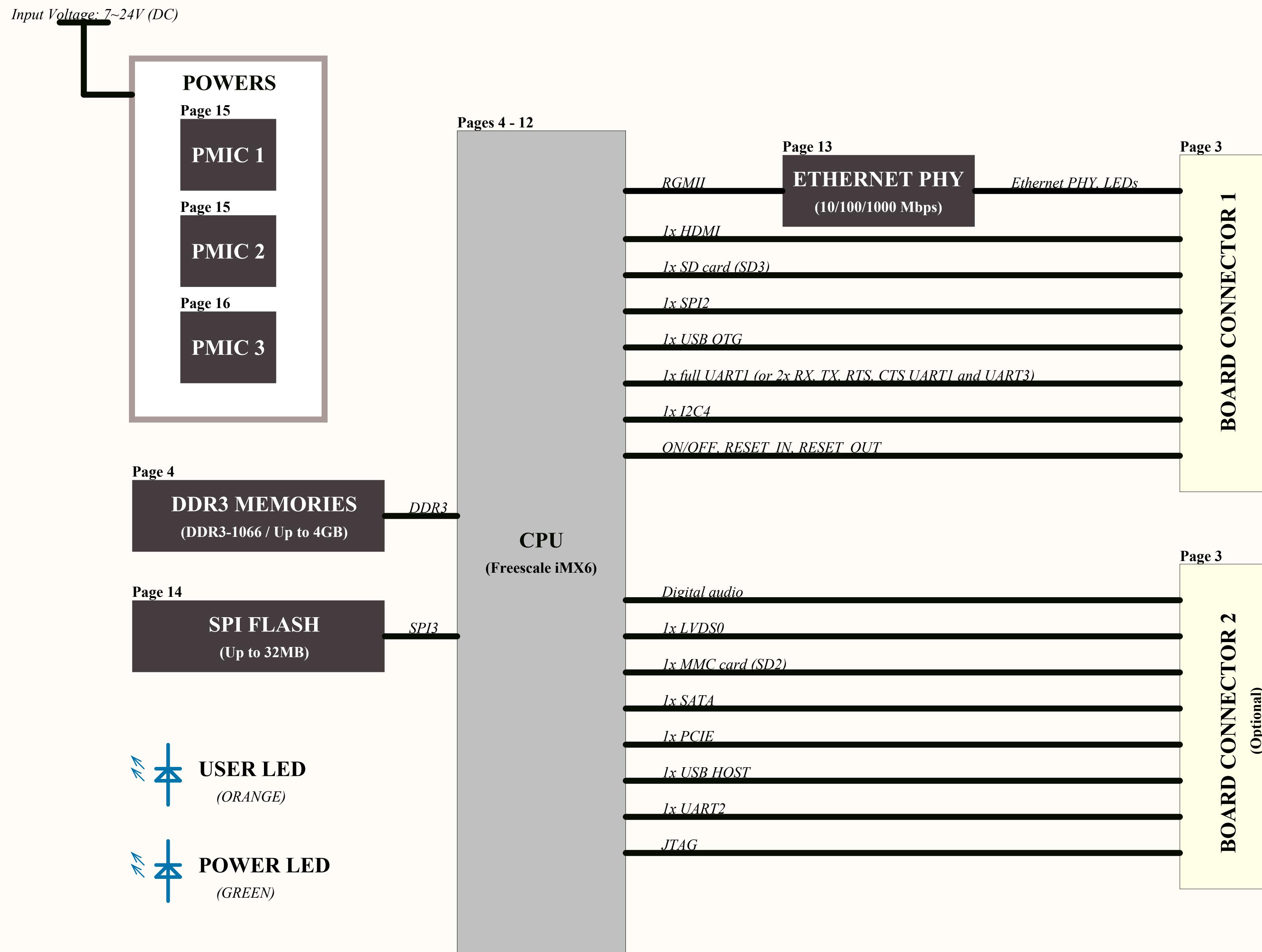


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Title:	iMX6 Rex Module
Variant:	Variant name not interpreted
Page Contents:	[01] - COVER PAGE.SchDoc
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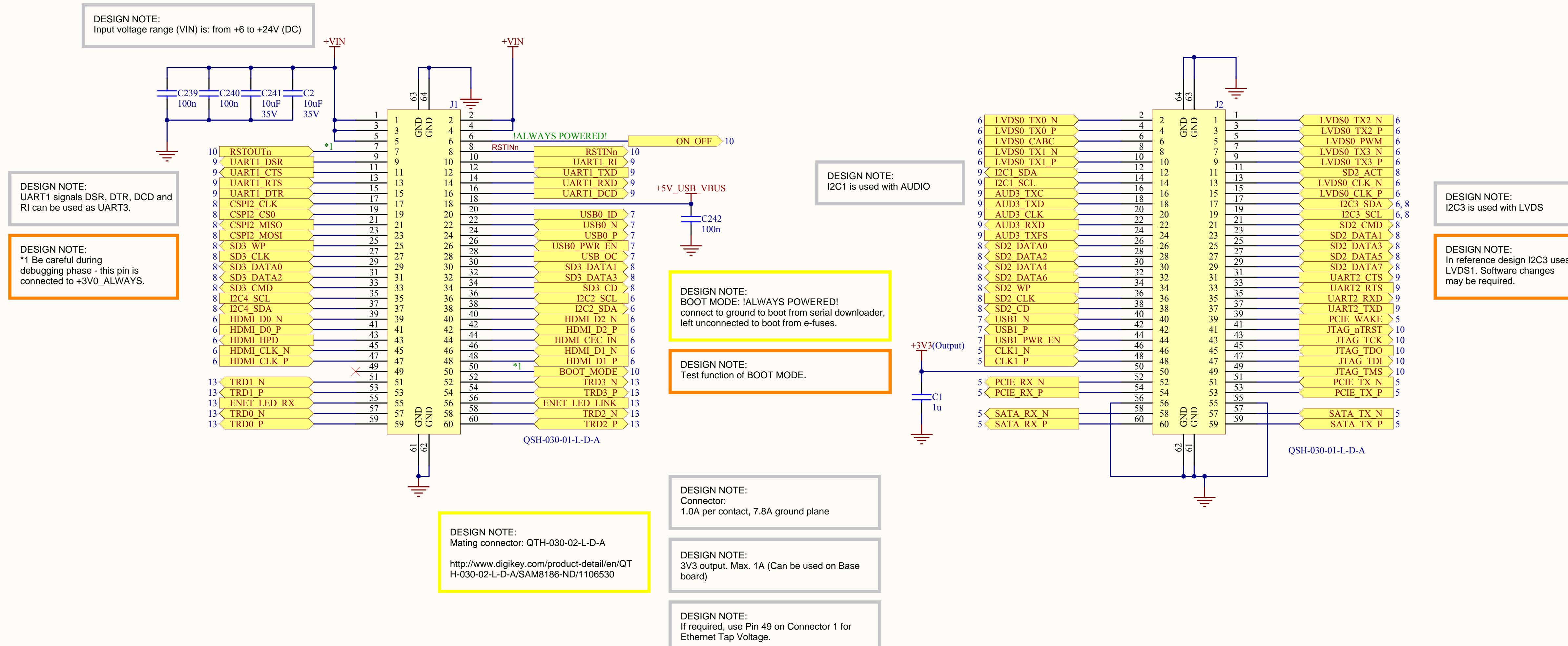
iMX6 Rex Module

(Block Diagram)

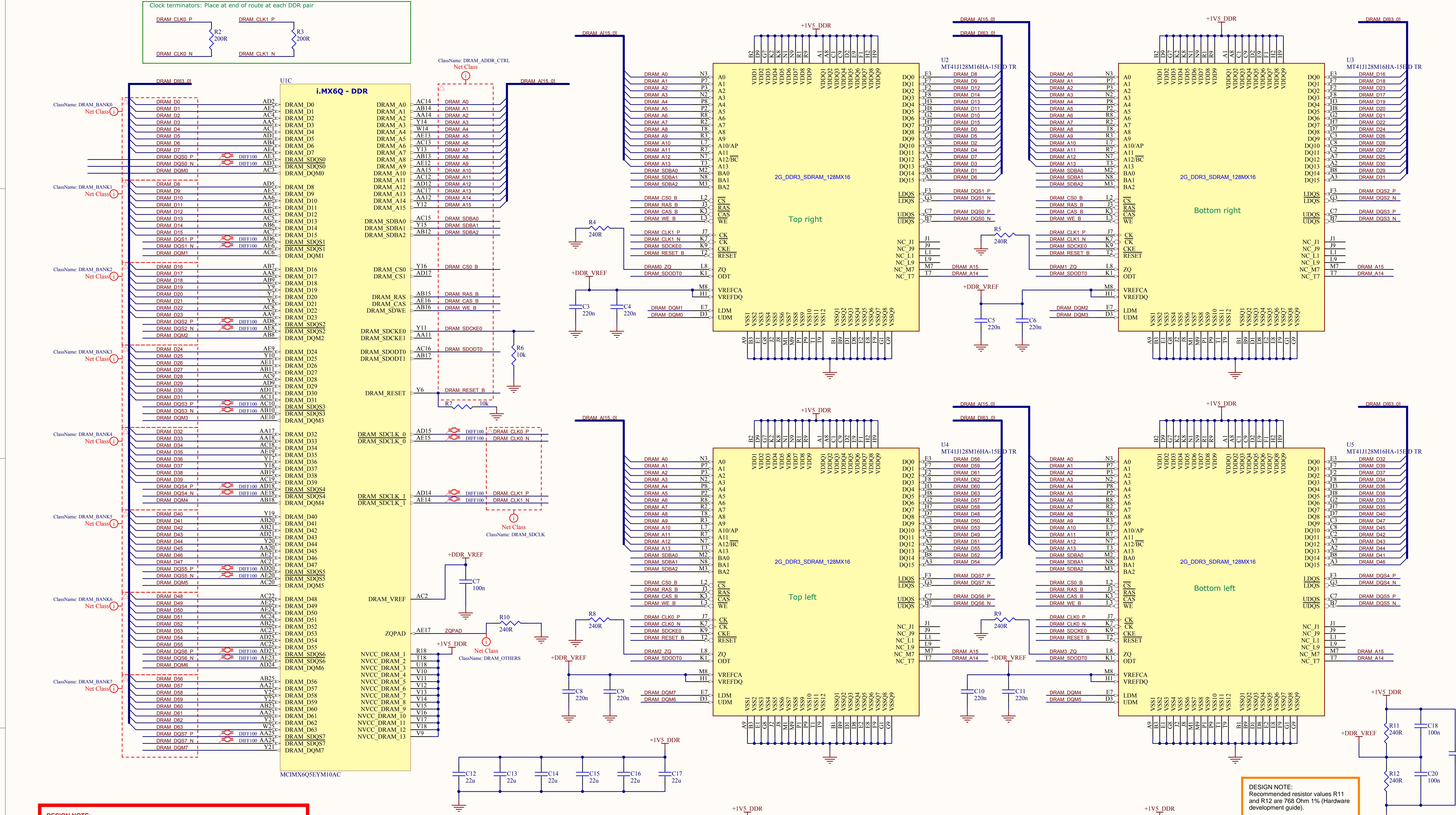


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CONNECTORS



CPU - DDR3, DDR3 MEM



DESIGN NOTE:
Pull down resistor RX3 is added to trace SDCKE0 in Rev B4 by soldering to an existing
via.

DESIGN NOTE:

DESIGN NOTE:
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration. Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

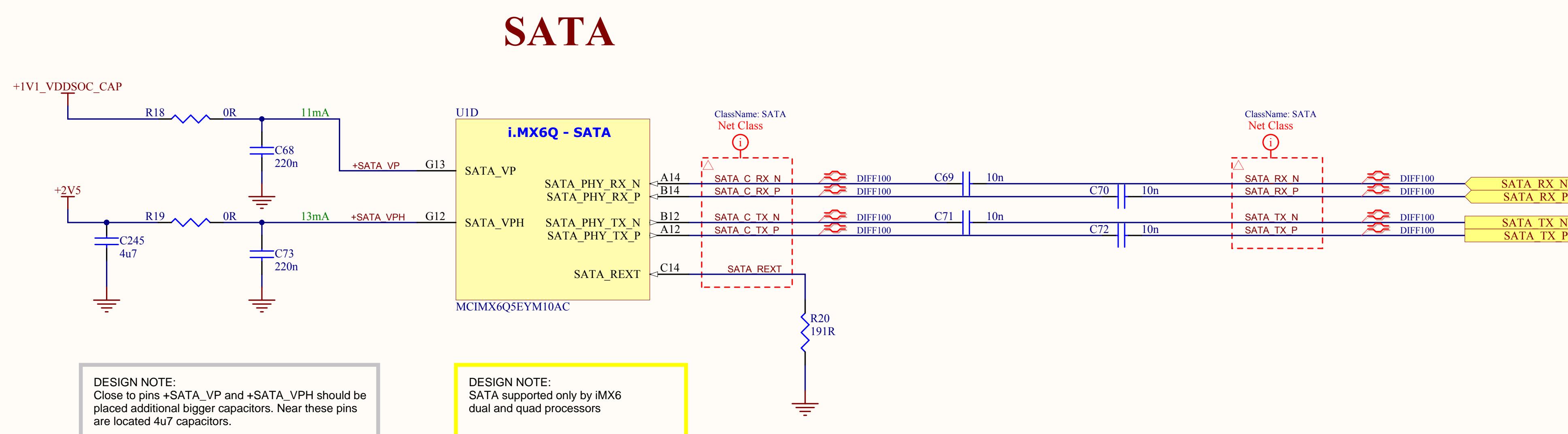
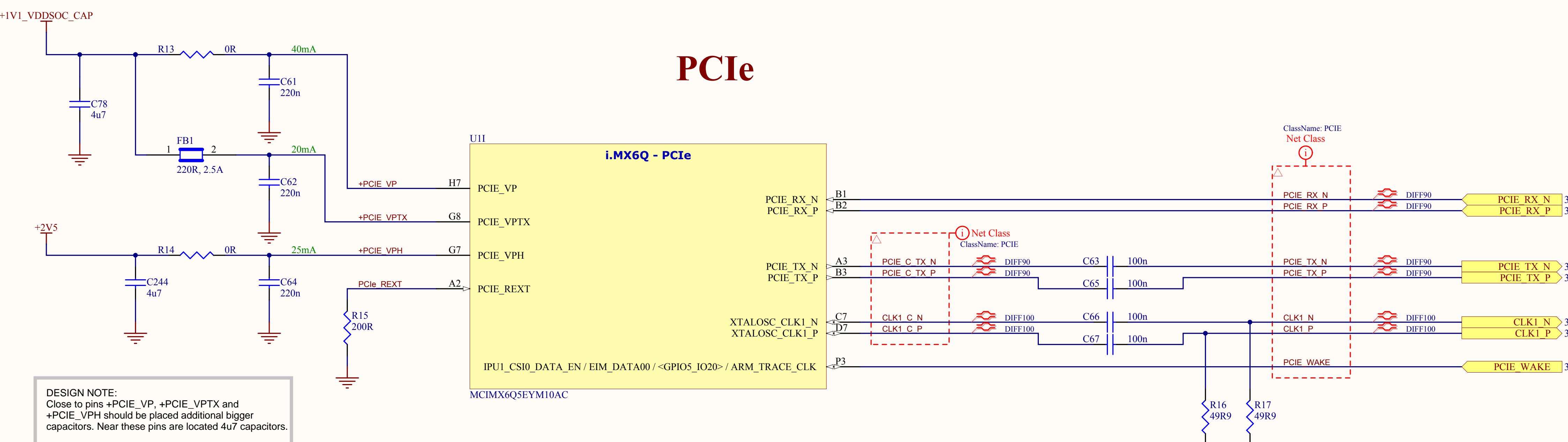
DESIGN NOTE:
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B pins to the new locations.

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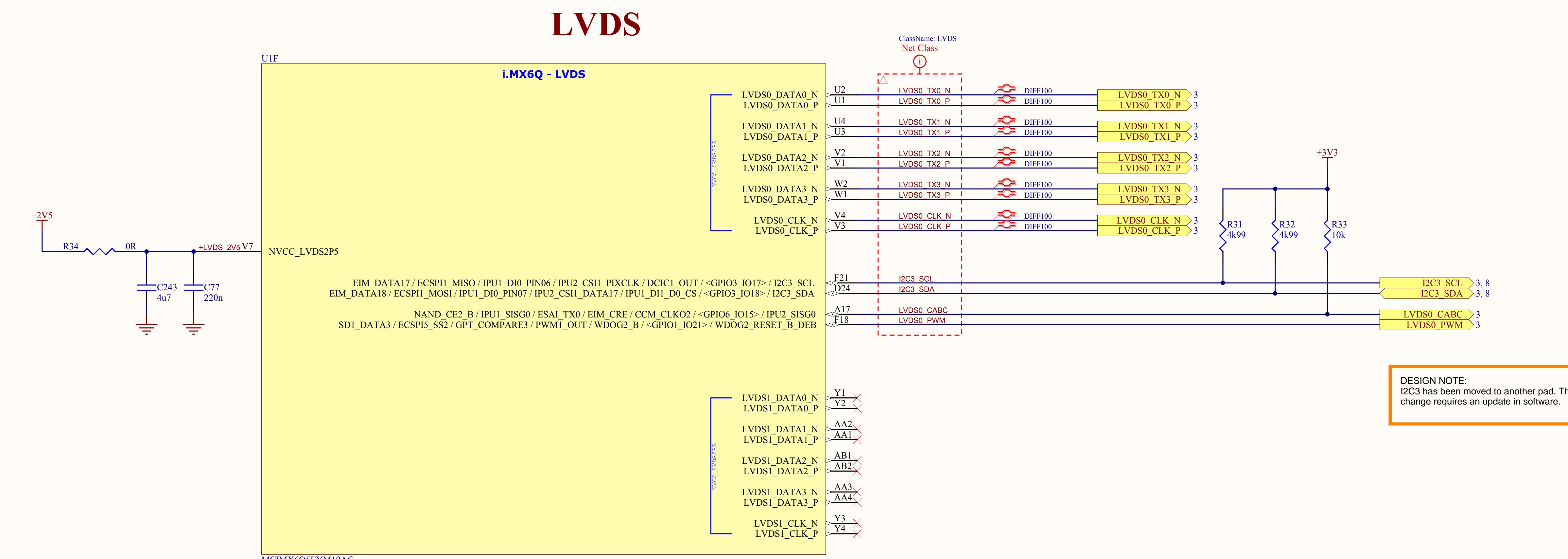
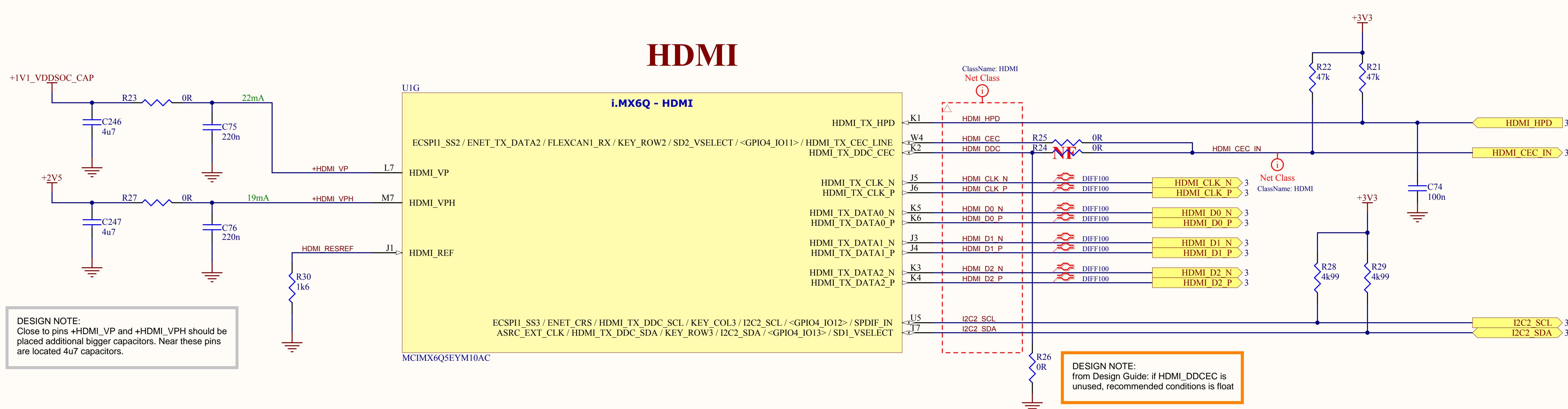
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Title:	Variant: iMX6 Rex Module Variant name not interpreted
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CPU - SATA, PCIe

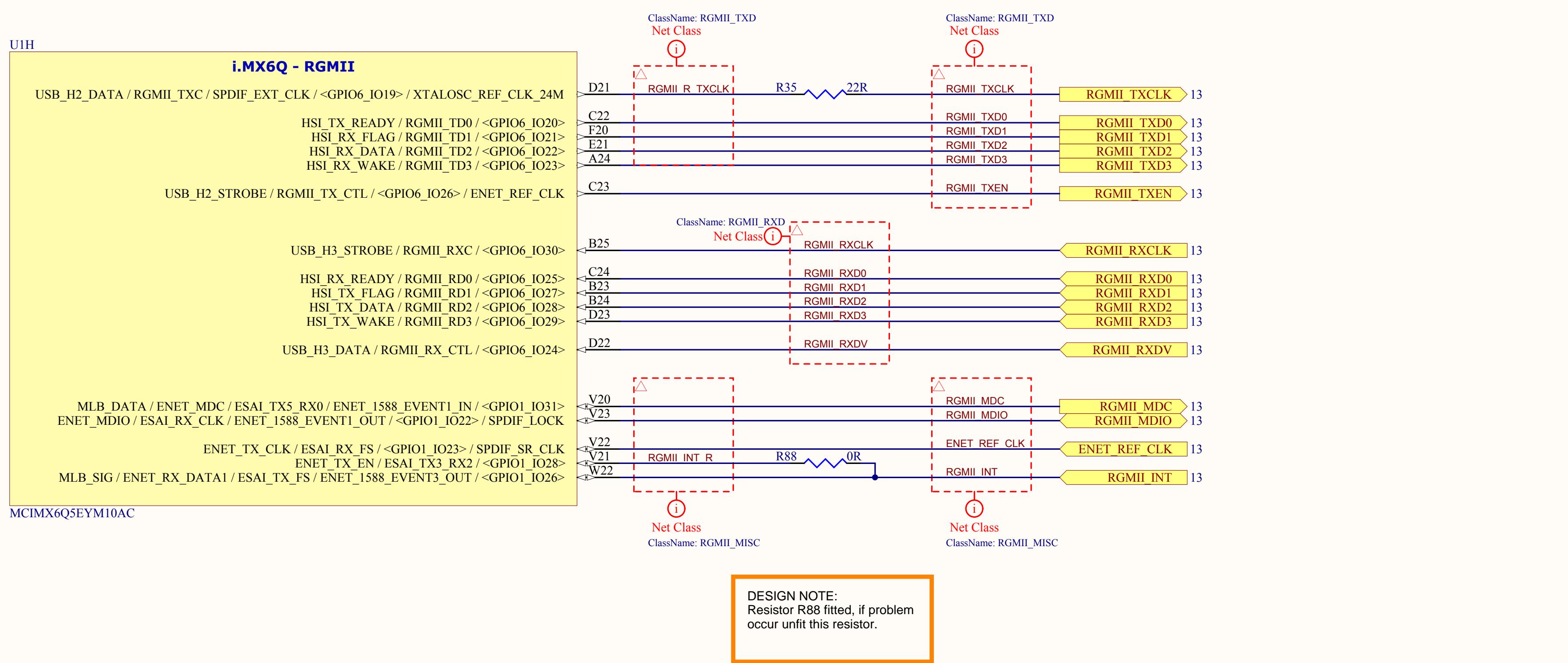


CPU - HDMI, LVDS

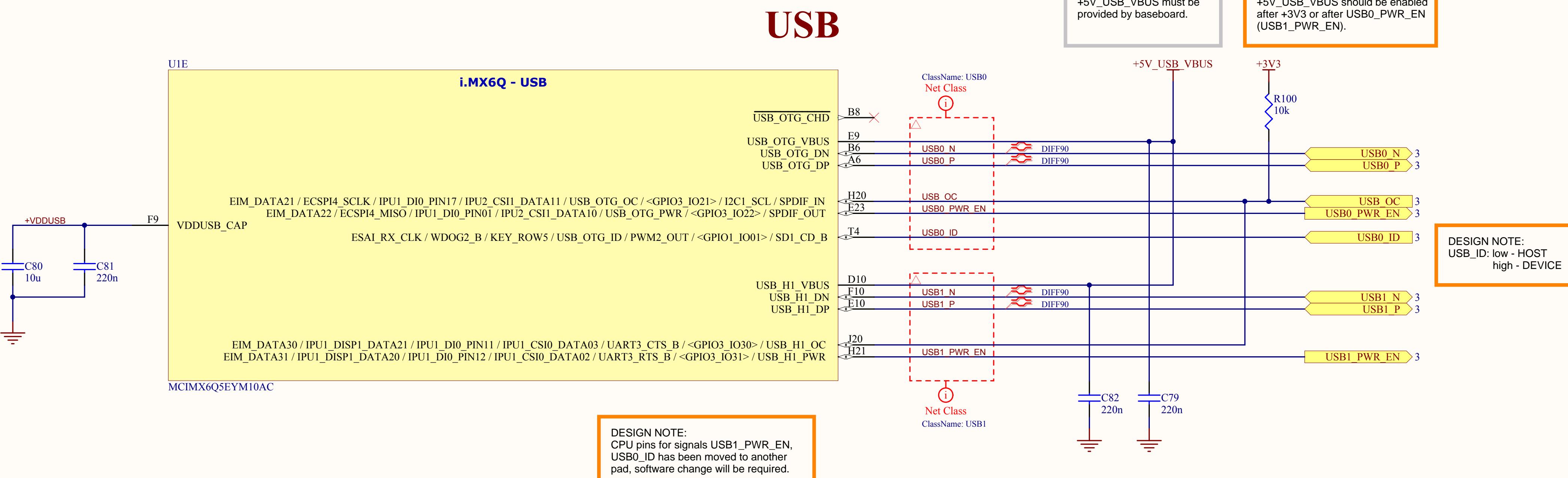


CPU - USB, ETHERNET

ETHERNET

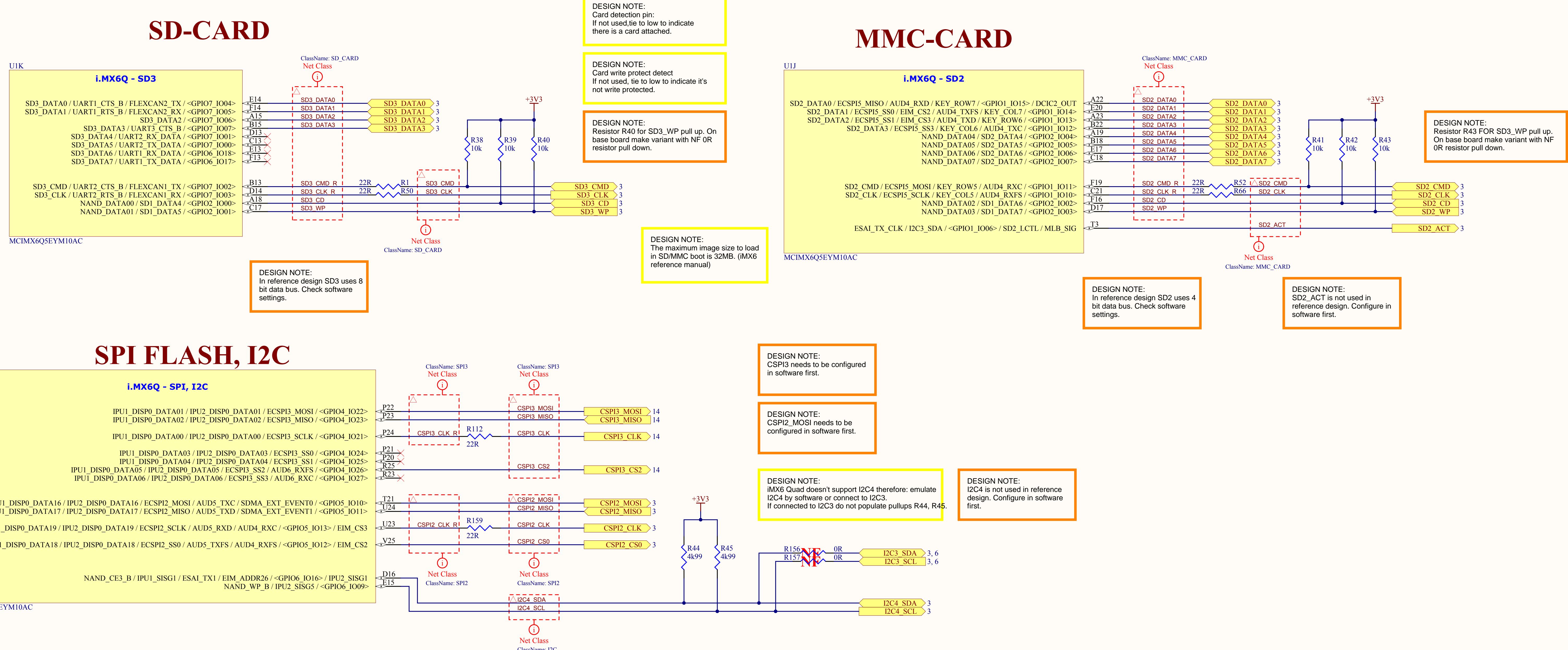


USB



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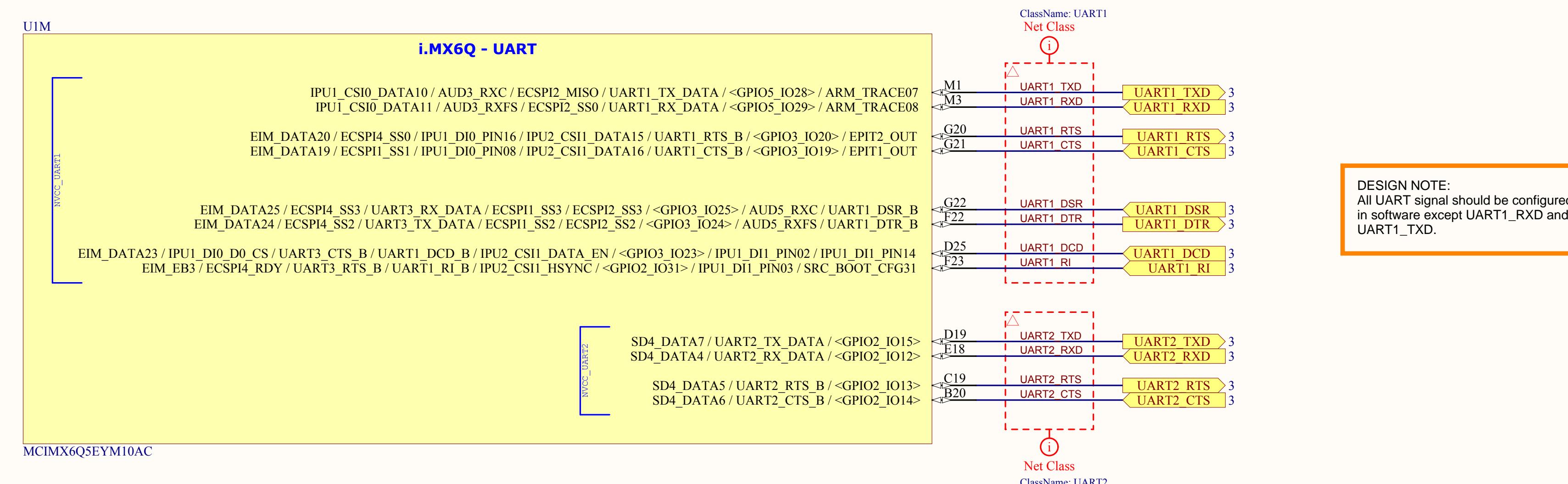
CPU - SPI, I2C, SD, MMC



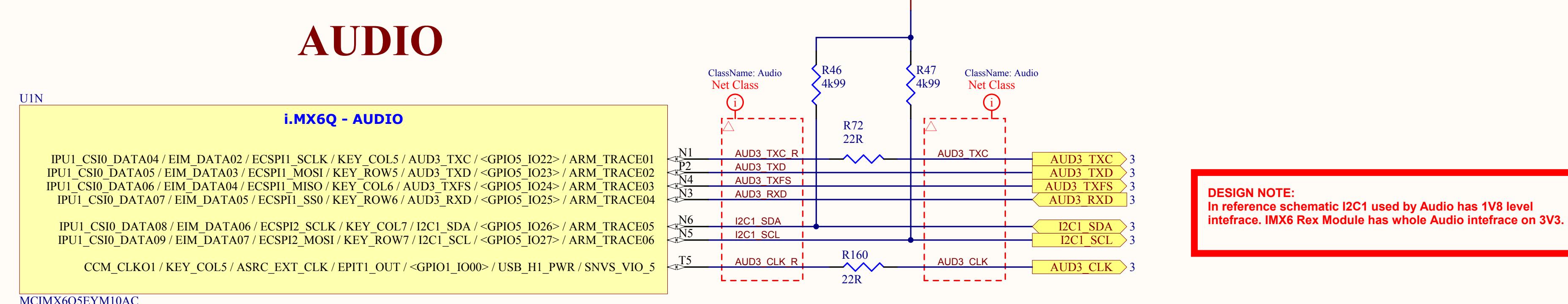
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Title:	iMX6 Rex Module
Variant:	Variant name not interpreted
Page Contents:	[08] - CPU - SPI, I2C, SD, MMC.SchDoc
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CPU - UART, AUDIO

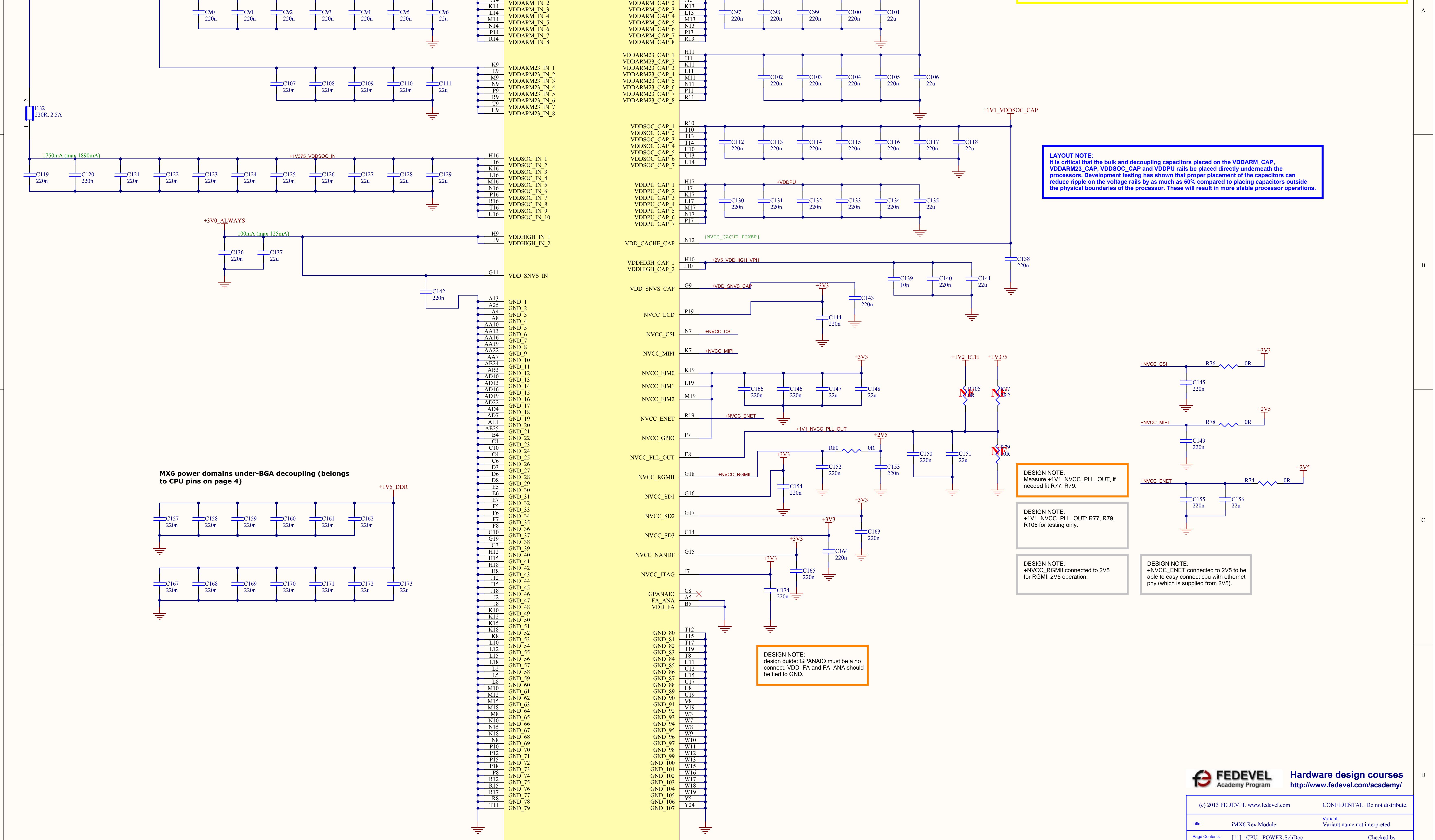
UART



AUDIO



CPU - POWER

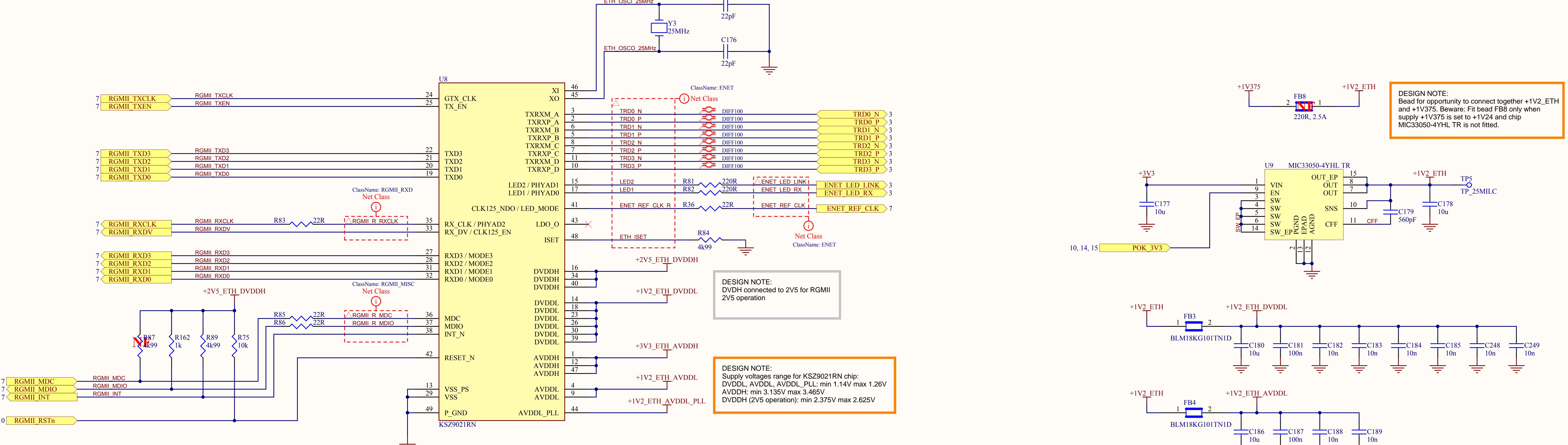


CPU - UNUSED PINS

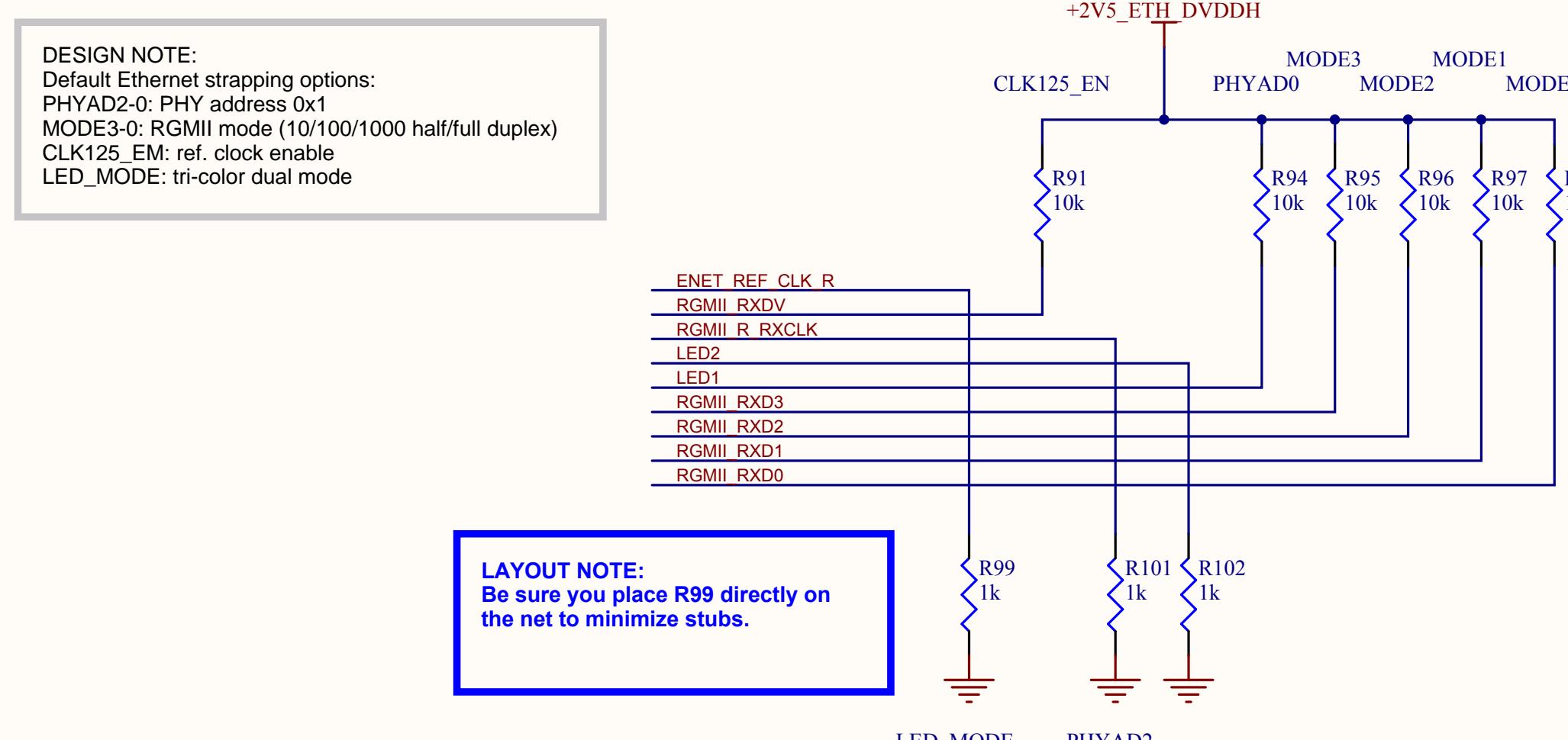


ETHERNET PHY

A



C

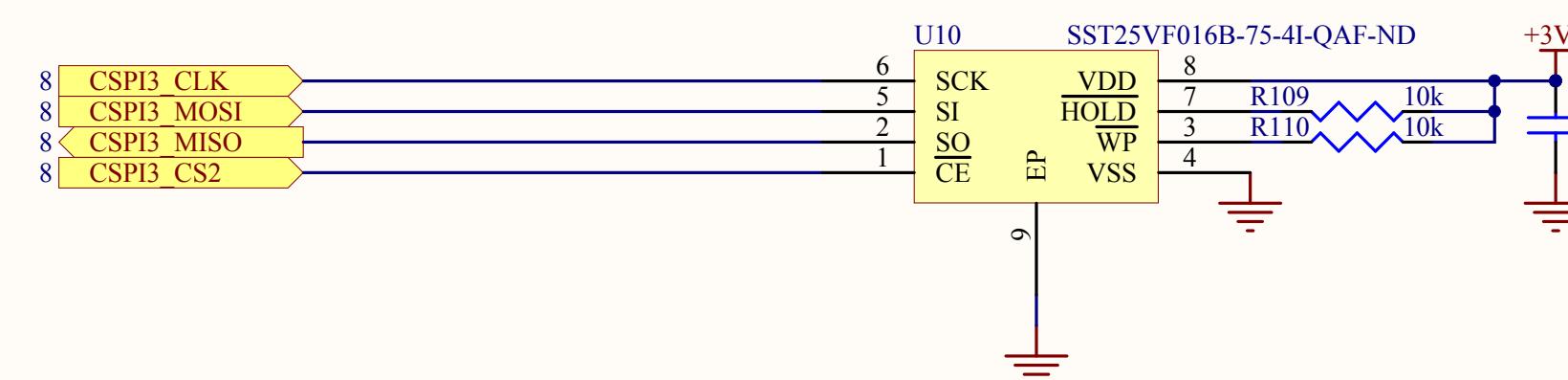


D

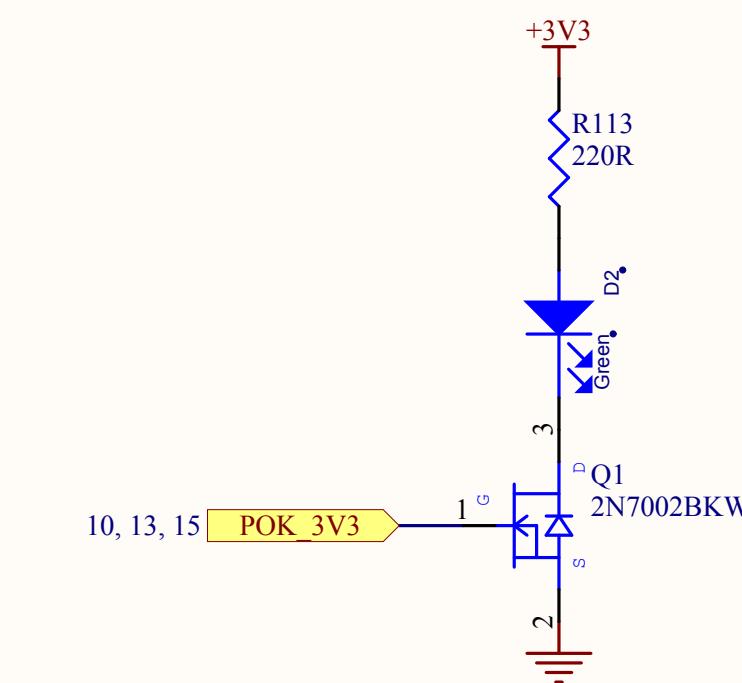
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SPI FLASH, LED

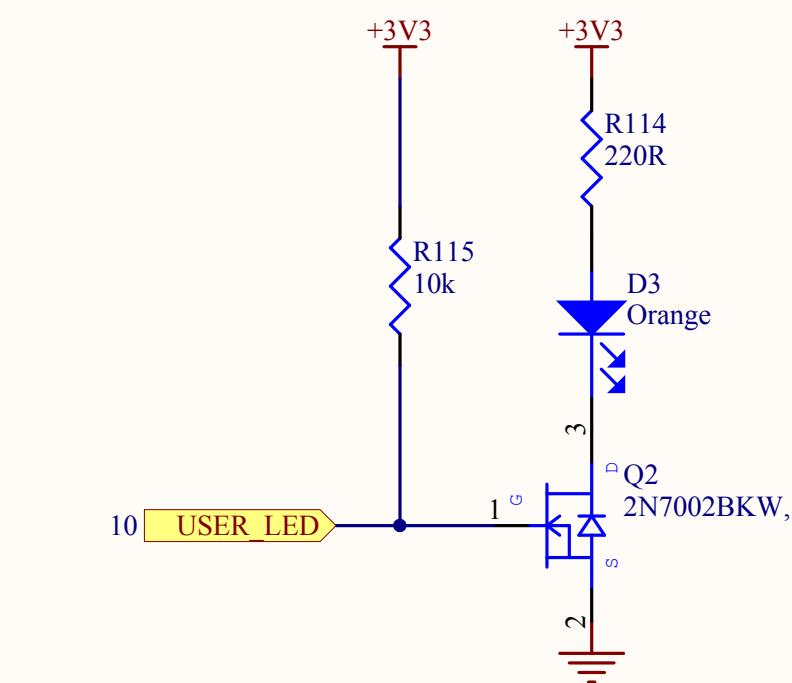
SPI NOR FLASH



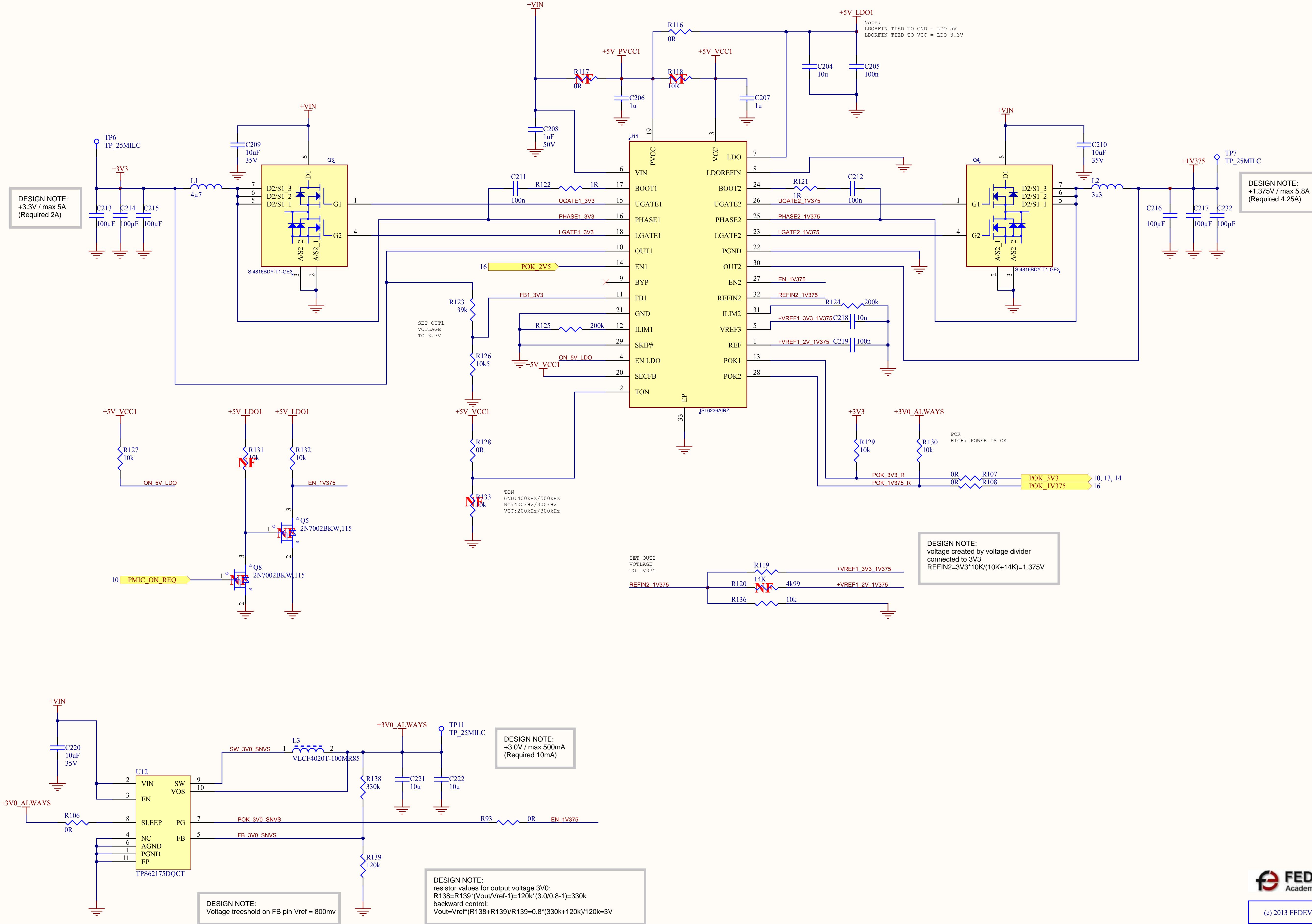
POWER LED



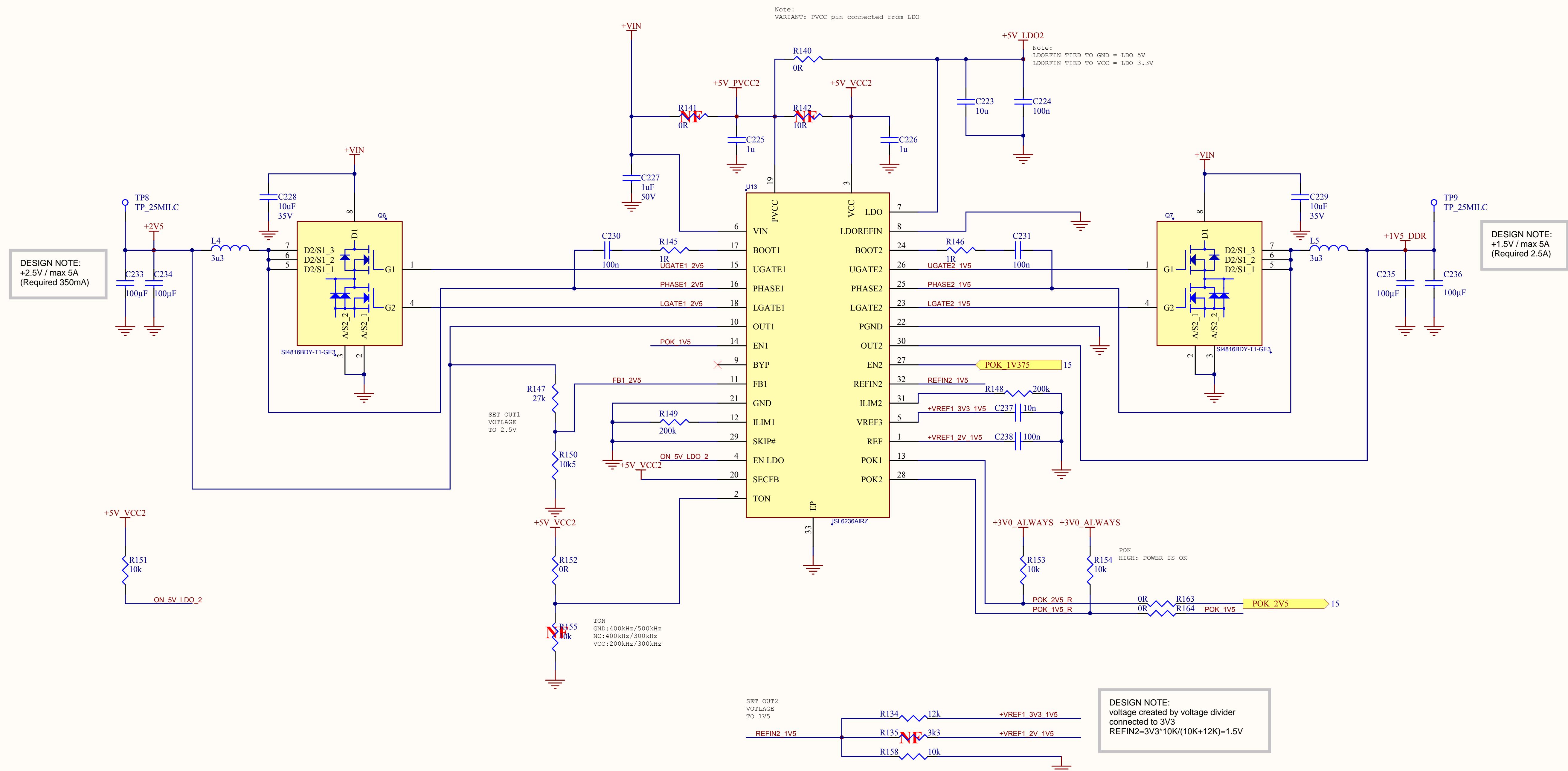
USER DEFINED LED



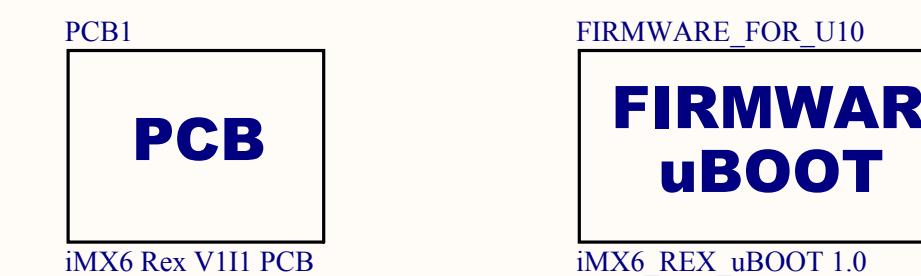
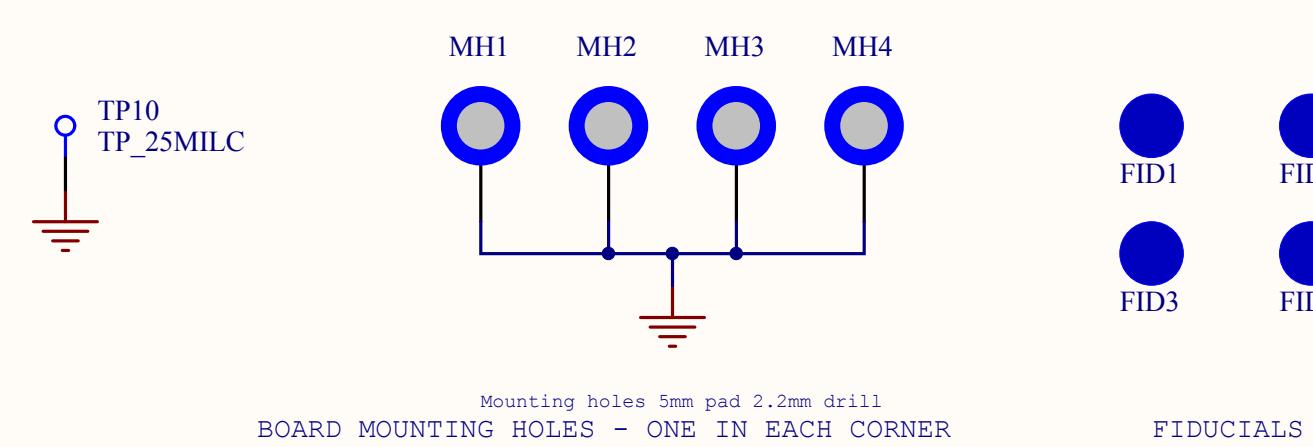
POWER +3.3V, +1.375V, +3.0_ALWAYS CON



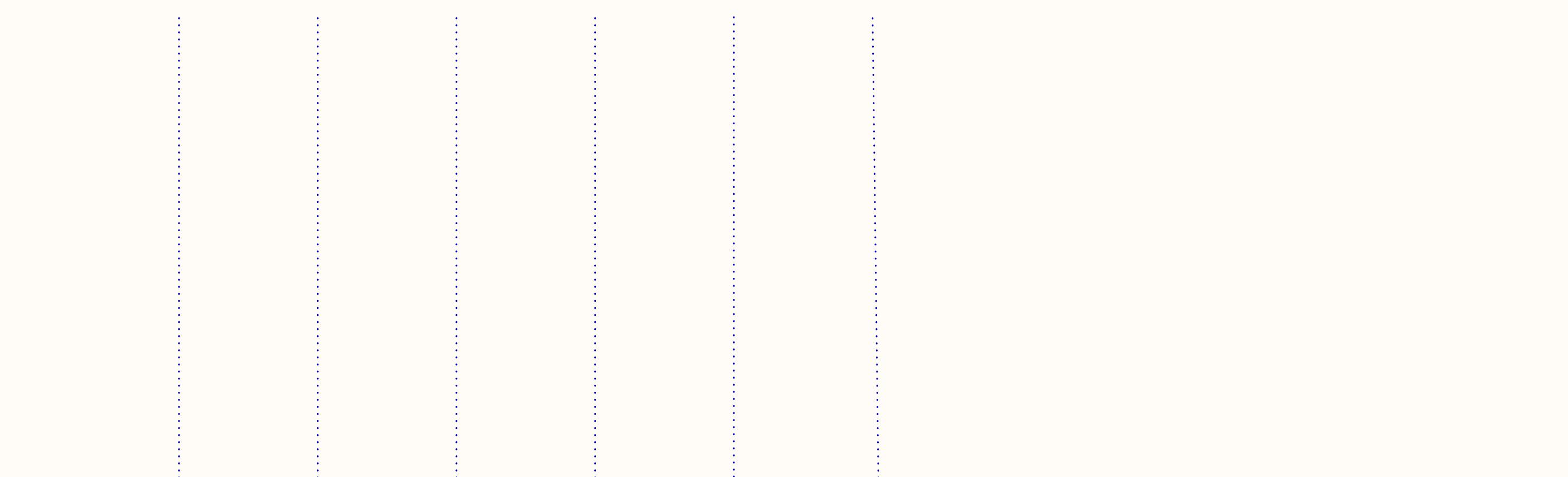
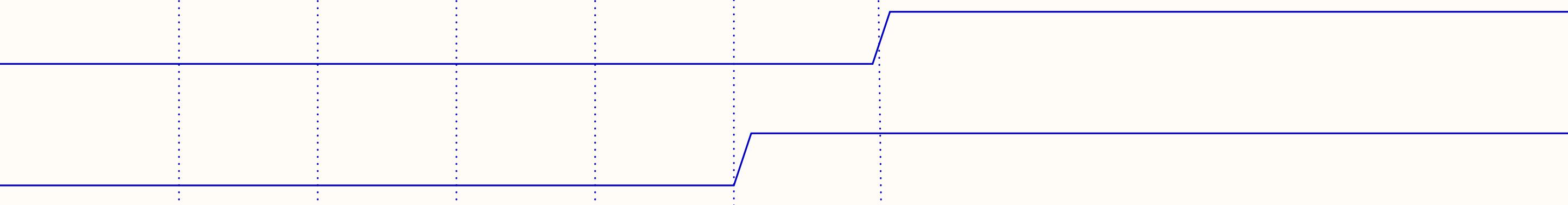
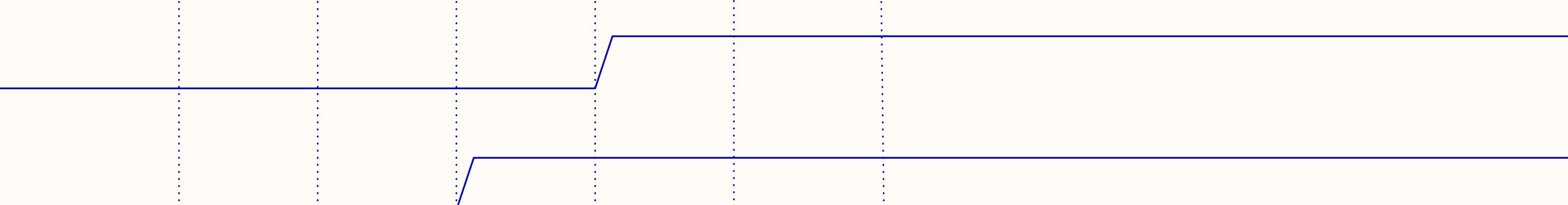
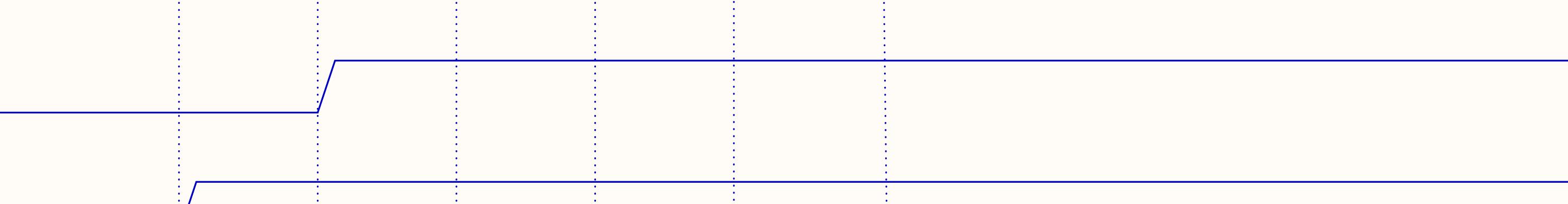
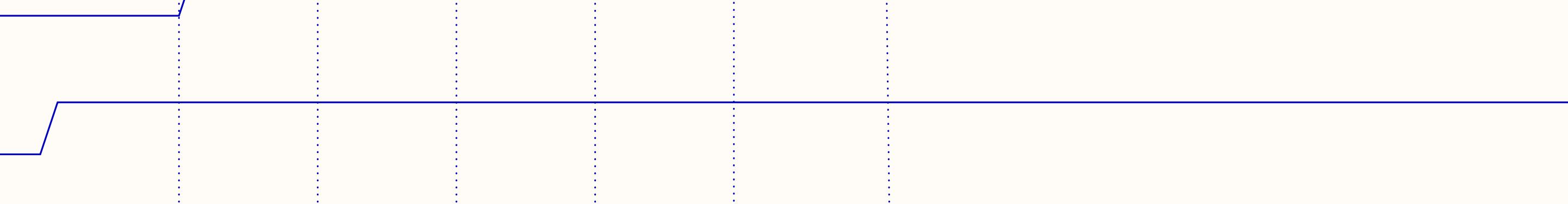
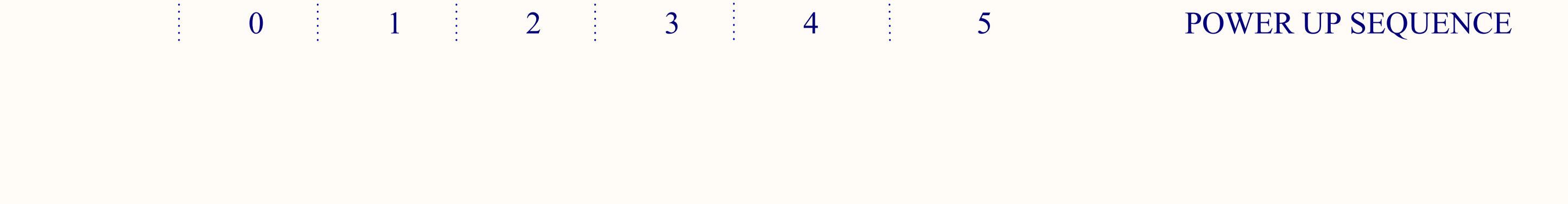
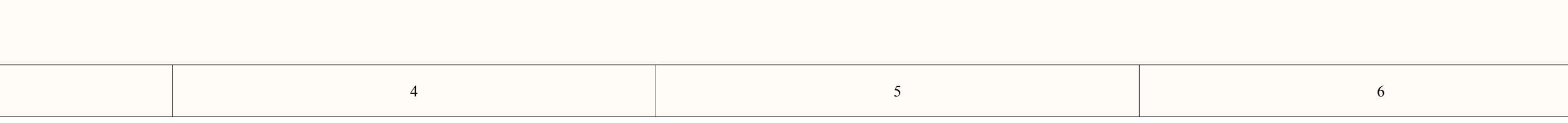
POWER +2.5V, +1.5V CON



MECHANICAL



CPU - POWER SEQUENCING

A	OTHER USED SIGNAL	LEVEL	GEN BY	SUPPLIED FROM SIGNAL	B	B
	+USB_VBUS	5V	connector	cpu		
	+DDR_VREF	0V75	+1V5_DDR	ref. for DDR memories, gen. with volt. divider		
	+1V2_VDD_ARM_CAP	1V2	iMX	cpu, core caps		
	+1V1_VDDSOC_CAP	1V1	iMX	core caps, cpu-sata, cpu-pcie, cpu-hdmi		
c	POK_3V3	+1V2_ETH	1V2	ethernet phy		c
	POK_2V5	+3V3	3V3	cpu, pull up		
	POK_1V5	+2V5	2V5	cpu, ethernet phy		
	POK_1V375	+1V5_DDR	1V5	cpu, memory		
	EN_1V375	+1V375	1V375	cpu, cpu core voltages		
	+VIN	+3V3_ALWAYS	3V3	cpu, supervisor, pull up		
d	+VIN	+VIN	4.75V-25V	switching power supplies		d
ENABLED BY	SIGNAL	LEVEL	SUPPLIED FROM SIGNAL	POWER UP SEQUENCE		

DOC: REVISION HISTORY

A 01-AUG-2013 Some HDMI and Ethernet signals swapped on J1

19-AUG-2013 Signals for SPI FLASH has been moved to CSPI3
Added additional capacitors to +2V5 and +1V1_VDDSOC_CAP

21-AUG-2013 Added resistor from CPU_XTALO to GND
I2C3_SDA and I2C3_SCL has been moved to another CPU pins

22-AUG-2013 Always powered voltage change level to 3V0 - supply voltage +3V0_ALWAYS
Added bead to connect together +1V2_ETH and +1V375 (Only for testing purpose).

23-AUG-2013 Added resistor to connect SLEEP pin of TPS62175DQCT to +3V0_ALWAYS.

27-AUG-2013 On connector J1 added BOOT_MODE signal to select boot source.



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D CLOCKS (CPU & PCI)

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[01] - COVER PAGE.SchDoc
[01] - COVER PAGE.SchDoc

[02] - BLOCK DIAGRAM.SchDoc
[02] - BLOCK DIAGRAM.SchDoc

[03] - CONNECTORS.SchDoc
[03] - CONNECTORS.SchDoc

[04] - CPU - DDR3, DDR3 MEM.SchDoc
[04] - CPU - DDR3, DDR3 MEM.SchDoc

[05] - CPU - PCIE, SATA.SchDoc
[05] - CPU - PCIE, SATA.SchDoc

[06] - CPU - HDMI, LVDS.SchDoc
[06] - CPU - HDMI, LVDS.SchDoc

[07] - CPU - USB, ETHERNET.SchDoc
[07] - CPU - USB, ETHERNET.SchDoc

[08] - CPU - SPI, I2C, SD, MMC.SchDoc
[08] - CPU - SPI, I2C, SD, MMC.SchDoc

A

A

TEMPLATE NOTES

Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Company, Project and Version Revision

Mark Not Fitted Components as
NF

Net Class Example



Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Title

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

[09] - CPU - UART, AUDIO.SchDoc
[09] - CPU - UART, AUDIO.SchDoc

[10] - CPU - JTAG, CONTROL.SchDoc
[10] - CPU - JTAG, CONTROL.SchDoc

[11] - CPU - POWER.SchDoc
[11] - CPU - POWER.SchDoc

[12] - CPU - UNUSED.SchDoc
[12] - CPU - UNUSED.SchDoc

[13] - ETHERNET PHY.SchDoc
[13] - ETHERNET PHY.SchDoc

[14] - SPI FLASH, LEDS.SchDoc
[14] - SPI FLASH, LEDS.SchDoc

[15] - PWR 3V3, 1V375.SchDoc
[15] - PWR 3V3, 1V375.SchDoc

[16] - PWR 2V5, 1V5.SchDoc
[16] - PWR 2V5, 1V5.SchDoc

[17] - MECH.SchDoc
[17] - MECH.SchDoc

[18] - POWER SEQUENCING.SchDoc
[18] - POWER SEQUENCING.SchDoc

[19] - DOC REVISION HISTORY.SchDoc
[19] - DOC REVISION HISTORY.SchDoc



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