iMX6 Rex Module

Variant: Variant name not interpreted

20. 5. 2013
V1I1

PRELIMINARY

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DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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iMX6 Rex Module

(Block Diagram)

Input Voltage: 5~24V (DC)

POWERS

Page 15

PMIC 1

Page 15

PMIC 2

Page 16

PMIC 3

Pages 4 - 12

CPU
(Freescale iMX6)

Page 13

ETHERNET PHY
(10/100/1000 Mbps)

RGMII

Ethernet PHY, LEDs

Page 3

BOARD CONNECTOR 1

1x HDMI

1x SD card (SD3)

1x SPI2

1x USB OTG

1x UART1

1x I2C4

ON/OFF, RESET_IN, RESET_OUT

Page 4

DDR3 MEMORIES
(DDR3-1066 / Up to 4GB)

DDR3

Page 14

SPI FLASH
(Up to 32MB)

SPI1

Digital audio

1x LVDS0

1x MMC card (SD2)

1x SATA

1x PCIE

1x USB HOST

1x UART2

JTAG

Page 3

BOARD CONNECTOR 2
(Optional)

USER LED
(ORANGE)

POWER LED
(GREEN)

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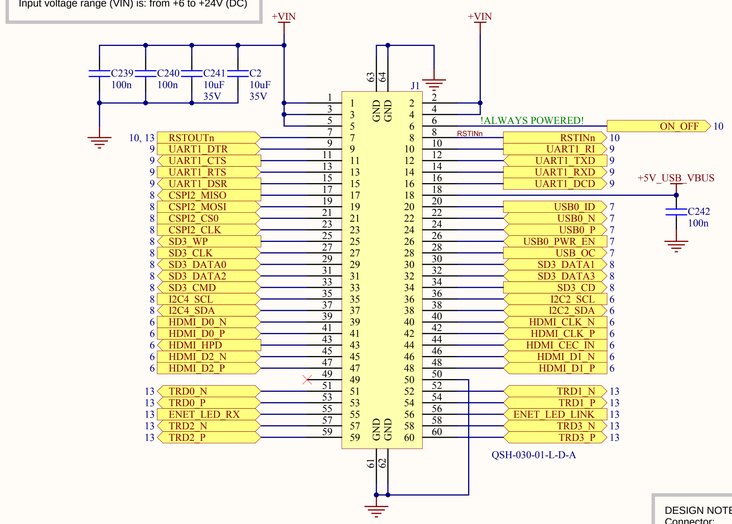
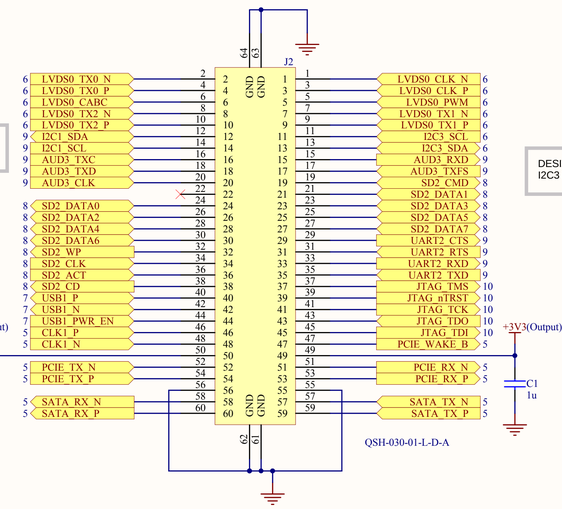
CONNECTORS

DESIGN NOTE:
Input voltage range (VIN) is: from +6 to +24V (DC)



DESIGN NOTE:
I2C1 is used with AUDIO



DESIGN NOTE:
I2C3 is used with LVDS

DESIGN NOTE:
Connector:
1.0A per contact, 7.8A per ground plane

DESIGN NOTE:
3V3 output. Max. 2A (Can be used on Base board)

DESIGN NOTE:
If required, use Pin 49 on Connector 1 for Ethernet Tap Voltage.

DESIGN NOTE:
J2 Pin 22 is free for future use

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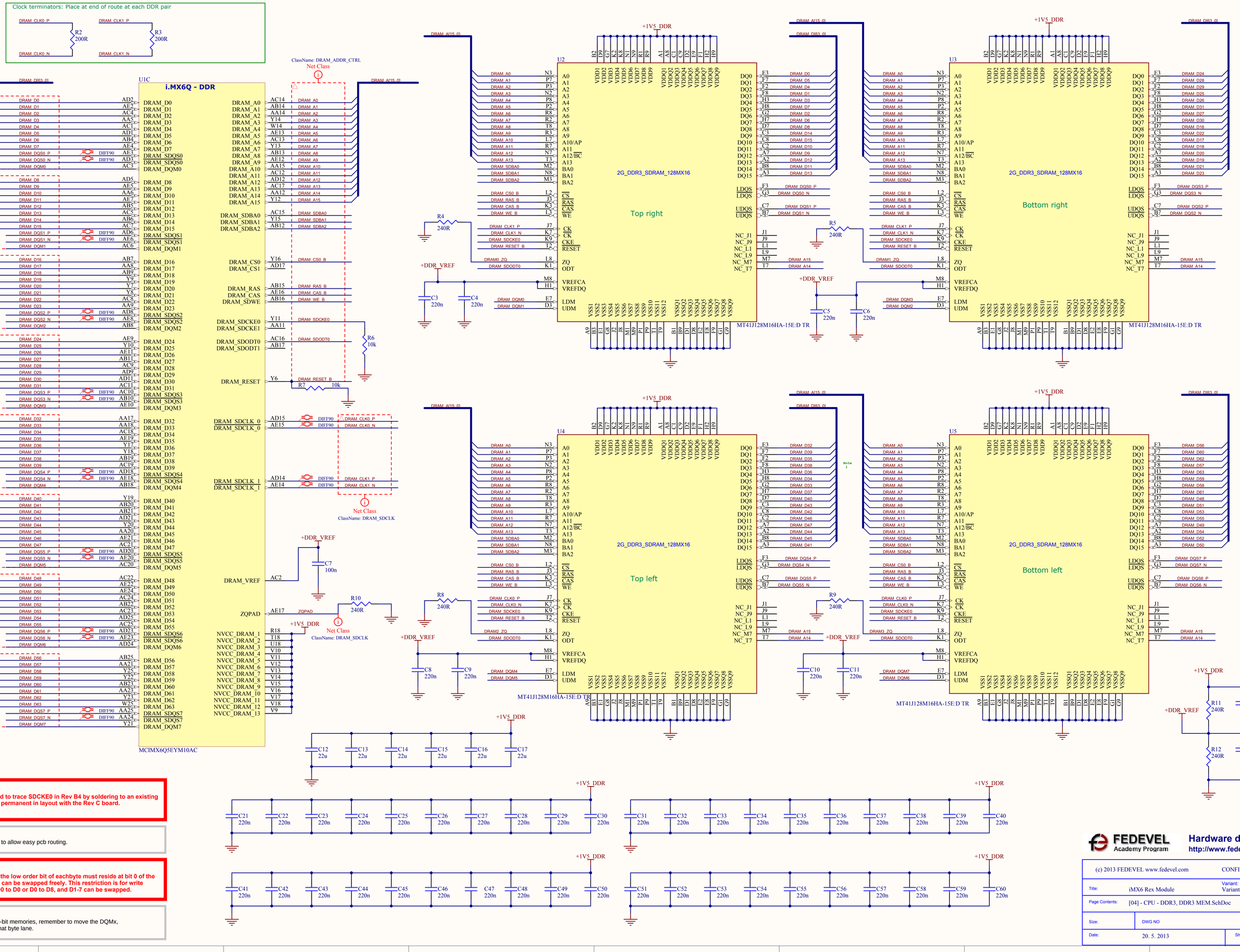
CPU - DDR3, DDR3 MEM



DESIGN NOTE:
Pull down resistor RX3 is added to trace SDCKE0 in Rev B4 by soldering to an existing open via. Change will be made permanent in layout with the Rev C board.

DESIGN NOTE:
Using bit swapping for DATA bus to allow easy pcb routing.

DESIGN NOTE:
When using data bit swapping the low order bit of eachbyte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration. Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

DESIGN NOTE:
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.

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Page Contents:	[04] - CPU - DDR3, DDR3 MEM.SchDoc		Checked by
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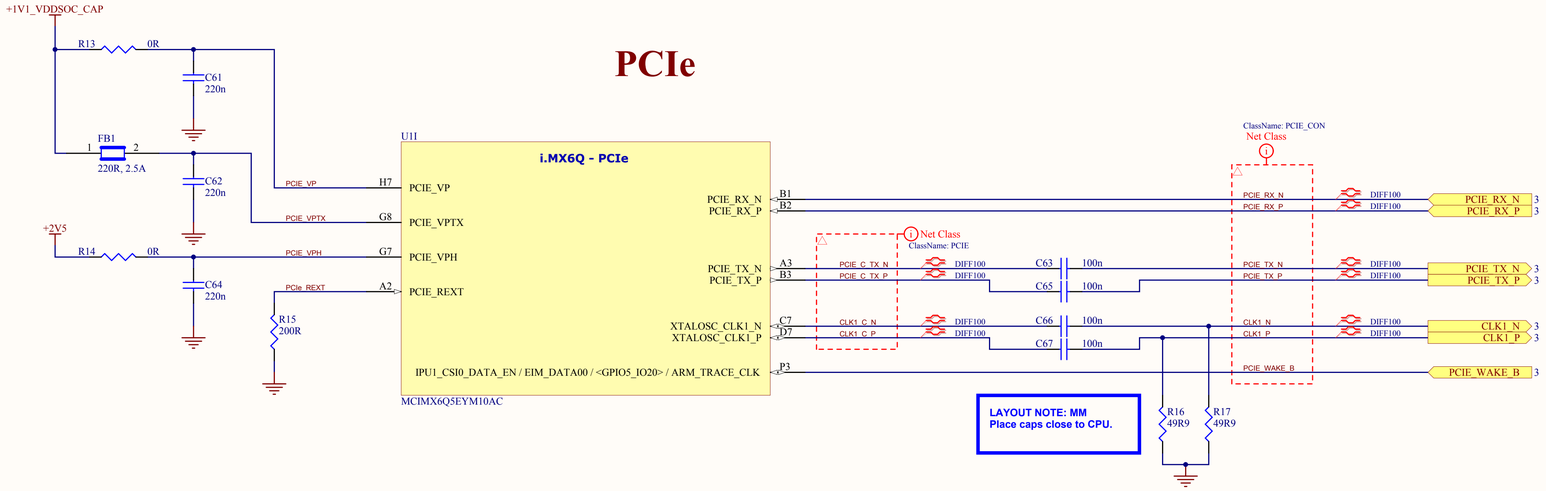
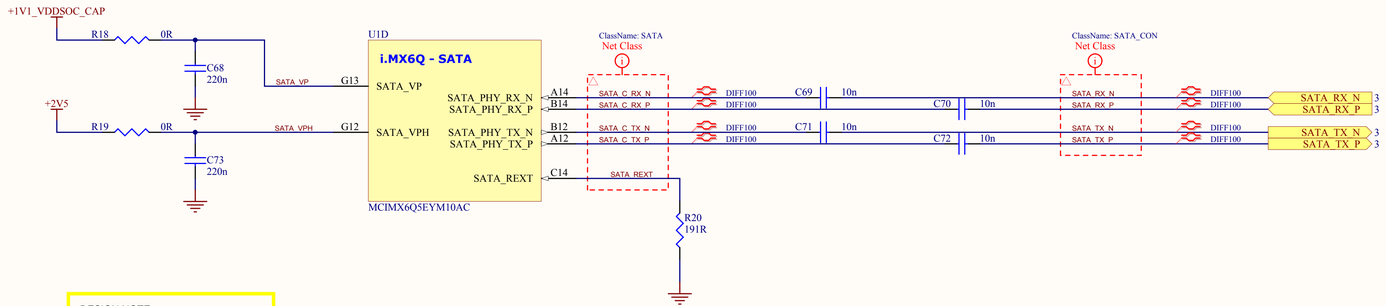
CPU - SATA, PCIe

PCIe



SATA



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Title:	iMX6 Rex Module	Variant:	Variant name not interpreted
Page Contents:	[05] - CPU - PCIE, SATA.SchDoc		Checked by
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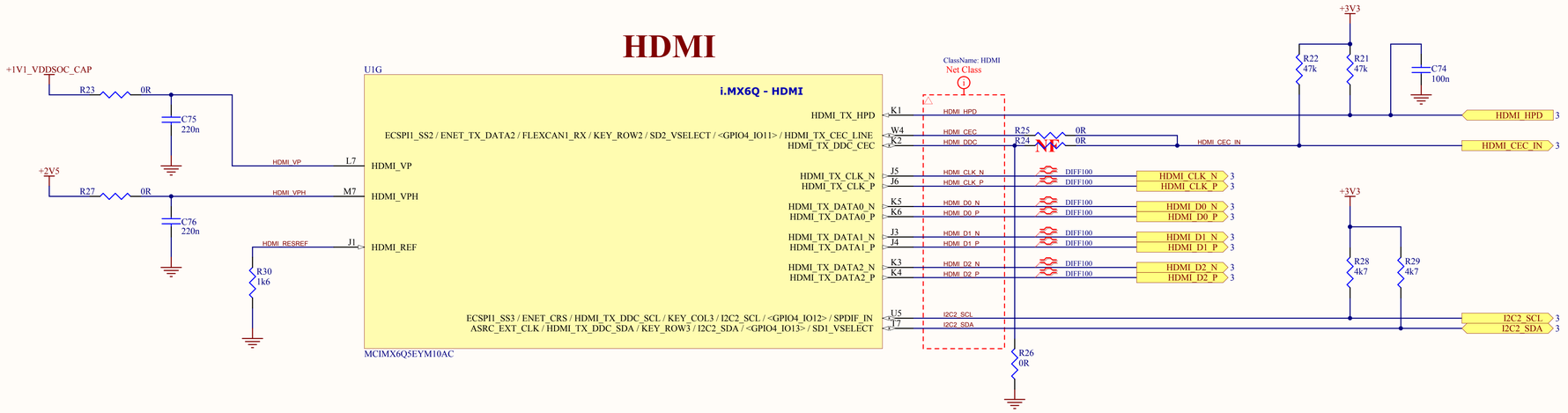
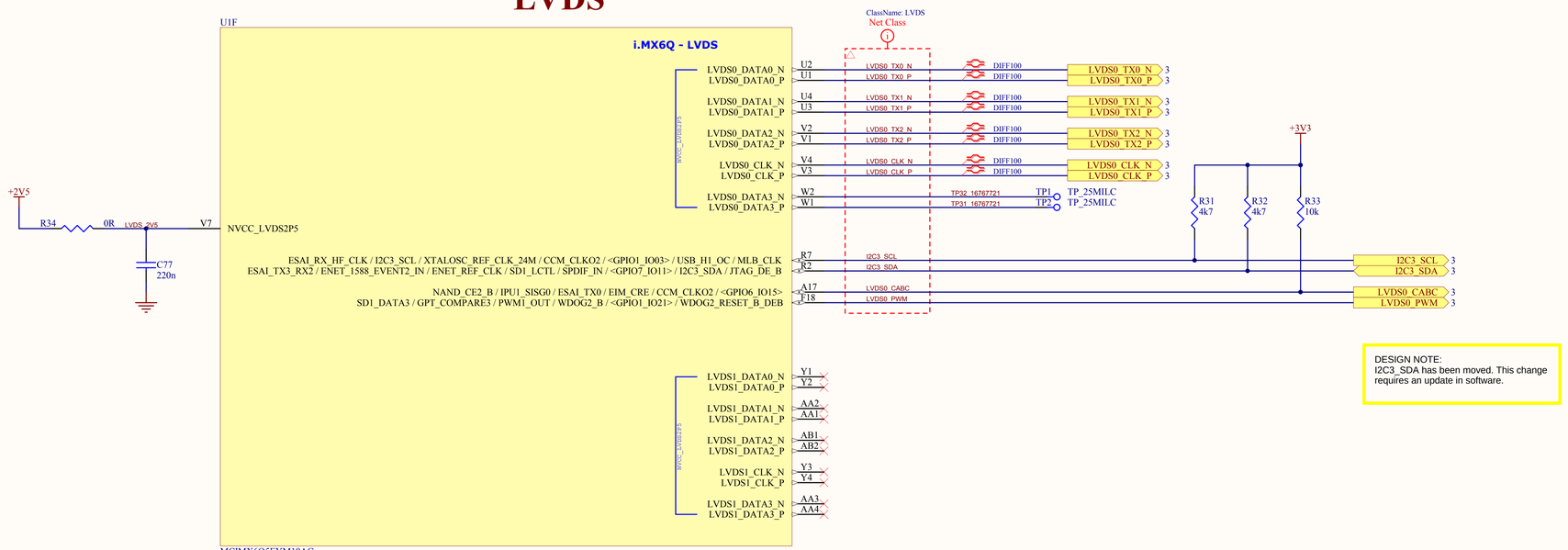
CPU - HDMI, LVDS

HDMI



LVDS



DESIGN NOTE:
I2C3_SDA has been moved. This change requires an update in software.

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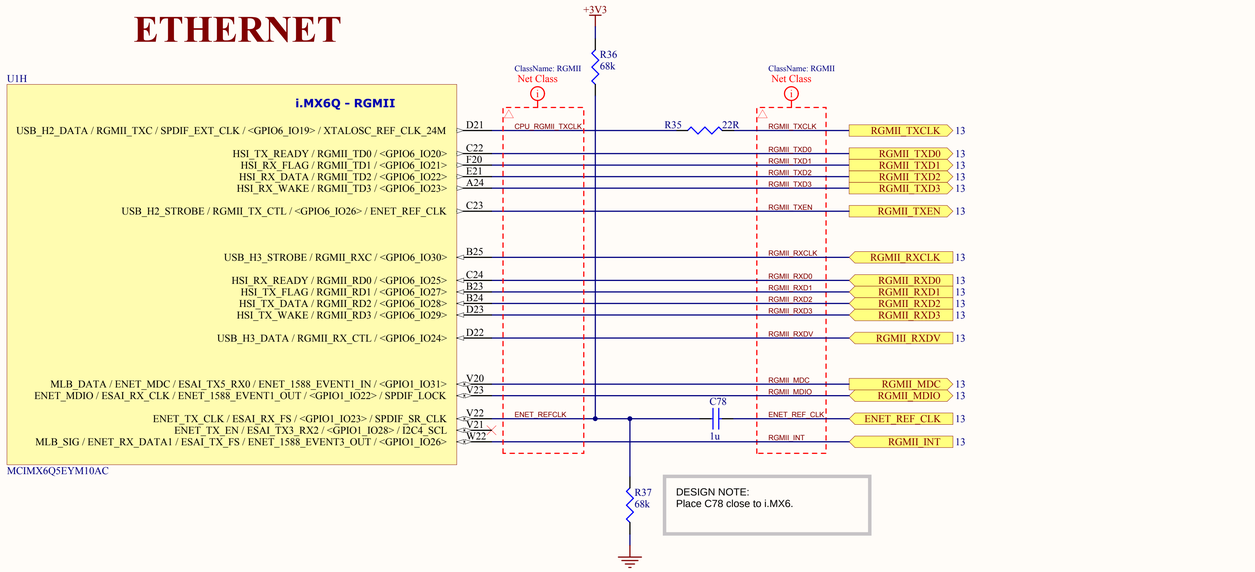
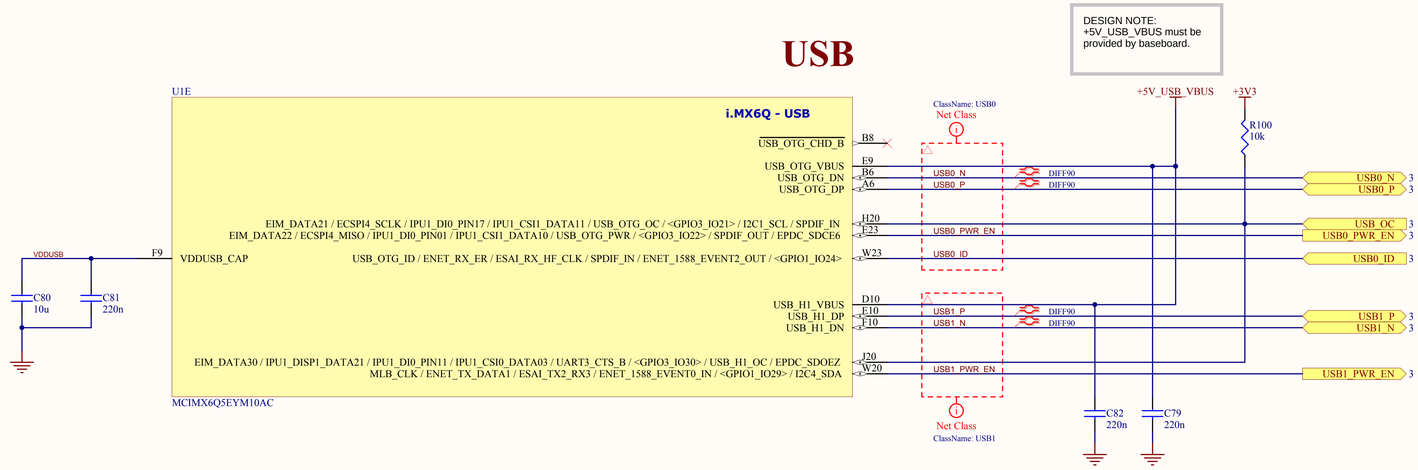
CPU - USB, ETHERNET

ETHERNET



USB



Title:	iMX6 Rex Module	Variant: Variant name not interpreted	
Page Contents:	[07] - CPU - USB, ETHERNET.SchDoc	Checked by	
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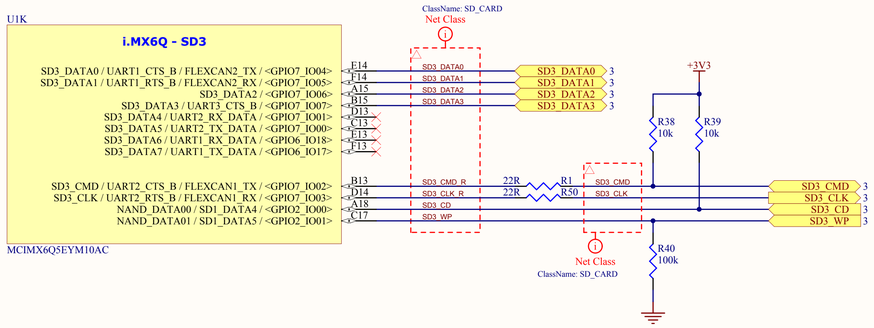
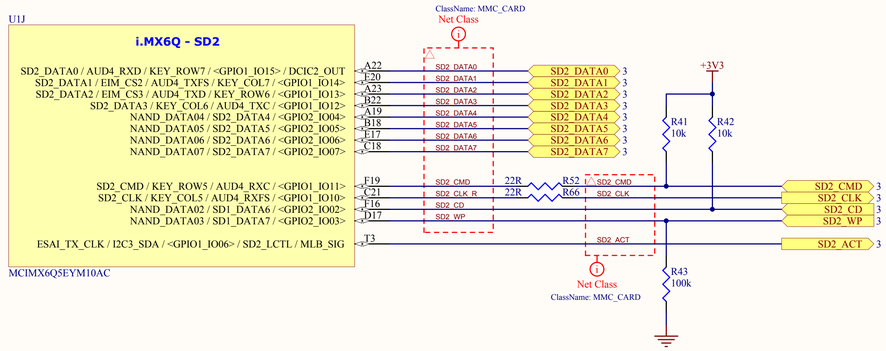
CPU - SPI, I2C, SD, MMC

SD-CARD

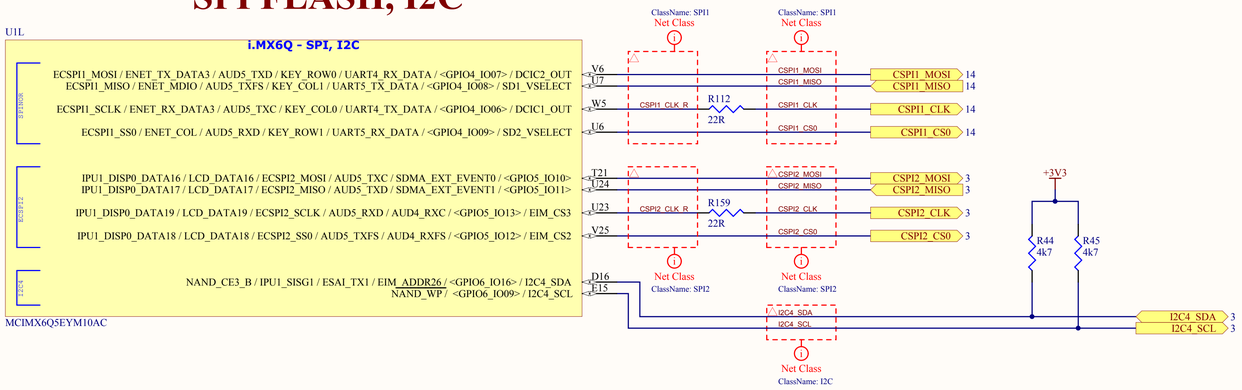


DESIGN NOTE:
The maximum image size to load in SD/MMC boot is 32MB. (iMX6 reference manual)

MMC-CARD



SPI FLASH, I2C



Title:	iMX6 Rex Module	Variant: Variant name not interpreted	
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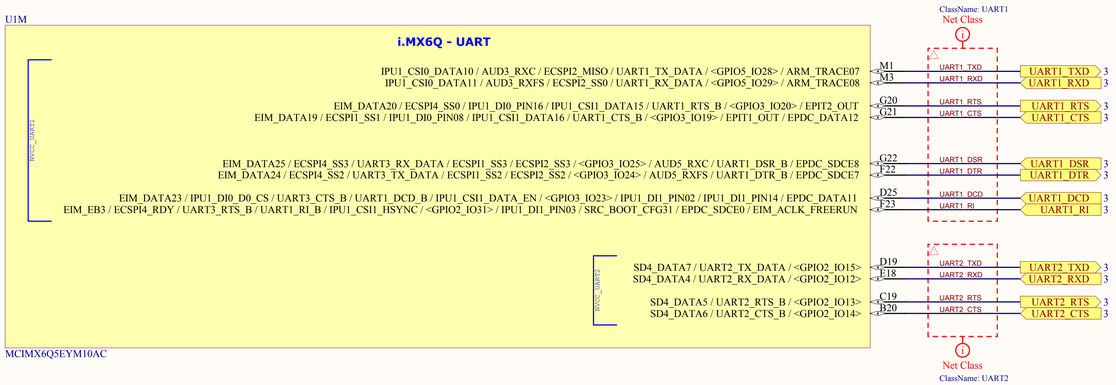
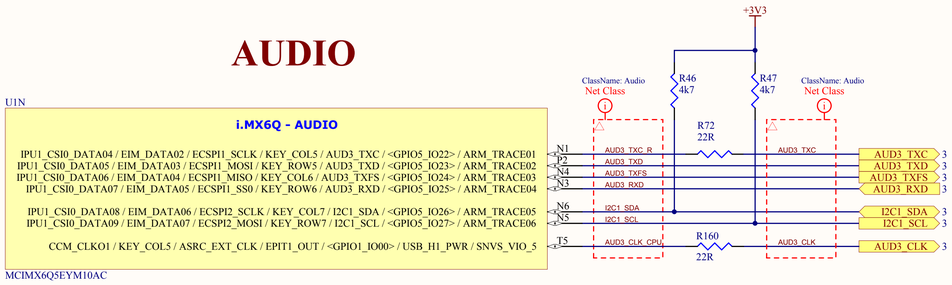
CPU - UART, AUDIO

UART



AUDIO



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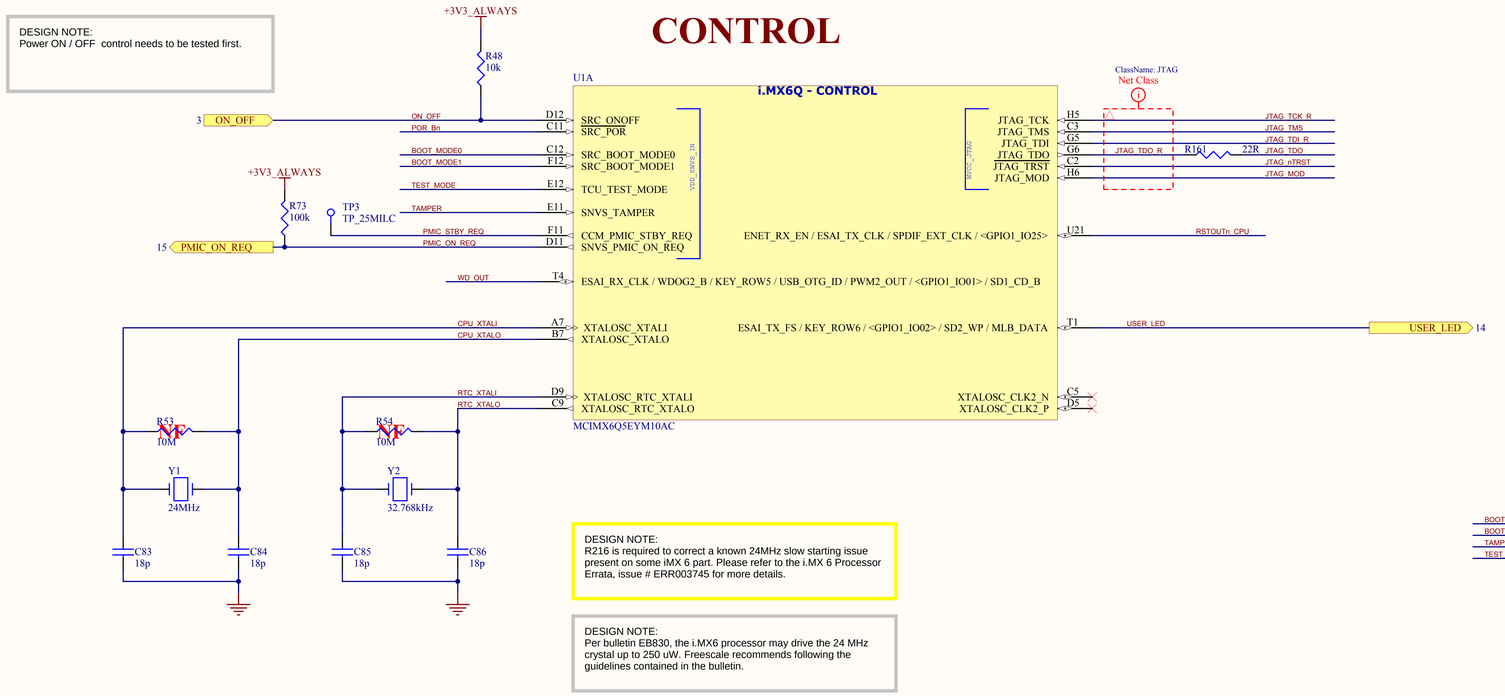
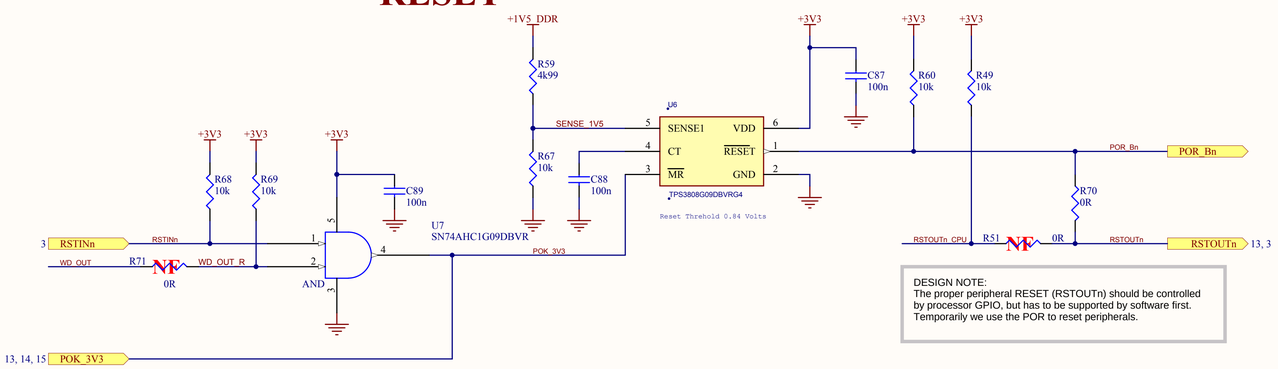
CPU - JTAG, CONTROL

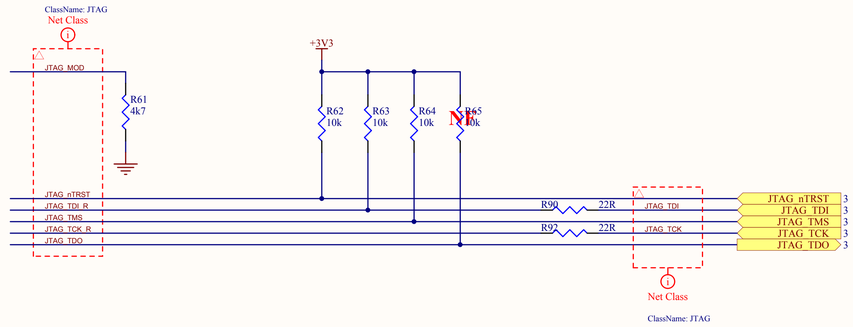
CONTROL



RESET



JTAG



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CPU - POWER

DESIGN NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

DESIGN NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 DualLite parts in which VDDSNVS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q TO1.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

MX6 power domains under-BGA decoupling (belongs to CPU pins on page 4)

DESIGN NOTE:
NVCC_PLL_OUT: R77, R79, R105 for testing only.

DESIGN NOTE:
NVCC_RGMII connected to 2V5 for RGMII 2V5 operation.

DESIGN NOTE:
Place close to NVCC_ENET pin

DESIGN NOTE:
Place close to NVCC_GPIO pin

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CPU - UNUSED PINS

U1O

i.MX6Q - UNUSED

D18	SD4_DATA0 / NAND_DQS / <GPIO2_IO08>	E16	SD4_CLK / NAND_WE_B / UART3_RX_DATA / <GPIO7_IO10>
B19	SD4_DATA1 / PWM3_OUT / <GPIO2_IO09>	B17	SD4_CMD / NAND_RE_B / UART3_TX_DATA / <GPIO7_IO09>
F17	SD4_DATA2 / PWM4_OUT / <GPIO2_IO10>		
A20	SD4_DATA3 / <GPIO2_IO11>	H24	<EIM_CS0> / IPU1_DI1_PIN05 / ECSPI2_SCLK / GPIO2_IO23 / EPDC_DATA06
		J23	<EIM_CS1> / IPU1_DI1_PIN06 / ECSPI2_MOSI / GPIO2_IO24 / EPDC_DATA08
B21	SD1_CMD / PWM4_OUT / GPT_COMPARE1 / <GPIO1_IO18>	N19	IPU1_DI0_DISP_CLK / LCD_CLK / <GPIO4_IO16> / LCD_WR_RWN
D20	SD1_CLK / GPT_CLKIN / <GPIO1_IO20>		
A17	SD1_DATA0 / GPT_CAPTURE1 / <GPIO1_IO16>	N25	IPU1_DI0_PIN02 / LCD_HSYNC / AUD6_TXD / <GPIO4_IO18> / LCD_RS
C20	SD1_DATA1 / PWM3_OUT / GPT_CAPTURE2 / <GPIO1_IO17>	V20	IPU1_DI0_PIN03 / LCD_VSYNC / AUD6_TXFS / <GPIO4_IO19> / LCD_CS
E19	SD1_DATA2 / GPT_COMPARE2 / PWM2_OUT / WDOG1_B / <GPIO1_IO19> / WDOG1_RESET_B_DEB	P25	IPU1_DI0_PIN04 / LCD_BUSY / AUD6_RXD / SD1_WP / <GPIO4_IO20> / LCD_RESET
		N21	IPU1_DI0_PIN15 / LCD_ENABLE / AUD6_TXC / <GPIO4_IO17> / LCD_RD_E
K22	<EIM_LBA> / IPU1_DI1_PIN17 / ECSPI2_SS1 / GPIO2_IO27 / SRC_BOOT_CFG26 / EPDC_DATA04		
J24	<EIM_OE> / IPU1_DI1_PIN07 / ECSPI2_MISO / GPIO2_IO25 / EPDC_PWR_IRQ	P24	IPU1_DISP0_DATA00 / LCD_DATA00 / ECSPI3_SCLK / <GPIO4_IO21>
K20	<EIM_RW> / IPU1_DI1_PIN08 / ECSPI2_SS0 / GPIO2_IO26 / SRC_BOOT_CFG29 / EPDC_DATA07	P22	IPU1_DISP0_DATA01 / LCD_DATA01 / ECSPI3_MOSI / <GPIO4_IO22>
		P23	IPU1_DISP0_DATA02 / LCD_DATA02 / ECSPI3_MISO / <GPIO4_IO23>
		P21	IPU1_DISP0_DATA03 / LCD_DATA03 / ECSPI3_SS0 / <GPIO4_IO24>
H25	<EIM_ADDR16> / IPU1_DI1_DISP_CLK / IPU1_CSI1_PIXCLK / GPIO2_IO22 / SRC_BOOT_CFG16 / EPDC_DATA00	P20	IPU1_DISP0_DATA04 / LCD_DATA04 / ECSPI3_SS1 / <GPIO4_IO25>
G24	<EIM_ADDR17> / IPU1_DISP1_DATA12 / IPU1_CSI1_DATA12 / GPIO2_IO21 / SRC_BOOT_CFG17 / EPDC_PWR_STAT	R25	IPU1_DISP0_DATA05 / LCD_DATA05 / ECSPI3_SS2 / AUD6_RXFS / <GPIO4_IO26>
J25	<EIM_ADDR18> / IPU1_DISP1_DATA13 / IPU1_CSI1_DATA13 / GPIO2_IO20 / SRC_BOOT_CFG18 / EPDC_PWR_CTRL0	R23	IPU1_DISP0_DATA06 / LCD_DATA06 / ECSPI3_SS3 / AUD6_RXC / <GPIO4_IO27>
G25	<EIM_ADDR19> / IPU1_DISP1_DATA14 / IPU1_CSI1_DATA14 / GPIO2_IO19 / SRC_BOOT_CFG19 / EPDC_PWR_CTRL1	R24	IPU1_DISP0_DATA07 / LCD_DATA07 / ECSPI3_RDY / <GPIO4_IO28>
H23	<EIM_ADDR20> / IPU1_DISP1_DATA15 / IPU1_CSI1_DATA15 / GPIO2_IO18 / SRC_BOOT_CFG20 / EPDC_PWR_CTRL2	R22	IPU1_DISP0_DATA08 / LCD_DATA08 / PWM1_OUT / WDOG1_B / <GPIO4_IO29>
H22	<EIM_ADDR21> / IPU1_DISP1_DATA16 / IPU1_CSI1_DATA16 / GPIO2_IO17 / SRC_BOOT_CFG21 / EPDC_GDCLK	T25	IPU1_DISP0_DATA09 / LCD_DATA09 / PWM2_OUT / WDOG2_B / <GPIO4_IO30>
F24	<EIM_ADDR22> / PU1_DISP1_DATA17 / IPU1_CSI1_DATA17 / GPIO2_IO16 / SRC_BOOT_CFG22 / EPDC_GDSP	R21	IPU1_DISP0_DATA10 / LCD_DATA10 / <GPIO4_IO31>
J21	<EIM_ADDR23> / IPU1_DISP1_DATA18 / IPU1_CSI1_DATA18 / IPU1_SISG3 / GPIO6_IO06 / SRC_BOOT_CFG23 / EPDC_GDOE	T23	IPU1_DISP0_DATA11 / LCD_DATA11 / <GPIO5_IO05>
F25	<EIM_ADDR24> / IPU1_DISP1_DATA19 / IPU1_CSI1_DATA19 / IPU1_SISG2 / GPIO5_IO04 / SRC_BOOT_CFG24 / EPDC_GDRL	T24	IPU1_DISP0_DATA12 / LCD_DATA12 / <GPIO5_IO06>
		R20	IPU1_DISP0_DATA13 / LCD_DATA13 / AUD5_RXFS / <GPIO5_IO07>
		U25	IPU1_DISP0_DATA14 / LCD_DATA14 / AUD5_RXC / <GPIO5_IO08>
M2	IPU1_CSI0_DATA12 / EIM_DATA08 / UART4_TX_DATA / <GPIO5_IO30> / ARM_TRACE09	U22	IPU1_DISP0_DATA15 / LCD_DATA15 / ECSPI1_SS1 / ECSPI2_SS1 / <GPIO5_IO09>
L1	IPU1_CSI0_DATA13 / EIM_DATA09 / UART4_RX_DATA / <GPIO5_IO31> / ARM_TRACE10		
M4	IPU1_CSI0_DATA14 / EIM_DATA10 / UART5_TX_DATA / <GPIO6_IO00> / ARM_TRACE11		
M5	IPU1_CSI0_DATA15 / EIM_DATA11 / UART5_RX_DATA / <GPIO6_IO01> / ARM_TRACE12	T20	IPU1_DISP0_DATA20 / LCD_DATA20 / ECSPI1_SCLK / AUD4_TXC / <GPIO5_IO14>
L4	IPU1_CSI0_DATA16 / EIM_DATA12 / UART4_RTS_B / <GPIO6_IO02> / ARM_TRACE13	V24	IPU1_DISP0_DATA21 / LCD_DATA21 / ECSPI1_MOSI / AUD4_TXD / <GPIO5_IO15>
L3	IPU1_CSI0_DATA17 / EIM_DATA13 / UART4_CTS_B / <GPIO6_IO03> / ARM_TRACE14	W24	IPU1_DISP0_DATA22 / LCD_DATA22 / ECSPI1_MISO / AUD4_TXFS / <GPIO5_IO16>
M6	IPU1_CSI0_DATA18 / EIM_DATA14 / UART5_RTS_B / <GPIO6_IO04> / ARM_TRACE15		IPU1_DISP0_DATA23 / LCD_DATA23 / ECSPI1_SS0 / AUD4_RXD / <GPIO5_IO17>
L6	IPU1_CSI0_DATA19 / EIM_DATA15 / UART5_CTS_B / <GPIO6_IO05>		
		W21	ENET_RX_DATA0 / ESAI_TX_HF_CLK / SPDIF_OUT / <GPIO1_IO27>
P4	IPU1_CSI0_HSYNC / CCM_CLKO1 / <GPIO5_IO19> / ARM_TRACE_CTL	U20	ENET_TX_DATA0 / ESAI_TX4_RX1 / <GPIO1_IO30>
P1	IPU1_CSI0_PIXCLK / <GPIO5_IO18> / ARM_EVENTO	W6	ECSPI1_SS1 / ENET_RX_DATA2 / FLEXCAN1_TX / KEY_COL2 / ENET_MDC / <GPIO4_IO10> / USB_H1_PWR_CTL_WAKE
N2	IPU1_CSI0_VSYNC / EIM_DATA01 / <GPIO5_IO21> / ARM_TRACE00	T6	FLEXCAN2_TX / IPU1_SISG4 / USB_OTG_OC / KEY_COL4 / UART5_RTS_B / <GPIO4_IO14>
		V5	FLEXCAN2_RX / IPU1_SISG5 / USB_OTG_PWR / KEY_ROW4 / UART5_CTS_B / <GPIO4_IO15>
D15	SD3_RESET / UART3_RTS_B / <GPIO7_IO08>	R6	ESAI_TX_HF_CLK / KEY_COL7 / <GPIO1_IO04> / SD2_CD_B
B11	MLB_CLK_P		
A11	MLB_CLK_N		
		R3	ESAI_TX4_RX1 / EPIT1_OUT / FLEXCAN1_TX / UART2_TX_DATA / <GPIO1_IO07> / SPDIF_LOCK / USB_OTG_HOST_MODE / I2C4_SCL
B9	MLB_SIG_P	R5	ESAI_TX5_RX0 / XTALOSC_REF_CLK_32K / EPIT2_OUT / FLEXCAN1_RX / UART2_RX_DATA / <GPIO1_IO08> / SPDIF_SR_CLK / USB_OTG_PWR_CTL_WAKE / I2C4_SDA
A9	MLB_SIG_N	T2	ESAI_RX_FS / WDOG1_B / KEY_COL6 / CCM_REF_EN_B / PWM1_OUT / <GPIO1_IO09> / SD1_WP
		R1	ESAI_TX0 / ENET_1588_EVENT3_IN / CCM_PMIC_READY / SDMA_EXT_EVENT0 / SPDIF_OUT / <GPIO7_IO12>
A10	MLB_DATA_P	P6	ESAI_TX1 / ENET_RX_CLK / SD3_VSELECT / SDMA_EXT_EVENT1 / ASRC_EXT_CLK / <GPIO7_IO13> / SNVS_VIO_5_CTL
B10	MLB_DATA_N	P5	KEY_COL5 / ENET_1588_EVENT0_OUT / SPDIF_OUT / CCM_CLKO1 / ECSPI1_RDY / <GPIO4_IO05> / ENET_TX_ER
F4	CSI_CLK0_N	H19	<EIM_ADDR25> / ECSPI4_SS1 / ECSPI2_RDY / IPU1_DI1_PIN12 / IPU1_DI0_D1_CS / GPIO5_IO02 / HDMI_TX_CEC_LINE / EPDC_DATA15 / EIM_ACLK_FREERUN
F3	CSI_CLK0_P		
		C25	EIM_DATA16 / ECSPI1_SCLK / IPU1_DI0_PIN05 / IPU1_CSI1_DATA18 / HDMI_TX_DDC_SDA / <GPIO3_IO16> / I2C2_SDA / EPDC_DATA10
E4	CSI_DATA0_N	T21	EIM_DATA17 / ECSPI1_MISO / IPU1_DI0_PIN06 / IPU1_CSI1_PIXCLK / DCIC1_OUT / <GPIO3_IO17> / I2C3_SCL / EPDC_VCOM0
E3	CSI_DATA0_P	D24	EIM_DATA18 / ECSPI1_MOSI / IPU1_DI0_PIN07 / IPU1_CSI1_DATA17 / IPU1_DI1_D0_CS / <GPIO3_IO18> / I2C3_SDA / EPDC_VCOM1
D1	CSI_DATA1_N	E24	EIM_DATA26 / IPU1_DI1_PIN11 / IPU1_CSI0_DATA01 / IPU1_CSI1_DATA14 / UART2_TX_DATA / <GPIO3_IO26> / IPU1_SISG2 / IPU1_DISP1_DATA22 / EPDC_SDOED
D2	CSI_DATA1_P	E25	EIM_DATA27 / IPU1_DI1_PIN13 / IPU1_CSI0_DATA00 / IPU1_CSI1_DATA13 / UART2_RX_DATA / <GPIO3_IO27> / IPU1_SISG3 / IPU1_DISP1_DATA23 / EPDC_SDOE
		G23	EIM_DATA28 / I2C1_SDA / ECSPI4_MOSI / IPU1_CSI1_DATA12 / UART2_CTS_B / <GPIO3_IO28> / IPU1_EXT_TRIG / IPU1_DI0_PIN13 / EPDC_PWR_CTRL3
E1	CSI_D2M	J19	EIM_DATA29 / IPU1_DI1_PIN15 / ECSPI4_SS0 / UART2_RTS_B / <GPIO3_IO29> / IPU1_CSI1_VSYNC / IPU1_DI0_PIN14 / EPDC_PWR_WAKE
E2	CSI_D2P		
		H21	EIM_DATA31 / IPU1_DISP1_DATA20 / IPU1_DI0_PIN12 / IPU1_CSI0_DATA02 / UART3_RTS_B / <GPIO3_IO31> / USB_H1_PWR / EPDC_SDCLK_P / EIM_ACLK_FREERUN
F2	CSI_D3M		
F1	CSI_D3P	E22	EIM_EB2 / ECSPI1_SS0 / IPU1_CSI1_DATA19 / HDMI_TX_DDC_SCL / <GPIO2_IO30> / I2C2_SCL / SRC_BOOT_CFG30 / EPDC_DATA05
D4	CSI_REXT	N22	<EIM_BCLK> / IPU1_DI1_PIN16 / GPIO6_IO31 / EPDC_SDCE9
		M25	<EIM_WAIT> / EIM_DTACK_B / GPIO5_IO00 / SRC_BOOT_CFG25
H3	DSI_CLK0_N	K21	<EIM_EB0> / IPU1_DISP1_DATA11 / IPU1_CSI1_DATA11 / CCM_PMIC_READY / GPIO2_IO28 / SRC_BOOT_CFG27 / EPDC_PWR_COM
H4	DSI_CLK0_P	K23	<EIM_EB1> / IPU1_DISP1_DATA10 / IPU1_CSI1_DATA10 / GPIO2_IO29 / SRC_BOOT_CFG28 / EPDC_SDSHR
G2	DSI_DATA0_N	L20	<EIM_AD00> / IPU1_DISP1_DATA09 / IPU1_CSI1_DATA09 / GPIO3_IO00 / SRC_BOOT_CFG00 / EPDC_SDCLK_N
G1	DSI_DATA0_P	J25	<EIM_AD01> / IPU1_DISP1_DATA08 / IPU1_CSI1_DATA08 / GPIO3_IO01 / SRC_BOOT_CFG01 / EPDC_SDLE
		J21	<EIM_AD02> / IPU1_DISP1_DATA07 / IPU1_CSI1_DATA07 / GPIO3_IO02 / SRC_BOOT_CFG02 / EPDC_BDR0
H2	DSI_DATA1_N	K24	<EIM_AD03> / IPU1_DISP1_DATA06 / IPU1_CSI1_DATA06 / GPIO3_IO03 / SRC_BOOT_CFG03 / EPDC_BDR1
H1	DSI_DATA1_P	J22	<EIM_AD04> / IPU1_DISP1_DATA05 / IPU1_CSI1_DATA05 / GPIO3_IO04 / SRC_BOOT_CFG04 / EPDC_SDCE0
		J23	<EIM_AD05> / IPU1_DISP1_DATA04 / IPU1_CSI1_DATA04 / GPIO3_IO05 / SRC_BOOT_CFG05 / EPDC_SDCE1
G4	DSI_REXT	K25	<EIM_AD06> / IPU1_DISP1_DATA03 / IPU1_CSI1_DATA03 / GPIO3_IO06 / SRC_BOOT_CFG06 / EPDC_SDCE2
		J25	<EIM_AD07> / IPU1_DISP1_DATA02 / IPU1_CSI1_DATA02 / GPIO3_IO07 / SRC_BOOT_CFG07 / EPDC_SDCE3
		J24	<EIM_AD08> / IPU1_DISP1_DATA01 / IPU1_CSI1_DATA01 / GPIO3_IO08 / SRC_BOOT_CFG08 / EPDC_SDCE4
F15	NAND_CE0_B / <GPIO6_IO11>	M21	<EIM_AD09> / IPU1_DISP1_DATA00 / IPU1_CSI1_DATA00 / GPIO3_IO09 / SRC_BOOT_CFG09 / EPDC_SDCE5
C16	NAND_CE1_B / SD4_VSELECT / SD3_VSELECT / <GPIO6_IO14>	M22	<EIM_AD10> / IPU1_DI1_PIN15 / IPU1_CSI1_DATA_EN / GPIO3_IO10 / SRC_BOOT_CFG10 / EPDC_DATA01
		M20	<EIM_AD11> / IPU1_DI1_PIN02 / IPU1_CSI1_HSYNC / GPIO3_IO11 / SRC_BOOT_CFG11 / EPDC_DATA03
A16	NAND_ALE / SD4_RESET / <GPIO6_IO08>	M24	<EIM_AD12> / IPU1_DI1_PIN03 / IPU1_CSI1_VSYNC / GPIO3_IO12 / SRC_BOOT_CFG12 / EPDC_DATA02
C15	NAND_CLE / <GPIO6_IO07>	M23	<EIM_AD13> / IPU1_DI1_D0_CS / GPIO3_IO13 / SRC_BOOT_CFG13 / EPDC_DATA13
B16	NAND_READY / <GPIO6_IO10>	N23	<EIM_AD14> / IPU1_DI1_D1_CS / GPIO3_IO14 / SRC_BOOT_CFG14 / EPDC_DATA14
		N24	<EIM_AD15> / IPU1_DI1_PIN01 / IPU1_DI1_PIN04 / GPIO3_IO15 / SRC_BOOT_CFG15 / EPDC_DATA09

MCIMX6Q5EYM10AC

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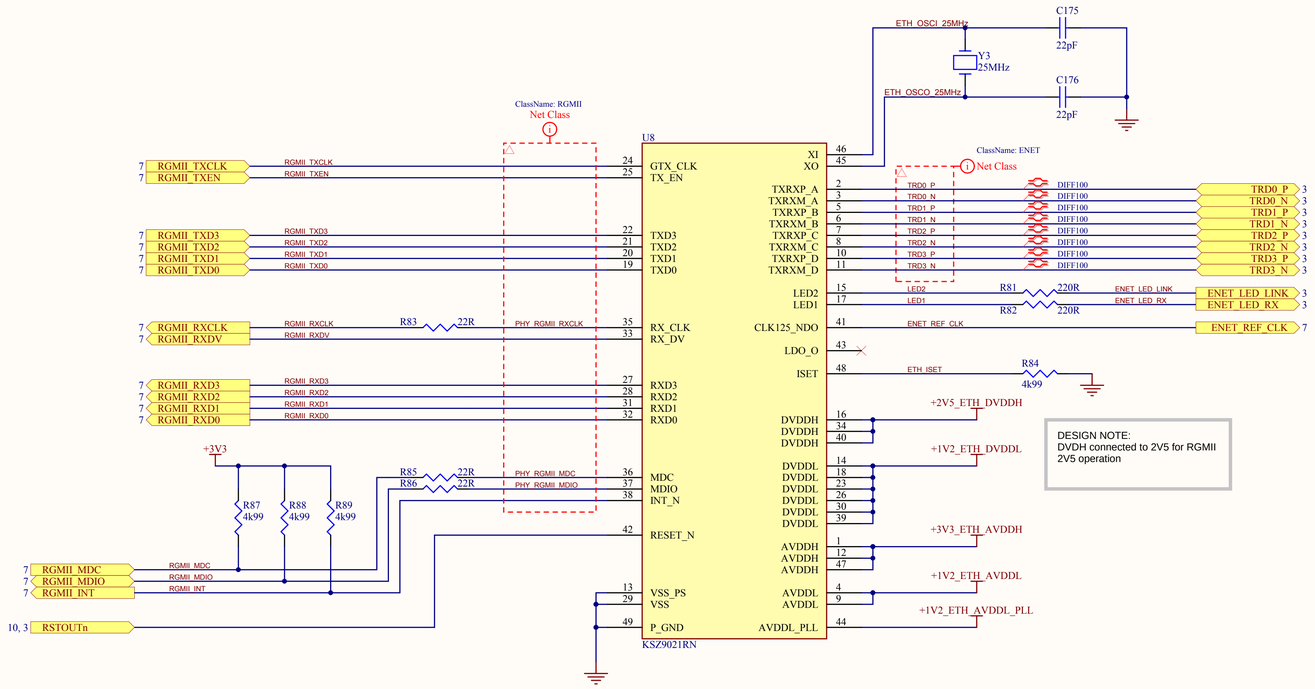
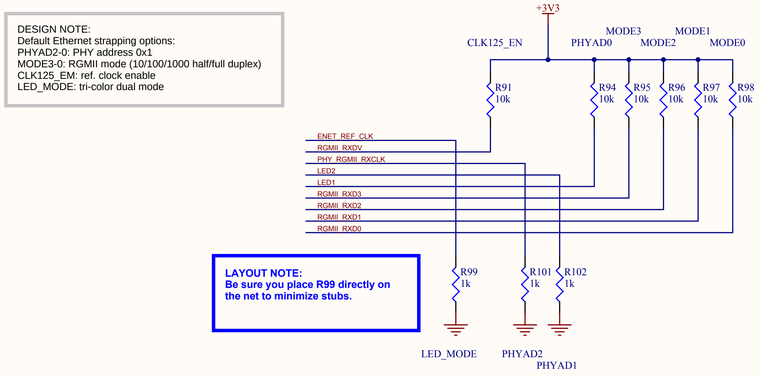
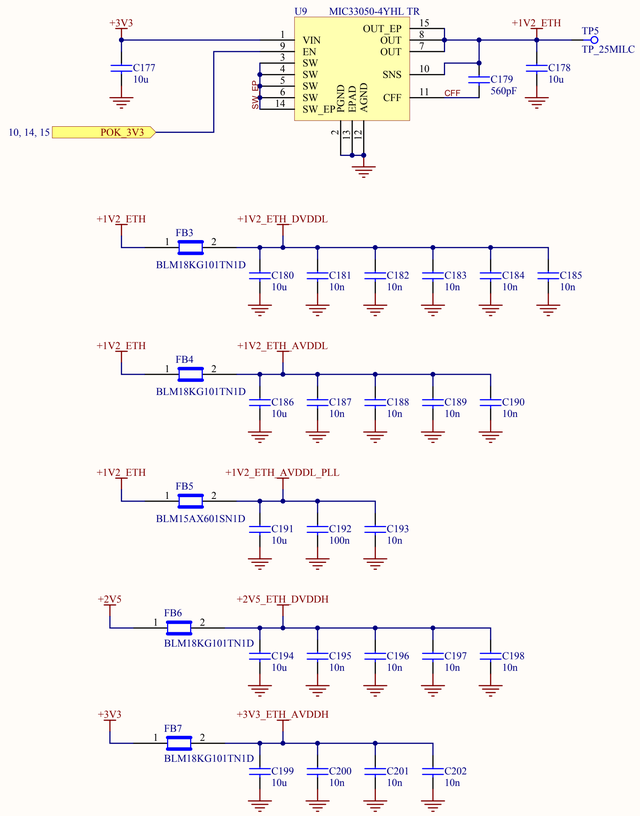
Title:	iMX6 Rex Module	Variant:	Variant name not interpreted
Page Contents:	[12] - CPU - UNUSED.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
Date:	20. 5. 2013	Sheet	12 of 20

ETHERNET PHY







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Title:	iMX6 Rex Module	Variant:	Variant name not interpreted
Page Contents:	[13] - ETHERNET PHY.SchDoc		Checked by
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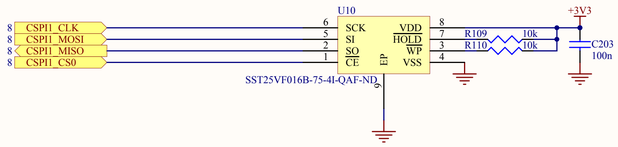
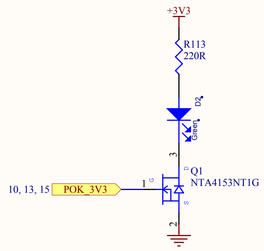
SPI FLASH, LED

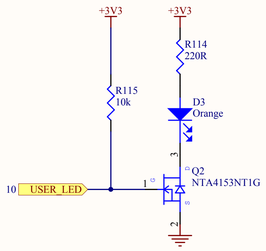
SPI NOR FLASH



POWER LED



USER DEFINED LED



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Title:	iMX6 Rex Module	Variant: Variant name not interpreted	
Page Contents:	[14] - SPI FLASH, LEDS.SchDoc	Checked by	
Size:	DWG NO		Revision: V1I1
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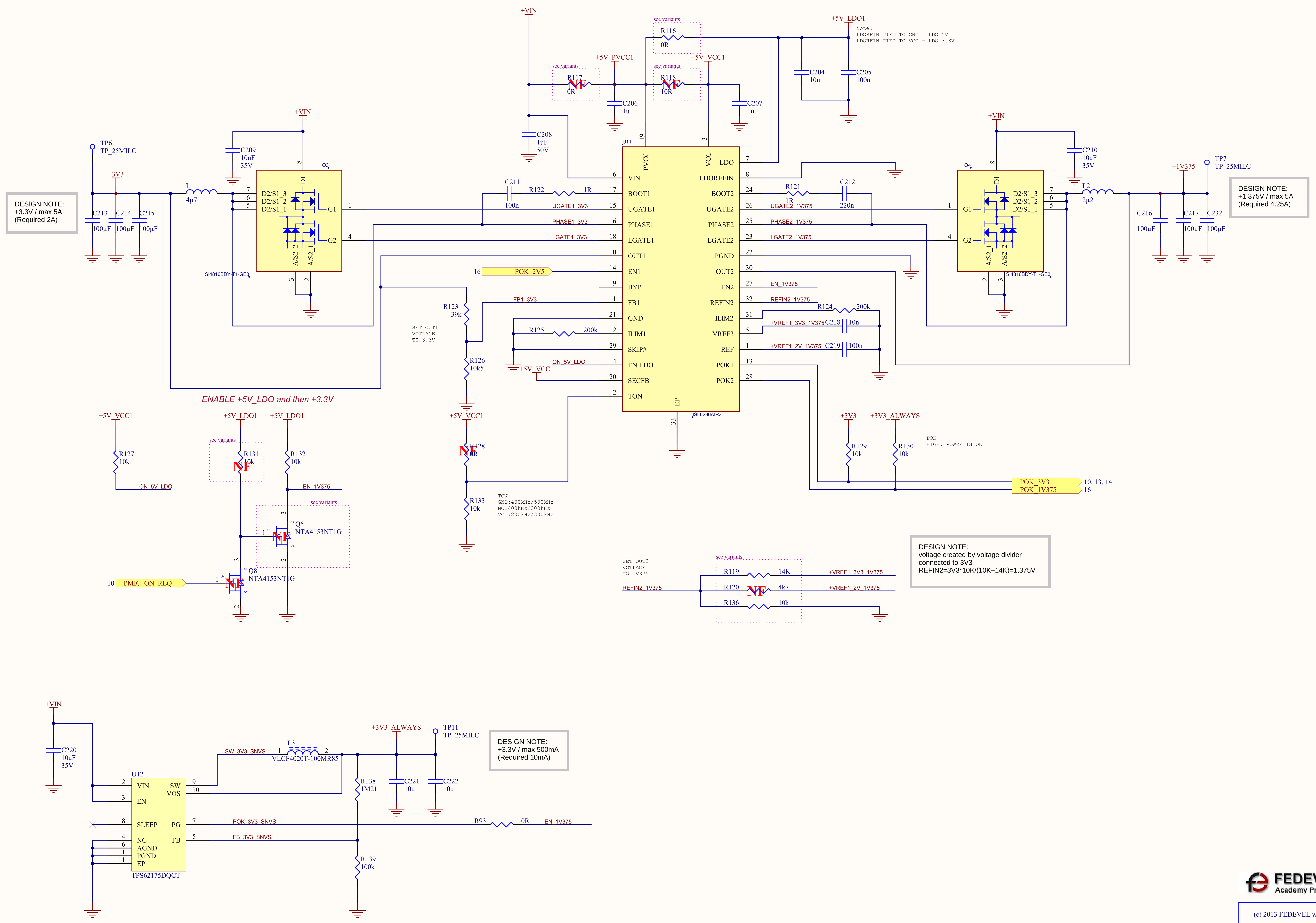
POWER +3.3V, +1.375V CON



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Title: iMX6 Rex Module	Variant: Variant name not interpreted
Page Contents: [15] - PWR 3V3, 1V375.SchDoc	Checked by
Size: DWG NO	Revision: V1I1
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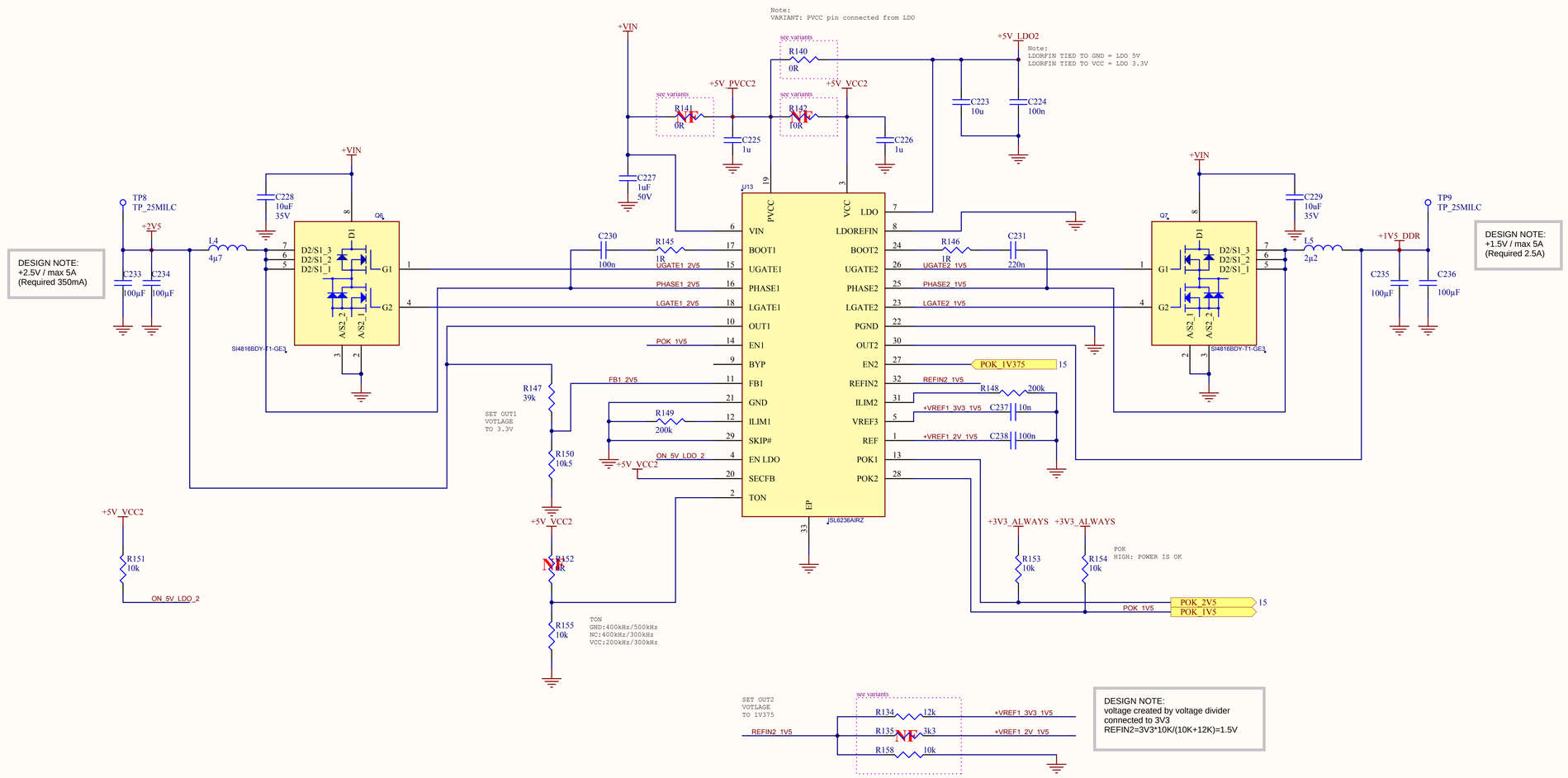
POWER +2.5V, +1.5V CON



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Title:	iMX6 Rex Module	Variant:	Variant name not interpreted
Page Contents:	[16] - PWR 2V5, 1V5.SchDoc		Checked by
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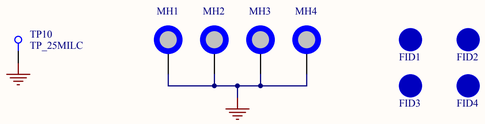
MECHANICAL



PCB1

PCB

iMX6 Rex V1I1 PCB

FIRMWARE_FOR_U10

FIRMWARE
uBOOT

iMX6_REX_uBOOT 1.0

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Title: iMX6 Rex Module	Variant: Variant name not interpreted	
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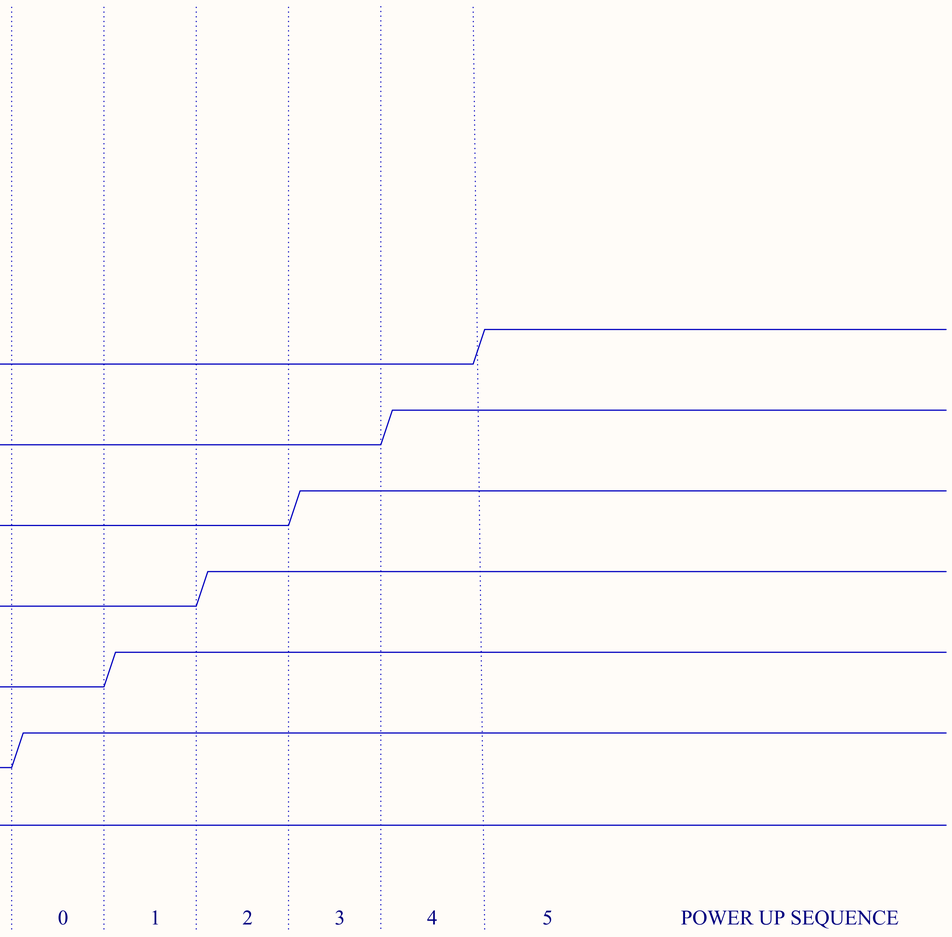
CPU - POWER SEQUENCING

+USB_VBUS	5V		
+DDR_VREF	0V75	+1V5_DDR	ref. for DDR memories, gen. with volt. divider
+1V2_VDD_ARM_CAP	1V2	iMX	cpu, core caps
+1V1_VDDSOC_CAP	1V1	iMX	core caps, cpu-sata, cpu-pcie, cpu-hdmi

OTHER USED SIGNAL	LEVEL	GEN BY	SUPPLIED FROM SIGNAL



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Title:	iMX6 Rex Module	Variant: Variant name not interpreted	
Page Contents:	[18] - POWER SEQUENCING.SchDoc	Checked by	
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DOC: REVISION HISTORY

CLOCKS (CPU & PCIE)

Title:	iMX6 Rex Module	Variant:	Variant name not interpreted
Page Contents:	[19] - DOC REVISION HISTORY.SchDoc	Checked by	
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[01] - COVER PAGE.SchDoc
[01] - COVER PAGE.SchDoc

[02] - BLOCK DIAGRAM.SchDoc
[02] - BLOCK DIAGRAM.SchDoc

[03] - CONNECTORS.SchDoc
[03] - CONNECTORS.SchDoc

[04] - CPU - DDR3, DDR3 MEM.SchDoc
[04] - CPU - DDR3, DDR3 MEM.SchDoc

[05] - CPU - PCIE, SATA.SchDoc
[05] - CPU - PCIE, SATA.SchDoc

[06] - CPU - HDMI, LVDS.SchDoc
[06] - CPU - HDMI, LVDS.SchDoc

[07] - CPU - USB, ETHERNET.SchDoc
[07] - CPU - USB, ETHERNET.SchDoc

[08] - CPU - SPI, I2C, SD, MMC.SchDoc
[08] - CPU - SPI, I2C, SD, MMC.SchDoc

[09] - CPU - UART, AUDIO.SchDoc
[09] - CPU - UART, AUDIO.SchDoc

[10] - CPU - JTAG, CONTROL.SchDoc
[10] - CPU - JTAG, CONTROL.SchDoc

[11] - CPU - POWER.SchDoc
[11] - CPU - POWER.SchDoc

[12] - CPU - UNUSED.SchDoc
[12] - CPU - UNUSED.SchDoc

[13] - ETHERNET PHY.SchDoc
[13] - ETHERNET PHY.SchDoc

[14] - SPI FLASH, LEDS.SchDoc
[14] - SPI FLASH, LEDS.SchDoc

[15] - PWR 3V3, 1V375.SchDoc
[15] - PWR 3V3, 1V375.SchDoc

[16] - PWR 2V5, 1V5.SchDoc
[16] - PWR 2V5, 1V5.SchDoc

[17] - MECH.SchDoc
[17] - MECH.SchDoc

[18] - POWER SEQUENCING.SchDoc
[18] - POWER SEQUENCING.SchDoc

[19] - DOC REVISION HISTORY.SchDoc
[19] - DOC REVISION HISTORY.SchDoc

TEMPLATE NOTES

Set Project Parameters

1) Go to Project -> Project Options -> Parameters
2) Set Company, Project and VersionRevision

Mark Not Fitted Components as
NF

Net Class Example

Net Class
ClassName: PCIE

Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Ttitle

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

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Title:	iMX6 Rex Module	Variant: Variant name not interpreted	
Page Contents:	iMX6 Rex_V1I1 Project.SchDoc	Checked by	
Size:	DWG NO		Revision: V1I1
Date:	20. 5. 2013	Sheet 20 of 20	