

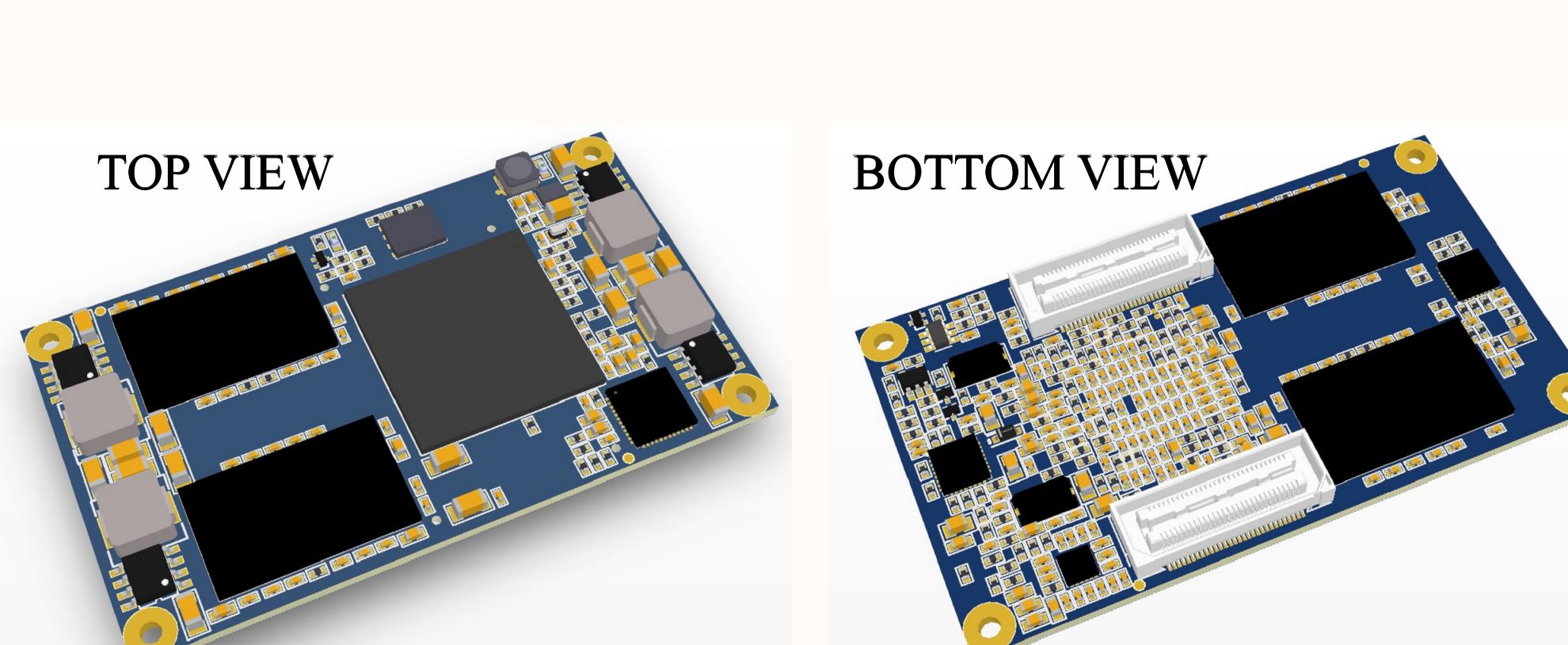
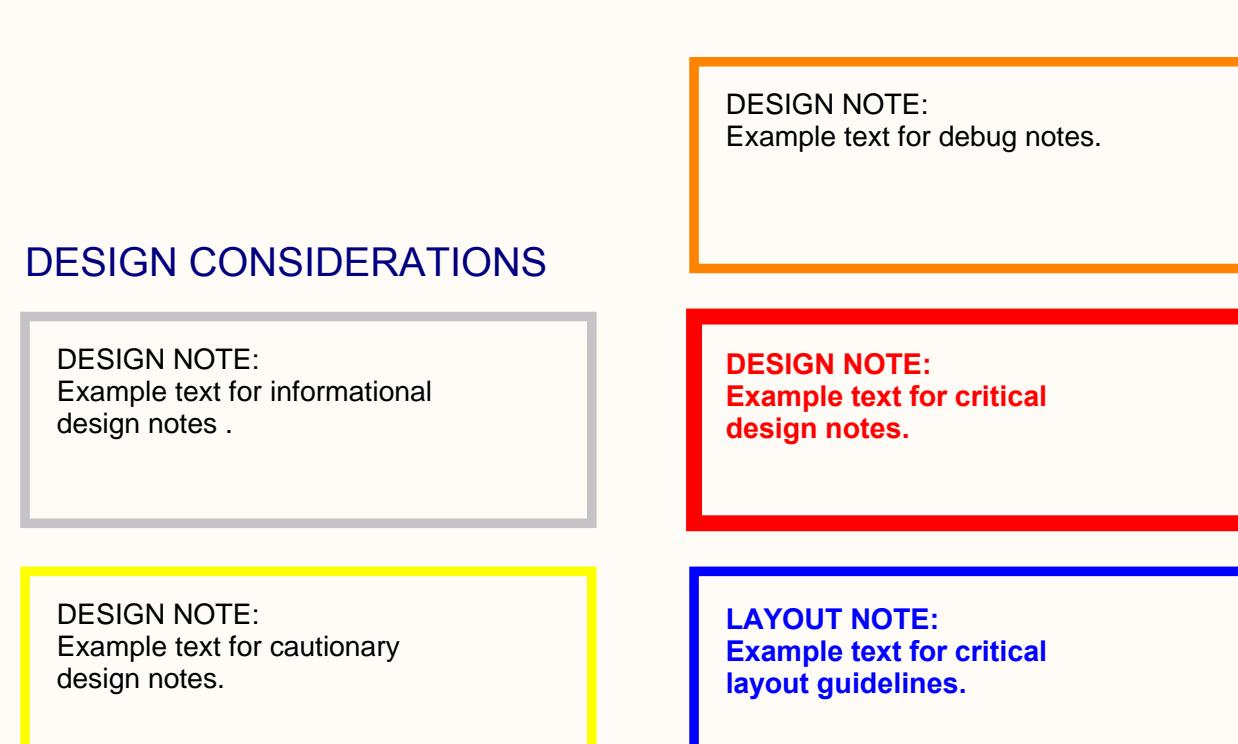
iMX6 Rex Module

Variant: Variant name not interpreted

19. 8. 2013
V1I1

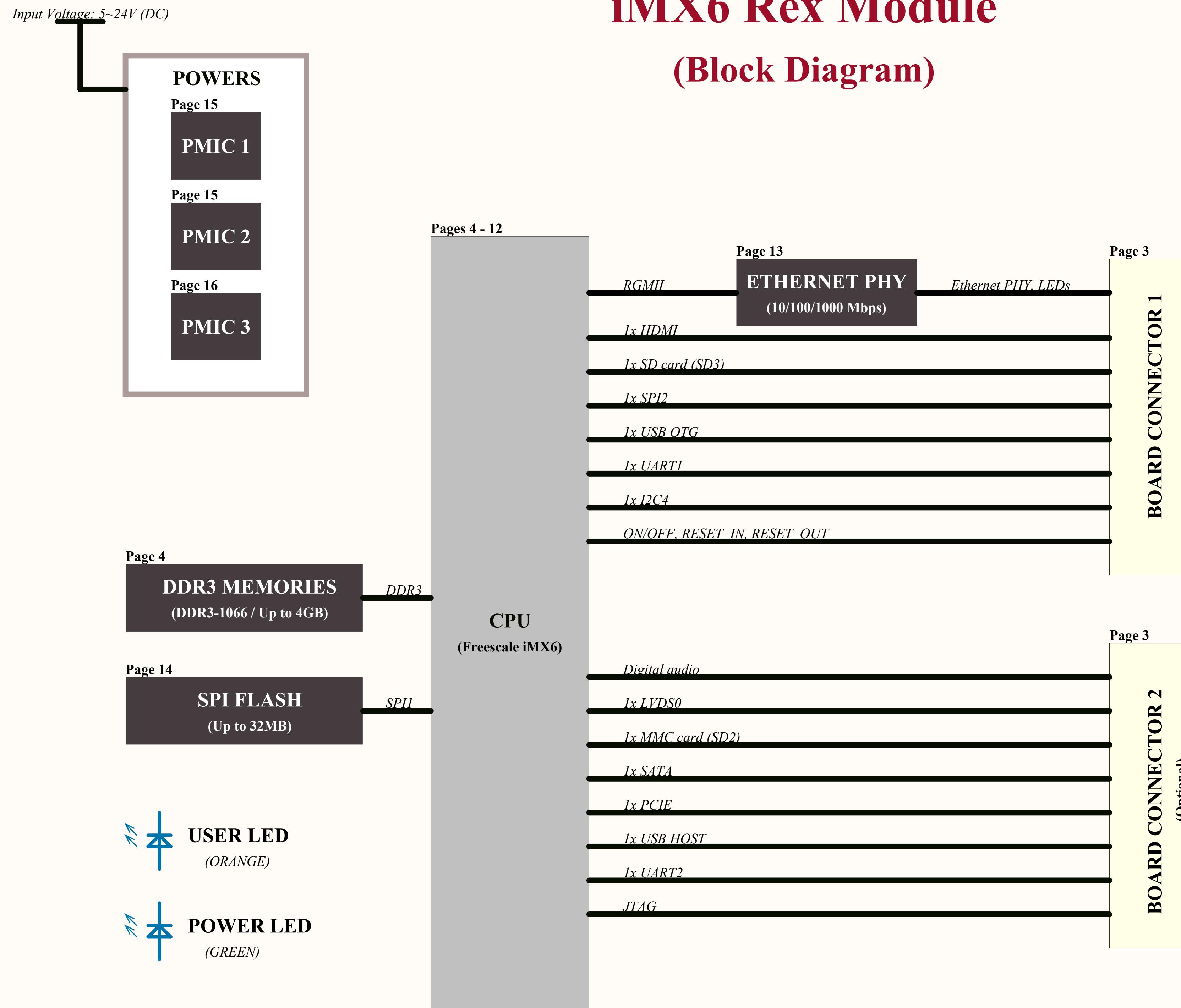
CHECKED

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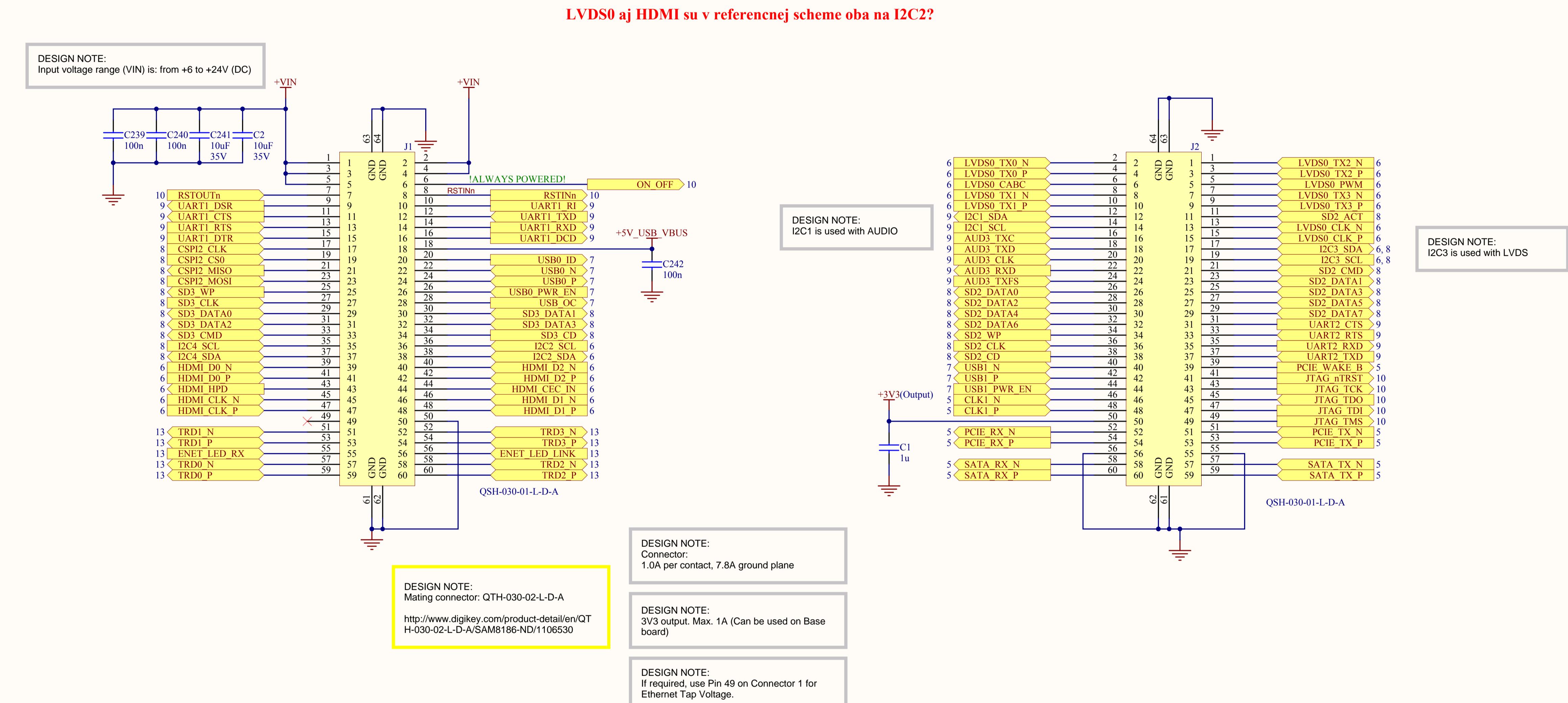
iMX6 Rex Module

(Block Diagram)

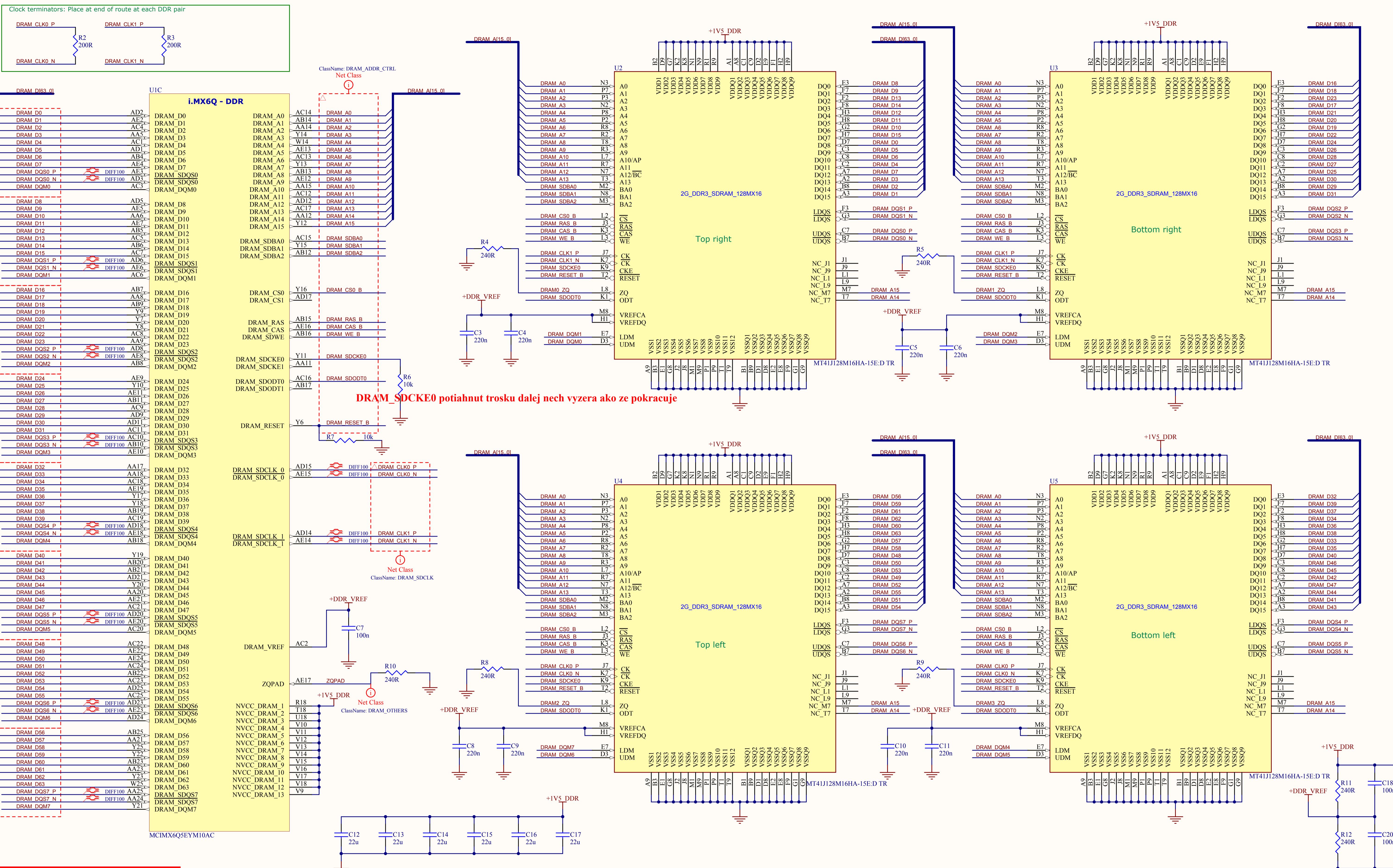


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CONNECTORS



CPU - DDR3, DDR3 MEM



DESIGN NOTE:
Pull down resistor RX3 is added to trace SDCKE0 in Rev B4 by soldering to an existing

DESIGN NOTE:

DESIGN NOTE:
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration. Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

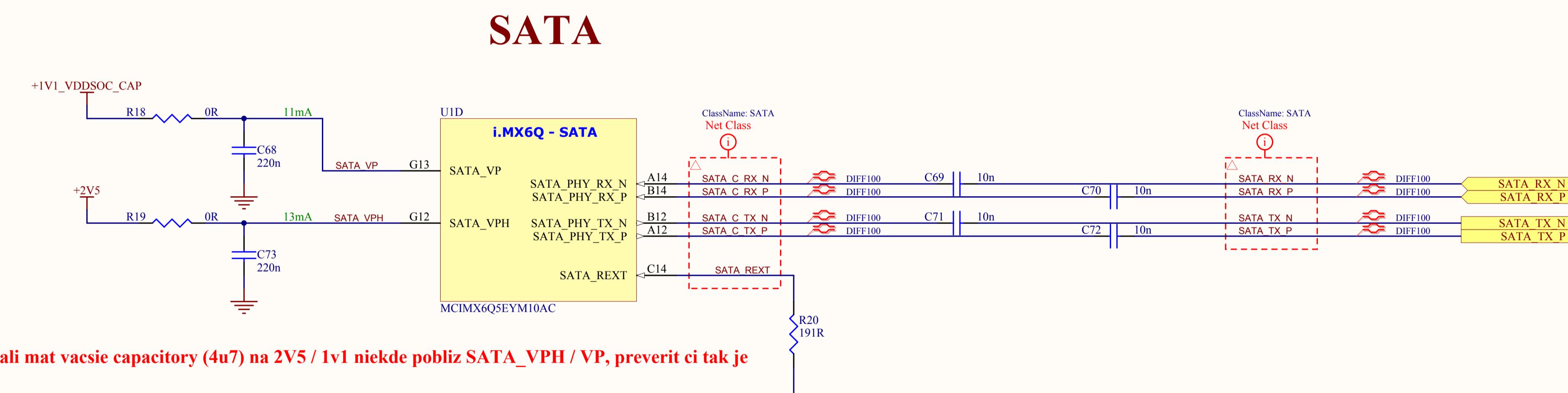
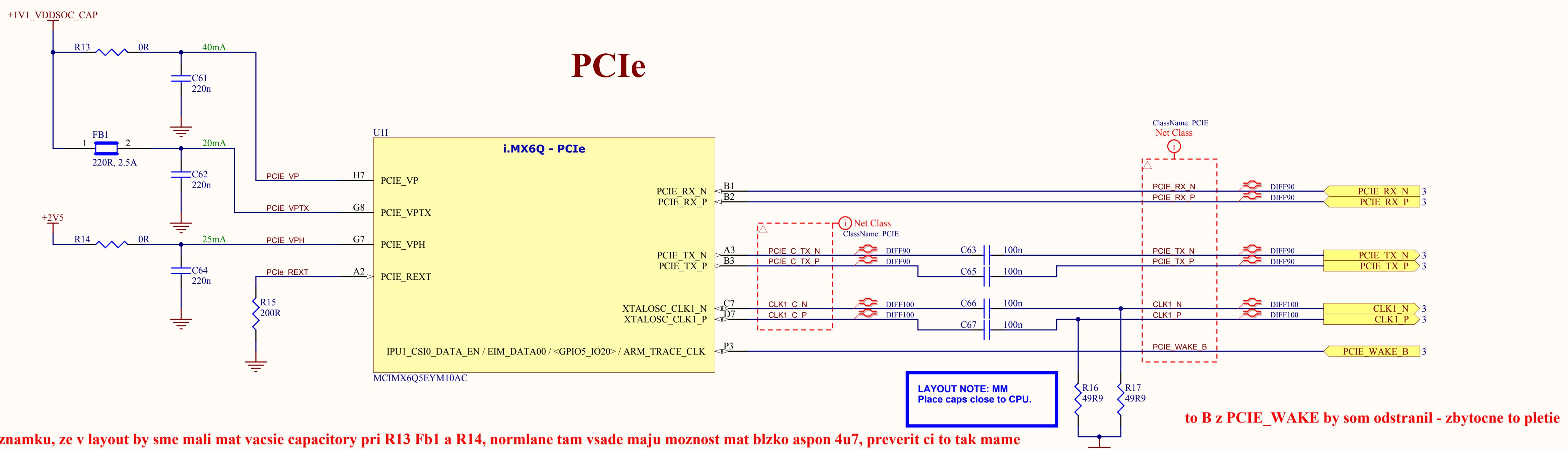
DESIGN NOTE:
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQS₀, and DQS₁ pins and for the left-to-right swap.



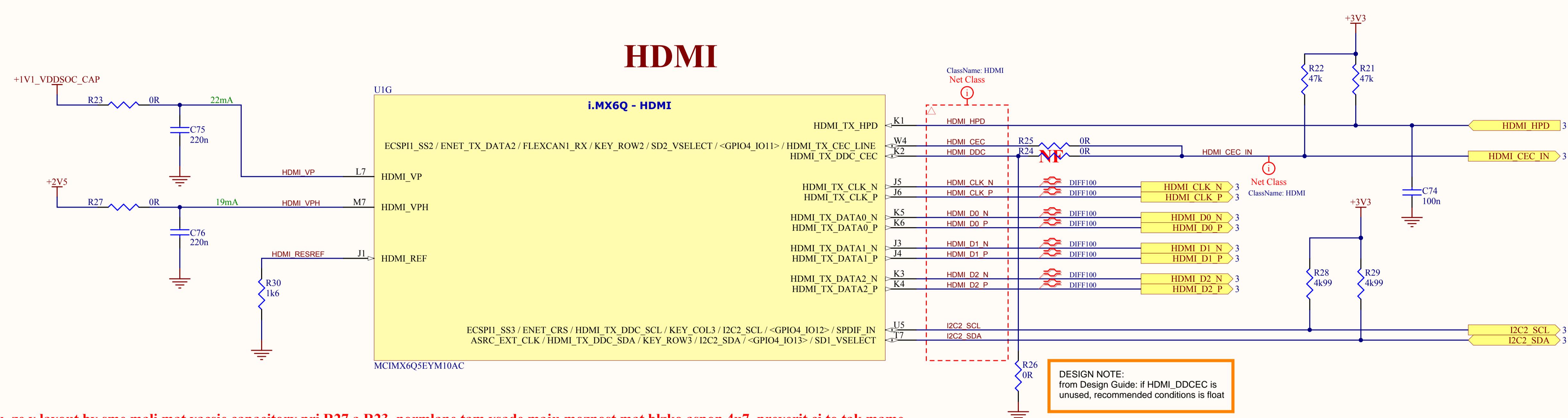
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Title:	iMX6 Rex Module
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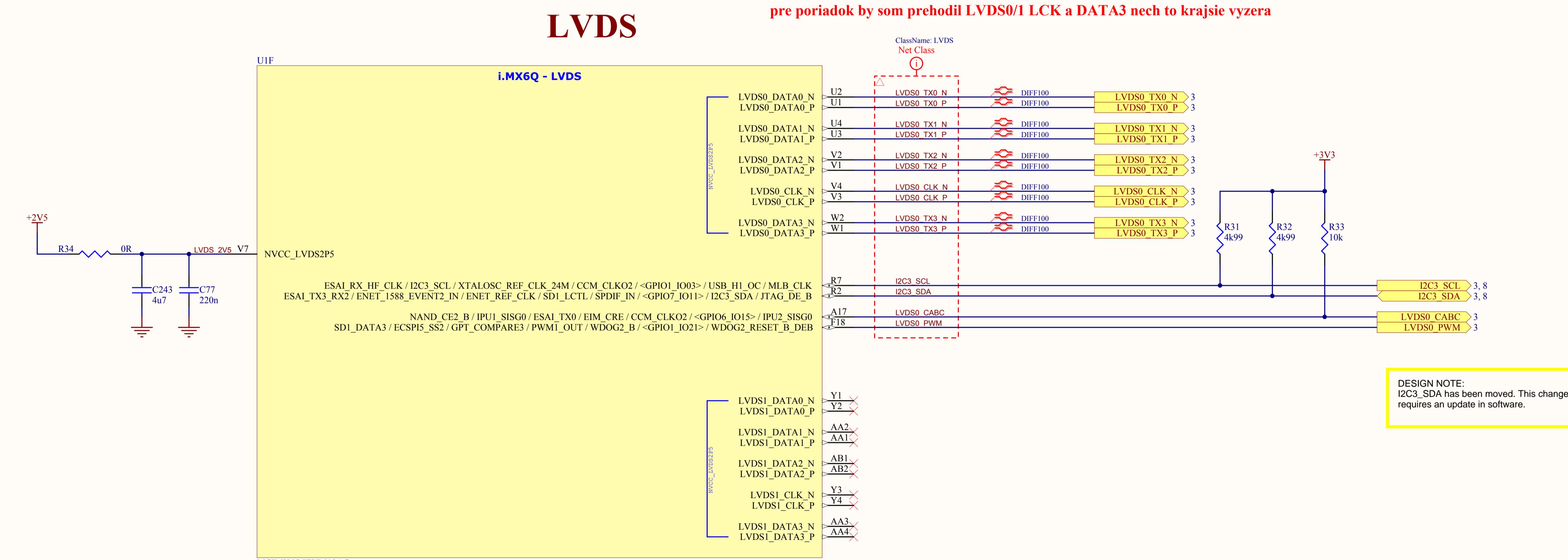
CPU - SATA, PCIe



CPU - HDMI, LVDS



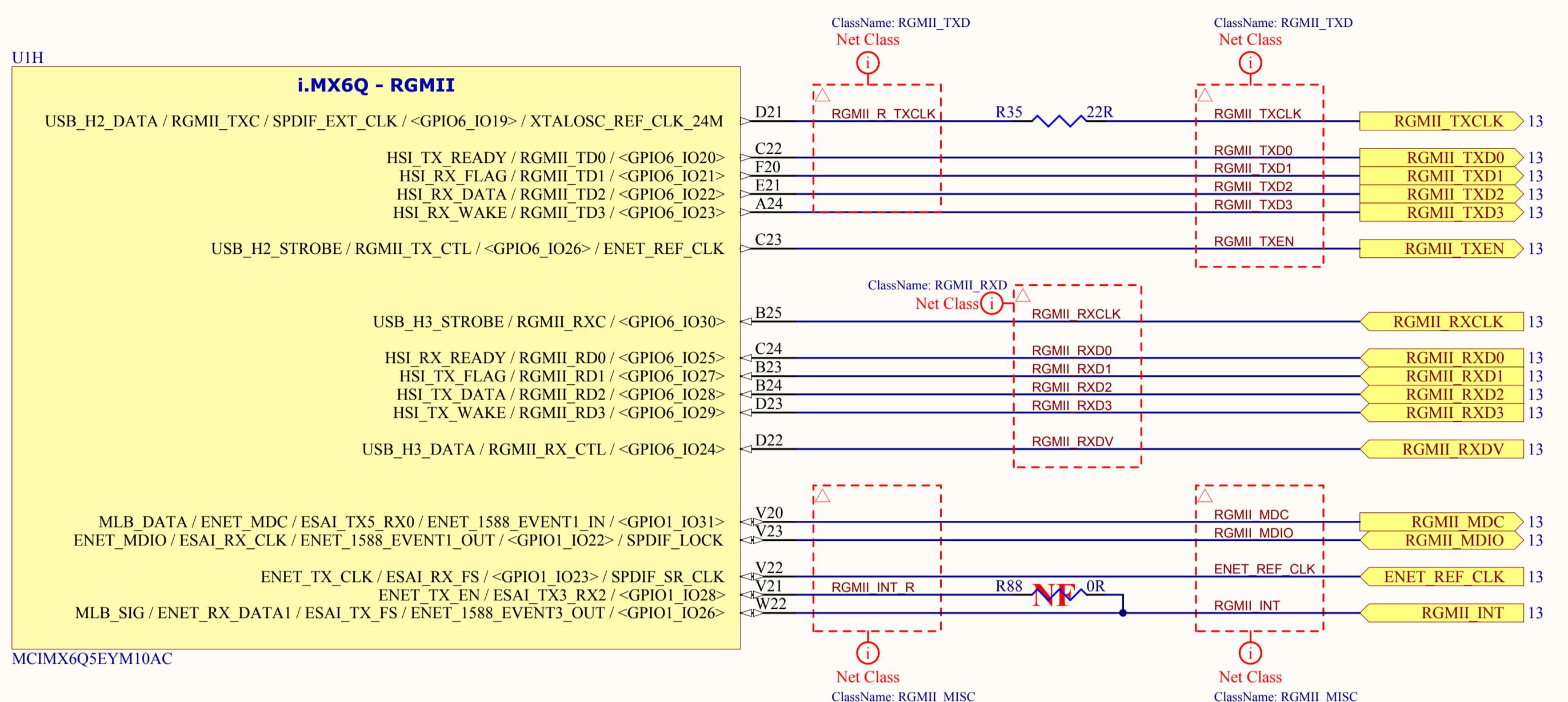
dat poznamku, ze v layout by sme mali mat vacsie capacitory pri R27 a R23, normlane tam vsade maju moznost mat blzko aspon 4u7, preverit ci to tak mame



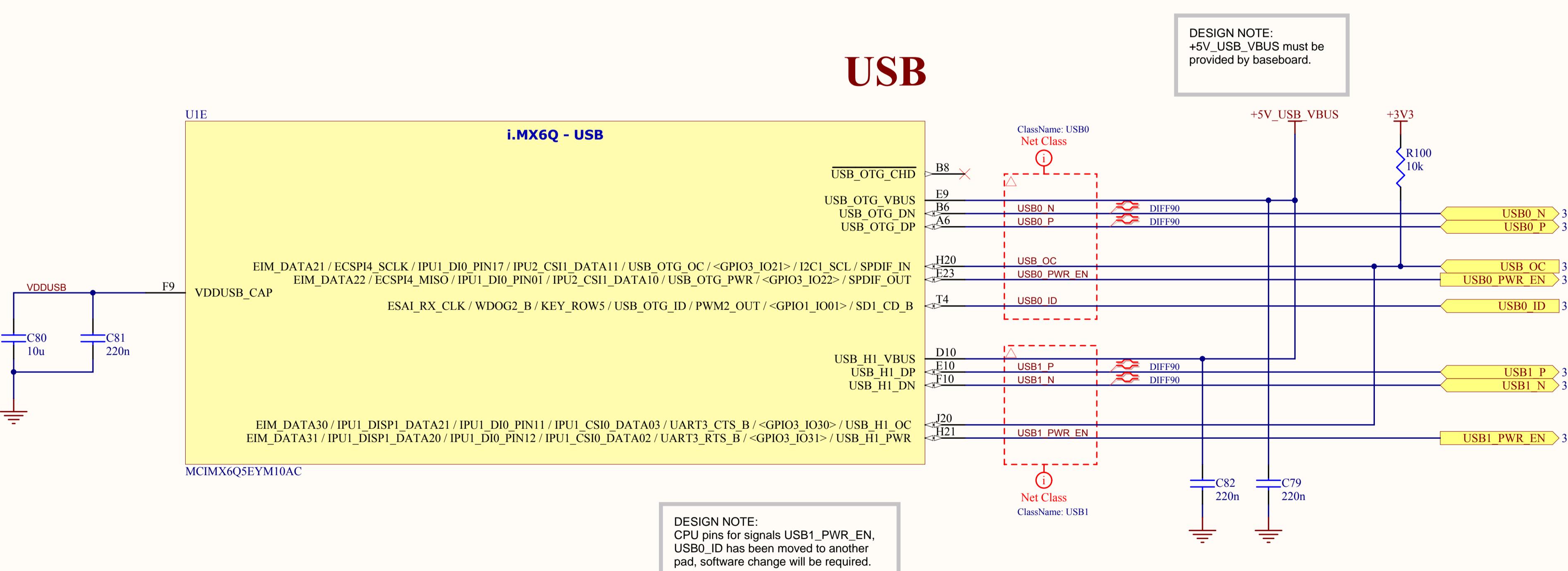
preco napriklad tu ste dali 4u7 na NVCC_LVDS2P5 a na sata a pcie ste nedali?

CPU - USB, ETHERNET

ETHERNET



USB



Vsetky diff mame N navrchu a P dole a USB H1 je naopak
Pridat poznamku, ked USB ID je 0 tak HOST, ked 1 tak DEVICE

dat poznamku, ze +5V_USB_VBUS by malo prist az po +3V3 alebo USB0_PWR_EN alebo USB1_PWR_EN

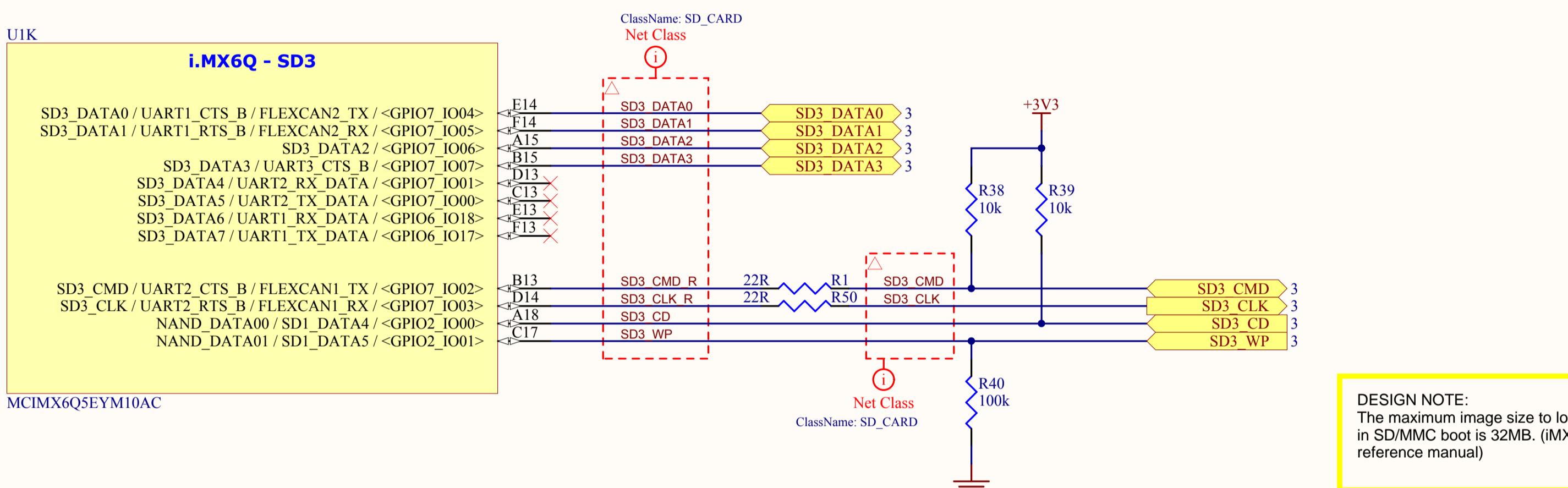
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Title:	iMX6 Rex Module
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CPU - SPI, I2C, SD, MMC

A

A

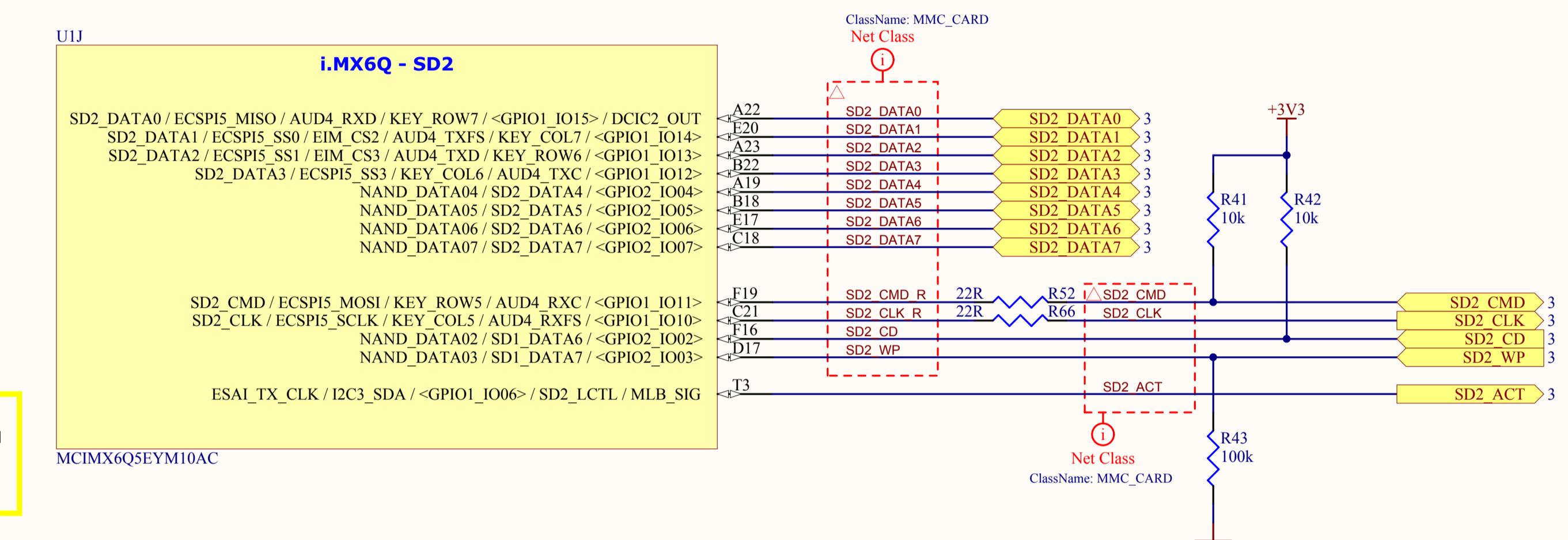
SD-CARD



R40 by som dal ako pull up a na Base board by som dal moznost pripojit na zem 0R (neosadeny)

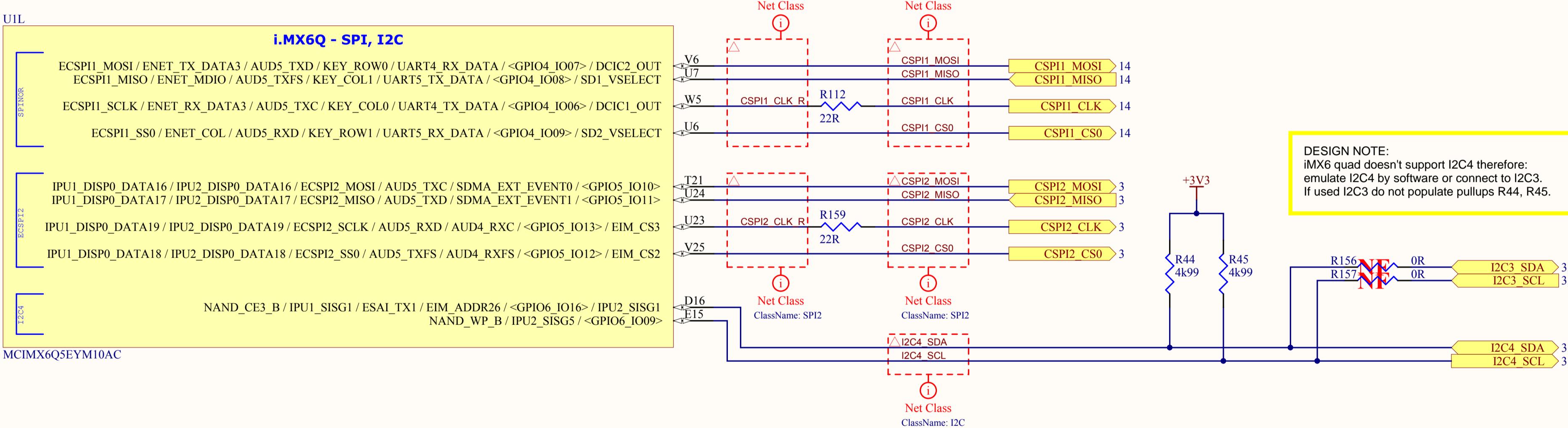
Pridat poznamku: V originalnej ref scheme je SD3 ako 8 bitove, ak bude problem, treba preverit nastavenia

MMC-CARD



R43 by som dal ako pull up a na Base board by som dal moznost pripojit na zem 0R (neosadeny)
pridat poznamku: SD2_ACT musi byt configurovana v softve

SPI FLASH, I2C



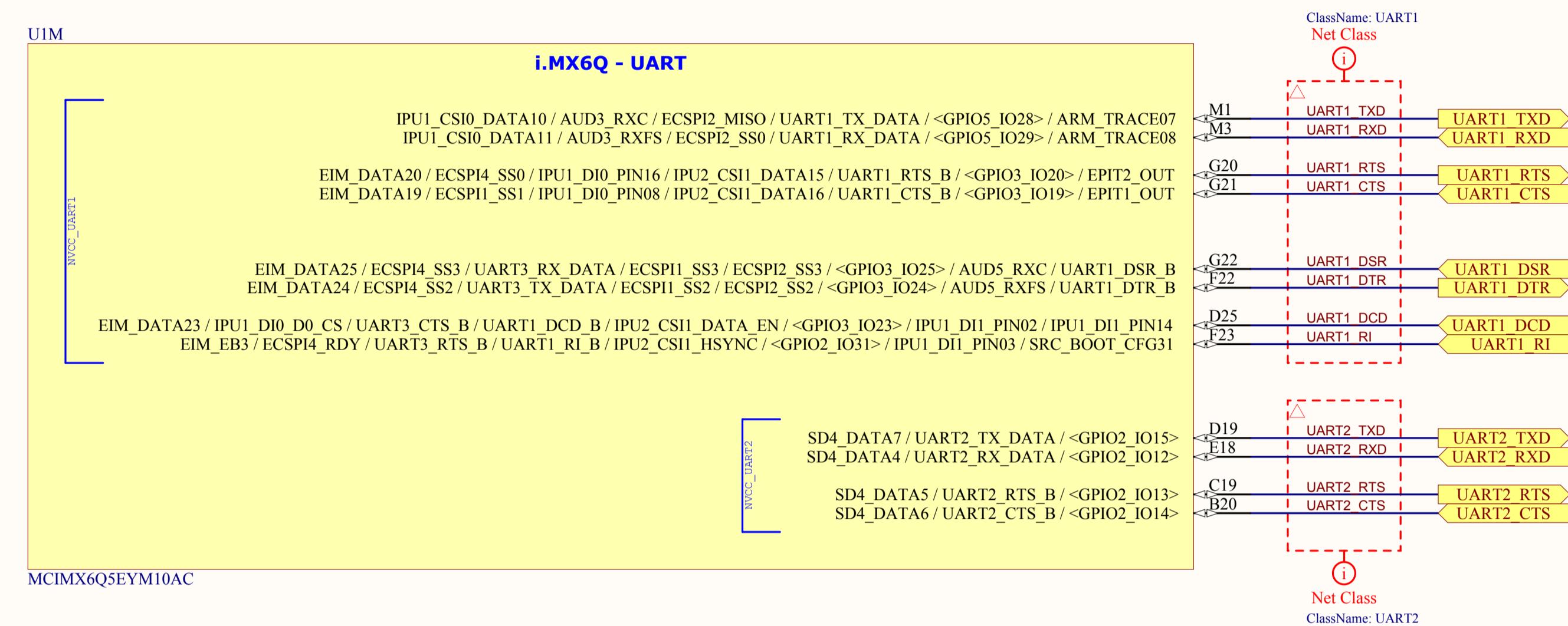
Pridat poznamku, ze I2C nie je default podporovane v softwery, treba nakonfigurovat a dorobit

Pridat poznamku: CSPI2_MOSI treba nastaviti - nie je default

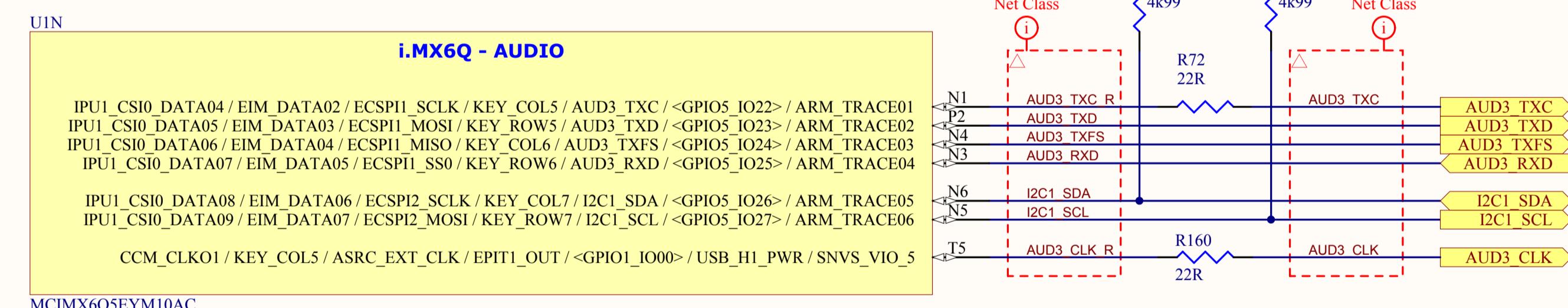
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CPU - UART, AUDIO

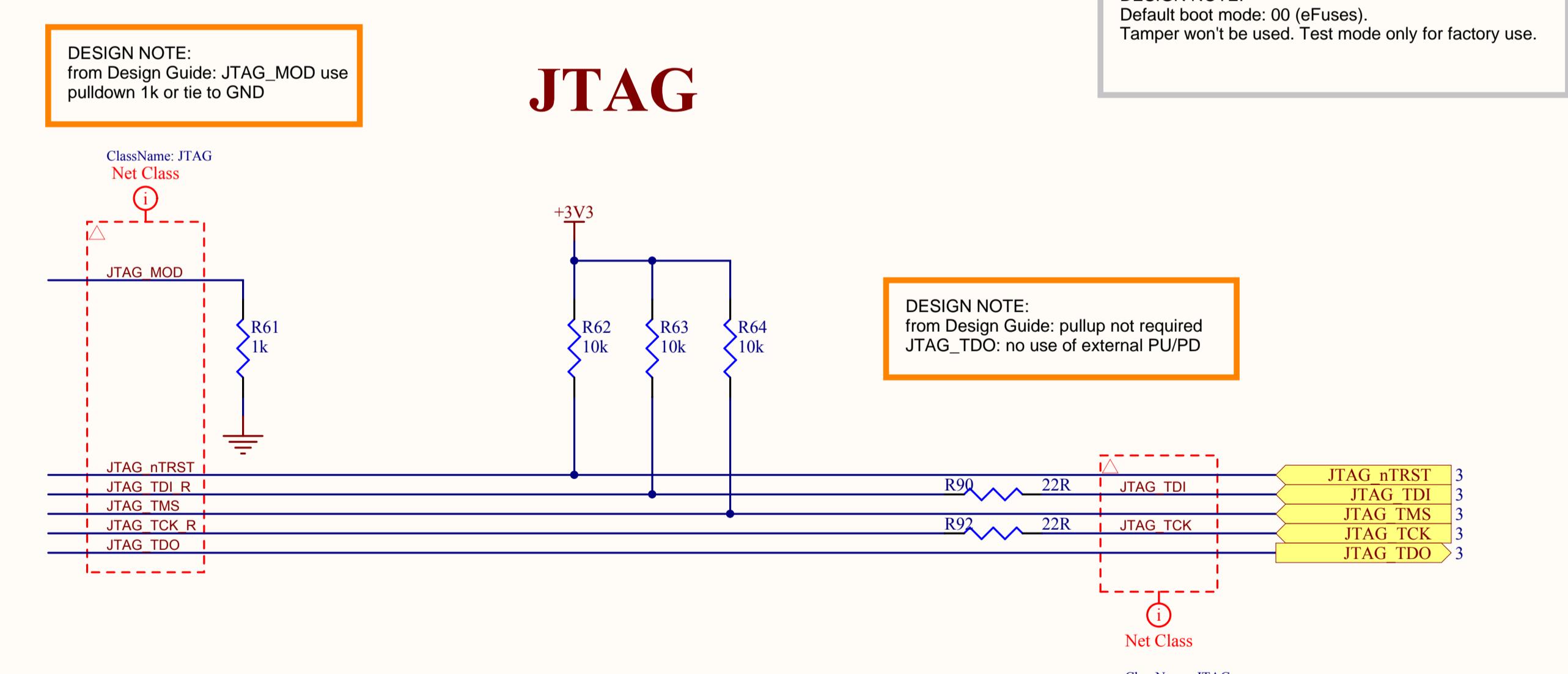
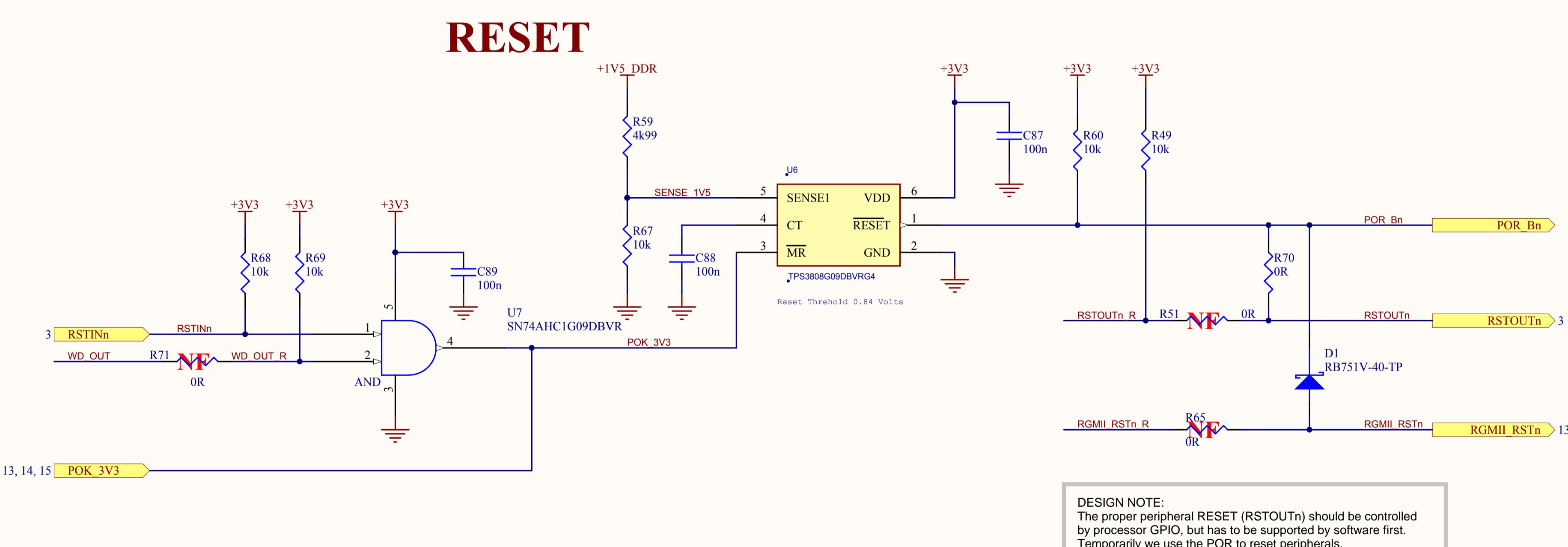
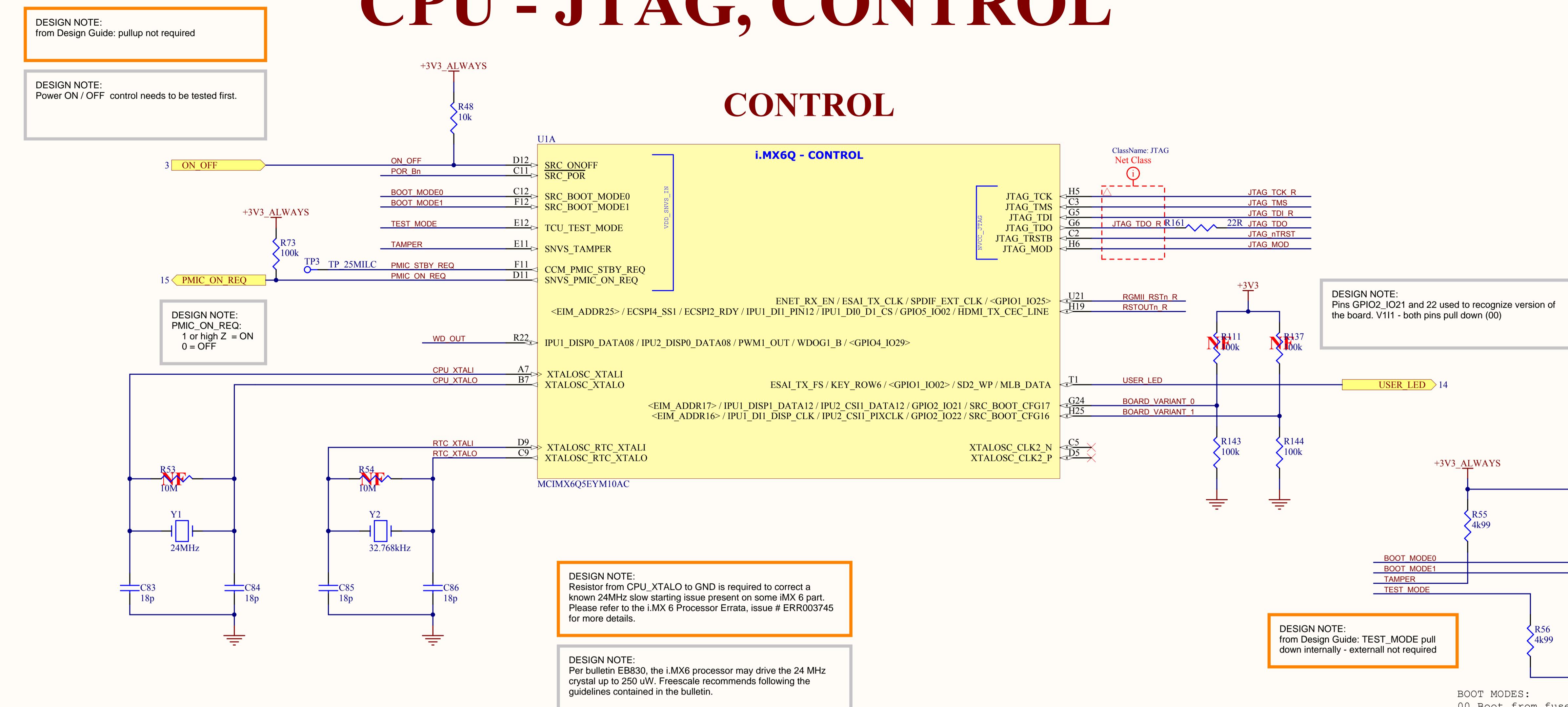
UART



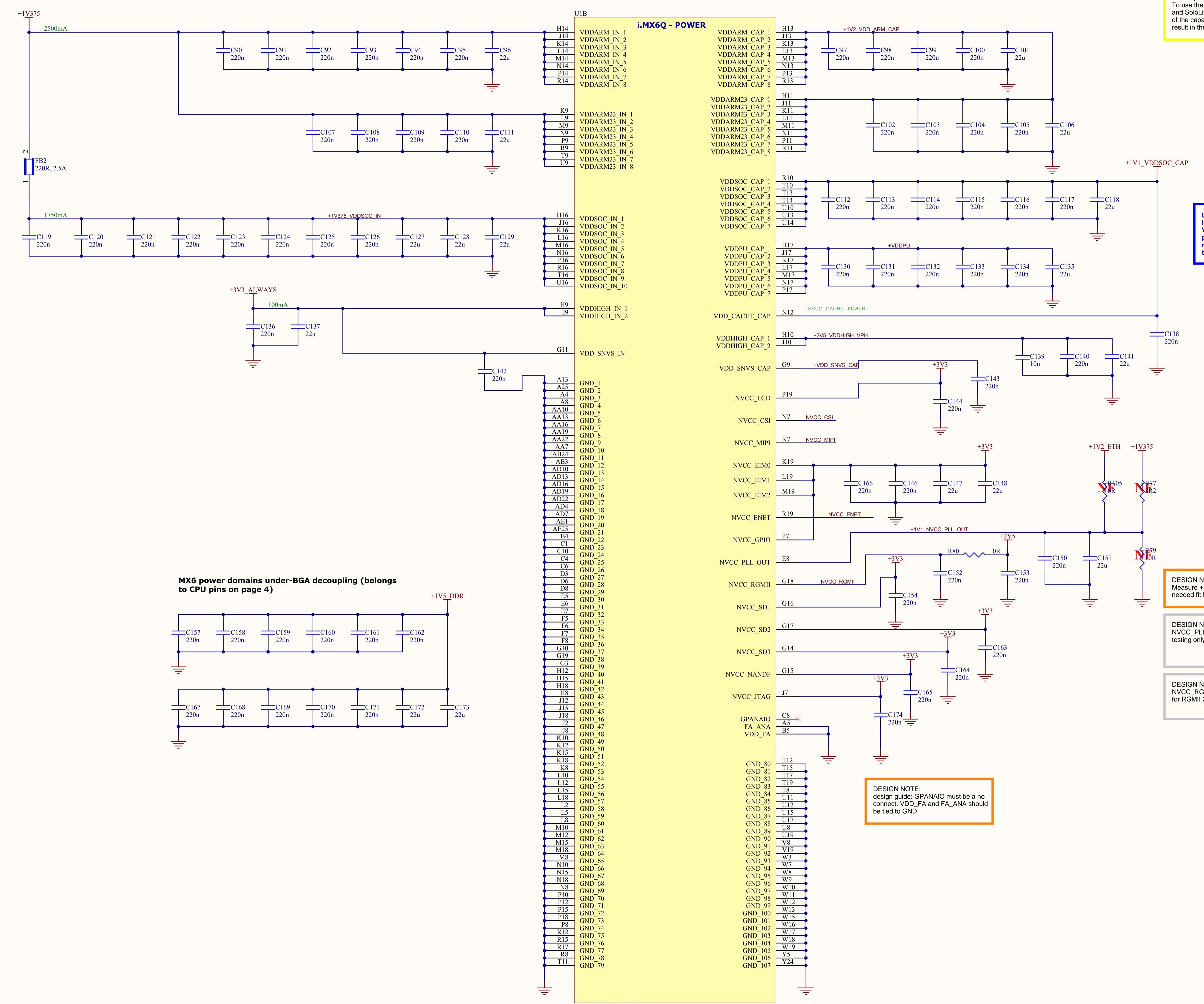
AUDIO



CPU - JTAG, CONTROL



CPU - POWER



DESIGN NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

DESIGN NOTE:
Measure +1V1_NVCC_PLL_OUT, if
needed fit R77, R79.

DESIGN NOTE:
NVCC_PLL_OUT: R77, R79, R105 for
testing only.

DESIGN NOTE:
NVCC_RGMII connected to 2V5

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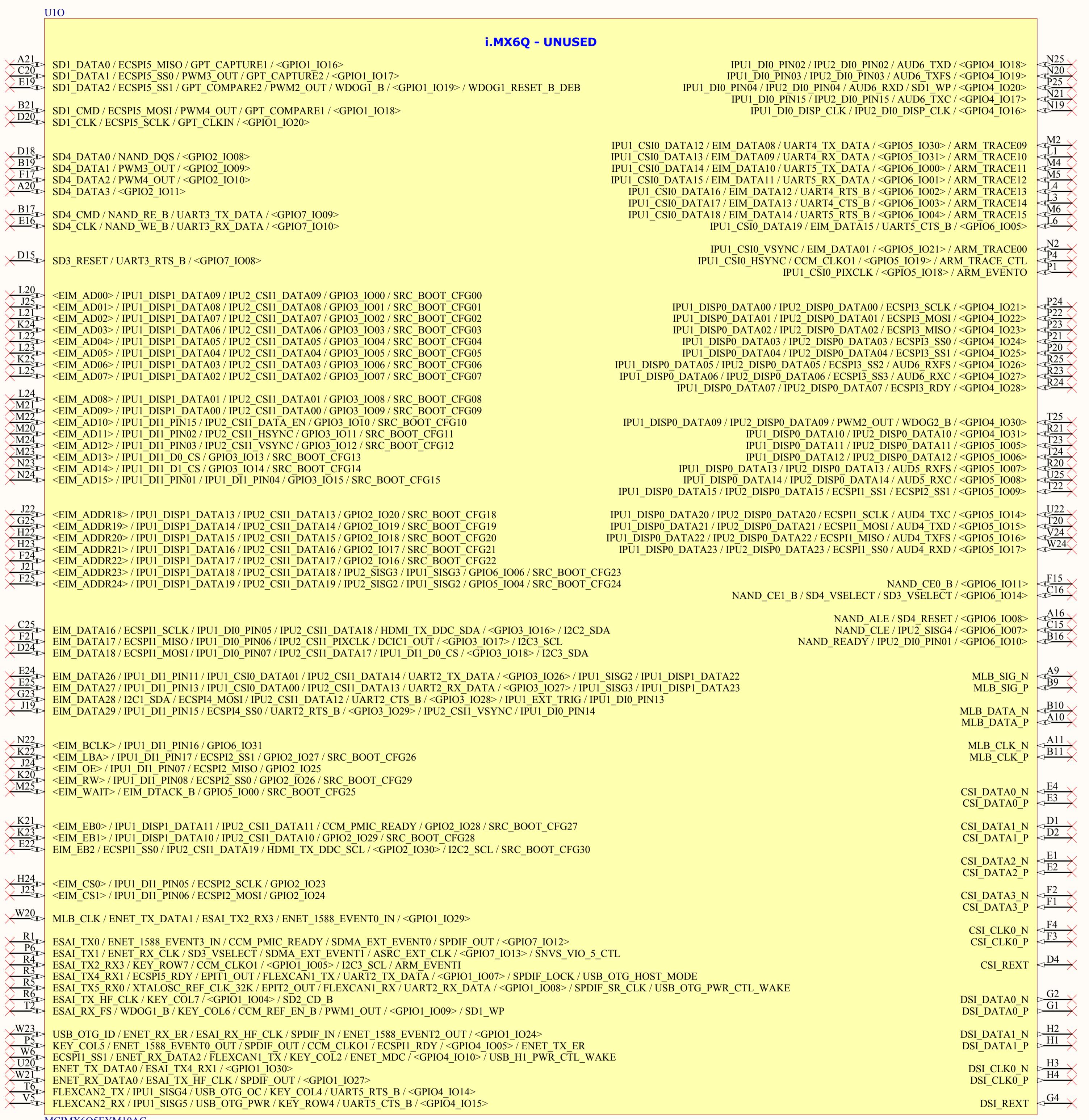
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CPU - UNUSED PINS

A

A



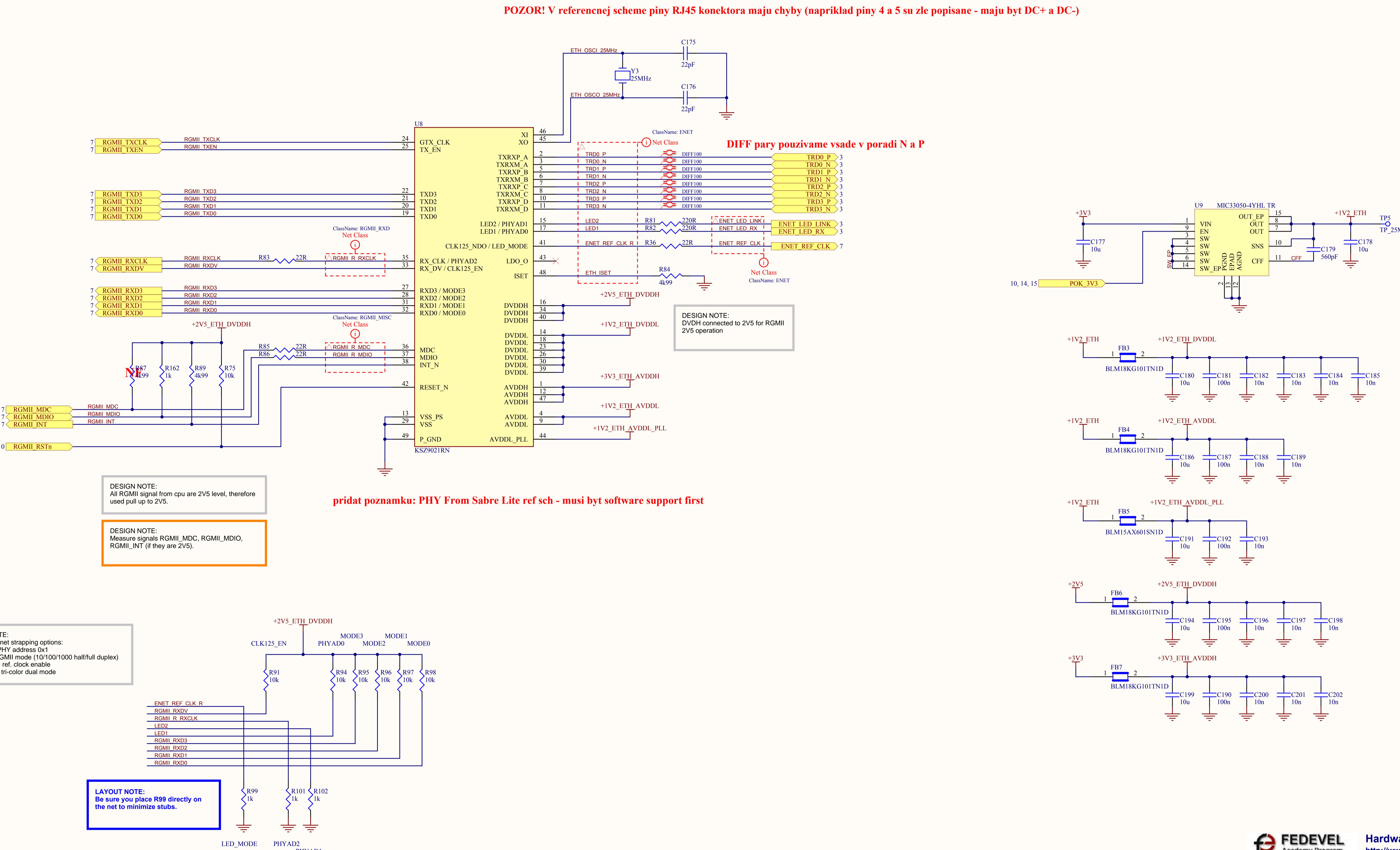
MCIMX6Q5EYM

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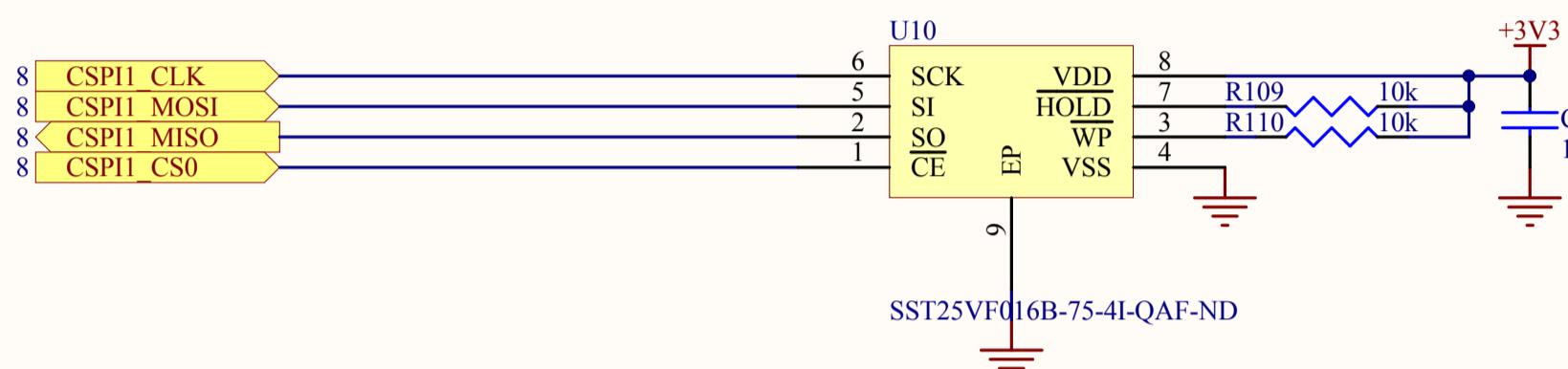
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ETHERNET PHY



SPI FLASH, LED

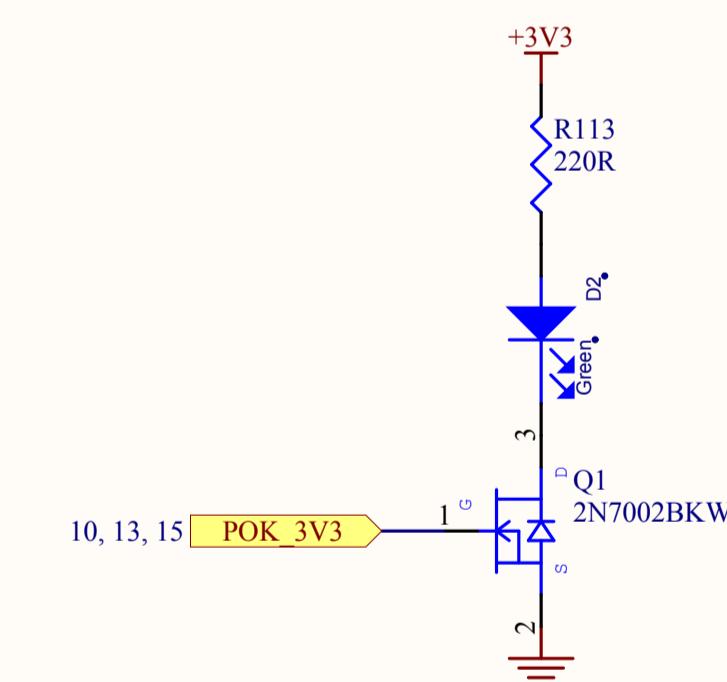
SPI NOR FLASH



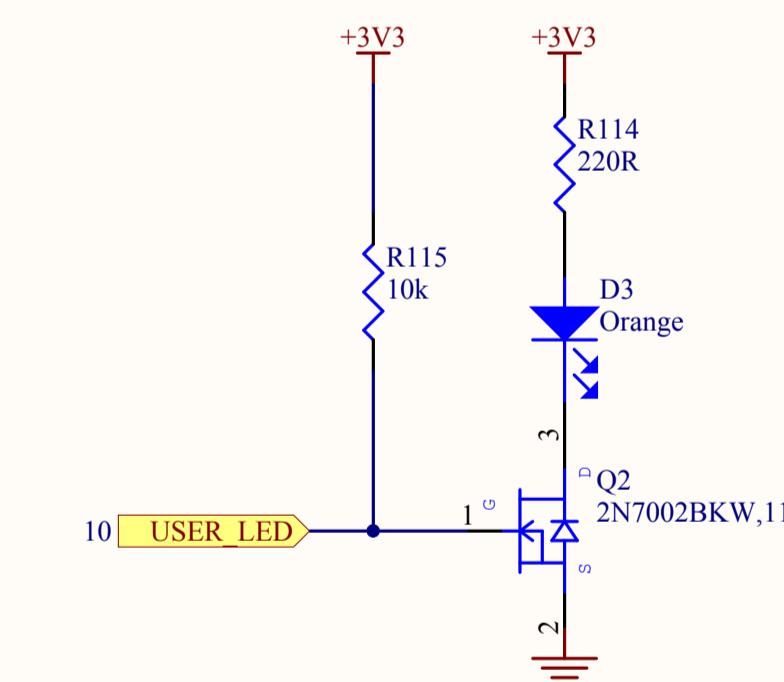
Pridat poznamku: toto je bootovacia flash zo Sabre Lite, ktorá je pripojená na uplné iný SPI PORT!!!!

Poznamka pre mňa: POZOR, vyzera ze oni z tej SPI ani nebootuju?! Odkial sa natiahne bootloader, priam s SD NAND?

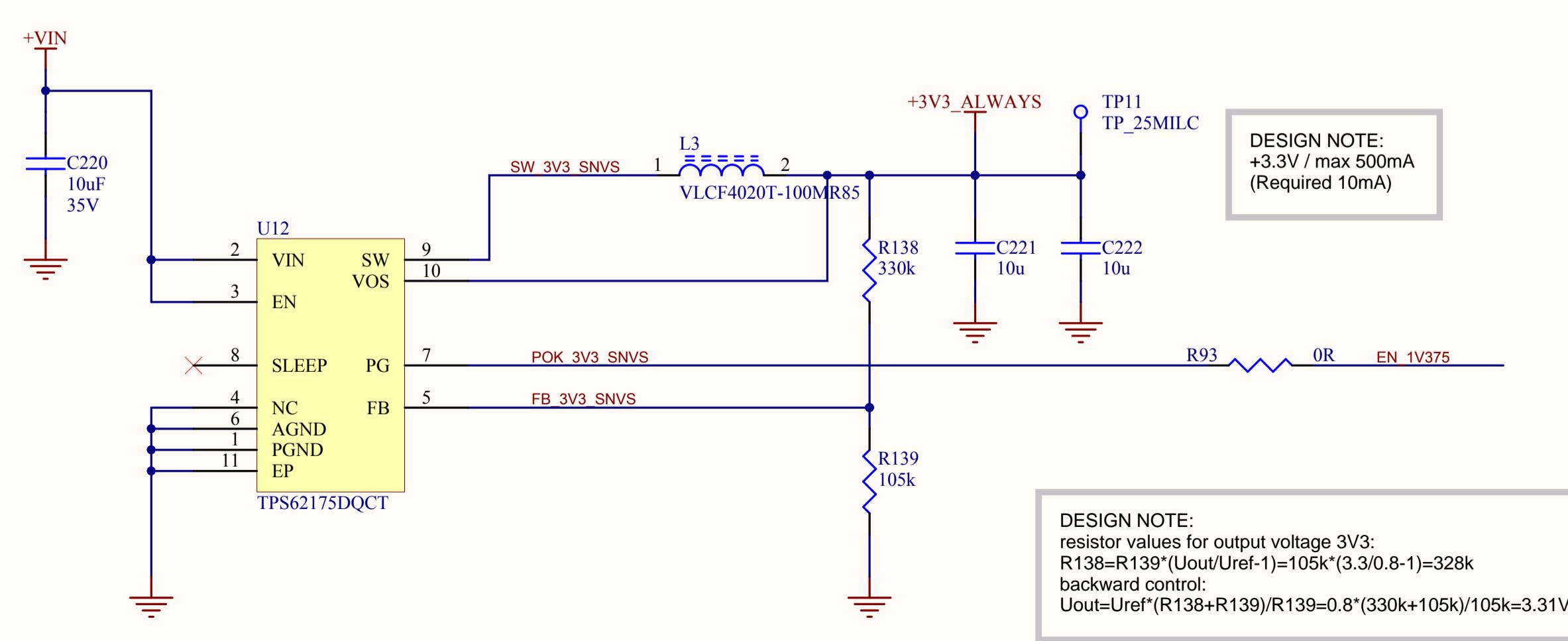
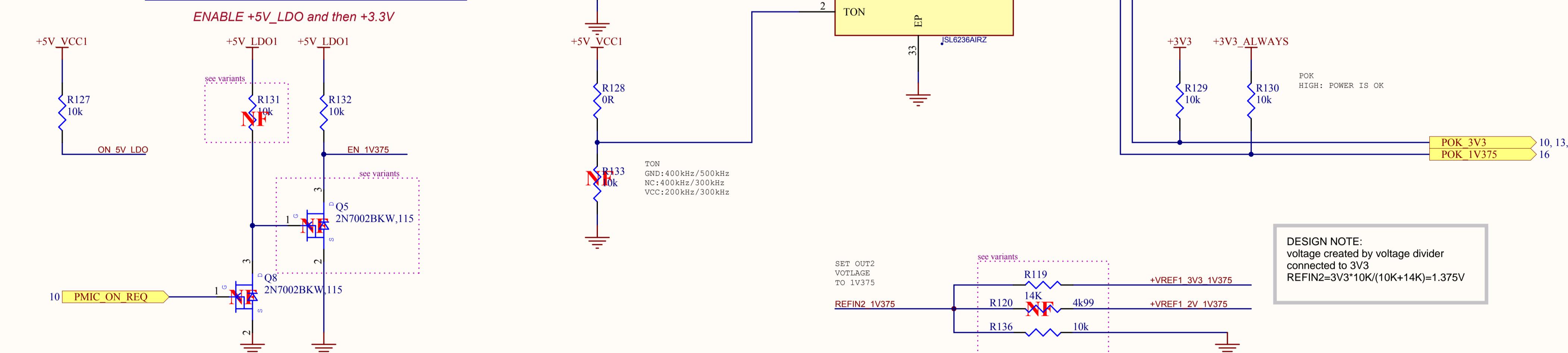
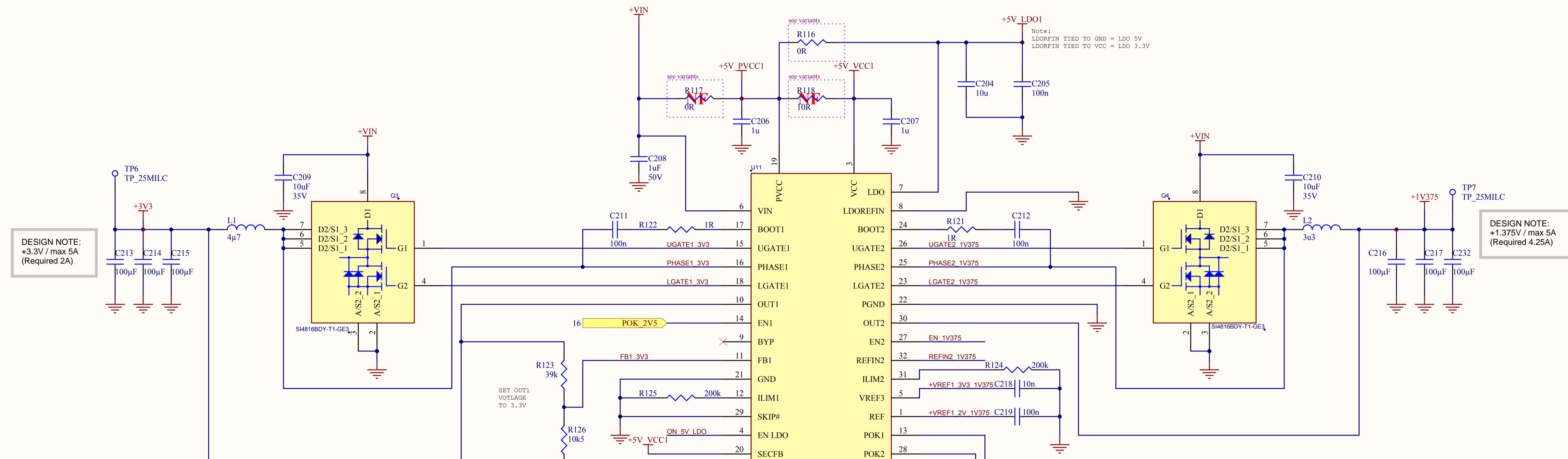
POWER LED



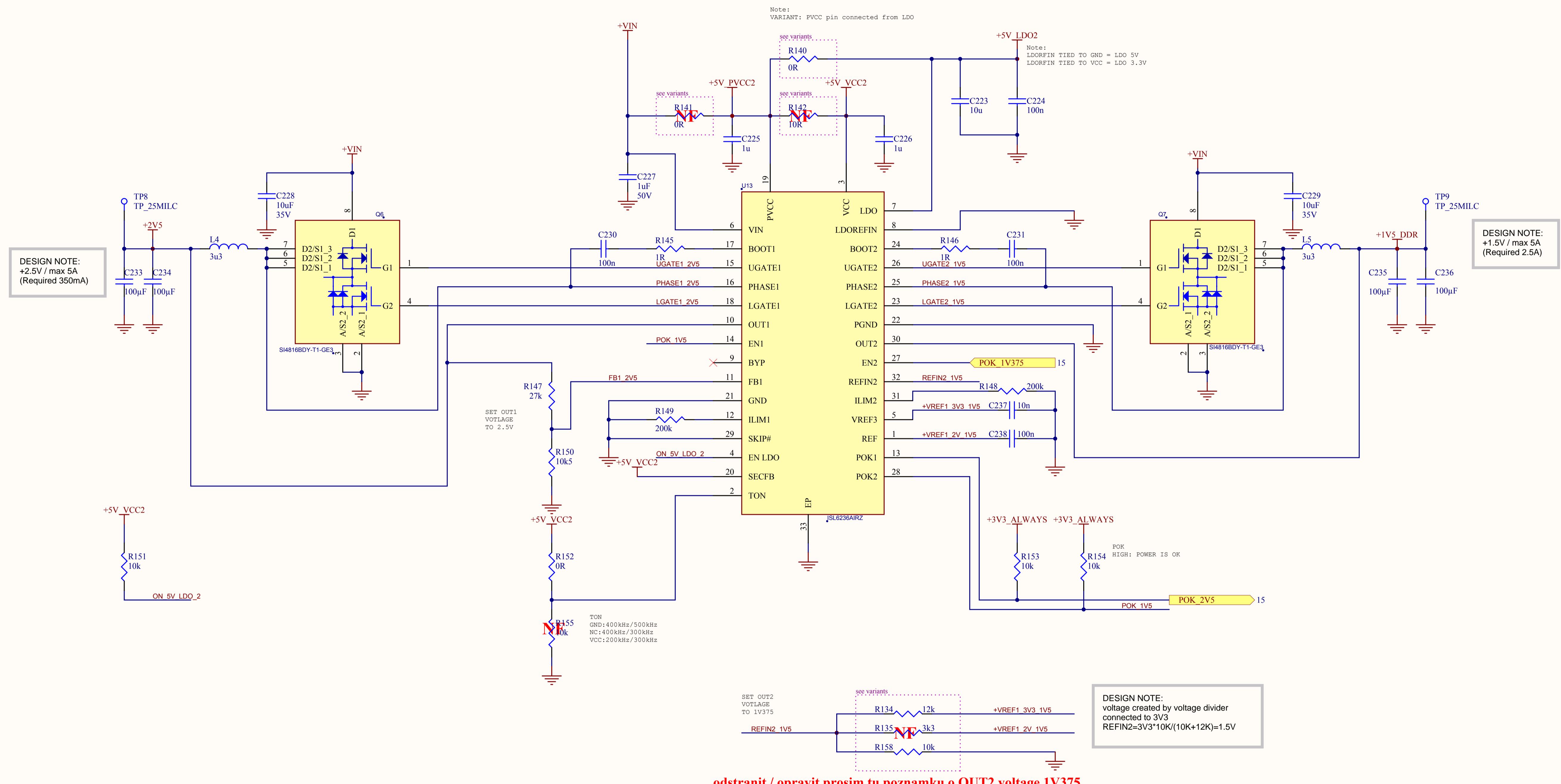
USER DEFINED LED



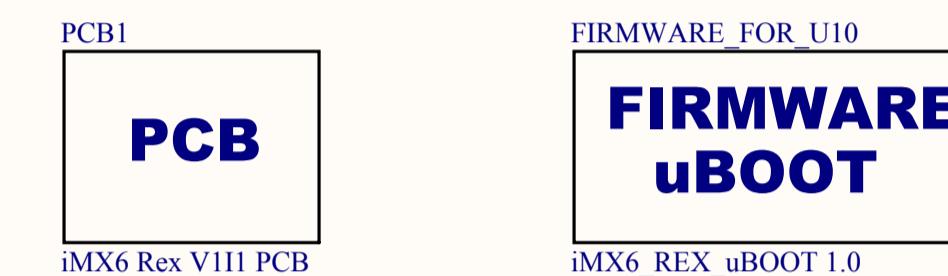
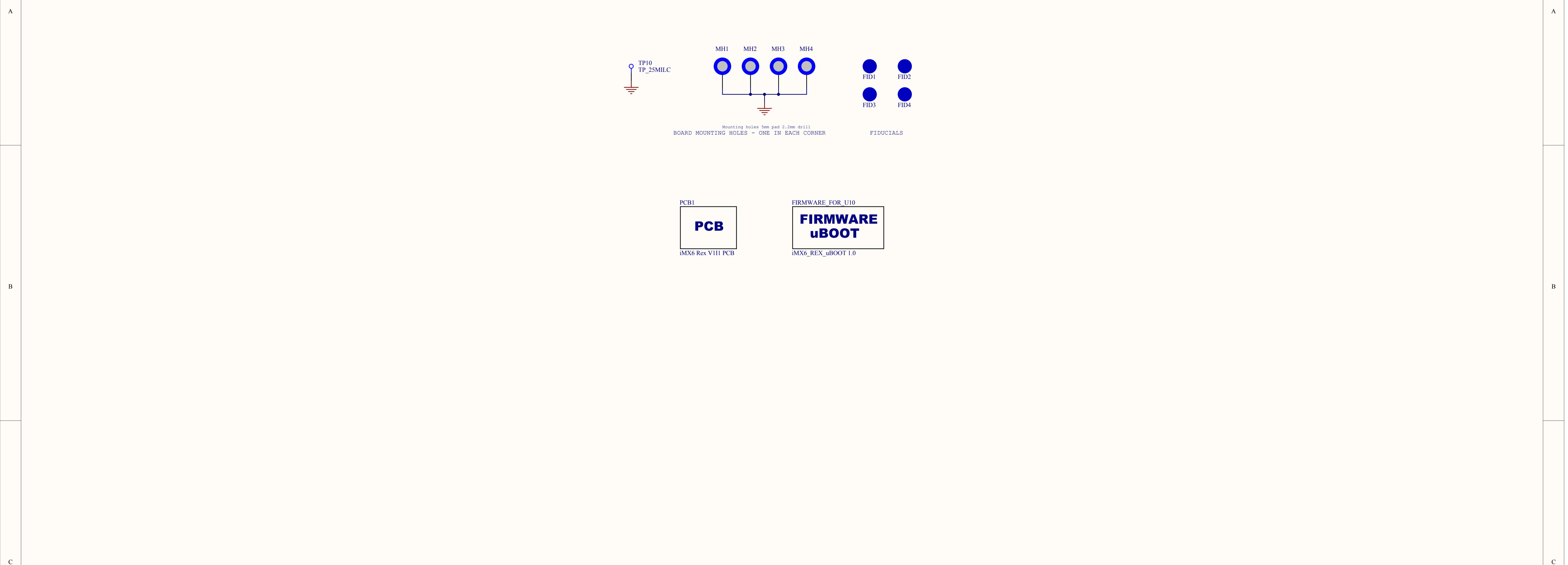
POWER +3.3V, +1.375V CON



POWER +2.5V, +1.5V CON

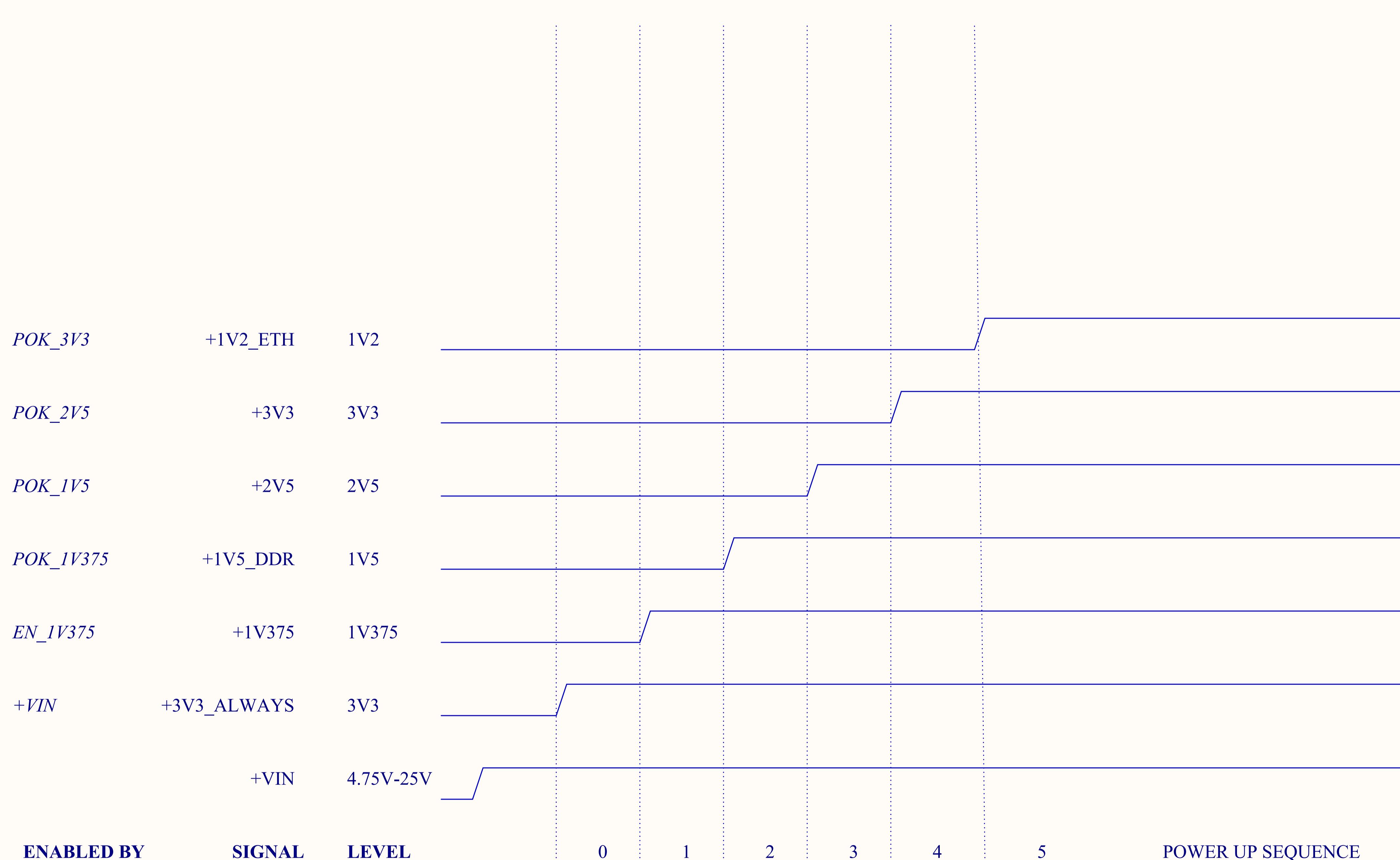


MECHANICAL



CPU - POWER SEQUENCING

+USB_VBUS	5V		
+DDR_VREF	0V75	+1V5_DDR	ref. for DDR memories, gen. with volt. divider
+1V2_VDD_ARM_CAP	1V2	iMX	cpu, core caps
+1V1_VDDSOC_CAP	1V1	iMX	core caps, cpu-sata, cpu-pcie, cpu-hdmi
OTHER USED SIGNAL	LEVEL	GEN BY	SUPPLIED FROM SIGNAL



ENABLED BY **SIGNAL** **LEVEL**

0 1 2 3 4 5 POWER UP SEQUENCE

DOC: REVISION HISTORY

A 01-AUG-2013 Some HDMI and Ethernet signals swapped on J1 A

B

B

C

C

D

D

CLOCKS (CPU & PCIe)



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[01] - COVER PAGE.SchDoc[02] - BLOCK DIAGRAM.SchDoc
[02] - BLOCK DIAGRAM.SchDoc[03] - CONNECTORS.SchDoc
[03] - CONNECTORS.SchDoc[04] - CPU - DDR3, DDR3 MEM.SchDoc
[04] - CPU - DDR3, DDR3 MEM.SchDoc[05] - CPU - PCIE, SATA.SchDoc
[05] - CPU - PCIE, SATA.SchDoc[06] - CPU - HDMI, LVDS.SchDoc
[06] - CPU - HDMI, LVDS.SchDoc[07] - CPU - USB, ETHERNET.SchDoc
[07] - CPU - USB, ETHERNET.SchDoc[08] - CPU - SPI, I2C, SD, MMC.SchDoc
[08] - CPU - SPI, I2C, SD, MMC.SchDoc

TEMPLATE NOTES

Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Company, Project and VersionRevision

Mark Not Fitted Components as
NF

Net Class Example



Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Title

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

[09] - CPU - UART, AUDIO.SchDoc
[09] - CPU - UART, AUDIO.SchDoc[10] - CPU - JTAG, CONTROL.SchDoc
[10] - CPU - JTAG, CONTROL.SchDoc[11] - CPU - POWER.SchDoc
[11] - CPU - POWER.SchDoc[12] - CPU - UNUSED.SchDoc
[12] - CPU - UNUSED.SchDoc[13] - ETHERNET PHY.SchDoc
[13] - ETHERNET PHY.SchDoc[14] - SPI FLASH, LEDS.SchDoc
[14] - SPI FLASH, LEDS.SchDoc[15] - PWR 3V3, 1V375.SchDoc
[15] - PWR 3V3, 1V375.SchDoc[16] - PWR 2V5, 1V5.SchDoc
[16] - PWR 2V5, 1V5.SchDoc[17] - MECH.SchDoc
[17] - MECH.SchDoc[18] - POWER SEQUENCING.SchDoc
[18] - POWER SEQUENCING.SchDoc[19] - DOC REVISION HISTORY.SchDoc
[19] - DOC REVISION HISTORY.SchDoc

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