IBIS Models
Correlation Report

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1.0 Introduction

This document demonstrates correlation between randomly selected Cyclone IV IBIS Models with HSPICE Models to prove the validity of the generated IBIS Models. The selection of models covers all the single-ended and differential I/O standards with a balanced mix of drive strength setting, row and column locations together with slew rate option.
The Cyclone IV IBIS and HSPICE Models for selected I/O standard are simulated based on the setup as shown in Figure 1-1. The simulation setup includes the **output buffer model,** passing through the **RLC package model**, followed by a standard **transmission line model** (simple and lossless) then to the receiver's **RLC package model** and finally into an **input buffer**. The package model used in the correlation setup is the lumped RLC package model with mutual coupling effect for both the inductance and capacitance.

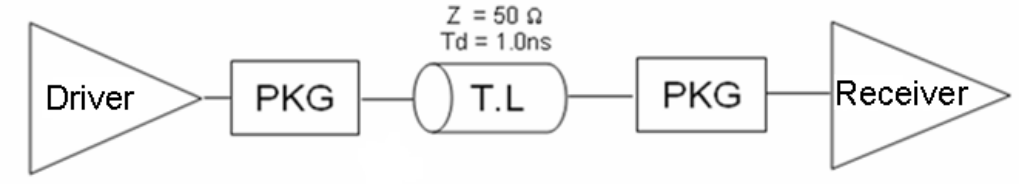

Figure 1-1. The Correlation Setup

Appropriate termination scheme is used for each I/O standard. Please refer to "*Chapter 6. I/O Features in Cyclone IV Devices*", Termination Scheme for I/O Standards section for the recommended and proper termination scheme.

The figures and tables in this document show the correlation between the IBIS Model and HSPICE Model for each I/O standard. It includes a diagram for termination scheme, an IBIS simulation plot, a HSPICE simulation plot and a table that compares the result between the IBIS simulation and HSPICE simulation in terms of rise time (t_r), fall time (t_f) of the models.

The rise and fall time measurement is from 10% to 90% in both HSPICE simulation and IBIS simulation, for all single-ended and differential standards (with or without on-chip termination). All models are simulated at the frequency of 100MHz and all measurements are taken at the point on the driver after the package model, as indicated as TX below. A common HSPICE input model is used while verifying the IBIS output model. For input buffer verification, the measurement is taken at the receiver point as indicated as RX below. A common HSPICE output buffer is used instead while verifying the IBIS input model. Please refer to each section of the verification for detail setup.

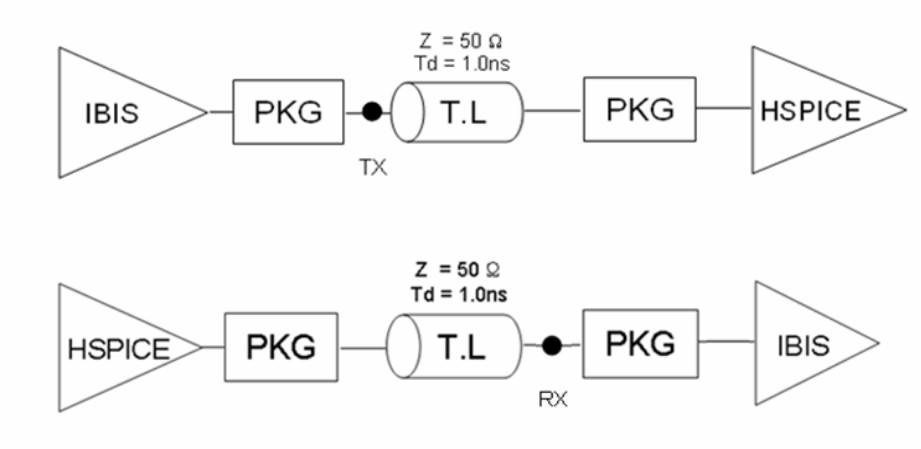

Figure 1-2. Measurement is taken at point TX and RX for both IBIS Driver and Receiver

In the simulations, the output node of the driver is indicated as YELLOW whereas the input receiver end is shown as RED.

2.0 HSTL Verification

Following shows the correlation between IBIS simulation and HSPICE simulation for 1.5V HSTL and 1.8V HSTL for Class I and Class II standard.

2.1 1.5V HSTL Class I Verification

Figure 2-1 and 2-2 shows the simulation setup for 1.5V HSTL Class I IBIS output model and HSPICE output model.

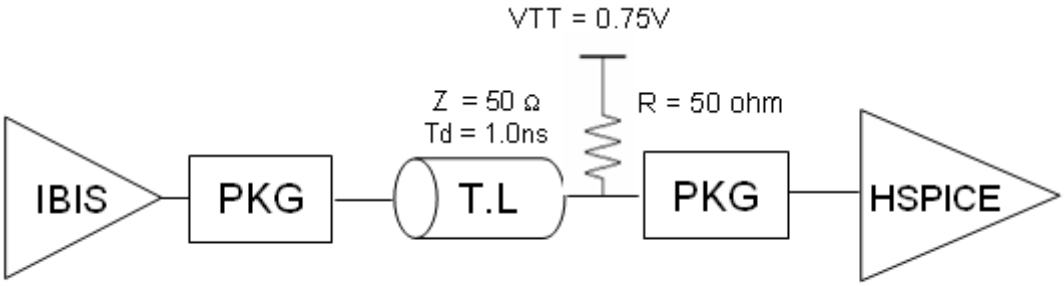

Figure 2-1. 1.5V HSTL Class I IBIS Model Simulation Setup

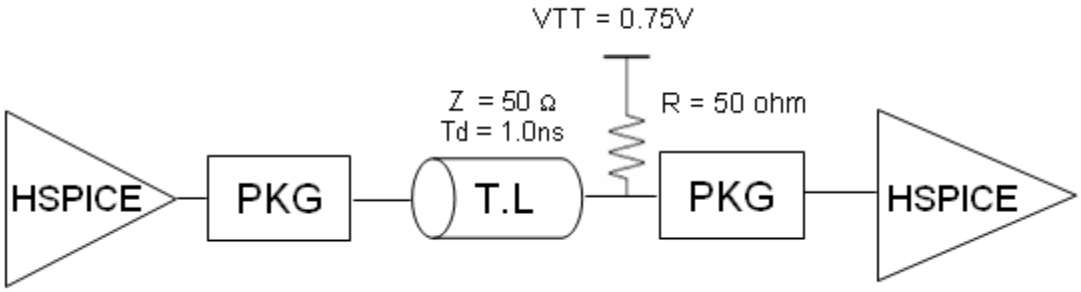

Figure 2-2. 1.5V HSTL Class I HSPICE Model Simulation Setup

2.1.1 Row I/O – 10ma Drive Strength with Medium Slew Rate, Fast Conditions

Figures 2-3 and 2-4 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 2-1 shows comparison between the two measurements.

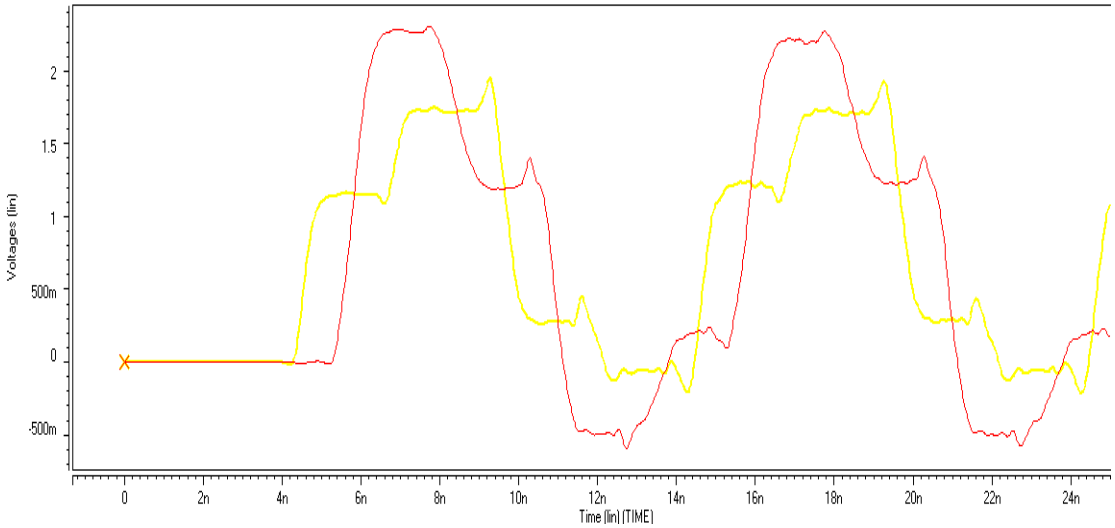

Figure 2-3. 1.5V HSTL Class I (Row I/O, 10mA Drive Strength, Medium Slew Rate) IBIS Model Simulation Result at Fast Conditions.

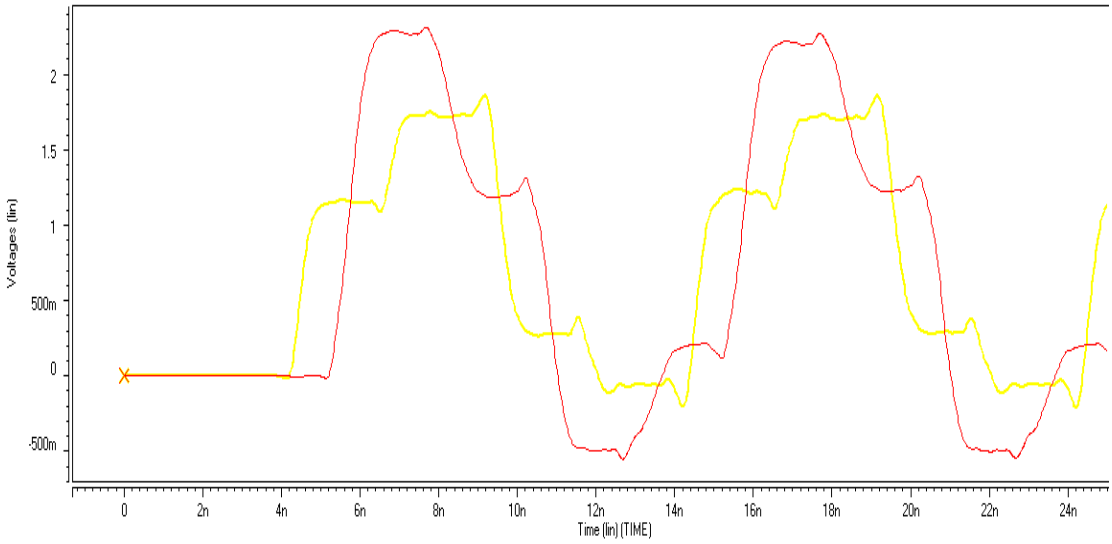

Figure 2-4. 1.5V HSTL Class I (Row I/O, 10mA Drive Strength, Medium Slew Rate) HSPICE Model Simulation Result at Fast Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.52	2.50	0.8
Fall time	2.43	2.41	0.8

Table 2-1 1.5V HSTL Class I (Row I/O, 10mA Drive Strength, Medium Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Fast Conditions

2.2 1.5V HSTL Class II Verification

Figure 2-5 and 2-6 shows the simulation setup for 1.5V HSTL Class II IBIS output model and HSPICE output model.

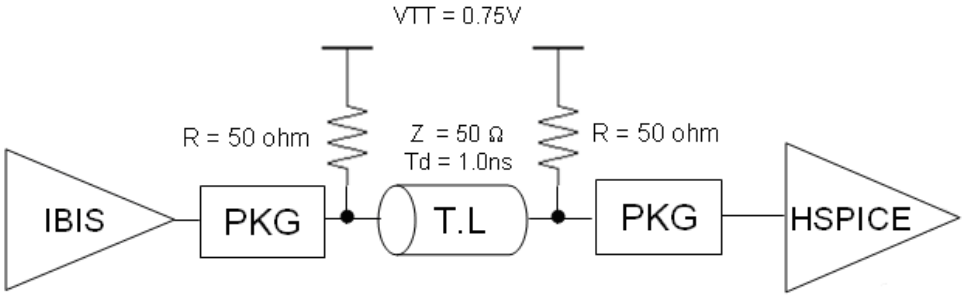

Figure 2-5. 1.5V HSTL Class II IBIS Model Simulation Setup

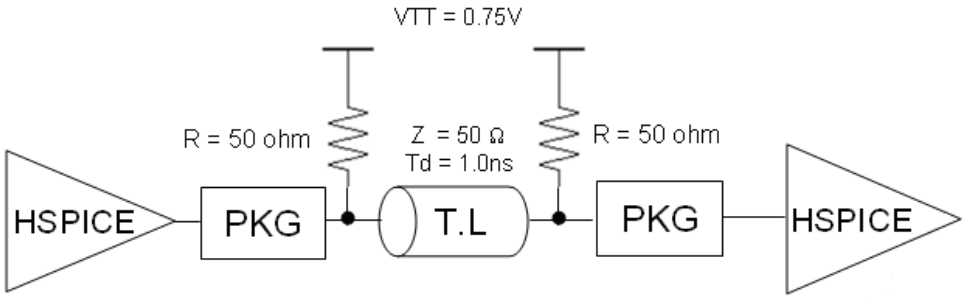

Figure 2-6. 1.5V HSTL Class II HSPICE Model Simulation Setup

2.2.1 Row I/O – 16ma Drive Strength with Fast Slew Rate, Typical Conditions

Figures 2-7 and 2-8 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 2-2 shows comparison between the two measurements.

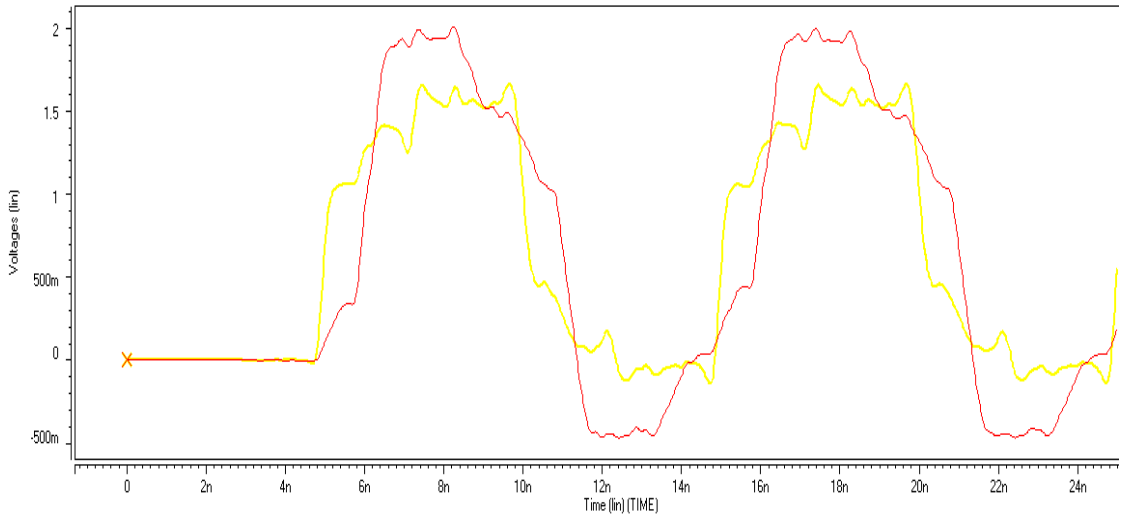

Figure 2-7. 1.5V HSTL Class II (Row I/O, 16mA Drive Strength, Fast Slew Rate) IBIS Model Simulation Result at Typical Conditions

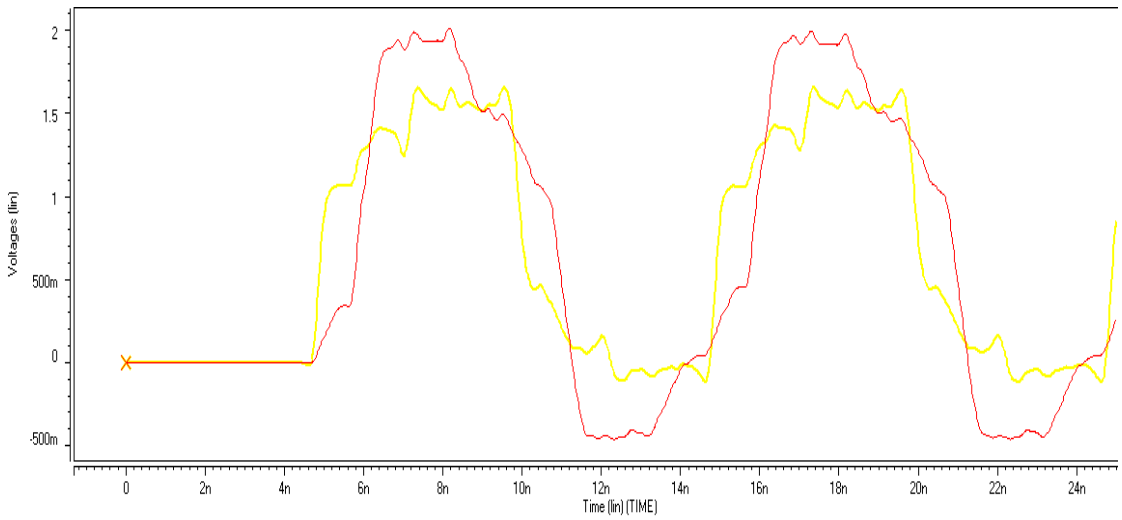

Figure 2-8. 1.5V HSTL Class II (Row I/O, 16mA Drive Strength, Fast Slew Rate) HSPICE Model Simulation Result at Typical Conditions

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	1.57	1.57	0.0
Fall time	1.32	1.33	0.8

Table 2.2. 1.5V HSTL Class II (Row I/O, 16mA Drive Strength, Fast Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

2.3 1.8V HSTL Class I Verification

Figure 2-9 and 2-10 shows the simulation setup for 1.8V HSTL Class I IBIS output model and HSPICE output model.

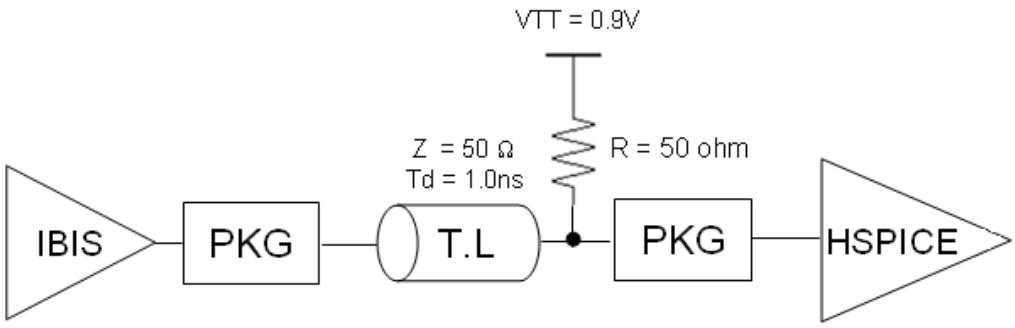

Figure 2-9. 1.8V HSTL Class I IBIS Model Simulation Setup

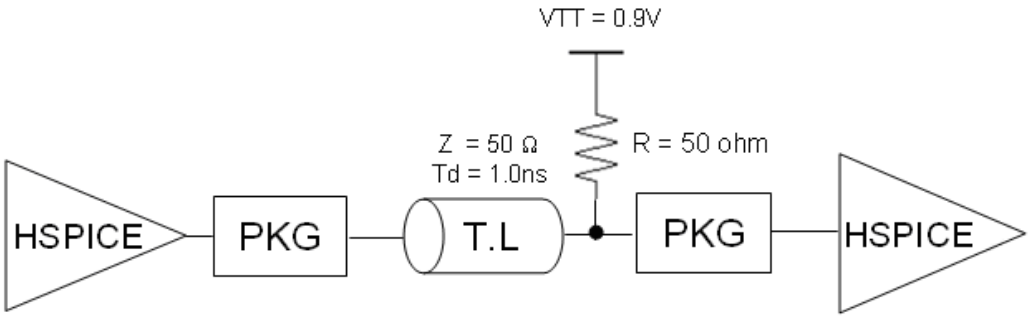

Figure 2-10. 1.8V HSTL Class I HSPICE Model Simulation Setup

2.3.1 Column I/O – 8ma Drive Strength with Slow Slew Rate, Typical Conditions

Figures 2-11 and 2-12 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 2-3 shows comparison between the two measurements.

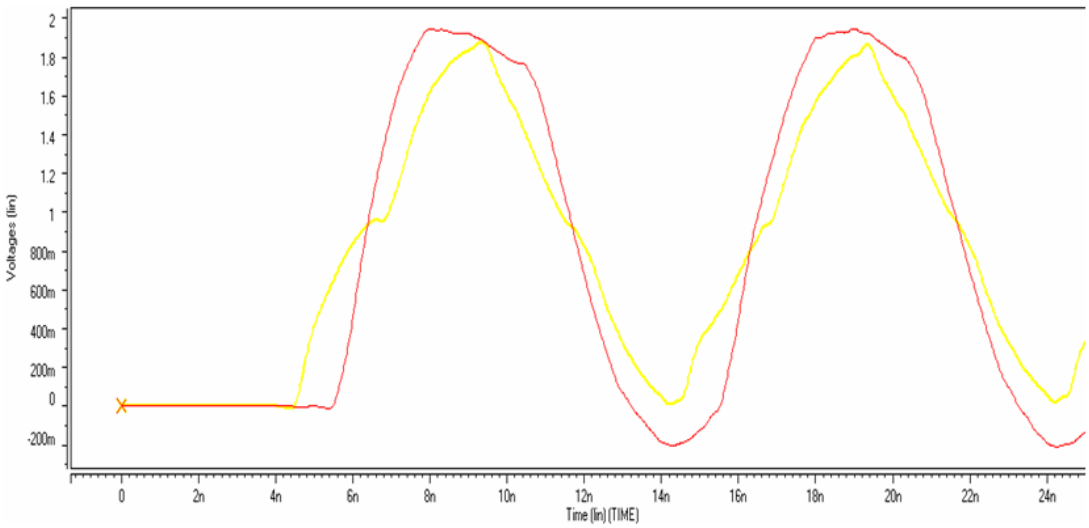

Figure 2-11. 1.8V HSTL Class I (Column I/O, 8mA Drive Strength, Slow Slew Rate) IBIS Model Simulation Result at Typical Conditions.

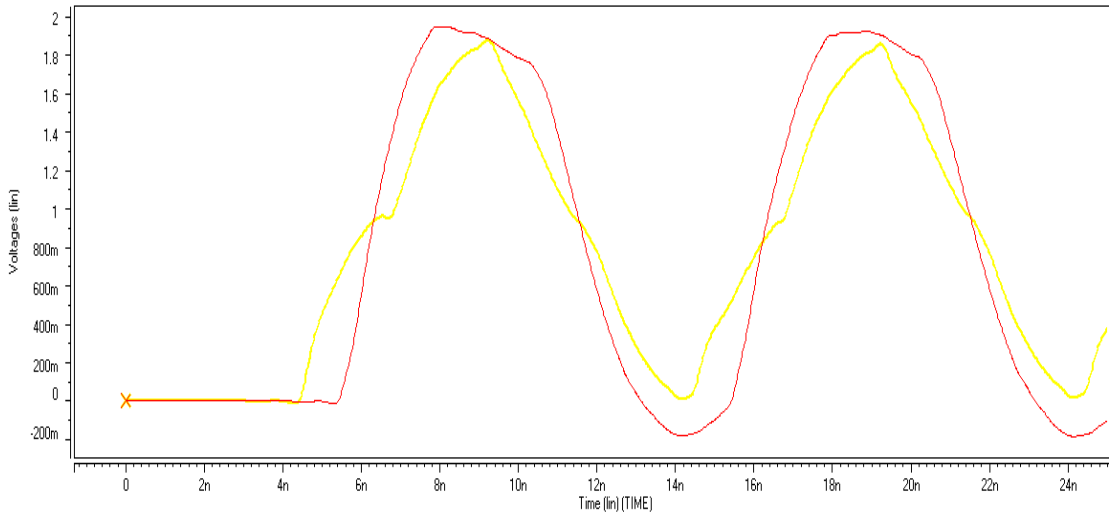

Figure 2-12. 1.8V HSTL Class I (Column I/O, 8mA Drive Strength, Slow Slew Rate) HSPICE Model Simulation Result at Typical Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	3.31	3.32	0.3
Fall time	3.48	3.48	0.0

Table 2-3 1.8V HSTL Class I (Column I/O, 8mA Drive Strength, Slow Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

2.3.2 Row I/O DIFFIO pin (Optional Pin Function) – 12ma Drive Strength with Fast Slew Rate, Slow Conditions

Figures 2-13 and 2-14 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 2-4 shows comparison between the two measurements.

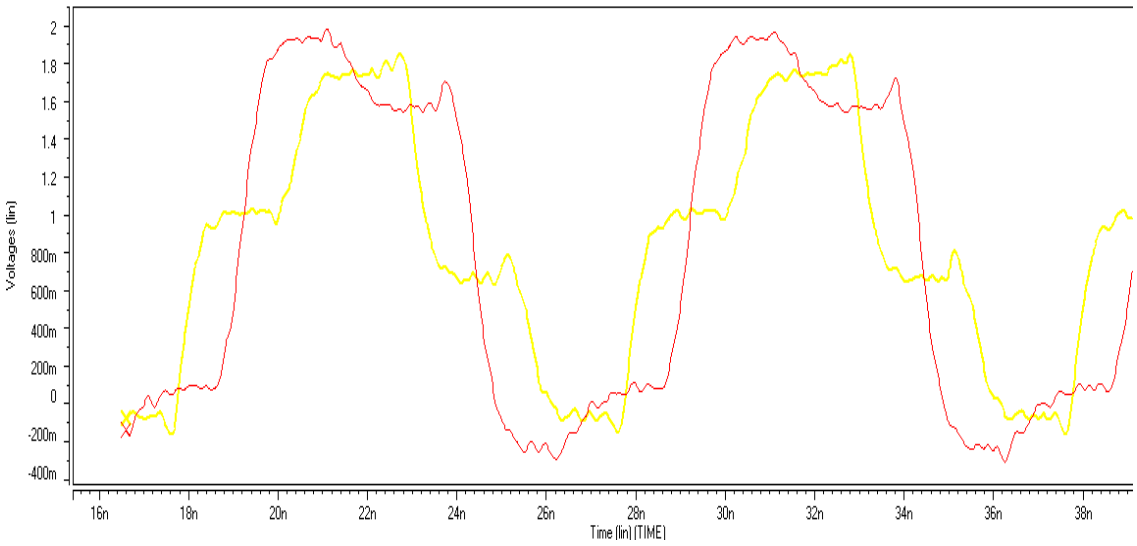

Figure 2-13. 1.8V HSTL Class I (Row I/O DIFFIO pin (Optional Pin Function), 12mA Drive Strength, Fast Slew Rate) IBIS Model Simulation Result at Slow Conditions.

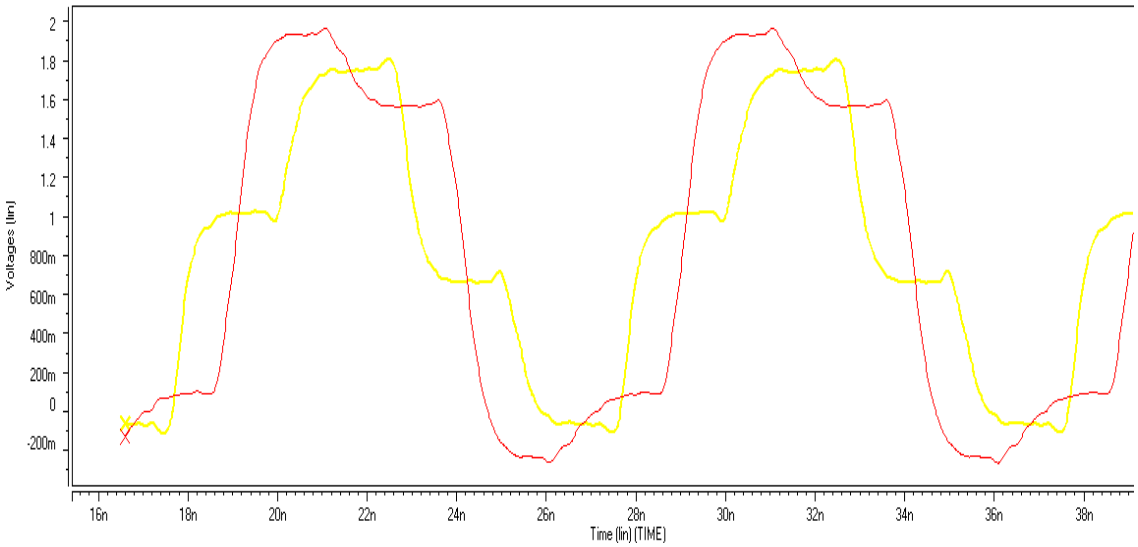

Figure 2-14. 1.8V HSTL Class I (Row I/O DIFFIO pin (Optional Pin Function), 12mA Drive Strength, Fast Slew Rate) HSPICE Model Simulation Result at Slow Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.81	2.78	1.1
Fall time	2.82	2.80	0.7

Table 2-4 1.8V HSTL Class I (Row I/O DIFFIO pin (Optional Pin Function), 12mA Drive Strength, Fast Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

2.4 1.8V HSTL Class II Verification

Figure 2-15 and 2-16 shows the simulation setup for 1.8V HSTL Class II IBIS output model and HSPICE output model.

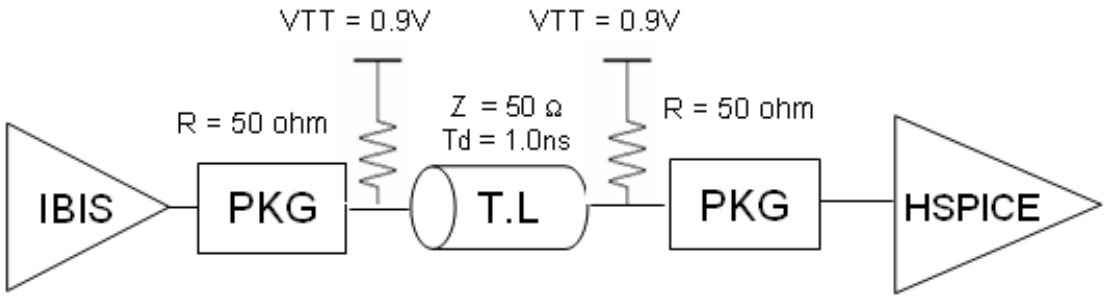

Figure 2-15. 1.8V HSTL Class II IBIS Model Simulation Setup

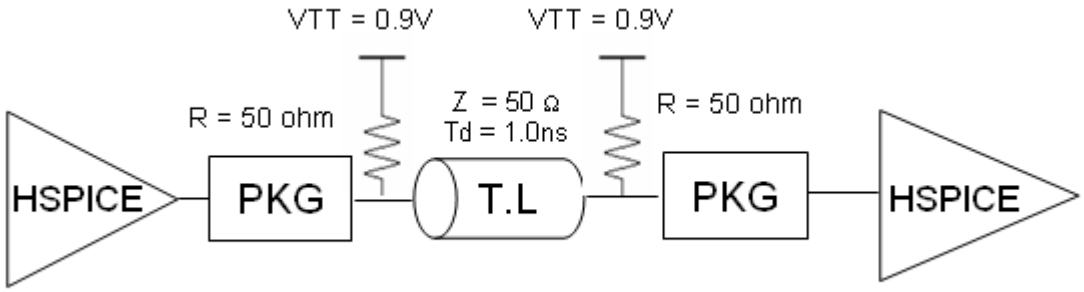

Figure 2-16. 1.8V HSTL Class II HSPICE Model Simulation Setup

2.4.1 Row I/O DIFFIO pin (Optional Pin Function) – 16ma Drive Strength with Fast Slew Rate, Slow Conditions

Figures 2-17 and 2-18 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 2-5 shows comparison between the two measurements.

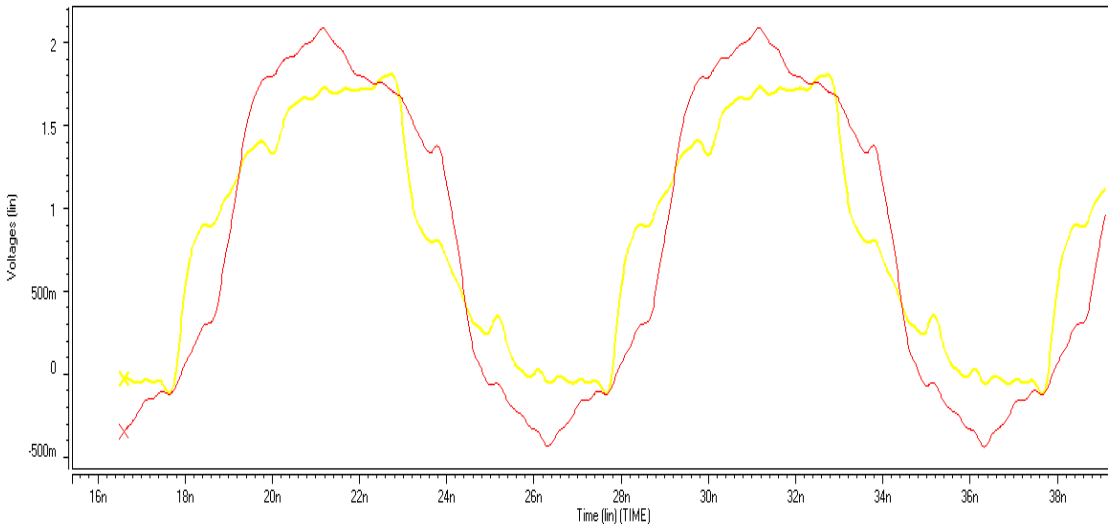

Figure 2-17. 1.8V HSTL Class II (Row I/O DIFFIO pin (Optional Pin Function), 16mA Drive Strength, Fast Slew Rate) IBIS Model Simulation Result at Slow Conditions.

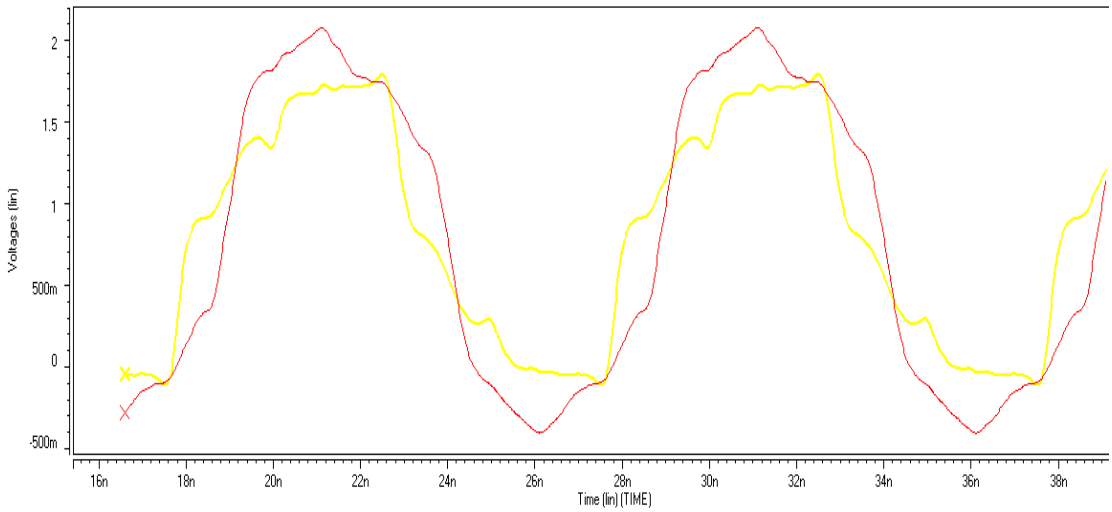

Figure 2-18. 1.8V HSTL Class II (Row I/O DIFFIO pin (Optional Pin Function), 16mA Drive Strength, Fast Slew Rate) HSPICE Model Simulation Result at Slow Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.42	2.44	0.8
Fall time	2.42	2.43	0.4

Table 2-5 1.8V HSTL Class II (Row I/O DIFFIO pin (Optional Pin Function), 16mA Drive Strength, Fast Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

3.0 SSTL Verification

Following shows the correlation between IBIS simulation and HSPICE simulation for 1.8V SSTL and 2.5V SSTL for Class I and Class II standard.

3.1 SSTL-18 Class I Verification

Figure 3-1 and 3-2 shows the simulation setup for 1.8V SSTL Class I IBIS output model and HSPICE output model.

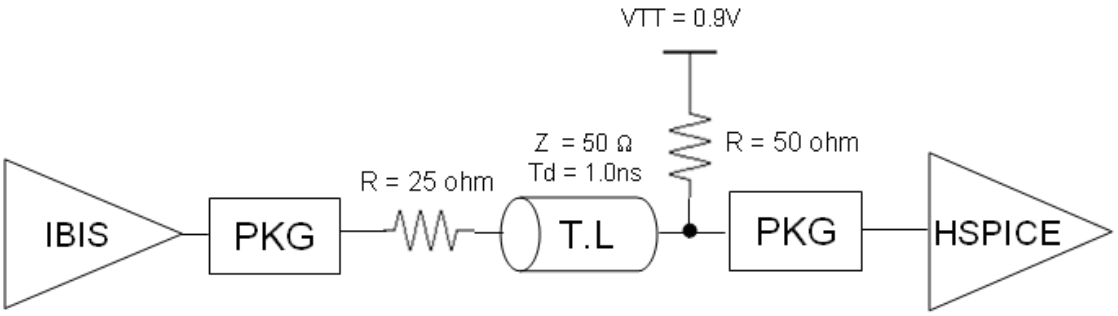

Figure 3-1. 1.8V SSTL Class I IBIS Model Simulation Setup

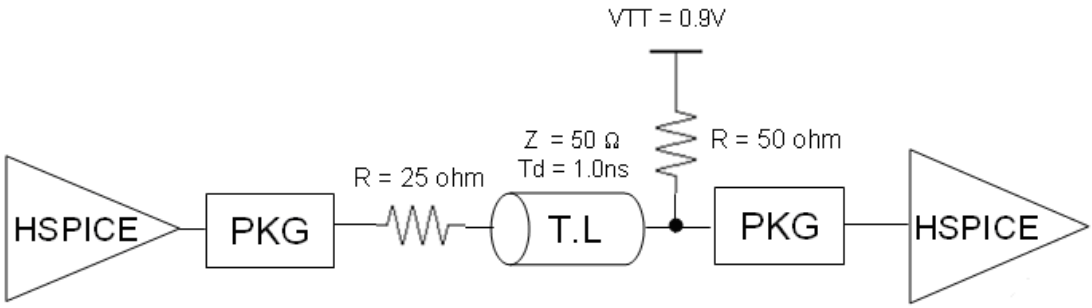

Figure 3-2. 1.8V SSTL Class I HSPICE Model Simulation Setup

3.1.1 Row I/O – 8ma Drive Strength with Slow Slew Rate, Typical Conditions

Figures 3-3 and 3-4 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 3-1 shows comparison between the two measurements.

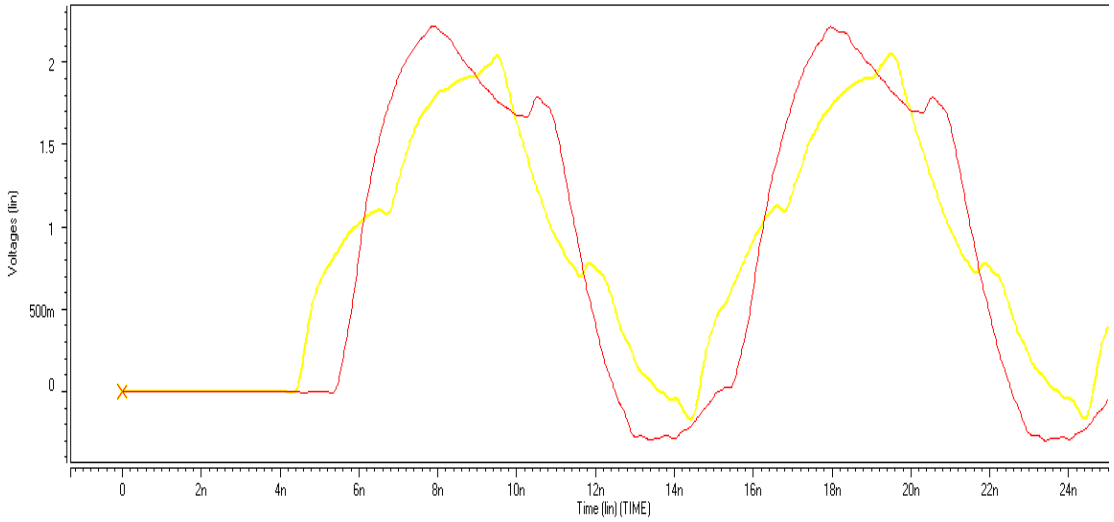

Figure 3-3. 1.8V SSTL Class I (Row I/O, 8mA Drive Strength, Slow Slew Rate) IBIS Model Simulation Result at Typical Conditions.

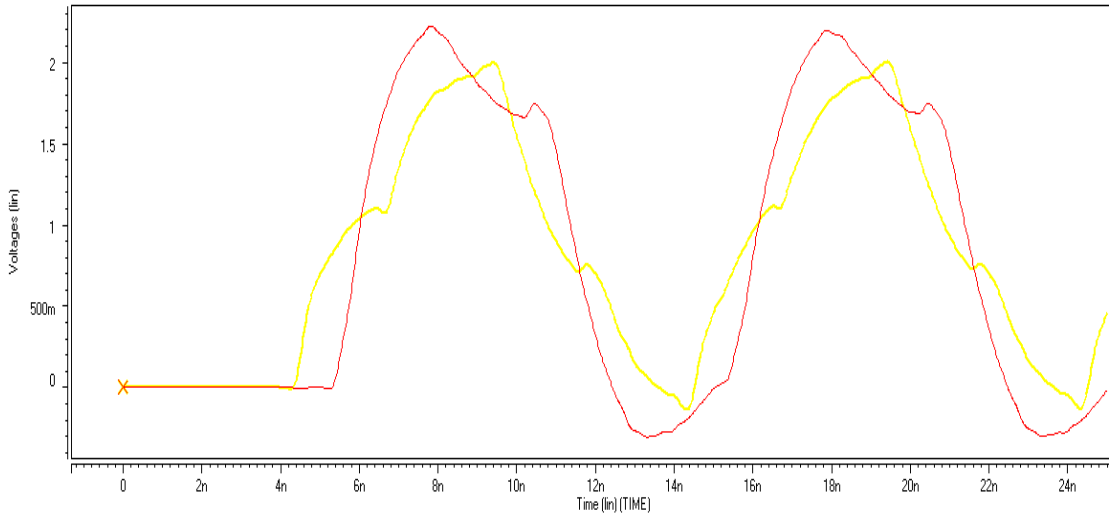

Figure 3-4. 1.8V SSTL Class I (Row I/O, 8mA Drive Strength, Slow Slew Rate) HSPICE Model Simulation Result at Typical Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	3.62	3.62	0.0
Fall time	3.67	3.67	0.0

Table 3-1 1.8V SSTL Class I (Row I/O, 8mA Drive Strength, Slow Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

3.1.2 Column I/O – 8ma Drive Strength with Medium Slew Rate, Slow Conditions

Figures 3-5 and 3-6 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 3-2 shows comparison between the two measurements.

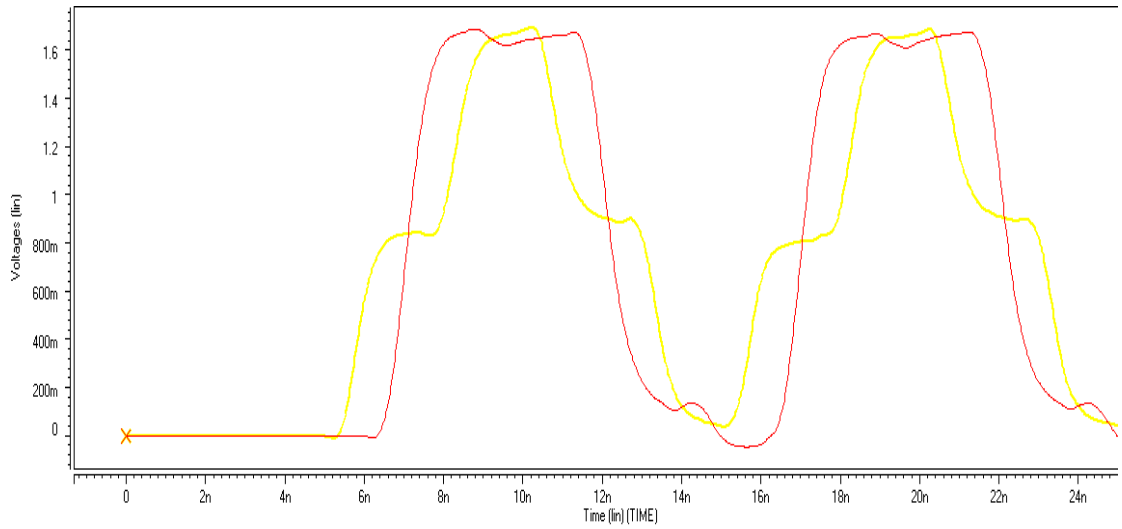

Figure 3-5. 1.8V SSTL Class I (Column I/O, 8mA Drive Strength, Medium Slew Rate) IBIS Model Simulation Result at Slow Conditions.

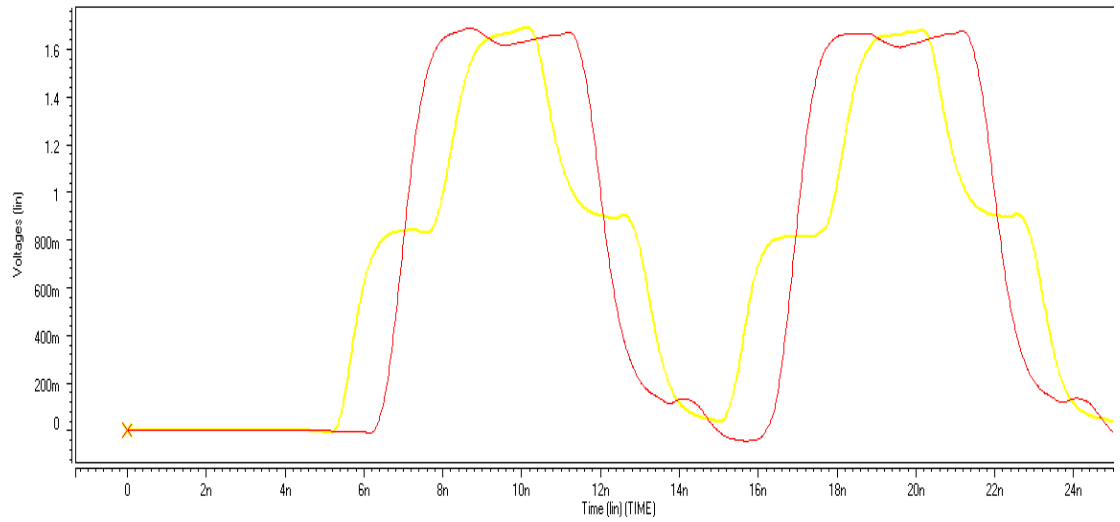

Figure 3-6. 1.8V SSTL Class I (Column I/O, 8mA Drive Strength, Medium Slew Rate) HSPICE Model Simulation Result at Slow Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	3.11	3.13	0.6
Fall time	3.20	3.26	1.8

Table 3-2 1.8V SSTL Class I (Column I/O, 8mA Drive Strength, Medium Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

3.2 SSTL-18 Class II Verification

Figure 3-7 and 3-8 shows the simulation setup for 1.8V SSTL Class II IBIS output model and HSPICE output model.

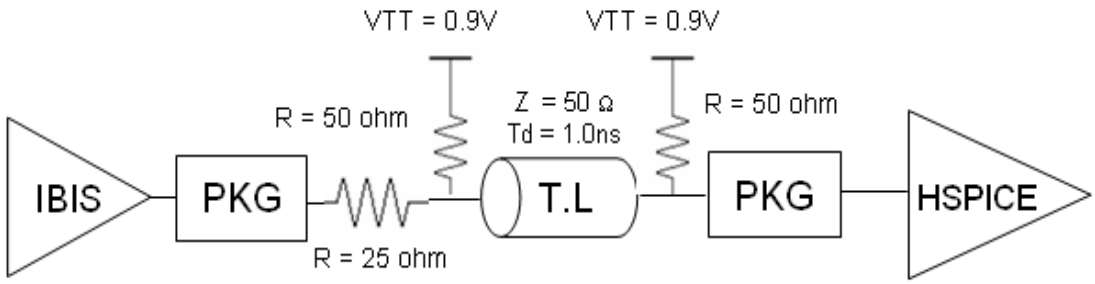

Figure 3-7. SSTL-18 Class II IBIS Model Simulation Setup

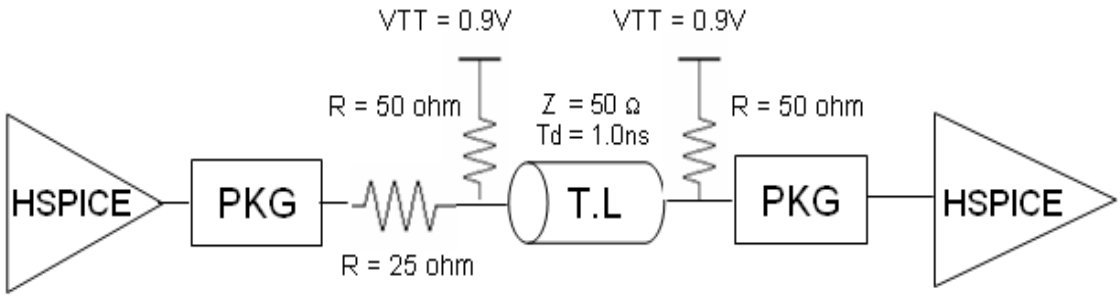

Figure 3-8. SSTL-18 Class II HSPICE Model Simulation Setup

3.2.1 Row I/O – 16ma Drive Strength with Medium Slew Rate, Fast Conditions

Figures 3-9 and 3-10 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 3-2 shows comparison between the two measurements.

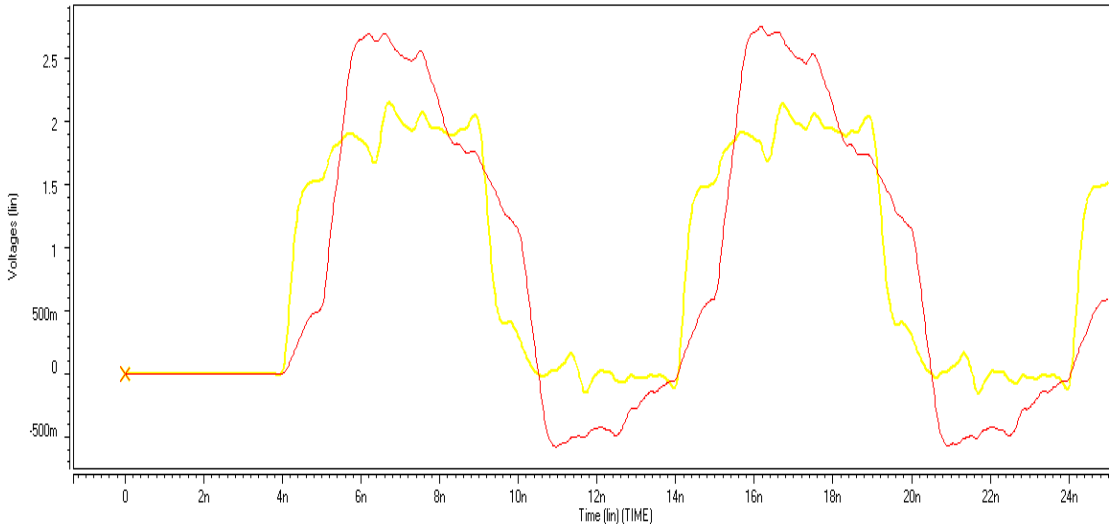

Figure 3-9. 1.8V SSTL Class II (Row I/O, 16mA Drive Strength, Medium Slew Rate) IBIS Model Simulation Result at Fast Conditions.

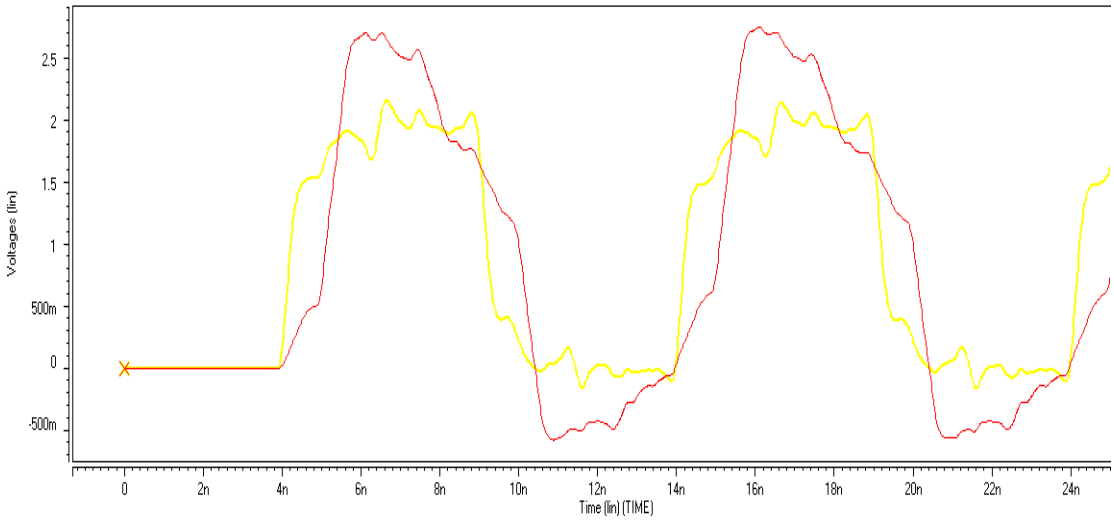

Figure 3-10. 1.8V SSTL Class II (Row I/O, 16mA Drive Strength, Medium Slew Rate) HSPICE Model Simulation Result at Fast Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	1.12	1.12	0.0
Fall time	1.04	1.03	1.0

Table 3-3 1.8V SSTL Class II (Row I/O, 16mA Drive Strength, Medium Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Fast Conditions

3.3 SSTL-2 Class I Verification

Figure 3-11 and 3-12 shows the simulation setup for 2.5V SSTL Class I IBIS output model and HSPICE output model.

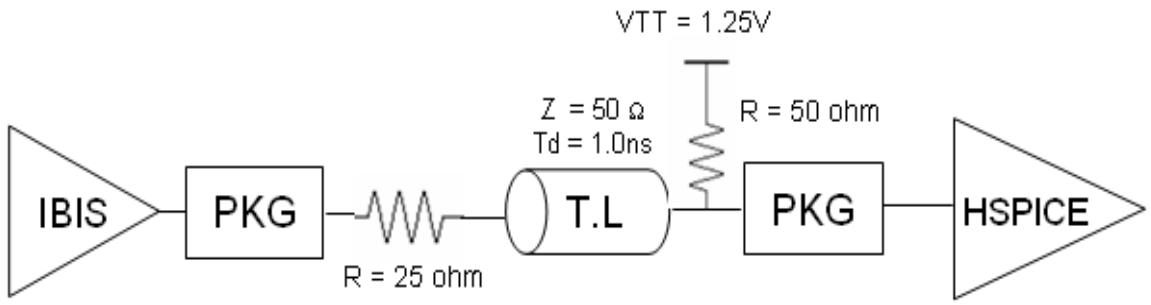

Figure 3-11. SSTL-2 Class I IBIS Model Simulation Setup

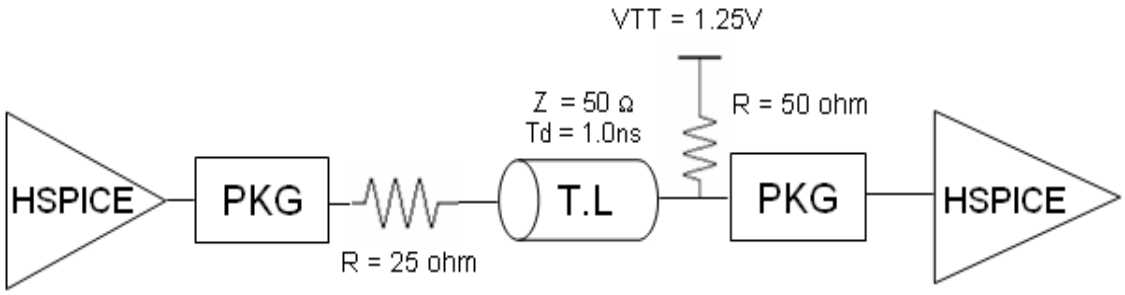

Figure 3-12. SSTL-2 Class I HSPICE Model Simulation Setup

3.3.1 Column I/O – 12ma Drive Strength with Medium Slew Rate, Slow Conditions

Figures 3-13 and 3-14 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 3-4 shows comparison between the two measurements.

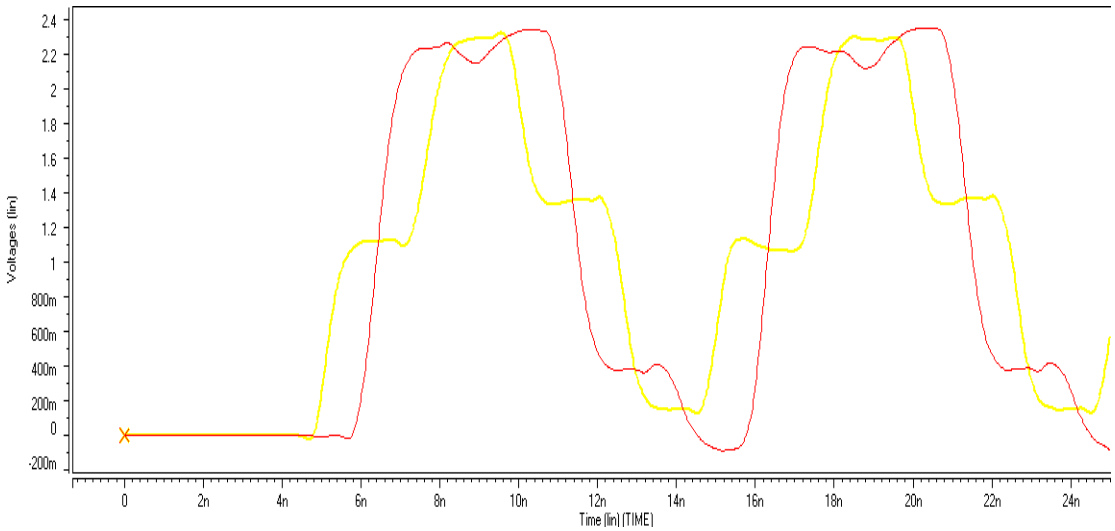

Figure 3-13. 2.5V SSTL Class I (Column I/O, 12mA Drive Strength, Medium Slew Rate) IBIS Model Simulation Result at Slow Conditions.

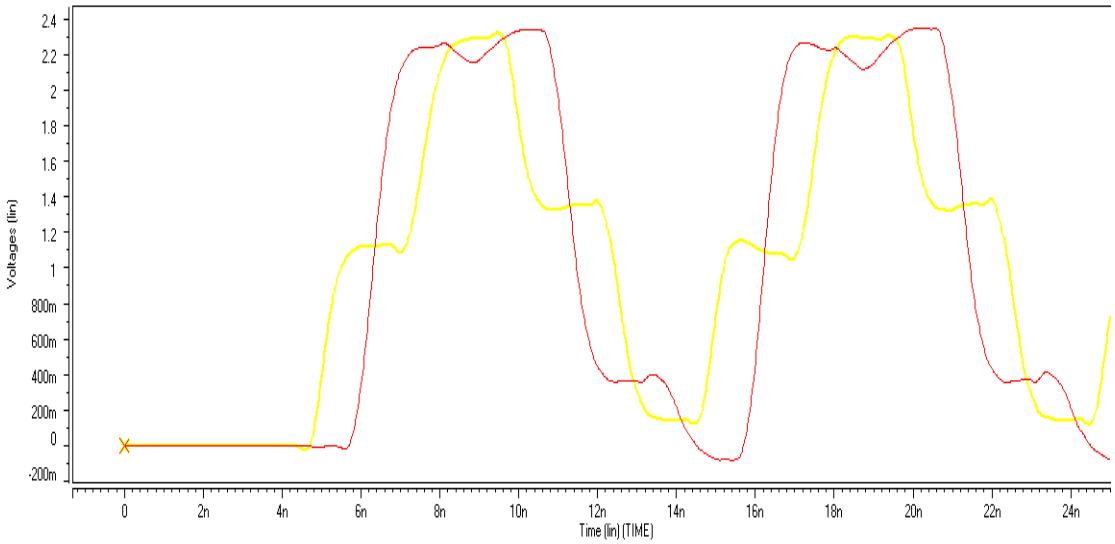

Figure 3-14. 2.5V SSTL Class I (Column I/O, 12mA Drive Strength, Medium Slew Rate) HSPICE Model Simulation Result at Slow Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	3.14	3.13	0.3
Fall time	3.24	3.29	1.5

Table 3-4 2.5V SSTL Class I (Column I/O, 12mA Drive Strength, Medium Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

3.4 SSTL-2 Class II Verification

Figure 3-15 and 3-16 shows the simulation setup for 2.5V SSTL Class II IBIS output model and HSPICE output model.

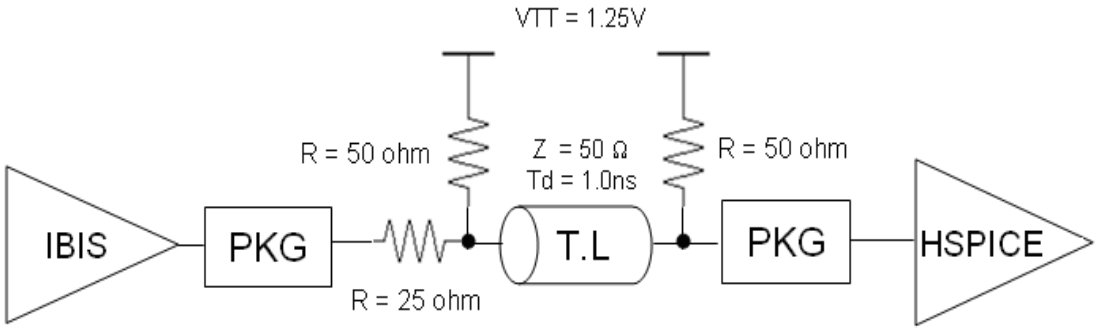

Figure 3-15. SSTL-2 Class II IBIS Model Simulation Setup

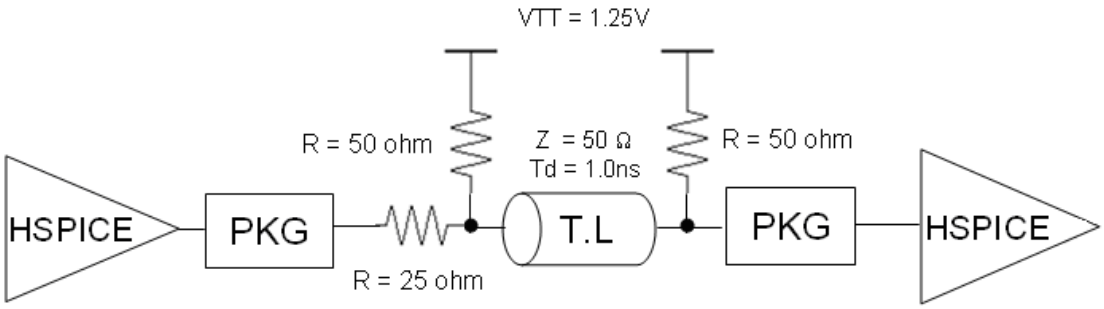

Figure 3-16. SSTL-2 Class II HSPICE Model Simulation Setup

3.4.1 Column I/O – 16ma Drive Strength with Medium Slew Rate, Typical Conditions

Figures 3-17 and 3-18 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 3-5 shows comparison between the two measurements.

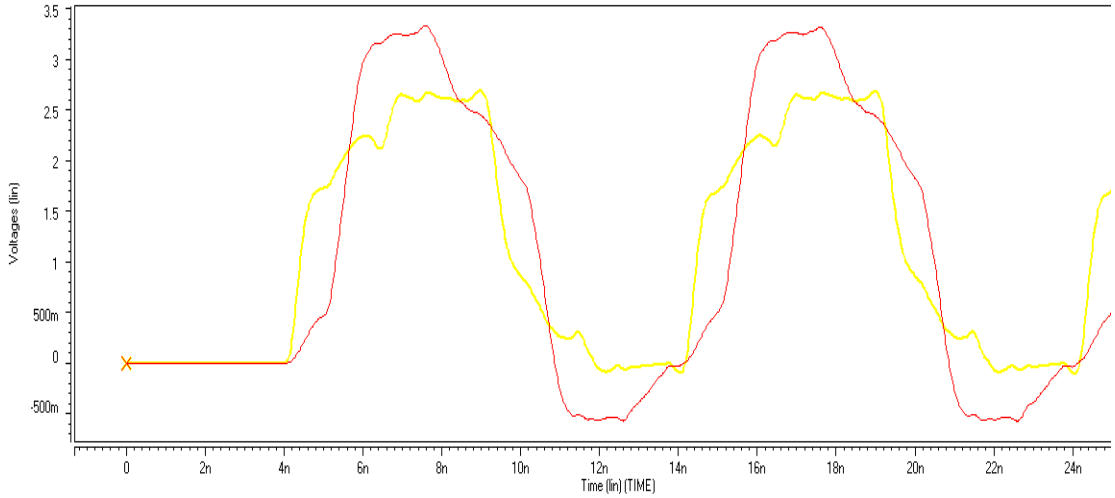

Figure 3-17. SSTL-2 Class II (Column I/O, 16mA Drive Strength, Medium Slew Rate) IBIS Model Simulation Result at Typical Conditions.

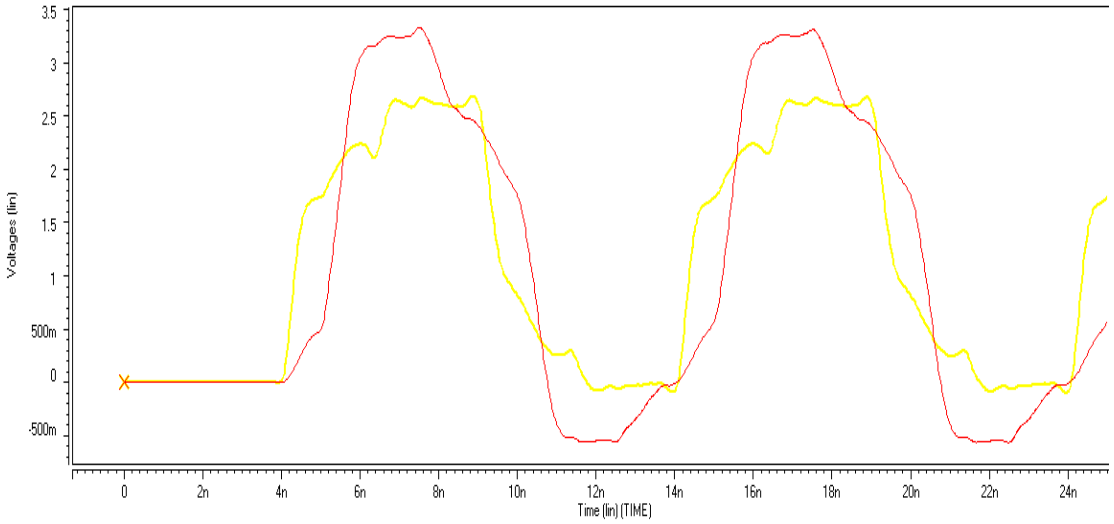

Figure 3-18. SSTL-2 Class II (Column I/O, 16mA Drive Strength, Medium Slew Rate) HSPICE Model Simulation Result at Typical Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.44	2.44	0.0
Fall time	1.74	1.76	1.1

Table 3-5. SSTL-2 Class II (Column I/O, 16mA Drive Strength, Medium Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

4.0 LVTTL Verification

Following shows the correlation between IBIS simulation and HSPICE simulation for 3.3V, 3.0V, 2.5V and 1.8V LVTTL.

4.1 3.3V LVTTL Verification

Figure 4-1 and 4-2 shows the simulation setup for 3.3V LVTTL IBIS output model and HSPICE output model.

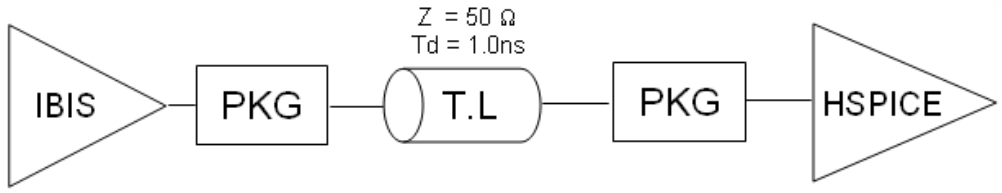

Figure 4-1. 3.3V LVTTL IBIS Model Simulation Setup

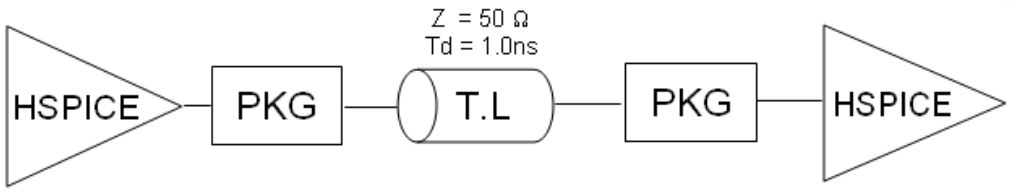

Figure 4-2. 3.3V LVTTL HSPICE Model Simulation Setup

4.1.1 Row I/O DIFFIO pin (Optional Pin Function) – 8mA Drive Strength, Typical Conditions

Figures 4-3 and 4-4 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 2-1 shows comparison between the two measurements.

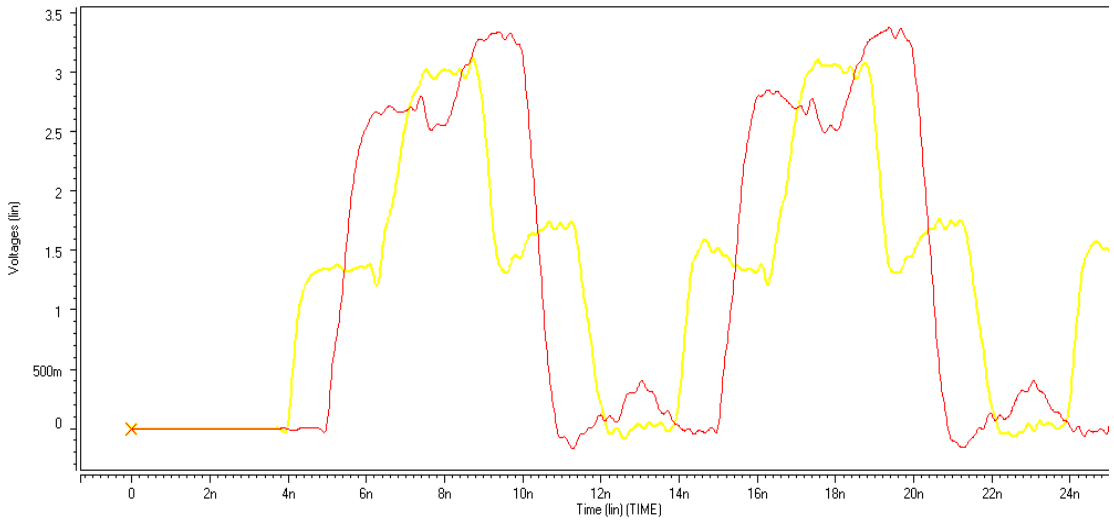

Figure 4-3. 3.3V LVTTL (Row I/O DIFFIO pin (Optional Pin Function), 8mA Drive Strength) IBIS Model Simulation Result at Typical Conditions.

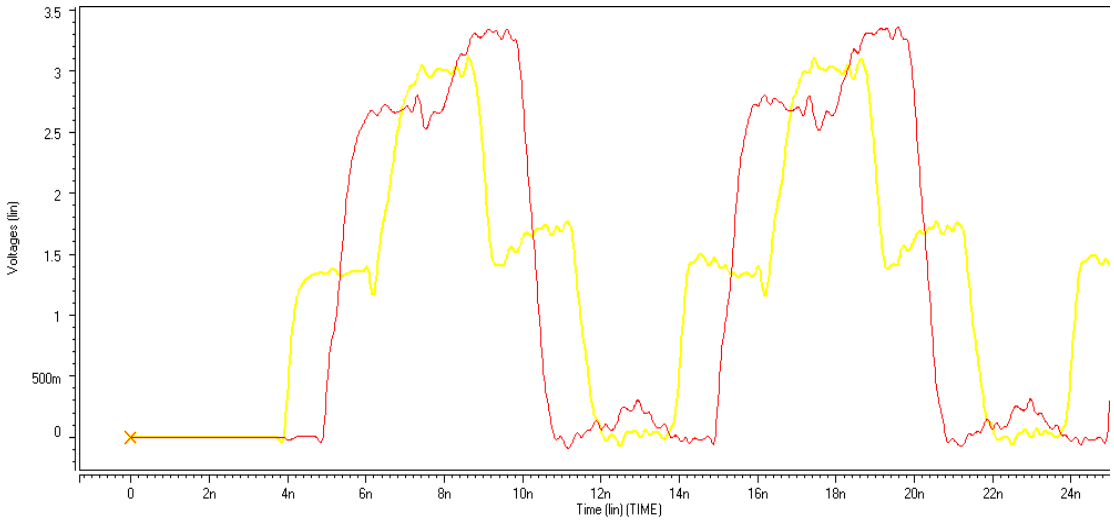

Figure 4-4. 3.3V LVTTL (Row I/O DIFFIO pin (Optional Pin Function), 8mA Drive Strength) HSPICE Model Simulation Result at Typical Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	3.02	2.95	2.4
Fall time	2.94	2.87	2.4

Table 4-1. 3.3V LVTTL (Row I/O DIFFIO pin (Optional Pin Function), 8mA Drive Strength) IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

4.2 3.0V LVTTL Verification

Figure 4-5 and 4-6 shows the simulation setup for 3.0V LVTTL IBIS output model and HSPICE output model.

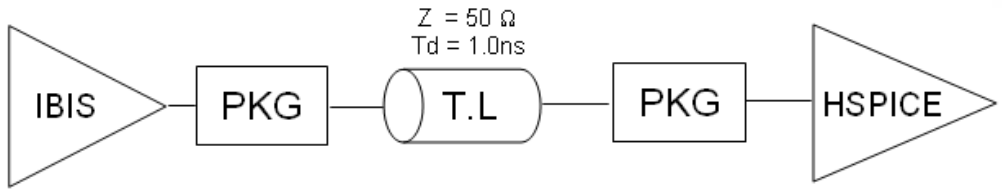

Figure 4-5. 3.0V LVTTL IBIS Model Simulation Setup

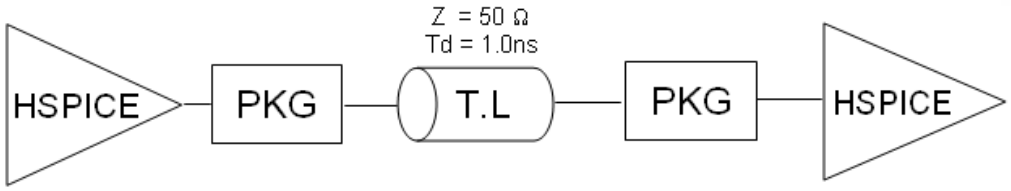

Figure 4-6. 3.0V LVTTL HSPICE Model Simulation Setup

4.2.1 Column I/O – 8ma Drive Strength with Fast Slew Rate, Slow Conditions

Figures 4-7 and 4-8 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 4-2 shows comparison between the two measurements.

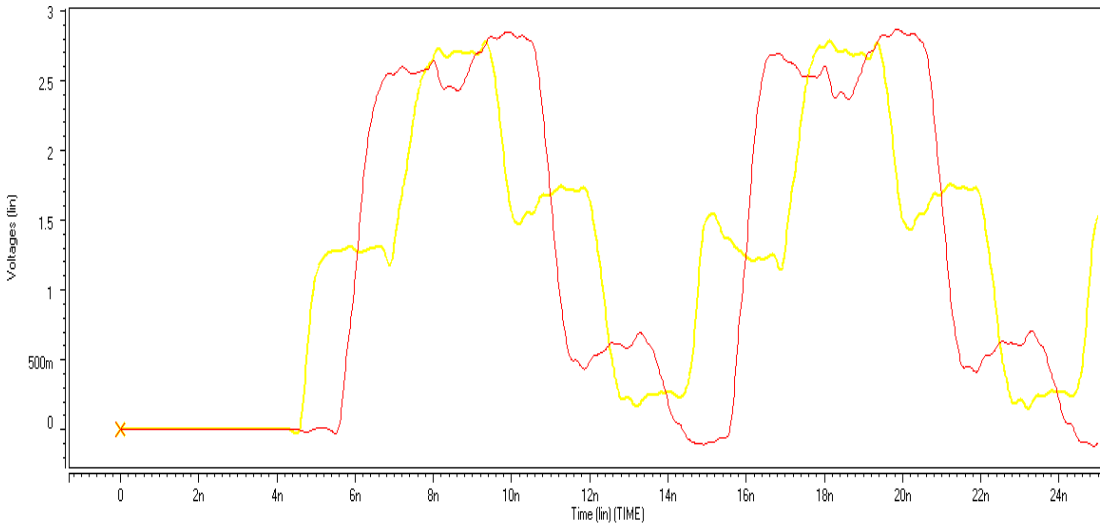

Figure 4-7. 3.0V LVTTL (Column I/O, 8mA Drive Strength, Fast Slew Rate) IBIS Model Simulation Result at Slow Conditions.

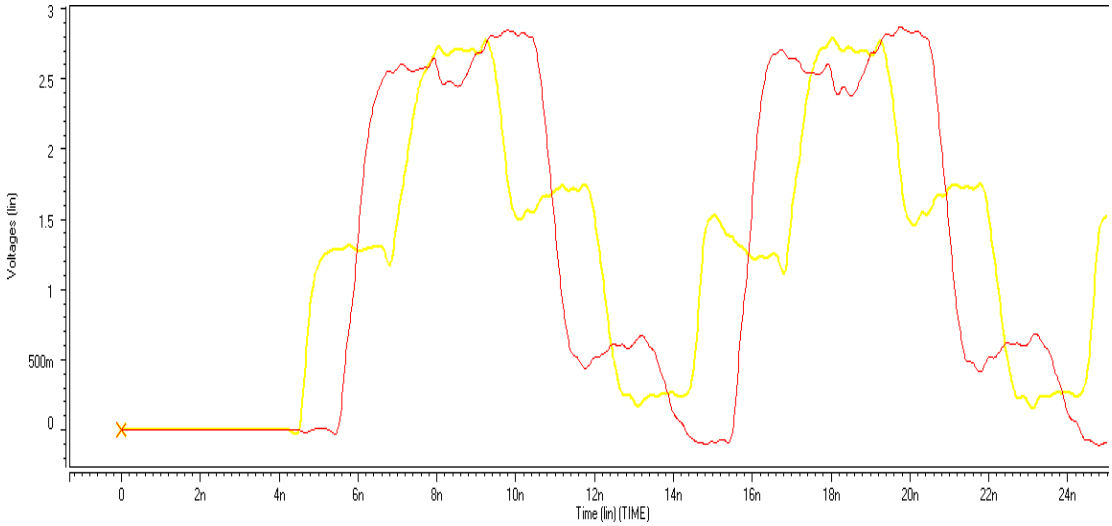

Figure 4-8. 3.0V LVTTL (Column I/O, 8mA Drive Strength, Fast Slew Rate)HSPICE Model Simulation Result at Slow Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	3.08	3.04	1.3
Fall time	3.12	3.13	0.3

Table 4-2 3.0V LVTTL (Column I/O, 8mA Drive Strength, Fast Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Fast Conditions

4.3 2.5V LVTTL Verification

Figure 4-9 and 4-10 shows the simulation setup for 2.5V LVTTL IBIS output model and HSPICE output model.

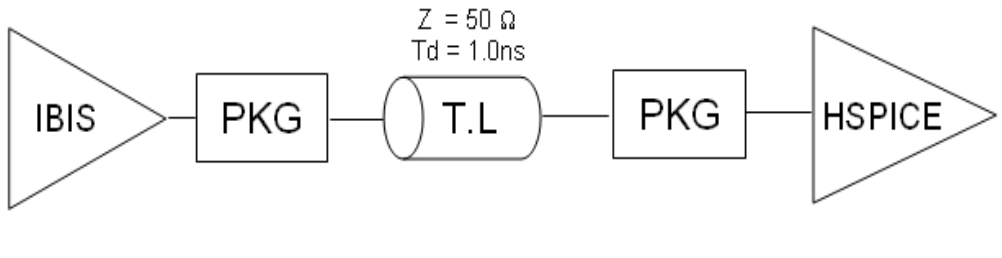

Figure 4-9. 2.5V LVTTL IBIS Model Simulation Setup

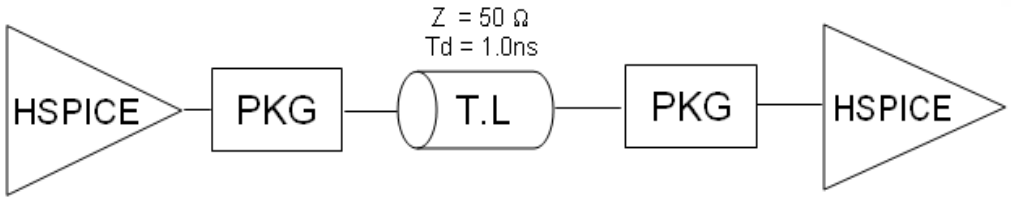

Figure 4-10. 2.5V LVTTL HSPICE Model Simulation Setup

4.3.1 Row I/O DIFFIO pin (Optional Pin Function) – 8ma Drive Strength with Medium Slew Rate, Slow Conditions

Figures 4-11 and 4-12 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 4-3 shows comparison between the two measurements.

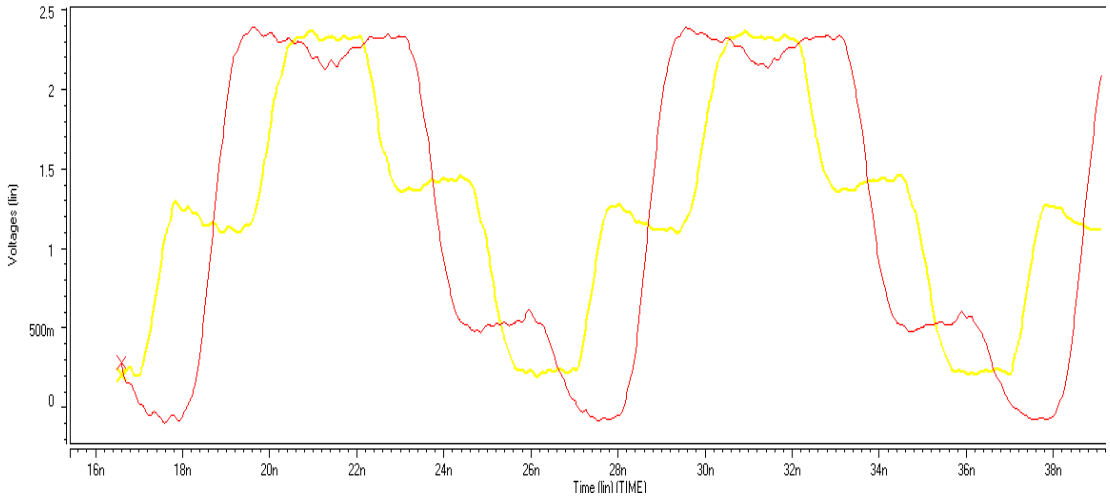

Figure 4-11. 2.5V LVTTL (Row I/O DIFFIO pin (Optional Pin Function), 8mA Drive Strength, Medium Slew Rate) IBIS Model Simulation Result at Slow Conditions.

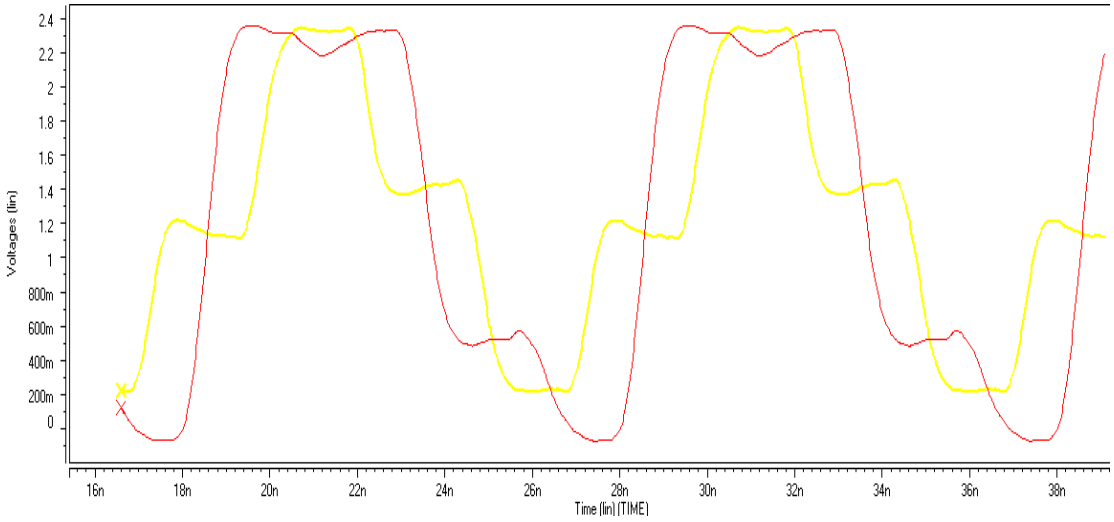

Figure 4-12. 2.5V LVTTL (Row I/O DIFFIO pin (Optional Pin Function), 8mA Drive Strength, Medium Slew Rate) HSPICE Model Simulation Result at Slow Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	3.25	3.33	2.4
Fall time	3.76	3.80	1.05

Table 4-3 2.5V LVTTL (Row I/O DIFFIO pin (Optional Pin Function), 8mA Drive Strength, Medium Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

4.3.2 Column I/O – 50 ohm OCT without Calibration, Fast Conditions

Figures 4-13 and 4-14 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 4-4 shows comparison between the two measurements.

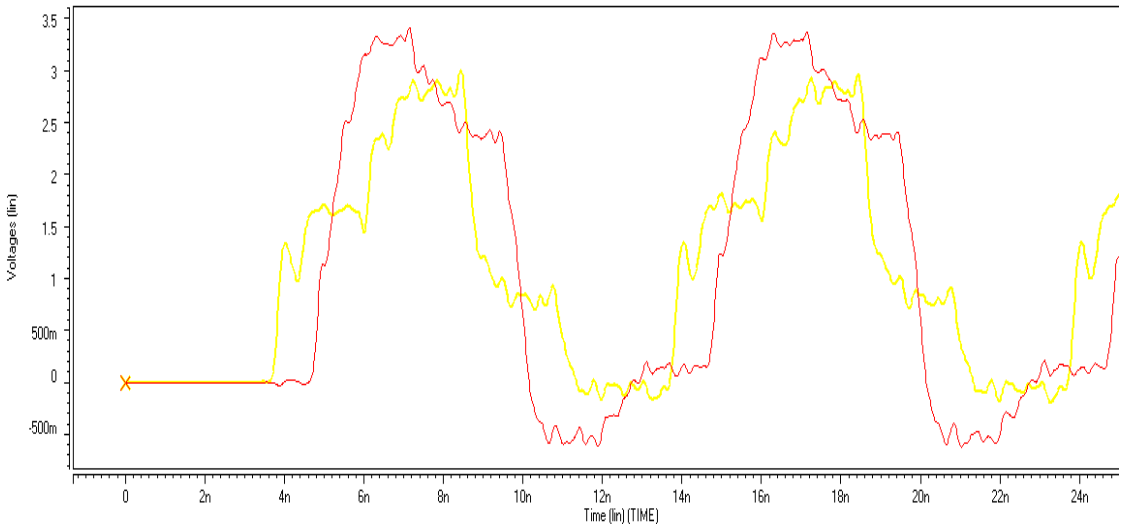

Figure 4-13. 2.5V LVTTL (Column I/O, 50 ohm OCT without Calibration) IBIS Model Simulation Result at Fast Conditions.

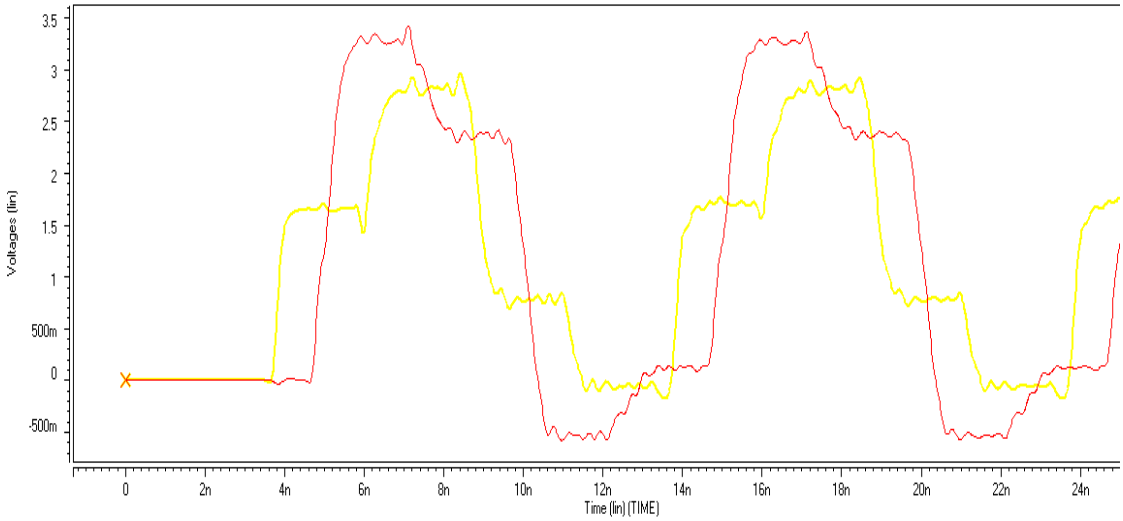

Figure 4-14. 2.5V LVTTL (Column I/O, 50 ohm OCT without Calibration) HSPICE Model Simulation Result at Fast Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.99	2.76	8.3
Fall time	2.50	2.56	2.3

Table 4-4. 2.5V LVTTL (Column I/O, 50 ohm OCT without Calibration) IBIS Simulation Vs HSPICE Simulation Result at Fast Condition

4.3.3 Row I/O DIFFIO pin (Optional Pin Function) – 16ma Drive Strength with PCI diode enabled, Fast Conditions

Figures 4-15 and 4-16 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 4-5 shows comparison between the two measurements.

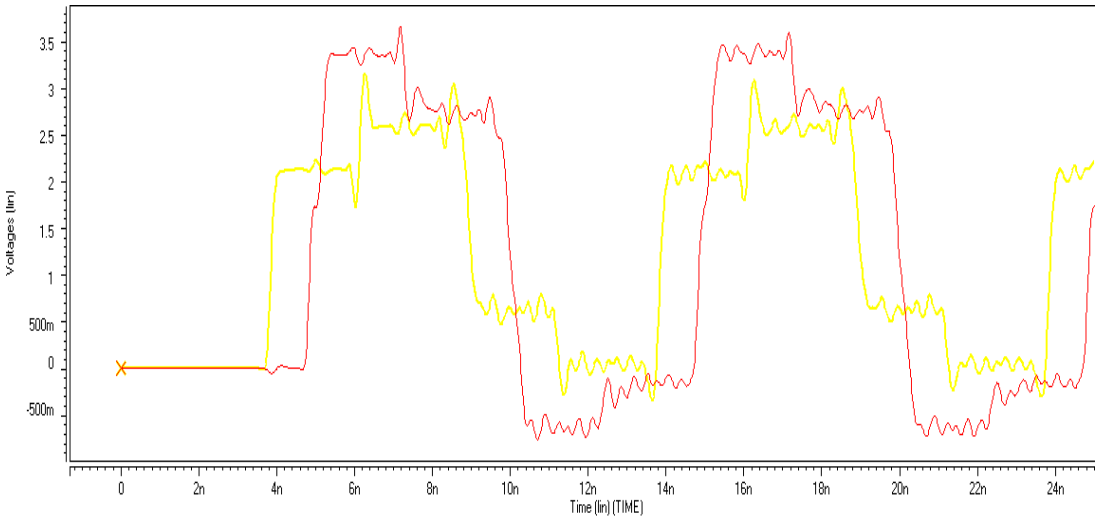

Figure 4-15. 2.5V LVTTL (Row I/O DIFFIO pin (Optional Pin Function), 16mA Drive Strength with PCI-diode enabled) IBIS Model Simulation Result at Fast Conditions.

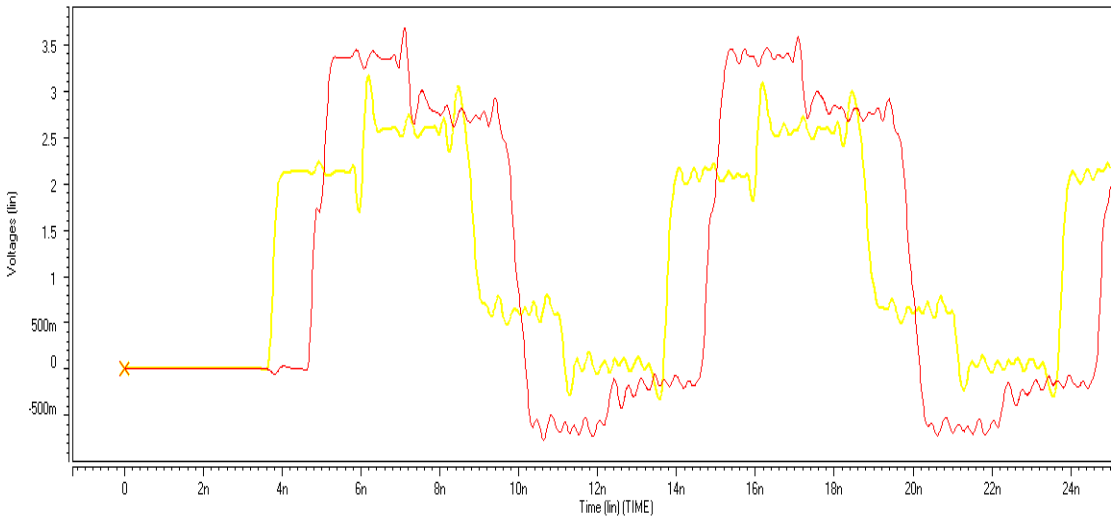

Figure 4-16. 2.5V LVTTL (Row I/O DIFFIO pin (Optional Pin Function), 16mA Drive Strength with PCI-diode enabled) HSPICE Model Simulation Result at Fast Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.33	2.33	0.0
Fall time	2.39	2.39	0.0

Table 4-5 2.5V LVTTL (Row I/O DIFFIO pin (Optional Pin Function), 16mA Drive Strength with PCI-diode enabled) IBIS Simulation Vs HSPICE Simulation Result at Fast Conditions

4.4 1.8V LVTTL Verification

Figure 4-17 and 4-18 shows the simulation setup for 1.8V LVTTL IBIS output model and HSPICE output model.

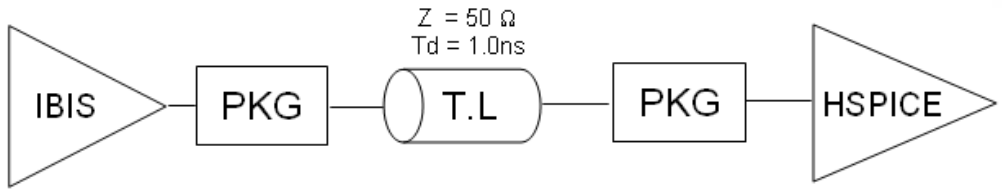

Figure 4-17. 1.8V LVTTL IBIS Model Simulation Setup

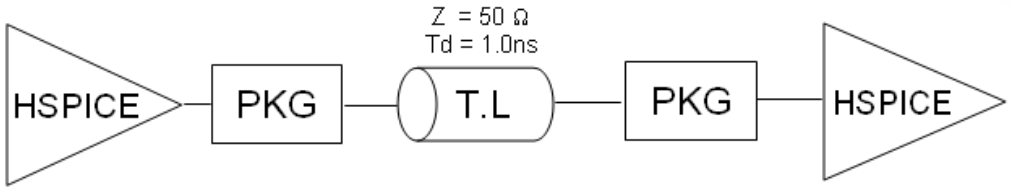

Figure 4-18. 1.8V LVTTL HSPICE Model Simulation Setup

4.4.1 Column I/O – 25 ohm OCT with Calibration, Slow Conditions

Figures 4-19 and 4-20 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 4-6 shows comparison between the two measurements.

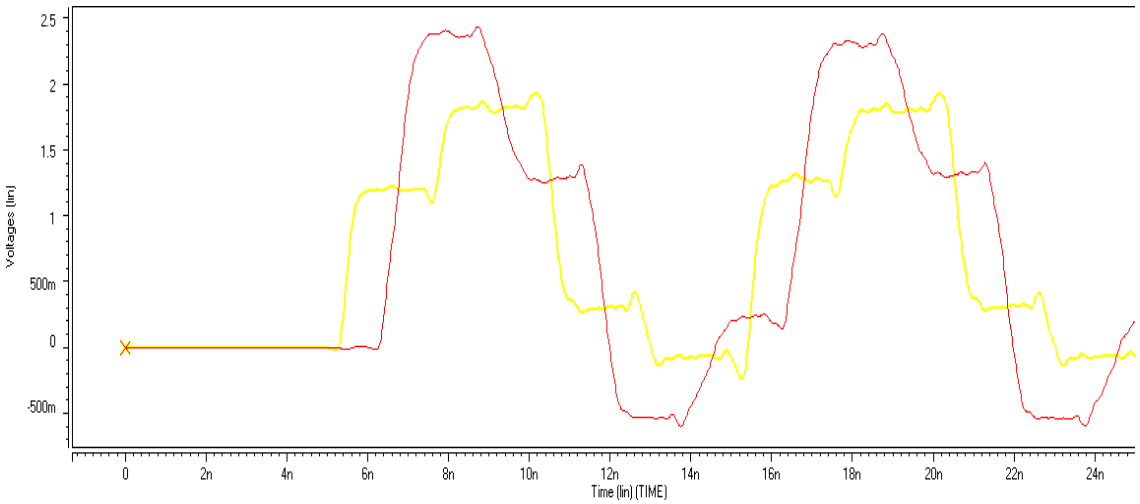

Figure 4-19. 1.8V LVTTL (Column I/O, 25 ohm OCT with Calibration) IBIS Model Simulation Result at Slow Conditions.

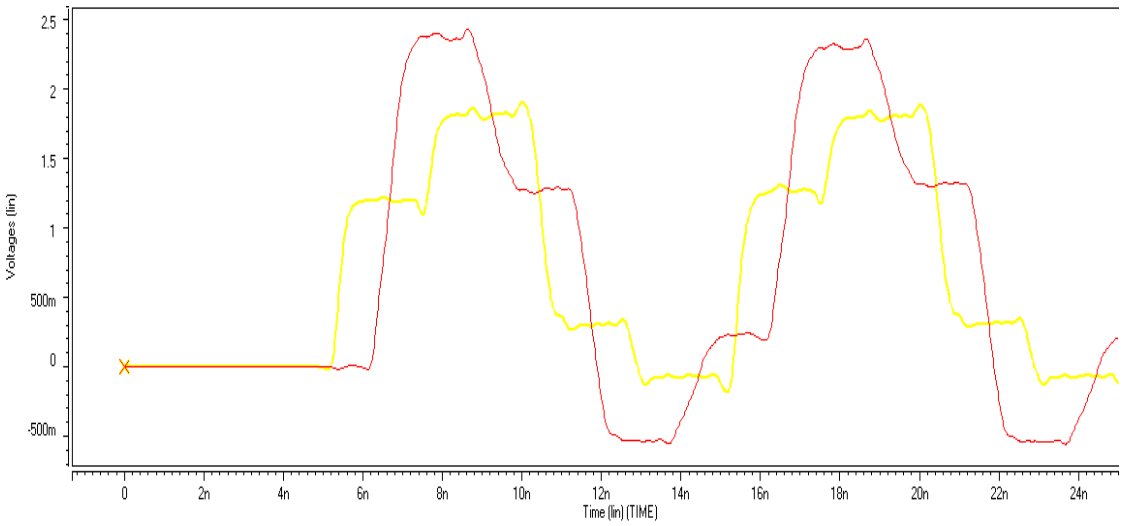

Figure 4-20. 1.8V LVTTL (Column I/O, 25 ohm OCT with Calibration) HSPICE Model Simulation Result at Slow Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.47	2.46	0.4
Fall time	2.41	2.44	1.2

Table 4-6. 1.8V LVTTL (Column I/O, 25 ohm OCT with Calibration) IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

5.0 LVCMOS Verification

Following shows the correlation between IBIS simulation and HSPICE simulation for 1.5V and 1.2V LVCMOS.

5.1 1.5V LVCMOS Verification

Figure 5-1 and 5-2 shows the simulation setup for 1.5V LVCMOS IBIS output model and HSPICE output model.

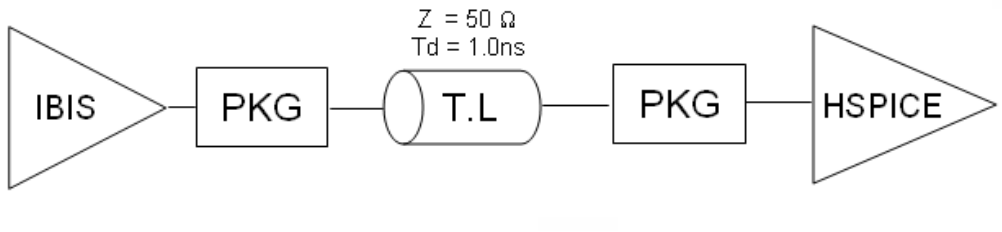

Figure 5-1. 1.5V LVCMOS IBIS Model Simulation Setup

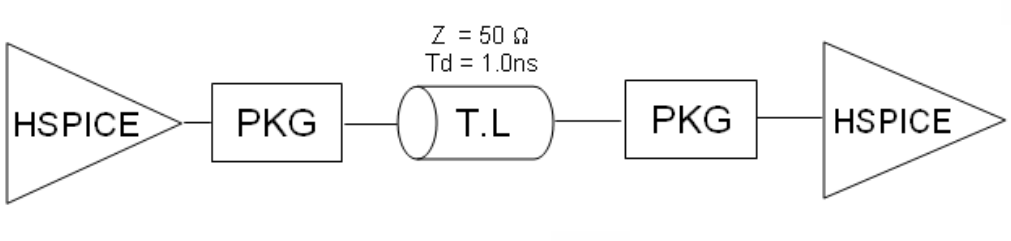

Figure 5-2. 1.5V LVCMOS HSPICE Model Simulation Setup

5.1.1 Row I/O – 12ma Drive Strength with Slow Slew Rate, Typical conditions

Figures 5-3 and 5-4 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 5-1 shows comparison between the two measurements.

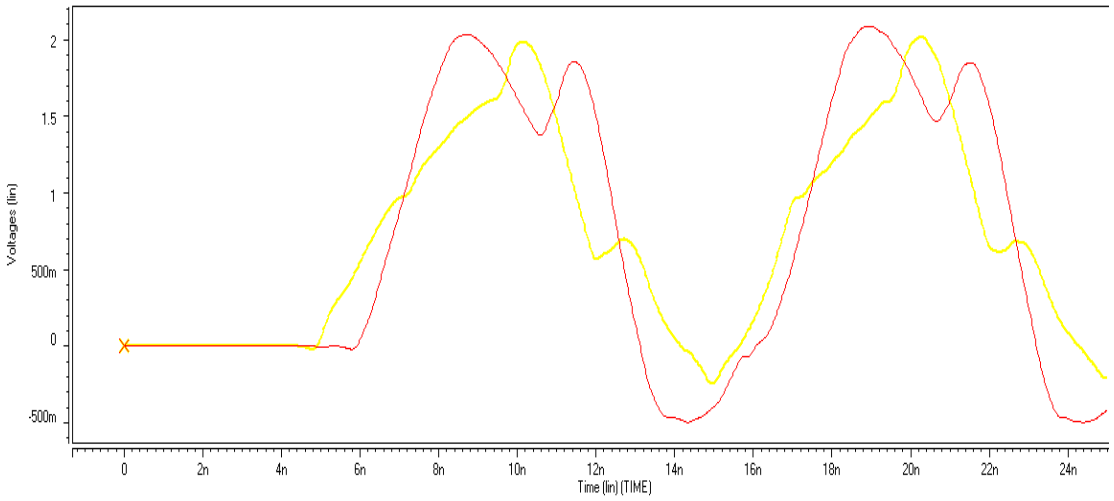

Figure 5-3. 1.5V LVCMOS (Row I/O, 12mA Drive Strength, Slow Slew Rate) IBIS Model Simulation Result at Typical Conditions.

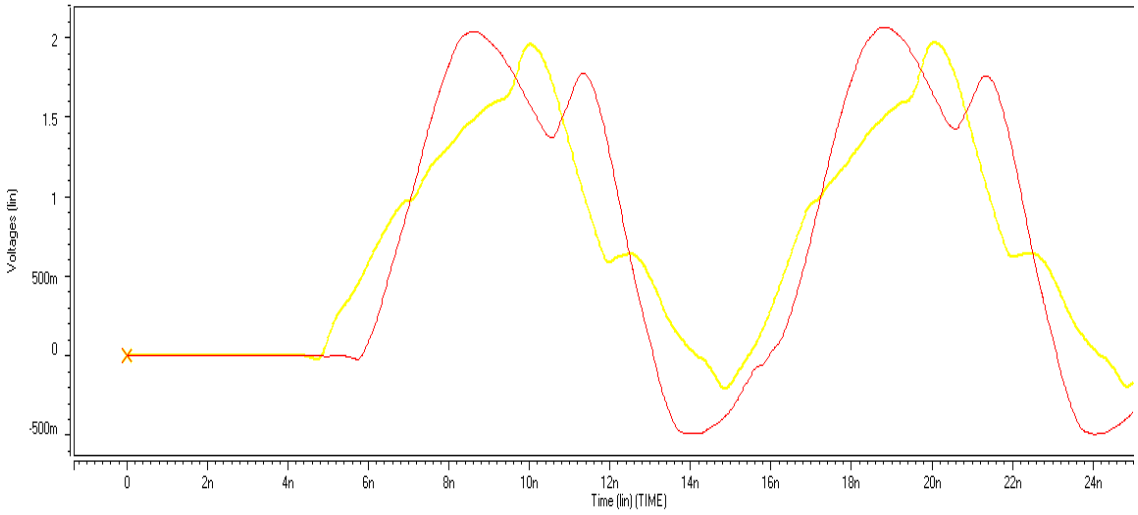

Figure 5-4. 1.5V LVCMOS (Row I/O, 12mA Drive Strength, Slow Slew Rate) HSPICE Model Simulation Result at Typical Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	3.34	3.39	1.5
Fall time	2.70	2.74	1.5

Table 5-1. 1.5V LVCMOS (Row I/O, 12mA Drive Strength, Slow Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

5.1.2 Row I/O DIFFIO pin (Optional Pin Function) – 4ma Drive Strength with Fast Slew Rate, Fast Conditions

Figures 5-5 and 5-6 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 5-2 shows comparison between the two measurements.

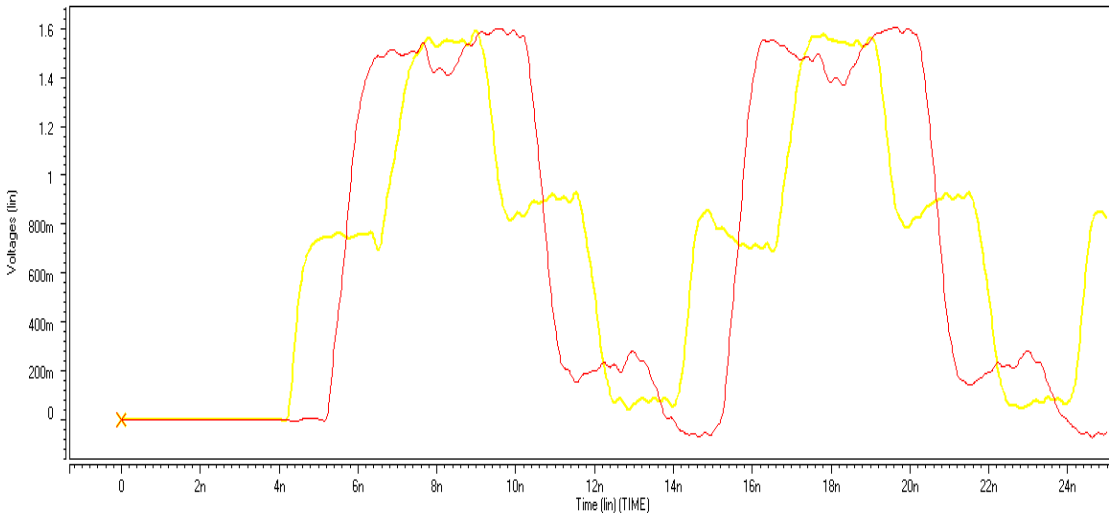

Figure 5-5. 1.5V LVCMOS (Row I/O DIFFIO pin (Optional Pin Function), 4mA Drive Strength, Fast Slew Rate) IBIS Model Simulation Result at Fast Conditions.

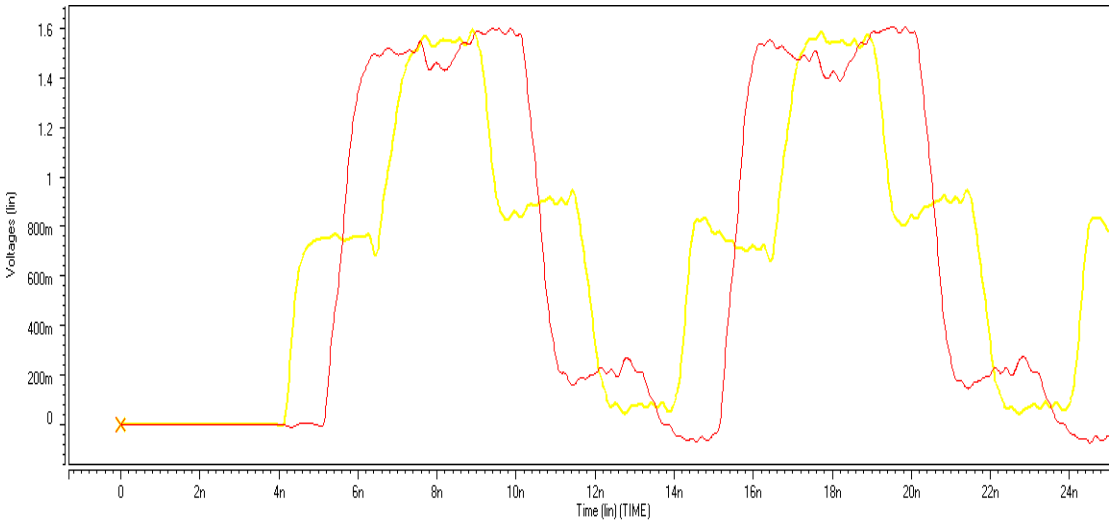

Figure 5-6. 1.5V LVCMOS (Row I/O DIFFIO pin (Optional Pin Function), 4mA Drive Strength, Fast Slew Rate) HSPICE Model Simulation Result at Fast Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.97	2.93	1.4
Fall time	3.03	3.00	1.0

Table 5-2 1.5V LVCMOS (Row I/O with LVDS load, 4mA Drive Strength, Fast Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Fast Conditions

5.2 1.2V LVCMOS Verification

Figure 5-7 and 5-8 shows the simulation setup for 1.2V LVCMOS IBIS output model and HSPICE output model.

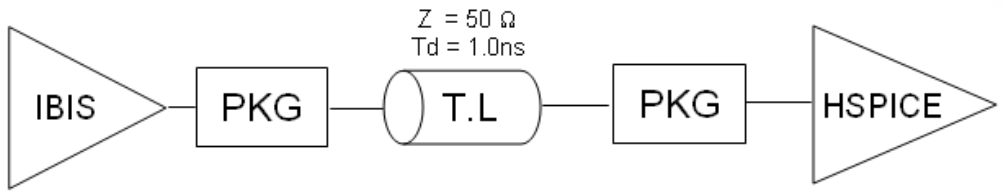

Figure 5-7. 1.2V LVCMOS IBIS Model Simulation Setup

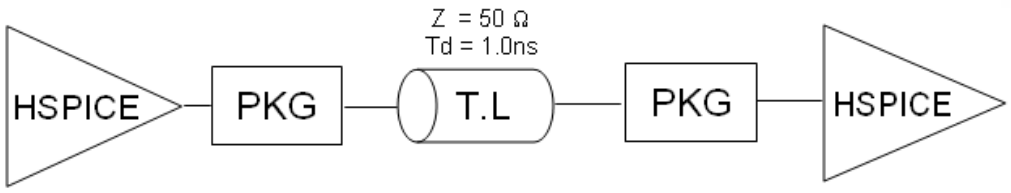

Figure 5-8. 1.2V LVCMOS HSPICE Model Simulation Setup

5.2.1 Column I/O – 25 ohm OCT with Calibration, Typical Conditions

Figures 5-9 and 5-10 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 5-3 shows comparison between the two measurements.

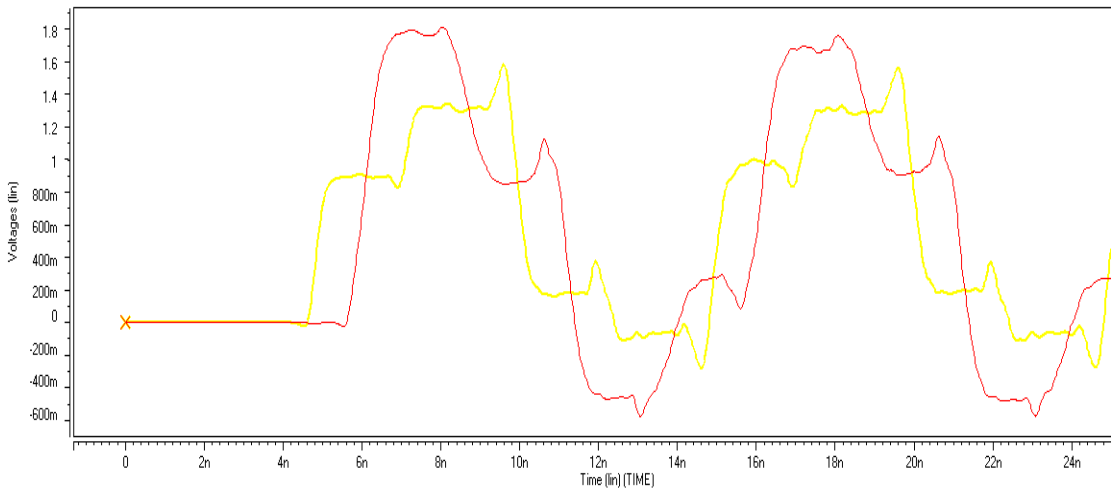

Figure 5-9. 1.2V LVCMOS (Column I/O, 25 ohm OCT with Calibration) IBIS Model Simulation Result at Typical Conditions.

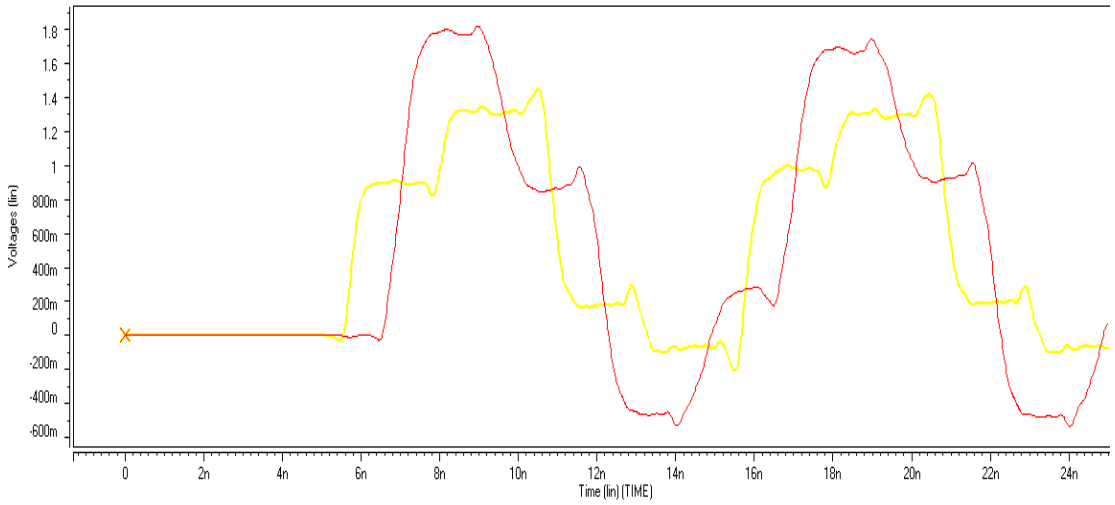

Figure 5-10. 1.2V LVCMOS (Column I/O, 25 ohm OCT with Calibration) HSPICE Model Simulation Result at Typical Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.53	2.53	0.0
Fall time	2.44	2.40	1.7

Table 5-3. 1.2V LVCMOS (Column I/O, 25 ohm OCT with Calibration) IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

5.2.2 Row I/O – 50 ohm OCT with Calibration, Fast Conditions

Figures 5-11 and 5-12 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 5-4 shows comparison between the two measurements.

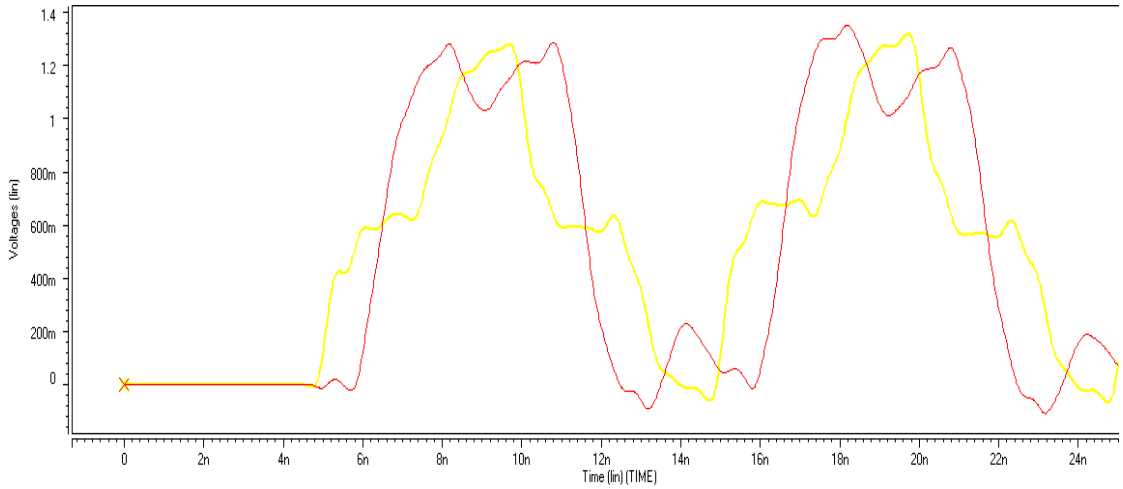

Figure 5-11. 1.2V LVCMOS (Row I/O, 50 ohm OCT with Calibration) IBIS Model Simulation Result at Fast Conditions.

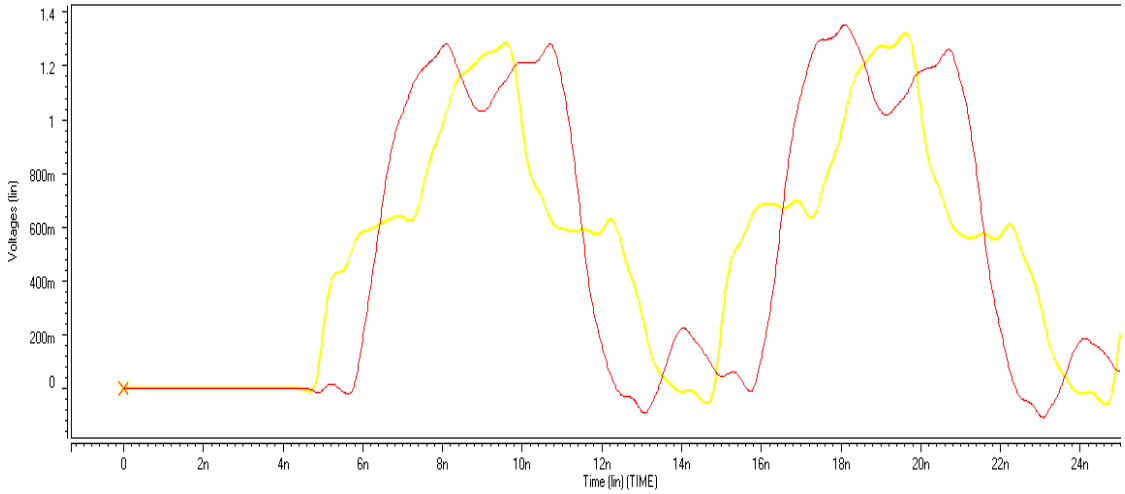

Figure 5-12. 1.2V LVCMOS (Row I/O, 50 ohm OCT with Calibration) HSPICE Model Simulation Result at Fast Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	3.37	3.38	0.3
Fall time	3.37	3.39	0.6

Table 5-4. 1.2V LVCMOS (Row I/O, 50 ohm OCT with Calibration) IBIS Simulation Vs HSPICE Simulation Result at Fast Conditions

5.2.3 Row I/O DIFFIO pin (Optional Pin Function) – 8ma Drive Strength with Fast Slew Rate, Fast Conditions

Figures 5-13 and 5-14 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 5-5 shows comparison between the two measurements.

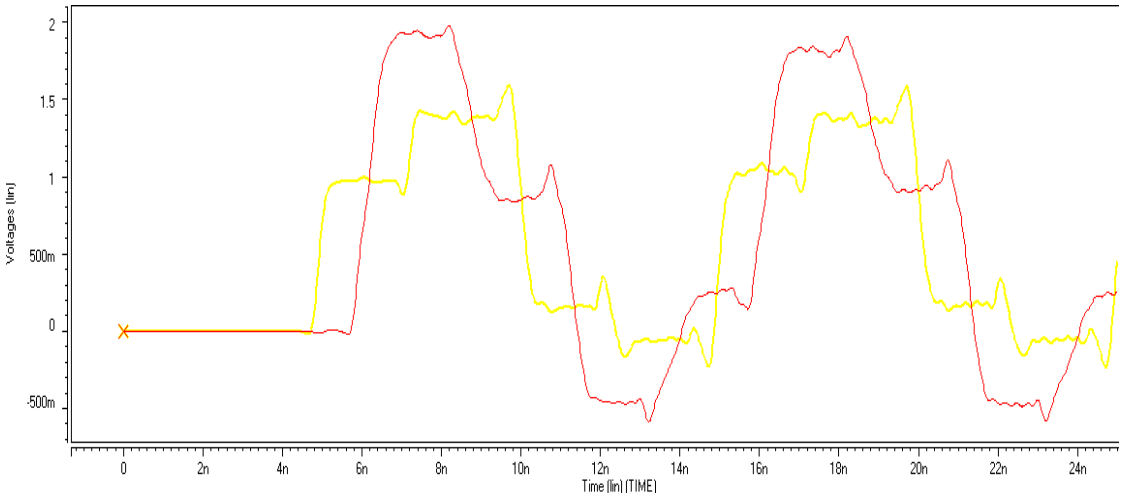

Figure 5-13. 1.2V LVCMOS (Row I/O DIFFIO pin (Optional Pin Function), 8mA Drive Strength, Fast Slew Rate) IBIS Model Simulation Result at Fast Conditions.

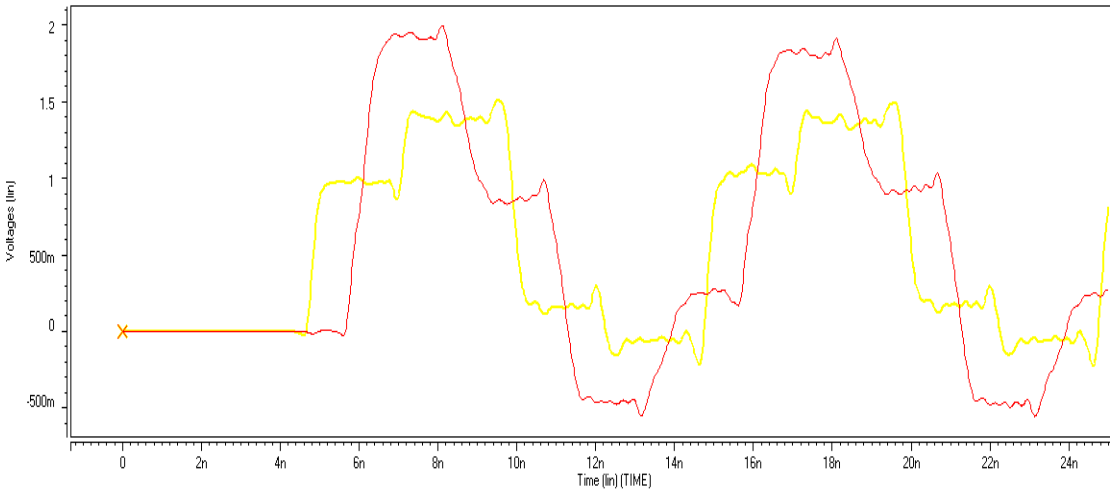

Figure 5-14. 1.2V LVCMOS (Row I/O DIFFIO pin (Optional Pin Function), 8mA Drive Strength, Fast Slew Rate) HSPICE Model Simulation Result at Fast Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.37	2.36	0.4
Fall time	2.37	2.38	0.4

Table 5-5 1.2V LVCMOS (Row I/O DIFFIO pin (Optional Pin Function), 8mA Drive Strength, Fast Slew Rate) IBIS Simulation Vs HSPICE Simulation Result at Fast Conditions

6.0 3.0V PCI and PCI-X Verification

Following shows the correlation between IBIS simulation and HSPICE simulation for 3.0V PCI and PCI-X standard.

6.1 3.0V PCI and PCI-X

Figure 6-1 and 6-2 shows the simulation setup for 3.0V PCI and PCI-X IBIS output model and HSPICE output model.

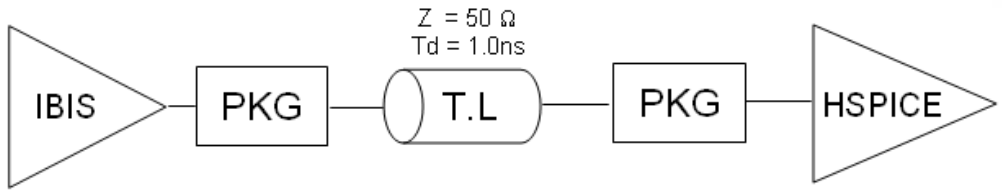

Figure 6-1. 3.0V PCI and PCI-X IBIS Model Simulation Setup

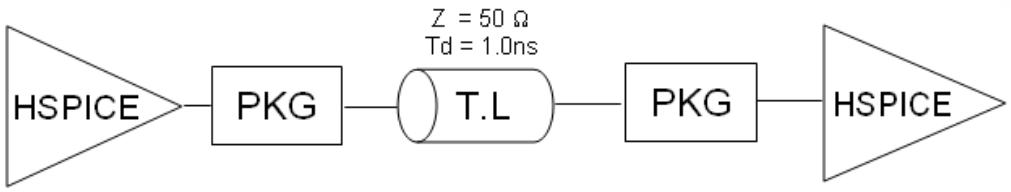

Figure 6-2. 3.0V PCI and PCI-X HSPICE Model Simulation Setup

6.1.1 Row I/O – PCI-X Standard, Typical Conditions

Figures 6-3 and 6-4 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 6-1 shows comparison between the two measurements.

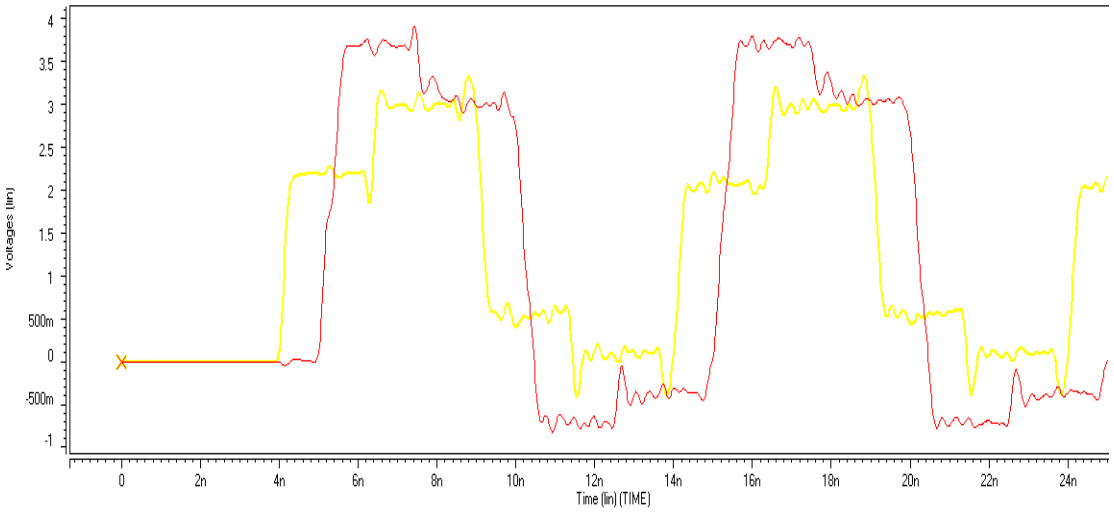

Figure 6-3. 3.0V PCI-X IBIS Model Simulation Result at Typical Conditions.

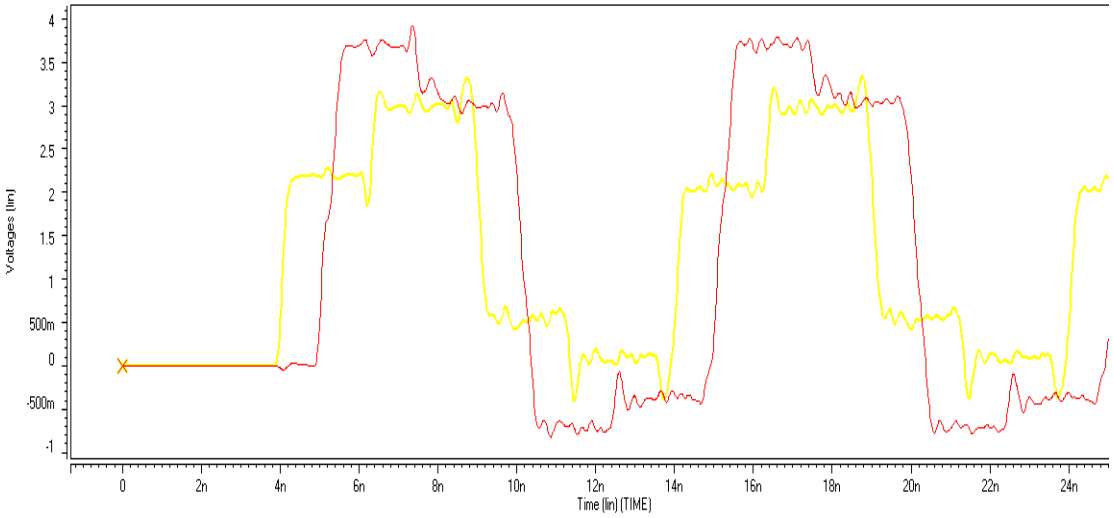

Figure 6-4. 3.0V PCI-X HSPICE Model Simulation Result at Typical Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (ns)
Rise time	2.39	2.39	0.0
Fall time	2.37	2.37	0.0

Table 6-1. 3.0V PCI-X IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

6.1.2 Column I/O – PCI Standard, Slow Conditions

Figures 6-5 and 6-6 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 6-2 shows comparison between the two measurements.

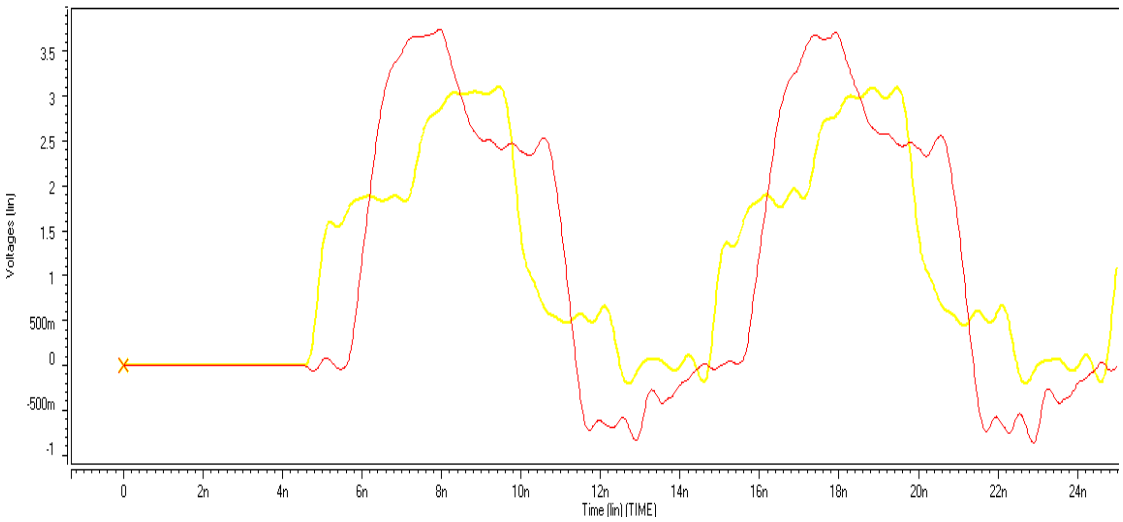

Figure 6-5. 3.0V PCI IBIS Model Simulation Result at Slow Conditions

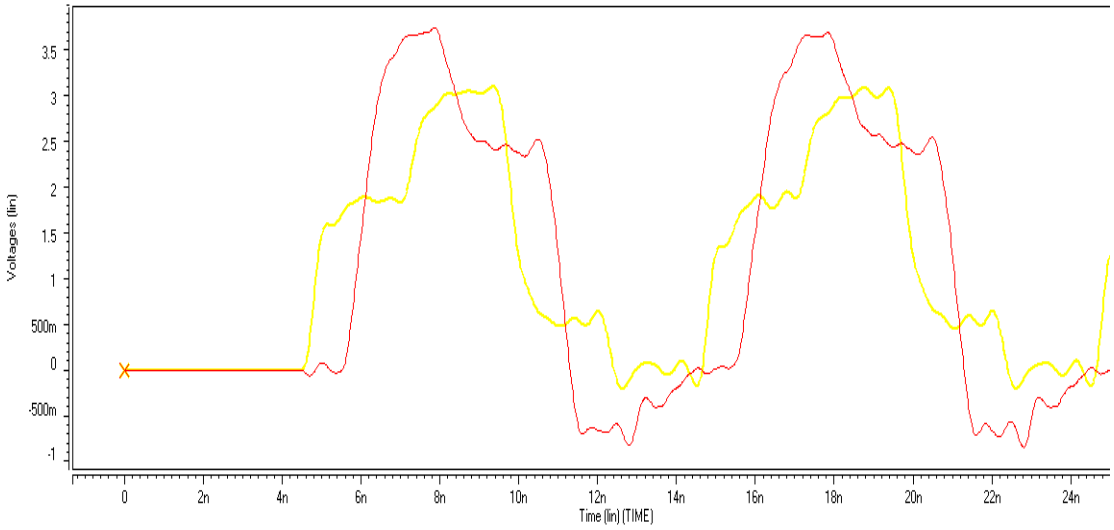

Figure 6-6. 3.0V PCI HSPICE Model Simulation Result at Slow Conditions

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	2.77	2.78	0.4
Fall time	2.64	2.64	0.0

Table 6-2. 3.0V PCI IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

7.0 2.5V LVDS Verification

Following shows the correlation between IBIS simulation and HSPICE simulation for 2.5V Differential LVDS standard.

7.1 2.5V LVDS Standard with Pre-Emphasis ON, Typical Conditions

Figure 7-1 and 7-2 shows the simulation setup for 2.5V Differential LVDS standard with Pre-emphasis ON.

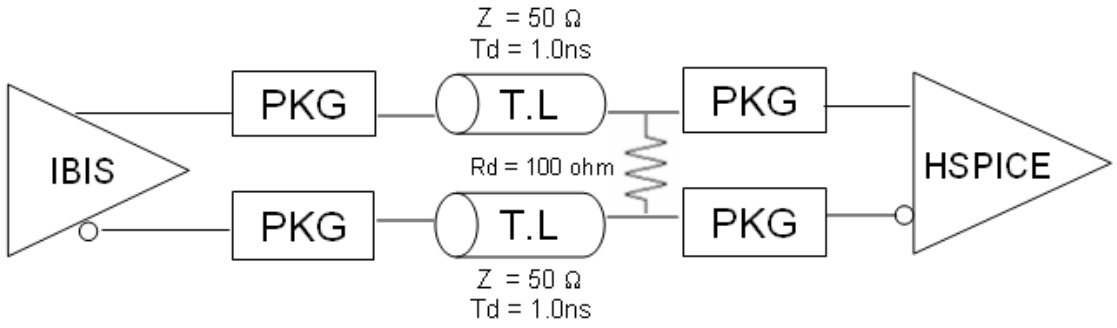

Figure 7-1. 2.5V LVDS Standard with Pre-Emphasis ON IBIS Model Simulation Setup

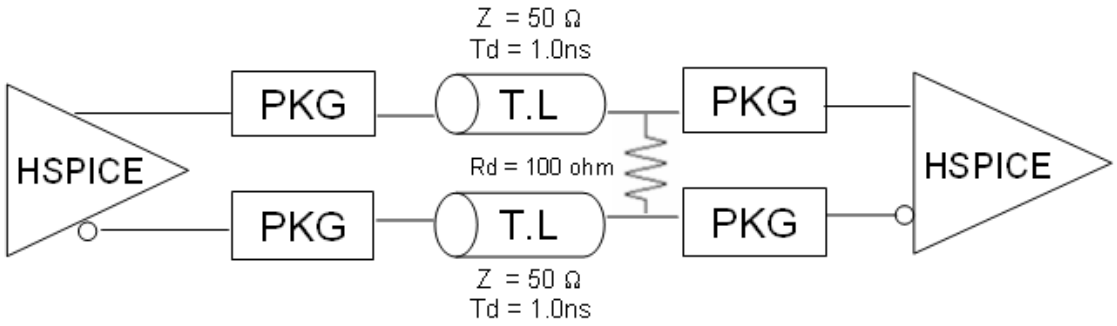

Figure 7-2. 2.5V LVDS Standard with Pre-Emphasis ON HSPICE Model Simulation Setup

7.1.1 Row I/O –2.5V LVDS standard with Pre-emphasis ON, Typical Conditions

Figures 7-3 and 7-4 show the simulation setup for 2.5V Differential LVDS standard with Pre-emphasis ON for IBIS output model and HSPICE output model. In the simulations, the measurement is obtained at the transmitter end, positive pin. **RED** curve indicates the negative pin and **YELLOW** curve indicating on the positive pin.

Table 7-1 shows comparison between the two measurements.

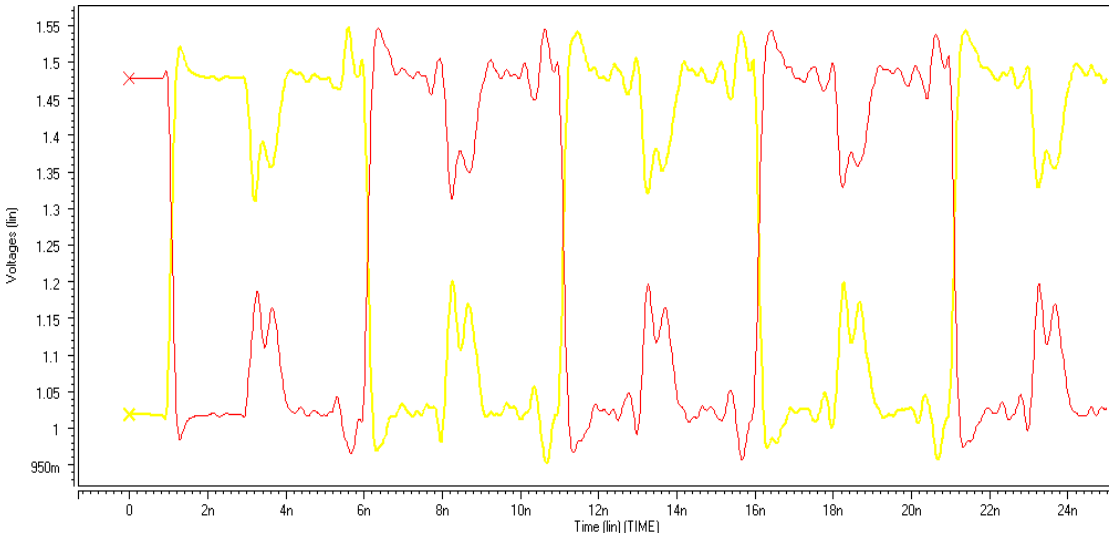

Figure 7-3. 2.5V LVDS standard with Pre-emphasis ON IBIS Simulation Result at Typical Conditions

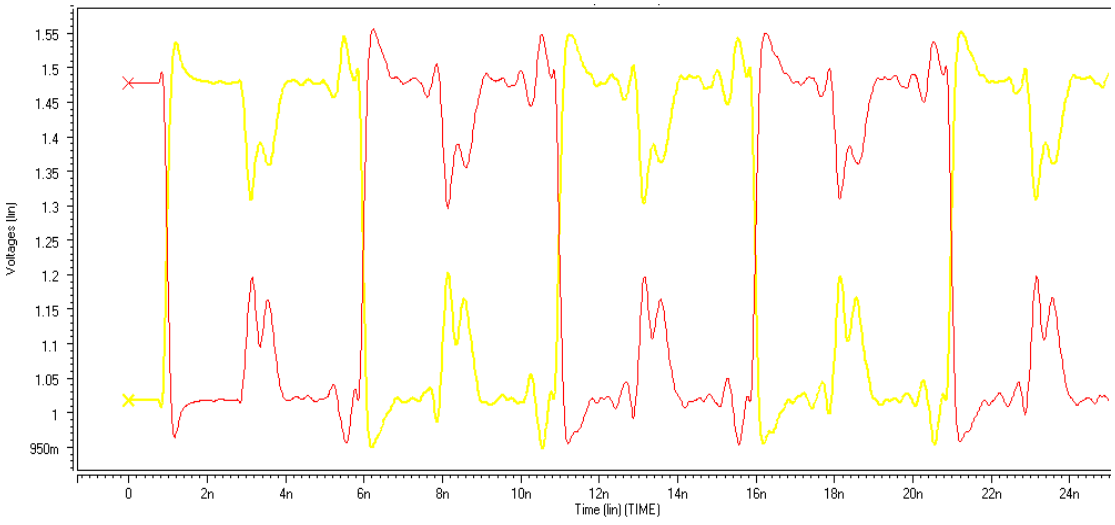

Figure 7-4. 2.5V LVDS standard with Pre-emphasis ON HSPICE Simulation Result at Typical Conditions

Parameters	IBIS model (ns)	HSPICE model (ns)	Differences (%)
Rise time	0.17	0.16	6.3
Fall time	0.16	0.15	6.7

Table 7-1. 2.5V LVDS standard with Pre-emphasis ON IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

7.2 2.5V LVDS Standard with Pre-Emphasis OFF, Slow Conditions

Figure 7-5 and 7-6 shows the simulation setup for 2.5V Differential LVDS standard with Pre-emphasis OFF.

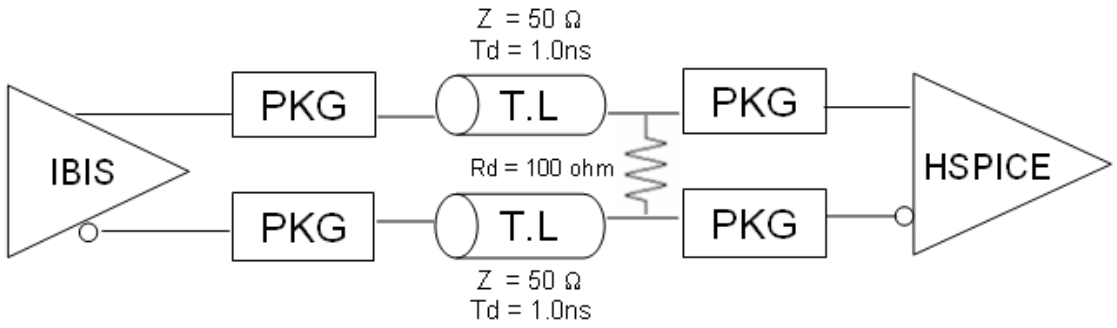

Figure 7-5. 2.5V LVDS Standard with Pre-Emphasis OFF IBIS Model Simulation Setup

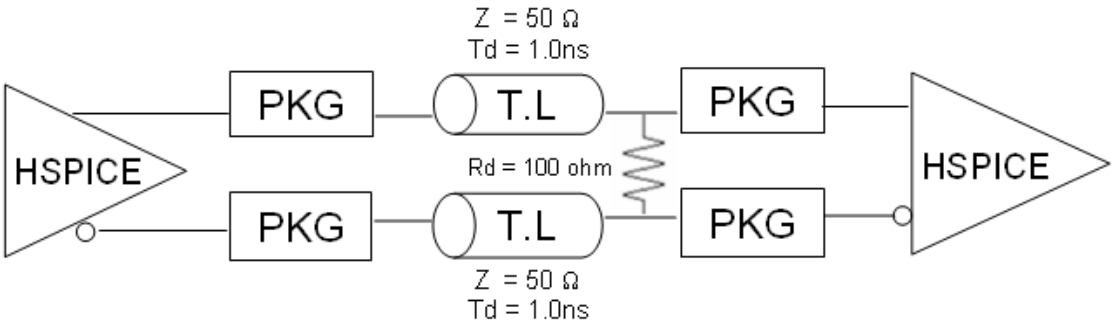

Figure 7-6. 2.5V LVDS Standard with Pre-Emphasis OFF HSPICE Model Simulation Setup

7.2.1 Row I/O –2.5V LVDS standard with Pre-emphasis OFF, Slow Conditions

Figures 7-7 and 7-8 show the simulation setup for 2.5V Differential LVDS standard with Pre-emphasis OFF for IBIS output model and HSPICE output model. In the simulations, the measurement is obtained at the transmitter end, positive pin. **RED** curve indicates the negative pin and **YELLOW** curve indicating on the positive pin.

Table 7-2 shows comparison between the two measurements.

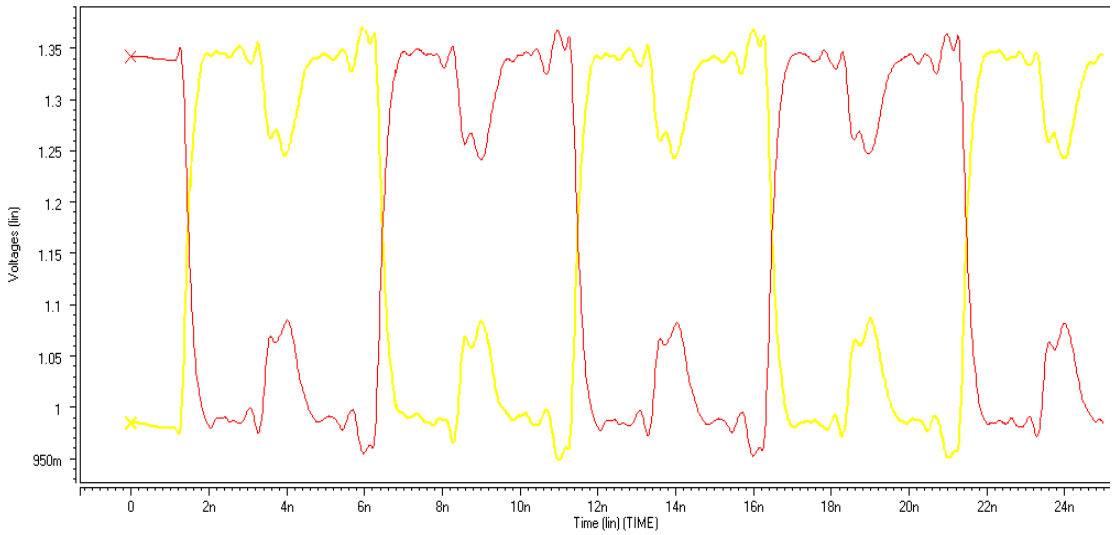

Figure 7-7. 2.5V LVDS standard with Pre-emphasis OFF IBIS Simulation Result at Slow Conditions

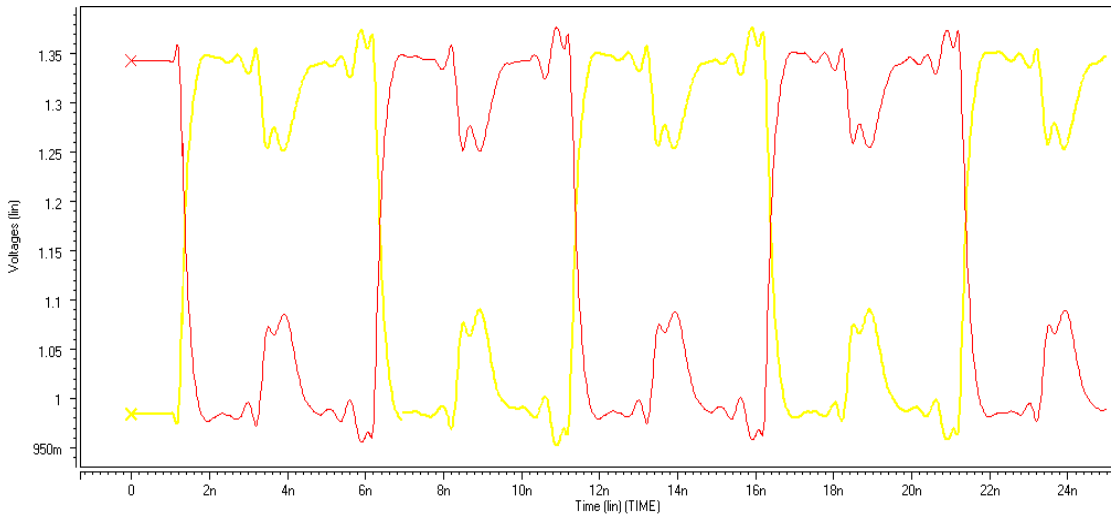

Figure 7-8. 2.5V LVDS standard with Pre-emphasis OFF HSPICE Simulation Result at Slow Conditions

Parameters	IBIS model (ns)	HSPICE model (ns)	Differences (%)
Rise time	0.37	0.35	5.7
Fall time	0.39	0.38	2.6

Table 7-2. 2.5V LVDS standard with Pre-emphasis OFF IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

7.3 2.5V Pseudo-LVDS Standard with 3 External Resistors Network (Row Output), Fast Conditions

Figure 7-9 and 7-10 shows the simulation setup for 2.5V Pseudo-LVDS standard with 3 External Resistors Network.

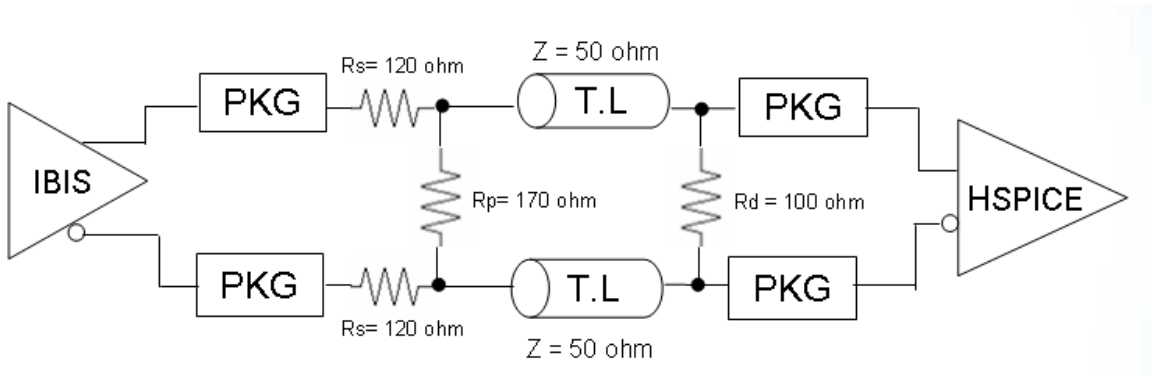

Figure 7-9. 2.5V Pseudo-LVDS Standard with 3 External Resistors Network (Row Output) IBIS Model Simulation Setup

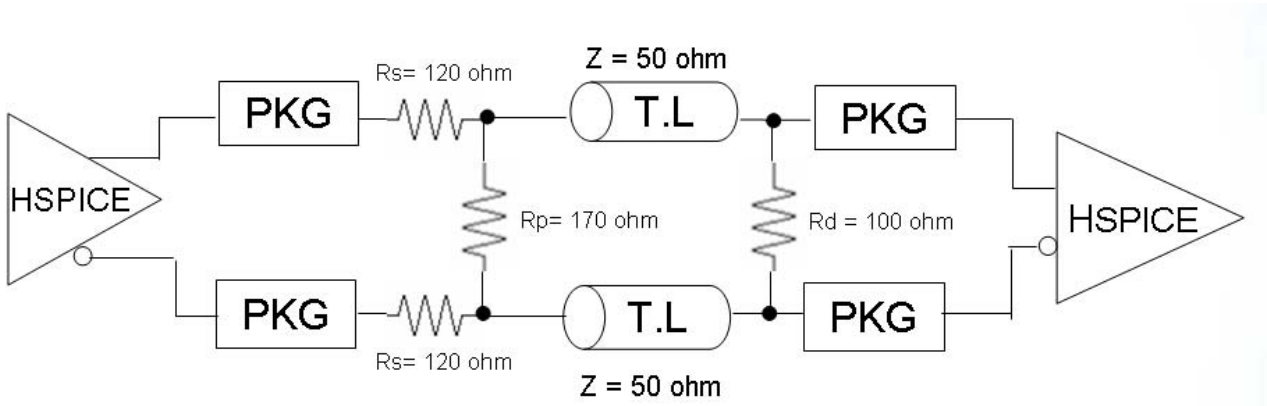

Figure 7-10. 2.5V Pseudo-LVDS Standard with 3 External Resistors Network (Row Output) HSPICE Model Simulation Setup

7.3.1 Row Output – 2.5V Pseudo-LVDS standard with 3 External Resistors Network, Fast Conditions

Figures 7-11 and 7-12 show the simulation setup for 2.5V Pseudo-LVDS with 3 external resistors network IBIS output model and HSPICE output model. In the simulations, the measurement is obtained at the transmitter end, positive pin. **RED** curve indicates the negative pin and **YELLOW** curve indicating on the positive pin.

Table 7-3 shows comparison between the two measurements.

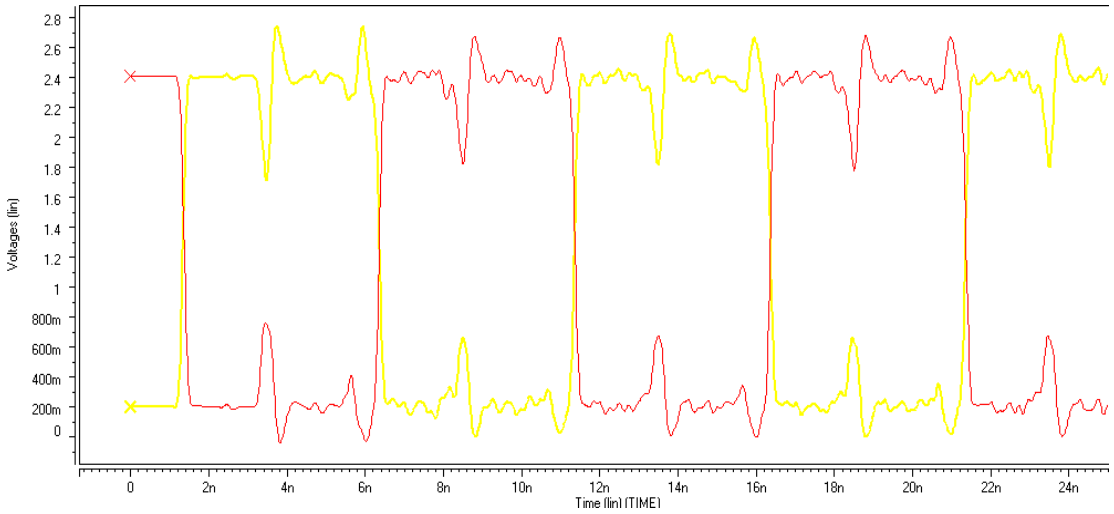

Figure 7-11. 2.5V Pseudo-LVDS standard with 3 External Resistors Network (Row Output) IBIS Simulation Result at Fast Conditions

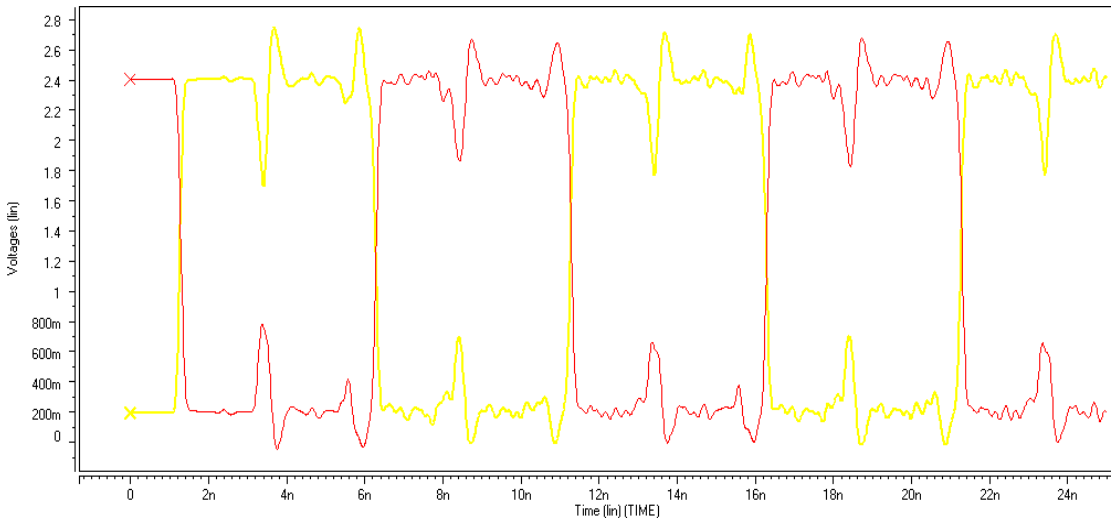

Figure 7-12. 2.5V Pseudo-LVDS standard with 3 External Resistors Network (Row Output) HSPICE Simulation Result at Fast Conditions

Parameters	IBIS model (ns)	HSPICE model (ns)	Differences (%)
Rise time	0.18	0.19	5.3
Fall time	0.24	0.23	4.3

Table 7-3. 2.5V Pseudo-LVDS standard with 3 External Resistors Network (Row Output) IBIS Simulation Vs HSPICE Simulation Result at Fast Conditions

7.4 2.5V Pseudo-LVDS Standard with 3 External Resistors Network (Column Output), Slow Conditions

Figure 7-13 and 7-14 shows the simulation setup for 2.5V Pseudo-LVDS standard with 3 External Resistors Network.

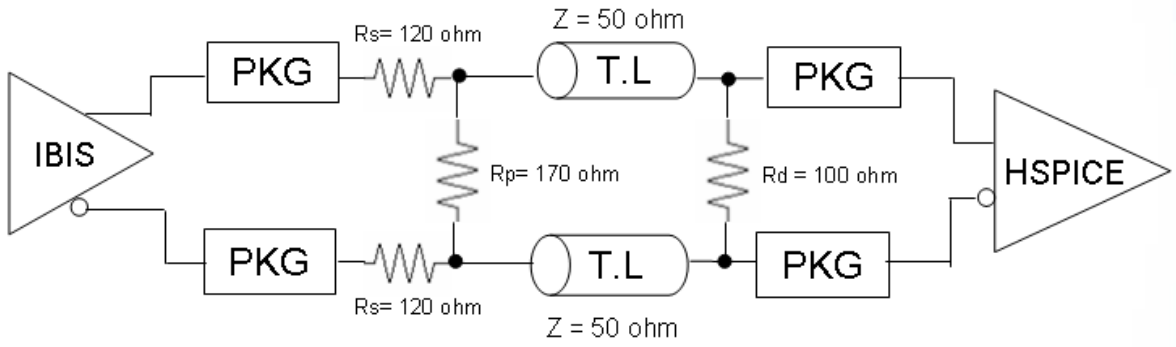

Figure 7-13. 2.5V Pseudo-LVDS Standard with 3 External Resistors Network (Column Output) IBIS Model Simulation Setup

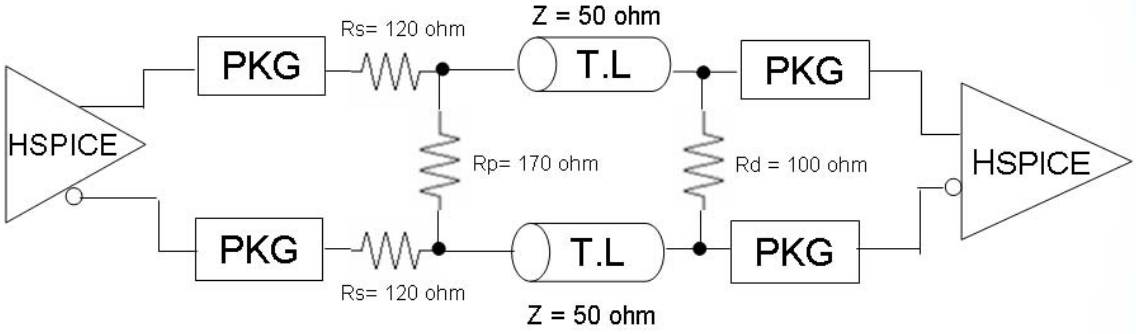

Figure 7-14. 2.5V Pseudo-LVDS Standard with 3 External Resistors Network (Column Output) HSPICE Model Simulation Setup

7.4.1 Column Output – 2.5V Pseudo-LVDS standard with 3 External Resistors Network, Slow Conditions

Figures 7-15 and 7-16 show the simulation setup for 2.5V Pseudo-LVDS with 3 external resistors network IBIS output model and HSPICE output model. In the simulations, the measurement is obtained at the transmitter end, positive pin. **RED** curve indicates the negative pin and **YELLOW** curve indicating on the positive pin.

Table 7-4 shows comparison between the two measurements.

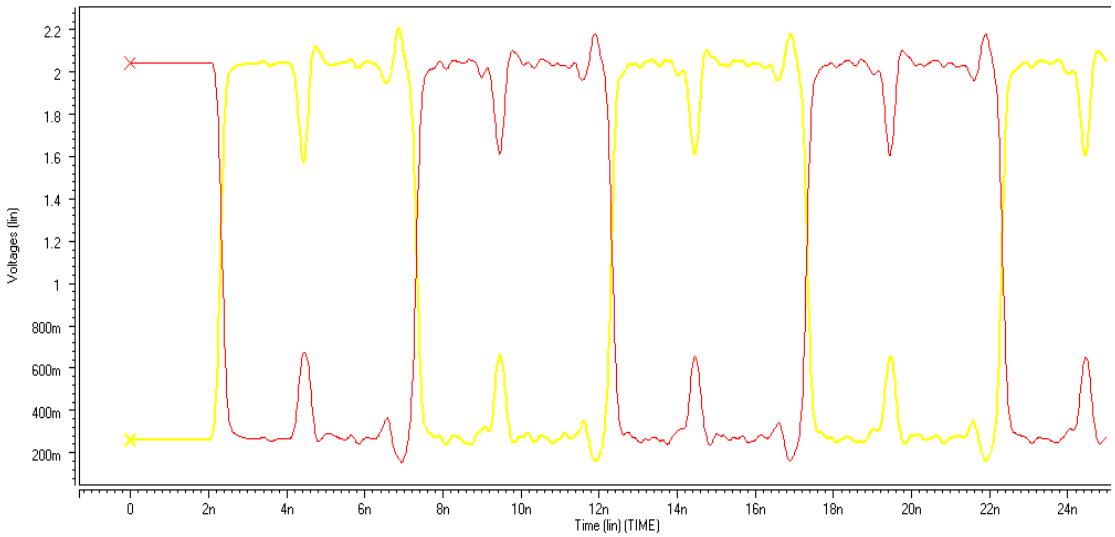

Figure 7-15. 2.5V Pseudo-LVDS standard with 3 External Resistors Network (Column Output) IBIS Simulation Result at Slow Conditions

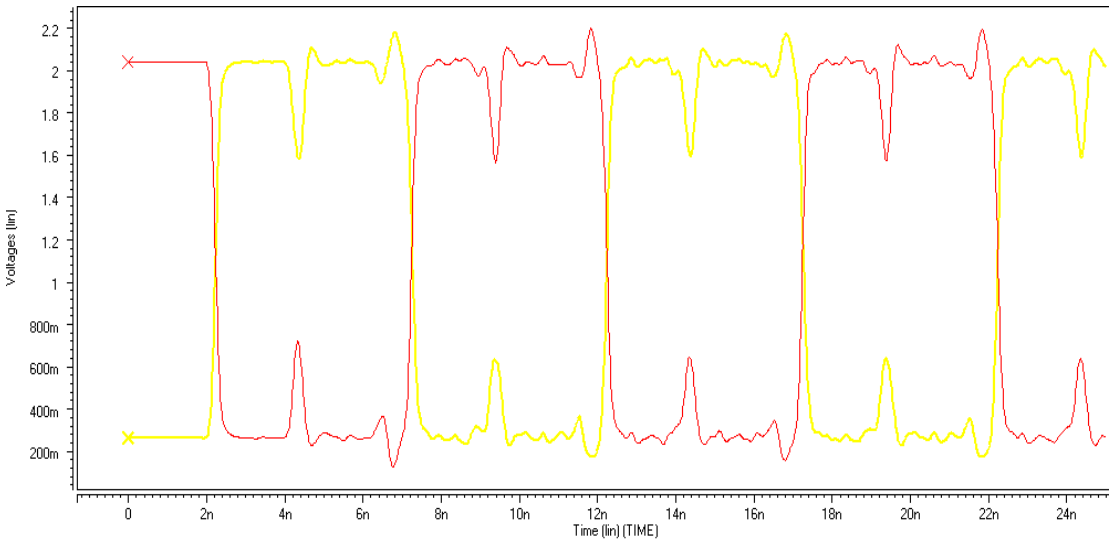

Figure 7-16. 2.5V Pseudo-LVDS standard with 3 External Resistors Network (Column Output) HSPICE Simulation Result at Slow Conditions

Parameters	IBIS model (ns)	HSPICE model (ns)	Differences (ns)
Rise time	0.25	0.25	0.0
Fall time	0.29	0.29	0.0

Table 7-4. 2.5V Pseudo-LVDS standard with 3 External Resistors Network (Column Output) IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

8.0 Input Models Verification

Following shows the correlation between IBIS simulation and HSPICE simulation for Input Models with PCI-diode enabled and disabled.

8.1 3.0V LVTTL with PCI-diode Disabled, Typical Conditions

Figure 8-1 and 8-2 shows the simulation setup for 3.0V LVTTL IBIS input model and HSPICE input model with PCI-diode disabled.

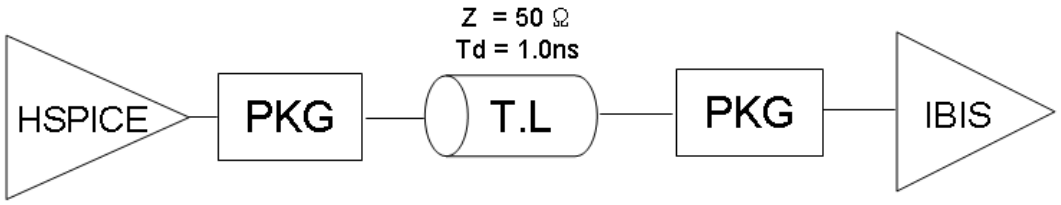

Figure 8-1. 3.0V LVTTL IBIS Input Model with PCI-diode Disabled Simulation Setup

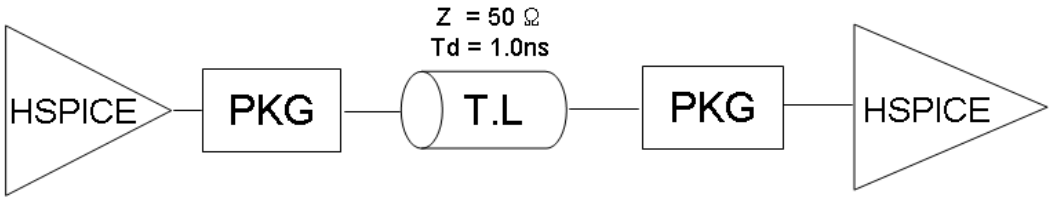

Figure 8-2. 3.0V LVTTL HSPICE Input Model with PCI-diode Disabled Simulation Setup

8.1.1 Column I/O – 3.0V LVTTL Input Model with PCI-diode Disabled, Typical Conditions

Figures 8-3 and 8-4 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 8-1 shows comparison between the two measurements.

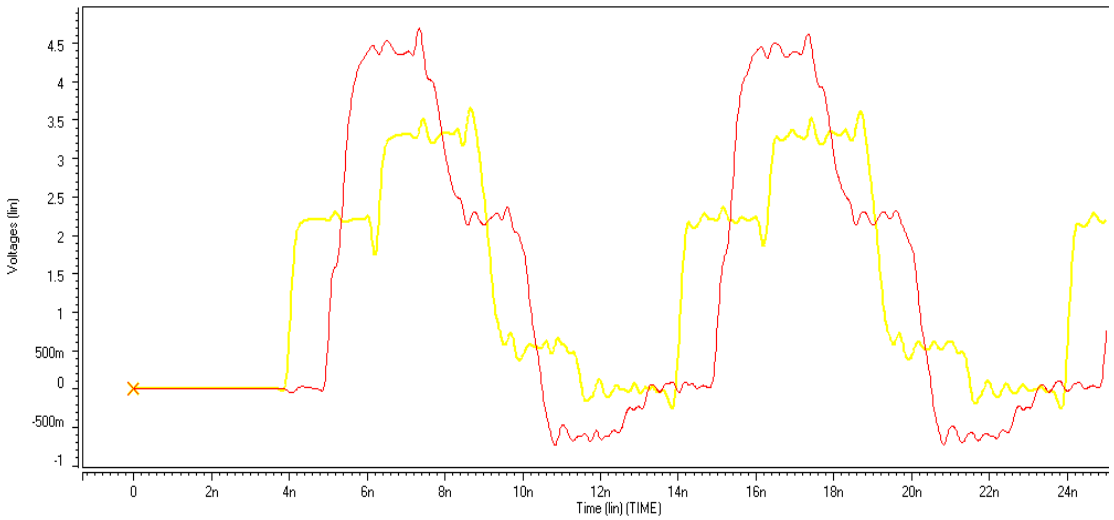

Figure 8-3. 3.0V LVTTL IBIS Input Model with PCI-diode Disabled Simulation Result at Typical Conditions.

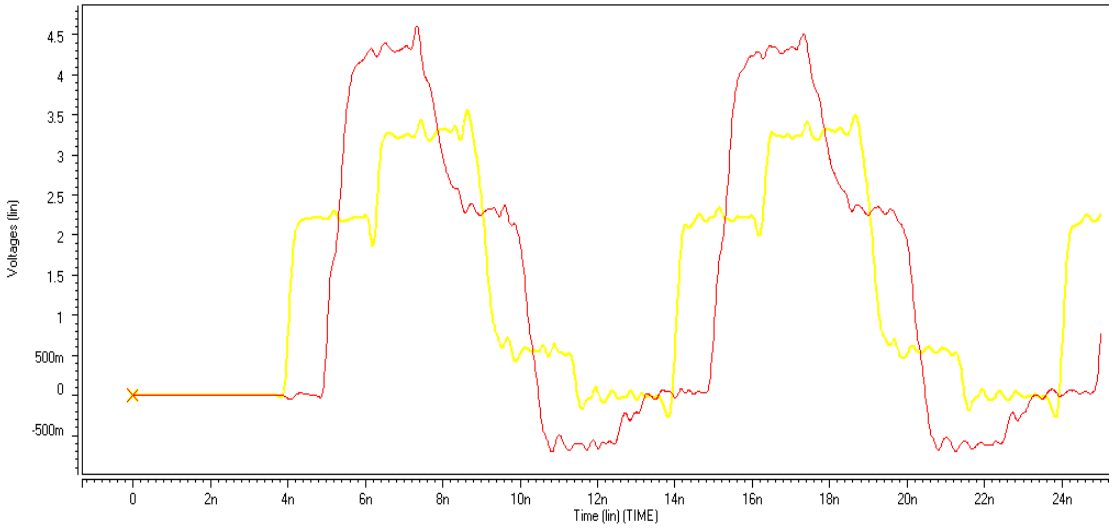

Figure 8-4. 3.0V LVTTL HSPICE Input Model with PCI-diode Disabled Simulation Result at Typical Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	0.45	0.43	4.7
Fall time	2.27	2.23	1.8

Table 8-1. 3.0V LVTTL Input Models with PCI-diode Disabled IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

8.2 3.0V LVTTL with PCI-diode Enabled, Typical Conditions

Figure 8-5 and 8-6 shows the simulation setup for 3.0V LVTTL IBIS input model and HSPICE input model with PCI-diode enabled.

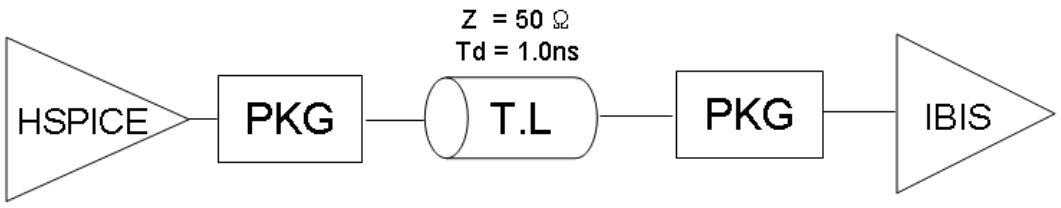

Figure 8-5. 3.0V LVTTL IBIS Input Model with PCI-diode Enabled Simulation Setup

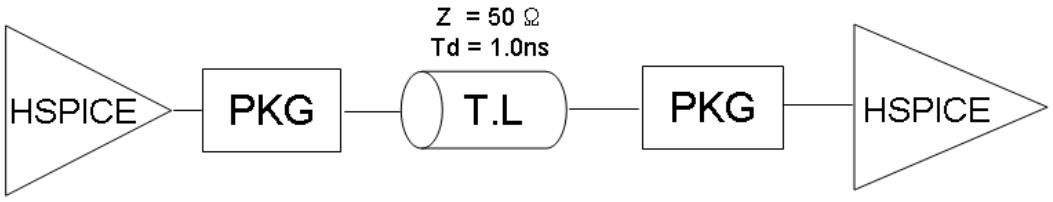

Figure 8-6. 3.0V LVTTL HSPICE Input Model with PCI-diode Enabled Simulation Setup

8.2.1 Column I/O – 3.0V LVTTL Input Model with PCI-diode enabled, Typical Conditions

Figures 8-7 and 8-8 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 8-2 shows comparison between the two measurements.

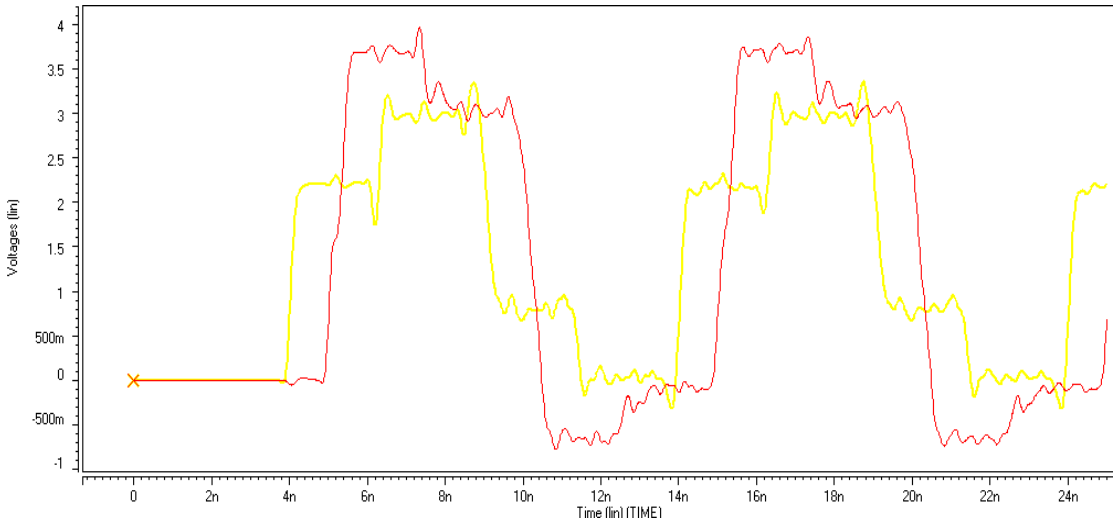

Figure 8-7. 3.0V LVTTL IBIS Input Model with PCI-diode Enabled Simulation Result at Typical Conditions.

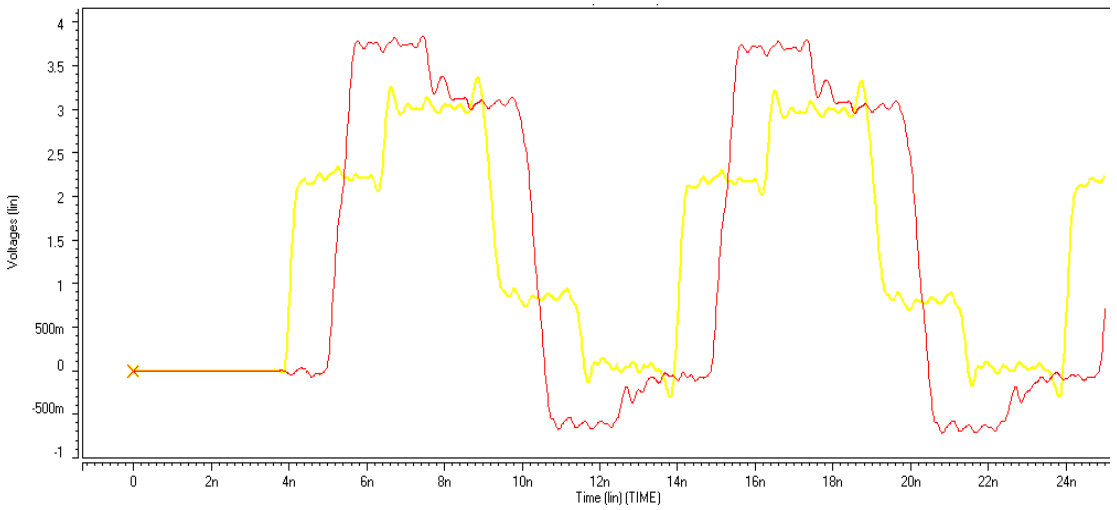

Figure 8-8. 3.0V LVTTL HSPICE Input Model with PCI-diode Enabled Simulation Result at Typical Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	0.45	0.43	4.7
Fall time	0.53	0.51	3.9

Table 8-2. 3.0V LVTTL Input Models with PCI-diode Enabled IBIS Simulation Vs HSPICE Simulation Result at Typical Conditions

8.3 2.5V LVTTL with PCI-diode Disabled, Slow Conditions

Figure 8-9 and 8-10 shows the simulation setup for 2.5V LVTTL IBIS input model and HSPICE input model with PCI-diode disabled.

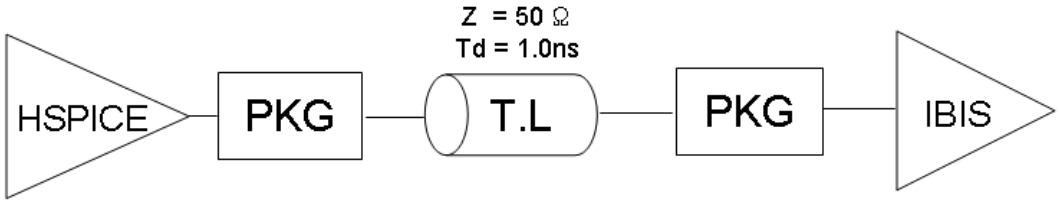

Figure 8-9. 2.5V LVTTL IBIS Input Model with PCI-diode Disabled Simulation Setup

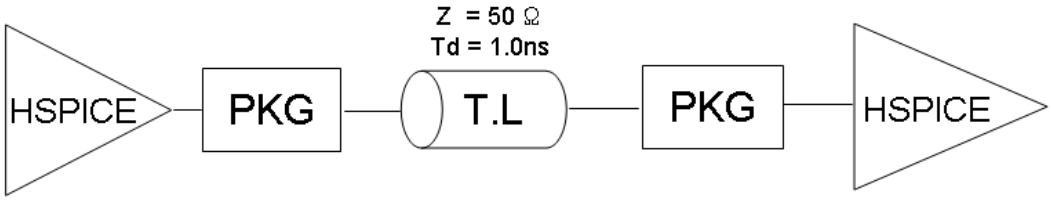

Figure 8-10. 2.5V LVTTL HSPICE Input Model with PCI-diode Disabled Simulation Setup

8.3.1 Row I/O – 2.5V LVTTL Input Model with PCI-diode Disabled, Slow Conditions

Figures 8-11 and 8-12 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 8-3 shows comparison between the two measurements.

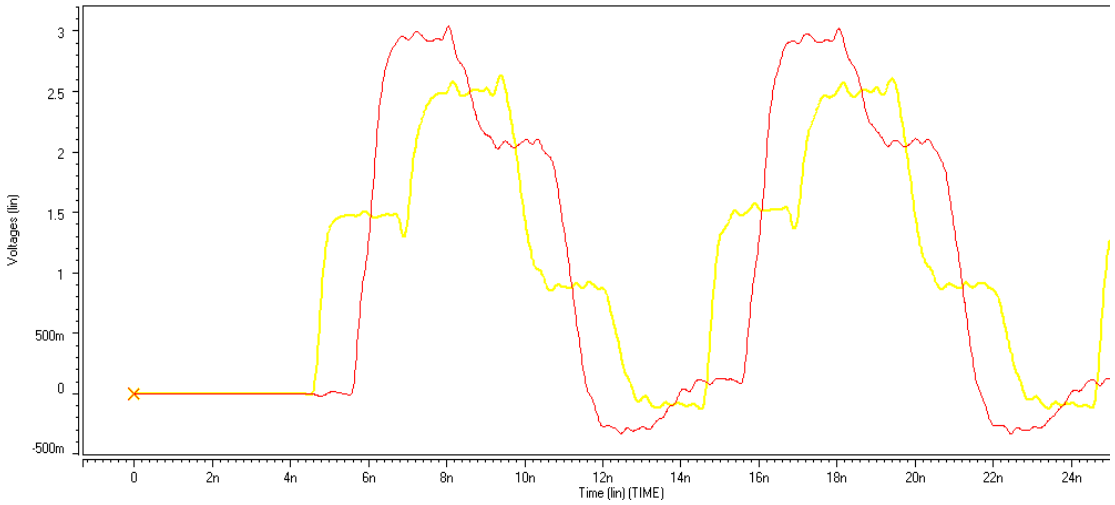

Figure 8-11. 2.5V LVTTL IBIS Input Model with PCI-diode Disabled Simulation Result at Slow Conditions.

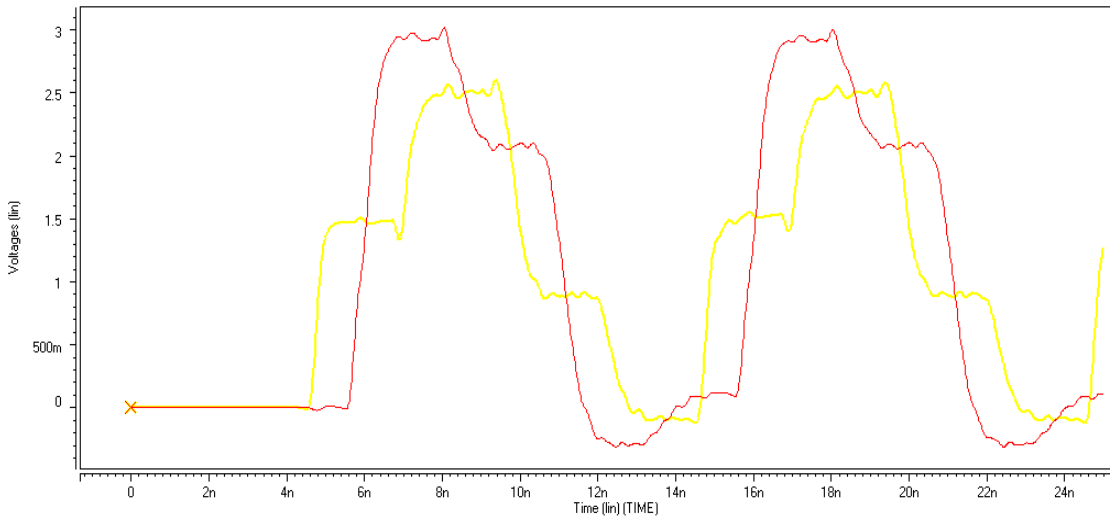

Figure 8-12 2.5V LVTTL HSPICE Input Model with PCI-diode Disabled Simulation Result at Slow Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	0.72	0.72	0.0
Fall time	2.95	2.98	0.3

Table 8-3. 2.5V LVTTL Input Models with PCI-diode Disabled IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

8.4 2.5V LVTTL with PCI-diode Enabled, Slow Conditions

Figure 8-13 and 8-14 shows the simulation setup for 2.5V LVTTL IBIS input model and HSPICE input model with PCI-diode enabled.

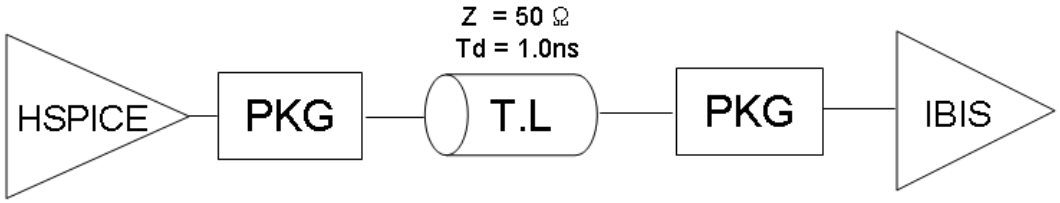

Figure 8-13. 2.5V LVTTL IBIS Input Model with PCI-diode Enabled Simulation Setup

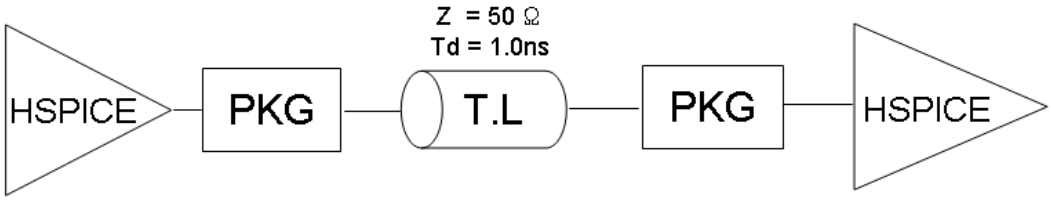

Figure 8-14. 2.5V LVTTL HSPICE Input Model with PCI-diode Enabled Simulation Setup

8.4.1 Row I/O – 2.5V LVTTL Input Model with PCI-diode enabled, Slow Conditions

Figures 8-15 and 8-16 show the IBIS and HSPICE results for this model in Star-HSPICE. Table 8-4 shows comparison between the two measurements.

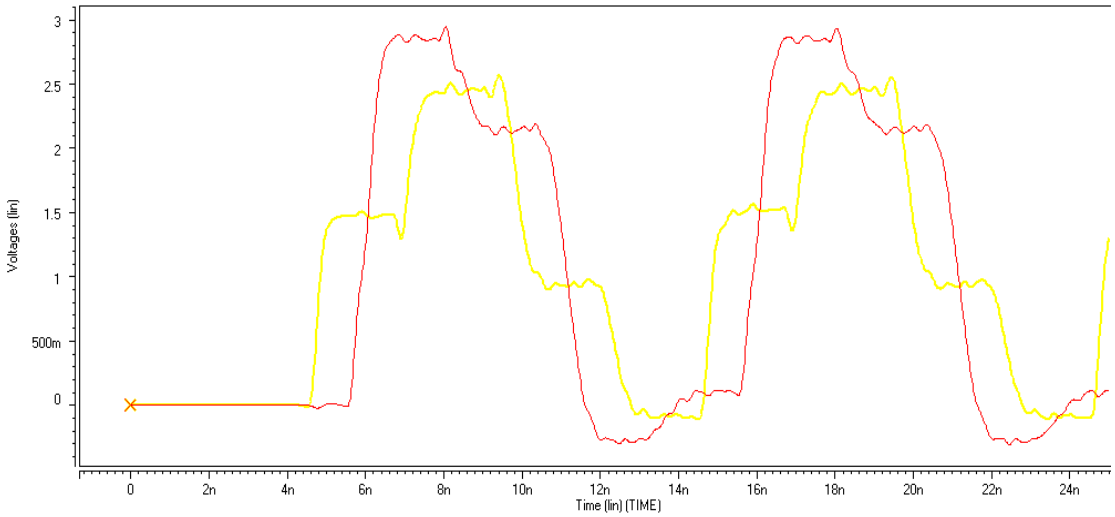

Figure 8-15. 2.5V LVTTL IBIS Input Model with PCI-diode Enabled Simulation Result at Slow Conditions.

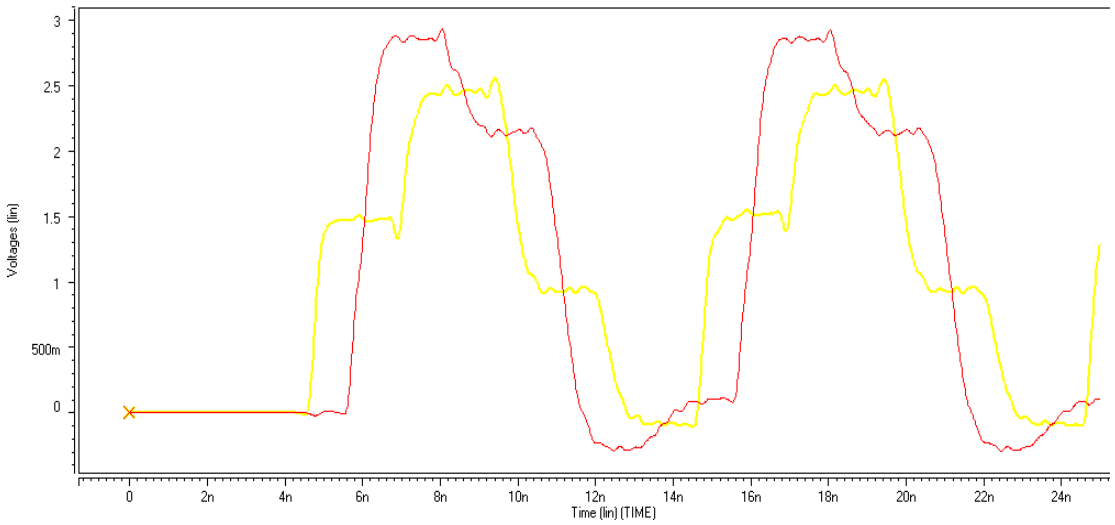

Figure 8-16. 2.5V LVTTL HSPICE Input Model with PCI-diode Enabled Simulation Result at Slow Conditions.

Parameters	IBIS Model (ns)	HSPICE Model (ns)	Differences (%)
Rise time	0.68	0.69	1.4
Fall time	2.94	2.93	0.3

Table 8-4. 2.5V LVTTL Input Models with PCI-diode Enabled IBIS Simulation Vs HSPICE Simulation Result at Slow Conditions

9.0 Conclusion

The purpose of this document is to show the accuracy of Cyclone IV IBIS Models by correlating them against the HSPICE Models. As the results indicate, the IBIS Models correlate well to the HSPICE Models.

10.0 Cyclone IV IBIS Model Correlation Report Revision History

File rev. 1.0
Correlated for: Cyclone IV IBIS Model Rev 2.0 < cyclone4.ibs>
Date Release: July 2010