iMX6 Rex

Variant: Variant name not interpreted

28/04/2013
V1I1

PRELIMINARY

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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iMX6 Rex

(Block Diagram)

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POWERS

- PMIC 1
- PMIC 2
- PMIC 3

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CPU

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ETHERNET PHY

Ethernet

Ethernet PHY, LEDs

Page 3

BOARD CONNECTOR 1

HDMI

SD card

SPI2

USB OTG

UART1

I2C4

Page 4

DDR3 MEMORIES

Page 14

SPI FLASH

SPI1

Page 3

BOARD CONNECTOR 2

Audio

LVDS0

MMC card

SATA

PCIE

USB HOST

UART2

JTAG

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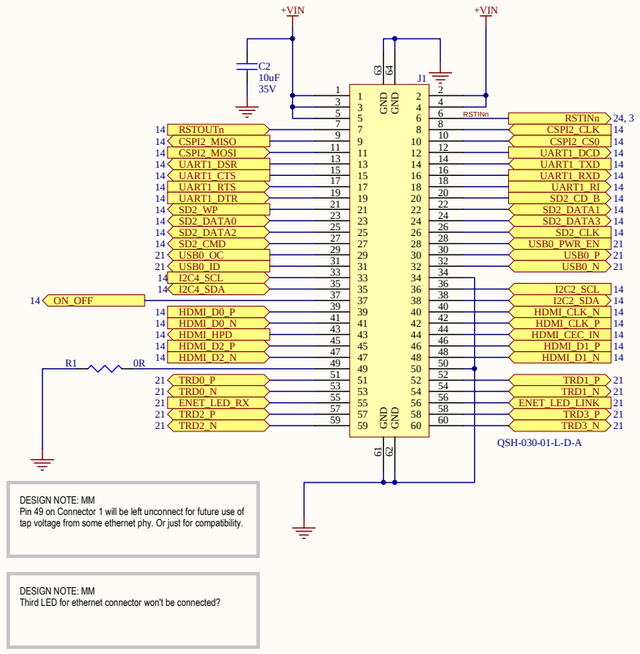
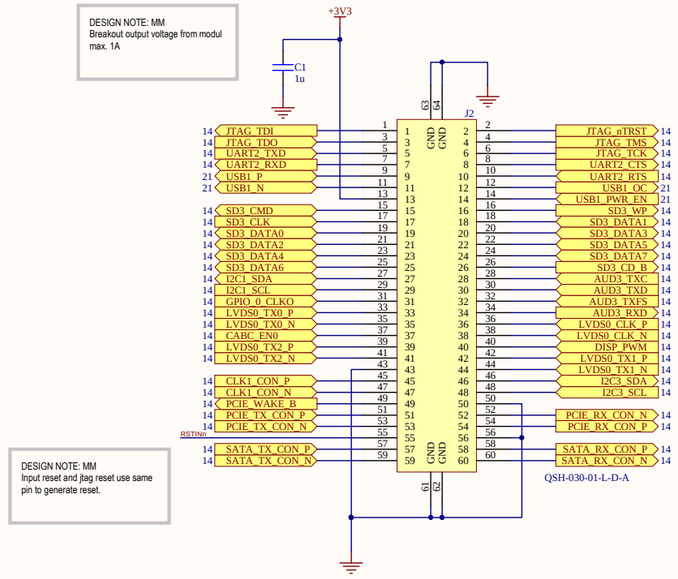
CONNECTORS

BOARD TO BOARD CONNECTORS





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Page Contents:	[03] - CONNECTORS.SchDoc		Checked by
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CPU - DDR3, DDR3

Clock terminators: Place at end of route at each DDR pair

DDR0_CLK0_P — R2 200R — DDR0_CLK0_N

DDR0_CLK1_P — R3 200R — DDR0_CLK1_N

ClassName: DDR0_ADDR_CTRL
Net Class

U1C

ClassName: DDR0_BANK0 / Net Class 1
ClassName: DDR0_BANK1 / Net Class 1
ClassName: DDR0_BANK2 / Net Class 1
ClassName: DDR0_BANK3 / Net Class 1
ClassName: DDR0_BANK4 / Net Class 1
ClassName: DDR0_BANK5 / Net Class 1
ClassName: DDR0_BANK6 / Net Class 1
ClassName: DDR0_BANK7 / Net Class 1

DRAM_D0 … DRAM_D63
DRAM_SDQS0 … DRAM_SDQS7 (DIFF90)
DRAM_DQM0 … DRAM_DQM7
DRAM_A0 … DRAM_A15
DRAM_SDBA0 … DRAM_SDBA2
DRAM_CS0 … DRAM_CS1
DRAM_RAS
DRAM_CAS
DRAM_SDWE
DRAM_SDCKE0 … DRAM_SDCKE1
DRAM_SDODT0 … DRAM_SDODT1
DRAM_RESET
DRAM_SDCLK_0 … DRAM_SDCLK_1 (DIFF90)
NVCC_DRAM_1 … NVCC_DRAM_13
DRAM_VREF — AC2
ZQPAD — AE17 — R10 240R — +DDR_VREF — C7 100n
R6 10k
R7 10k

MCIMX6Q5EYM10AC

U2 / U3 / U4 / U5 — 2G_DDR3_SDRAM_128MX16 — MT41J128M16HA-15E:D TR

+1V5_DDR
+DDR_VREF
R4 240R
R5 240R
R8 240R
R9 240R
C3 220n
C4 220n
C5 220n
C6 220n
C8 220n
C9 220n
C10 220n
C11 220n

Note 1

C12 22u
C13 22u
C14 22u
C15 22u
C16 22u
C17 22u

C21 220n
C22 220n
C23 220n
C24 220n
C25 220n
C26 220n
C27 220n
C28 220n
C29 220n
C30 220n
C31 220n
C32 220n
C33 220n
C34 220n
C35 220n
C36 220n
C37 220n
C38 220n
C39 220n
C40 220n
C41 220n
C42 220n
C43 220n
C44 220n
C45 220n
C46 220n
C47 220n
C48 220n
C49 220n
C50 220n
C51 220n
C52 220n
C53 220n
C54 220n
C55 220n
C56 220n
C57 220n
C58 220n
C59 220n
C60 220n

R11 240R
R12 240R
C18 100n
C19 10u
C20 100n

DESIGN NOTE:
Pull down resistor RX3 is added to trace SDCKE0 in Rev B4 by soldering to an existing open via. Change will be made permanent in layout with the Rev C board.

DESIGN NOTE:
Using bit swapping for DATA bus to allow easy pcb routing.

DESIGN NOTE:
When using data bit swapping the low order bit of eachbyte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration. Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

DESIGN NOTE:
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.

DESIGN NOTE: MM
C which bypass +1V5_DDR and gnd selected for 6V3 max

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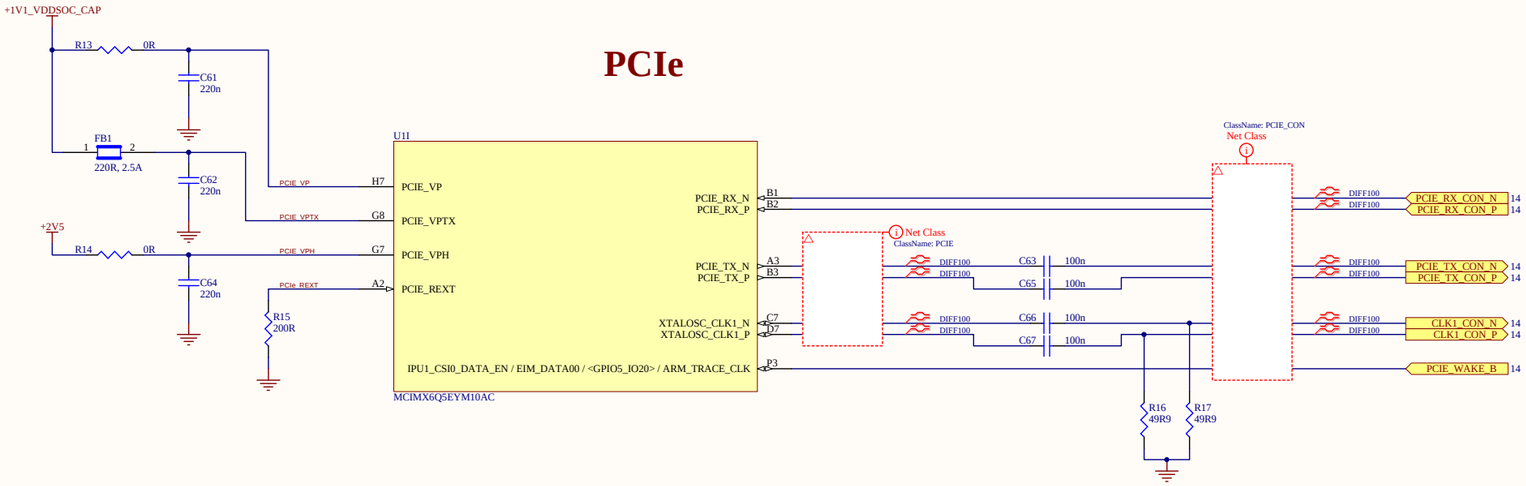
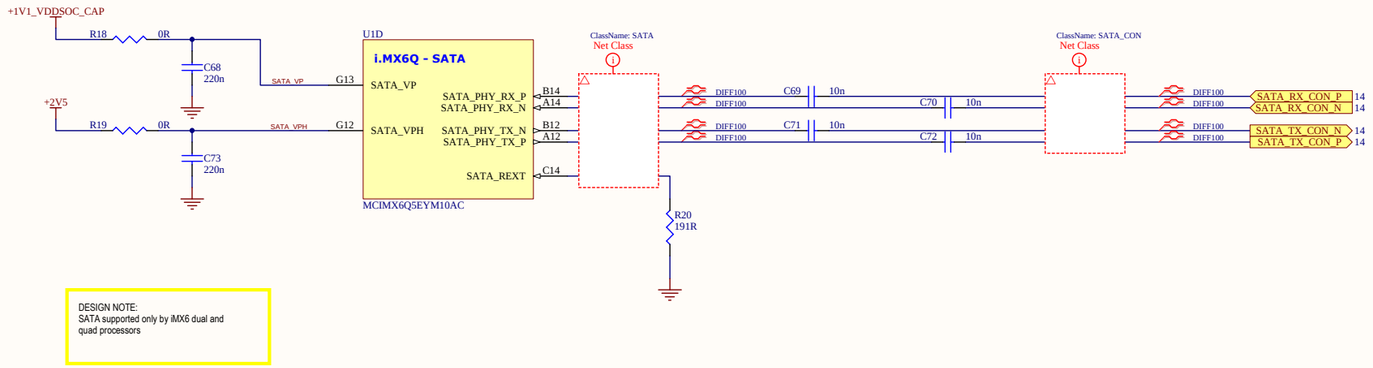
CPU - SATA, PCIe

PCIe



SATA



DESIGN NOTE:
SATA supported only by iMX6 dual and quad processors

Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	[05] - CPU - PCIE, SATA.SchDoc		Checked by
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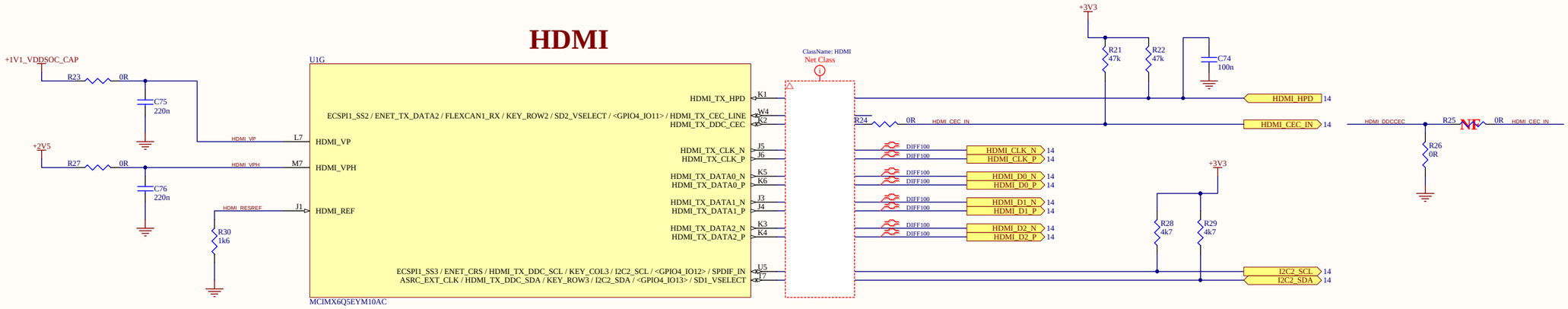
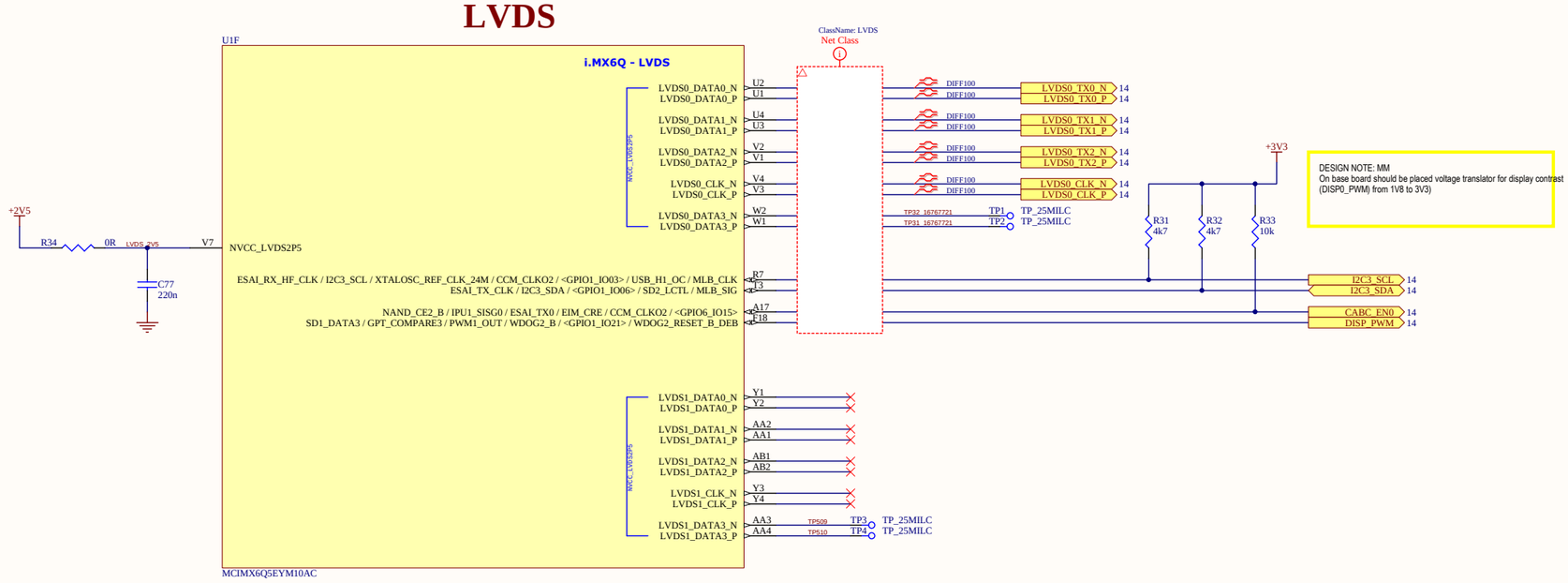
CPU - HDMI, LVDS

HDMI



LVDS



Title: iMX6 Rex	Variant: Variant name not interpreted	
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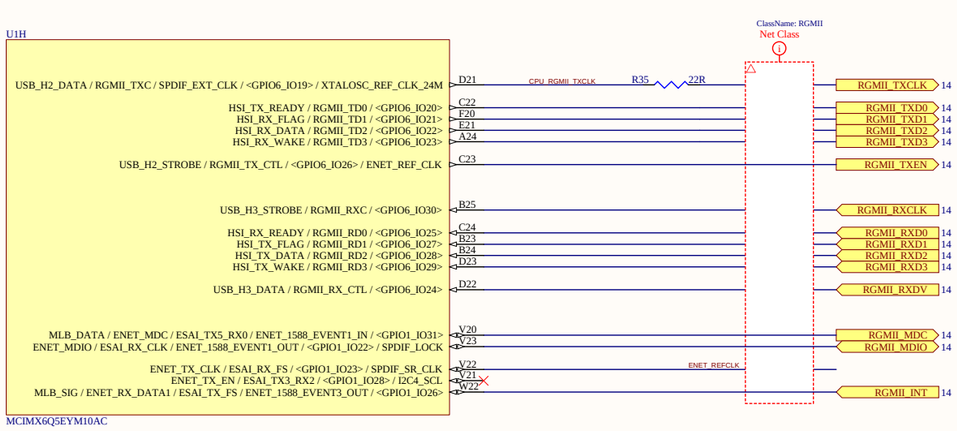
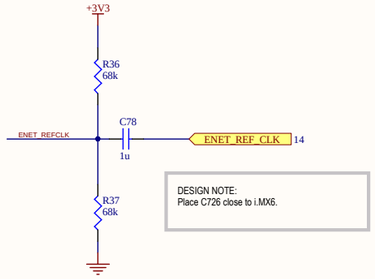
CPU - USB, ETHERNET

ETHERNET



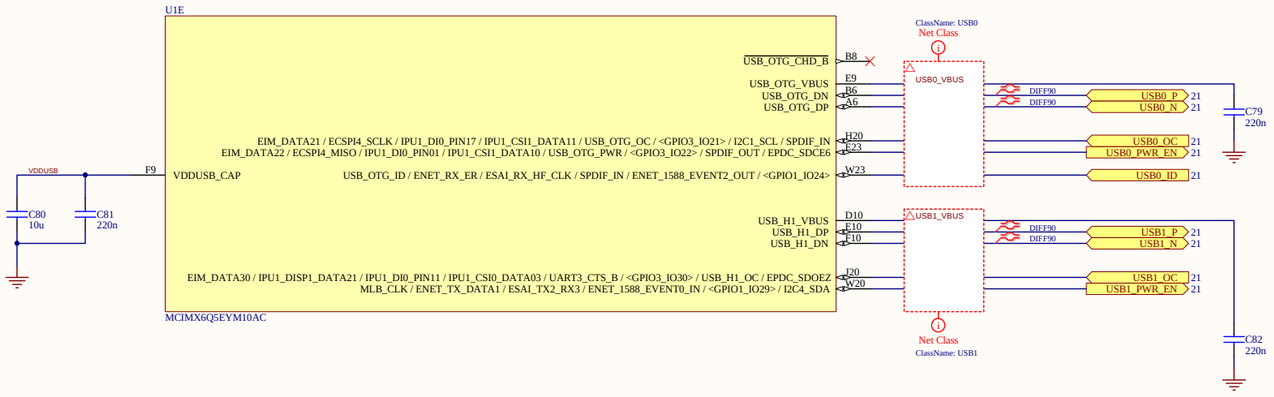
DESIGN NOTE:
Place C726 close to i.MX6.



DESIGN NOTE:
Place C726 close to i.MX6.

DESIGN NOTE: MM
Reset of ethernet moved to control sheet

USB



DESIGN NOTE: MM
USB will be supplied from source located on base board, controlled with power enable pins.

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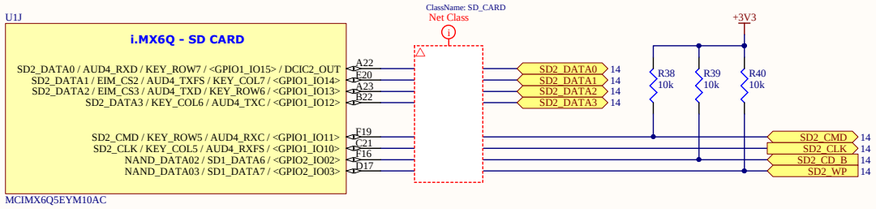
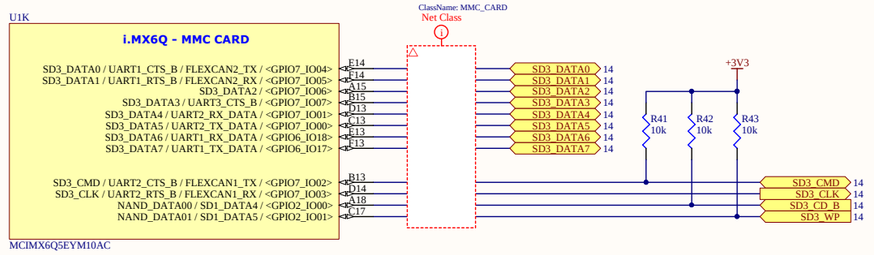
CPU - SPI, I2C, SD, MMC

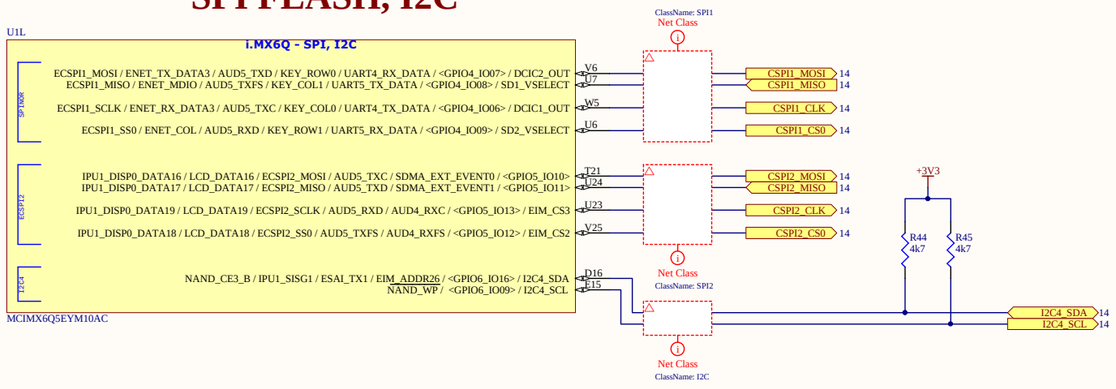
SD-CARD



MMC-CARD



SPI FLASH, I2C



Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	[08] - CPU - SPI, I2C, SD, MMC.SchDoc	Checked by	
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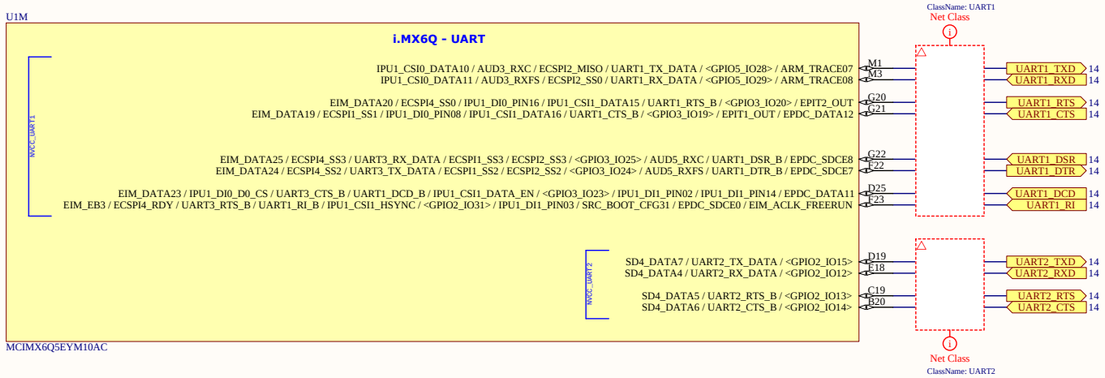
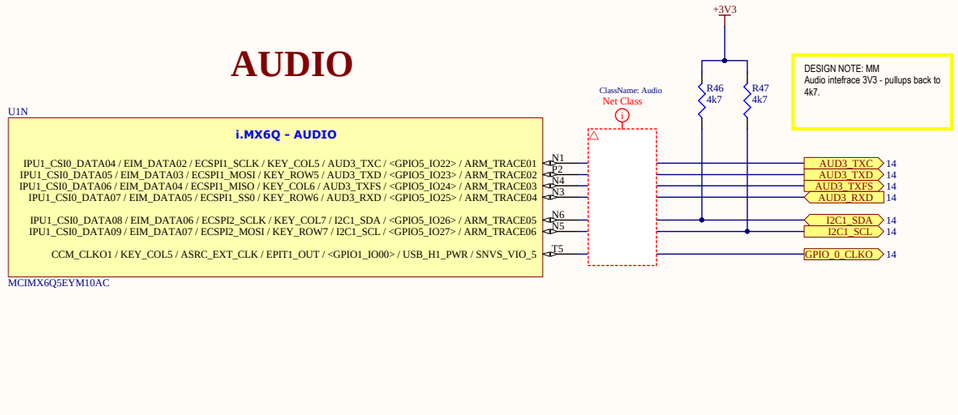
CPU - UART, AUDIO

UART



AUDIO



Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	[09] - CPU - UART, AUDIO.SchDoc		Checked by
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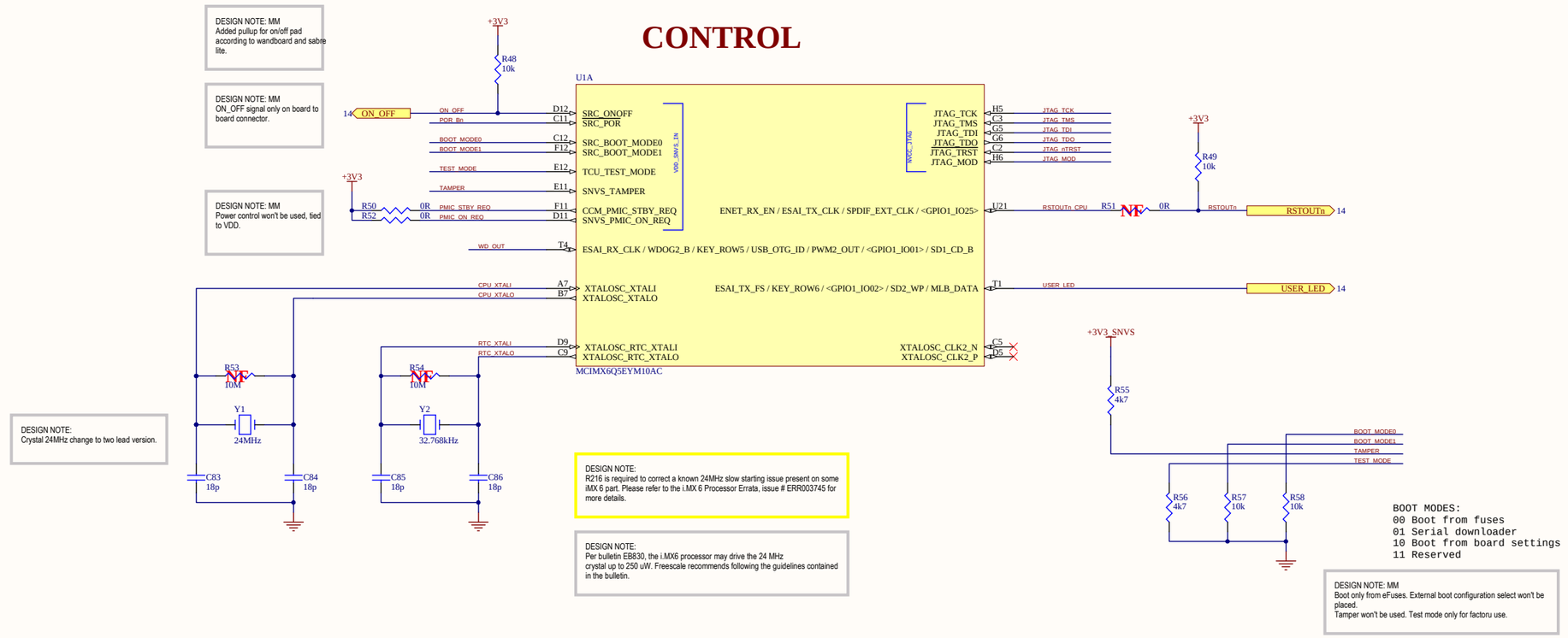
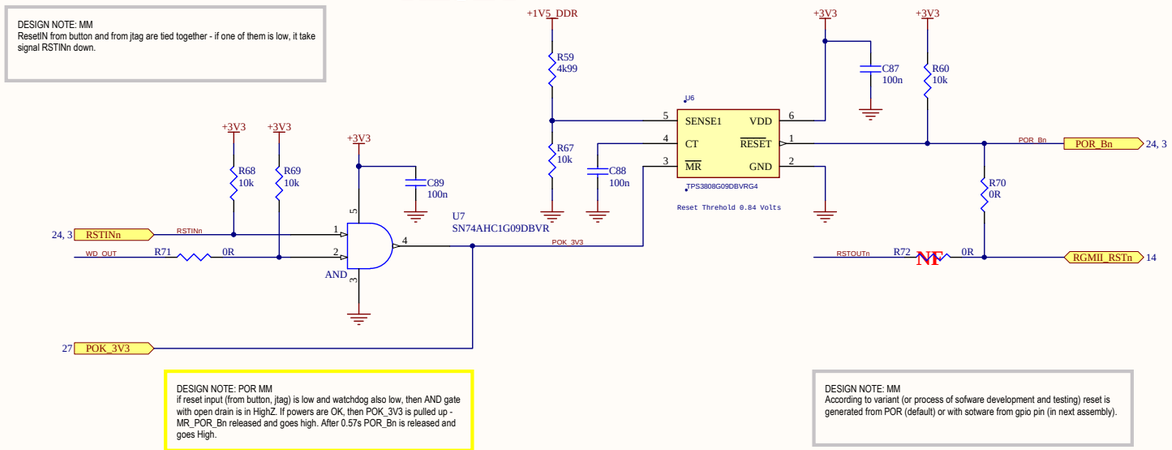
CPU - JTAG, CONTROL

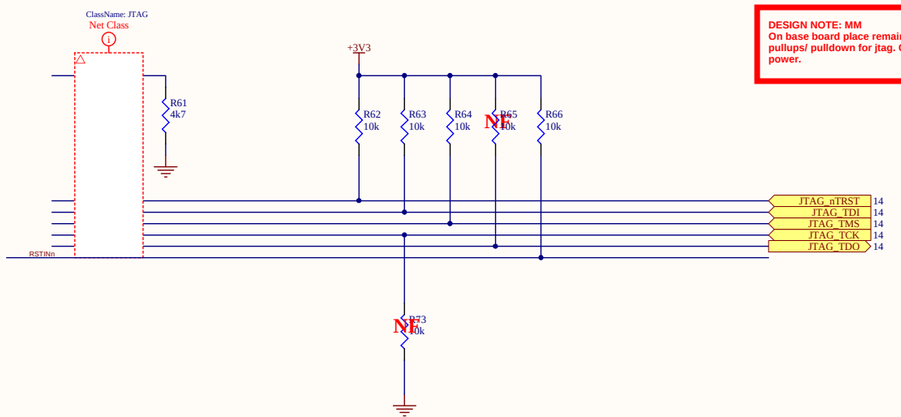
CONTROL



RESET



JTAG



Title:	iMX6 Rex	Variant:	Variant name not interpreted
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CPU - POWER

DESIGN NOTE: MM
VDDARM_IN pads and VDDOSC_IN pads are in wandboard and sabre lite connected throught bead. In ref design they this power rail are generated separateli in pmic, so there isn't connection between them. Bead added.

DESIGN NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

DESIGN NOTE: MM
According to above note there was added variants resistors to optimize schematic according to processoor selection. Default version is for quad processors (caps _23_CAP aren't shorted).

DESIGN NOTE: MM
In other designs there are by VDDOSC_IN pins fewer capacitors. Couldn't we remove some of them?

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

DESIGN NOTE: MM
From pins VDDHIGH_CAP there is a possibility to supply other cpu block for peripherals. Since we have 2V5 poewr rail this option isn't used.

DESIGN NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 DualLite parts in which VDDSNVS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q TO1.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

DESIGN NOTE: MM
Diode D10 will remain here?

MX6 power domains under-BGA decoupling

DESIGN NOTE: MM
In other designs there are by +1V5_DDR pins fewer capacitors. Couldn't we remove some of them?

DESIGN NOTE: MM
Connect GPANAIO, FA_ANA, VDD_FA rather to testpoints? In wandboard is tp conected to them.

DESIGN NOTE: MM
There is 3 different way to connect pin NVCC_PLL_OUT. Should be voltage divider (from wandboard) OK? It's within pins operate range.

DESIGN NOTE: MM
MIPI connected to 3V3 on wandboard and sabre lite

DESIGN NOTE: MM
MIPI connected to 3V3 on wandboard and sabre lite

DESIGN NOTE: MM
Capacitors for NVCC_ENET

DESIGN NOTE: MM
Capacitors for NVCC_GPIO

DESIGN NOTE: MM
In other schemtaics then in ref design, ther isn't place cap 22u for ethernet. Will be removed?

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CPU - UNUSED PINS

U1P

ACCL_INT_IN B21
CSI_RST_B D20
CSI0_PWN A21
CSI0_RST_B C20
CSI_PWN E19
DISP0_PWM

SD1_CMD / PWM4_OUT / GPT_COMPARE1 / <GPIO1_IO18>
SD1_CLK / GPT_CLKIN / <GPIO1_IO20>
SD1_DATA0 / GPT_CAPTURE1 / <GPIO1_IO16>
SD1_DATA1 / PWM3_OUT / GPT_CAPTURE2 / <GPIO1_IO17>
SD1_DATA2 / GPT_COMPARE2 / PWM2_OUT / WDOG1_B / <GPIO1_IO19> / WDOG1_RESET_B_DEB

NVCC_SD1

NVCC_SD2

ENET_RX_DATA0 / ESAI_TX_HF_CLK / SPDIF_OUT / <GPIO1_IO27> W21 UOK_B
ENET_TX_DATA0 / ESAI_TX4_RX1 / <GPIO1_IO30> U20 DISP0_PWR_EN

NVCC_SD3

HEADPHONE_DET D15
SD3_RESET / UART3_RTS_B / <GPIO7_IO08>

ECSPI1_SS1 / ENET_RX_DATA2 / FLEXCAN1_TX / KEY_COL2 / ENET_MDC / <GPIO4_IO10> / USB_H1_PWR_CTL_WAKE W6 CODEC_PWR_EN
FLEXCAN2_TX / IPU1_SISG4 / USB_OTG_OC / KEY_COL4 / UART5_RTS_B / <GPIO4_IO14> T6 KEY_COL4
FLEXCAN2_RX / IPU1_SISG5 / USB_OTG_PWR / KEY_ROW4 / UART5_CTS_B / <GPIO4_IO15> V5 KEY_ROW4

MLB_CP B11
MLB_CN A11
MLB_CLK_P
MLB_CLK_N

MLB_SP B9
MLB_SN A9
MLB_SIG_P
MLB_SIG_N

MLB_DP A10
MLB_DN B10
MLB_DATA_P
MLB_DATA_N

ESAI_TX_HF_CLK / KEY_COL7 / <GPIO1_IO04> / SD2_CD_B R6 KEY_COL7
ESAI_TX2_RX3 / KEY_ROW7 / CCM_CLKO1 / <GPIO1_IO05> / I2C3_SCL / ARM_EVENTI R4 KEY_ROW7
ESAI_TX4_RX1 / EPIT1_OUT / FLEXCAN1_TX / UART2_TX_DATA / <GPIO1_IO07> / SPDIF_LOCK / USB_OTG_HOST_MODE / I2C4_SCL R3 SPDIF_CLK
ESAI_TX5_RX0 / XTALOSC_REF_CLK_32K / EPIT2_OUT / FLEXCAN1_RX / UART2_RX_DATA / <GPIO1_IO08> / SPDIF_SR_CLK / USB_OTG_PWR_CTL_WAKE / I2C4_SDA R5 DISP0_SER_RS
ESAI_RX_FS / WDOG1_B / KEY_COL6 / CCM_REF_EN_B / PWM1_OUT / <GPIO1_IO09> / SD1_WP T2 KEY_COL6
ESAI_TX3_RX2 / ENET_1588_EVENT2_IN / ENET_REF_CLK / SD1_LCTL / SPDIF_IN / <GPIO7_IO11> / I2C3_SDA / JTAG_DE_B R2 GPIO7_IO11
ESAI_TX0 / ENET_1588_EVENT3_IN / CCM_PMIC_READY / SDMA_EXT_EVENT0 / SPDIF_OUT / <GPIO7_IO12> R1 SPDIF_OUT
ESAI_TX1 / ENET_RX_CLK / SD3_VSELECT / SDMA_EXT_EVENT1 / ASRC_EXT_CLK / <GPIO7_IO13> / SNVS_VIO_5_CTL T6 PMIC_INT_B
KEY_COL5 / ENET_1588_EVENT0_OUT / SPDIF_OUT / CCM_CLKO1 / ECSPI1_RDY / <GPIO4_IO05> / ENET_TX_ER T5 KEY_COL5

NAND_CE0_B / <GPIO6_IO11> F15 DISP_RST_B
NAND_CE1_B / SD4_VSELECT / SD3_VSELECT / <GPIO6_IO14> C16 DISP_PWR_EN

NAND_ALE / SD4_RESET / <GPIO6_IO08> A16 CAP_TCH_INT0
NAND_CLE / <GPIO6_IO07> C15 CAP_TCH_INT1

NAND_READY / <GPIO6_IO10> B16 AUX_5V_EN

NVCC_NAND

NAND_DATA04 / SD2_DATA4 / <GPIO2_IO04> A19 SD2_DATA4
NAND_DATA05 / SD2_DATA5 / <GPIO2_IO05> B18 SD2_DATA5
NAND_DATA06 / SD2_DATA6 / <GPIO2_IO06> E17 SD2_DATA6
NAND_DATA07 / SD2_DATA7 / <GPIO2_IO07> C18 SD2_DATA7

SD4_CLK / NAND_WE_B / UART3_RX_DATA / <GPIO7_IO10> E16 SD4_CLK
SD4_CMD / NAND_RE_B / UART3_TX_DATA / <GPIO7_IO09> B17 SD4_CMD

SD4_DATA0 / NAND_DQS / <GPIO2_IO08> D18 SD4_DATA0
SD4_DATA1 / PWM3_OUT / <GPIO2_IO09> B19 SD4_DATA1
SD4_DATA2 / PWM4_OUT / <GPIO2_IO10> U17 SD4_DATA2
SD4_DATA3 / <GPIO2_IO11> V20 SD4_DATA3

MCIMX6Q5EYM10AC

U1O

NVCC_EIM1

<EIM_LBA> / IPU1_DI1_PIN17 / ECSPI2_SS1 / GPIO2_IO27 / SRC_BOOT_CFG26 / EPDC_DATA04 K22 EIM_LBA
<EIM_OE> / IPU1_DI1_PIN07 / ECSPI2_MISO / GPIO2_IO25 / EPDC_PWR_IRQ J24 EIM_OE
<EIM_RW> / IPU1_DI1_PIN08 / ECSPI2_SS0 / GPIO2_IO26 / SRC_BOOT_CFG29 / EPDC_DATA07 K20 EIM_RW

<EIM_CS0> / IPU1_DI1_PIN05 / ECSPI2_SCLK / GPIO2_IO23 / EPDC_DATA06 H24 EIM_CS0
<EIM_CS1> / IPU1_DI1_PIN06 / ECSPI2_MOSI / GPIO2_IO24 / EPDC_DATA08 J23 EIM_CS1

<EIM_ADDR16> / IPU1_DI1_DISP_CLK / IPU1_CSI1_PIXCLK / GPIO2_IO22 / SRC_BOOT_CFG16 / EPDC_DATA00 H25 EIM_A16
<EIM_ADDR17> / IPU1_DISP1_DATA12 / IPU1_CSI1_DATA12 / GPIO2_IO21 / SRC_BOOT_CFG17 / EPDC_PWR_STAT G24 EIM_A17
<EIM_ADDR18> / IPU1_DISP1_DATA13 / IPU1_CSI1_DATA13 / GPIO2_IO20 / SRC_BOOT_CFG18 / EPDC_PWR_CTRL0 J22 EIM_A18
<EIM_ADDR19> / IPU1_DISP1_DATA14 / IPU1_CSI1_DATA14 / GPIO2_IO19 / SRC_BOOT_CFG19 / EPDC_PWR_CTRL1 G25 EIM_A19
<EIM_ADDR20> / IPU1_DISP1_DATA15 / IPU1_CSI1_DATA15 / GPIO2_IO18 / SRC_BOOT_CFG20 / EPDC_PWR_CTRL2 H22 EIM_A20
<EIM_ADDR21> / IPU1_DISP1_DATA16 / IPU1_CSI1_DATA16 / GPIO2_IO17 / SRC_BOOT_CFG21 / EPDC_GDCLK H23 EIM_A21
<EIM_ADDR22> / PU1_DISP1_DATA17 / IPU1_CSI1_DATA17 / GPIO2_IO16 / SRC_BOOT_CFG22 / EPDC_GDSP F24 EIM_A22
<EIM_ADDR23> / IPU1_DISP1_DATA18 / IPU1_CSI1_DATA18 / IPU1_SISG3 / GPIO6_IO06 / SRC_BOOT_CFG23 / EPDC_GDOE G21 EIM_A23
<EIM_ADDR24> / IPU1_DISP1_DATA19 / IPU1_CSI1_DATA19 / IPU1_SISG2 / GPIO5_IO04 / SRC_BOOT_CFG24 / EPDC_GDRL F25 EIM_A24

<EIM_ADDR25> / ECSPI4_SS1 / ECSPI2_RDY / IPU1_DI1_PIN12 / IPU1_DI0_D1_CS / GPIO5_IO02 / HDMI_TX_CEC_LINE / EPDC_DATA15 / EIM_ACLK_FREERUN H19 EIM_A25

EIM_DATA16 / ECSPI1_SCLK / IPU1_DI0_PIN05 / IPU1_CSI1_DATA18 / HDMI_TX_DDC_SDA / <GPIO3_IO16> / I2C2_SDA / EPDC_DATA10 C25 EIM_D16
EIM_DATA17 / ECSPI1_MISO / IPU1_DI0_PIN06 / IPU1_CSI1_PIXCLK / DCIC1_OUT / <GPIO3_IO17> / I2C3_SCL / EPDC_VCOM0 F21 EIM_D17
EIM_DATA18 / ECSPI1_MOSI / IPU1_DI0_PIN07 / IPU1_CSI1_DATA17 / IPU1_DI1_D0_CS / <GPIO3_IO18> / I2C3_SDA / EPDC_VCOM1 D24 EIM_D18

NVCC_EIM0

EIM_DATA26 / IPU1_DI1_PIN11 / IPU1_CSI0_DATA01 / IPU1_CSI1_DATA14 / UART2_TX_DATA / <GPIO3_IO26> / IPU1_SISG2 / IPU1_DISP1_DATA22 / EPDC_SDOED E24 EIM_D26
EIM_DATA27 / IPU1_DI1_PIN13 / IPU1_CSI0_DATA00 / IPU1_CSI1_DATA13 / UART2_RX_DATA / <GPIO3_IO27> / IPU1_SISG3 / IPU1_DISP1_DATA23 / EPDC_SDOE E25 EIM_D27
EIM_DATA28 / I2C1_SDA / ECSPI4_MOSI / IPU1_CSI1_DATA12 / UART2_CTS_B / <GPIO3_IO28> / IPU1_EXT_TRIG / IPU1_DI0_PIN13 / EPDC_PWR_CTRL3 G23 EIM_D28
EIM_DATA29 / IPU1_DI1_PIN15 / ECSPI4_SS0 / UART2_RTS_B / <GPIO3_IO29> / IPU1_CSI1_VSYNC / IPU1_DI0_PIN14 / EPDC_PWR_WAKE J19 PWR_BTN_SNS

EIM_DATA31 / IPU1_DISP1_DATA20 / IPU1_DI0_PIN12 / IPU1_CSI0_DATA02 / UART3_RTS_B / <GPIO3_IO31> / USB_H1_PWR / EPDC_SDCLK_P / EIM_ACLK_FREERUN H21 EIM_D31

EIM_EB2 / ECSPI1_SS0 / IPU1_CSI1_DATA19 / HDMI_TX_DDC_SCL / <GPIO2_IO30> / I2C2_SCL / SRC_BOOT_CFG30 / EPDC_DATA05 E22 EIM_EB2

<EIM_BCLK> / IPU1_DI1_PIN16 / GPIO6_IO31 / EPDC_SDCE9 N22 EIM_BCLK
<EIM_WAIT> / EIM_DTACK_B / GPIO5_IO00 / SRC_BOOT_CFG25 M25 EIM_WAIT

<EIM_EB0> / IPU1_DISP1_DATA11 / IPU1_CSI1_DATA11 / CCM_PMIC_READY / GPIO2_IO28 / SRC_BOOT_CFG27 / EPDC_PWR_COM K21 EIM_EB0
<EIM_EB1> / IPU1_DISP1_DATA10 / IPU1_CSI1_DATA10 / GPIO2_IO29 / SRC_BOOT_CFG28 / EPDC_SDSHR K23 EIM_EB1

<EIM_AD00> / IPU1_DISP1_DATA09 / IPU1_CSI1_DATA09 / GPIO3_IO00 / SRC_BOOT_CFG00 / EPDC_SDCLK_N L20 EIM_DA0
<EIM_AD01> / IPU1_DISP1_DATA08 / IPU1_CSI1_DATA08 / GPIO3_IO01 / SRC_BOOT_CFG01 / EPDC_SDLE J25 EIM_DA1
<EIM_AD02> / IPU1_DISP1_DATA07 / IPU1_CSI1_DATA07 / GPIO3_IO02 / SRC_BOOT_CFG02 / EPDC_BDR0 L21 EIM_DA2
<EIM_AD03> / IPU1_DISP1_DATA06 / IPU1_CSI1_DATA06 / GPIO3_IO03 / SRC_BOOT_CFG03 / EPDC_BDR1 K24 EIM_DA3
<EIM_AD04> / IPU1_DISP1_DATA05 / IPU1_CSI1_DATA05 / GPIO3_IO04 / SRC_BOOT_CFG04 / EPDC_SDCE0 L22 EIM_DA4
<EIM_AD05> / IPU1_DISP1_DATA04 / IPU1_CSI1_DATA04 / GPIO3_IO05 / SRC_BOOT_CFG05 / EPDC_SDCE1 L23 EIM_DA5
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<EIM_AD07> / IPU1_DISP1_DATA02 / IPU1_CSI1_DATA02 / GPIO3_IO07 / SRC_BOOT_CFG07 / EPDC_SDCE3 L25 EIM_DA7
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<EIM_AD11> / IPU1_DI1_PIN02 / IPU1_CSI1_HSYNC / GPIO3_IO11 / SRC_BOOT_CFG11 / EPDC_DATA03 M20 EIM_DA11
<EIM_AD12> / IPU1_DI1_PIN03 / IPU1_CSI1_VSYNC / GPIO3_IO12 / SRC_BOOT_CFG12 / EPDC_DATA02 M24 EIM_DA12
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<EIM_AD14> / IPU1_DI1_D1_CS / GPIO3_IO14 / SRC_BOOT_CFG14 / EPDC_DATA14 N23 EIM_DA14
<EIM_AD15> / IPU1_DI1_PIN01 / IPU1_DI1_PIN04 / GPIO3_IO15 / SRC_BOOT_CFG15 / EPDC_DATA09 N24 EIM_DA15

MCIMX6Q5EYM10AC

U1Q

i.MX6Q - DISP; CSI

CSI0_HSYNCH P4
CSI0_PIXCLK P1
CSI0_VSYNCH N2

IPU1_CSI0_HSYNC / CCM_CLKO1 / <GPIO5_IO19> / ARM_TRACE_CTL
IPU1_CSI0_PIXCLK / <GPIO5_IO18> / ARM_EVENTO
IPU1_CSI0_VSYNC / EIM_DATA01 / <GPIO5_IO21> / ARM_TRACE00

NVCC_CSI

IPU1_DI0_DISP_CLK / LCD_CLK / <GPIO4_IO16> / LCD_WR_RWN N19 DSP0_CLK

IPU1_DI0_PIN02 / LCD_HSYNC / AUD6_TXD / <GPIO4_IO18> / LCD_RS N25 DI0_PIN2
IPU1_DI0_PIN03 / LCD_VSYNC / AUD6_TXFS / <GPIO4_IO19> / LCD_CS N20 DI0_PIN3
IPU1_DI0_PIN04 / LCD_BUSY / AUD6_RXD / SD1_WP / <GPIO4_IO20> / LCD_RESET P25 DI0_PIN4
IPU1_DI0_PIN15 / LCD_ENABLE / AUD6_TXC / <GPIO4_IO17> / LCD_RD_E V21 DI0_PIN15

IPU1_DISP0_DATA00 / LCD_DATA00 / ECSPI3_SCLK / <GPIO4_IO21> P24 DSP0_DAT0
IPU1_DISP0_DATA01 / LCD_DATA01 / ECSPI3_MOSI / <GPIO4_IO22> P22 DSP0_DAT1
IPU1_DISP0_DATA02 / LCD_DATA02 / ECSPI3_MISO / <GPIO4_IO23> P23 DSP0_DAT2
IPU1_DISP0_DATA03 / LCD_DATA03 / ECSPI3_SS0 / <GPIO4_IO24> P21 DSP0_DAT3
IPU1_DISP0_DATA04 / LCD_DATA04 / ECSPI3_SS1 / <GPIO4_IO25> P20 DSP0_DAT4
IPU1_DISP0_DATA05 / LCD_DATA05 / ECSPI3_SS2 / AUD6_RXFS / <GPIO4_IO26> R25 DSP0_DAT5
IPU1_DISP0_DATA06 / LCD_DATA06 / ECSPI3_SS3 / AUD6_RXC / <GPIO4_IO27> R23 DSP0_DAT6
IPU1_DISP0_DATA07 / LCD_DATA07 / ECSPI3_RDY / <GPIO4_IO28> R24 DSP0_DAT7
IPU1_DISP0_DATA08 / LCD_DATA08 / PWM1_OUT / WDOG1_B / <GPIO4_IO29> R22 DSP0_DAT8
IPU1_DISP0_DATA09 / LCD_DATA09 / PWM2_OUT / WDOG2_B / <GPIO4_IO30> T25 DSP0_DAT9
IPU1_DISP0_DATA10 / LCD_DATA10 / <GPIO4_IO31> R21 DSP0_DAT10
IPU1_DISP0_DATA11 / LCD_DATA11 / <GPIO5_IO05> T23 DSP0_DAT11
IPU1_DISP0_DATA12 / LCD_DATA12 / <GPIO5_IO06> T24 DSP0_DAT12
IPU1_DISP0_DATA13 / LCD_DATA13 / AUD5_RXFS / <GPIO5_IO07> R20 DSP0_DAT13
IPU1_DISP0_DATA14 / LCD_DATA14 / AUD5_RXC / <GPIO5_IO08> T25 DSP0_DAT14
IPU1_DISP0_DATA15 / LCD_DATA15 / ECSPI1_SS1 / ECSPI2_SS1 / <GPIO5_IO09> T22 DSP0_DAT15

NVCC_CSI

IPU1_DISP0_DATA20 / LCD_DATA20 / ECSPI1_SCLK / AUD4_TXC / <GPIO5_IO14> U22 DSP0_DAT20
IPU1_DISP0_DATA21 / LCD_DATA21 / ECSPI1_MOSI / AUD4_TXD / <GPIO5_IO15> L20 DSP0_DAT21
IPU1_DISP0_DATA22 / LCD_DATA22 / ECSPI1_MISO / AUD4_TXFS / <GPIO5_IO16> V24 DSP0_DAT22
IPU1_DISP0_DATA23 / LCD_DATA23 / ECSPI1_SS0 / AUD4_RXD / <GPIO5_IO17> W24 DSP0_DAT23

CSI_CLK0M F4
CSI_CLK0P F3
CSI_CLK0_N
CSI_CLK0_P

CSI_D0M E4
CSI_D0P E3
CSI_DATA0_N
CSI_DATA0_P

CSI_D1M D1
CSI_D1P D2
CSI_DATA1_N
CSI_DATA1_P

CSI_D2M E1
CSI_D2P E2
CSI_D2M
CSI_D2P

CSI_D3M F2
CSI_D3P F1
CSI_D3M
CSI_D3P

CSI_REXT D4
CSI_REXT

NVCC_MIPI

DSI_CLK0_N H3 DSI_CLK0M
DSI_CLK0_P H4 DSI_CLK0P

DSI_DATA0_N G2 DSI_D0M
DSI_DATA0_P G1 DSI_D0P

DSI_DATA1_N H2 DSI_D1M
DSI_DATA1_P H1 DSI_D1P

DSI_REXT G4 DSI_REXT

NVCC_MIPI

MCIMX6Q5EYM10AC

Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	[12] - CPU - UNUSED.SchDoc		Checked by
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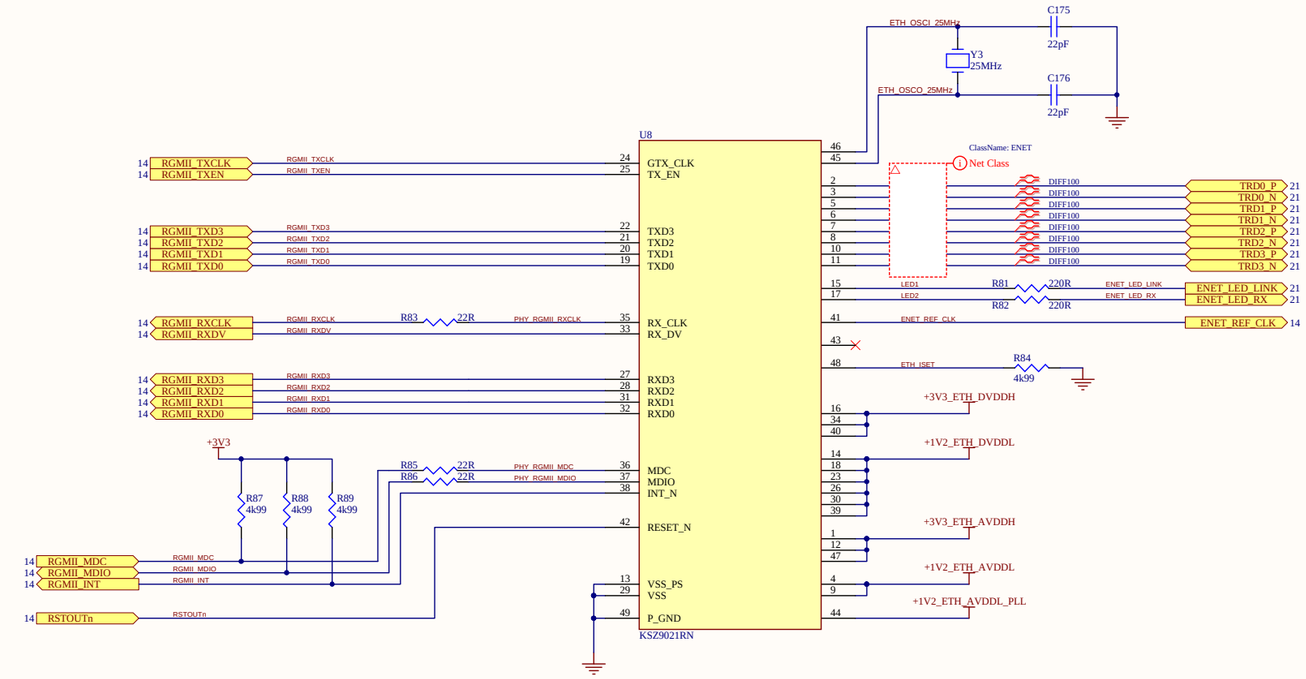
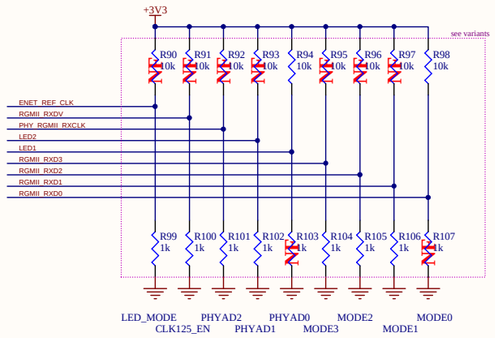
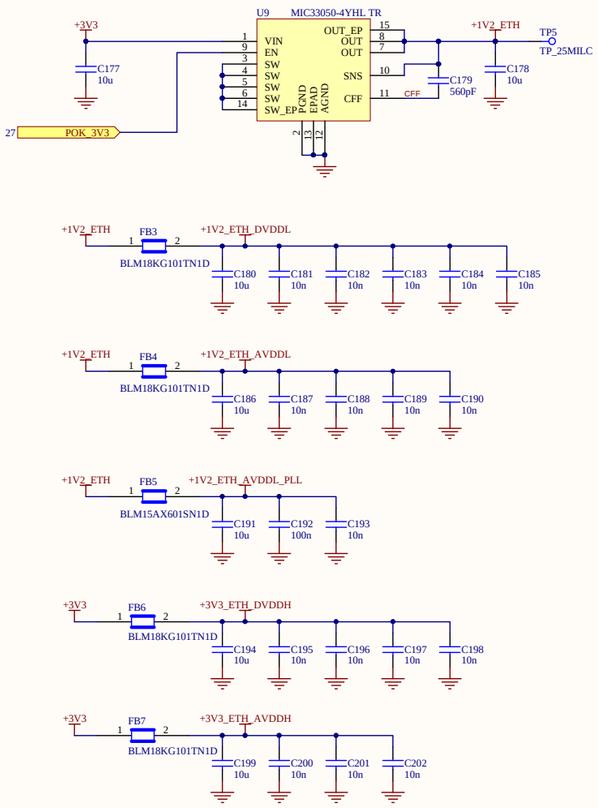
ETHERNET PHY



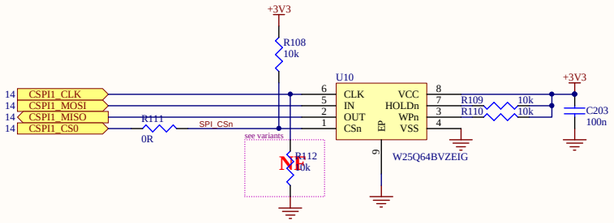




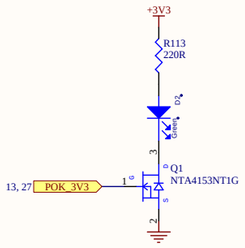
Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	[13] - ETHERNET PHY.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
Date:	28/04/2013	Sheet	13 of 20

SPI FLASH, LED

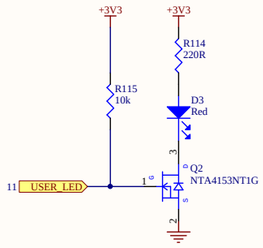
SPI NOR FLASH



POWER LED



USER DEFINED LED



Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	[14] - FLASH, LED.SchDoc		Checked by
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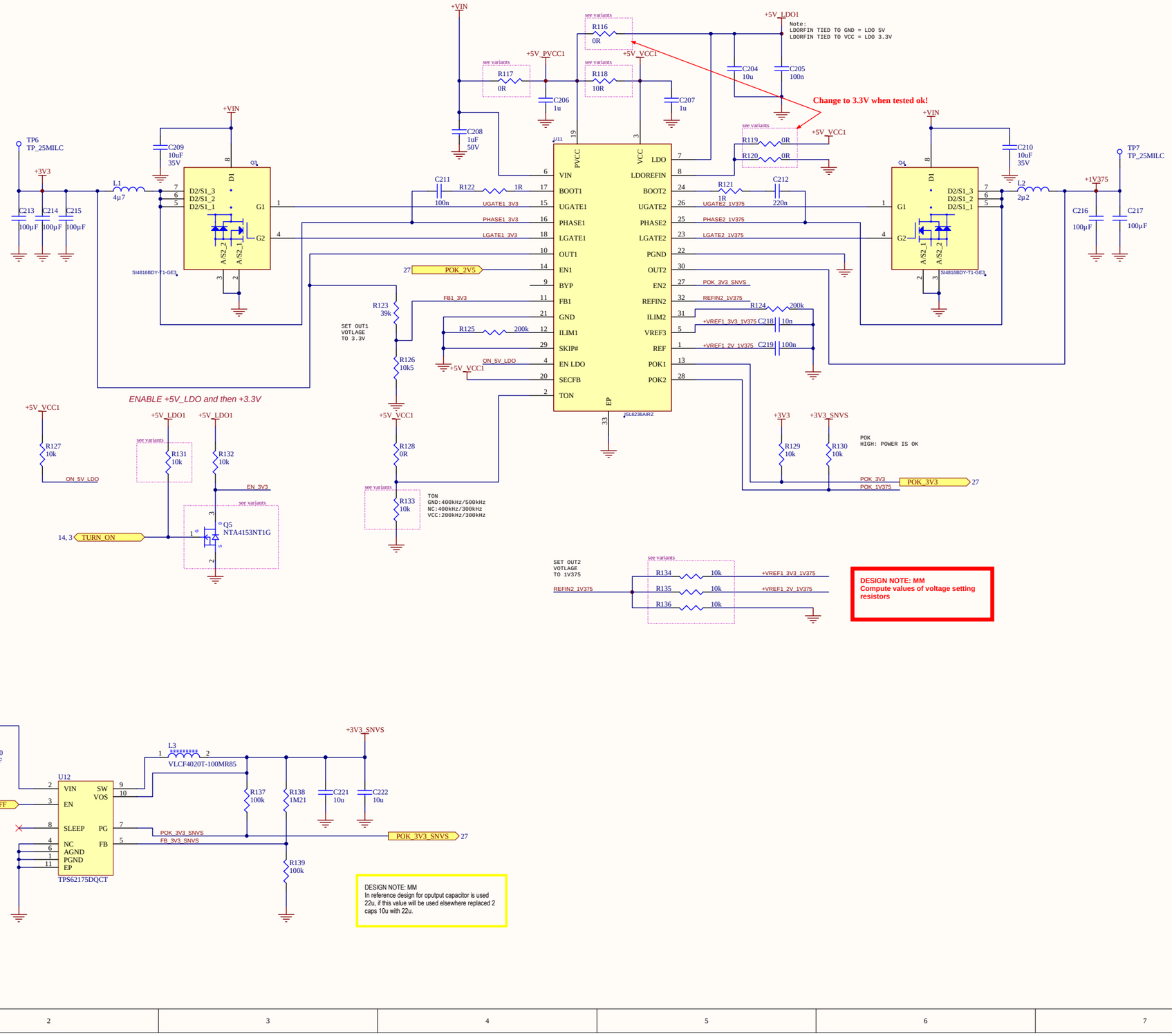
POWER +3.3V, +1.375V CON



Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	[15] - PWR 3V3, 1V375.SchDoc		Checked by
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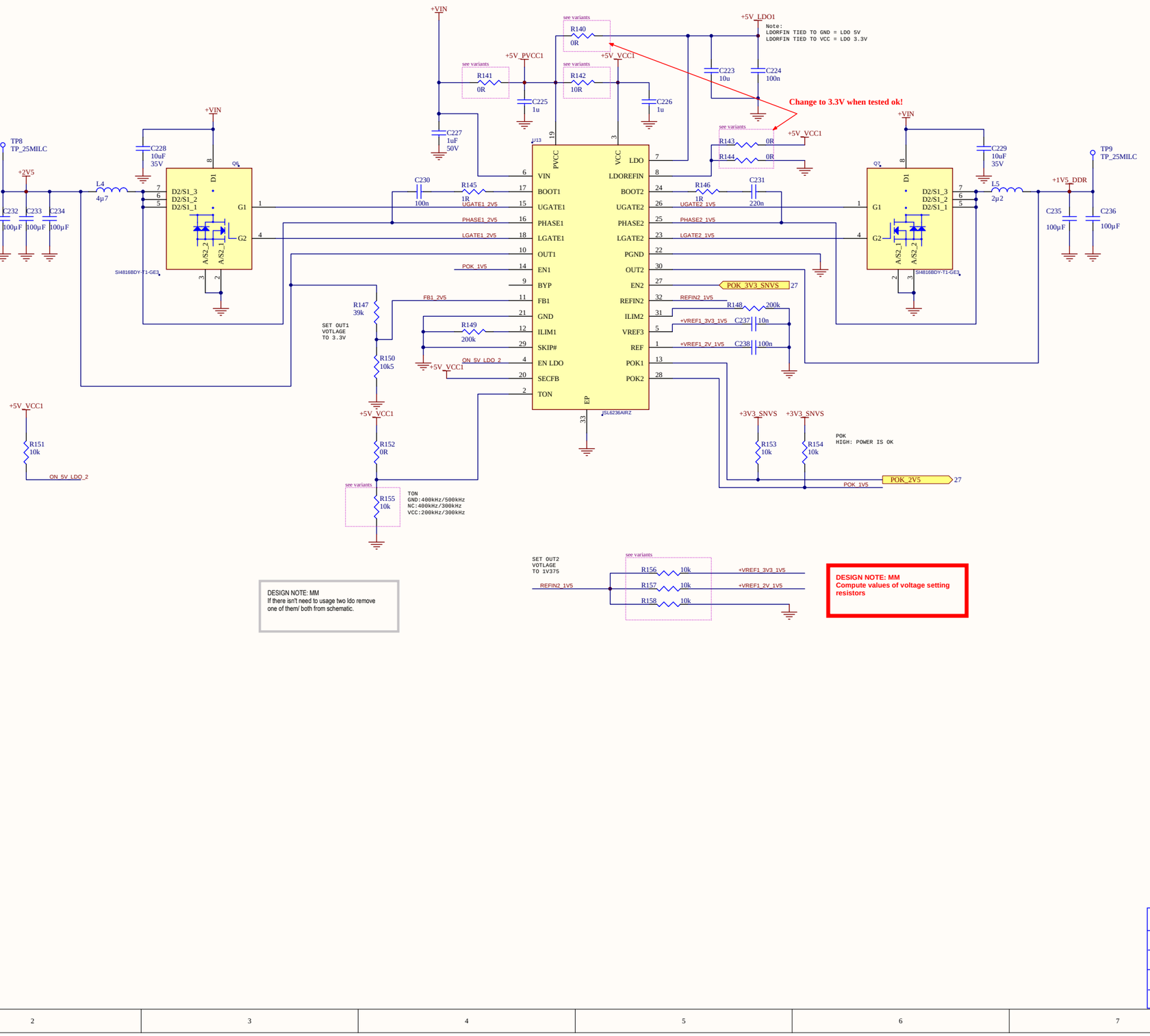
POWER +2.5V, +1.5V CON



Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	[16] - PWR 2V5, 1V5.SchDoc		Checked by
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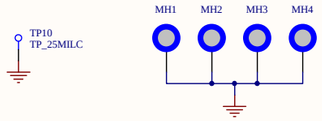
MECHANICAL



Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	[17] - MECH.SchDoc		Checked by
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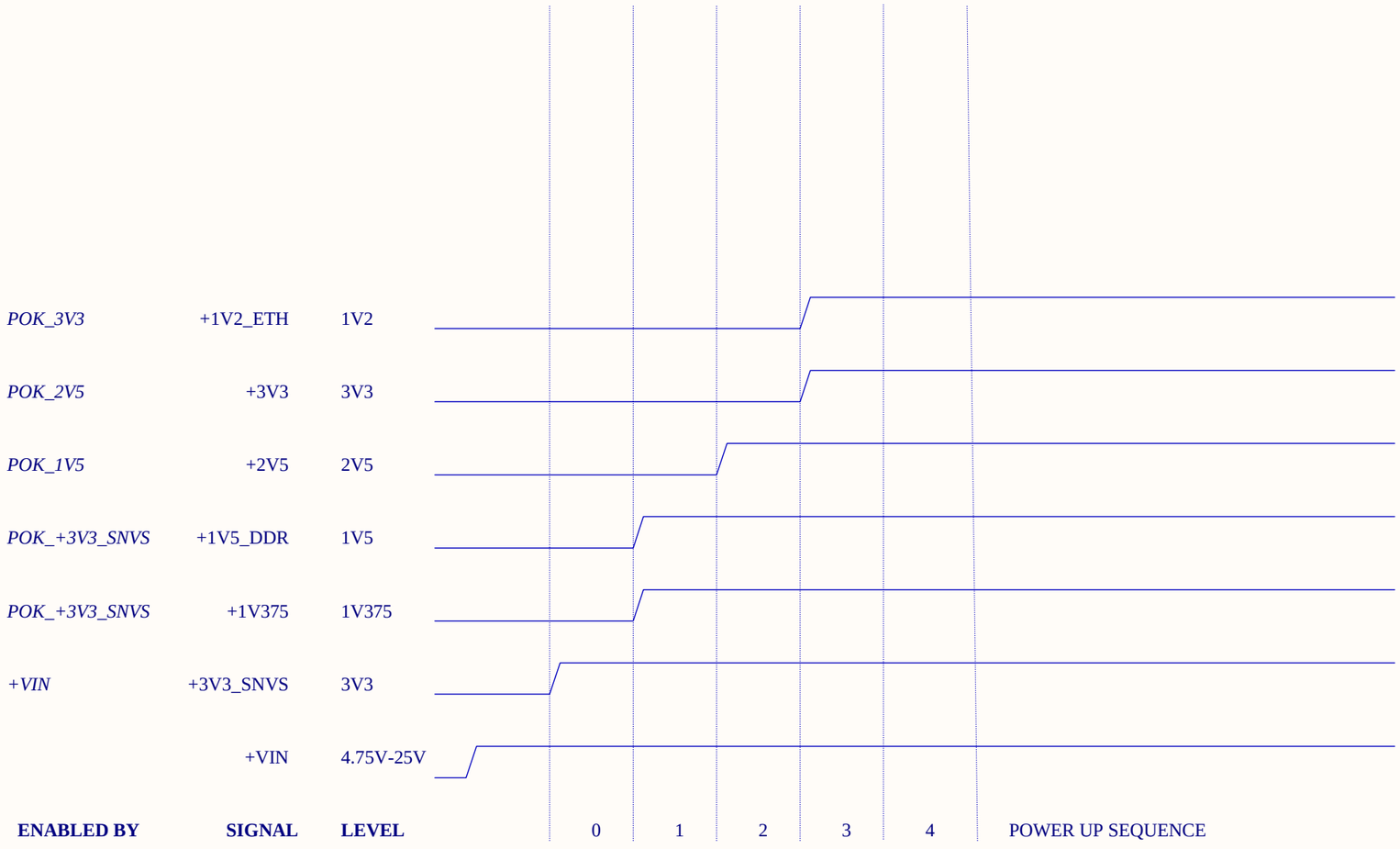
CPU - POWER SEQUENCING

+DDR_VREF	0V75	+1V5_DDR	ref. for DDR memories, gen. with volt. divider
+1V2_VDD_ARM_CAP	1V2	iMX	cpu, core caps
+1V1_VDDSOC_CAP	1V1	iMX	core caps, cpu-sata, cpu-pcie, cpu-hdmi

OTHER USED SIGNAL	LEVEL	GEN BY	SUPPLIED FROM SIGNAL



Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	[18] - POWER SEQUENCING.SchDoc		Checked by
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DOC: REVISION HISTORY

CLOCKS (CPU & PCIE)

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Designator
[01] - COVER PAGE.SchDoc

Designator
[02] - BLOCK DIAGRAM.SchDoc

Designator
[03] - CONNECTORS.SchDoc

Designator
[04] - CPU - DDR3, DDR3.SchDoc

Designator
[05] - CPU - PCIE, SATA.SchDoc

Designator
[06] - CPU - HDMI, LVDS.SchDoc

Designator
[07] - CPU - USB, ETHERNET.SchDoc

Designator
[08] - CPU - SPI, I2C, SD, MMC.SchDoc

Designator
[09] - CPU - UART, AUDIO.SchDoc

Designator
[10] - CPU - JTAG, CONTROL.SchDoc

Designator
[11] - CPU - POWER.SchDoc

Designator
[12] - CPU - UNUSED.SchDoc

Designator
[13] - ETHERNET PHY.SchDoc

Designator
[14] - FLASH, LED.SchDoc

Designator
[15] - PWR 3V3, 1V375.SchDoc

Designator
[16] - PWR 2V5, 1V5.SchDoc

Designator
[17] - MECH.SchDoc

Designator
[18] - POWER SEQUENCING.SchDoc

Designator
[19] - DOC REVISION HISTORY.SchDoc

TEMPLATE NOTES

Set Project Parameters

1) Go to Project -> Project Options -> Parameters
2) Set Company, Project and VersionRevision

Mark Not Fitted Components as
NF

Net Class Example

Net Class
ClassName: PCIE

Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Ttitle

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

Title:	iMX6 Rex	Variant:	Variant name not interpreted
Page Contents:	iMX6 Rex_V1I1 Project.SchDoc		Checked by
Size:	DWG NO	Revision:	V1I1
Date:	28/04/2013	Sheet	20 of 20