

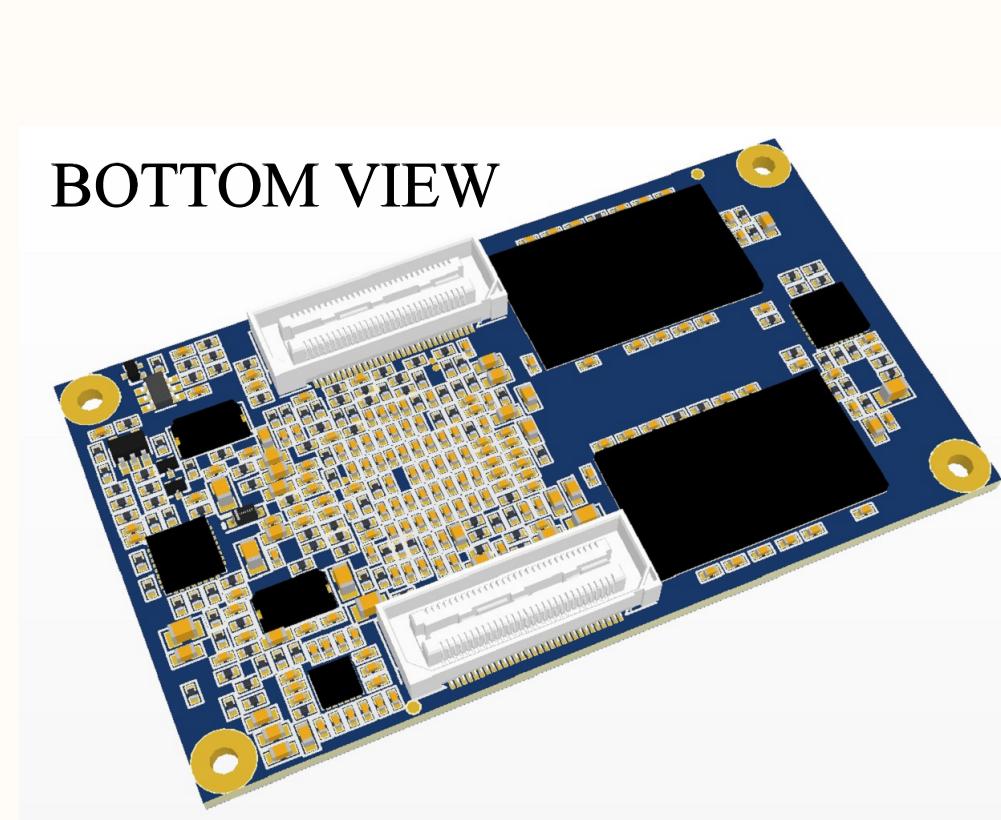
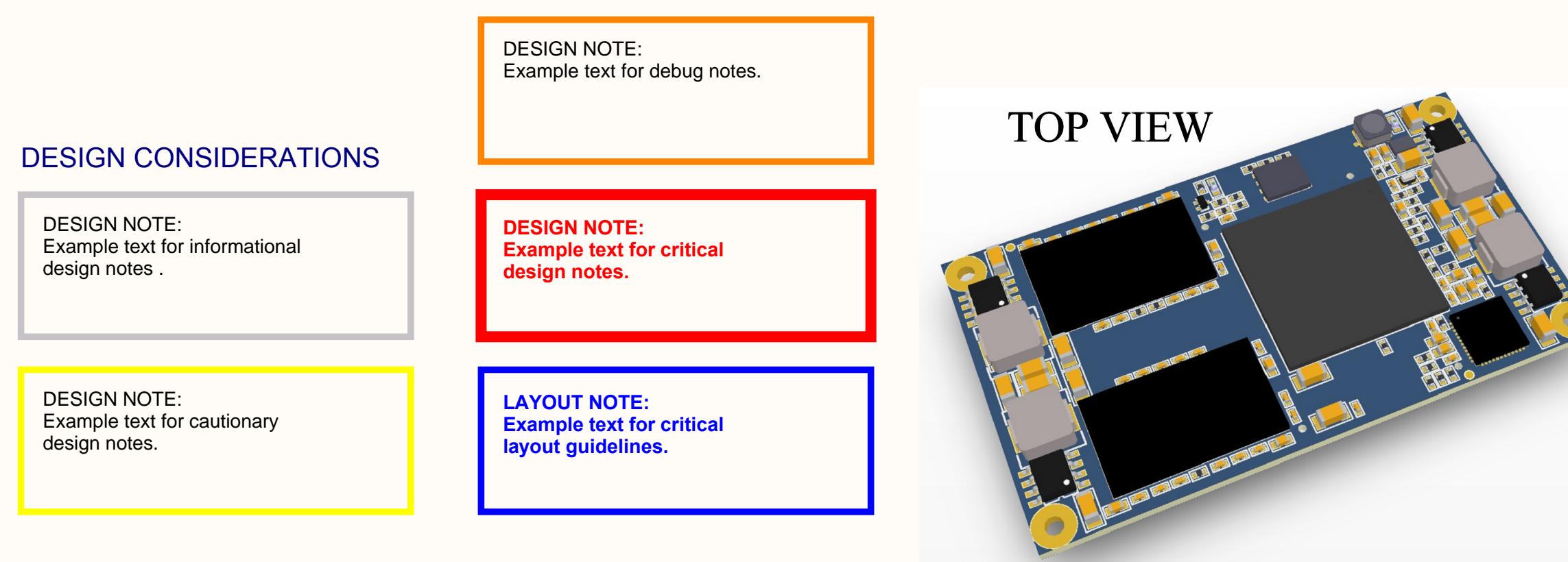
iMX6 Rex Module

Variant: Variant name not interpreted

28. 6. 2013
V1I1

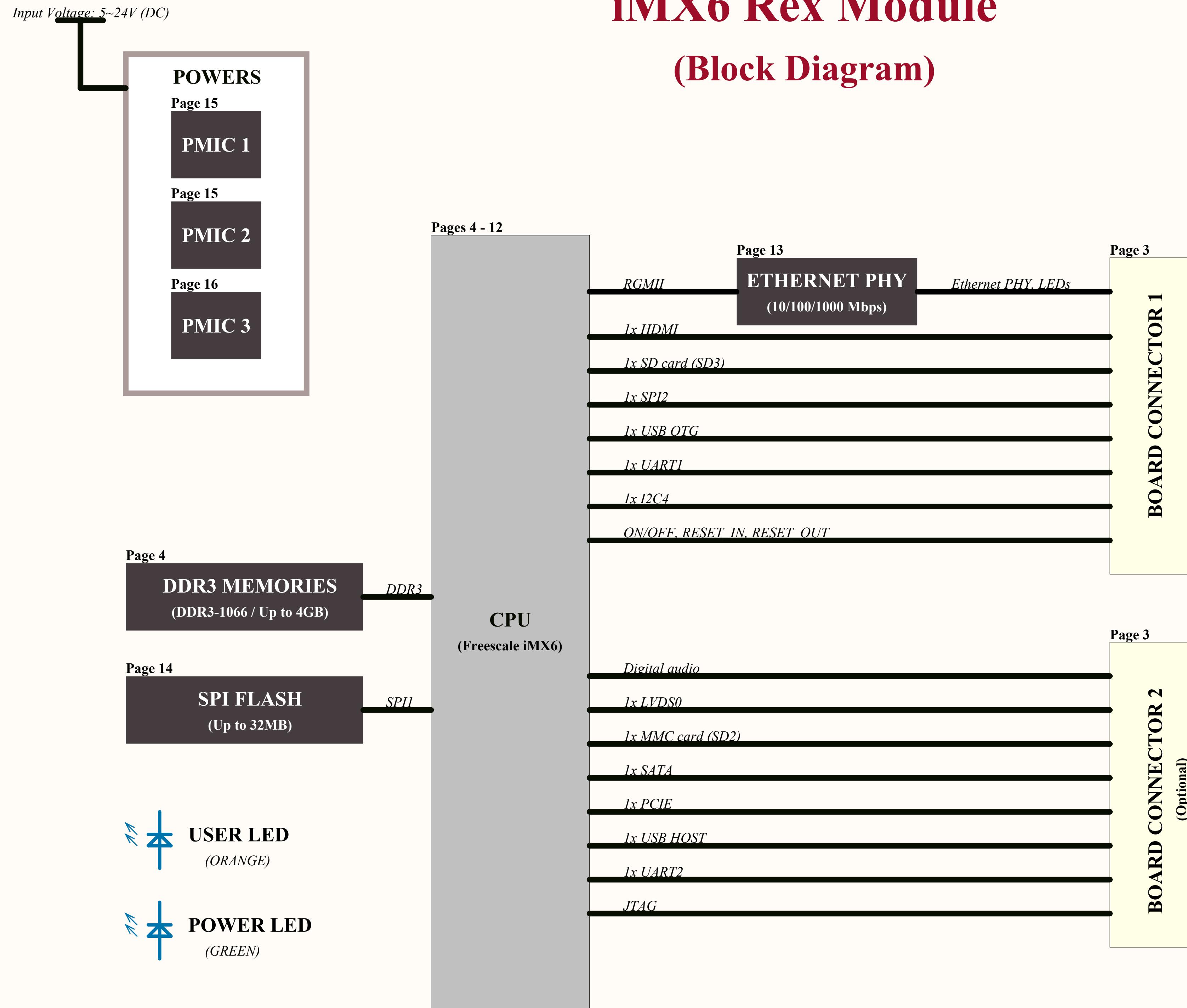
CHECKED

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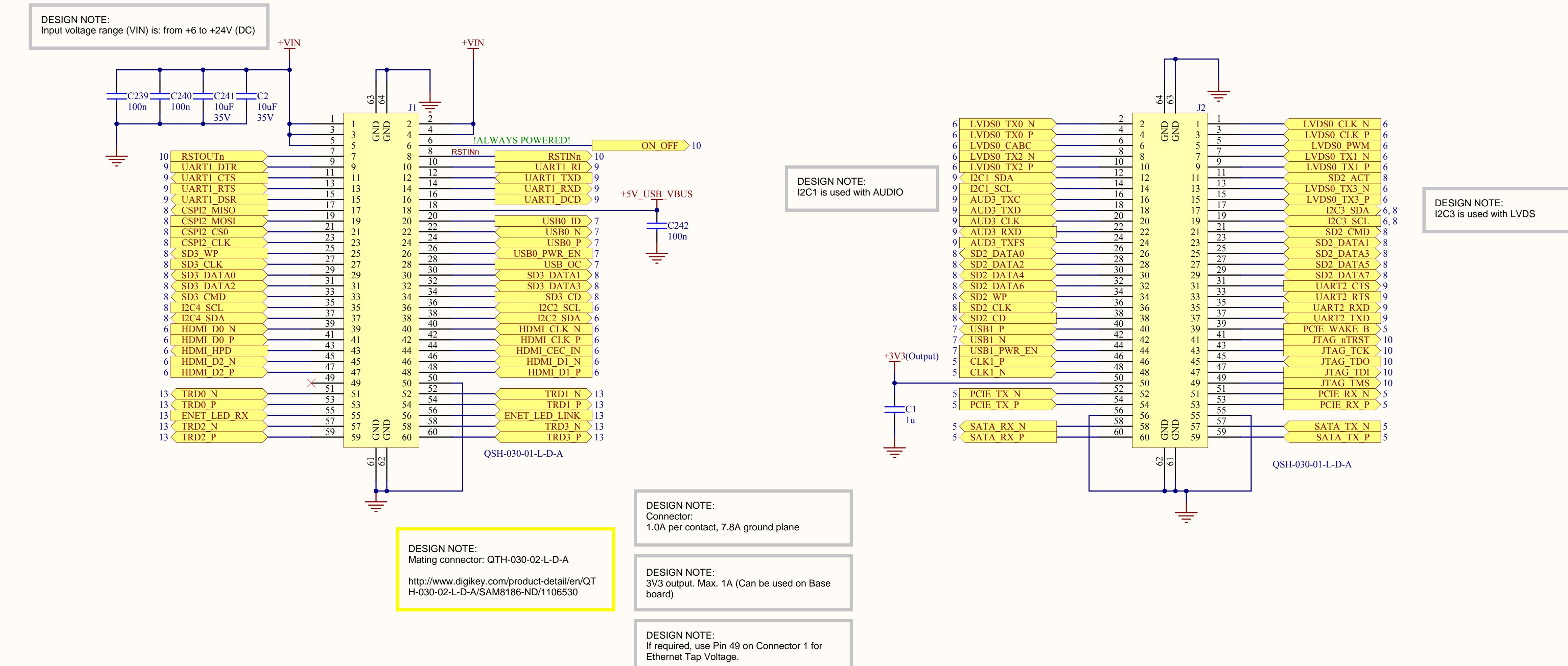


iMX6 Rex Module

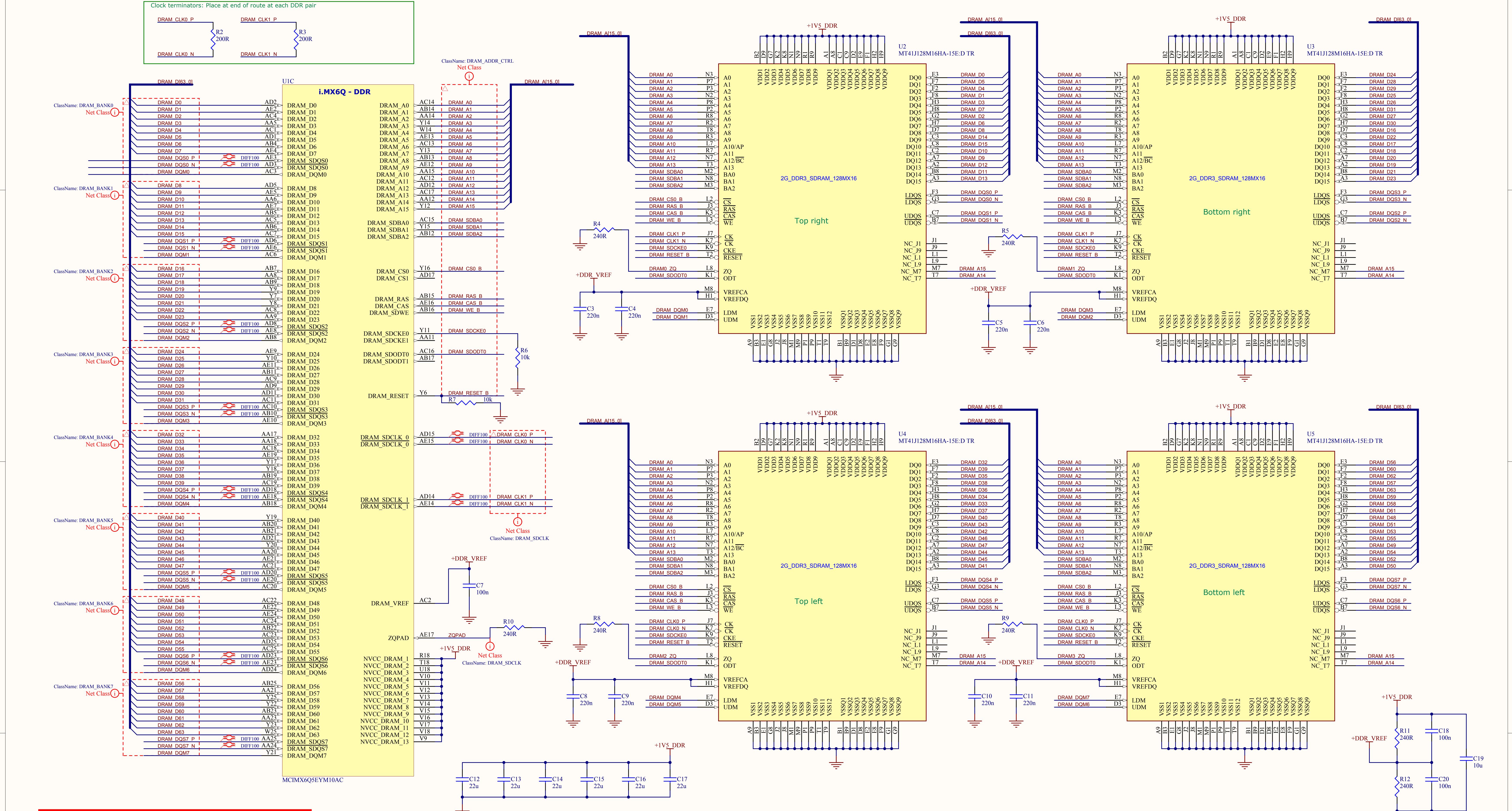
(Block Diagram)



CONNECTORS



CPU - DDR3, DDR3 MEM



DESIGN NOTE:
Pull down resistor RX3 is added to trace SDCKE0 in Rev B4 by soldering to an existing open via. Change will be made permanent in layout with the Rev C board.

DESIGN NOTE:

DESIGN NOTE:
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration. Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

DESIGN NOTE:
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B pins to the new locations.



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Variant:
Variant name not interpreted

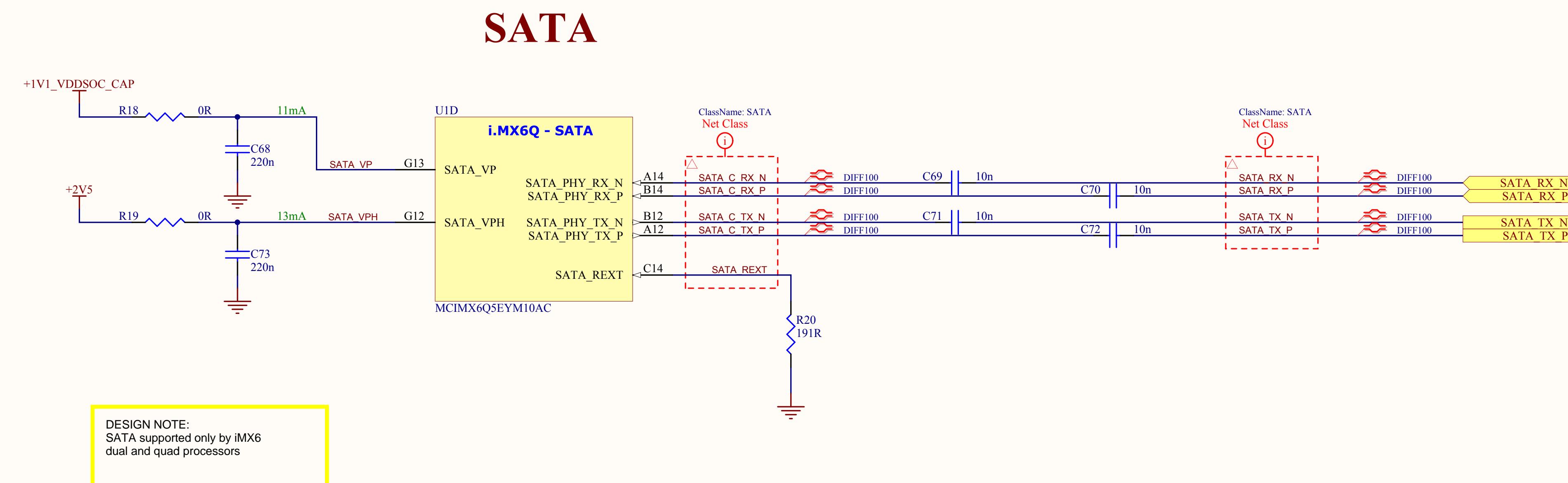
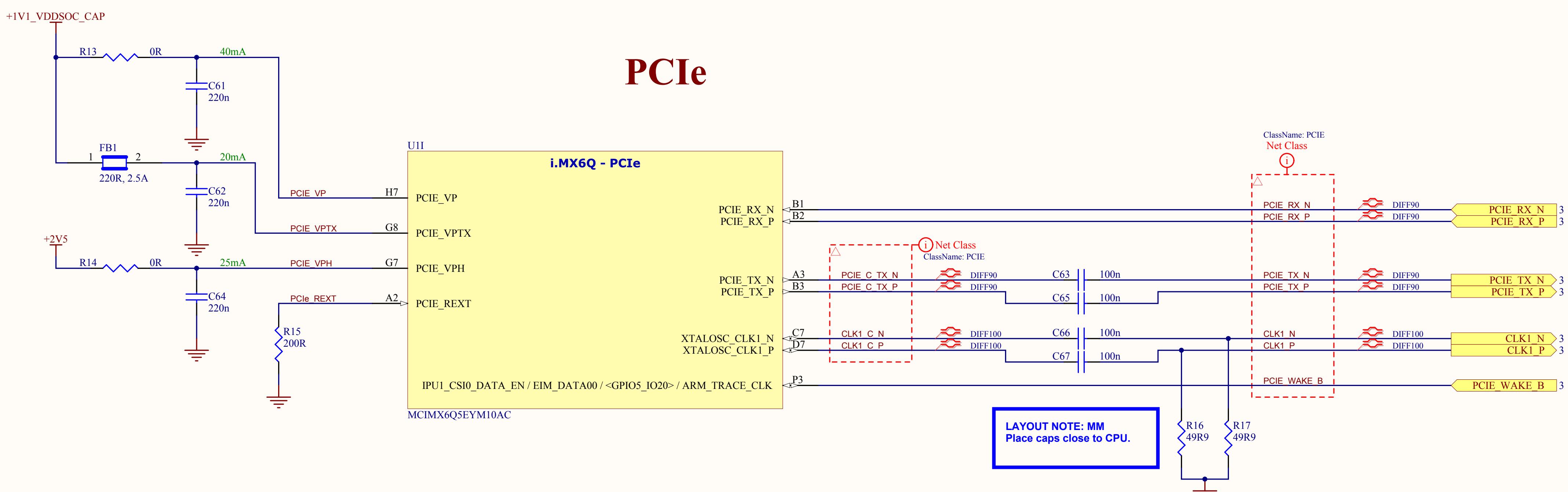
, DDR3 MEM.SchDoc Checked by

Revision:
V1I1

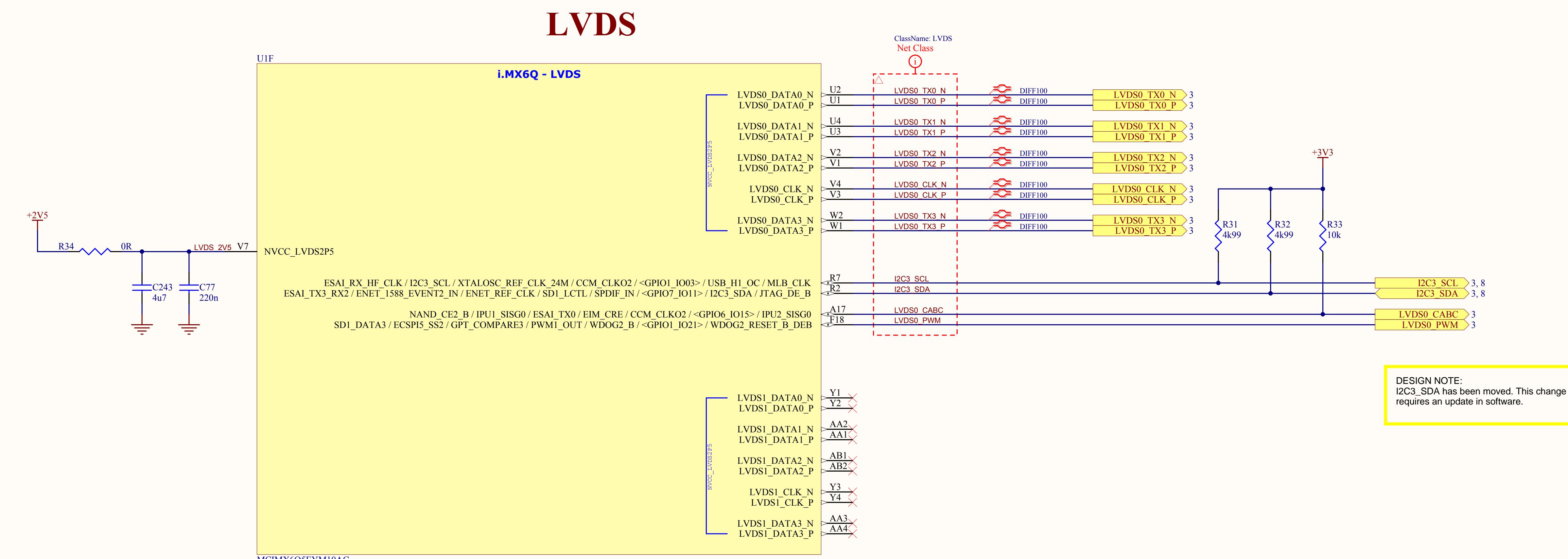
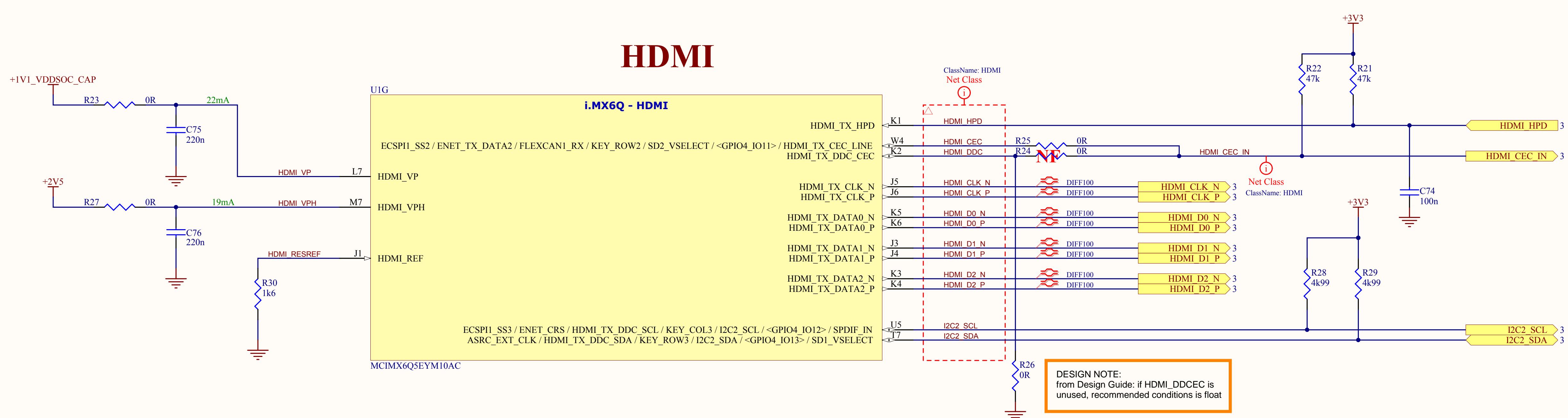
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CPU - SATA, PCIe

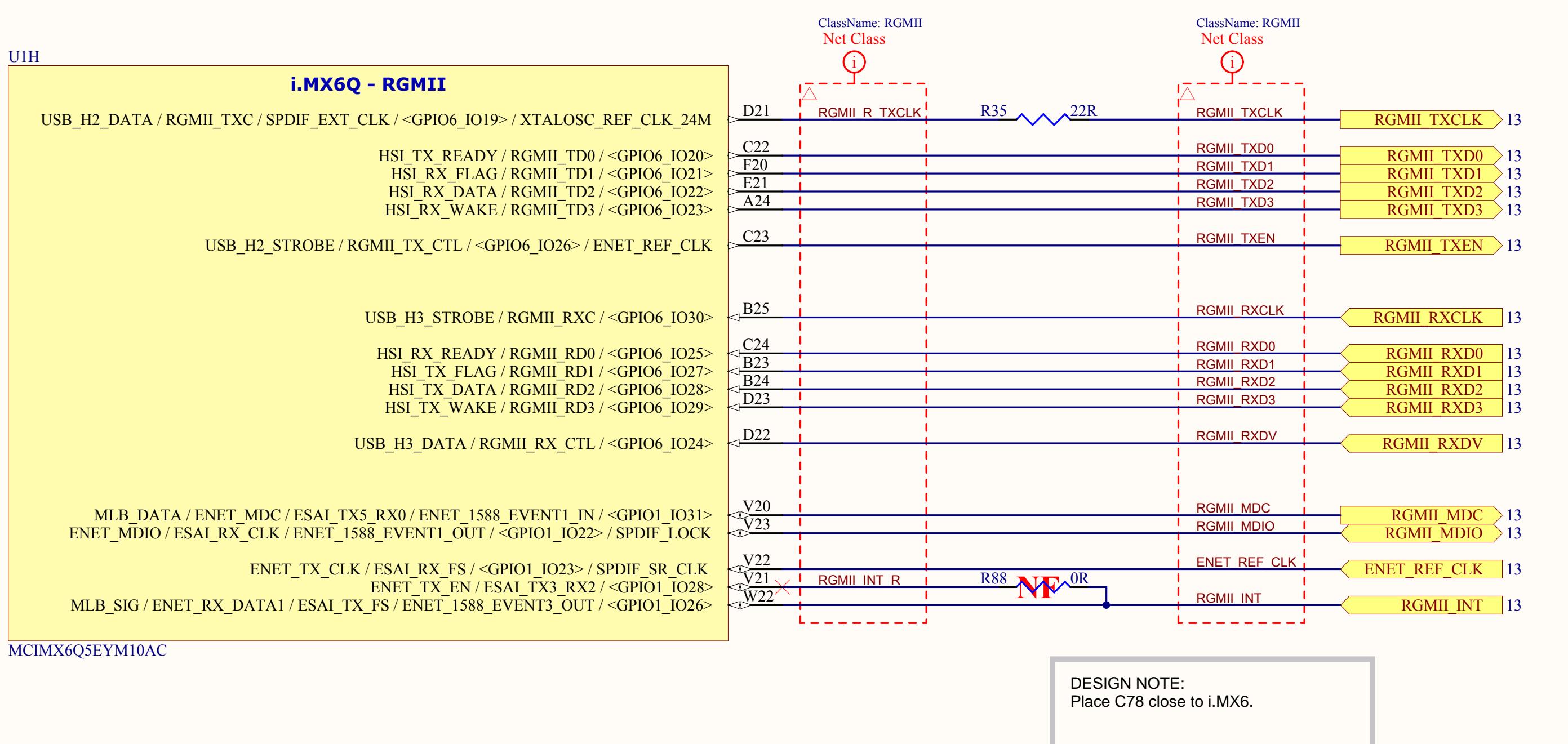


CPU - HDMI, LVDS



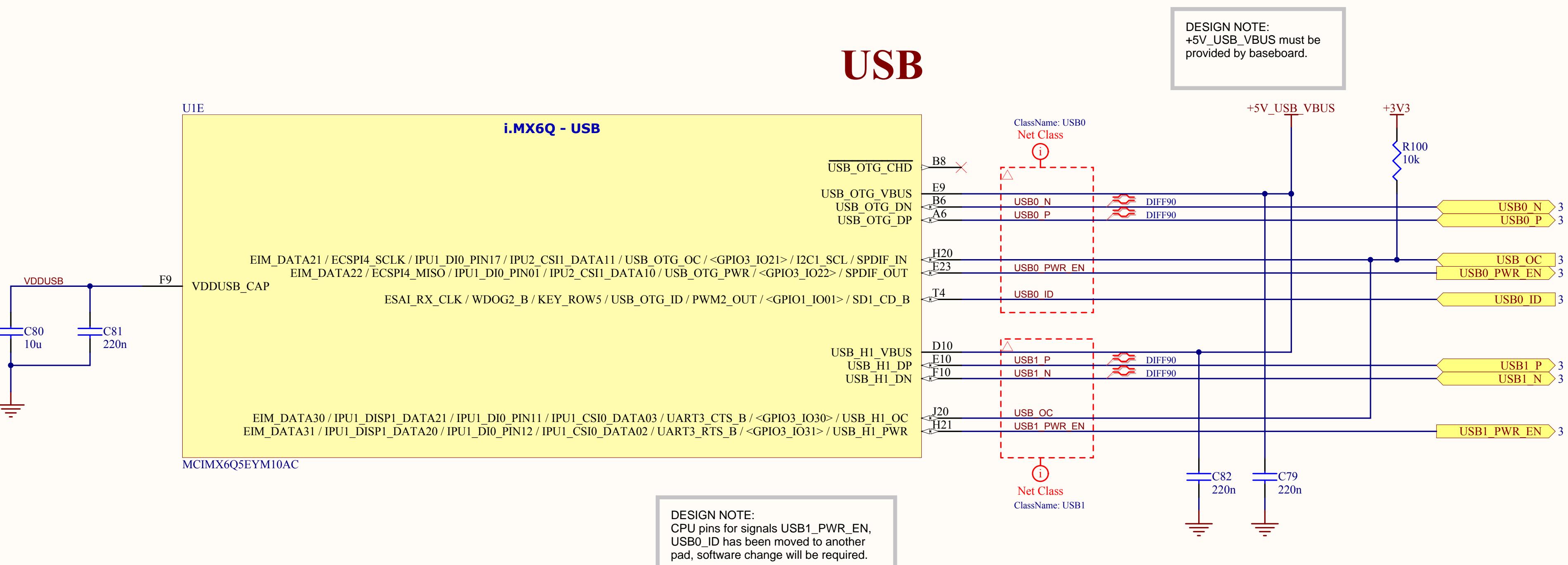
CPU - USB, ETHERNET

ETHERNET



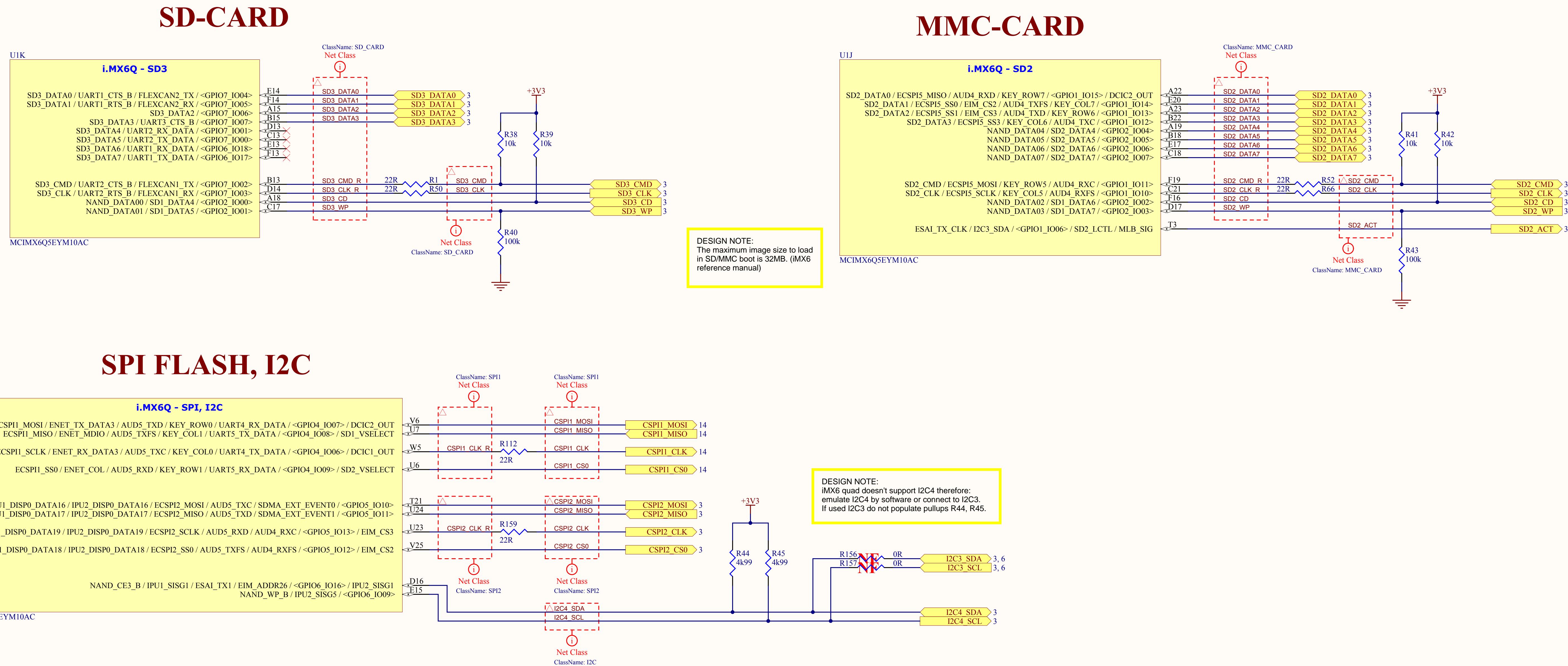
DESIGN NOTE:
Place C78 close to i.MX6

USB



DESIGN NOTE:
CPU pins for signals USB1_PWR_E
USB0_ID has been moved to another
pad. software change will be required

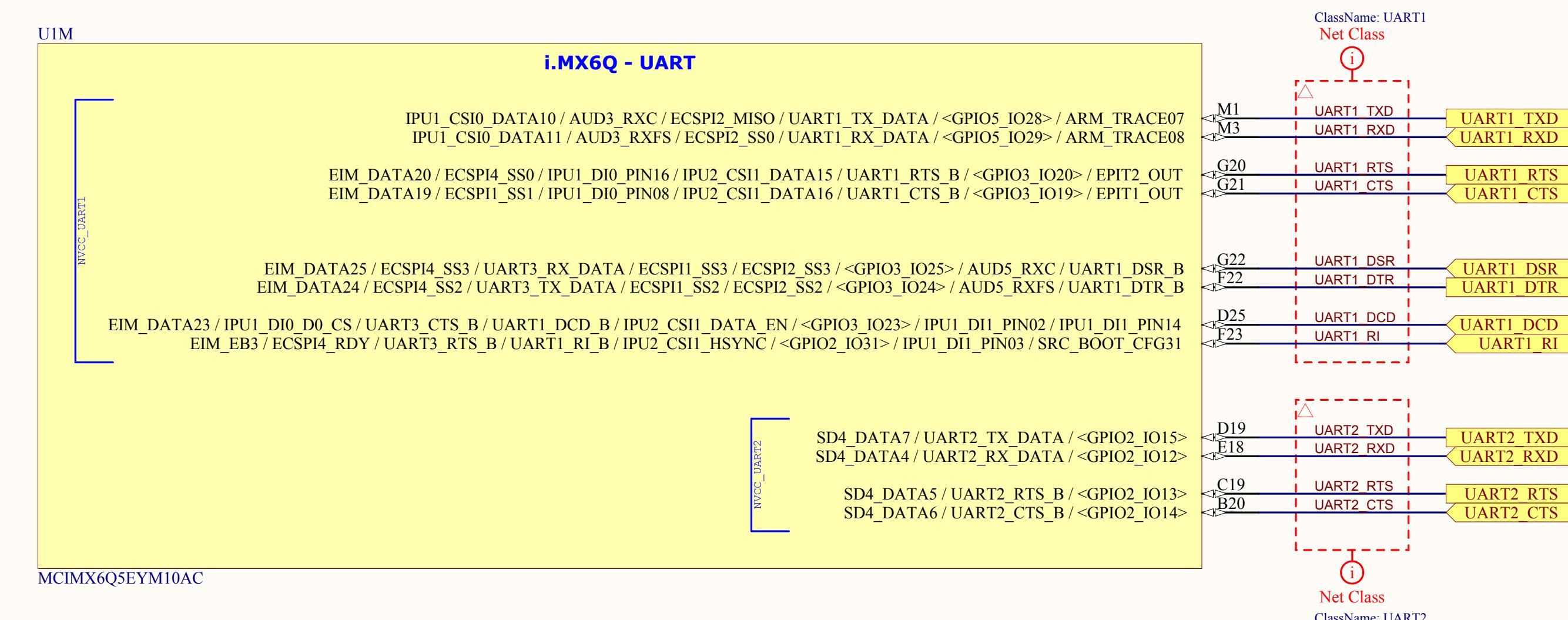
CPU - SPI, I2C, SD, MMC



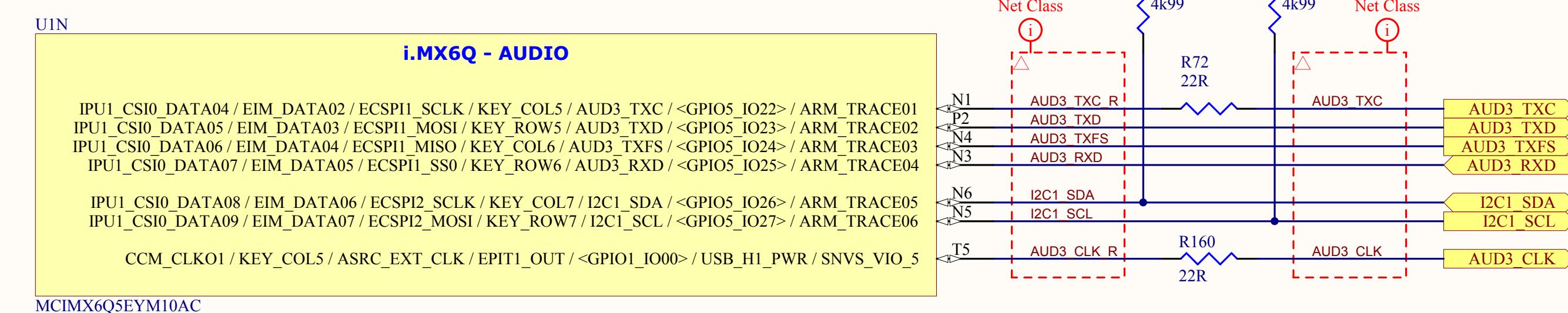
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Title:	iMX6 Rex Module
Variant:	Variant name not interpreted
Page Contents:	[08] - CPU - SPI, I2C, SD, MMC.SchDoc
Checked by:	
Size:	DWG NO
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CPU - UART, AUDIO

UART

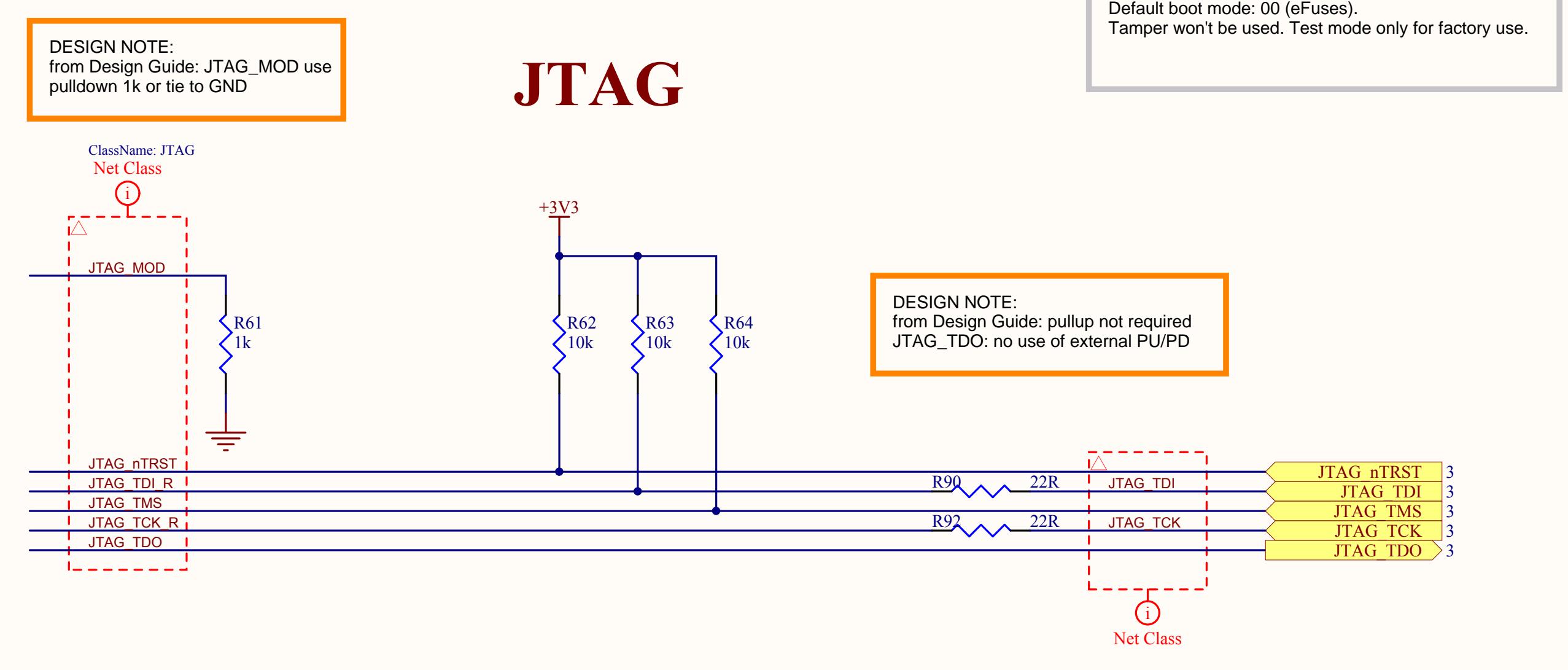
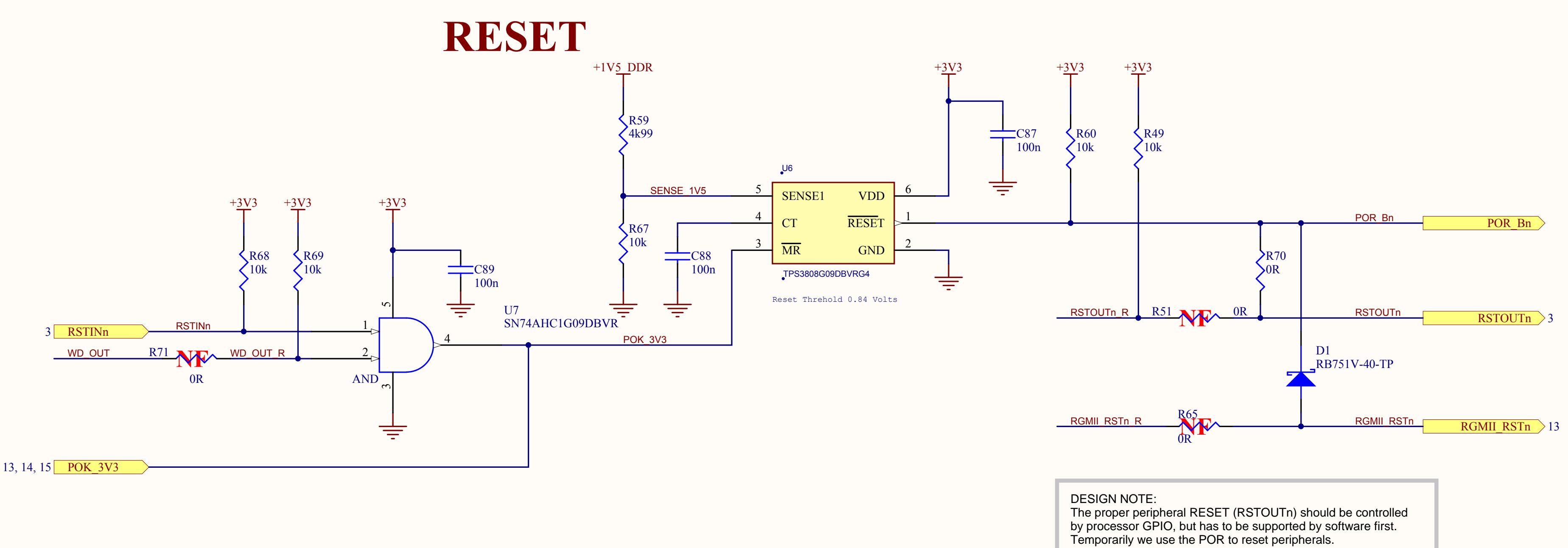
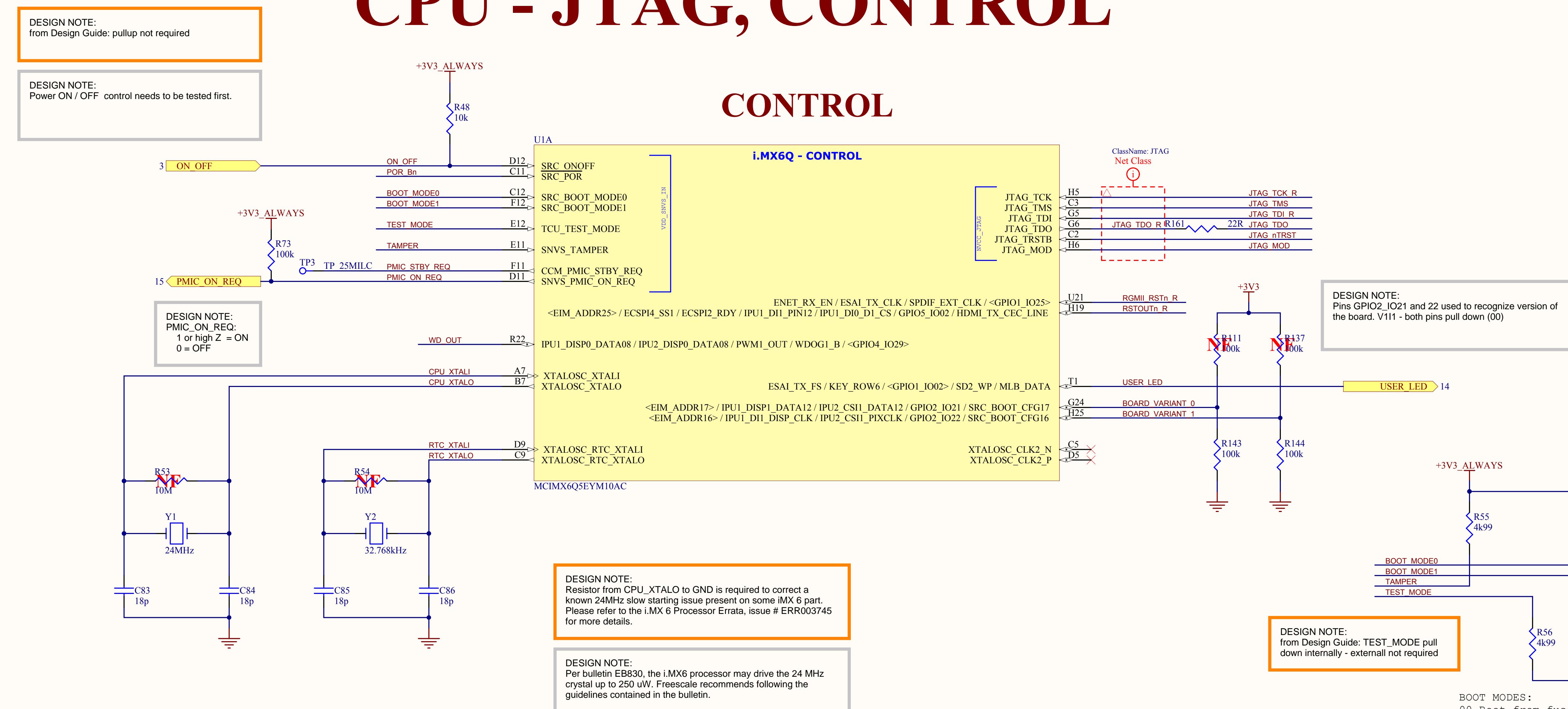


AUDIO

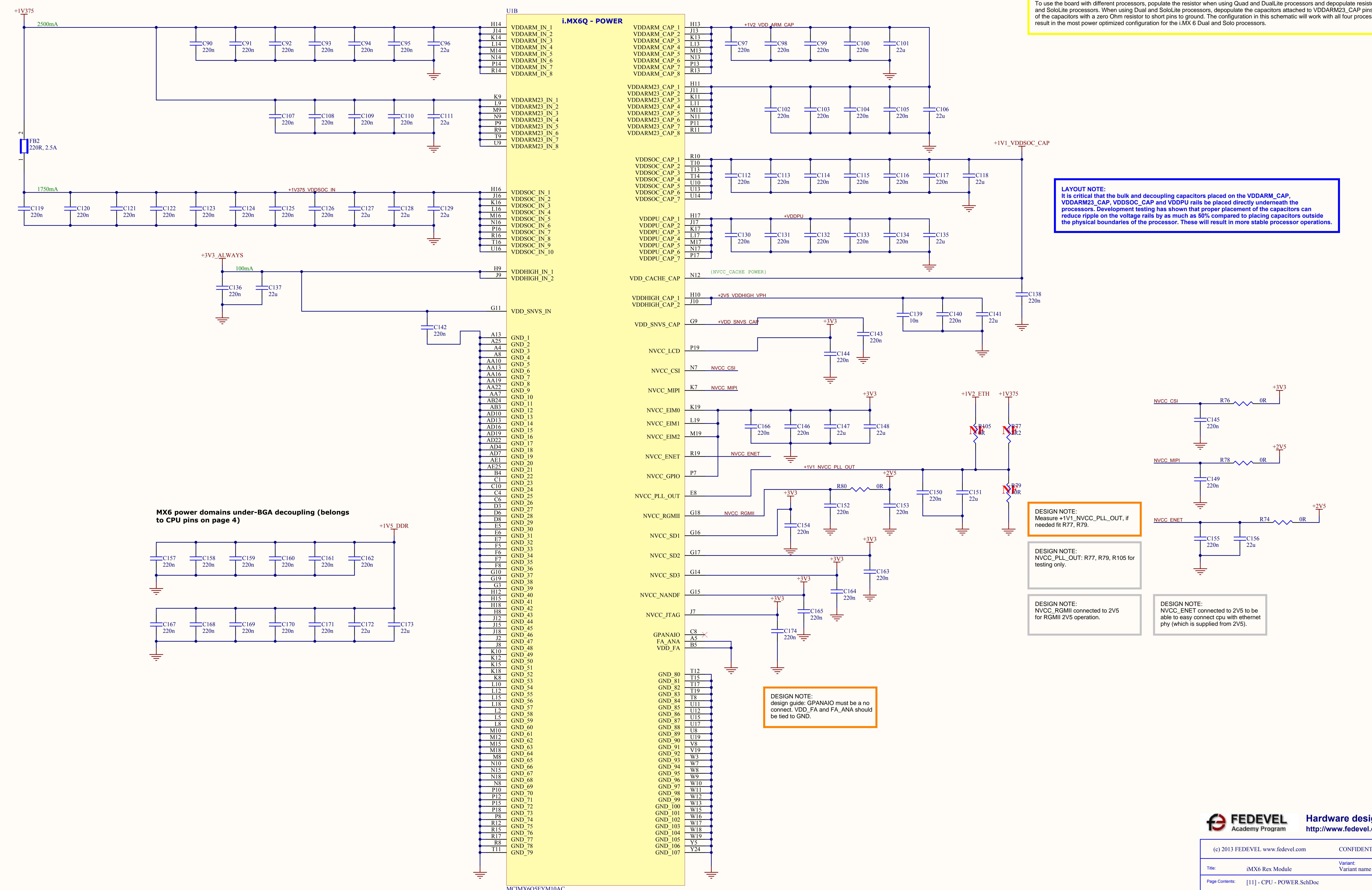


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Title:	iMX6 Rex Module
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Page Contents:	[09] - CPU - UART, AUDIO.SchDoc
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CPU - JTAG, CONTROL



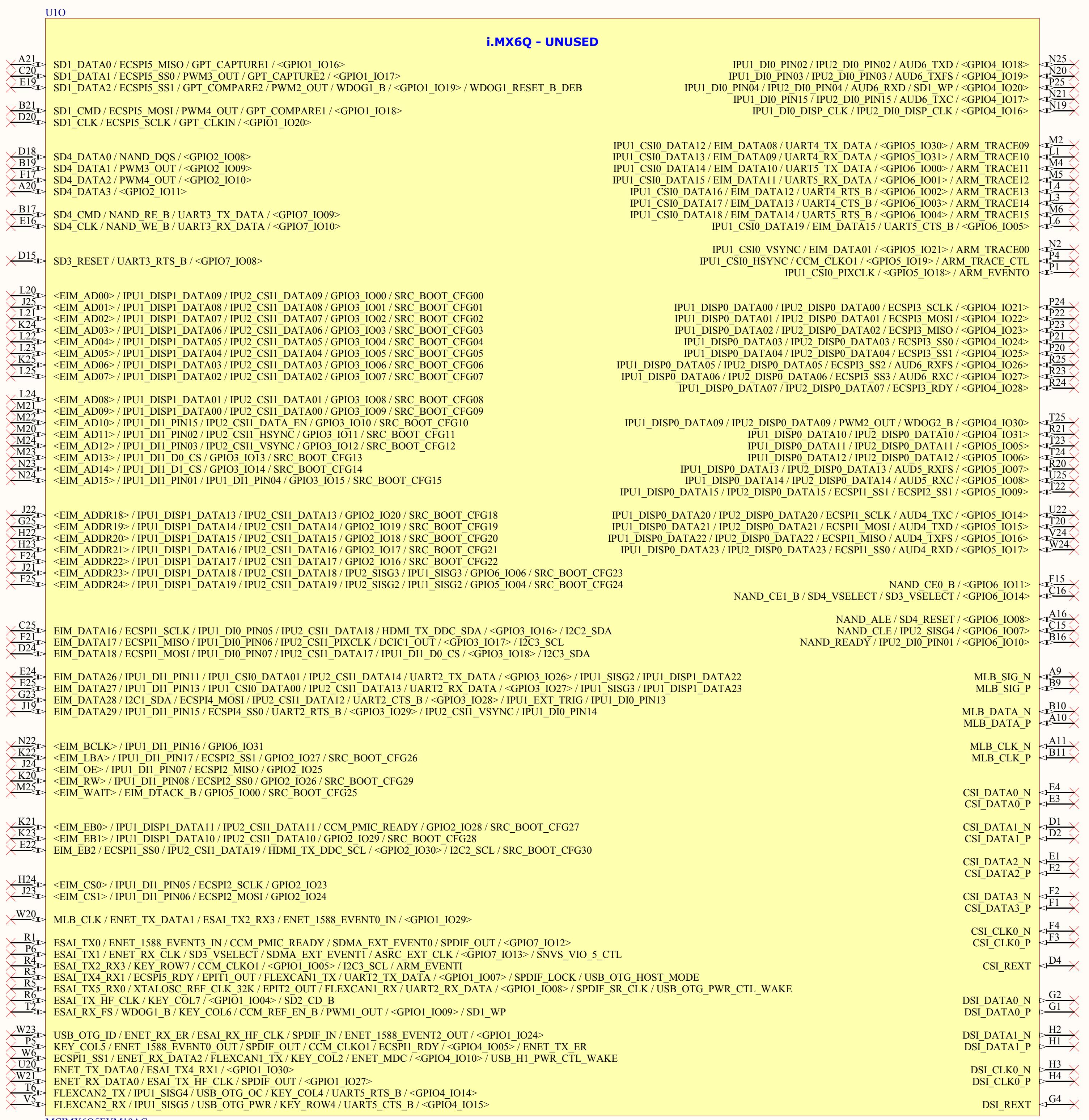
CPU - POWER



CPU - UNUSED PINS

A

A



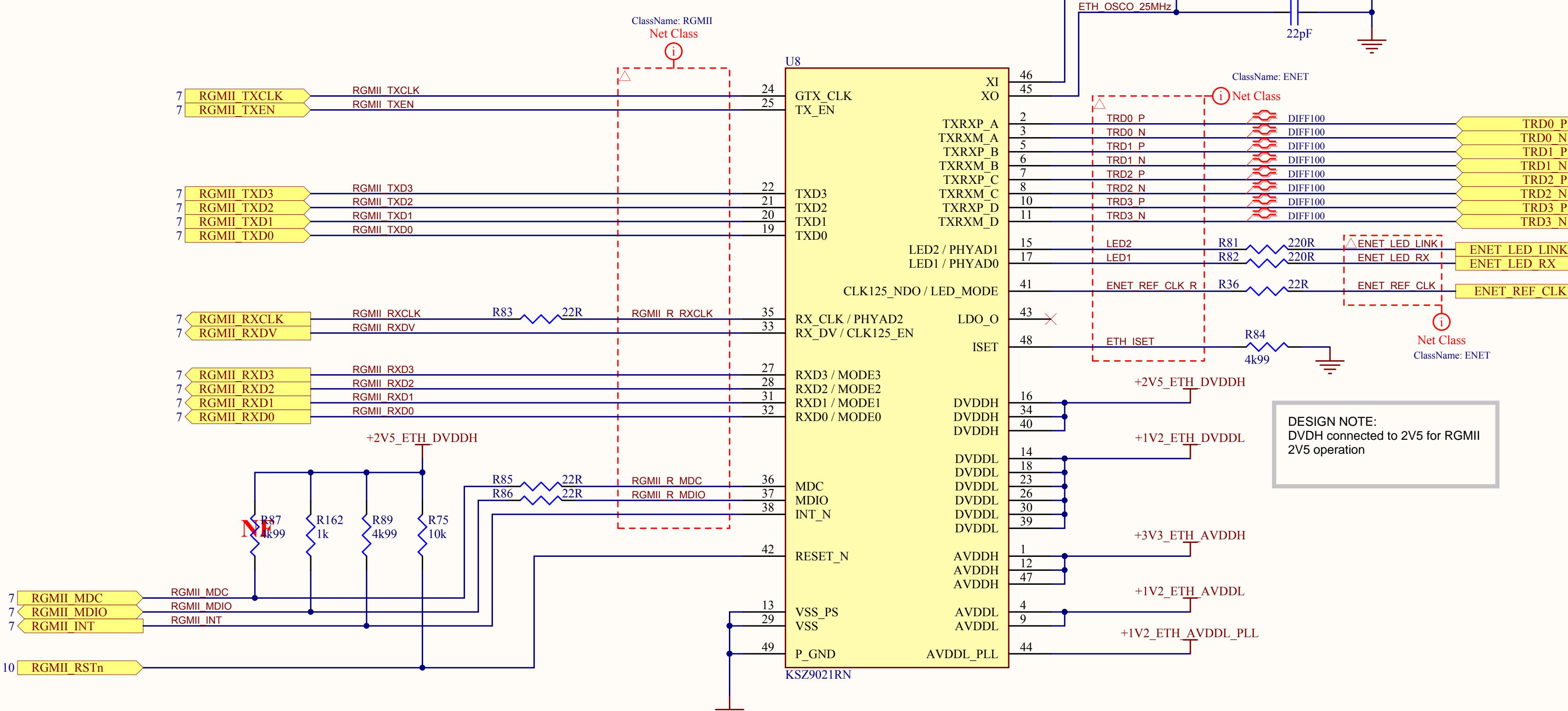
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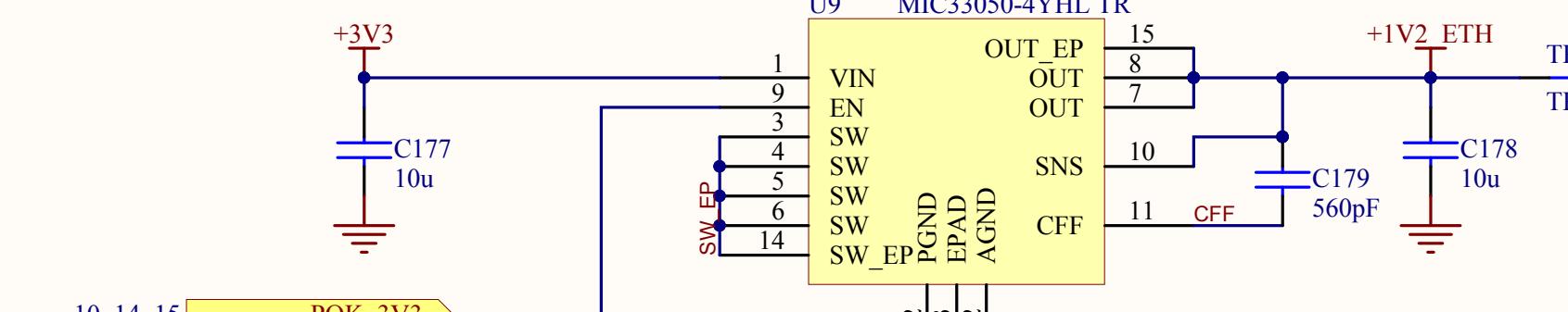
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ETHERNET PHY

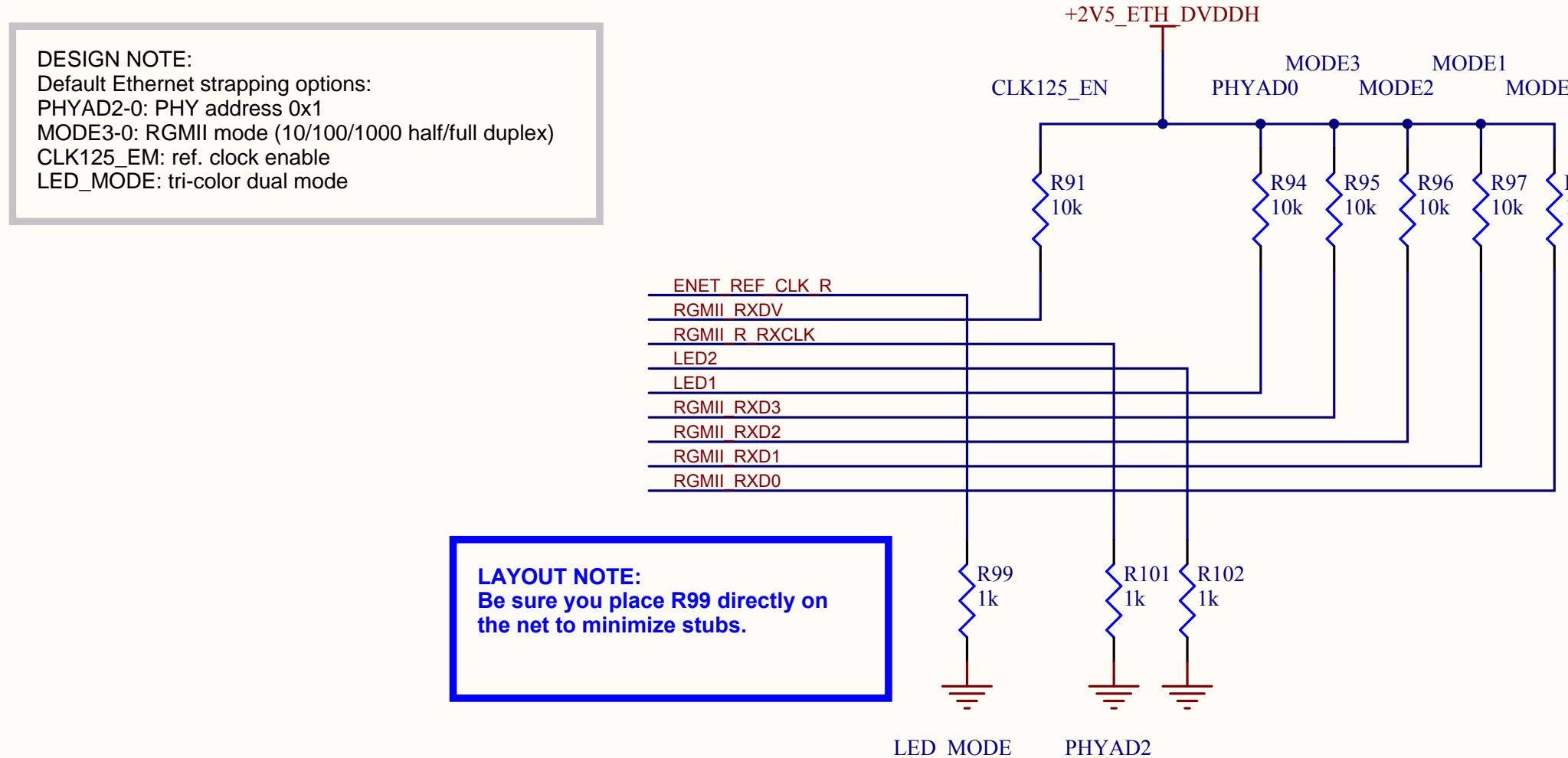
A



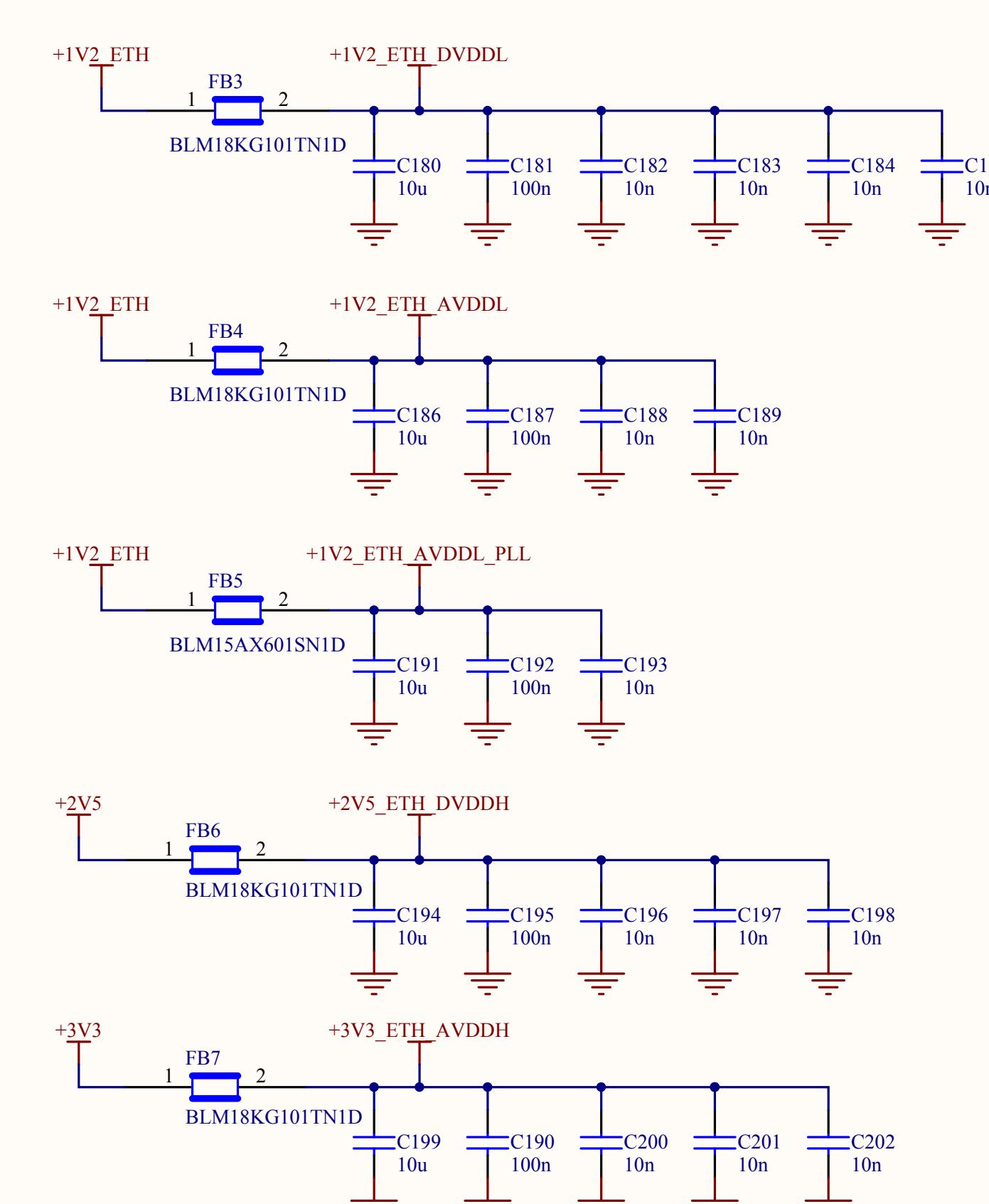
B



C

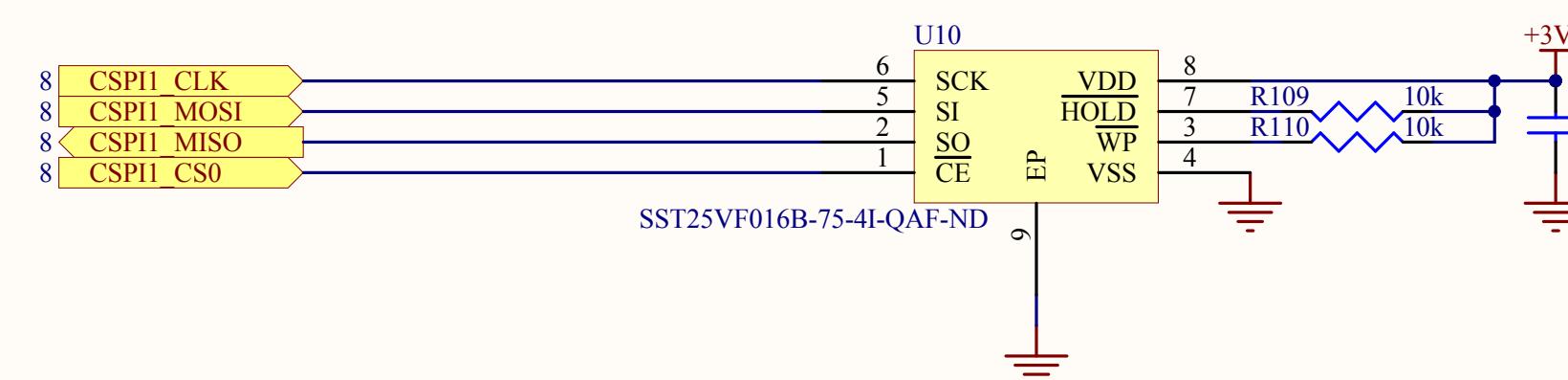


D

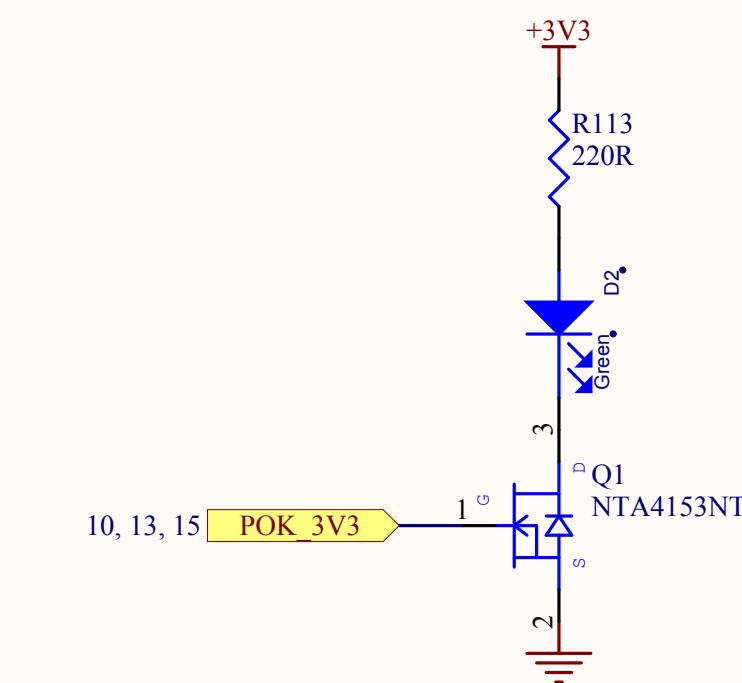


SPI FLASH, LED

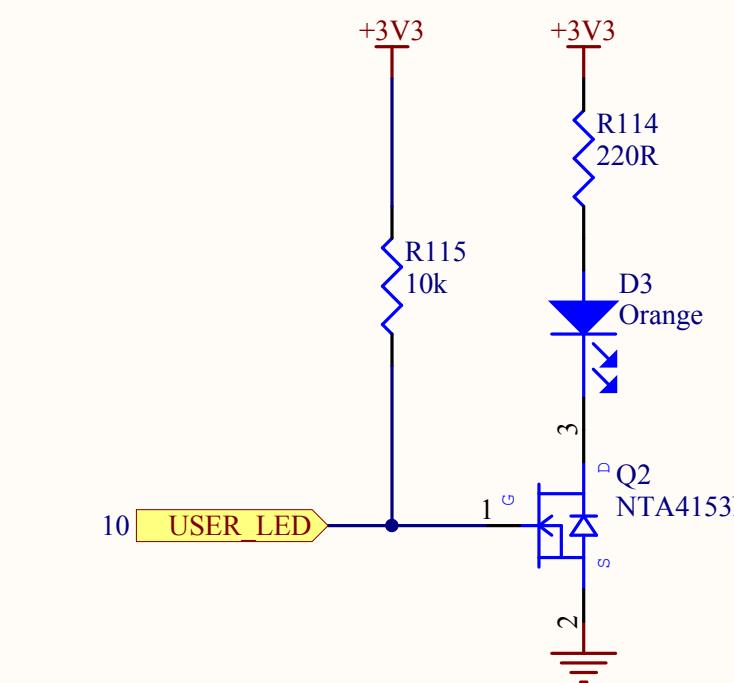
SPI NOR FLASH



POWER LED

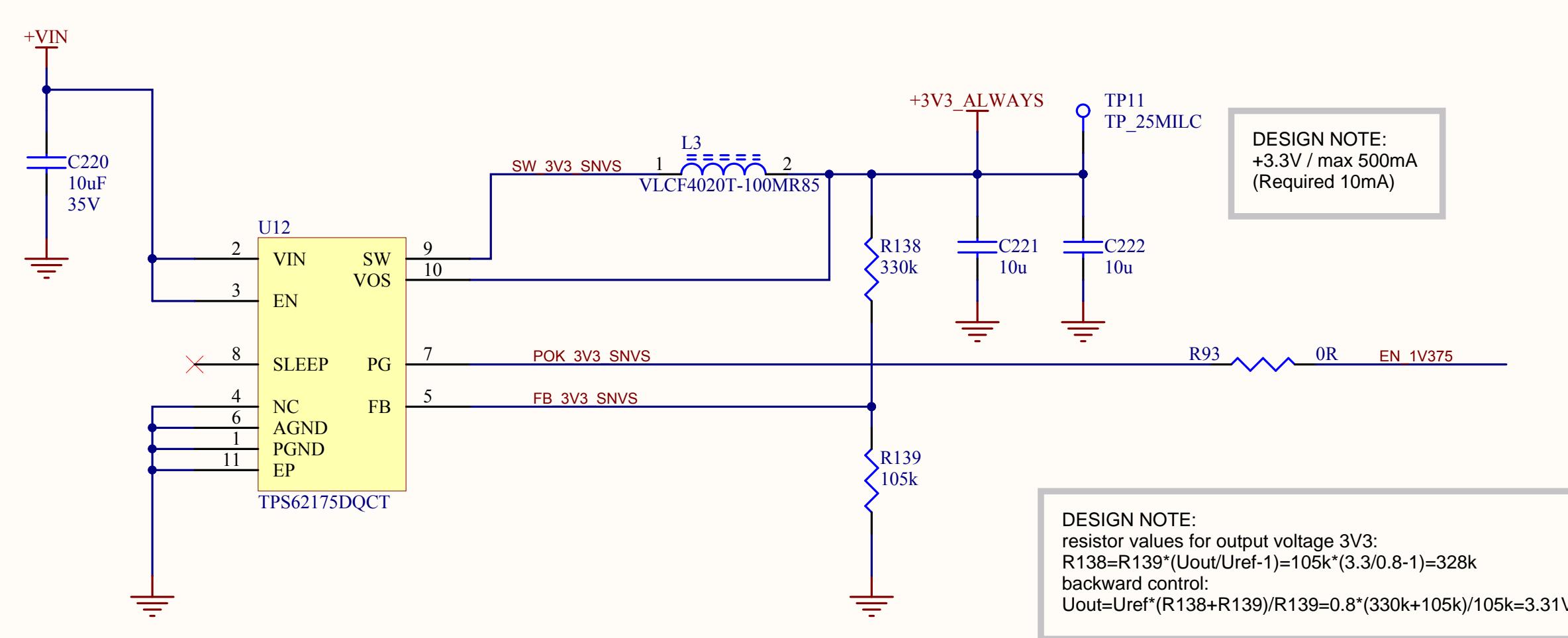
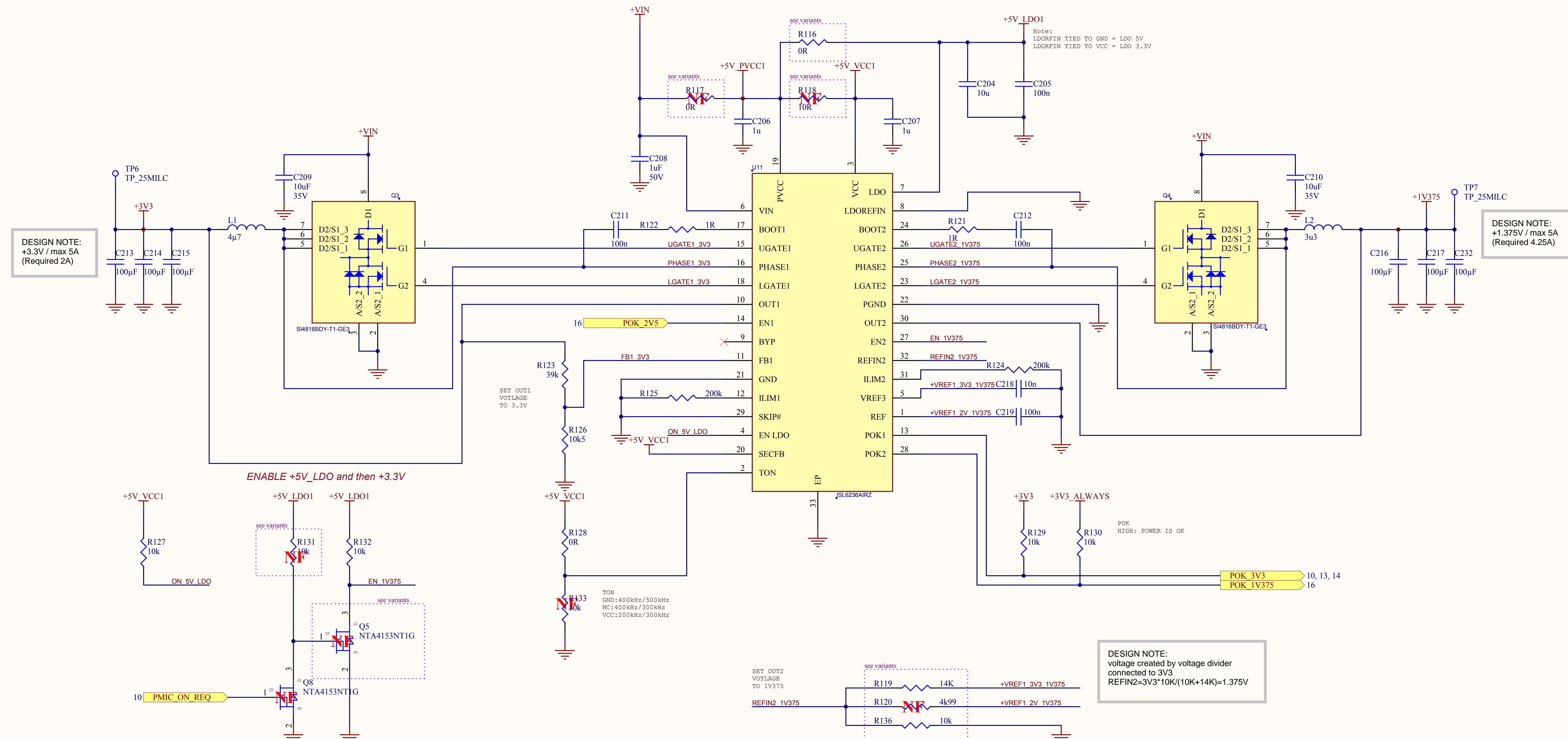


USER DEFINED LED

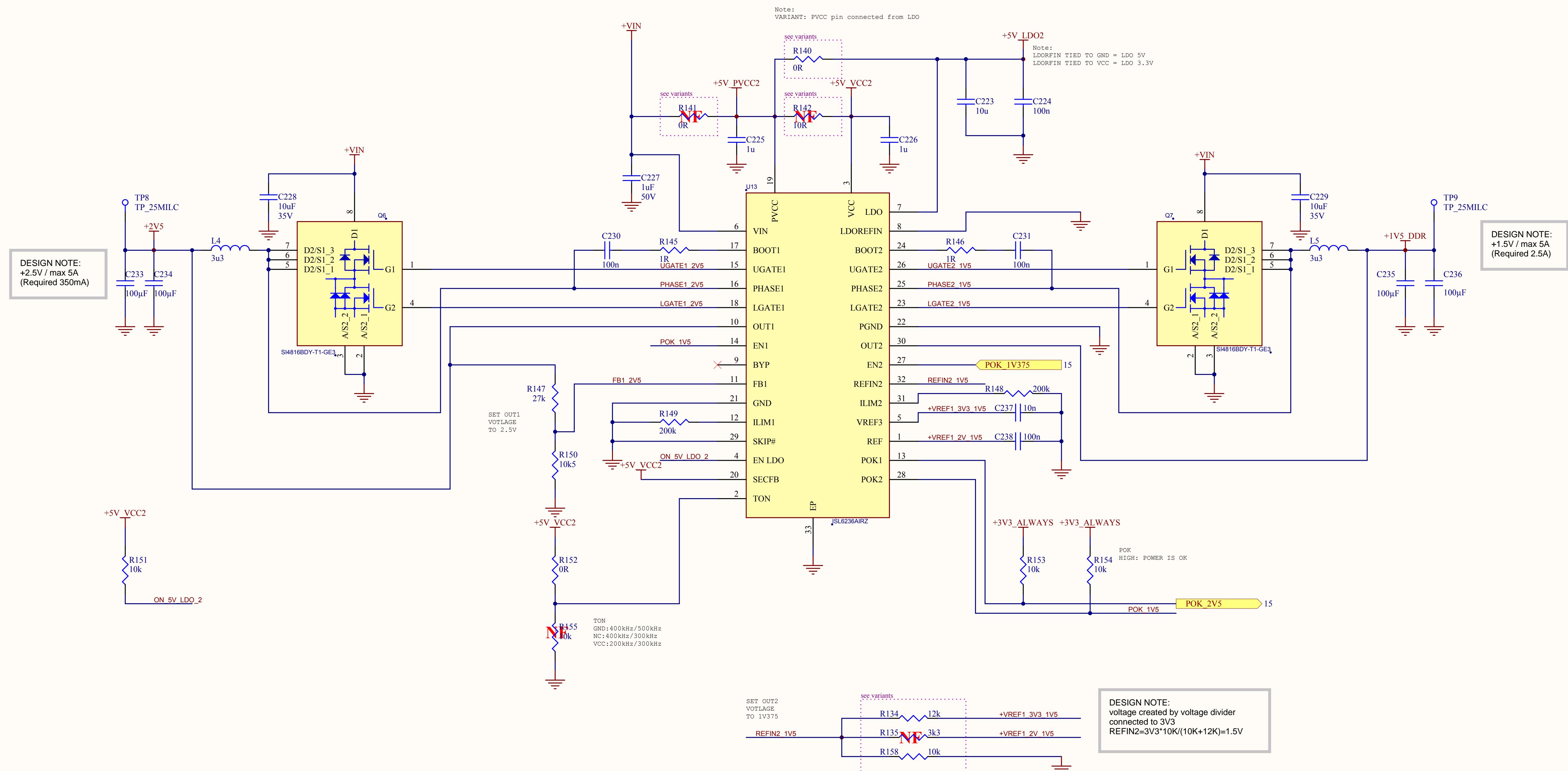


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Title:	iMX6 Rex Module
Variant:	Variant name not interpreted
Page Contents:	[14] - SPI FLASH, LED.SchDoc
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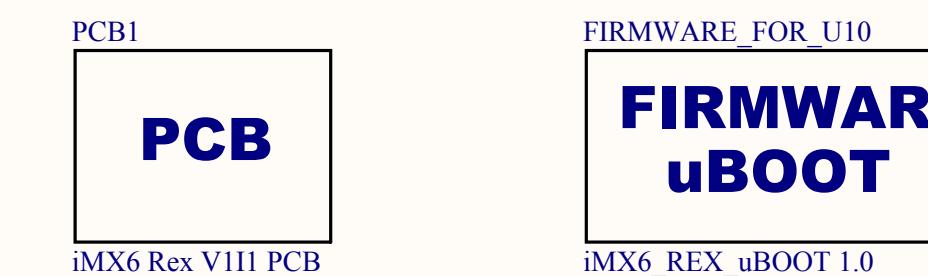
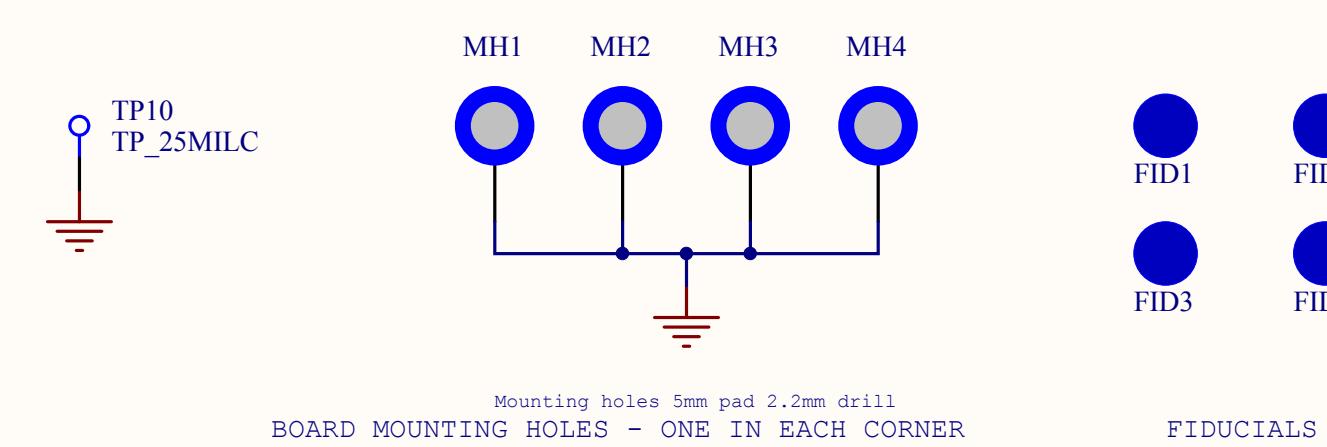
POWER +3.3V, +1.375V CON



POWER +2.5V, +1.5V CON

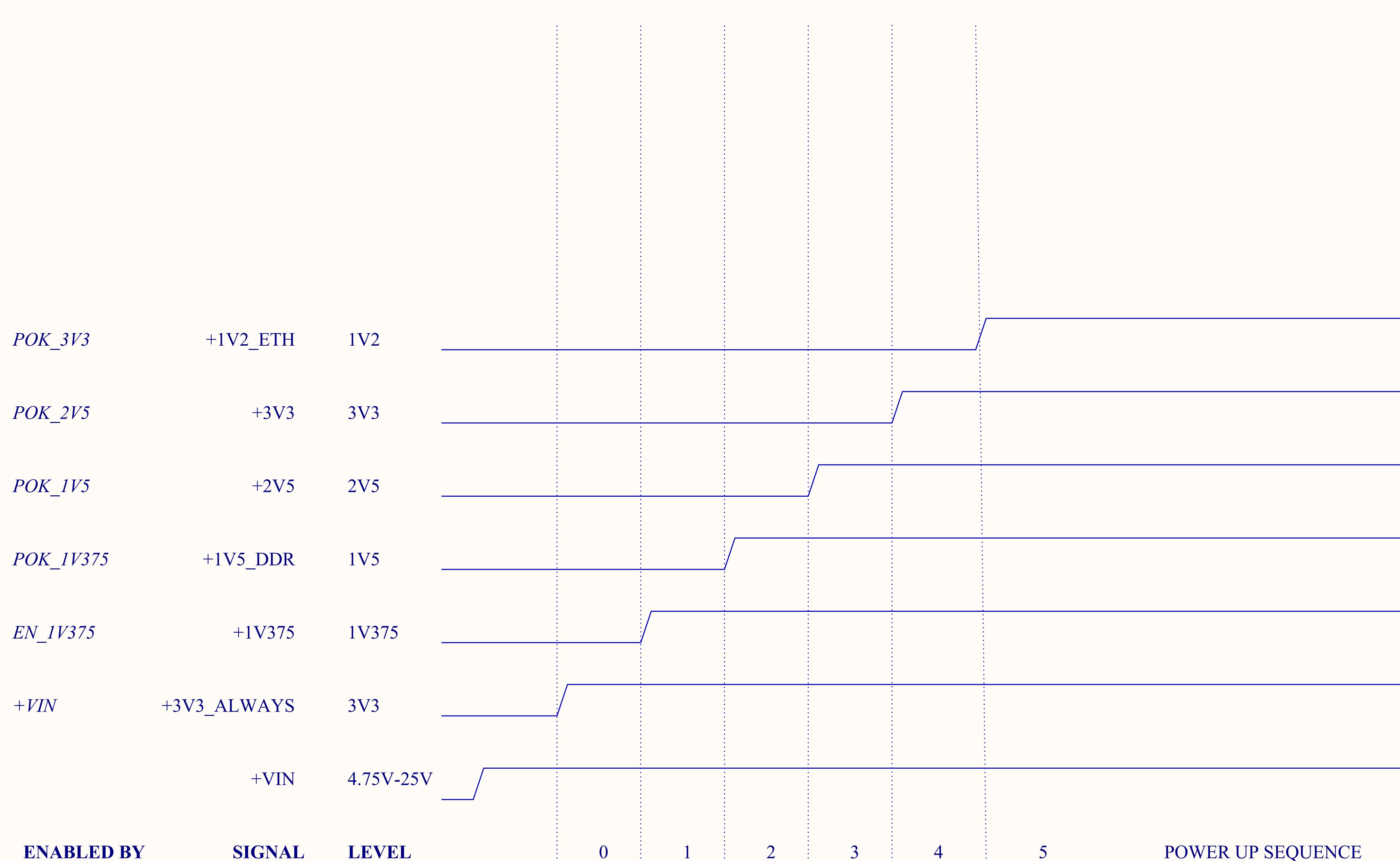


MECHANICAL



CPU - POWER SEQUENCING

+USB_VBUS	5V		
+DDR_VREF	0V75	+1V5_DDR	ref. for DDR memories, gen. with volt. divider
+1V2_VDD_ARM_CAP	1V2	iMX	cpu, core caps
+1V1_VDDSOC_CAP	1V1	iMX	core caps, cpu-sata, cpu-pcie, cpu-hdmi
OTHER USED SIGNAL	LEVEL	GEN BY	SUPPLIED FROM SIGNAL



ENABLED BY	SIGNAL	LEVEL

POWER UP SEQUENCE

DOC: REVISION HISTORY

A A

B B

C C

D D
CLOCKS (CPU & PCI)

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Page Contents: [19] - DOC REVISION HISTORY.SchDoc		Checked by
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[01] - COVER PAGE.SchDoc
[01] - COVER PAGE.SchDoc

[02] - BLOCK DIAGRAM.SchDoc
[02] - BLOCK DIAGRAM.SchDoc

[03] - CONNECTORS.SchDoc
[03] - CONNECTORS.SchDoc

[04] - CPU - DDR3, DDR3 MEM.SchDoc
[04] - CPU - DDR3, DDR3 MEM.SchDoc

[05] - CPU - PCIE, SATA.SchDoc
[05] - CPU - PCIE, SATA.SchDoc

[06] - CPU - HDMI, LVDS.SchDoc
[06] - CPU - HDMI, LVDS.SchDoc

[07] - CPU - USB, ETHERNET.SchDoc
[07] - CPU - USB, ETHERNET.SchDoc

[08] - CPU - SPI, I2C, SD, MMC.SchDoc
[08] - CPU - SPI, I2C, SD, MMC.SchDoc

A

A

TEMPLATE NOTES

Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Company, Project and Version Revision

Mark Not Fitted Components as
NF

Net Class Example



Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Title

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

[09] - CPU - UART, AUDIO.SchDoc
[09] - CPU - UART, AUDIO.SchDoc

[10] - CPU - JTAG, CONTROL.SchDoc
[10] - CPU - JTAG, CONTROL.SchDoc

[11] - CPU - POWER.SchDoc
[11] - CPU - POWER.SchDoc

[12] - CPU - UNUSED.SchDoc
[12] - CPU - UNUSED.SchDoc

[13] - ETHERNET PHY.SchDoc
[13] - ETHERNET PHY.SchDoc

[14] - SPI FLASH, LEDS.SchDoc
[14] - SPI FLASH, LEDS.SchDoc

[15] - PWR 3V3, 1V375.SchDoc
[15] - PWR 3V3, 1V375.SchDoc

[16] - PWR 2V5, 1V5.SchDoc
[16] - PWR 2V5, 1V5.SchDoc

[17] - MECH.SchDoc
[17] - MECH.SchDoc

[18] - POWER SEQUENCING.SchDoc
[18] - POWER SEQUENCING.SchDoc

[19] - DOC REVISION HISTORY.SchDoc
[19] - DOC REVISION HISTORY.SchDoc



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Title:	iMX6 Rex Module
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