

# iMX6 Rex Module

## Variant: Prototype

26. 9. 2013  
V1I1

RELEASED 27-SEP-2013

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### DESIGN CONSIDERATIONS

DESIGN NOTE:  
Example text for debug notes.

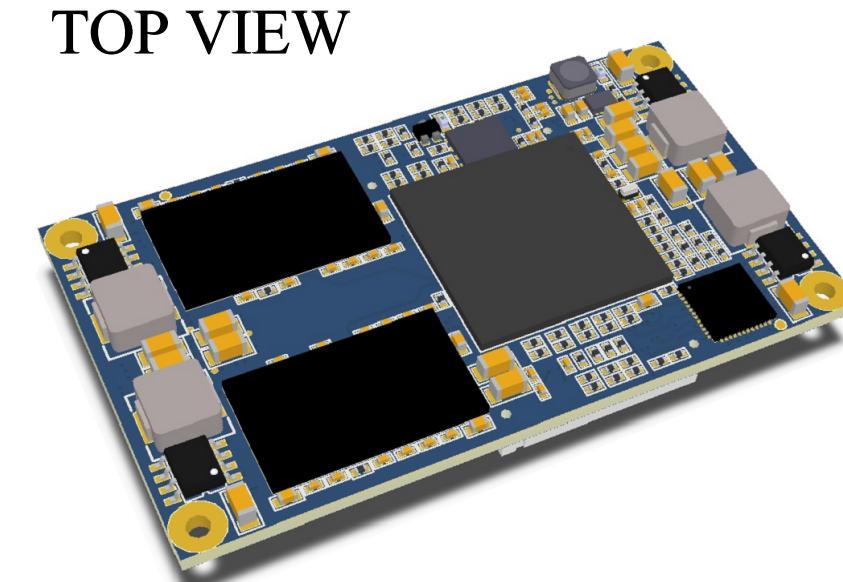
DESIGN NOTE:  
Example text for informational design notes .

DESIGN NOTE:  
Example text for cautionary design notes.

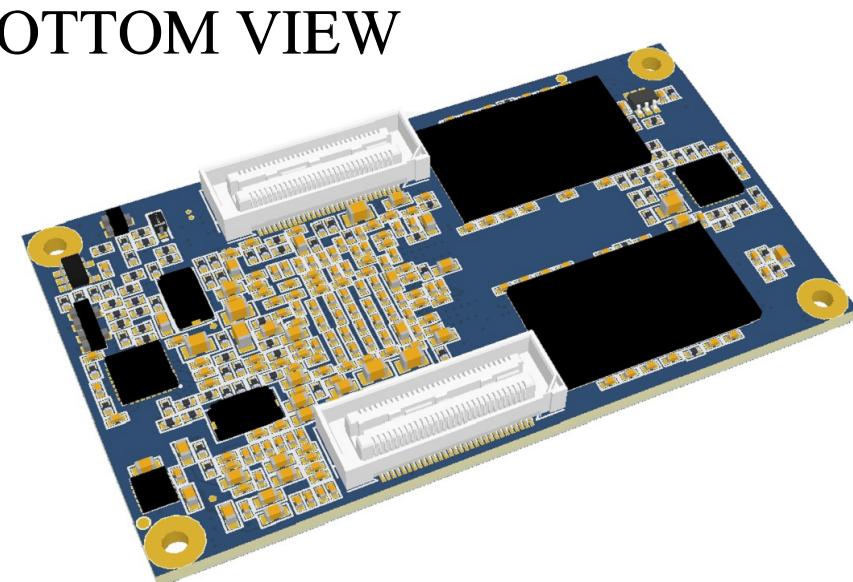
DESIGN NOTE:  
Example text for critical design notes.

LAYOUT NOTE:  
Example text for critical layout guidelines.

TOP VIEW



BOTTOM VIEW

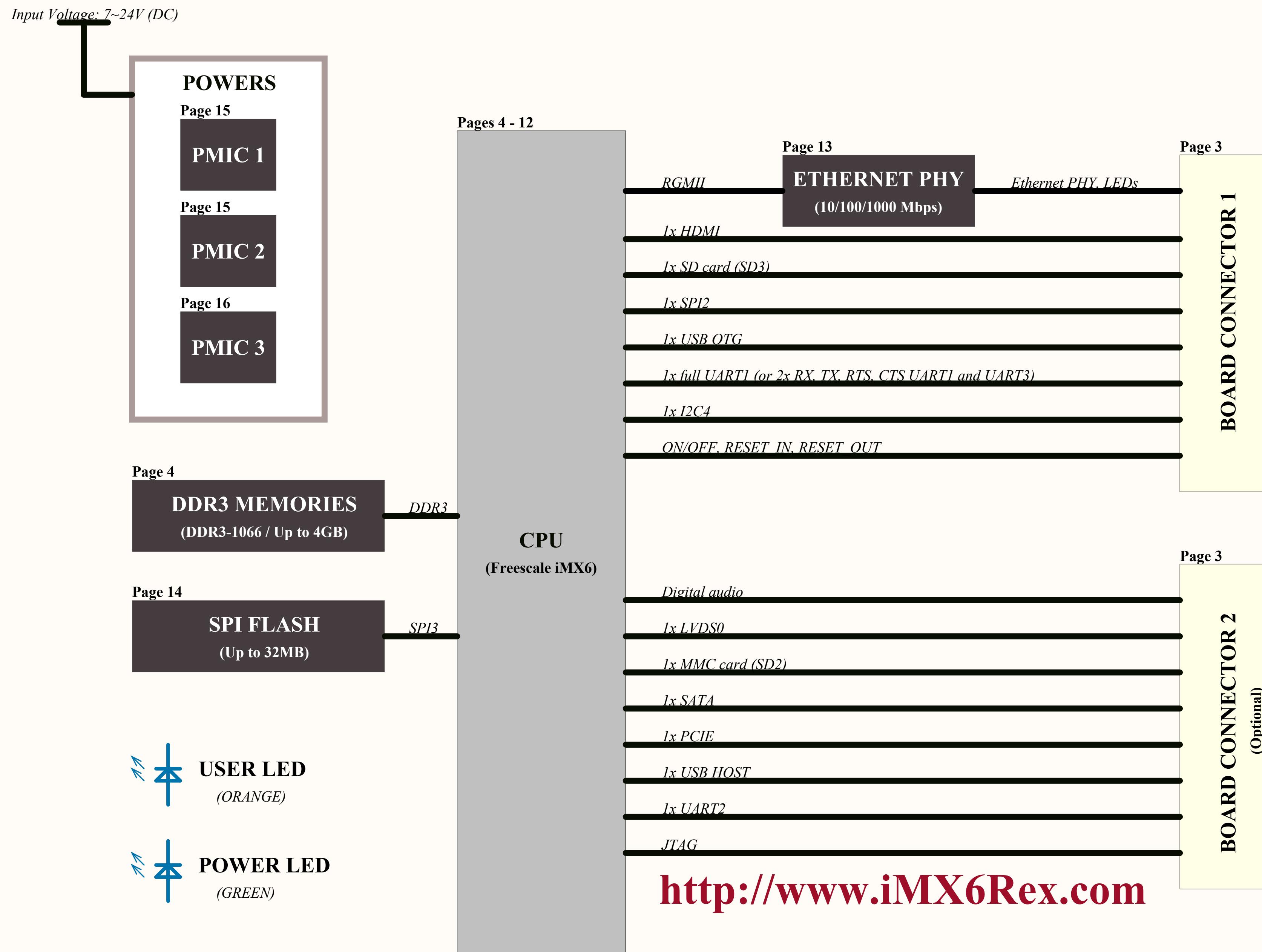


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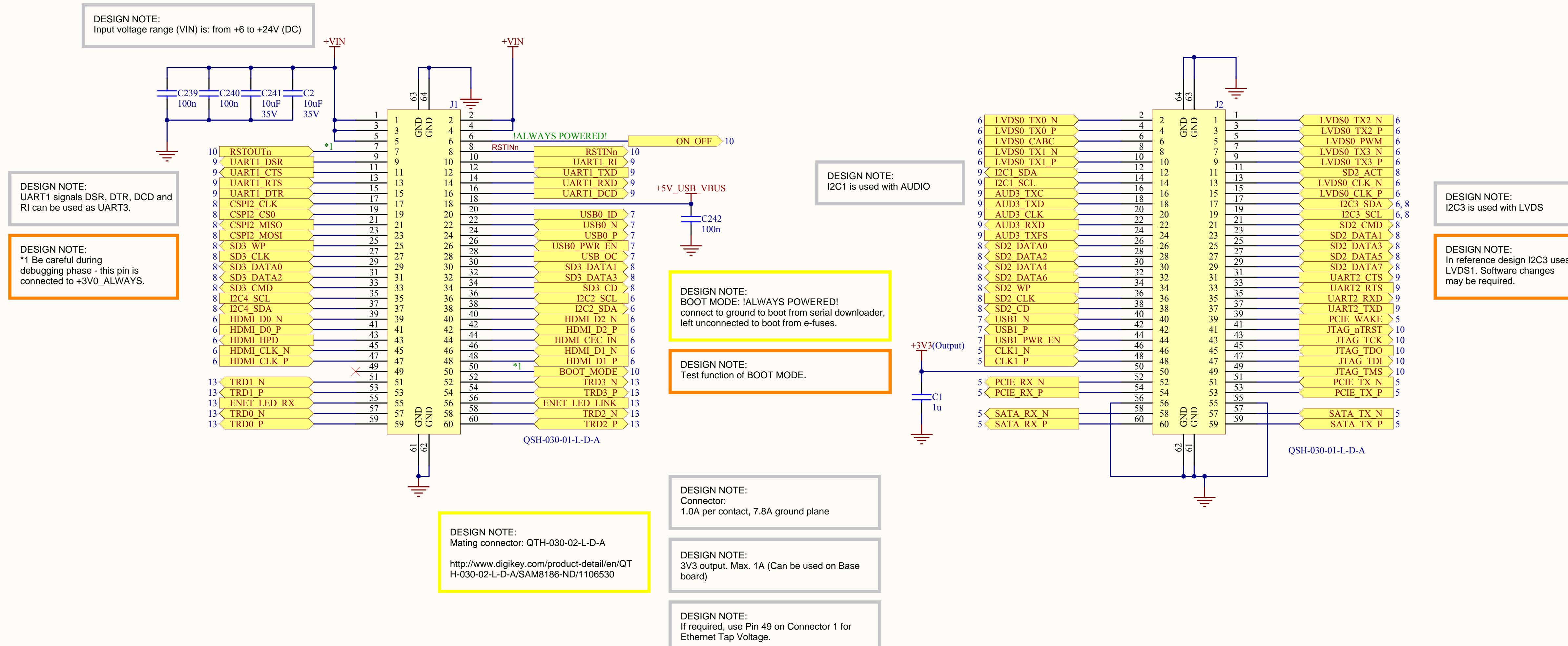
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# iMX6 Rex Module

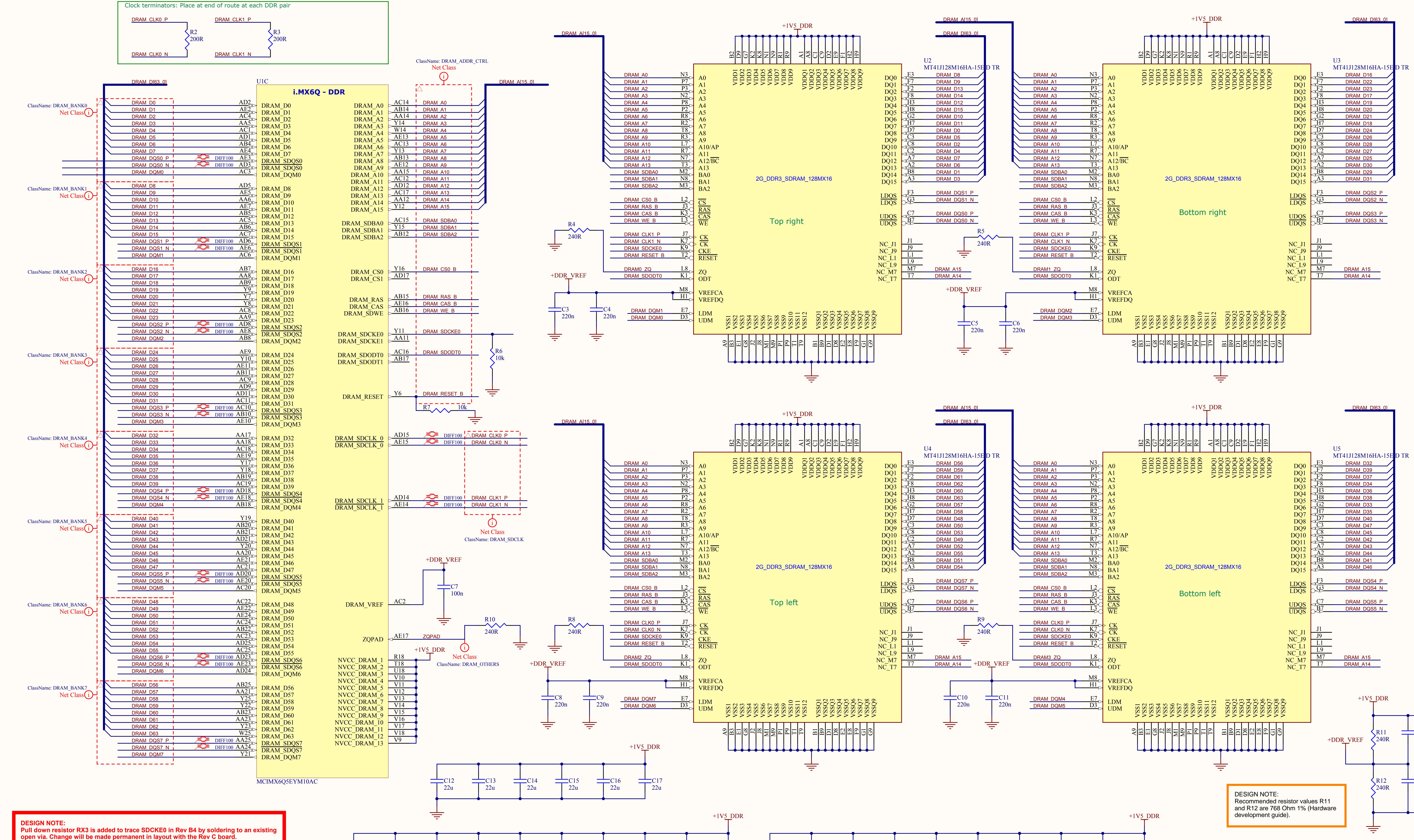
## (Block Diagram)



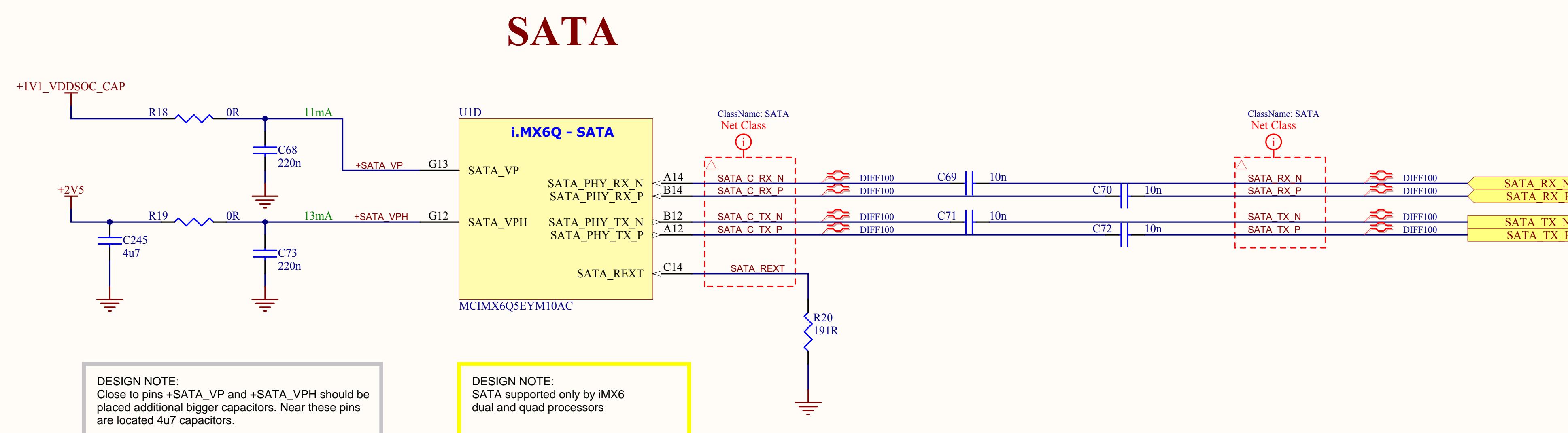
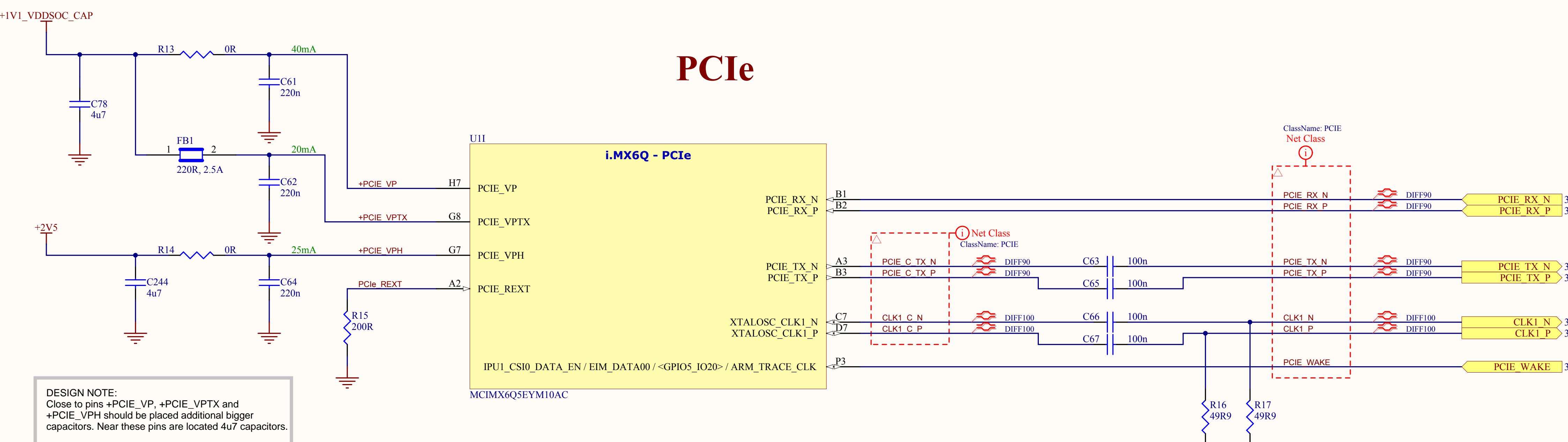
# CONNECTORS



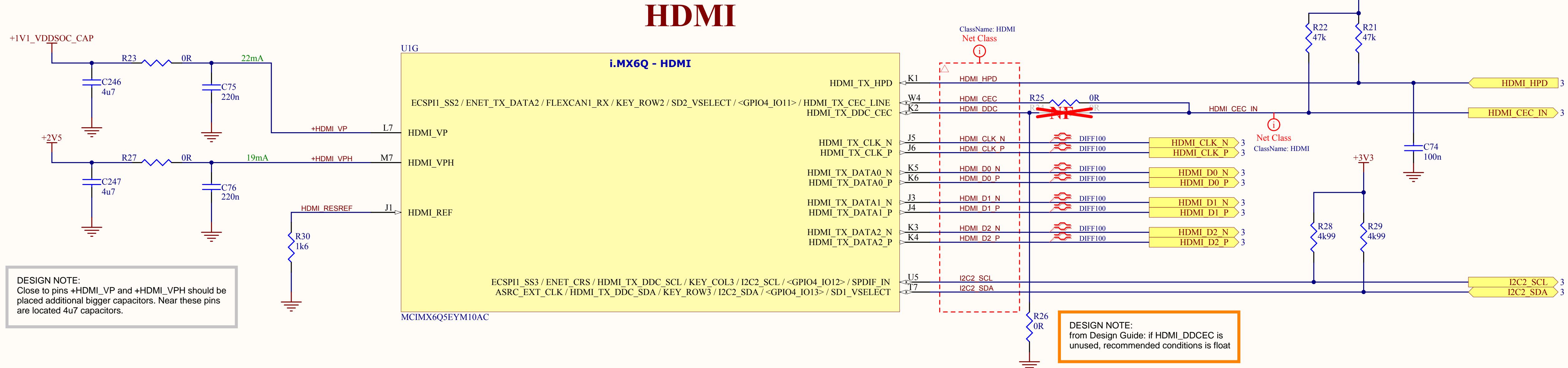
# CPU - DDR3, DDR3 MEM



# CPU - SATA, PCIe

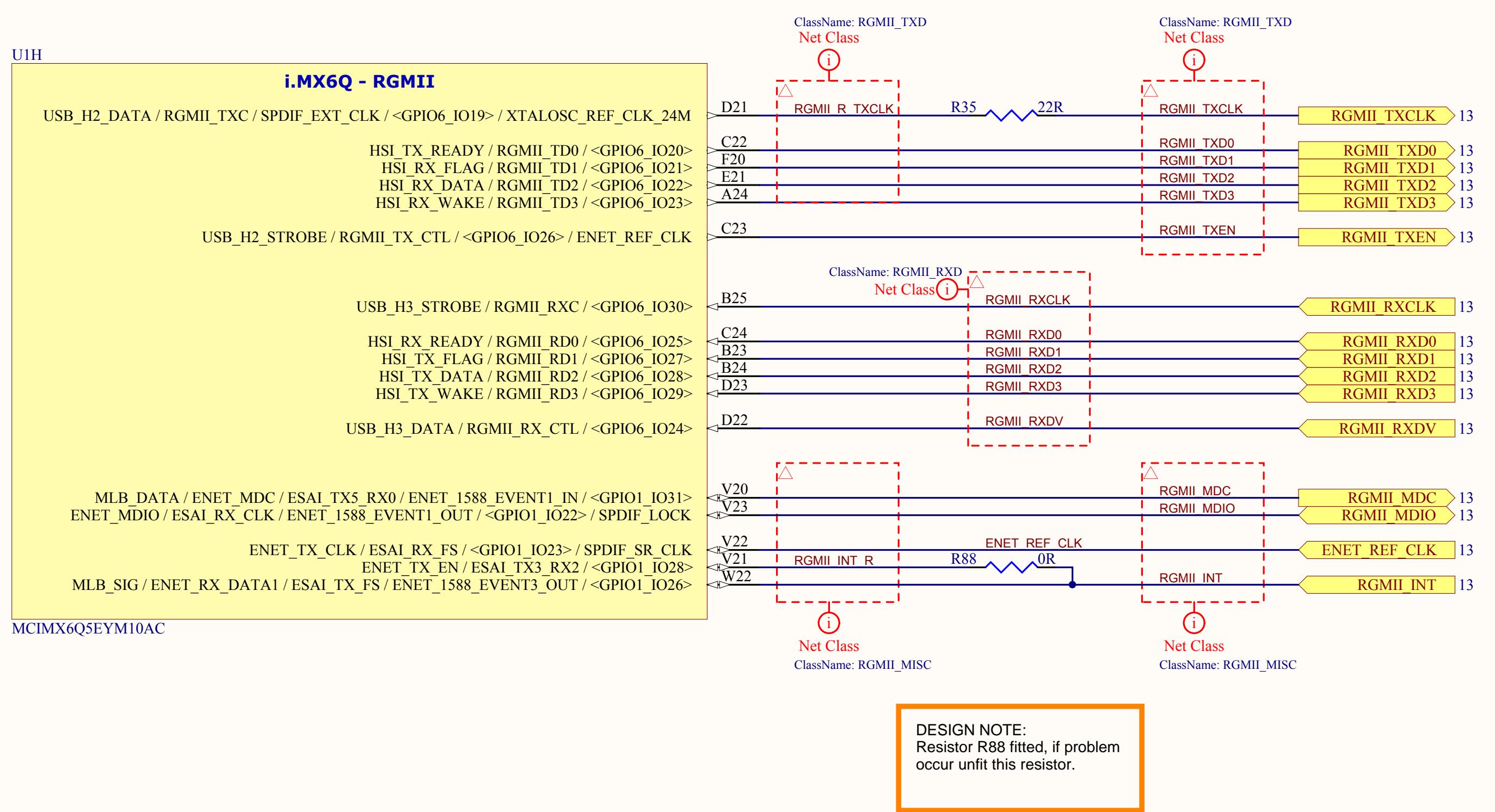


# CPU - HDMI, LVDS

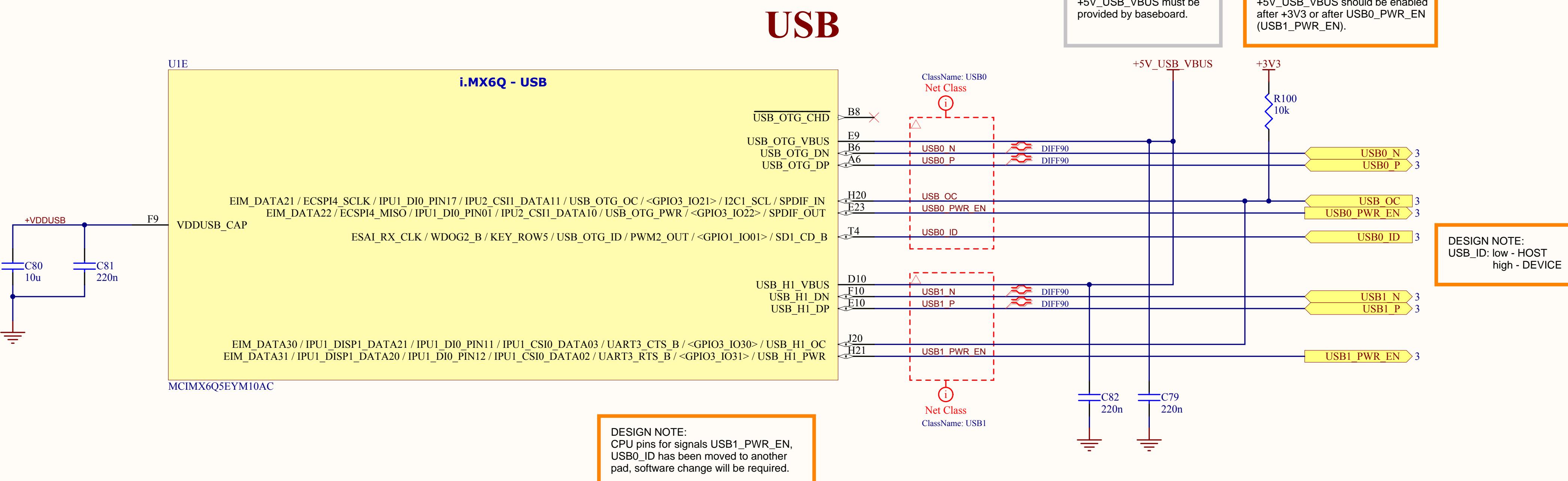


# CPU - USB, ETHERNET

## ETHERNET

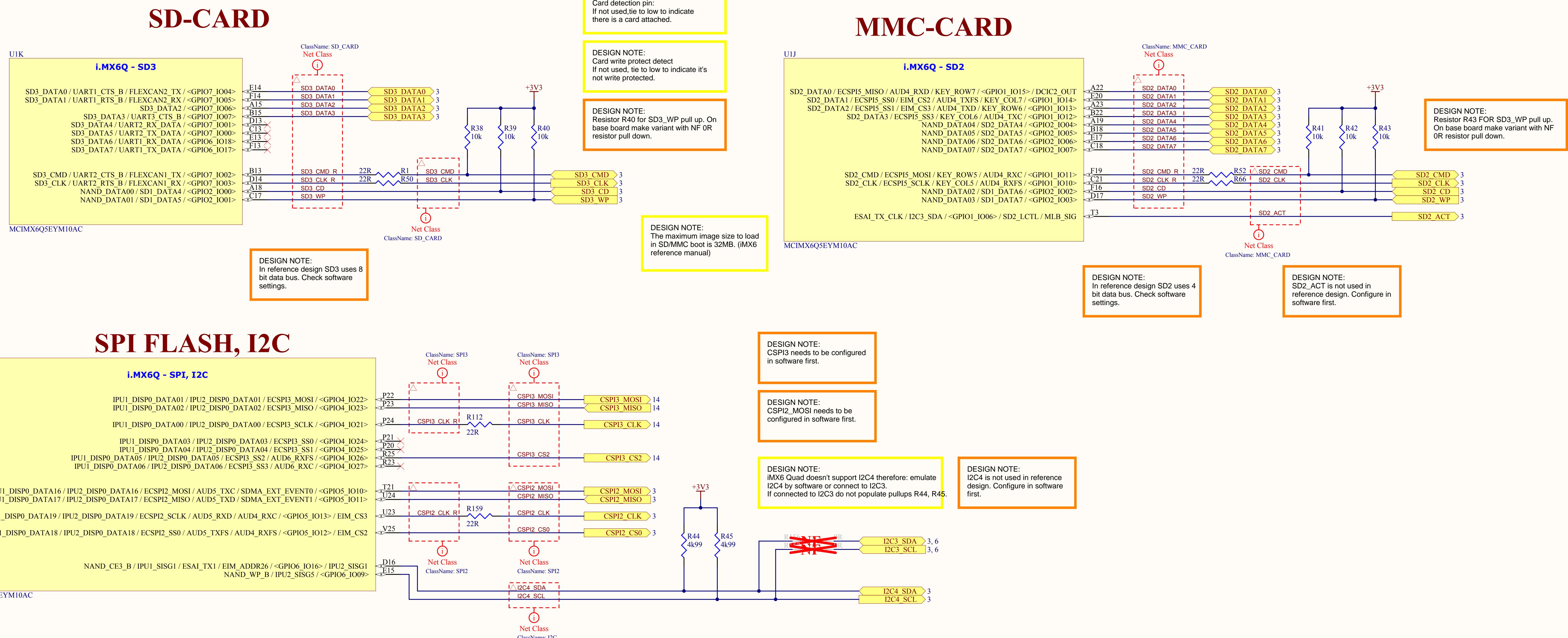


## USB



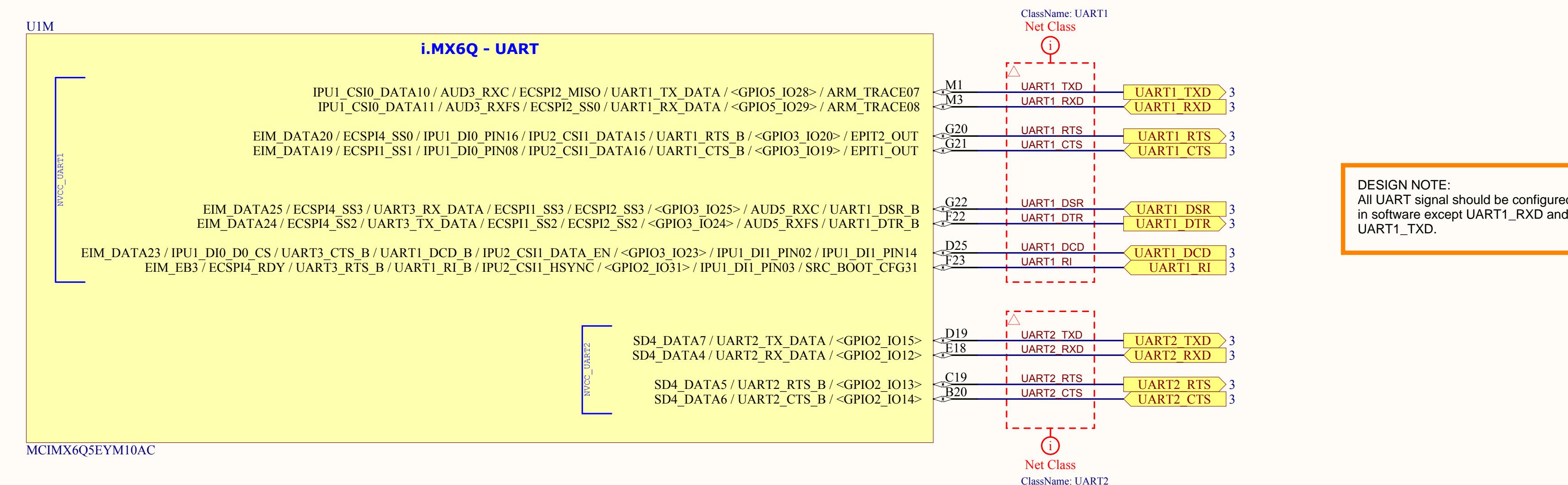
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# CPU - SPI, I2C, SD, MMC

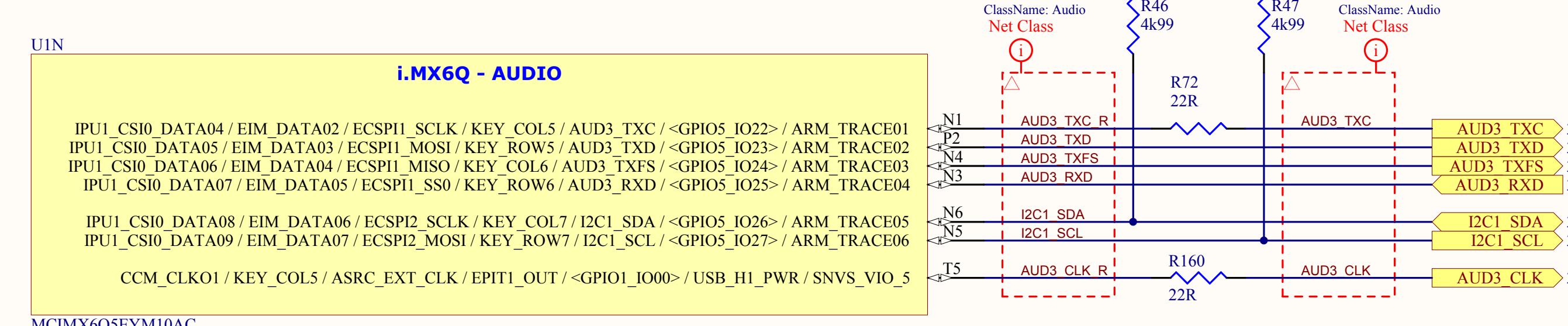


# CPU - UART, AUDIO

## UART

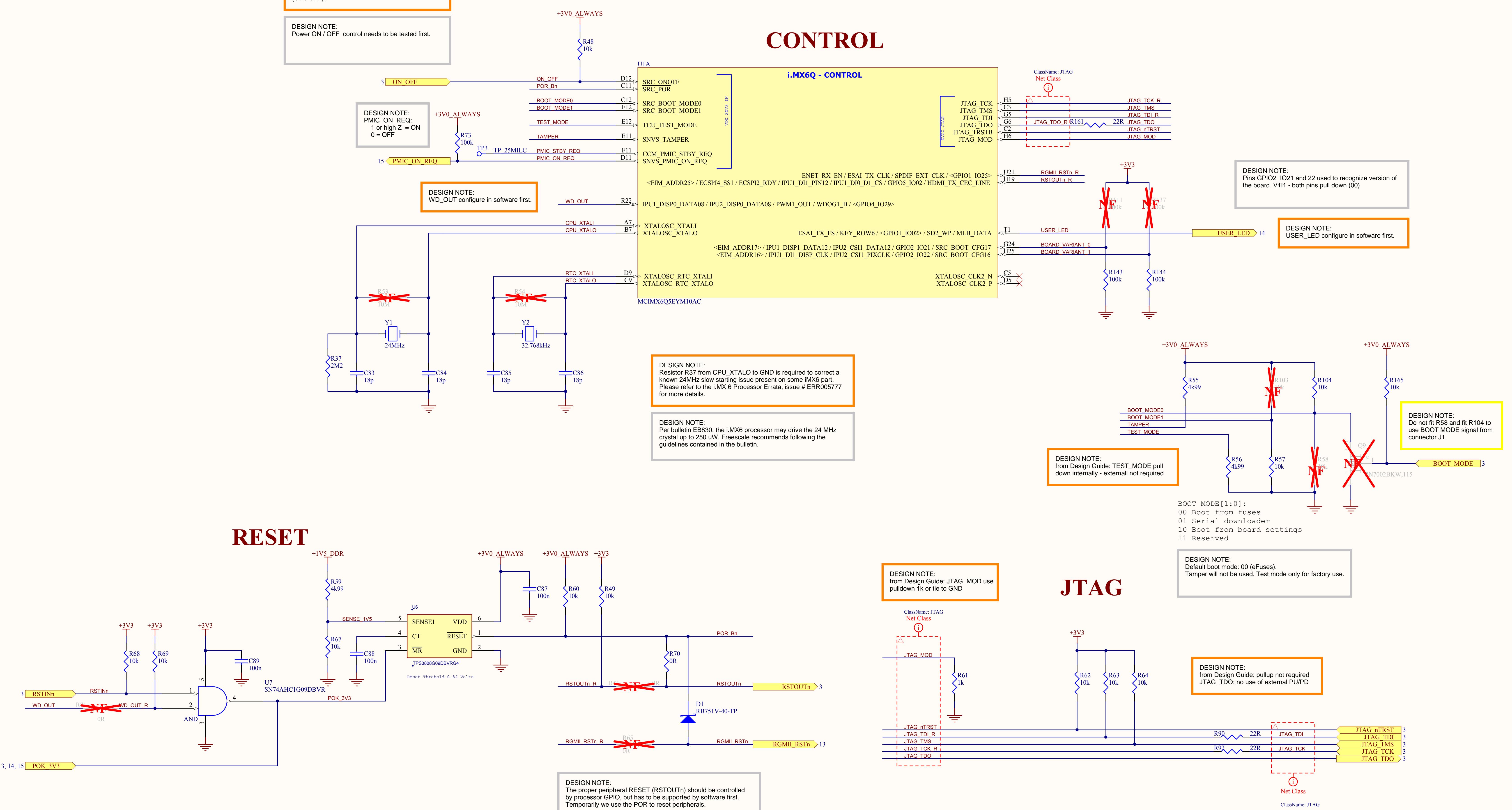


## AUDIO

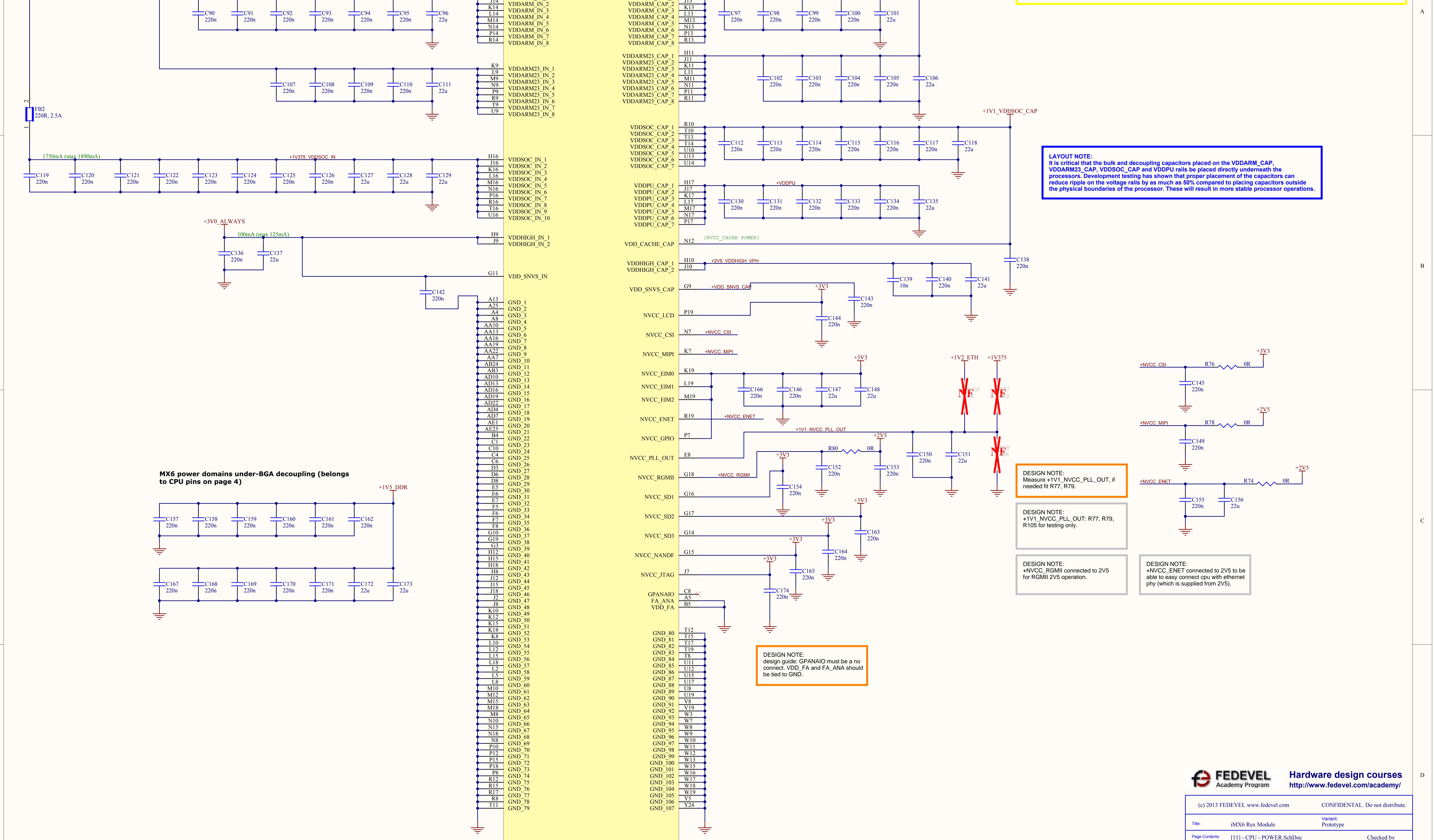


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# CPU - JTAG, CONTROL



# CPU - POWER



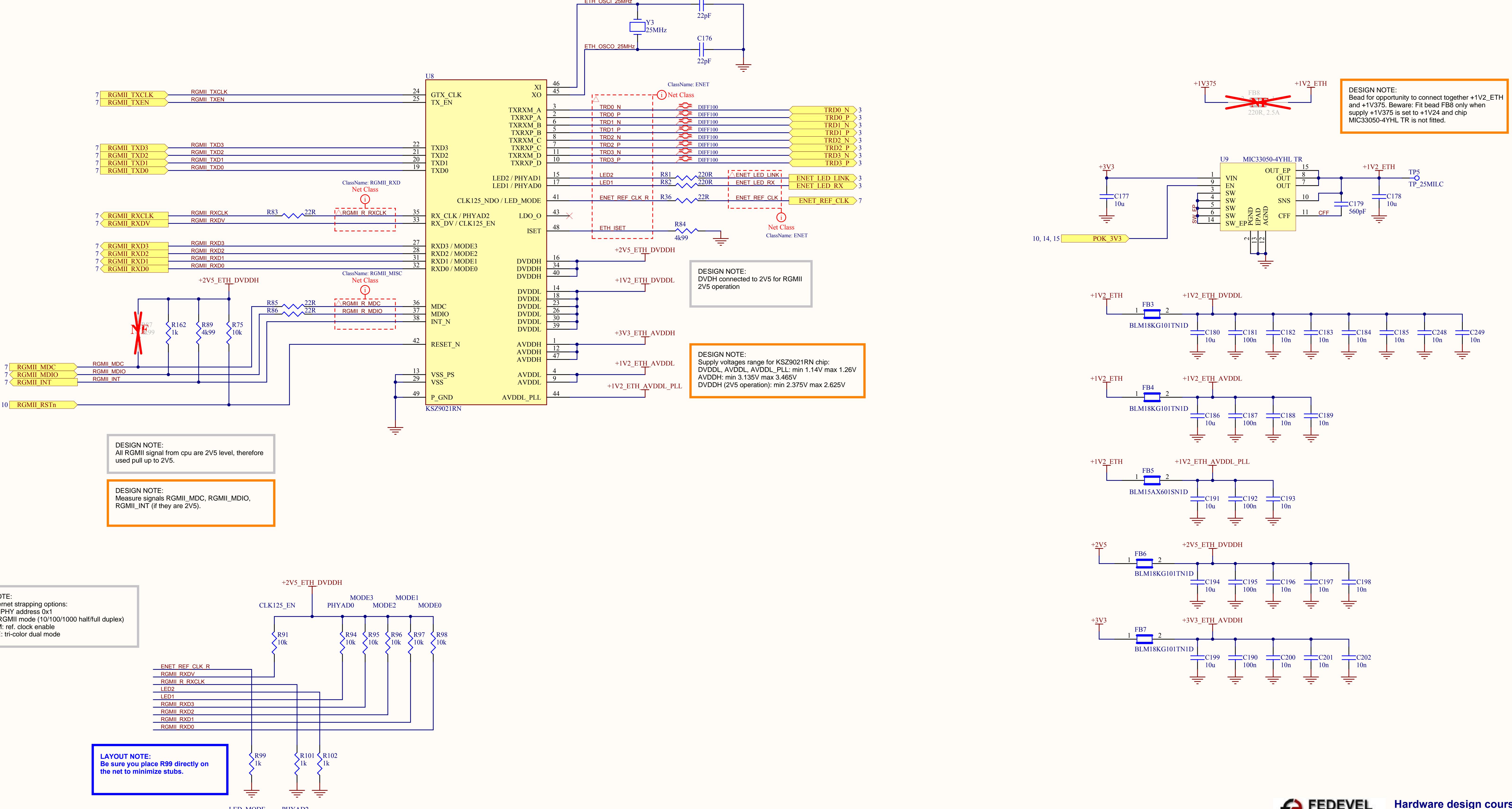
# CPU - UNUSED PINS



# ETHERNET PHY

A

A



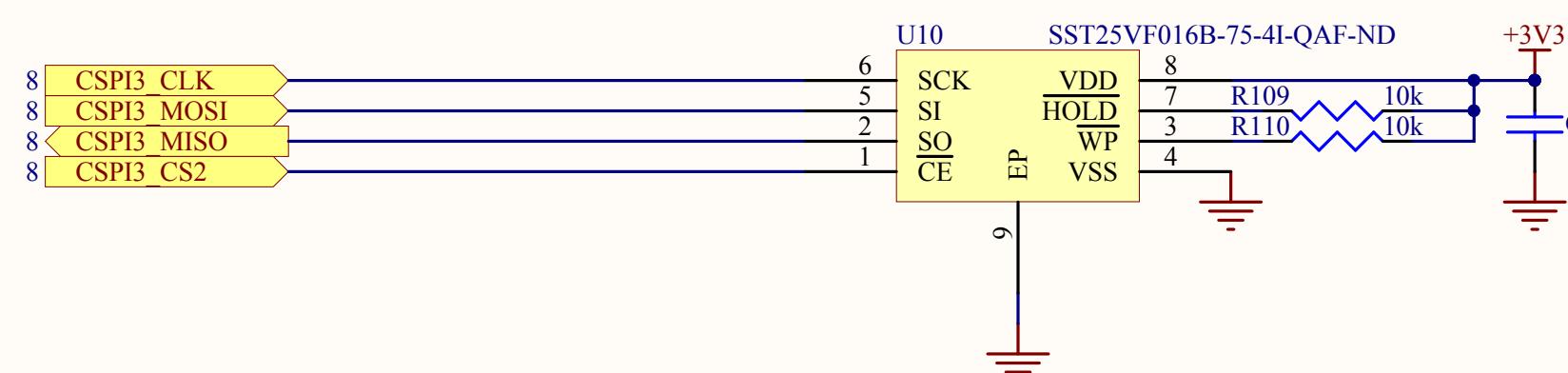
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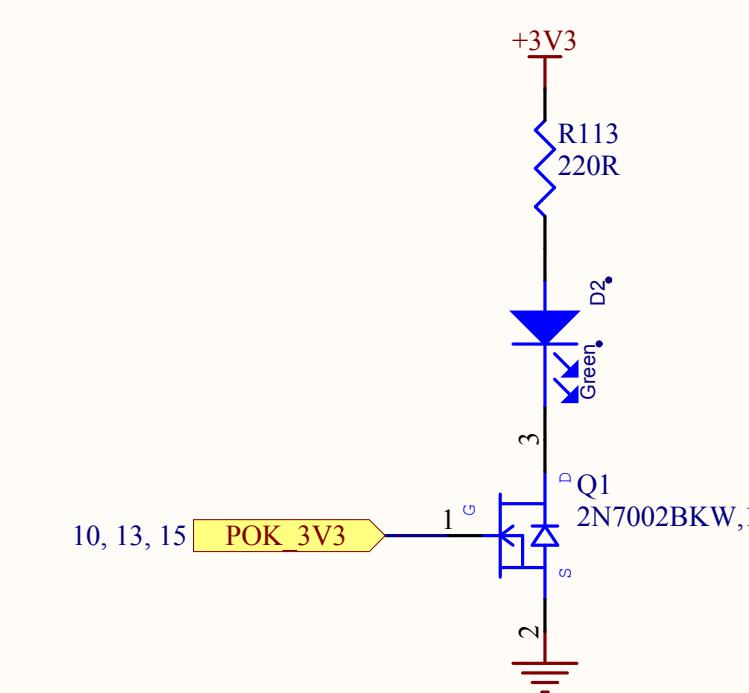
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# SPI FLASH, LED

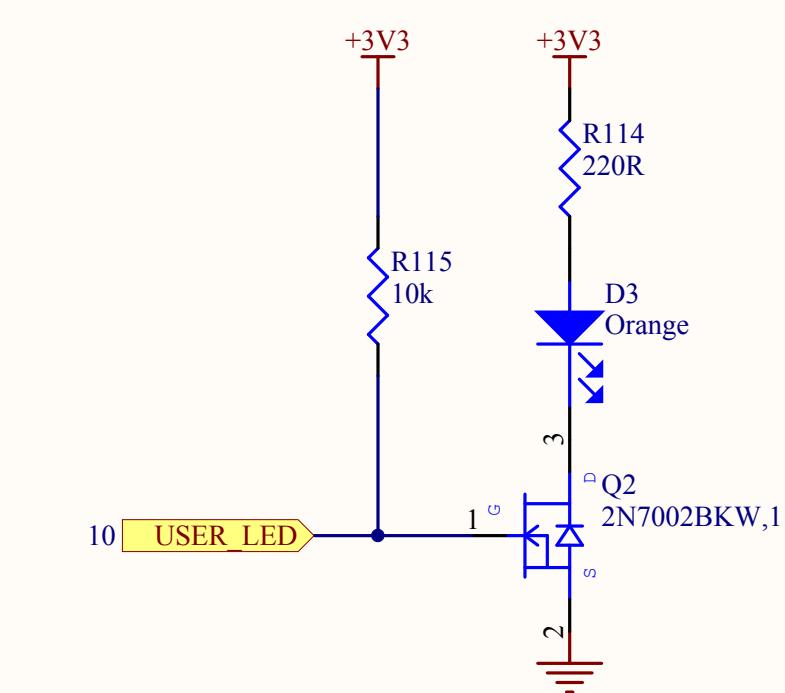
## SPI NOR FLASH



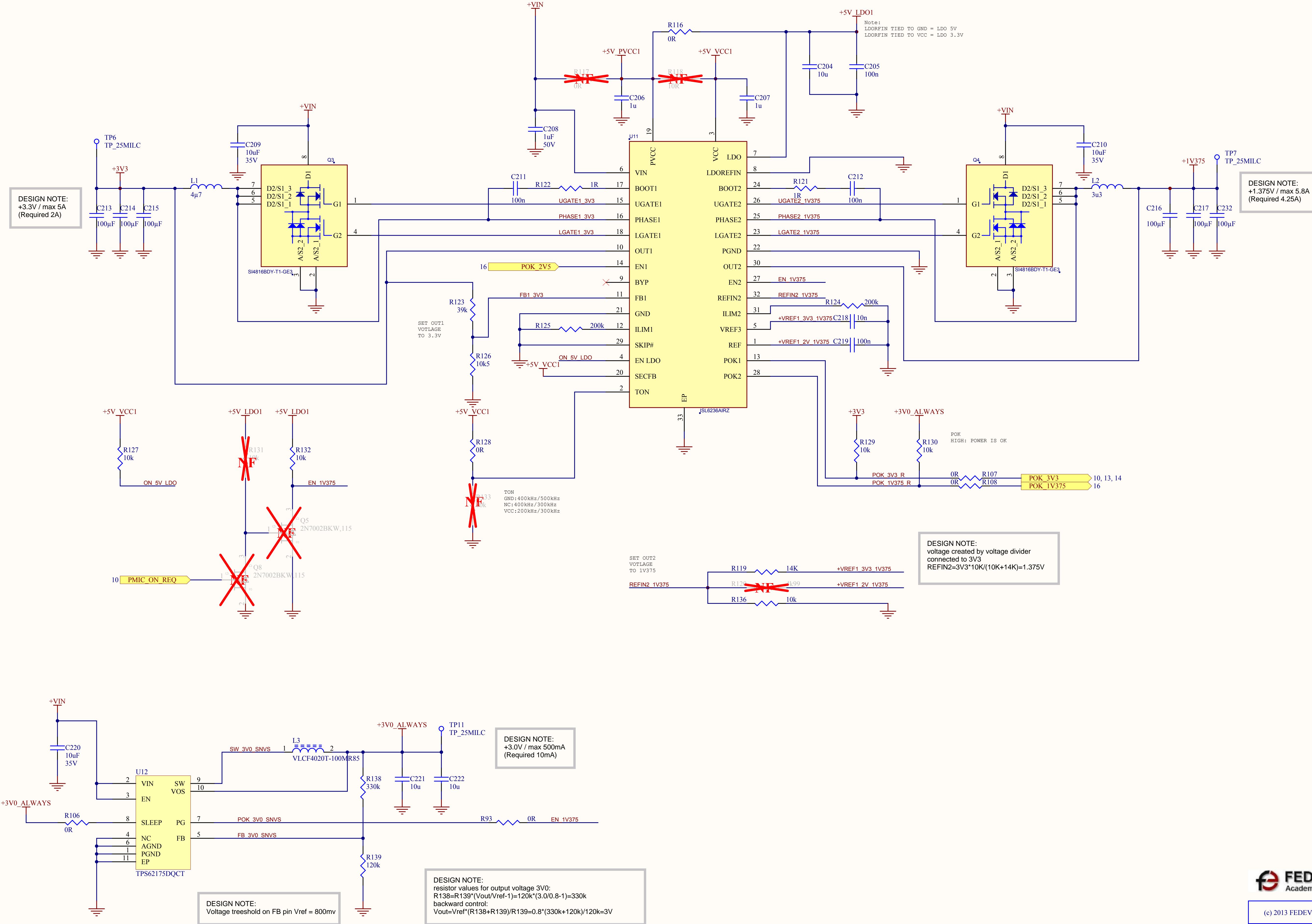
## POWER LED



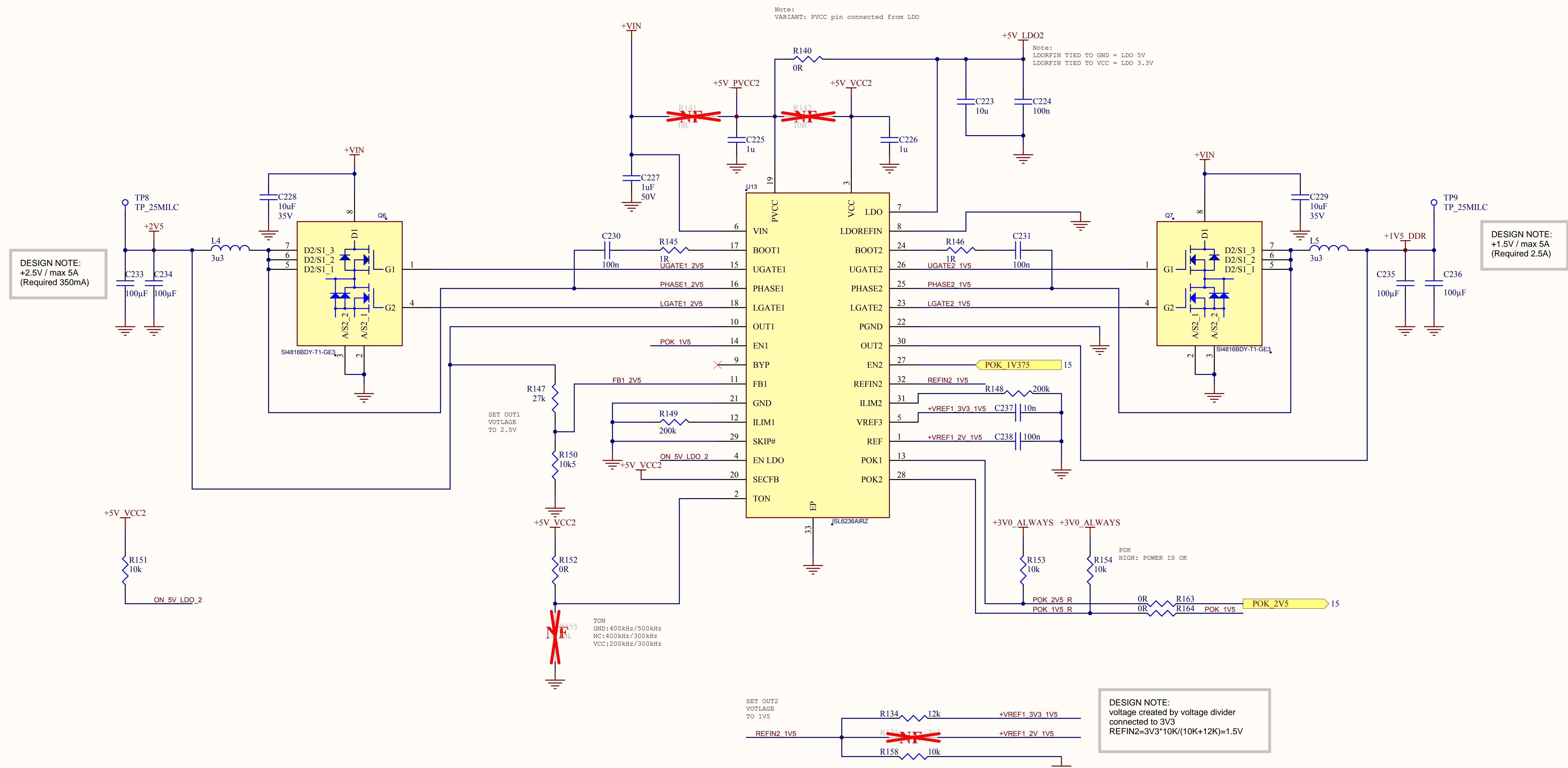
## USER DEFINED LED



# POWER +3.3V, +1.375V, +3.0\_ALWAYS CON

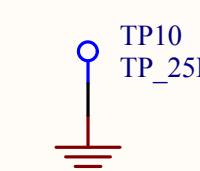


# POWER +2.5V, +1.5V CON

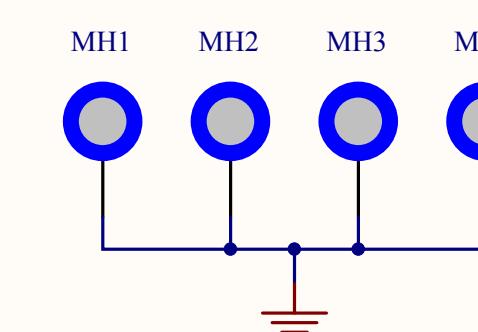


# MECHANICAL

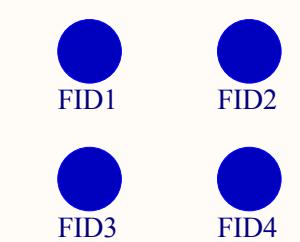
## TESTPOINT



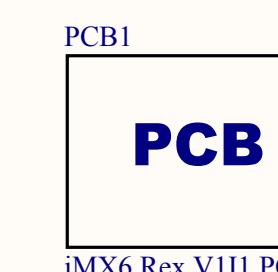
## MOUNTING HOLES



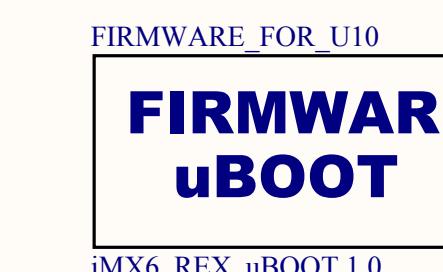
## FIDUCIALS



## PCB



## FIRMWARE



## LICENCE

ORIGINAL AUTHOR: FEDEVEL 2013  
WEBSITE: <http://www.iMX6Rex.com>

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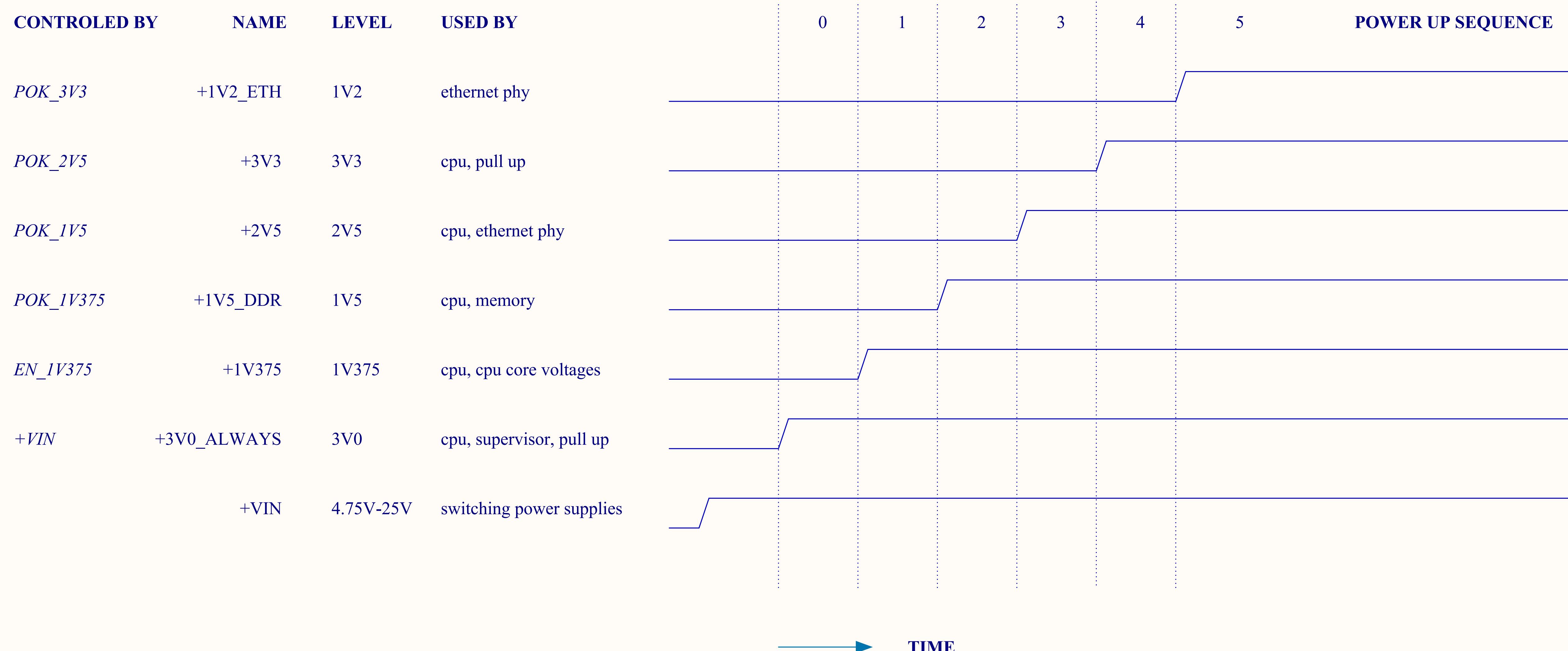


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# CPU - POWER SEQUENCING

OTHER POWERS	LEVEL	FROM	USED BY
+USB_VBUS	5V	connector	cpu
+DDR_VREF	0V75	+1V5_DDR	ref. for DDR memories, gen. with volt. divider
+1V2_VDD_ARM_CAP	1V2	iMX	cpu, core caps
+1V1_VDDSOC_CAP	1V1	iMX	core caps, cpu-sata, cpu-pcie, cpu-hdmi



# DOC: REVISION HISTORY

A 01-AUG-2013 Some HDMI and Ethernet signals swapped on J1

19-AUG-2013 Signals for SPI FLASH has been moved to CSPI3  
Added additional capacitors to +2V5 and +1V1\_VDDSOC\_CAP

21-AUG-2013 Added resistor from CPU\_XTALO to GND  
I2C3\_SDA and I2C3\_SCL has been moved to another CPU pins

22-AUG-2013 Always powered voltage change level to 3V0 - supply voltage +3V0\_ALWAYS  
Added bead to connect together +1V2\_ETH and +1V375 (Only for testing purpose).

23-AUG-2013 Added resistor to connect SLEEP pin of TPS62175DQCT to +3V0\_ALWAYS.

27-AUG-2013 On connector J1 added BOOT\_MODE signal to select boot source.



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D CLOCKS (CPU & PCI)

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[01] - COVER PAGE.SchDoc

[02] - BLOCK DIAGRAM.SchDoc  
[02] - BLOCK DIAGRAM.SchDoc

[03] - CONNECTORS.SchDoc  
[03] - CONNECTORS.SchDoc

[04] - CPU - DDR3, DDR3 MEM.SchDoc  
[04] - CPU - DDR3, DDR3 MEM.SchDoc

[05] - CPU - PCIE, SATA.SchDoc  
[05] - CPU - PCIE, SATA.SchDoc

[06] - CPU - HDMI, LVDS.SchDoc  
[06] - CPU - HDMI, LVDS.SchDoc

[07] - CPU - USB, ETHERNET.SchDoc  
[07] - CPU - USB, ETHERNET.SchDoc

[08] - CPU - SPI, I2C, SD, MMC.SchDoc  
[08] - CPU - SPI, I2C, SD, MMC.SchDoc

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## TEMPLATE NOTES

Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Company, Project and Version Revision

Mark Not Fitted Components as  
**NF**

Net Class Example



Differential signal example

TITLE Examples (You can change the color to reflect your company color)

# PAGE TITLE

*Peripheral / Group of component title*

*Smaller Title*

Schematic Status Explanation

**DRAFT** - Very early stage of schematic, ignore details.

**PRELIMINARY** - Close to final schematic.

**CHECKED** - There should not be any mistakes. Tell the engineer if you find one.

**RELEASED** - A board with this schematic has been sent to production.

[09] - CPU - UART, AUDIO.SchDoc  
[09] - CPU - UART, AUDIO.SchDoc

[10] - CPU - JTAG, CONTROL.SchDoc  
[10] - CPU - JTAG, CONTROL.SchDoc

[11] - CPU - POWER.SchDoc  
[11] - CPU - POWER.SchDoc

[12] - CPU - UNUSED.SchDoc  
[12] - CPU - UNUSED.SchDoc

[13] - ETHERNET PHY.SchDoc  
[13] - ETHERNET PHY.SchDoc

[14] - SPI FLASH, LEDS.SchDoc  
[14] - SPI FLASH, LEDS.SchDoc

[15] - PWR 3V3, 1V375.SchDoc  
[15] - PWR 3V3, 1V375.SchDoc

[16] - PWR 2V5, 1V5.SchDoc  
[16] - PWR 2V5, 1V5.SchDoc

[17] - MECH.SchDoc  
[17] - MECH.SchDoc

[18] - POWER SEQUENCING.SchDoc  
[18] - POWER SEQUENCING.SchDoc

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