YICHEN JIA

Architect Across HW/SW Boundaries

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EDUCATION

Ph.D. in Computer Science

Louisiana State University

Aug 2014 – May 2020

Dissertation: Understanding and Optimizing Flash-based Key-value Systems in Data Centers

B.S. in Computational Science

Jilin University

Aug 2009 – June 2013

Thesis: Seamless Instant Image Cloning Based on Derivative and Intensity Interpolation

SKILLS

Programming: C/C++ Python Shell Makefile x86/Arm Intrinsic/Assembly

Source Control: Git Gerrit OSS Licenses

Development Kits: SPDK PMDK

Debugging Tools: GDB KGDB JTAG

Perf Tools: Linux Perf Arm SPE

SELECTED PUBLICATIONS

ICDCS'20 Jia *et al. Kill Two Birds with One Stone: Auto-tuning RocksDB for High Bandwidth and Low Latency, 2020*

ISPASS'20 *Jia et al. From Flash to 3D XPoint: Performance Bottlenecks and Potentials in RocksDB with Storage Evolution, 2020*

MSST'19 *Jia et al. When NVMe over Fabrics Meets Arm: Performance and Implications, 2019*

MASCOTS'18 *Jia et al. SlimCache: Exploiting Data Compression Opportunities in Key-Value Caching Systems, 2018*

FAST'17 *Shen et al. DIDACache: A Deep Integration of Device and Application for Flash Based Key-Value Caching, 2017*

FEATURED DELIVERABLES

SPDK*: Optimizing write operations on Arm*
Snappy: *Workaround for memcpy for GCC10*
PMEM emulator: *Firmware emulator for PMEM*
IPI: *Measure and breakdown IPI latency in kernel*
Chiplet: *A concrete proposal for Arm Infra LoB*

INDUSTRIAL EXPERIENCE

Staff Performance Engineer

ARM, INC. | Oct 2022 – Present | Austin, TX

- Post-silicon bring-up and tuning (via control registers)
- Interrupt generation profiling and latency breakdown
- Workload reduction for simulation (EBM) and emulation (RTL/FGPA)
- Identifying bottlenecks by profiling micro-architecture units
- I/O intensive workloads characterization and improvement
- Exploring challenges and opportunities for Chiplet-based solutions
- Contributing to Future Arm Infra IP evolution (CPU, GIC, etc.)
- Resolving technical issues for customers (BRCM, WD, Micron, etc.)

Senior Performance Engineer

ARM, INC. | June 2020 – Sept 2022 | Austin, TX

- Investigating and optimizing NVMe over RoCEv2/TCP and SPDK
- Enabling and optimizing memory tiering patch for persistent memory
- Investigating the impact of SIMD/NEON optimizations for video codes
- Pre-silicon analysis for compression algorithms (ZSTD, etc.)
- Automating performance analysis process (Juju, Ansible)
- Comparing Arm and x86 CPUs for cloud applications
- Publishing technical blogs for video codecs, compression, NVMe-oF

Engineering Intern

ARM, INC. | May 2019 - Aug 2019 | May 2018 - Aug 2018 | Austin, TX

- Implementing an UEFI firmware driver to emulate PMEM on Arm-based servers, enabling DAX for EXT4 and benchmarking popular key-value stores (Redis, MongoDB, etc.) on the emulated PMEM
- Investigating NVMe and NVMe over RoCEv2 on ARM-based multi-core hardware, identifying bottlenecks, and proposing solutions

RESEARCH EXPERIENCE

Tuning and Optimizing Apps for Emerging Hardware

Louisiana State University | Sep 2017 – May 2020 | Baton Rouge, LA

- Performance benchmarking for Intel DC flash SSD and Optane SSD
- Understanding and optimizing RocksDB on 3D XPoint based SSD
- Auto-tuning RocksDB for high bandwidth and low latency
- Applying machine learning methods to improve system performance

Optimizing Key-value Caching System for Flash SSDs

Louisiana State University | Aug 2014 – May 2017 | Baton Rouge, LA

- Optimizing internal flash management inside flash SSDs
- Applying compression onto flash-based key-value caching system
- Customizing key-value caching system on open-channel SSDs
- Exploring the effect of deduplication on the flash caching system
- Studying reliability related issues of flash-based SSDs