# 74AHC138; 74AHCT138

3-to-8 line decoder/demultiplexer; inverting Rev. 03 — 28 November 2007

Product data sheet

#### **General description** 1.

The 74AHC138; 74AHCT138 are high-speed Si-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC138; 74AHCT138 is a 3-to-8 line decoder/demultiplexer. It accepts three binary weighted address inputs (A0, A1 and A2) and, when enabled, provides eight mutually exclusive outputs ( $\overline{Y}$ 0 to  $\overline{Y}$ 7) that are LOW when selected.

There are three enable inputs: two active LOW (\$\overline{E}\$1 and \$\overline{E}\$2) and one active HIGH (\$\overline{E}\$3). Every output will be HIGH unless E1 and E2 are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 74AHC138; 74AHCT138 devices and one inverter. The 74AHC138; 74AHCT138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

#### 2. **Features**

- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Inputs accepts voltages higher than V<sub>CC</sub>
- For 74AHC138 only: operates with CMOS input levels
- For 74AHCT138 only: operates with TTL input levels
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

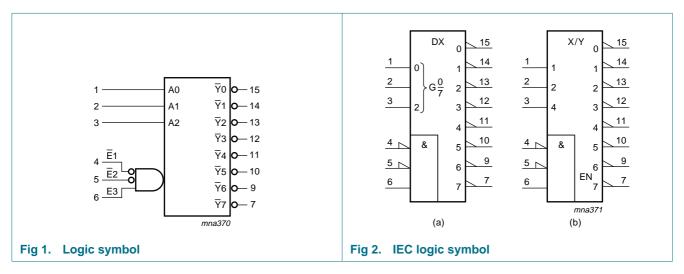


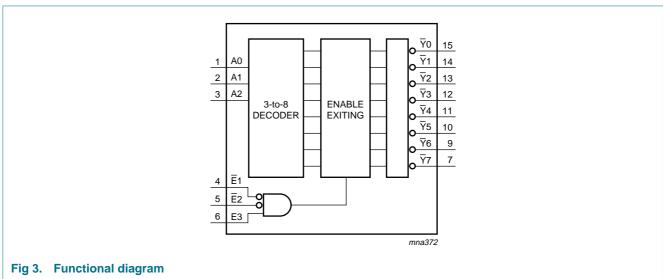
## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC138D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads;	SOT109-1
74AHCT138D			body width 3.9 mm	
74AHC138PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads;	SOT403-1
74AHCT138PW			body width 4.4 mm	
74AHC138BQ	–40 °C to +125 °C	DHVQFN16	1	SOT763-1
74AHCT138BQ			thin quad flat package; no leads; 16 terminals; body $2.5 \times 3.5 \times 0.85$ mm	

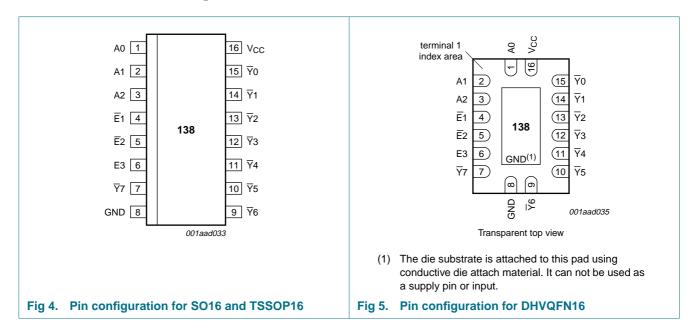
## 4. Functional diagram





## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	address input
A1	2	address input
A2	3	address input
E1	4	enable input (active LOW)
E2	5	enable input (active LOW)
E3	6	enable input (active HIGH)
GND	8	ground (0 V)
$\overline{Y}$ 0 to $\overline{Y}$ 7	15, 14, 13, 12, 11, 10, 9, 7	output
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table [1]

Input						Outp	ut						
E1	E2	E3	A0	A1	A2	₹0	<u>\</u>	<b>₹</b> 2	<b>∀</b> 3	<del>Y</del> 4	<b>₹</b> 5	<b>∀</b> 6	<b>Y</b> 7
Н	X	Χ	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н
Χ	Н	Χ	Χ	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н
Χ	Χ	L	Χ	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
L	L	Н	Н	L	L	Н	L	Н	Н	Н	Н	Н	Н
L	L	Н	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
L	L	Н	Н	Н	L	Н	Н	Н	L	Н	Н	Н	Н
L	L	Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	$V_1 < -0.5 \text{ V}$	[1] -20	-	mA
I <sub>OK</sub>	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	[1] _	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-	±25	mA
I <sub>CC</sub>	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$			
	SO16 package		[2] _	500	mW
	TSSOP16 package		[3]	500	mW
	DHVQFN16 package		<u>[4]</u> _	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>[2]</sup>  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

<sup>[3]</sup>  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

<sup>[4]</sup>  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC	138		74AHC	Г138		Unit
			Min	Тур	Max	Min	Тур	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	0	-	5.5	V
$V_{O}$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise	$V_{CC}$ = 3.3 V $\pm$ 0.3 V	-	-	100	-	-	-	ns/V
	and fall rate	$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	-	-	20	ns/V

### 9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	to +85 °C	-40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
For type	74AHC138									
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level	$V_{CC} = 2.0 \text{ V}$	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = -50 \mu\text{A};  V_{CC} = 2.0 \text{V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu\text{A};  V_{CC} = 3.0 \text{V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu A$ ; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -4.0 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.4	-	V
		$I_{O} = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.8	-	3.7	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
Iı	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V or 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF

**Table 6. Static characteristics** ...continued Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C	to +85 °C	-40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
For type	74AHCT138					'				
V <sub>IH</sub>	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	8.0	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_{O} = -50  \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_0 = -8.0 \text{ mA}$	3.94	-	-	3.8	-	3.7	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_{O} = 50 \mu A$	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
l <sub>l</sub>	input leakage current	$V_{I} = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V or } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
Δl <sub>CC</sub>	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other pins at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
Cı	input capacitance		-	3.0	10	-	10	-	10	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics** *GND = 0 V; For test circuit see Figure 8.* 

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C 1	to +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
For type	e 74AHC138										
t <sub>pd</sub>	propagation	An to $\overline{Y}$ n; see Figure 6	[2]								
	delay	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$									
		$C_L = 15 pF$		-	6.0	11.4	1.0	13.0	1.0	14.5	ns
		$C_L = 50 pF$		-	8.6	15.8	1.0	18.0	1.0	20.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		$C_L = 15 pF$		-	4.4	8.1	1.0	9.5	1.0	10.5	ns
		$C_L = 50 pF$		-	6.3	10.1	1.0	11.5	1.0	13.0	ns
		E3 to $\overline{Y}$ n; see Figure 6	[2]								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$									
		$C_L = 15 pF$		-	5.8	12.8	1.0	15.0	1.0	16.0	ns
		$C_L = 50 pF$		-	8.2	16.3	1.0	18.5	1.0	20.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C <sub>L</sub> = 15 pF		-	4.2	8.1	1.0	9.5	1.0	10.5	ns
		$C_L = 50 pF$		-	6.0	10.1	1.0	11.5	1.0	13.0	ns
		$\overline{E}$ 1, $\overline{E}$ 2 to $\overline{Y}$ n; see $\overline{F}$ igure $\overline{7}$	[2]								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$									
		C <sub>L</sub> = 15 pF		-	5.7	11.4	1.0	13.5	1.0	14.5	ns
		$C_L = 50 pF$		-	8.2	14.9	1.0	17.0	1.0	19.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C <sub>L</sub> = 15 pF		-	4.2	8.1	1.0	9.5	1.0	10.5	ns
		$C_L = 50 pF$		-	6.0	10.1	1.0	11.5	1.0	13.0	ns
$C_{PD}$	power dissipation capacitance	$C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$	[4]	-	18.0	-	-	-	-	-	pF

Table 7. Dynamic characteristics ...continued

GND = 0 V; For test circuit see Figure 8.

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
For type	74AHCT138								ı		
t <sub>pd</sub>	propagation	An to $\overline{Y}$ n; see Figure 6	[2]								
	delay	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C <sub>L</sub> = 15 pF		-	4.4	10.4	1.0	12.0	1.0	13.0	ns
		$C_L = 50 pF$		-	6.2	11.4	1.0	13.0	1.0	14.5	ns
		E3 to $\overline{Y}$ n; see Figure 6	[2]								
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C <sub>L</sub> = 15 pF		-	4.3	9.1	1.0	10.5	1.0	11.5	ns
		$C_L = 50 pF$		-	6.2	10.1	1.0	11.5	1.0	13.0	ns
		E3 to $\overline{Y}$ n; see Figure 7	[2]								
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C <sub>L</sub> = 15 pF		-	4.3	9.6	1.0	11.0	1.0	12.0	ns
		$C_L = 50 pF$		-	6.2	10.6	1.0	12.0	1.0	13.5	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50 \text{ pF}; f_i = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	<u>[4]</u>	-	23.0	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3 \text{ V}$  and  $V_{CC} = 5.0 \text{ V}$ ).
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$ 

 $f_i$  = input frequency in MHz,  $f_o$  = output frequency in MHz

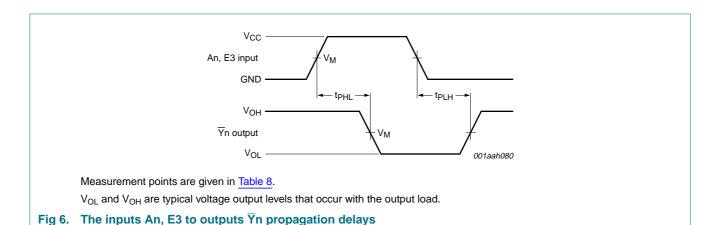
C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

### 11. Waveforms



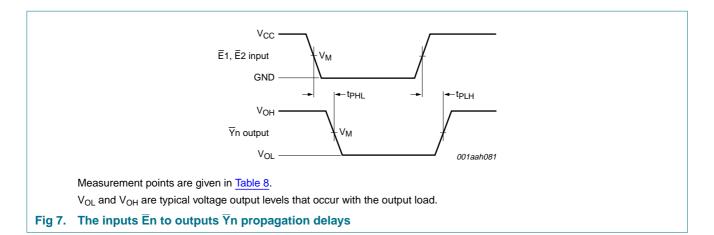
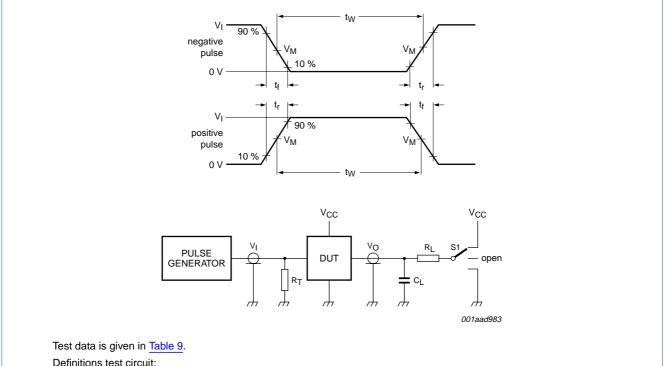


Table 8. Measurement points

Туре	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
74AHC138	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
74AHCT138	1.5 V	0.5V <sub>CC</sub>



Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>L</sub> = Load resistance.

S1 = Test selection switch.

Fig 8. Load circuit for switching times

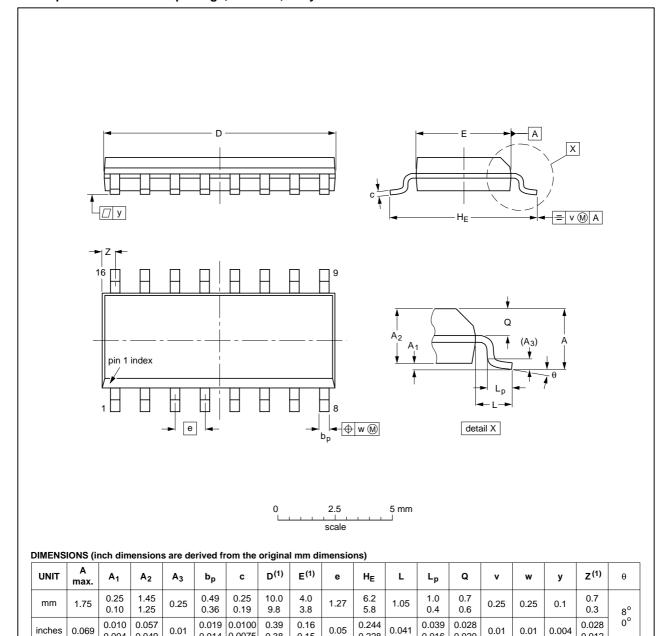
Table 9. **Test data** 

Туре	Input		Load		S1 position		
	VI	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
74AHC138	$V_{CC}$	≤ 3.0 ns	15 pF, 50 pF	1 k $\Omega$	open	GND	V <sub>CC</sub>
74AHCT138	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	$V_{CC}$

## 12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.014 0.0075

0.38

0.15

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012			<del>99-12-27</del> 03-02-19

0.228

0.016

0.020

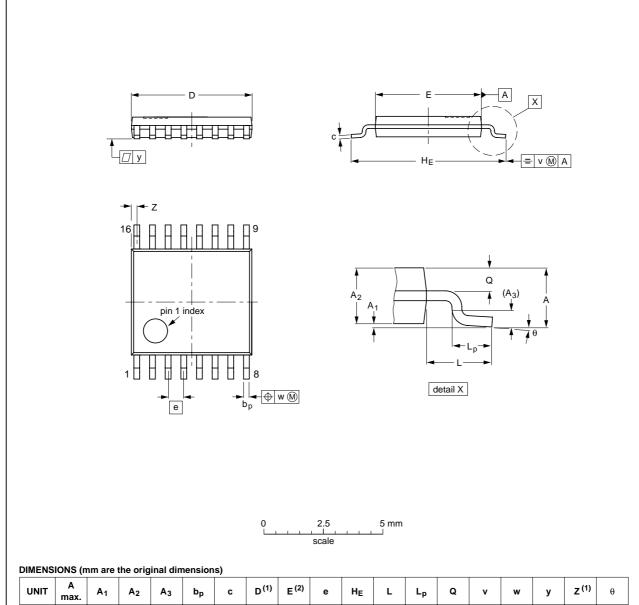
Fig 9. Package outline SOT109-1 (SO16)

0.004

0.049

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



 						-,												
UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(2)</sup>	е	HE	L	Lp	Q	v	w	у	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT403-1		MO-153				<del>99-12-27</del> 03-02-18	

Fig 10. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

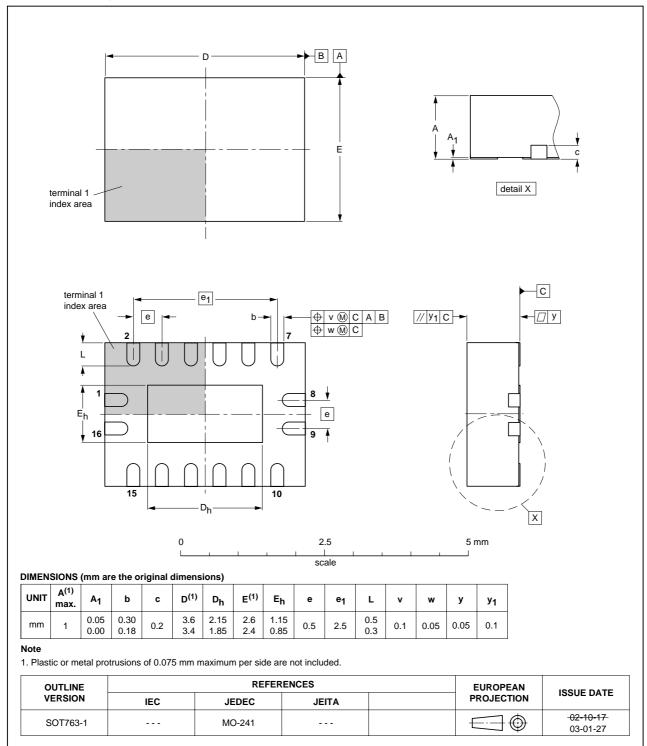


Fig 11. Package outline SOT763-1 (DHVQFN16)

## 13. Abbreviations

### Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
CDM	Charged-Device Model
TTL	Transistor-Transistor Logic

## 14. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74AHC_AHCT138_3	20071128	Product data sheet	-	74AHC_AHCT138_2				
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>							
	<ul> <li>Legal texts have l</li> </ul>	been adapted to the new	company name where a	ppropriate.				
	<ul> <li>Section 3: DHVQ</li> </ul>	FN16 package added.						
	<ul> <li>Section 8: derating</li> </ul>	ng values added for DHVC	QFN16 package.					
	<ul> <li>Section 12: outlin</li> </ul>	e drawing added for DHV	QFN16 package.					
74AHC_AHCT138_2	19990927	Product specification	-	74AHC_AHCT138_1				
74AHC_AHCT138_1	19900331	Product specification	-	-				

## 15. Legal information

### 15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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