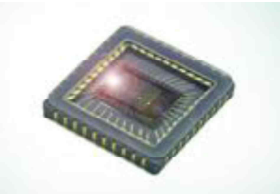
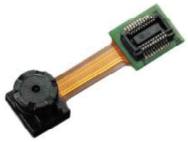
Image Sensor & Vision Technology

Pixelplus Co.,Ltd

PO1030 Data sheet





PO1030x-MSxx

PO1030xB
1/4.5 Inch VGA Mono Single Chip CMOS IMAGE SENSOR

PO1030xC
1/4.5 Inch VGA Color Single Chip CMOS IMAGE SENSOR

[Preliminary]

Rev 3.8

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CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

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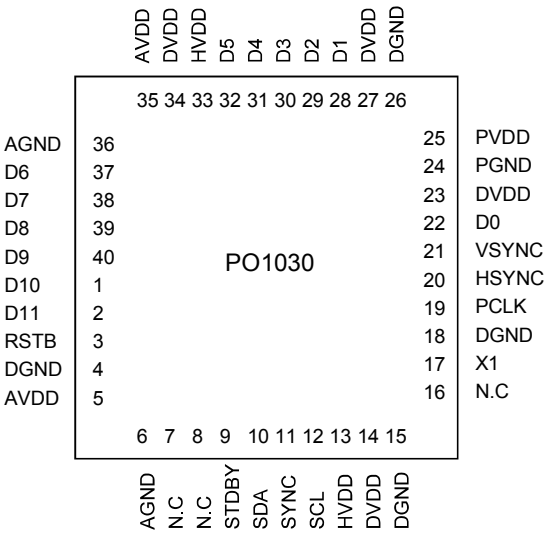
CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

§ This document is an initial draft. It will be revised on without prior notice.
Contact Pixelplus for up-to-date information.

Features

- 1/4.5 inch 640 X 480 active pixel array with color filters and micro-lens.
- Power supply 2.5V for core and 2.5 ~ 3.3V for I/O.
- Output formats : 8bit YCbCr / YUV / 9Bit Bayer data / 5:6:5 RGB, 12bit 8:8:8 RGB
- 30 frames/sec progressive scan.
- Image processing on chip : defect correction, color interpolation, color correction, edge enhancement, contrast stretch, white balance, exposure control, color saturation, gamma correction.
- Still image capture with electrical or mechanical shutter.
- Frame size, window size and position controllable through a serial interface bus.
- VGA/QVGA sub-sampling.
- Horizontal / Vertical mirroring.
- 50Hz, 60Hz flicker cancellation.
- Package : 40 pin CLCC, 32 pin CSP



< Figure. 1> Pin Diagram

Table 1. Typical Parameters

Pixel Array	640 X 480
Pixel Size	5.2um X 5.2um
Image Area	3.43mm X 2.6mm
Clock Rate	27MHz (Max.)
Frame rate	Variable up to 30fps
Dark Current	0.3nA/㎠
Sensitivity	3.1V/Lux.sec @15fps,IR cut filter
Saturation Level	770mV
Conversion Gain	15~50㎶/electrons
Fill Factor	40%
Supply voltage	2.5~3.3V I/O,2.5V Core
Power consumption	75mW @30fps, active
	60mW @15fps, active
	200uW @standby
Operation Temp.	-30 ~ 40℃
Dynamic Range	50dB
Package	40 pin CLCC, 32 pin CSP

PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
1	D10	O	Bit 10 of data output. Luminance data Y<7:0> are mapped to output pins D<11:4>. Chrominance data UV<7:0> and Bayer RGB data are also mapped to output pins D<11:4>. 5:6:5 RGB data are mapped to D<11:4> such that (R<4:0>, G<5:3>) or (G<2:0>, B<4:0>) correspond to D<11:4>. 8:8:8 RGB data are mapped to D<11:0> such that (R<7:0>, G<7:4>) or (G<3:0>, B<7:0>) correspond to D<11:0>.
2	D11	O	Bit 11 of data output.
3	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
4	DGND	P	Digital ground. Core and I/O circuits share the ground pads.
5	AVDD	P	Analog vdd : 2.5V DC. 100nF capacitor to AGND.
6	AGND	P	Analog ground.
7	N.C	-	No Connection
8	N.C	-	No Connection
9	STDBY	I	Power standby mode. When STDBY='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<11:0> and PCLK, HSYNC, VSYNC pins are tri-stated.
10	SDA	I/O	I2C serial data bus.
11	SYNC	I	Still image capture mode. When there's a SYNC pulse, the sensor assumes the operation of a mechanical shutter or the sensor utilizes its built-in electrical shutter to grab a still image.
12	SCL	I	I2C serial clock input.
13	HVDD	P	Digital vdd for I/O : DC 2.5~3.3V. Sensor can be interfaced directly to 3.3V devices if HVDD power is set to 3.3V. Core vdd must remain 2.5V always.
14	DVDD	P	Digital vdd for core logic : 2.5V DC. 100nF capacitor to DGND.
15	DGND	P	Digital ground for core and I/O circuits.
16	N.C	-	No Connection
17	X1	I	Master clock : Crystal input pad.
18	DGND	P	Digital ground.

Table 2-1. PIN Descriptions

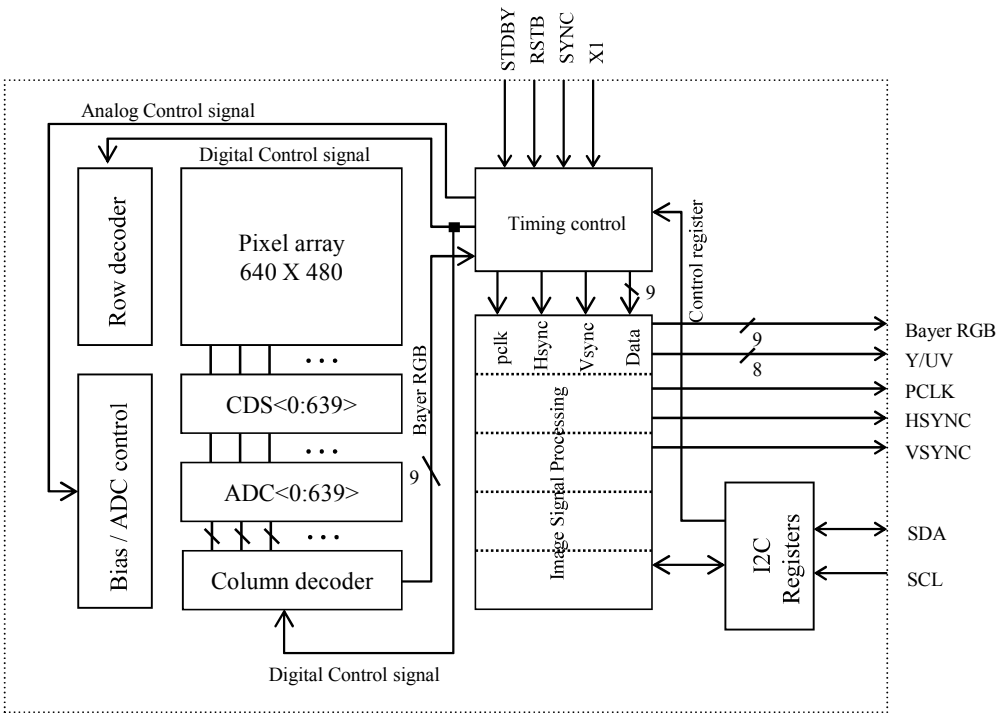
Pin No.	Name	I/O Type	Functions / Descriptions
19	PCLK	O	Pixel clock. Each data are latched by external devices at the rising or falling edge of PCLK. The polarity can be controlled anyway.
20	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not appear outside the vertical window of interest.
21	VSYNC	O	Vertical sync : Indicates the start of a new frame.
22	D0	O	Bit 0 of data output.
23	DVDD	P	Digital vdd : 2.5V DC. 100nF to DGND
24	PGND	P	Ground for pixel array.
25	PVDD	P	Pixel array current is supplied from PVDD : 2.5V DC. 100nF to AGND
26	DGND	P	Digital ground.
27	DVDD	P	Digital vdd : 2.5V DC. 100nF to DGND
28	D1	O	Bit 1 of data output.
29	D2	O	Bit 2 of data output.
30	D3	O	Bit 3 of data output.
31	D4	O	Bit 4 of data output.
32	D5	O	Bit 5 of data output.
33	HVDD	P	Vdd for I/O : 2.5~3.3V
34	DVDD	P	Digital vdd : 2.5V DC. 100nF to DGND
35	AVDD	P	Analog vdd : 2.5V DC, 100nF to AGND
36	AGND	P	Analog ground.
37	D6	O	Bit 6 of data output.
38	D7	O	Bit 7 of data output.
39	D8	O	Bit 8 of data output.
40	D9	O	Bit 9 of data output.

Table 2-2. PIN Description

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Chip Architecture

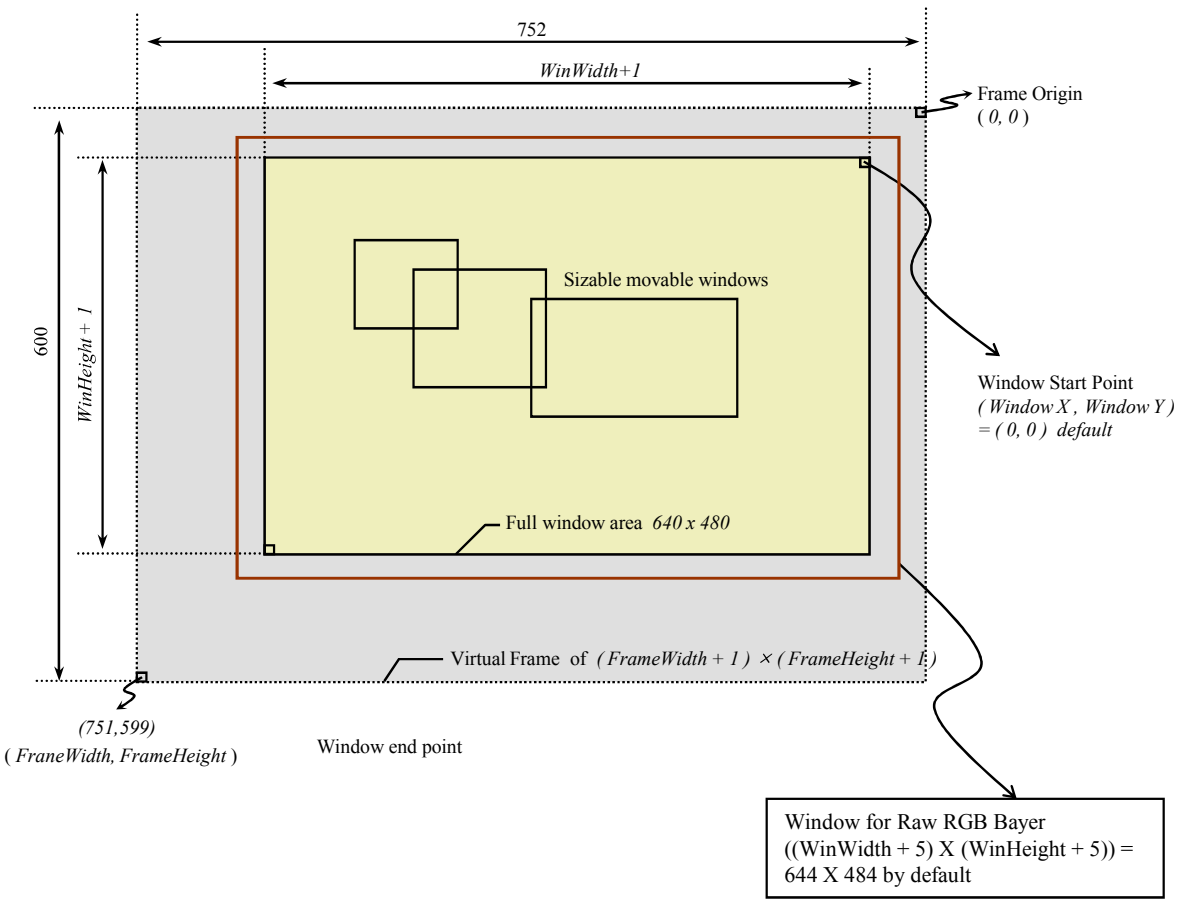
PO1030 has 640 x 480 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as defect pixel correction, color interpolation, color correction, gamma correction, contrast enhancement, edge enhancement, color saturation enhancement, white balance and exposure control. Internal functions and output signal timing can be programmed simply by modifying the register files through I^2C serial interface.



<Figure. 2> Block Diagram

Frame Structure and Windowing

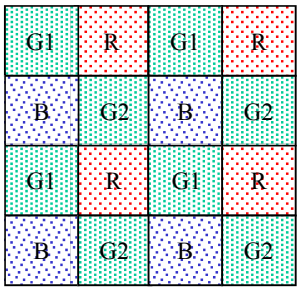
Origin *(0, 0)* of the frame is at the upper right corner. Size of the frame is determined by two registers : *FrameWidth* and *FrameHeight.* One frame consists of *FrameWidth + 1* columns and *FrameHeight + 1* rows. *FrameWidth* and *FrameHeight* can be programmed to be larger than physical array size. Physical array of 640 × 480 pixels is positioned at *(14, 6)*. It is possible to define a specific region of the frame as a window. Pixel scanning begins from *(0, 0)* and proceeds row by row downward, and for each line scan direction is from right to the left. HSYNC signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *FrameHeight* , and 0 to *FrameWidth* respectively. The counter values increase at the pace of pixel clock (PCLK) or half the PCLK, which does not change as the frame size is altered : The pixel data rate is fixed and is independent of frame size (frame rate.)



< Fig. 3 > Default structure of frame and window. (Top view)

Data Formats

Pixel array is covered by Bayer color filters as can be seen in the figure below. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PO1030 provides this Bayer pattern RGB data through an 9bit channel. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PO1030 adopts a low pass filter to prevent the interference patterns(called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. These three color components R, G, B can be routed to 12 bit output pins in such a way that 8bit R data and upper 4bits of G data are passed first and then, lower 4 bits of G data and 8bit B data are passed to output pins. It takes two PCLK's to pass one pixel RGB data to output bus.



< Fig. 4> Bayer filter pattern

For low grade display devices, it is not necessary to have 3 RGB data of all 8bit precision. PO1030 provides lower precision RGB data such that, 5bit R data and upper 3 bits of 6bit precision G data are passed first to output pins, and then the remaining 3 bits of G and 5 bit B data are routed outward. It takes two PCLK's to get 5:6:5 RGB data for each pixel.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$U = 0.492 (B - Y)$$

$$V = 0.877 (R - Y)$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

U1	Y1	V1	Y2	U3	Y3	V3	Y4	…

< Fig. 5> 4:2:2 YUV data sequence.

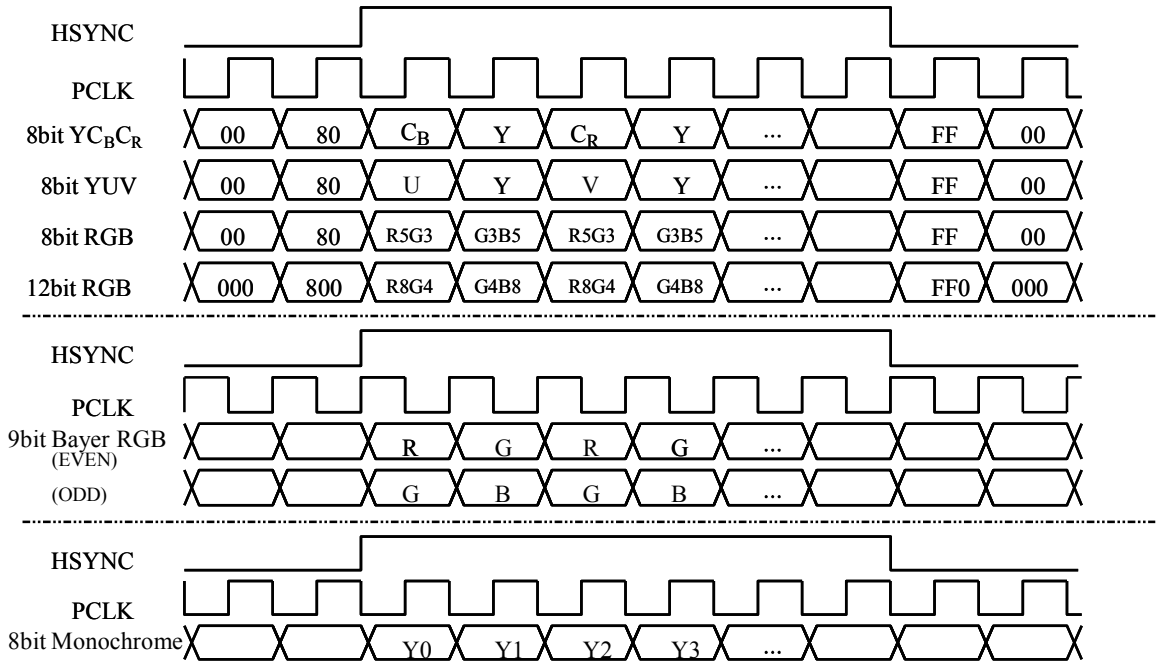
PO1030 supports 4:2:2 YUV data format where U and V components are horizontally sub-sampled such that U and V for every other pixel are omitted. PO1030 also supports ITU-R BT.601 YC_BC_R format which is a scaled, offset version of YUV. Y is the same in both formats but the C_BC_R is formed as follows.

$$C_B = 0.564 (B - Y) + 128$$

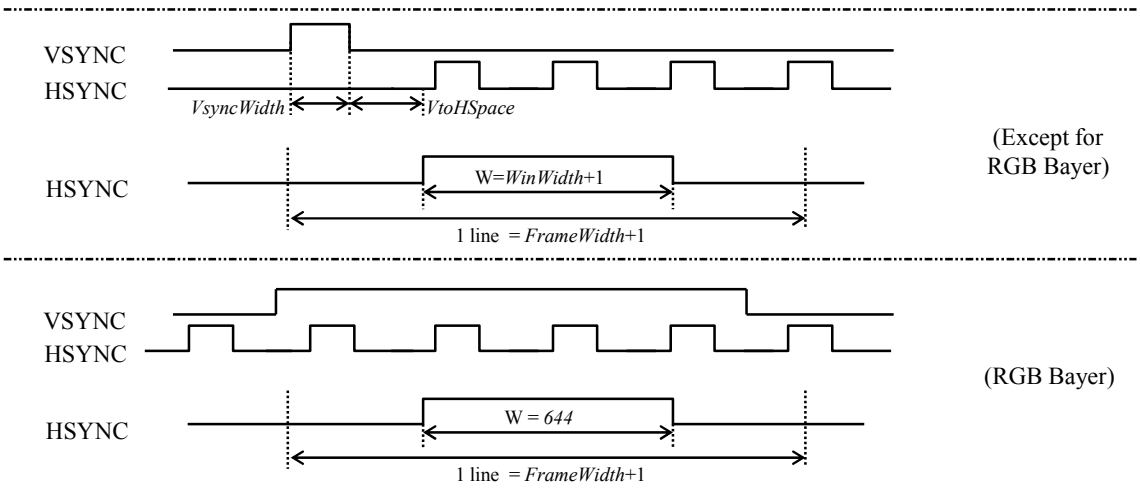
$$C_R = 0.713 (R - Y) + 128$$

Data and Synchronization Timing

In <Fig.6>, HSYNC / VSYNC / PCLK polarity can have any combinations possible (Except for RGB Bayer). Data can be latched at the rising or falling edge of PCLK. HSYNC and VSYNC can be set to be active high or active low. Every type of data (RGB or YUV) comes out at the fixed rate of PCLK, which can have the same or ½ ~ 1/128 the frequency of MCLK. The sequence RGB Raw Bayer data for even rows is RGRGRG… and for odd rows is GBGBGB….



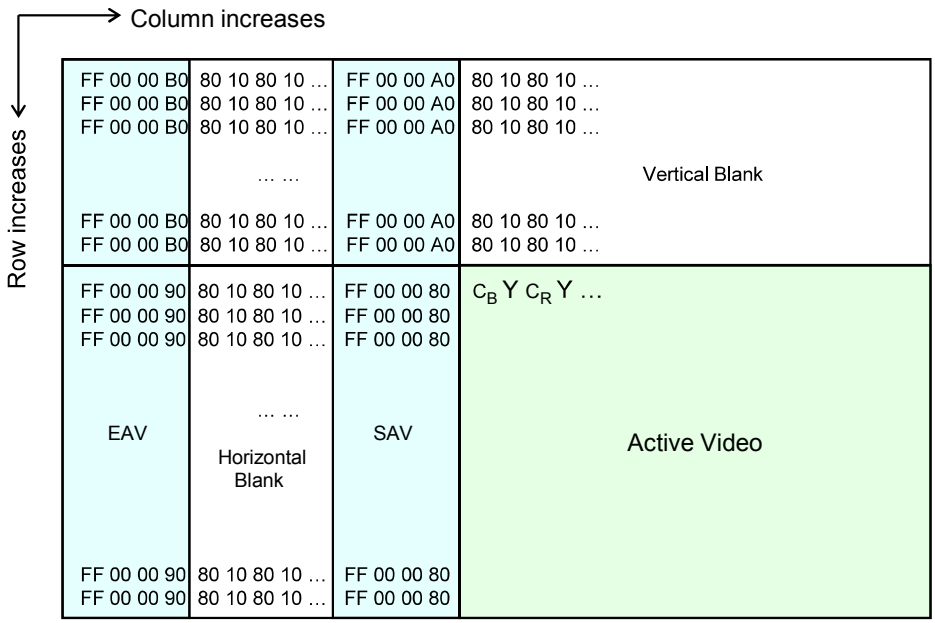
< Figure. 6 > Timing diagram for HSYNC, PCLK and data



< Figure. 7> Timing diagram for VSYNC and HSYNC

In <Fig.7>, VSYNC is set high(or low) a few lines before the start of a new frame. The width of VSYNC pulse is controlled by *VsyncWidth* register : VSYNC width = (*VsyncWidth+1*) × (1 line time). VSYNC space to HSYNC is controlled by *VtoHSpace* register : Space = (*VtoHSpace*+1) × (1 line time). HSYNC is set high while the frame column counter value lies within the window of interest : *Window X* to *(WindowX + WinWidth)*.

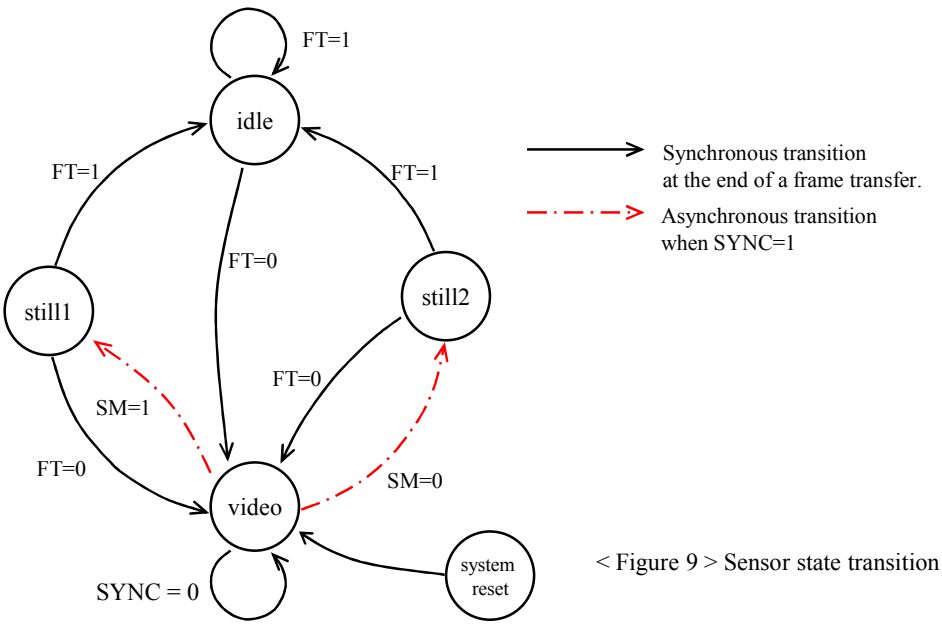
In <Fig. 8>, EAV(End of Active Video) and SAV(Start of Active Video) signals are inserted for synchronization purposes. EAV is a 4 byte sequence of “FF 00 00 90” for active lines, and “FF 00 00 B0” for blank lines. SAV is a 4 byte sequence of “FF 00 00 80” for active lines, and “FF 00 00 A0” for vertical blank lines. HSYNC signal is asserted right after the SAV sequence and de-asserted right before the EAV sequence. Horizontal and vertical blank area is repeatedly filled with “80 10”.



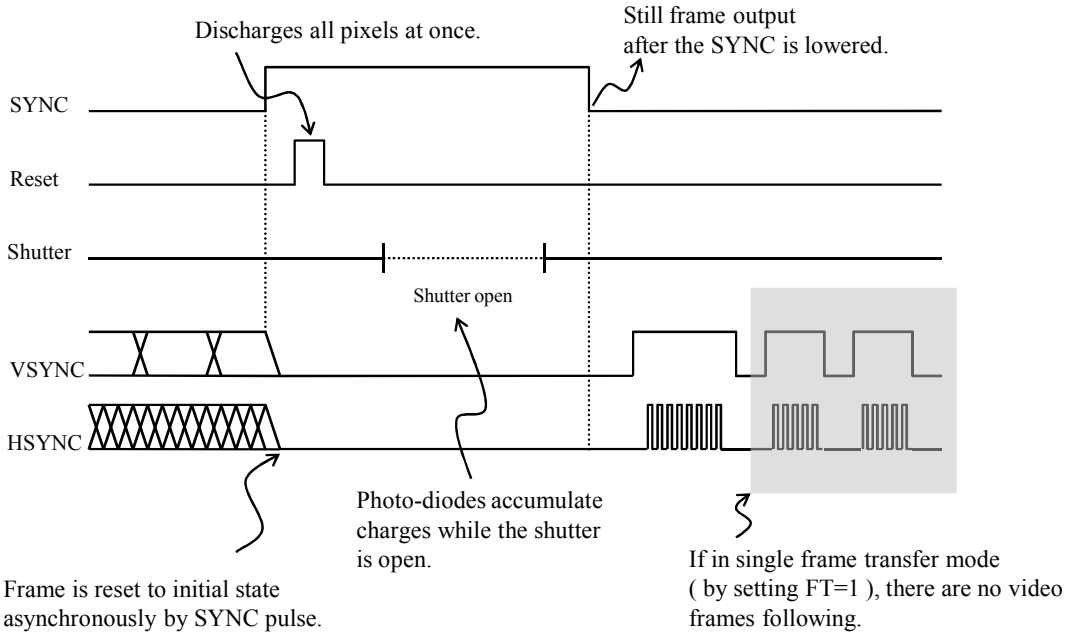
< Figure 8 > Frame data sequence including EAV and SAV.

Video Mode(Preview Mode) and Still Image Capture Mode

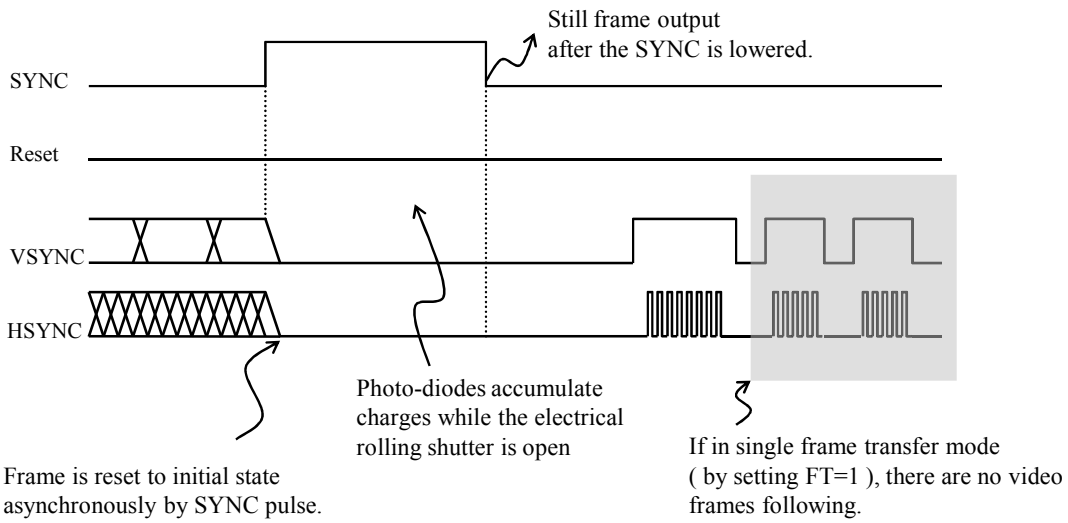
PO1030 normally operates in video mode. There are two kinds of still image capture mode. The first one is for a system that utilizes mechanical shutter (still1 mode). If there is a pulse on SYNC input (or bit 4 of register 63 (RS bit)), each and every pixel of the array is reset to dark state where there are no photo-charges accumulated, and row/column counters are reset to initial states. While the SYNC is high, shutter is open and sensor is exposed to light. After the SYNC input goes low, there comes out the still image data. The other one (still2 mode) utilizes integrated electrical rolling shutter. After a still image capture mode, video mode may follow immediately, or the sensor may be in idle state until an appropriate bit(FT) is reset in the I^2C register file. While the sensor is in idle state, there's no HSYNC or VSYNC pulse. Image resolution switch between video and still mode (for example, video in QVGA resolution and still image in VGA resolution) can be done manually or automatically. Frame rate for the two modes can be adjusted manually or it can be automatically kept same by slowing down the clock while capturing lower resolution images. Exposure time can also be matched manually or automatically between the two modes of operation.



< Figure 9 > Sensor state transition diagram



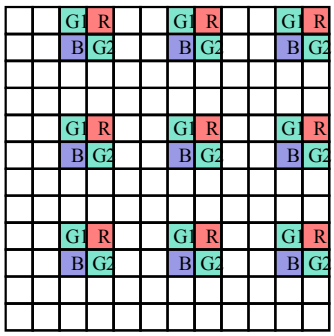
<Figure 10> Still image capture with mechanical shutter



<Figure 11> Still image capture with electrical shutter

Sub-sampling

PO1030 supports one modes of sub-sampling : ¼ sub-sampling . Figure 12 shows the way PO1030 selects sub-sample data from whole picture array. Since unselected rows and columns are omitted from counting, it takes only ¼ pixel clocks compared to the full-sampling case so that the frame rate is incremented by 4 times given the clock rate is identical for all modes. There are some combinations of operations that can be applied to keep the frame rate equal between sampling mode switches. The clock rate can be reduced by a factor of 4 leaving frame size identical. *FrameWidth* is incremented by 4 times and the clock rate remains the same. *FrameHeight* is incremented by a factor of 2 and the clock frequency is decremented to half it used to be. PO1030 supports automatic frame rate equalizations between full and sub-sampling mode by dividing master clocks, while leaving frame size untouched. Window position and size are all with respect to the full-sampling mode. It's not necessary to adjust these data in considerations of reduction in number of samples.



< Figure 12 > 1/4 sub-sampling

Exposure Time Control

IntLines<19:0> register controls the exposure time. *IntLines*<19:6> is the number of lines for which electrical shutter will be open to collect photons. *IntLines*<5:0> is the number of partial line times to be added to integer line numbers, which means the exposure time can be controlled by 1/64 line time. To guarantee same amount of exposure time between two different sampling modes, it is necessary to adjust some parameters. The parameters are : *IntLines*, *FrameWidth*, clock frequency, number of sampled data. For two different sampling modes A and B, the exposure time has a relation like

$$\text{exposure time(A)} = \frac{(\#\text{ of data(A)}) \times IntLines(A) \times FrameWidth(A) \times \text{clkfreq(B)}}{(\#\text{ of data(B)}) \times IntLines(B) \times FrameWidth(B) \times \text{clkfreq(A)}} \text{ exposure time(B)}$$

Suppose A is ¼ sampling mode and B is full sampling mode. The ratio of sample numbers is ¼ and lets assume the *IntLines* and *FrameWidth* register values are kept identical in both modes. If clock frequency is also fixed before and after the mode switch, the exposure time in mode A is ¼ that of mode B. To adjust the exposure level to be equal, mode A clock frequency can be slowed down by a factor of 1/4. Or the *IntLines* register value can be incremented four times while leaving other parameters same as mode B. Or the *FrameWidth* can be doubled while clock frequency is halved. PO1030 supports auto-mode in which the exposure time is maintained across sub-sampling modes by adjusting clock frequency.

I2C Description

The registers of PO1030 are written and read through the I²C interface. The PO1030 has I²C slave. The PO1030 is controlled by the I²C clock (SCL), which is driven by the I²C master. Data is transferred into and out of the PO1030 through the I²C data (SDA) line. The SCL and SDA lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The I²C protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of an I²C device consists of 7 bits of address and 1 bit of direction. A 0 in the LSB of the address indicates write mode, and a 1 indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The I²C clock pulse is provided by the master. The data must be stable during the HIGH period of the I²C clock : it can only change when the I²C clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

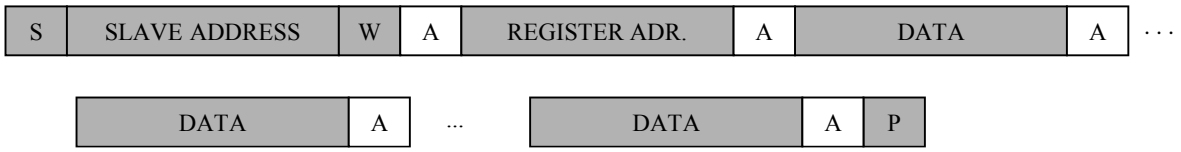
If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PO1030 uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

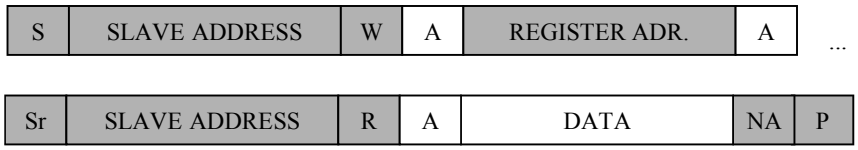
I²C Functional Description

Single Write Mode operation

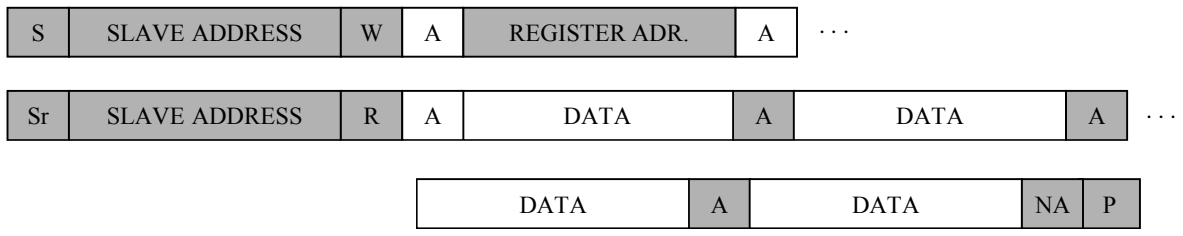
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



S: Start condition. Sr : Repeated Start (Start without preceding stop.)
SLAVE ADDRESS: write address = DCh = 11011100b
read address = DDh = 11011101b
R/W: Read/Write selection. High = read / LOW = write.
A: Acknowledge bit. NA : No Acknowledge.
DATA: 8-bit data
P: Stop condition

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Register Table

Table 3. Register Table

Addr.	Default	Name	Description	R/W
00h	10h	*DeviceID(H)*	Device ID (0x1030)	R
01h	30h	*DeviceID(L)*		
04h	02h	*FrmWidth(H)*	Frame Width (default : 751 d = 0x2EF , Max. : 0x3FFF)	R/W
05h	EFh	*FrmWidth(L)*	1 line time = frame width x 1 pixel time $\text{frame rate} = \frac{\text{freq(PCLK)}}{(FrmHeight+1)\times(FrmWidth+1)}$	
06h	02h	*FrmHeight(H)*	Frame Height (default : 599 d = 0x257, Max. : 0x3FFF)	R/W
07h	57h	*FrmHeight(L)*	1 frame time = frame height x frame width x 1 pixel time ref. <Fig.3>	
08h	X0h	*WindowX(H)*	WindowX (Max. : 0x7FF)	R/W
09h	00h	*WindowX(L)*	X coordinate of Window start point ref. <Fig.3>	
0Ah	X0h	*WindowY(H)*	WindowY (Max. : 0x7FF)	R/W
0Bh	00h	*WindowY(L)*	Y coordinate of Window start point ref. <Fig.3>	
0Ch	X2h	*WinWidth(H)*	Window Width (default : 639 d = 0x27F, Max. : 0x7FF) ref. <Fig.3>	R/W
0Dh	7Fh	*WinWidth(L)*		
0Eh	X1h	*WinHeight(H)*	Window Height (default : 479 d = 0x1DF, Max. : 0x7FF) ref. <Fig.3>	R/W
0Fh	DFh	*WinHeight(L)*		
12h	X3h	*GlobalIbais*	Global Current bias. Analog OP-Amp biased by current mirror. The current is determined by *GlobalIbias* x 1uA	R/W
13h	X2h	*PixelIBias*	Pixel Current Bias. Ipixel = *PixelIBias* x 1uA	R/W
15h	03h	*GlobalGain*	Global Gain (Max. : 0x4F). 0x03 => 1x, 0x10 => 2x, 0x20 : 4x, 0x30 => 8x, 0x40 => 16x, 0x4F => 32x	R/W
16h	85h	*Rgain*	R Gain. 0x40 => 1x, 0x80 => 2x, 0xC0 => 3x, 0xFF => 4x	R/W
17h	40h	*G1Gain*	G1 Gain	R/W
18h	4Ah	*Bgain*	B Gain	R/W
19h	40h	*G2Gain*	G2 Gain	R/W
1Ah	00h	*IntLines(H)*	Integration Lines (Max. : Frame height)	R/W
1Bh	80h	*IntLines(M)*	Read Only when AE is On. (refer to Reg. 3Eh)	
1Ch	00h	*IntLines(L)*	Integration Columns (MSB 6bit, 000000xx), Read Only when AE is On.	R/W
1Dh	18h	*Control1*	Control 1 ref. <Fig.9> and <Table 4>	R/W

X	SM	FT	AS	FE	CLK2	CLK1	CLK0
X	Shutter Mode	Frame Transfer	Auto Subsampling	Frame Equalization	Master clk Division		

1Eh	00h	*Control2*	Control 2	R/W

HM	VM	reserved					
H Mirror (0: Disable 1: Enble)	V Mirror (0: Disable 1: Enable)	0	0	0	0	0	0

1Fh	00h	*Control3*	Control 3 ref. <Fig.9,10,12> and <Table 5>	R/W

X	MS1	MS0	X	X	RF0	X	CF0
X	Auto Subsampling Mode		X	X	Manual Subsampling	X	Manual Subsampling

20h	04h	*Control4*	Control 4 ref. <Table 6>	R/W

AF	PD	F5	F6	reserved
Auto flicker detection	Auto Flicker Period	Manual flicker 50Hz	Manual flicker 60Hz	

21h	00h	*reserved*		R/W
22h	X0h	*reserved*		R/W
23h	00h	*Period50(H)*	Period 50	R/W
24h	B0h	*Period50(L)*	Flicker Period Control register for 50Hz light source	

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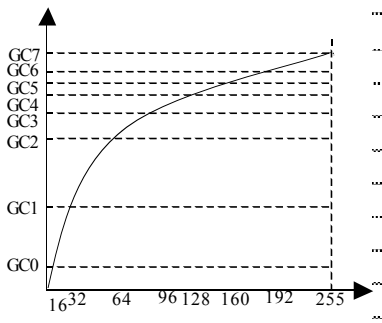
Addr.	Default	Name	Description	R/W
25h	00h	*Period60*	Period 60	R/W
26h	94h		Flicker Period Control register for 60Hz light source	
27h	58h	*RegClk167*	Regclk167 = 1.667ms / master clock period # of Master clock for flicker detection standard time or 1.667 ms time ratio	R/W
28h	00h	*delta50*	50Hz flicker delta	R/W
29h	00h	*delta60*	60Hz flicker delta	R/W
2Ah	00h	*reserved*		R/W
2Bh	03h	*reserved*		R/W
2Ch	00h	*ADCoffset*	ADC offset	R/W *
2Dh	14h	*GammaCorr0*	Gamma Correction Coefficient 0	R/W *
2Eh	35h	*GammaCorr1*	Gamma Correction Coefficient 1	R/W *
2Fh	61h	*GammaCorr2*	Gamma Correction Coefficient 2	R/W
30h	84h	*GammaCorr3*	Gamma Correction Coefficient 3	R/W
31h	A2h	*GammaCorr4*	Gamma Correction Coefficient 4	R/W
32h	BDh	*GammaCorr5*	Gamma Correction Coefficient 5	R/W
33h	D8h	*GammaCorr6*	Gamma Correction Coefficient 6	R/W
34h	FFh	*GammaCorr7*	Gamma Correction Coefficient 7	R/W
35h	06h	*ColorCorr0*	Color Transform Matrix Coefficient, m00	R/W
36h	1Eh	*ColorCorr1*	Color Transform Matrix Coefficient, m01	R/W
37h	12h	*ColorCorr2*	Color Transform Matrix Coefficient, m02	R/W
38h	02h	*ColorCorr3*	Color Transform Matrix Coefficient, m10	R/W
39h	AAh	*ColorCorr4*	Color Transform Matrix Coefficient, m11	R/W
3Ah	53h	*ColorCorr5*	Color Transform Matrix Coefficient, m12	R/W
3Bh	37h	*ColorCorr6*	Color Transform Matrix Coefficient, m20	R/W
3Ch	D5h	*ColorCorr7*	Color Transform Matrix Coefficient, m21	R/W
3Dh	F2h	*ColorCorr8*	Color Transform Matrix Coefficient, m22	R/W
3Eh	03h	*AutoControl1*	Auto ISP Function Control I (ref. <Table 7>) Reserved | | Reserved | WW1 | WW0 | Reserved | AE | AWE 0 | X | 0 | Window [4Fh-56h] Weighting factor | 0 | Auto exposure enable | Auto whiteblance enable	R/W
3Fh	04h	*AutoControl2*	Auto ISP Function Control II | Reserved | RST | RS | Reserved | | FE X | 0 | Register STandby | Still Mode Enable | 0 | 1 | X | anti-Flicker Enable	R/W
40h	80h	*Ytarget*	Y Target : Reference Brightness in auto-exposure mode	R/W
41h	03h	*GlobalGainMin*	Global Gain Min. : Minimum limit of global gain	R/W
42h	03h	*GlobalGainMax*	Global Gain Max. : Maximum limit of global gain	R/W
43h	30h	*reserved*		R/W
44h	46h	*reserved*		R/W
45h	FFh	*reserved*		R/W
46h	FFh	*reserved*		R/W
47h	80h	*AWBT-R*	AWB Red Tuning	R/W
48h	80h	*AWBT-B*	AWB Blue Tuning	R/W
49h	40h	*reserved*		R/W
4Ah	42h	*reserved*		R/W



$$\begin{bmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{bmatrix} = 64 \cdot \begin{bmatrix} 0.257 & 0.504 & 0.098 \\ -0.148 & -0.291 & 0.439 \\ 0.439 & -0.368 & -0.071 \end{bmatrix} \cdot CC$$

, where $[R'\ G'\ B']T = CC \cdot [R\ G\ B]T$

$$\overline{R} = \frac{AWBT\_R}{128} \times \overline{G} \qquad \overline{B} = \frac{AWBT\_B}{128} \times \overline{G}$$

Addr.	Default	Name	Description	R/W
4Bh	02h	*FrmWMin(H)*	Auto frame width minimum	R/W
4Ch	EFh	*FrmWMin(L)*		
4Dh	08h	*FrmWMax(H)*	Auto frame width maximum	R/W
4Eh	CDh	*FrmWMax(L)*		
4Fh	00h	*WeightX1(H)*	WeightX1 : X1 coordination of weight window of auto-exposure process	R/W
50h	D5h	*WeightX1(L)*		
51h	00h	*WeightY1(H)*	WeightY1 : Y1 coordination of weight window of auto-exposure process	R/W
52h	A0h	*WeightY1(L)*		
53h	01h	*WeightX2(H)*	WeightX2 : X2 coordination of weight window of auto-exposure process	R/W
54h	AAh	*WeightX2(L)*		
55h	01h	*WeightY2(H)*	WeightY2 : Y2 coordination of weight window of auto-exposure process	R/W
56h	40h	*WeightY2(L)*		
57h	00h	*reserved*		R
58h	01h	*reserved*		R
59h	9Bh	*reserved*		R/W
5Ah	50h	*OutformCtrl1*	Output Format Control 1 — ref. <Table 8> VBE: Vref. Enable; HRE: Href. Enable; AV: Pclk in Vref; WH: Hsync always; AP: Pclk in Href; NH: Not Hsync; NF: Not Fsync; NP: Not Pclk	R/W
5Bh	00h	*OutformCtrl2*	Output Format Control 2 — ref. <Table 9> Reserved; SEL2; SEL1; SEL0 0; 0; 0; 0; 0; Output Form Select	R/W
5Ch	30h	*OutformCtrl3*	Output Format Control 3 VW3; VW2; VW1; VW0; VS3; VS2; VS1; VS0 Width of FSYNC; Space between FSYNC falling edge and 1'st rising edge HREF after FSYNC falling	R/W
5Dh	03h	*OutformCtrl4*	Output Format Control 4 HY; HC; HW5; HW4; HW3; HW2; HW1; HW0 Change order Y & CbCr; Change order Cb & Cr; Width of HSYNC	R/W
5Eh	00h	*OutformCtrl5*	Output Format Control 3 Reserved; HS5; HS4; HS3; HS2; HS1; HS0 0; 0; Space between HSYNC falling edge and 1'st rising edge of Active Data after HSYNC falling	R/W
5Fh	10h	*EEO*	Edge enhancement offset value	R/W
60h	40h	*EGA*		
61h	FFh	*PCO*		
62h	40h	*reserved*		
63h	40h	*Cb/U-Gain*	Cb or U component gain	R/W
64h	40h	*Cr/V-Gain*	Cr or V component gain	R/W
65h	37h	*reserved*		R/W
66h	55h	*reserved*		R/W
67h	7Dh	*reserved*		R/W

Addr.	Default	Name	Description	R/W
6Bh	X8h	*reserved*		R/W
6Ch	FFh	*reserved*		R/W
6Dh	00h	*reserved*		R/W
6Eh	00h	*reserved*		R/W
6Fh	04h	*reserved*		R/W
70h	00h	*reserved*		R/W
71h	80h	*reserved*		R/W
72h	14h	*reserved*		R/W
73h	10h	*YBright*	Y Bright Offset	R/W
74h	80h	*Ycont*	Y Contrast $Y' = \frac{Ycont}{128} \times (Y - 16) + Ybright$	R/W
75h	EBh	*Ysaturation*	Y Saturation	R/W
76h	03h	*reserved*		R/W
77h	02h	*reserved*		R/W
78h	30h	*reserved*		R/W
79h	00h	*reserved*		R/W

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Register Detail Tables

<Table4> 1Dh Control Register 1

		Description
SM	1	Mechanical Shutter used case (Still 1 case)
	0	Electrical Shutter used case (Still 2 case)
FT	1	Single Frame Transfer enable
	0	Single Frame Transfer disable
AS	1	Automatic sub sampling mode control enable
	0	Automatic sub sampling mode control disable (manual control)
FE	1	Automatic Frame Equalizer control enable
	0	Automatic Frame Equalizer control disable (manual control)
CK(2:0)	000	pixel clock = (External Master clock) / 2 : Default Case
	001	pixel clock = (External Master clock) / 3
	010	pixel clock = (External Master clock) / 4
	011	pixel clock = (External Master clock) / 8
	100	pixel clock = (External Master clock) / 16
	101	pixel clock = (External Master clock) / 32
	110	pixel clock = (External Master clock) / 64
	111	pixel clock = (External Master clock) / 128 ***based on the bayer output**

<Table5> 1Fh Control Register 3

Automatic Sub sampling mode Description

MS	Video Mode	Still Mode
00	Full Sampling	Full Sampling
01	1/4 sub sampling	Full Sampling
10	1/4 sub sampling	1/4 sub sampling
11	Full Sampling	Full Sampling

Manual Sub sampling mode Description

RF = 0	Full sampling
RF = 1	1/2 sub sampling(Row)
CF = 0	Full sampling
CF = 1	1/2 sub sampling(Column)

<Table6> 20h Control Register 4

		Description
AF	1	Automatic flicker detection enable
	0	Automatic flicker detection disable (Manual detection case)
PD	1	Automatic flicker period calculation enable
	0	Automatic flicker period calculation disable (manual prd : period50Hz, 60Hz register)
F5	1	Manual 50Hz period enable
	0	function OFF
F6	1	Manual 60Hz period enable
	0	function OFF

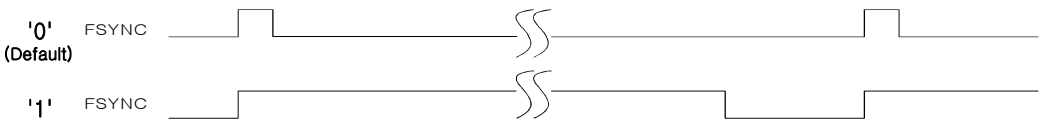
<Table7> 3Eh Auto Control 1

mnemonic	Description
WW[1:0]	**Weighting window mode** **Default** = "00" **Related Registers** : weighting window register [4Fh-56h] Brightness data within the weighting window [4Fh-56h] have weighting factor according to the weighting window mode as follows; 00 : x1 01 : x2 10 : x4 11 : x8 As weighting factor is growing, central image brightness within the weighting window has more impact on overall auto exposure function. Size and mode of weighting window have also some effects on the resultant brightness of image after AE process.
AE	**Auto Exposure Enable** **Default** : '1' **Related Registers** : *Auto Control1*[3Eh], *Y_Target*[40h], I*ntegration Lines*[1Ah-1Ch], *AELock*[44h], *Global Gain*[15h], *Global Gain min*[41h], *Global Gain max*[42h], *Frame Width* [04h-05h], *FrmWmin*[4Bh-4Ch], *FrmWmax*[4Dh-4Eh], *Frame Height*[06h-07h] '1' : auto exposure mode '0' : auto exposure mode off During the auto exposure mode, *Integration Lines, GlobalGain, FrameWidth* registers cannot be written. Refer to *Y_Target or other related* registers for more detailed description.
AWE	**Auto White Balance Enable** **Default** : '1' **Related Registers** : *AWBLock*[43h], *AWBTune*[47h-48h], *R-Gain*[16h], *B-Gain*[18h] '1' : auto white balance mode enabled '0' : auto white balance mode disenabled Refer to *AWBTune* and *AWBLock* registers to gain more detailed desctiption.

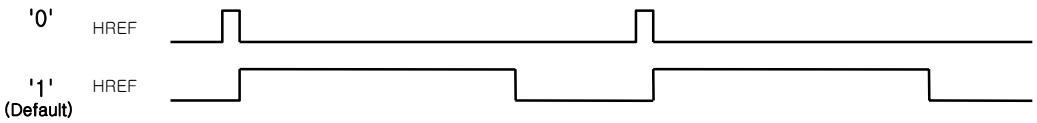
<Table8> 5Ah Output Format Control 1

mnemonic	Description
VRE	Vref. Enable
HRE	Href. Enable
AV	And PCLK with Vref (PCLK in all Active Window)
WH	Whole HSYNC
AP	And PCLK with Href (PCLK in Active Window)
NH	Not HSYNC
NF	Not FSYNC
NP	Not PCLK

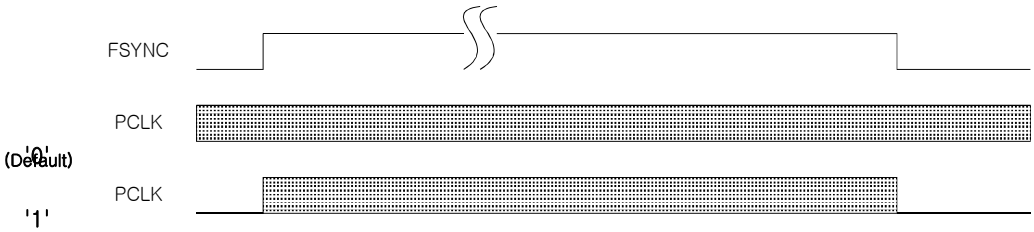
VRE : Vreference Enable



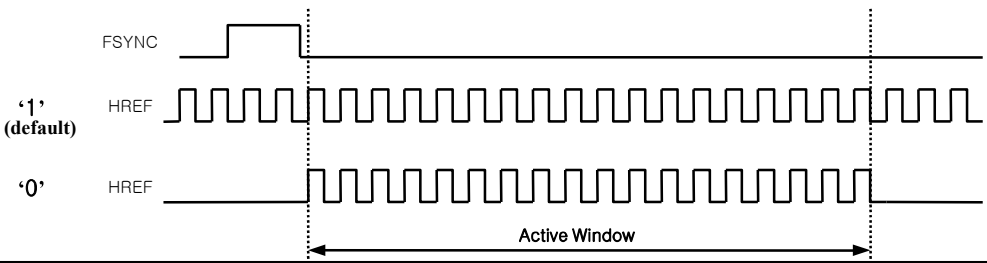
HRE : Hreference Enable



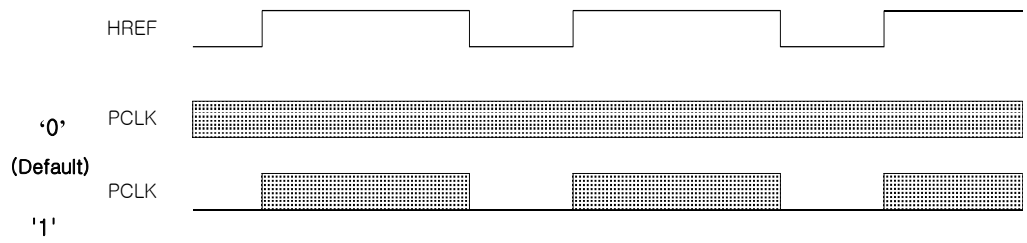
AV : And PCLK with Vref (PCLK in all Active Window)



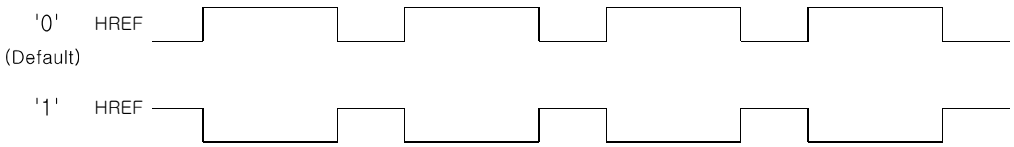
WH : Hsync control (0 : HSYNC output for Active period 1 : HSYNC output for whole period)



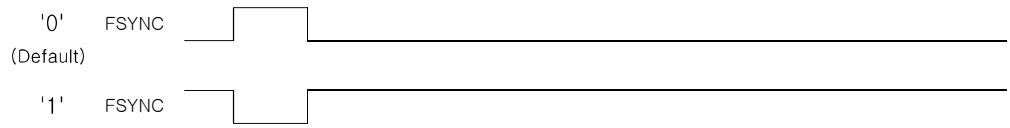
AP : And PCLK with Href (PCLK in Active Window)



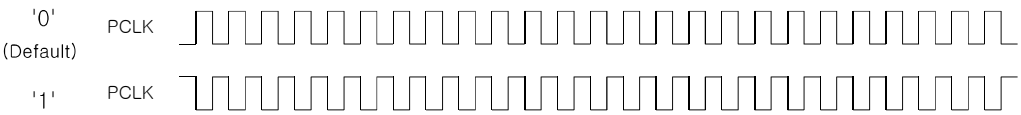
NH : inverted HSYNC



NF : inverted FSYNC



NP : inverted PCLK

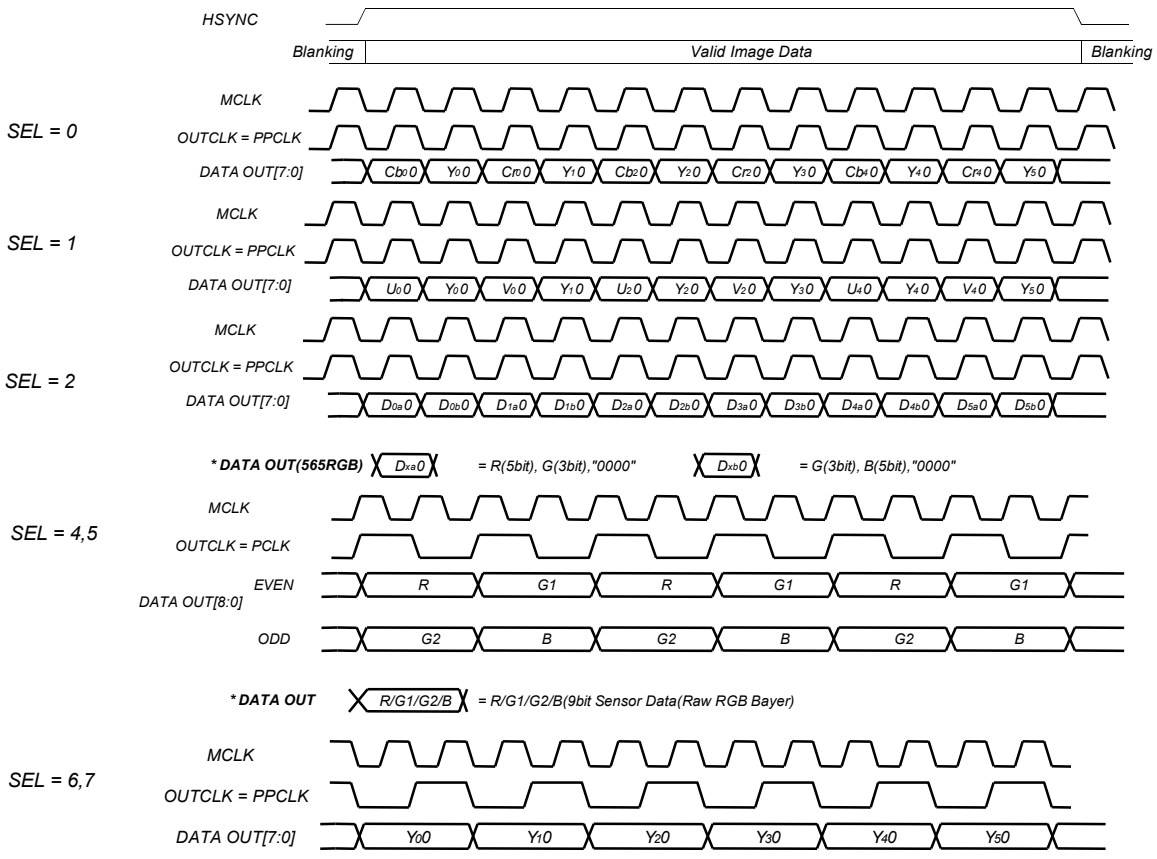


<Table9> 5Bh Output format Control 2

SEL	OUTPUT Data(12bit)	CLK / (DATA)	Output Pin
000	YCbCr	PPCLK/(8bit)	D<11:4>
001	YUV	"	"
010	565RGB	"	D<11:4> (R<4:0>, G<5:3>) or (G<2:0>, B<4:0>)
011	888RGB	PPCLK/(12bit)	D<11:0> (R<7:0>, G<7:4>) or (G<3:0>, B<7:0>)
100	Raw RGB Bayer	PCLK/(9bit)	D<11:3>
101	ISP Bayer	PCLK/(8bit)	D<11:4>
110	Mono-Mono	"	"
111	Color-Mono	"	"

- Mono-Mono : Mono Sensor
- Color-Mono : Color Sensor, Mono output
- Bayer : Sensor Data , HSYNC, VSYNC output

< Figure of waveform >



Electrical Characteristics

Absolute Maximum Ratings *

VDD Supply Voltage ---------- -0.3V to 2.8V
DC Voltage at any input pin ---------- -0.3V to VDD+0.3V
DC current at any input pin ---------- -10mA to +10mA
Storage Temperature ---------- -40°C to +125 °C

Table 10. DC Characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
V_{DD}	Digital, Analog, Pixel VDD voltage relative to GND(DGND, AGND, PGND) level.	2.2	2.5	2.8	V
HV_{DD}	High VDD(HVDD) voltage relative to GND(DGND) level.	2.2	2.5 or 3.3	3.6	V
I_{DD1}	Supply current at 30 fps. Currents are programmable through I2C serial interface.		25	30	mA
I_{DD2}	Standby supply current		30	80	uA
V_{IL1}	Input voltage LOW level			0.2VDD	V
V_{IH1}	Input voltage HIGH level	0.8VDD			V
V_{IL2}	Input voltage LOW level for SCL, SDA.			0.7	V
V_{IH2}	Input voltage HIGH level for SCL, SDA.	1.5			V
C_{IN}	Input pin capacitance			10	pF
V_{OL1}	Output Voltage LOW			0.1VDD	V
V_{OH1}	Output Voltage HIGH	0.9VDD			V
V_{OL2}	Output Voltage LOW level for SCL, SDA.			0.2	V
V_{OH2}	Output Voltage HIGH level for SCL, SDA.	VDD-0.2			V
I_{IN}	Input leakage current			5	nA

* Excessive stresses may cause permanent damage to the device.

Table 11. AC Characteristics (All outputs : 15pF load conditions)

Symbol	Descriptions	Min	Typ	Max	Unit
f_{MCLK}	Master clock Frequency			27	MHz
duty	Master clock duty cycle		50		%
t1	Master clock rise/fall time		10		ns
t2	PCLK rise/fall time		15		ns
t3	MCLK falling edge to HSYNC			15	ns
t4	MCLK falling edge to digital output			15	ns
t5	MCLK rising to PCLK			15	ns

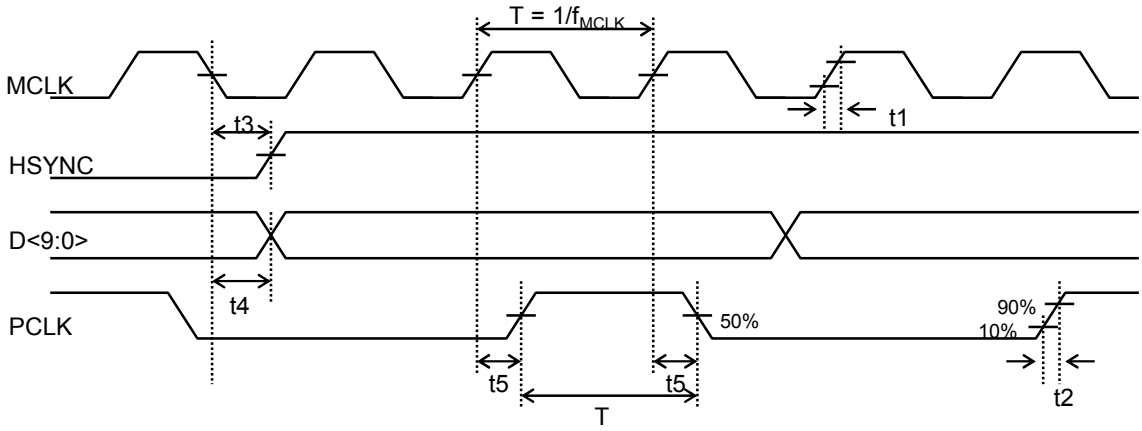


Fig. 13 Clock, Data, and Sync Timing.

Symbol	Descriptions	Min	Typ	Max	Unit
t6	Reset time	8			T

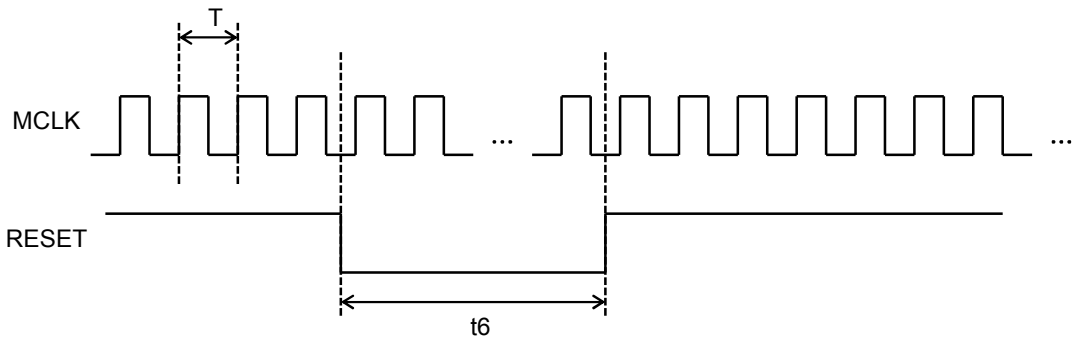


Table 12. Electro- Optical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Sens	Sensitivity	1)	2.25	3.1	4.65	V/Lux.sec
Vsat	Saturation Level	2)	0.69	0.77	0.85	V
Vdrk	Dark Signal	3)		13	21.3	mV
PSNU	PIXEL Signal NON-Uniformity	4)		15	40	%
DR	Dynamic range	5)		50		dB

Notes :

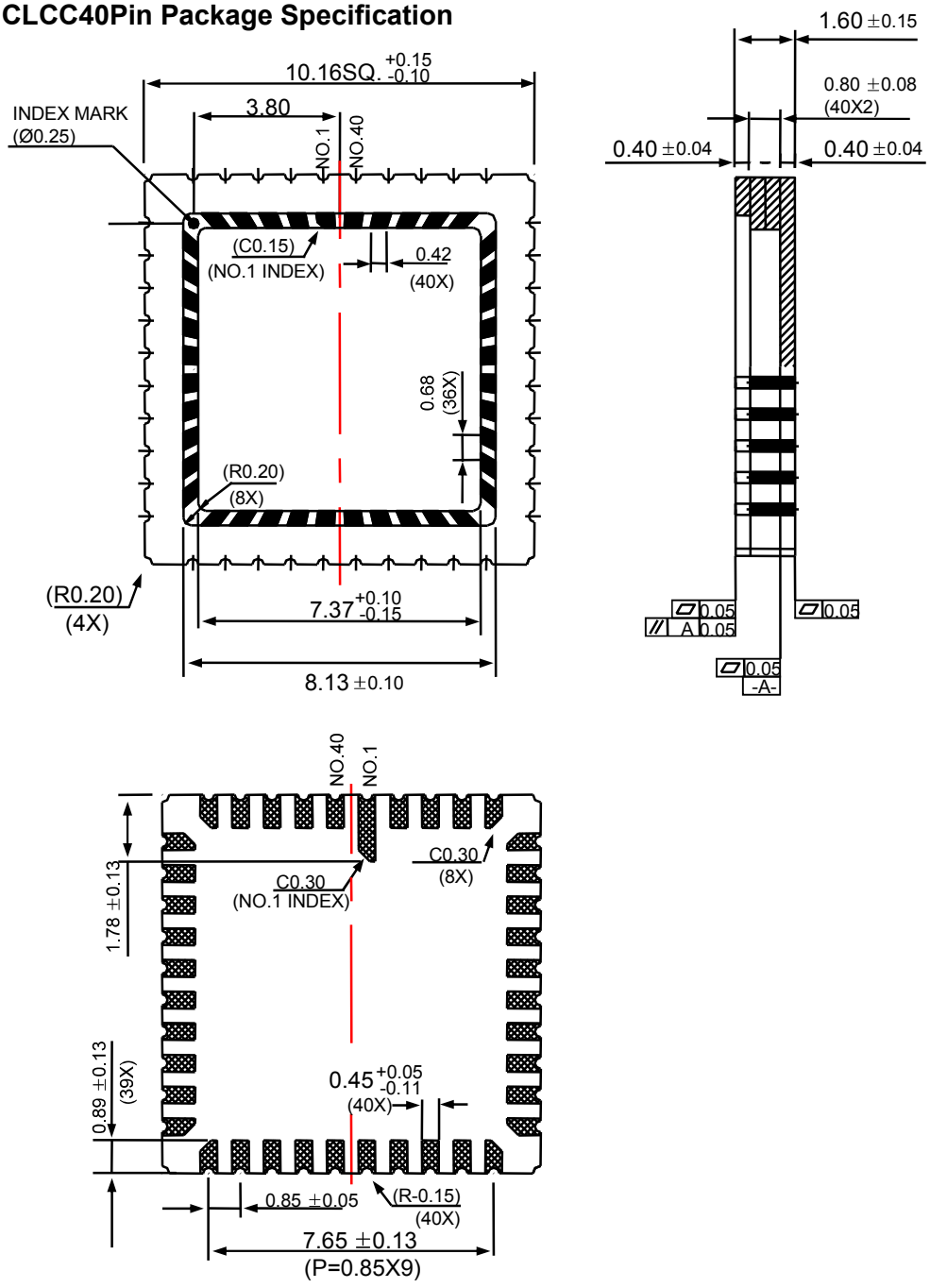
1) Measured sensitivity of Green pixel at 3lux illumination for 54ms integration time
2) For λ=550 wavelength
3) Measured at the zero illumination for 66ms at the 40 degree
4) For 16X16 pixel region under illumination with output signal equal to 50% of saturation signal.

$$\frac{\text{Max value of Block} - \text{Min value of Block}}{\text{Average value of all blocks}} \times 100$$

5) For frame rate = 30 fps
20*Log (Saturation Signal / Dark signal) [dB]

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

CLCC40Pin Package Specification



NOTE:
1. NI 2.0um + Au 0.5um MIN
2. NO METALLIZATION ON SEAL RING AND DIE ATTACH PAD.
3. UNIT : mm

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

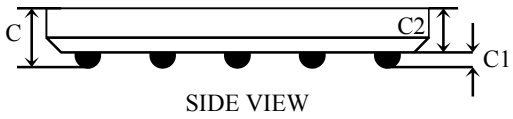
CSP(Chip Scale Package) Specification

	Symbol	Normal	Min	Max
Package Body Dimension X	**A**	3.830	3.805	3.855
Package Body Dimension Y	**B**	5.410	5.385	5.435
Package Height	**C**	0.960	0.900	1.020
Package Body Thickness	**C2**	0.830	0.795	0.865
Ball Height	**C1**	0.130	0.100	0.160
Ball Diameter	**D**	0.25	0.220	0.280
Pins Pitch X ,Y axis	**J**	0.68	.	.
Edge to Ball Center Distance along X	**S1**	0.555	0.525	0.585
Edge to Ball Center Distance along Y	**S2**	0.665	0.635	0.695

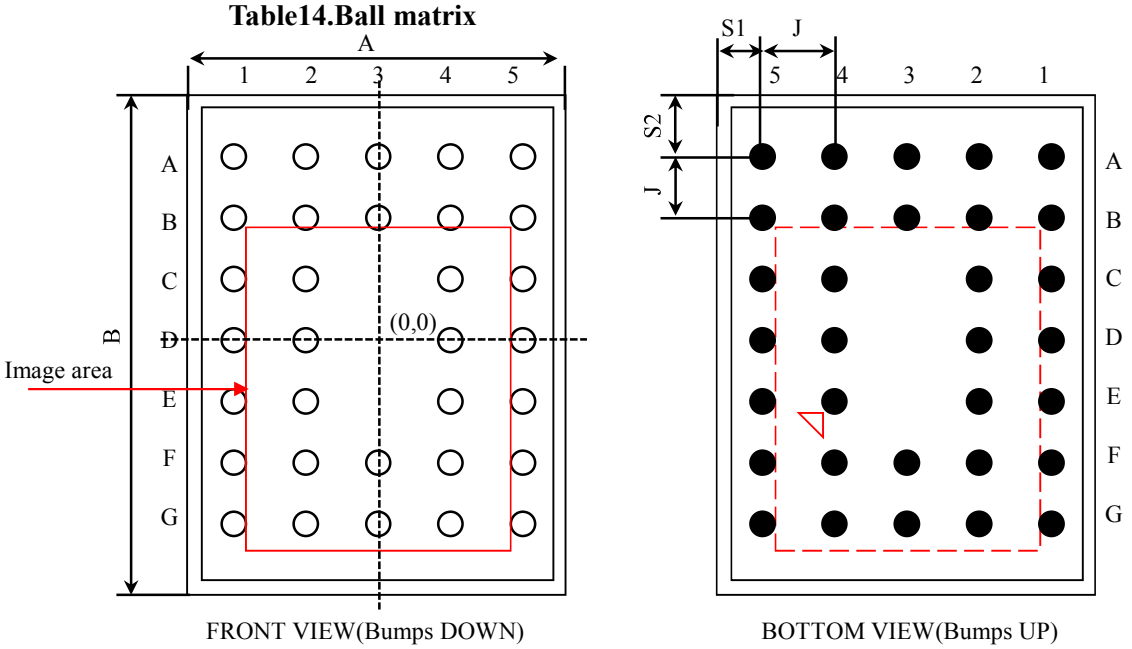
Table 13. Package Dimensions Unit:mm

	1	2	3	4	5
A	PVDD	DVDD	HSYNC	PCLK	MCLK
B	DGND	VSYNC	N.C	SYNC DGND	DVDD
C	DVDD	PGND		N.C	HVDD
D	D0	D1		STDBY	SCL
E	DVDD	D2		D6	SDA
F	AVDD	D4	N.C	RSTB	AGND
G	AGND	D3	D5	D7	AVDD

Table14.Ball matrix



SIDE VIEW



FRONT VIEW(Bumps DOWN)

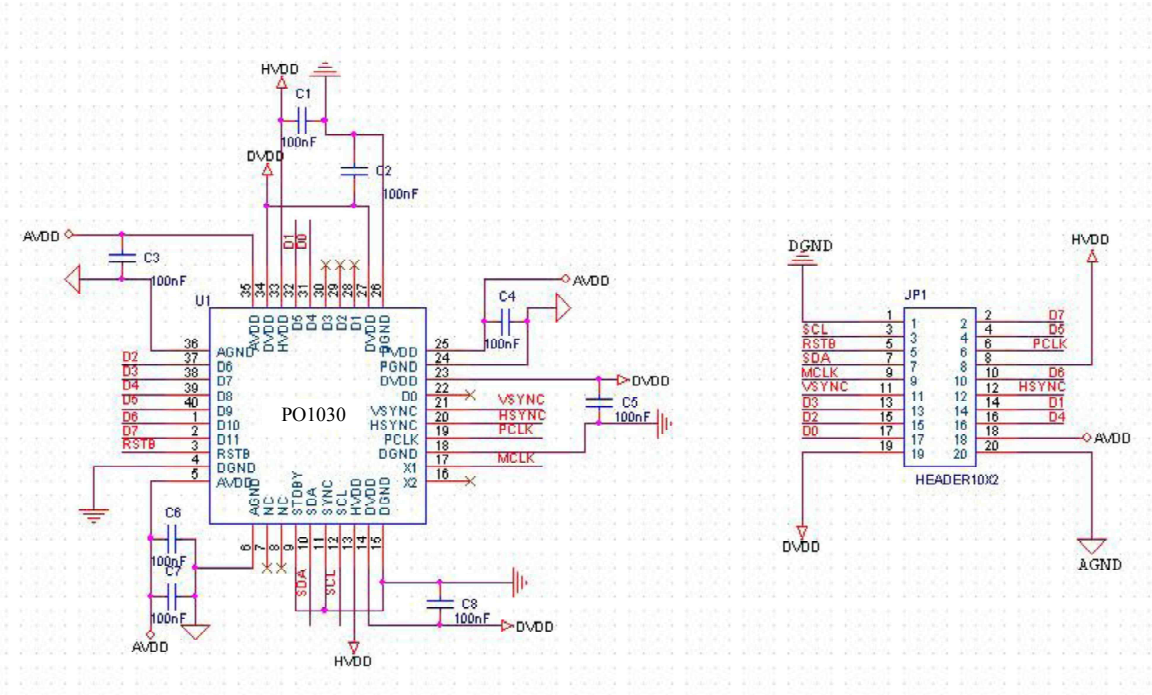
BOTTOM VIEW(Bumps UP)

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Module Specification(&Lens)

Module name	PO1030xC-MSx1-PP0x
Size	6.0mmX7.0mmX5.7(+0.0/-0.3)mm
Lens construction	2 Plastic & IR filter(0.4T)
Focal Length	3.37mm ± 5%
View angle	62.2º ± 5%(diagonal 4.16mm)
Aperture	F#2.8
TV Distortion	-0.94
Outer Mechanical Dimension is Flexible According to Customer's Requirement	

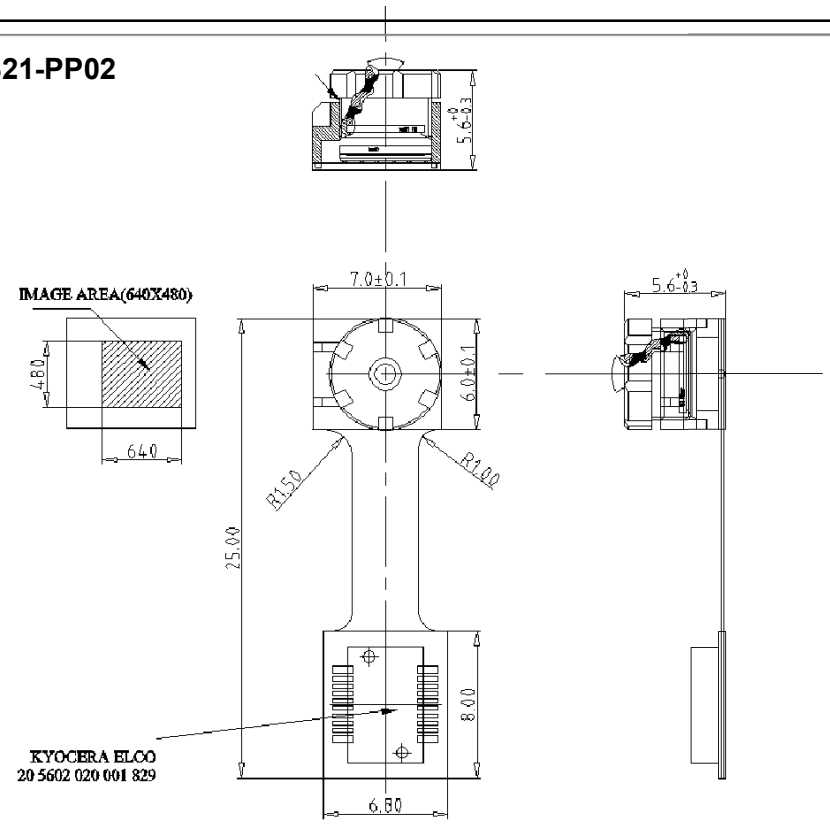
Module schematic



CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Module Diagram

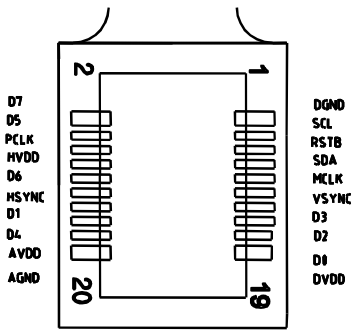
PO1030xC-MS21-PP02



Unit : mm

Standard Pin assignment

19	DVDD	20	AGND
17	D0	18	AVDD
15	D2	16	D4
13	D3	14	D1
11	VSYNC	12	HSYNC
9	MCLK	10	D6
7	SDA	8	HVDD
5	RSTB	6	PCLK
3	SCL	4	D5
1	DGND	2	D7



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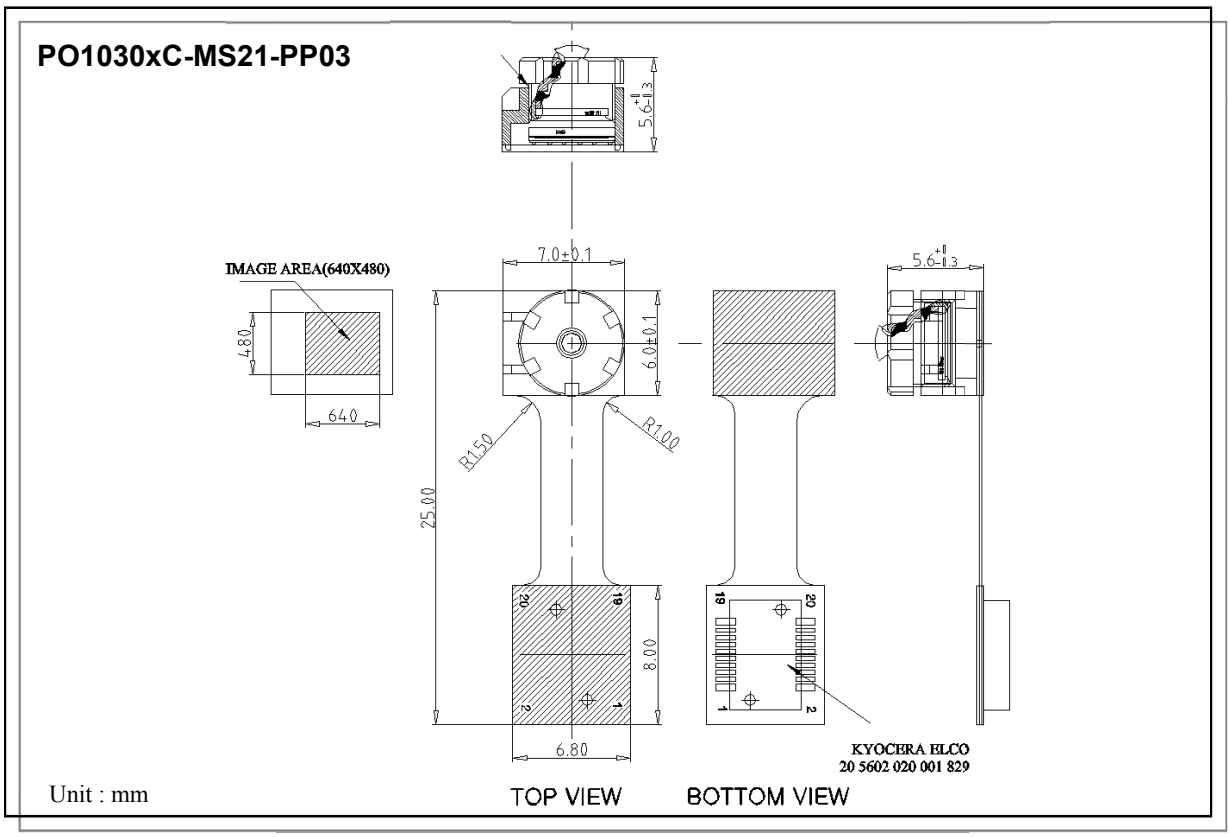
*Outer Mechanical Dimension is Flexible According to Customer's Requirement

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Module Diagram



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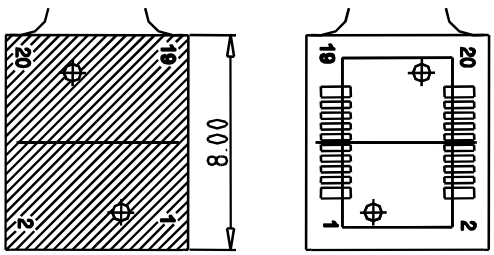
13	D3	14	D1
11	VSYNC	12	HSYNC
9	MCLK	10	D6
7	SDA	8	HVDD
5	RSTB	6	PCLK
3	SCL	4	D5
1	DGND	2	D7



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Recommended Register Values

Overview

- The better image can be acquired to set up recommended register value.

- **step 1>** Write 0Ah to Register 3Eh
- **step 2>** Give delay time of 1 frame.
- **step 3>** Write 50h to Register 16h and 50h to Register 18h.
- **step 4>** Write the following recommended register values.

1. Initialization registers

Address (Hex)	Register Name	Default Value	Recommended value	Descriptions
1E	*Control2*	00000000 (00h)	00000011 (03h)	
21	*Control5*	00000000 (00h)	10010000 (90h)	
2D	*Gamma Corr.0*	00010100 (14h)	00011100 (1Ch)	Gamma Correction Value
2E	*Gamma Corr.1*	00110101 (35h)	01000110 (46h)	
2F	*Gamma Corr.2*	01100001 (61h)	01110101 (75h)	
30	*Gamma Corr.3*	10000100 (84h)	10010110 (96h)	
31	*Gamma Corr.4*	10100010 (A2h)	10110001 (B1h)	
32	*Gamma Corr.5*	10111101 (BDh)	11001000 (C8h)	
33	*Gamma Corr.6*	11011000 (D8h)	11011111 (DFh)	
3E	*AutoControl1*	00000011 (03h)	00001011 (0Bh)	
40	*Ytarget*	10000000 (80h)	10010000 (90h)	
59	*Conv. Control*	10011011 (9Bh)	00011011 (1Bh)	
5F	*EEO*	00010000 (10h)	00000000 (00h)	Edge Enhancement offset value
60	*EGA*	01000000 (40h)	10000000 (80h)	Edge Enhancement rate

2. Normal Mode (after applying table 1 register values)

Address (Hex)	Register Name	Default Value	Recommended value	Descriptions
78	*Da_subD*	00110000 (30h)	00010100 (14h)	
6F	*Conv_ctrl2*	00000100 (04h)	00000001 (01h)	
1D	*Control1*	X0011000 (18h)	X0011000 (18h)	
42	*Global Gain Max*	00000011 (03h)	00010100 (14h)	
63	*Cb/U-Gain*	01000000 (40h)	00111000 (38h)	
64	*Cr/V-Gain*	01000000 (40h)	00111000 (38h)	

Column Fixed Pattern Noise Removal : Register 12h

Global I Bias register controls the overall current biases in every branch of analog circuits. The recommended values in the table were acquired from various experimentations. If extremely low power is required, *Global I Bias* can be lowered further, but the images may be degraded because of Column FPN Noise if the frame rate is not lowered. Under low luminance, vertical stripe patterns may appear. Then, the current biases must be increased to remove the fixed noise pattern.

•IMPORTANT

PO1030 has oscillation problem in very high luminance. The following support code in SYSTEM(MCU) using the camera need to be implemented.

This code must be executed periodically (At least, every 0.5 seconds.) by using the method such as internal timer.

Void code()
{
Read Integration Register (0x1A, 0x1B);
if (Integration < 20)
Write Register 0x1E to 0x00;
else if (Integration > 80)
Write Register 0x1E to 0x03;
}

EX)

```
// ReadRegister(unsigned char RegisterAddress);
// WriteRegister(unsigned char RegisterAddress, unsigned char RegisterValue);

int g_bstate, g_cstate;

// Initialize variable everytime camera start
void camera_start()
{
        g_bstate = g_cstate = 1;
}
…
void _isr TimerInterrput()
{
        unsigned char intTH, intTL;
        int intT;
        unsigned char Rsrst;

        intTH = ReadRegister(0x1A);
        intTL = ReadRegister(0x1B);
        intT = 256*intTH + intTL;

        if (intT < 20)  {
              g_cstate = 0;
              Rsrst = 0x00;
        }
        else if (intT > 80)  {
              g_cstate = 1;
              Rsrst = 0x03;
        }

        if (g_cstate != g_bstate)  {
             WriteRegister(0x1E, Rsrst);
             g_bstate = g_cstate;
        }
}
```

Framerate Control

If you apply following algorithm in your system, frame rate is changed in low luminance and make image bright, and also horizontal noise is reduced in low luminance**.** You can change MAX_GAIN and MAX_FRAMEWIDTH as you want. This code must be executed periodically (At least, every 0.5 seconds.) by using the method such as internal timer.

EX)

```
// ReadRegister(unsigned char RegisterAddress);
// WriteRegister(unsigned char RegisterAddress, unsigned char RegisterValue);

#define MAX_GAIN                0x14
int     gState;

// Initialize this variable everytime camera start
void camera_start()
{
    gState = 0;
}
…
Void FrateRateControl()
{
     unsigned char gain;

    gain = ReadRegister ( 0x15 );
    switch ( gState ) {
    case 0 : if ( gain >= MAX_GAIN ) {
                WriteRegister (0x3e, 0x0E);
                gState = 1;
            }
            break;
    case 1: if ( gain == 0x03) {
                WriteRegister (0x3e, 0x0B);
                gState = 0;
            }
            break;
    }
}
```

PC Board Layout Considerations

It is important that care be given to the PC board layout to reduce power noise. Following Figures show recommended connection diagrams for the PO1030 according to the standby method.

Stand-by method

1. Method 1: Power cut-off

MCLK, RSTB pins of the module must be made to '0' with power cut-off. Otherwise, leakage current can be measured.

=> Sensor reset can be controlled by power cut-off by connecting RSTB pin to HVDD not other VDD using 10K register and 1uF capacitor as shown in above Figure 1.

(1) **Case 1** : I/O VDD of Backend chip ≤ (Sensor Core VDD (= 2.5V) + 0.3V)

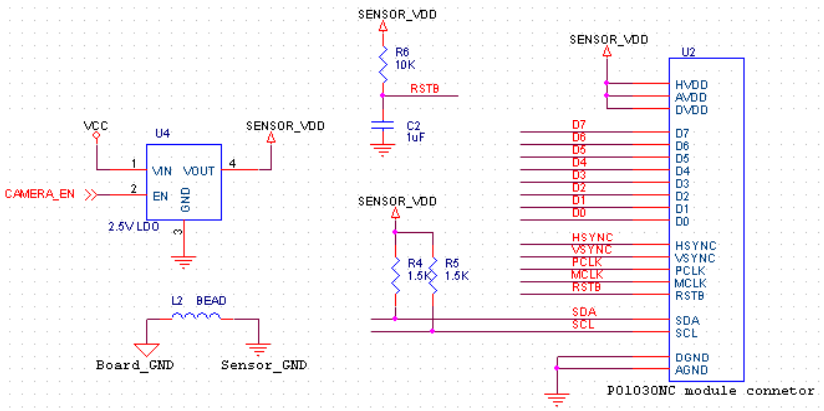

Figure 1. PO1030 module typical connection diagram for case 1 of Method 1

(2) **Case 2** : I/O VDD of Backend chip > (Sensor Core VDD (2.5V) + 0.3V)

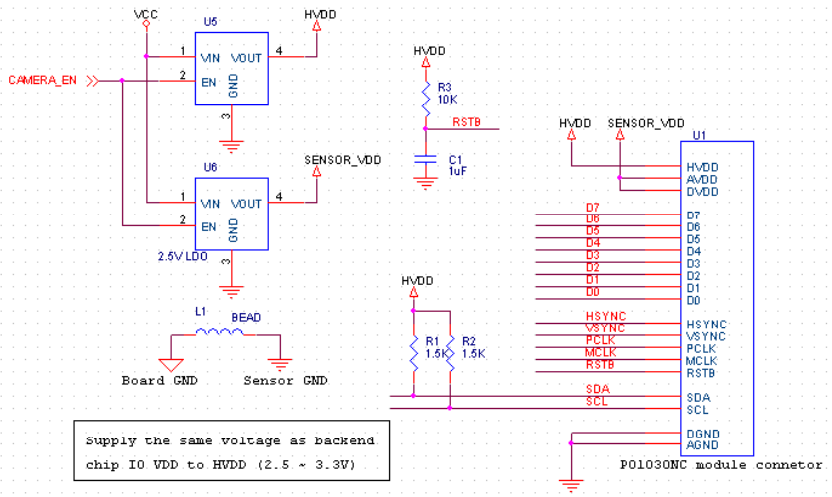

Figure 2. PO1030 module typical connection diagram for case 2 of Method 1

2. Method 2 : Set stand-by register though I2C
- When entering to Stand-by Mode
  1> Set Reg.0x07 to 0x11
  2> Delay 1 frame time
  3> Set RST bit of Reg.0x3F to '1'
  4> Delay 1 frame time
  5> Set RST bit of Reg.0x3F to '0'
  6> Delay ¼ frame time
  7> Set RST bit of Reg.0x3F to '1'
- When coming back to Normal Mode
  1> Set RST bit of Reg. 0x3F to '0'
  2> Set Reg.0x07 to 0x57

=> Tie RSTB pin to GPIO of MCU or backend chip so that you can control sensor reset.

(1) **Case 3** : I/O VDD of Backend chip ≤ (Sensor Core VDD (= 2.5V) + 0.3V)

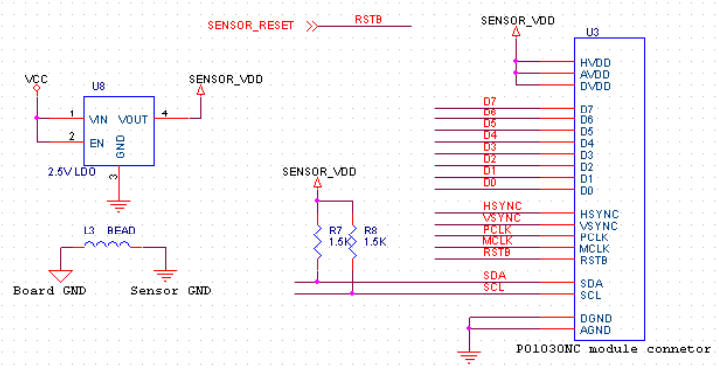

Figure 3. PO1030 module typical connection diagram for Case 3

(2) **Case 4** : I/O VDD of Backend chip ≤ (Sensor Core VDD (= 2.5V) + 0.3V)

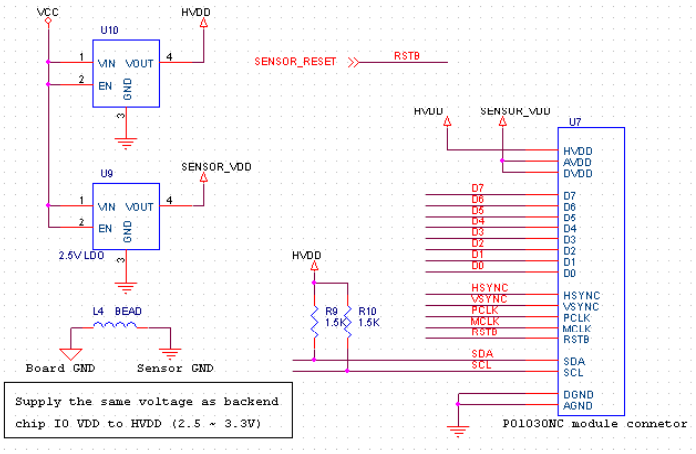

Figure 4. PO1030 module typical connection diagram for Case 4

Flicker Free Mode

Address (Hex)	Register Name	Default Value	Appropriate value	Descriptions
23	*Period50H*	00000000 (00h)	Refer to following example	See the following example. (When X1(mclk)= 12 MHz)
24	*Period50L*	00000000 (B0h)	,,	
25	*Period60H*	00000000 (00h)	,,	
26	*Period60L*	10010100 (94h)	,,	

Address (Hex)	Register Name	Flicker Off	Flicker On	Descriptions
20	*Control4*	0000010X (04h)	0010010X (24h)/ 0001010X (14h)	50Hz / 60Hz
3F	*Auto Control 2*	X0000100 (04h)	X0000101 (05h)	
72	*Reserved*	00010100 (14h)	00010000 (10h)	

-Flicker Period Control Register Setting

Related Registers **:** *Reg.23(h), Reg.24(h) – for 50Hz light source.*

Reg.25(h), Reg.26(h) – for 60Hz light source.

Flicker Period Reg. Value = (Frame Height*Frame Rate)/(Freq.*2) << 6

ex) - 60Hz, MCLK = 12MHz

Frame Height = 600 line (default)

Frame Rate = (15 x 12 / 13.5) fps; // when MCLK = 13.5 MHz, Framerate = 15 fps .

Flicker Period = 600 x (15 x 12 / 13.5) / (60 x 2) = 0x43

Flicker Period Reg. Value = Flicker Period <<(shift) 6 = 0x10C0

Reg.25(h) = 0x10; Reg.26(h) = 0xC0;

- 50Hz, MCLK = 12MHz

Frame Height = 600 line (default)

Frame Rate = (15 x 12 / 13.5) fps; // when MCLK = 13.5 MHz, Framerate = 15 fps .

Flicker Period = 600 x (15 x 12 / 13.5) / (50 x 2) = 0x50

Flicker Period Reg. Value = Flicker Period <<(shift) 6 = 0x1400

Reg.23(h) = 0x14; Reg.24(h) = 0x00;