PCF8591

8-bit A/D and D/A converter

Rev. 7 — 27 June 2013 Product data sheet

1. General description

The PCF8591 is a single-chip, single-supply low-power 8-bit CMOS data acquisition device with four analog inputs, one analog output and a serial I^2C-bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C-bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional I^2C-bus.

The functions of the device include analog input multiplexing, on-chip track and hold function, 8-bit analog-to-digital conversion and an 8-bit digital-to-analog conversion. The maximum conversion rate is given by the maximum speed of the I^2C-bus.

2. Features and benefits

- Single power supply
- Operating supply voltage 2.5 V to 6.0 V
- Low standby current
- Serial input and output via I^2C-bus
- I^2C address selection by 3 hardware address pins
- Max sampling rate given by I^2C-bus speed
- 4 analog inputs configurable as single ended or differential inputs
- Auto-incremented channel selection
- Analog voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analog output.

3. Applications

- Supply monitoring
- Reference setting
- Analog control loops

6. Block diagram

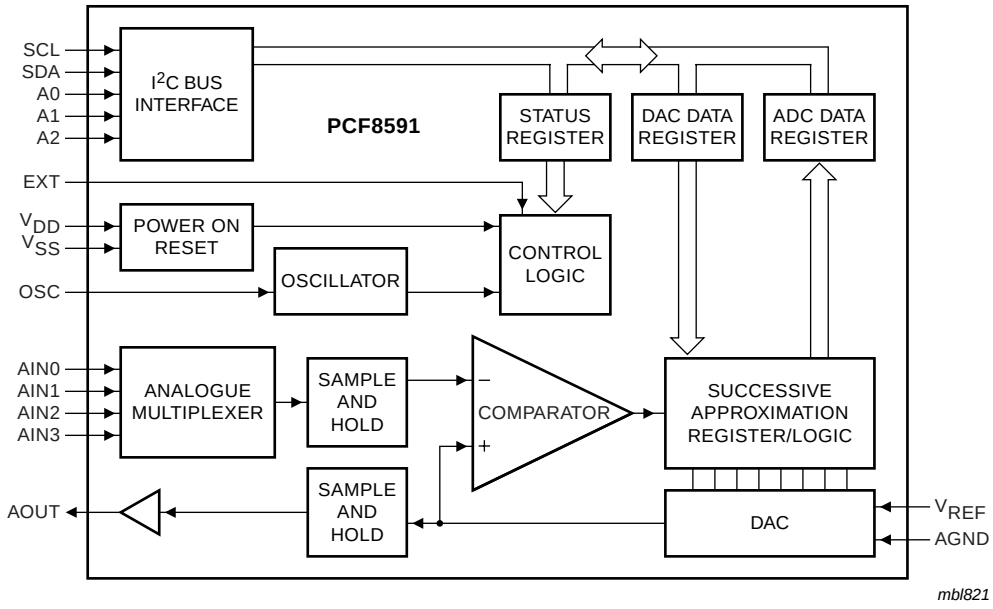
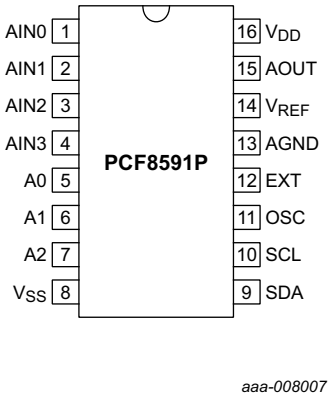


Fig 1. Block diagram of PCF8591

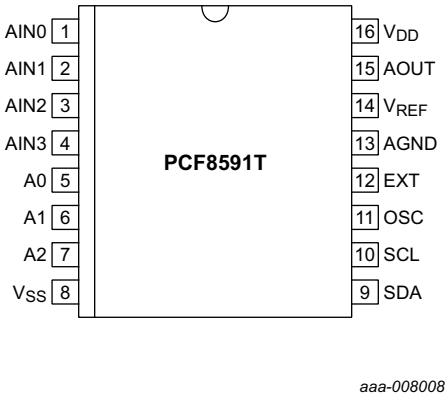
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 22 on page 21.

Fig 2. Pin configuration for PCF8591P (DIP16)



Top view. For mechanical details, see Figure 23 on page 22.

Fig 3. Pin configuration for PCF8591T (SO16)

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
AIN0	1	analog inputs (A/D converter)
AIN1	2	
AIN2	3	
AIN3	4	
A0	5	hardware slave address
A1	6	
A2	7	
V_{SS}	8	ground supply voltage
SDA	9	I^2C-bus serial data input and output
SCL	10	I^2C-bus serial clock input
OSC	11	oscillator input/output
EXT	12	external/internal switch for oscillator input
AGND	13	analog ground supply
V_{REF}	14	voltage reference input
AOUT	15	analog output (D/A converter)
V_{DD}	16	supply voltage

8. Functional description

8.1 Addressing

Each PCF8591 device in an I^2C-bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address is always sent as the first byte after the start condition in the I^2C-bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Table 5 on page 13, Figure 15 on page 13 and Figure 16 on page 13).

8.2 Control byte

The second byte sent to a PCF8591 device is stored in its control register and is required to control the device function. The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Figure 4). If the auto-increment flag is set, the channel number is incremented automatically after each A/D conversion.

If the auto-increment mode is desired in applications where the internal oscillator is used, the analog output enable flag must be set in the control byte (bit 6). This allows the internal oscillator to run continuously, by this means preventing conversion errors resulting from oscillator start-up delay. The analog output enable flag can be reset at other times to reduce quiescent power consumption.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel is always channel 0. The most significant bits of both nibbles are reserved for possible future functions and must be set to logic 0. After a Power-On Reset (POR) condition, all bits of the control register are reset to logic 0. The D/A converter and the oscillator are disabled for power saving. The analog output is switched to a high-impedance state.

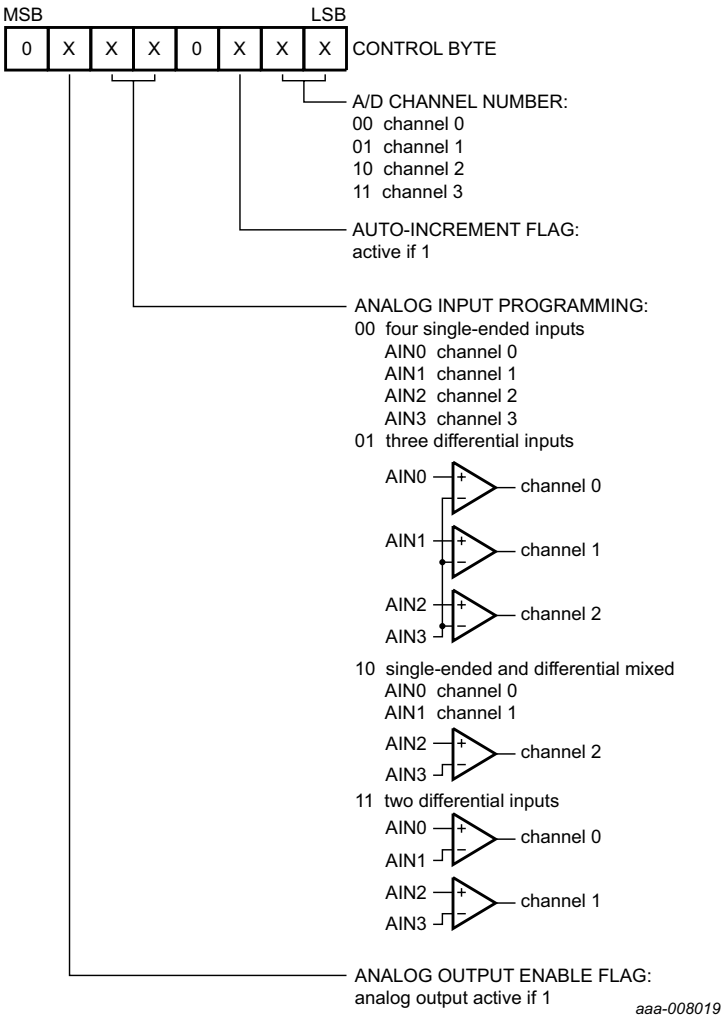


Fig 4. Control byte

8.3 D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analog voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Figure 5).

The analog output voltage is buffered by an auto-zeroed unity gain amplifier. Setting the analog output enable flag of the control register switches this buffer amp on or off. In the active state, the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The formula for the output voltage supplied to the analog output AOUT is shown in Figure 6. The waveforms of a D/A conversion sequence are shown in Figure 7.

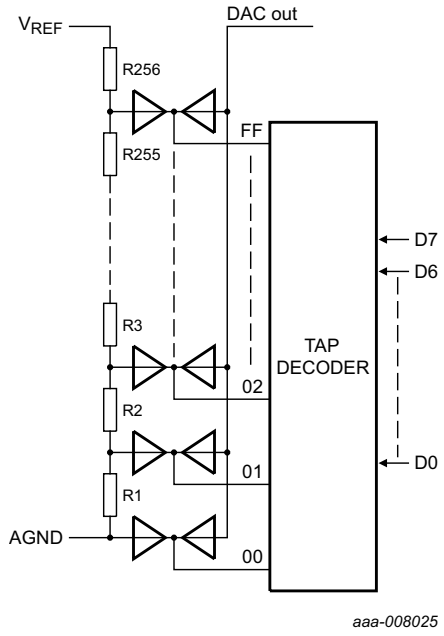


Fig 5. DAC resistor divider chain

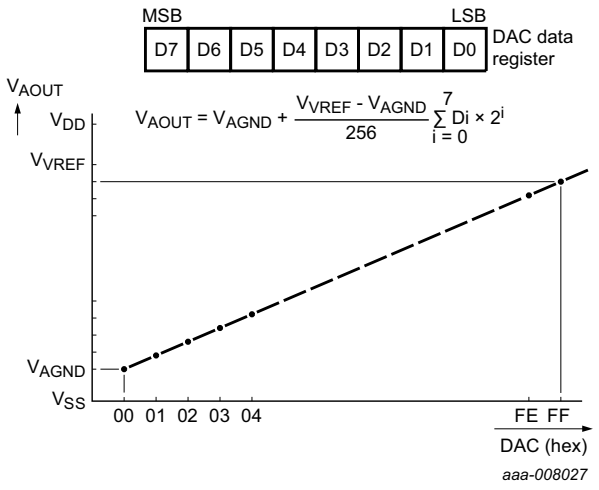


Fig 6. DAC data and DC conversion characteristics

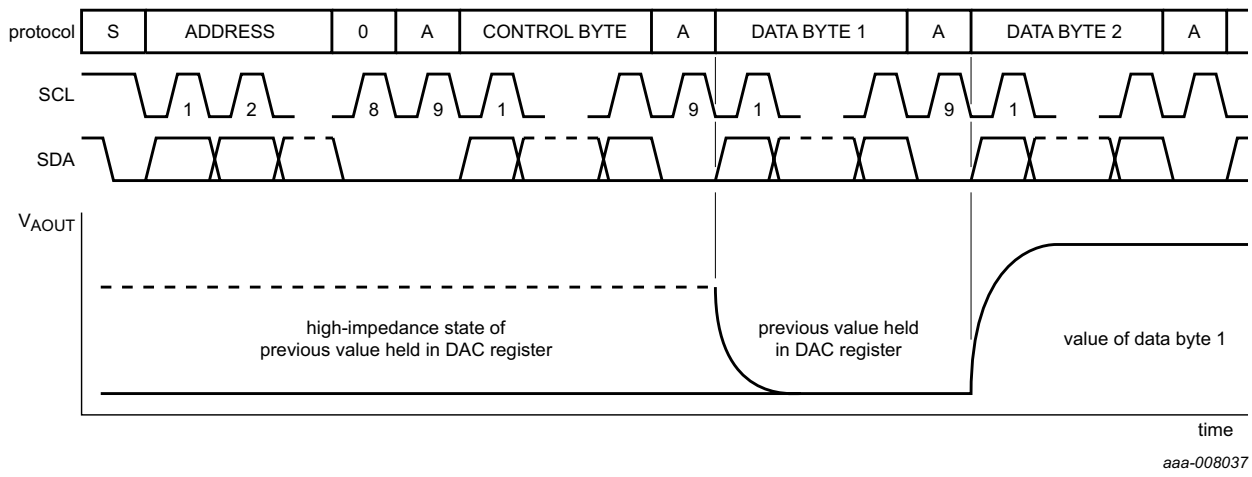


Fig 7. D/A conversion sequence

8.4 A/D conversion

The A/D converter uses the successive approximation conversion technique. The on-chip D/A converter and a high-gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Figure 8).

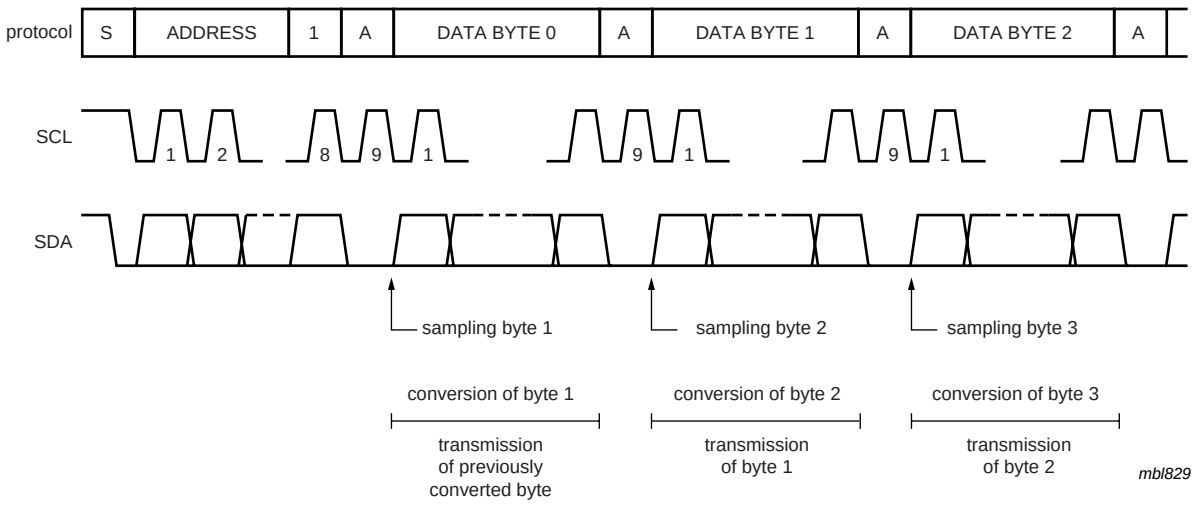


Fig 8. A/D conversion sequence

Once a conversion cycle is triggered, an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Figure 9 and Figure 10).

The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set, the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a POR condition, the first byte read is 80h. The protocol of an I^2C-bus read cycle is shown in Section 9.

The maximum A/D conversion rate is given by the actual speed of the I^2C-bus.

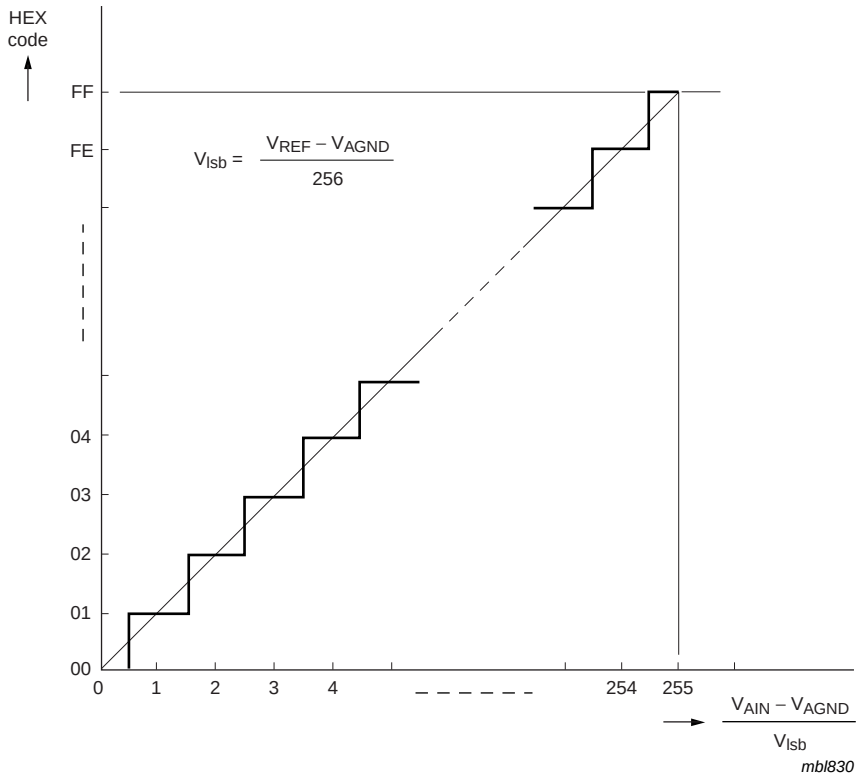


Fig 9. A/D conversion characteristics of single ended inputs

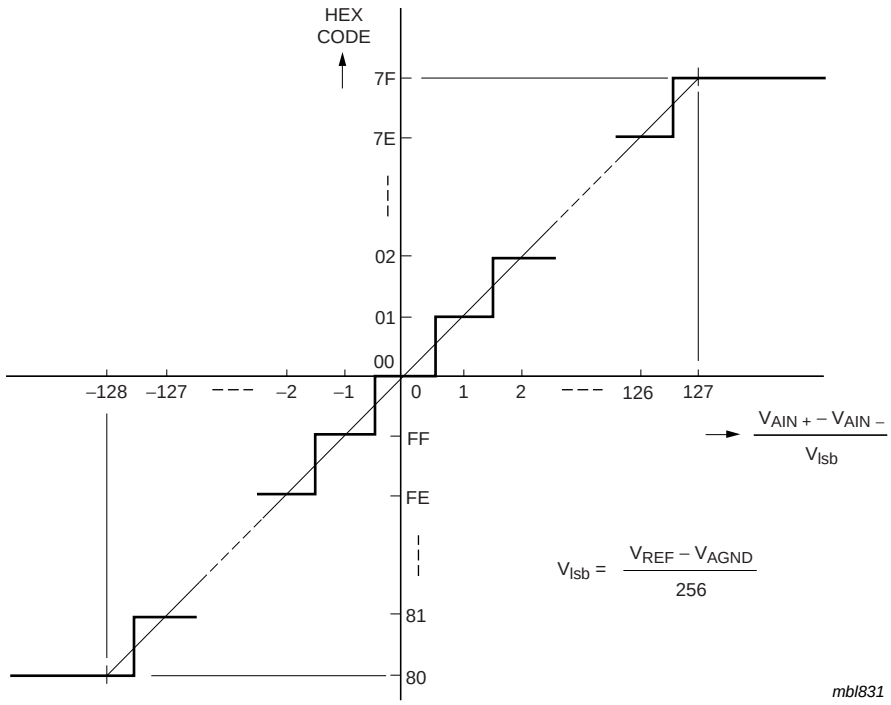


Fig 10. A/D conversion characteristics of differential inputs

8.5 Reference voltage

For the D/A and A/D conversion, either a stable external voltage reference or the supply voltage must be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analog ground. It may have a DC off-set with reference to V_{SS}.

A low frequency can be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier (see Section 10 and Figure 6)

The A/D converter can also be used as a one or two quadrant analog divider. The analog input voltage is divided by the reference voltage. The result is converted to a binary code. In this application, the reference voltage must be kept stable during the conversion cycle.

8.6 Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin must be connected to V_{SS}. The oscillator frequency is available at the OSC pin.

If the EXT pin is connected to V_{DD}, the oscillator output OSC is switched to a high-impedance state allowing to feed an external clock signal to OSC.

9. Characteristics of the I²C bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signal (see Figure 11).

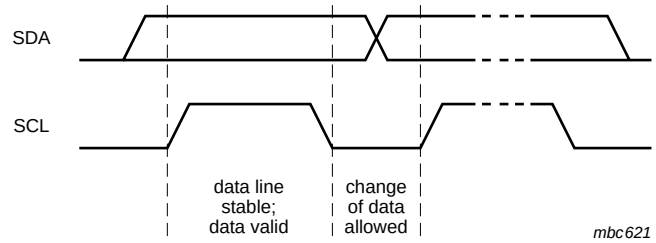


Fig 11. Bit transfer

9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 12).

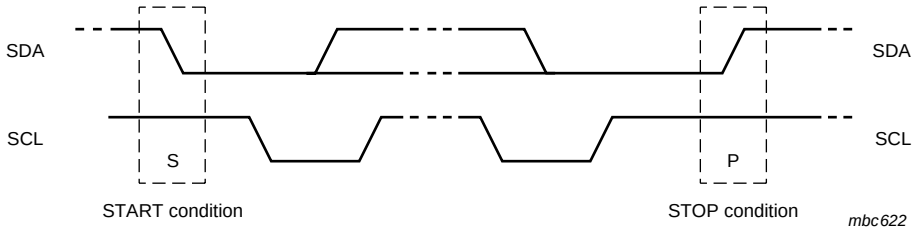


Fig 12. Definition of START and STOP conditions

9.3 System configuration

A device generating a message is a transmitter; a device receiving a message is a receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves (see Figure 13).

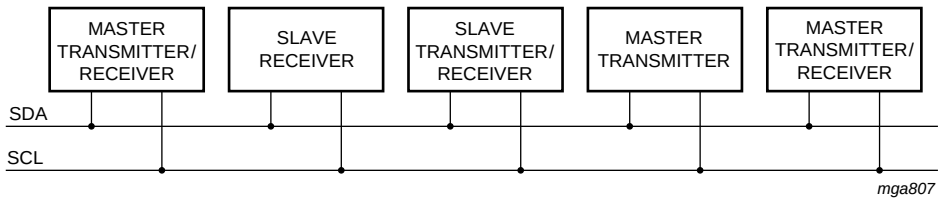


Fig 13. System configuration

9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered)
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition

Acknowledgement on the I²C-bus is shown in Figure 14.

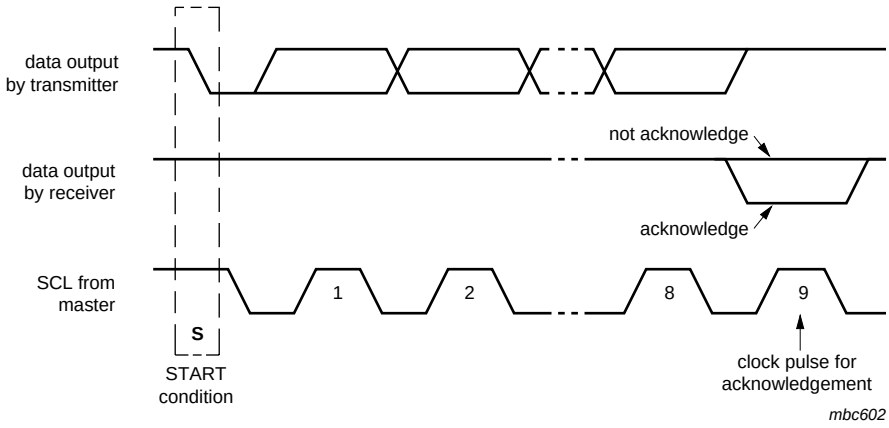


Fig 14. Acknowledgement on the I²C-bus

9.5 I²C bus protocol

After a START condition, the I²C slave address has to be sent to the PCF8591 device.

Eight different I²C-bus slave addresses can be used to address the PCF8591 (see Table 5).

Table 5. I²C slave address byte

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
slave address	1	0	0	1	A2	A1	A0	R/$\overline{W}$

The least significant bit of the slave address byte is bit R/$\overline{W}$ (see Table 6).

Table 6. R/$\overline{W}$-bit description

R/$\overline{W}$	Description
0	write data
1	read data

Bit 1 to bit 3 of the slave address are defined by connecting the input pins A0 to A2 to either V_{SS} (logic 0) or V_{DD} (logic 1). Therefore, eight instances of PCF8591 can be distinguished on the same I²C-bus.

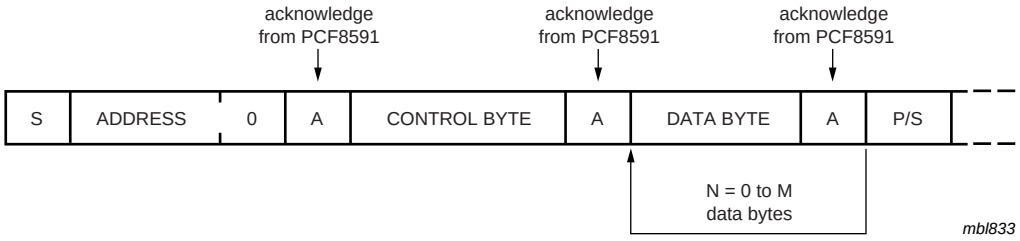


Fig 15. Bus protocol for write mode, D/A conversion

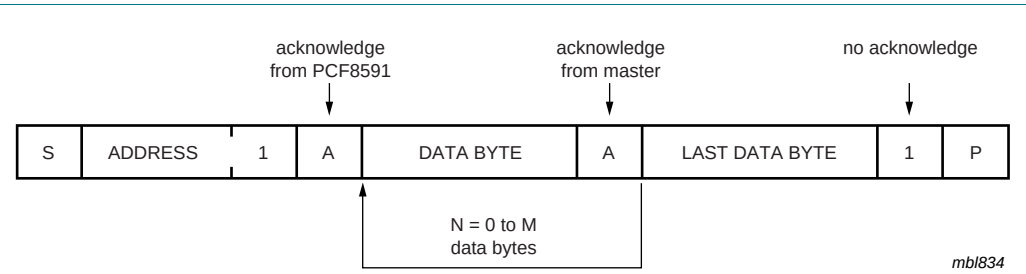


Fig 16. Bus protocol for read mode, A/D conversion

10. Application design-in information

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analog inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize crosstalk of the digital to analog signal paths the printed-circuit board layout must be very carefully designed. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (>10 μF) are recommended for power supply and reference voltage inputs.

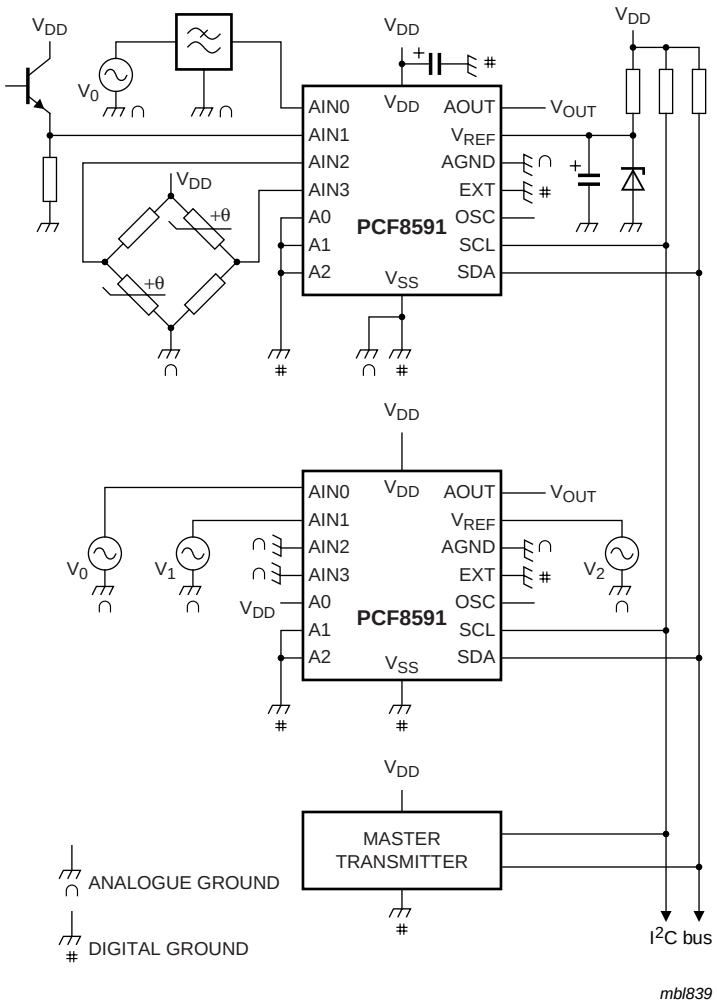


Fig 17. Application diagram