Response to Editors and Reviewers

Paper Title: Low-complexity, Multi Sub-band Digital Predistortion: Novel Algorithms and SDR Verification
Authors: Chance Tarver, Mahmoud Abdelaziz, Lauri Anttila, Mikko Valkama, Joseph R. Cavallaro
Manuscript ID: VLSI-D-17-00269

Dear editors and anonymous reviewers,

This revised manuscript entitled "Low-complexity, Multi Sub-band Digital Predistortion: Novel Algorithms and SDR Verification" is a revised version of the manuscript VLSI-D-17-00269. Thank you reviewers and editors for the time and effort spent on our paper. We appreciate the thoughtful comments. We have responded to these comments one by one in this letter. We have also updated the manuscript accordingly including, e.g., a block diagram. All bigger major to the manuscript are written in red font while other, smaller-scale additions and corrections of typos have been implemented.

Sincerely,

Chance Tarver, Mahmoud Abdelaziz, Lauri Anttila, Mikko Valkama, Joseph R. Cavallaro

Houston, TX; Tampere, Finland; August 16, 2017

1 Response to Reviewer 1

Reviewer overview: *An extension of the DPD solution in [15, 20] was proposed in [21], where an iterative learning algorithm is used between the right and left IM3 sub-bands until they are both properly suppressed. (Better to have numbers based on frequencies F1/F2/2F1-F2/2F2-F1)*

Response:

Comment 1: *The Intermodulation/ACP is also depend on the PAR and the peaks from the Waveforms. I don't see term like PAR/Peak/CFR.*

Response:

Comment 2: *IMD/Intermodulation's/Third order non-linearities are mixes, may be reduce the complexity and stick to one of them.*

Response:

Comment 3: *The DPD curve achieved through the PA feedback path, nothing mentioned in the Document.*

Response:

Comment 4: *Nothing mentioned about currents and Efficiency. Document Missing technical terms. could be better if we add top level block diagram.*

Response:

2 Response to Reviewer 2

Comment 1: *The first concern is on the iterative processing method. Yes, this method can guarantee better performance. But, how to evaluate the increased latency?*

Response:

Comment 2: *It is mentioned that the learning is based on the serial processing manner for hardware complexity consideration. However, this will further increase the latency.*

Response:

Comment 3: *For the convergence speed up, both adaption and on-the-fly storage are adopted. However, both methods will introduce complexity. Authors should comment on the balance of performance and complexity.*

Response:

Comment 4: *It is good the design is implemented by WarpLab. It would be better if the authors can compare this.*

Response:

Comment 5: *It is not suggested to have Figure 2 occupy the entire page.*

Response: