CertusPro-NX Hardware Checklist

Technical Note

FPGA-TN-02255-1.5

May 2025

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
BGA	Ball Grid Array
CML	Current-Mode Logic
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling

1. Introduction

When designing complex hardware using the CertusPro™-NX device, you must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the CertusPro-NX device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The device family consists of FPGA densities ranging from 50k to 100k Logic Cells. This technical note assumes that the reader is familiar with the CertusPro-NX device features as described in CertusPro-NX Family Data Sheet (FPGA-DS-02086). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Refer to CertusPro-NX Family Data Sheet (FPGA-DS-02086) for details. The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the CertusPro-NX power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: You should refer to the following documents for detailed recommendations.

- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244)
- Thermal Management (FPGA-TN-02044)
- sysDSP Block User Guide for Nexus Platform (FPGA-TN-02096)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02148)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02150)
- LatticeSC™ SERDES Jitter (TN1084)
- HSPICE SERDES simulation package (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- Related pinout information can be found on the CertusPro-NX web page.
- ADC User Guide for Nexus Platform (FPGA-TN-02129)

2. Power Supplies

The V_{CC}, V_{CCAUXA}, and V_{CCIOx} power supplies are monitored to determine the CertusPro-NX internal Power Good condition during power-up. These supplies need to be at a valid and stable level before the device becomes operational. All other supplies are not monitored during power-up, but need to be at valid and stable level before the device configuration is complete and enters into User Mode. Several other supplies are used in conjunction with onboard SERDES Blocks and ADCs on CertusPro-NX devices.

Table 2.1 describes the power supplies and the appropriate voltage levels for each supply.

Table 2.1. Single-Ended I/O Standards

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.0 V	FPGA core power supply. Required for Power Good condition.
V_{CCECLK}	1.0 V	FPGA core clock power supply. Required for Power Good condition.
V_{CCAUX}	1.8 V	Auxiliary power supply pin for I/O Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7. Used for generating stable drive current for the I/O.
$V_{CCAUXHx}$	1.8 V	Auxiliary power supply pin for I/O Bank 3, Bank 4, and Bank 5. Used for generating stable current for the differential input comparators and stable drive current for the I/O.
V_{CCAUXA}	1.8 V	Auxiliary Supply Voltage for internal analog circuitry. Required for Power Good condition.
$V_{CCIO[7:0]}$	Banks 0, 1, 2, 6, 7: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 3, 4, 5: 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.	Bank I/O Driver Supply Voltage. Each bank has its own V_{CCIO} supply: V_{CCIO0} and V_{CCIO1} are used in conjunction with pins dedicated and shared with device configuration, and are required to reach a proper level for Power Good condition.
$V_{CCADC18}$	1.8 V	ADC Block power supply. Should be isolated from excessive noise.
ADC_REFP[1:0]	1.0 V to 1.8 V Typical	ADC External Reference. Should be isolated from excessive noise and have high accuracy (< 0.1%).
V_{CCSDx}	1.0 V	SERDES Block Core power supply voltage. Should be isolated from excessive noise.
V_{CCSDCK}	1.0 V	SERDES Block Clock buffer supply voltage. Should be isolated from excessive noise.
$V_{CCPLLSDx}$	1.8 V	SERDES Block PLL power supply voltage. Should be isolated from excessive noise.
$V_{CCAUXSDQx}$	1.8 V	SERDES Block Auxiliary power supply voltage. Should be isolated from excessive noise.

The CertusPro-NX FPGA device has a power-on-reset state machine that depends on several of the power supplies.

These supplies should come up monotonically. Initialization of the device does not proceed until all monitored power supplies have reached their minimum operating voltages.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noises.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to regulator's feedback pin which sets regulator's output voltage.
- Expected voltage drops due to power filtering ferrite bead's ESR * expected current draw.
- Expected voltage drops due to current measuring resistor's ESR * expected current draw.

With 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.0 V rail is especially sensitive to noise as every 10 mV is 1% of the rail voltage. For SERDES differential power rails, it is recommended to target a maximum 1% peak noise. For PLLs, target less than 0.25% peak noise.

3. CertusPro-NX SERDES and ADC Power Supplies

There are supplies dedicated to the operation of the CertusPro-NX SERDES Blocks and ADCs. These supplies are also paired with dedicated ground pins. Providing a quiet supply is critical for these blocks. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins with short traces to keep inductance low.

For the best jitter performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB related crosstalk to sensitive blocks is related to FPGA outputs located in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}, V_{CCECLK}	10 µF x 2 + 100 nF per pin	Core and clock logic. Tie V_{CC} and V_{CCECLK} pins together. 1.0 V
V_{CCAUX}, $V_{CCAUXHx}$ (Single Ended)	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pins. Tie together V_{CCAUX} pins with $V_{CCAUXHx}$ pins for banks without high-speed differential pair I/O. 1.8 V
$V_{CCAUXHx}$ (Fast Differential)	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pin for I/O Bank 3, Bank 4, and Bank 5. Use separate FB + Capacitor filter for banks with high-speed differential I/O. 1.8 V
V_{CCAUXA}	120 Ω FB + 10 µF + 100 nF per pin	Auxiliary power supply pin for internal analog circuitry 1.8 V
$V_{CCIO[7:0]}$	10 µF + 100 nF per pin	Bank I/O. Unused banks can replace the 10 µF with a 1.0 µF. For banks with lots of outputs or large capacitive loading replace the 10 µF with a 22 µF (or add one additional 10 µF). Banks 0, 1, 2, 6, 7 = 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V. Banks 3, 4, 5 = 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V.
$V_{CCADC18}$	220 Ω or 120 Ω FB + 10 µF + 100 nF per pin	ADC Block. If ADC Block not used, leave open. 1.8 V
ADC_REFP[1:0]	220 Ω or 120 Ω FB + 1.0 µF + 100 nF per pin	ADC Block External Reference. Must have extremely low noise and high accuracy (< 0.1%). Voltage source/regulator should be filtered by 220 Ω or 120 Ω FB + 1 µF If ADC Block not used, leave open. 1.0 V to 1.8 V Typical
V_{CCSDx}	120 Ω FB + 10 µF + 100 nF per pin	SERDES Block Core. If SERDES Block not used, leave open. 1.0 V
V_{CCSDCK}	120 Ω FB + 10 µF + 100 nF per pin	SERDES Block Clock buffer. If both SERDES Blocks are not used, leave open. 1.0 V

Power Input	Recommended Filter	Notes
$V_{CCPLLSDx}$	220 Ω FB + 47 µF + 470 nF per pin IMPORTANT: Connect capacitor grounds only to FPGA pin SDx_REFRET	SERDES Block PLL. If SERDES Block not used, leave open. Bypass capacitor grounds go only to SDx_REFRET 1.8 V
$V_{CCAUXSDQx}$	120 Ω FB + (10 µF and 100 nF to each channel's SDx_REFRET)	SERDES Block Auxiliary. If SERDES Block not used, leave open. Bypass capacitor grounds go only to SDx_REFRET 1.8 V

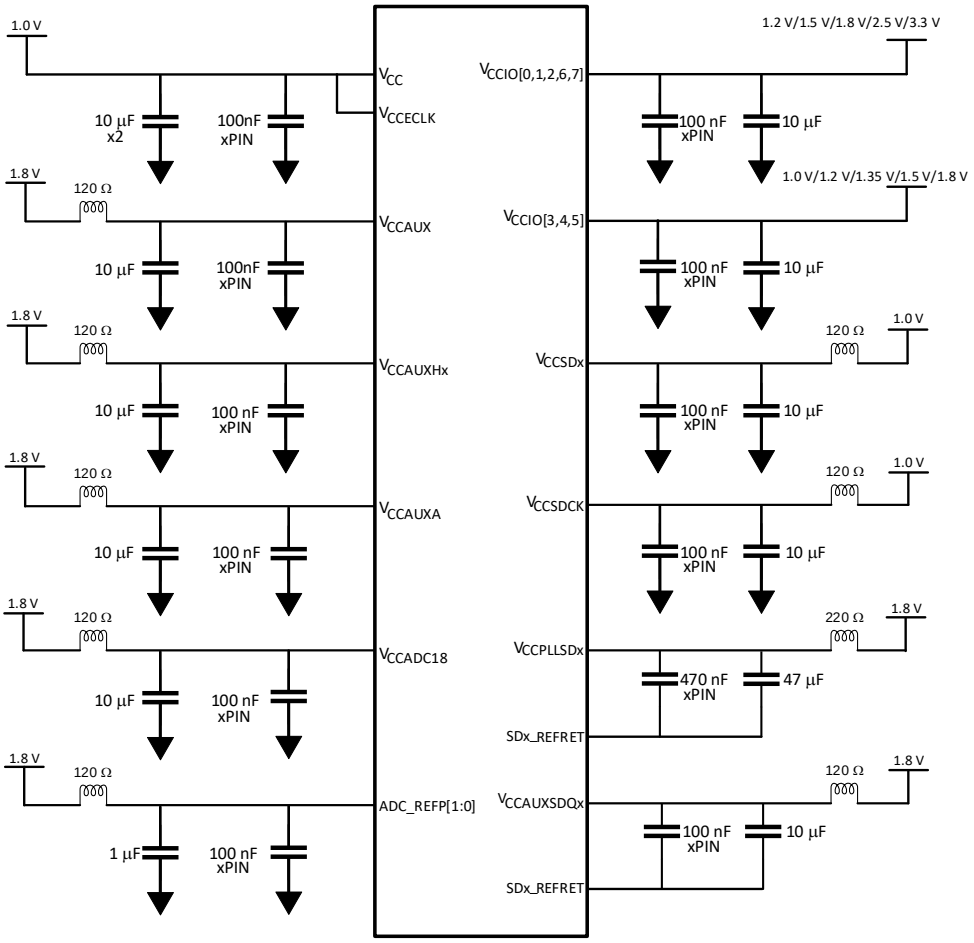


Figure 3.1. Recommended Power Filters

3.2. Ferrite Bead Selection Notes

- Most designs work well using ferrite beads between 120 Ω at 100 MHz and 240 Ω at 100 MHz.
- Ferrite bead induced noise voltage from ESR × CURRENT should be < 1% of rail voltage for non-analog rails and < 0.25% for sensitive rails.
- Non-PLL rails should use ferrite beads with ESR between 0.025 Ω and 0.10 Ω depending on current load.
- PLL rails are low current which allow ferrite beads with ESR ≤ 0.3 Ω.
- Small package size ferrite beads have higher ESR than large package size ferrite beads of same impedance.
- High impedance ferrite beads have higher ESR than low impedance ferrite beads in the same package size.

3.3. Ground Pins

- All ground pins need to be connected to the board's ground plane.
- V_{SSSDx} and V_{SSADC} pins are sensitive to noise and should be isolated from fast switching high current pathways on the ground plane. Ground plane islands can be used to help isolate sensitive grounds from noisy ground areas. The ground plane islands must connect at only one location to the main ground plane. Connection locations should be at least 2 mm wide. Only signals in the same domain as the ground plane island should be referenced to that island.
- SDx_REFRET — Input SERDES Reference Return Input. This pin should be AC coupled (bypassed) to the $V_{CCPLLSDx}$ supply.

3.4. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA from, for example, a single-ended or differential clock oscillator, proper power supply isolation and decoupling of the clock oscillator is recommended.

When specifying components, choose good quality ceramic capacitors in small packages, and place them as close to the clock oscillator supply pins as practically possible. *Good quality* capacitors for bypassing generally meet the following requirements:

3.5. Capacitor Selection

When specifying components, choose good quality ceramic capacitors in small packages, and place them as close to the power supply pins as practically possible. Good quality capacitors for bypassing generally meet the requirements discussed in the following sections.

3.5.1. Dielectric

Use dielectrics such as X5R, X7R and similar which have good capacitance tolerance (≤ ±20%) over temperature range. Avoid Y5V, Z5U and similarly poor capacitance-controlled dielectrics.

3.5.2. Voltage Rating

Capacitor working capacitance decreases non-linearly with higher voltage bias. To maintain capacitance, the capacitor voltage rating should target at least 80% higher than the voltage rail (maximum). For example, 3.3 V rail bypass capacitors should use the commonly available 6.3 V rating as a minimum.

3.5.3. Size

Smaller body capacitors have lower inductance, work to higher frequencies, and improve board layout. For a given voltage rating, smaller body capacitors tend to cost more than larger body capacitors. Optimizing between market pricing and size related inductance, the following capacitor sizes are recommended:

Table 3.2. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF	0201	0402
1.0 µF, 2.2 µF	0402	0603
4.7 µF	0603	0402
10 µF	0603	0805
22 µF	0805	1206

3.6. Unused Bank V_{CCIOx}

Connect unused V_{CCIO} pins to a power rail. Do not leave them open.

3.7. Unused ADC Blocks

Connect V_{SSADC}, ADC_REFx, ADC_DPx, and ADC_DNx pins to board ground. Leave $V_{CCADC18}$ floating (not connected).

3.8. Unused SERDES Quads

- Connect to board ground V_{SSSDQ}, and the Rx differential inputs, SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REFRET.
- Leave $V_{CCAUXSDQx}$ [x=0,1], V_{CCSDx} [x= 0-7], $V_{CCPLLSDx}$ [x = 0-7], SDx_REXT, and Tx differential pair outputs open.
- If both SERDES Quads are not in use, leave V_{CCSDCK} open.

3.9. Unused SERDES Channels in a Quad

- Connect all V_{SSSDQ} pins to board ground.
- Channel 1 of the used quad must be supplied with filtered power, regardless of whether it is in use. Connect $V_{CCAUXSDQx}$ [x=0,1], V_{CCSDx} [x= 1,5], and $V_{CCPLLSDx}$ [x = 1,5] pins to filtered power rails.
- Connect to board ground the Rx differential inputs, SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REFRET.
- Leave V_{CCSDx} [x= 0-7], $V_{CCPLLSDx}$ [x = 0-7], SDx_REXT, and Tx differential pair outputs open.

4. Power Sequencing

There is no power up sequence required for the CertusPro-NX device.

5. Power Estimation

Once the CertusPro-NX device density, package, and logic implementation is decided, power estimation for the system environment should be determined based on the Power Calculator provided as part of the Lattice Radiant™ design tool. When estimating power, the designer should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current and maximum DC and AC current for the given system environmental conditions.
- The ability for the system environment and CertusPro-NX device packaging to be able to support the specified maximum operating junction temperature.

By determining these two criteria, the CertusPro-NX device power requirements can be taken into consideration early in the design phase.

6. Configuration Considerations

PCB layout design and breakout suggestions are outlined in PCB Layout Recommendations for BGA Packages (FPGA-TN-02024). WLCSP packages are similar to other BGA (ball grid array) packages with regard to the PCBs the packages are to be mounted on. For application-specific assembly guidance, consult the design guidelines of the assembly service provider.

The CertusPro-NX device includes provisions to configure the FPGA via the JTAG interface or several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations.

Table 6.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI/SI	4.7 kΩ pull-up to V_{CCIO1}
TMS/SCSN	4.7 kΩ pull-up to V_{CCIO1}
TDO/SO	4.7 kΩ pull-up to V_{CCIO1}
TCK/SCLK	2.2 kΩ pull-down to GND

Every PCB is recommended to have easy access to FPGA JTAG pins, even if the primary configuration interface is not using the JTAG port. This JTAG port enables debugging in the final system. For best results, route the TCK, TMS, TDI, and TDO signals to a common test header along with V_{CCIO1} and ground.

External resistors are necessary on configuration signals if they are used to handshake with other devices. Recommended pull-up resistors to the appropriate bank V_{CCIO} and pull-down to board ground should be used on the pins in Table 6.2. External pull-resistors are not necessary on individual configuration pins when the signal pin is not persisted.

Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	4.7 kΩ pull-up to V_{CCIO0}
INITN	4.7 kΩ pull-up to V_{CCIO0}
DONE	4.7 kΩ pull-up to V_{CCIO0}
MCLK	1.0 kΩ to GND (Not installed by default) 1.0 kΩ to V_{CCIO0} (Not installed by default)
MCSN	4.7 kΩ pull-up to V_{CCIO0}
JTAG_EN	4.7 kΩ pull-down to GND (JTAG port disabled) or 1.0 kΩ pull-up to V_{CCIO1} (JTAG port enabled)
TMS/SCSN	4.7 kΩ pull-up to V_{CCIO1}
SCL/SDA[1]	1.0 kΩ to 4.7 kΩ pull-up to V_{CCIO1}

Note:

1. Pull-up resistors are not required in Target I3C configuration mode.

Table 6.3. Configuration Pins Needed per Programming Mode[2]

Configuration Mode	Bank	Enablement	Clock		Bus Size	Pins
			Pin	I/O		
MSPI	0	(Default)	MCLK	Output	1	MCLK, MCSN, MOSI, MISO
					2	MCLK, MCSN, MD0, MD1
					4	MCLK, MCSN, MD0, MD1, MD2, MD3
JTAG	1	JTAG_EN pin[1]	TCLK	Input	1	TCK, TMS, TDI, TDO
SSPI	1	Activation key[1]	SCLK	Input	1	SCLK, SCSN, SI, SO
					2	SCLK, SCSN, SD0, SD1
					4	SCLK, SCSN, SD0, SD1, SD2, SD3
I2C/I3C	1	Activation key	SCL	Input	1	SCL, SDA

Notes:

1. JTAG and SSPI ports share pins. When JTAG_EN is asserted, the JTAG port takes precedence over SSPI.
2. Leave unused configuration ports open.

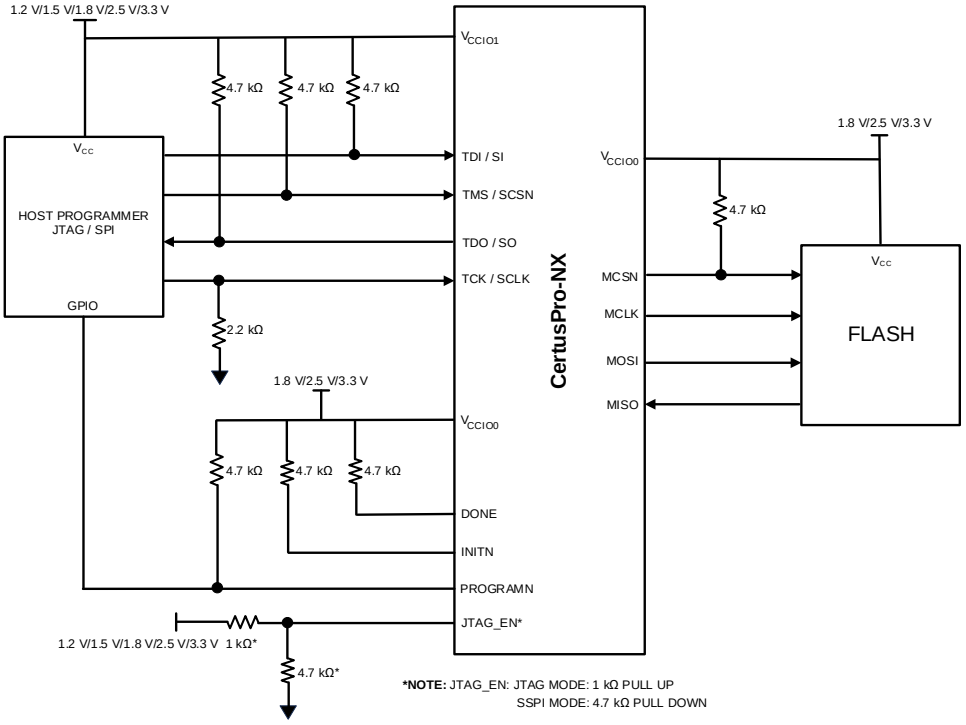


Figure 6.1. Typical Connections for Programming SRAM or External Flash via JTAG/SSPI

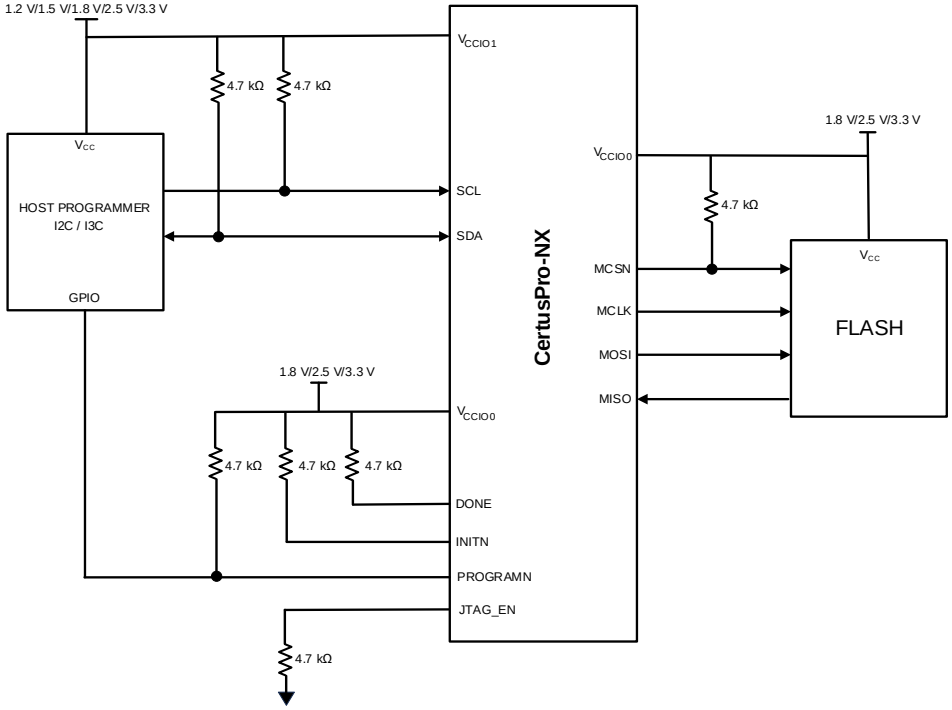


Figure 6.2. Typical Connections for Programming SRAM via I2C/I3C

Some architectures require Bank 0 and Bank 1 to have different bank voltages. One such architecture is illustrated in Figure 6.3. In the event a control signal, such as PROGRAMN, originates in one voltage domain but is terminated in another, a voltage translating device or circuit must be implemented to reduce excess current leakage or possible device damage. Figure 6.3 shows a voltage translator utilized for PROGRAMN, allowing a 3.3 V driver to drive the 1.8 V bank 0 input buffer safely and efficiently.

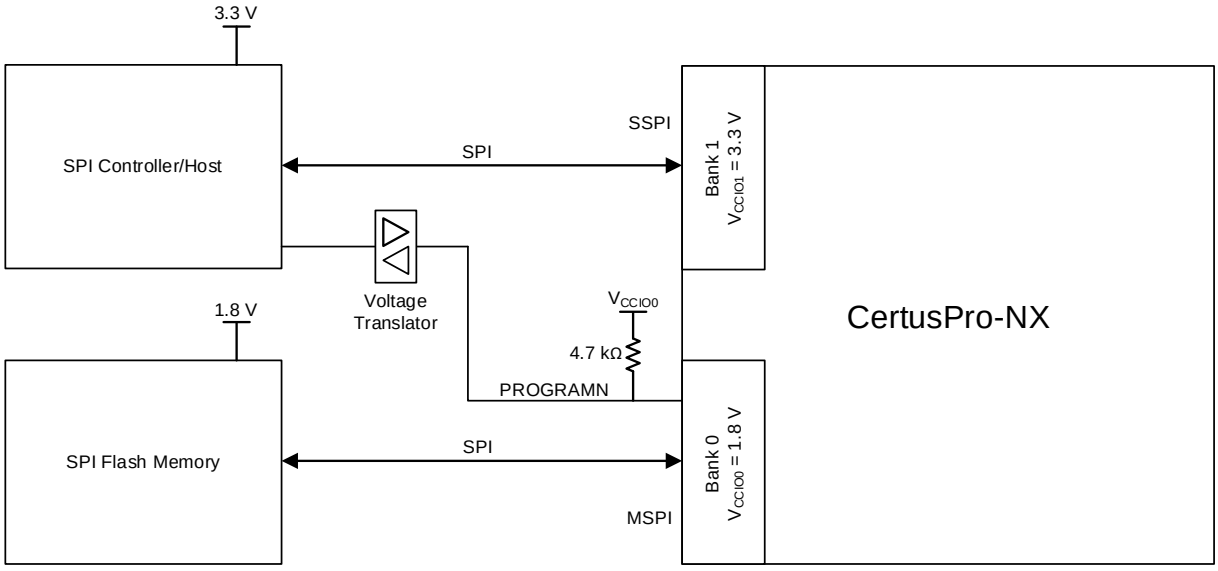


Figure 6.3. Accommodation for Mixed Voltage Across Configuration Banks

7. External SPI Flash

The Flash Voltage should match the V_{CCIO0} voltage.

It is recommended to use an SPI flash device that is supported in the Radiant Programmer. To see the list of supported devices, go to the Radiant Programmer; under the Help menu, choose Help, then search for SPI Flash support.

For a list of SPI Flash devices that are not supported by SPI Flash, use the custom flash option to make the non-supported devices work.

8. I/O Pin Assignments

Assembly and rework parameters for WLCSP packages are similar to other BGA packages. Refer to Solder Reflow Guide for Surface Mount Devices (FPGA-TN-02041), which outlines the reflow parameters for all the various package styles offered, including WLCSP.

The V_{CCSDCK}, $V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ provide *quiet* supplies for the SERDES blocks. For the best jitter performance, careful pin assignment keeps *noisy* I/O pins away from *sensitive* pins. The leading causes of PCB related SERDES crosstalk is related to FPGA outputs located in close proximity to the sensitive SERDES power supplies. These supplies require cautious board layout to insure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies; however, robust PCB layout is required to insure that noise does not infiltrate into these analog supplies.

Although crosstalk generated coupling has been reduced in the device packages of CertusPro-NX devices, the PCB board can cause significant noise injection from any I/O pin adjacent to SERDES data, reference clock, and power pins as well as other critical I/O pins such as clock signals. Electrical Recommendations for Lattice SERDES (FPGA-TN-02077) provides detailed guidelines for optimizing the hardware to reduce the likelihood of crosstalk to the analog supplies. PCB traces running in parallel for long distances need careful analysis. Simulate any suspicious traces using a PCB crosstalk simulation tool to determine if they cause problems.

It is common practice for designers to select pinouts for their system early in the design cycle. For the FPGA designer, this requires a detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/O. Lattice Semiconductor provides detailed pinout information that can be downloaded from the Lattice Semiconductor website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, you can gather the pinout details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

9. sys I/O

The CertusPro-NX provides the flexibility to configure each I/O according to user requirement. These pins can be configured as input, output, and tri-state. Additionally, attributes such as PULLMODE, CLAMP, HYSTERESIS, VREF, OPENDRAIN, SLEWRATE, DIFFRESISTOR, TERMINATION, and DRIVE STRENGTH can also be setup.

For the PULLMODE, Pull-up and Pull-down resistors can be set. The implementation of these resistor is by using a constant current that have the following values:

Table 9.1. Weak Pull Up/Down Current Specifications

	Parameter	Condition	Min	Max	Unit
Pull-Up	I/O weak pull-up resistor current	$0 \le V_{IN} \le 0.7 \times V_{CCIO}$	-30	-150	µA
Pull-Down	I/O weak pull-down resistor current	V_{IL} (max) $\le V_{IN} \le V_{CCIO}$	30	150	µA

The CertusPro-NX also provides special I/Os like, HPIO and WRIO that can be used for High-Speed communication. Figure 9.1 shows the block diagram for HPIO and Figure 9.2 shows the block diagram for WRIO.

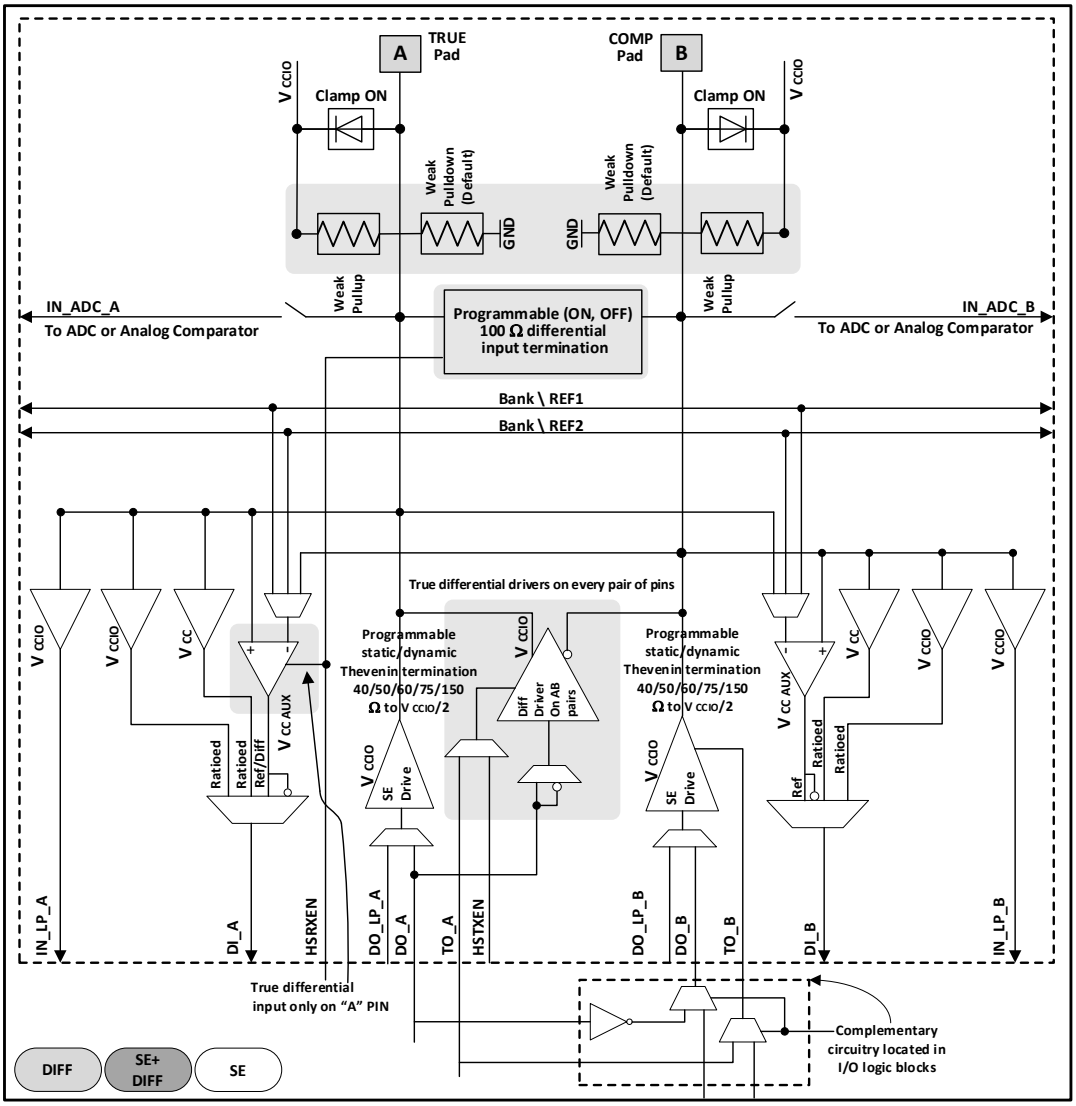


Figure 9.1. High Performance sysI/O Buffer Pair for Bottom Side

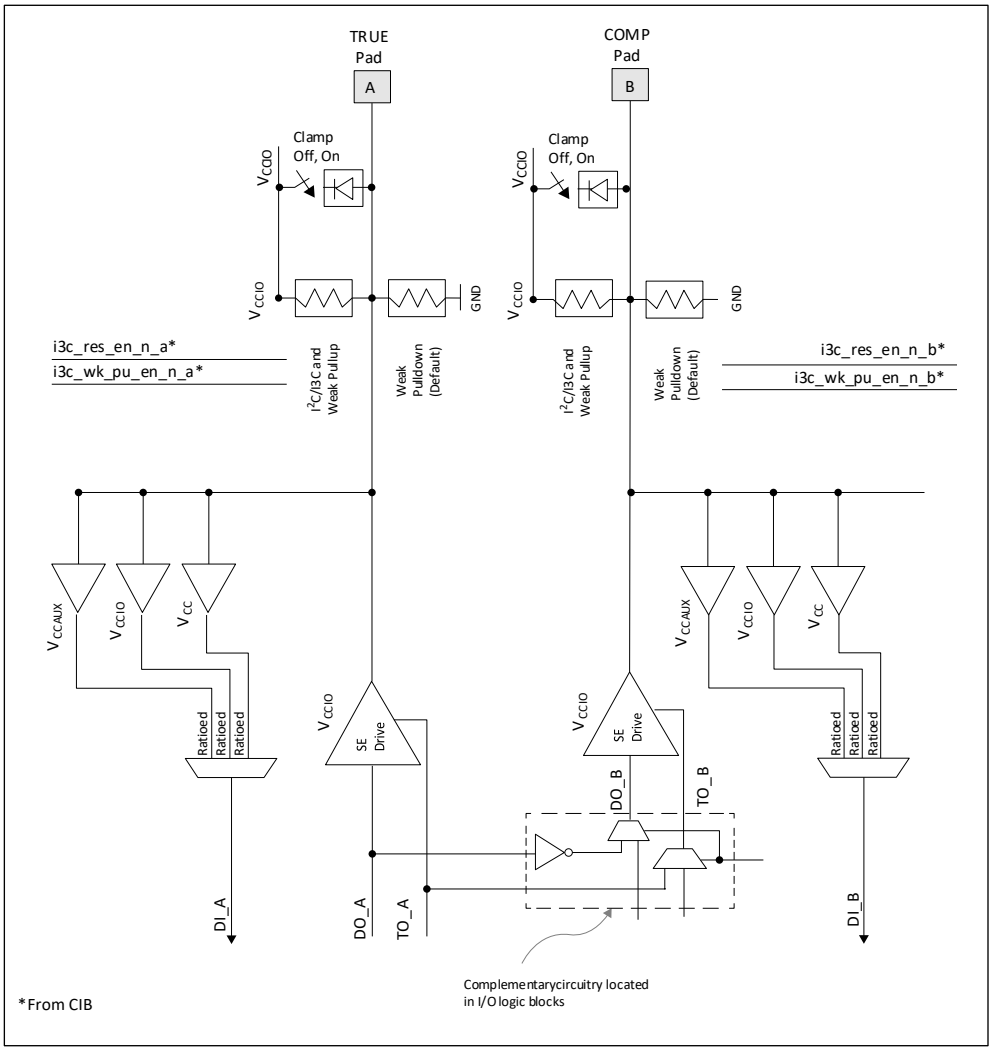


Figure 9.2. Wide Range sysI/O Buffer for Top, Left/Right Side

10. Clock Inputs

The CertusPro-NX device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for General Purpose I/O.

When these pins are used for clocking purpose, you need to pay attention to minimize signal noise on these pins. Refer to CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244).

These shared clock input pins, typically named GPLL and PCLK, can be found under the Dual Function column of the pinlist.csv file.

High-speed differential interfaces (such as MIPI) being received by the FPGA must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (-complement).

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. Good power supply decoupling of the clock oscillator is required to reduce clock jitter. A typical bypassing circuit is shown in Figure 10.1.

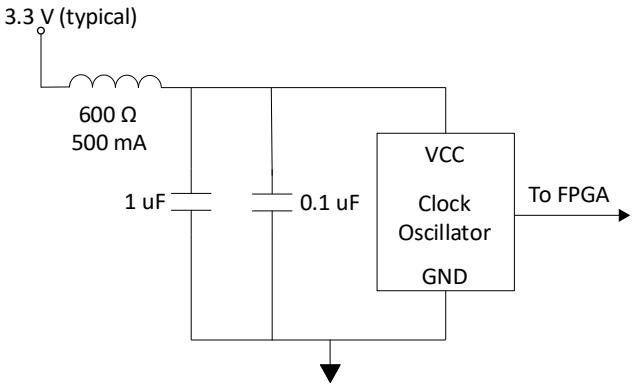


Figure 10.1. Clock Oscillator Bypassing

For differential clock inputs to banks with V_{CCIO} voltage of 1.5 V and lower it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO}. An LVDS oscillator can also be used if AC coupled and then DC biased at half the V_{CCIO} voltage. Example dual footprint design supporting HCSL and LVDS shown below in Figure 10.2.

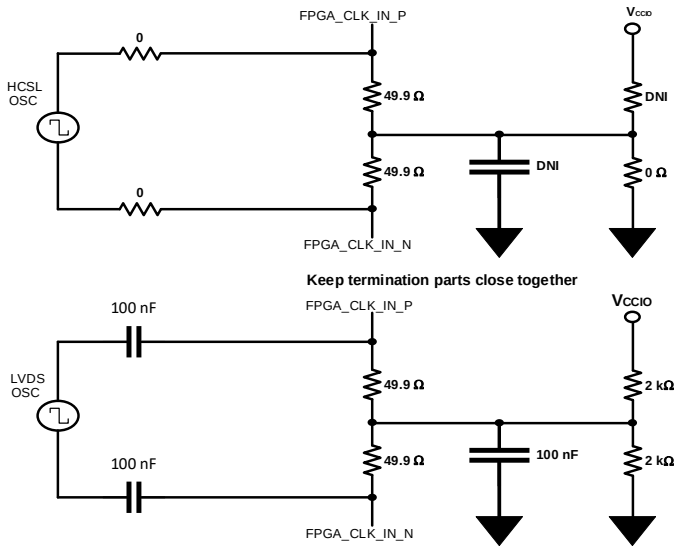


Figure 10.2. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

11. Pinout Considerations

The CertusPro-NX device supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design on these high-speed interfaces. The pinout selection must be completed with an understanding of the interface building blocks implemented in the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL and DLL usage. Refer to CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244) for rules pertaining to these interface types.

12. LVDS Pin Assignments

True LVDS inputs and outputs are available on I/O pins on the device bottom banks 3, 4, and 5 only . Top, left, and right side I/O banks do not support True LVDS standard, but can support emulated LVDS outputs. True LVDS input pairing on bottom banks can be found under the High-Speed column in the pinlist.csv file.

Emulated LVDS output are available on pairs around all banks, but this requires external termination resistors. This is described in sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067).

13. HSUL, SSTL and LVSTL Pin Assignments

The HSUL , SSTL and LVSTL interfaces are referenced I/O standards require an external reference voltage. HSUL, SSTL and LVSTL are supported on the device bottom banks 3, 4, and 5 only. The V_{REF} pin(s) should get high priority when assigning pins on the PCB. These pins can be found in the Dual Function column with V_{REF} label. Each bank includes a separate V_{REF} voltage. V_{REF} sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank supply and reference voltages.

14. DPHY and SERDES Pin Considerations

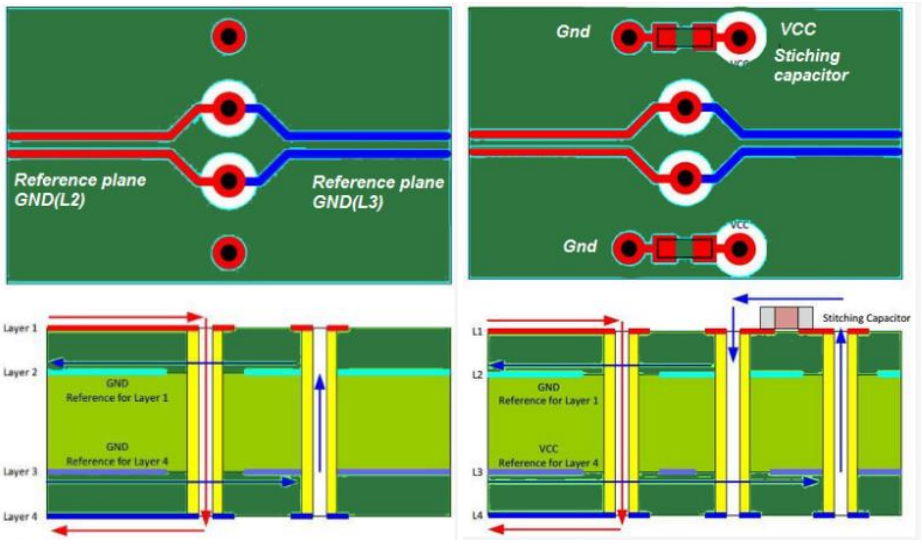
High-speed signaling requires careful PCB design. Maintaining good transmission line characteristics is a requirement. A continuous ground reference should be maintained with high-speed routing. This includes tightly length matched differential routing (no larger than ±4 mil length mismatch) with very few discontinuities.

The DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree. Refer to High-Speed PCB Design Considerations (FPGA-TN-02178) for suggested methods and guidance.

15. Layout Recommendations

A good design from a schematic should also reflect a good layout for the system design to work without any issues with noise or power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes; this is to ensure good power delivery and thermal stability.
2. Each power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. The placement of analog circuits must be away from digital circuits or high-switching components.
4. High-speed signals should have a clearance of five times the trace width of other signals.
5. High-speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are grounded. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}).



6. High-speed signals have a corresponding impedance requirement; calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with the PCB vendor.
7. For differential pairs, be sure to match the length as closely as possible. A good rule of thumb is to match up to ±5mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

16. Checklist

Table 16.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	Core Supplies		
1.1.1	V_{CC} and V_{CCECLK} core at 1.0 V ±5%		
1.1.2	Use a PCB plane for V_{CC} core with proper decoupling		
1.1.3	V_{CC} and V_{CCECLK} core sized to meet power requirement calculation from software		
1.1.4	V_{CCAUX}, $V_{CCAUXHx}$, and V_{CCAUXA} at 1.8 V –3%/+5%		
1.1.5	V_{CCAUX}, $V_{CCAUXHx}$, and V_{CCAUXA} Must be *quiet* and isolated from other switching noises.		
1.1.6	V_{CCAUX} pins and $V_{CCAUXHx}$ pins for banks without high-speed differential pair I/O ganged together. Solid PCB plane is recommended.		
1.1.7	$V_{CCAUXHx}$ banks with high-speed differential pair I/O should use separate FB + Capacitor filter. Solid PCB plane is recommended.		
1.1.8	V_{CCAUXA} pins should be ganged together, and a solid PCB plane is recommended.		
1.2	I/O Supplies		
1.2.1	All *Wide Range* V_{CCIO} (Banks 0,1,2,6,7) are between 1.2 V to 3.3 V		
1.2.2	All *High Performance* (Bank 3,4,5) V_{CCIO} are between 1.0 V to 1.8 V		
1.2.3	All Configuration V_{CCIO} (Banks 0,1), when used with configuration interfaces (for example, memory devices), need to match specifications.		
1.2.4	$V_{CCIO[7:2]}$ used based on user design		
1.3	ADC power supplies		
1.3.1	$V_{CCADC18}$ is 1.8 V +5%		
1.3.2	$V_{CCADC18}$ *quiet* and *isolated*		
1.4	SERDES Power Supplies		
1.4.1	V_{CCSDx} and V_{CCSDCK} are at 1.0 V ±5%		
1.4.2	V_{CCSDx} and V_{CCSDCK} *quiet* and *isolated* from each other and other 1.0 V supplies		
1.4.3	$V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ are 1.8 V +5%		
1.4.4	$V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ *quiet* and *isolated* from each other and other 1.8 V supplies		
1.4.5	$V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ bypass capacitor grounds go only to SDx_REFRET		
2	**JTAG**		
2.1	Pull-up or Pull-down on JTAG_EN, per Table 6.2.		
2.2	Keep JTAG_EN accessible on PCB to recover JTAG port, especially during development.		
2.3	Keep JTAG port pins accessible on PCB, especially during development		
2.4	Pull-down on TCK per Table 6.1.		
2.5	Pull-up on TMS, TDI, and TDO per Table 6.1.		
3	**Configuration**		
3.1	Pull-ups or pull-downs on persisted configuration specific pins per Table 6.1 and Table 6.2		
3.2	V_{CCIO0}, V_{CCIO1} bank voltage matches sysCONFIG peripheral devices such as SPI Flash		
4	**Special Pin Assignments**		
4.1	V_{REF} assignments followed for single-ended SSTL inputs		
4.2	Properly decouple the VREF source		

	Item	OK	NA
5	**Critical Pinout Selection**		
5.1	Pinout is chosen to address FPGA resource connections to I/O logic and clock resources per CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244).		
5.2	Shared general purpose I/O are used as inputs for FPGA PLL and Clock inputs.		
5.3	The DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree.		
6	**DDR3, DDR3L, LPDDR2, and LPDDR4 Interface Requirements**		
6.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
6.2	Maintain trace length matching to a maximum of ±20 mil between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
6.3	All data groups must reference a ground plane within the stack-up.		
6.4	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
6.5	Provide a separation of 3 W spacing between a data group and any other unrelated signals to avoid crosstalk issues. Use a minimum of 2 W spacing between all DDR traces excluding differential CK and DQS signals. (W is the minimum width of the signal trace allowed)		
6.6	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
6.7	Differential pair of DQS to DQS_N trace lengths should be matched to ±10 mil.		
6.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
6.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		
6.10	Address/control signals and the associated CK and CK_N differential FPGA clock should be routed with a control trace matching ±100 mil.		
6.11	CK to CK_N trace lengths must be matched to within ±10 mil.		
6.12	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		
6.13	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
6.14	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
6.15	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		
7	**External Flash**		
7.1	Flash voltage should match V_{CCIO0} voltage		
8	**SERDES**		
8.1	Dedicated reference clock input from clock source meets the DC and AC requirements		
8.2	External AC coupling caps may be required for compatibility to common-mode levels		
8.3	Ref clock termination resistors may be needed for compatible signaling levels		
8.4	Maintain good high-speed transmission line routing with at least 60 mil spacing to other signals		
8.5	Continuous ground reference plane to serial channels		
8.6	Tightly length matched differential traces, ±4 mils maximum		
8.7	Do not pass other signals on the PCB above or below the high-speed SERDES without isolation.		
8.8	Keep non- SERDES signal traces from passing above or below the V_{CCSDCK}, $V_{CCPLLSD0}$ and $V_{CCAUXSD}$ power plane without isolation.		
9	**ADC**		
9.1	When using ADC function, use the lower right corner PLL.		

References

For more information refer to:

- CertusPro-NX web page
- CertusPro-NX Family Data Sheet (FPGA-DS-02086)
- CertusPro-NX High-Speed I/O Interface (FPGA-TN-02244)
- sysCONFIG User Guide for Nexus Platform (FPGA-TN-02099)
- sysI/O User Guide for Nexus Platform (FPGA-TN-02067)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-02095)
- sysDSP Block User Guide for Nexus Platform (FPGA-TN-02096)
- Memory User Guide for Nexus Platform (FPGA-TN-02094)
- Thermal Management (FPGA-TN-02044)
- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- High-Speed PCB Design Considerations (FPGA-TN-02148)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02150)
- LatticeSC™ SERDES Jitter (TN1084)
- ADC User Guide for Nexus Platform (FPGA-TN-02129)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.5, May 2025

Section	Change Summary
All	• Minor editorial fixes. • Changed *SerDes* to *SERDES*.
Abbreviations in This Document	Replaced *Acronyms* with *Abbreviations*.

CertusPro-NX SerDes and ADC Power Supplies	• Changed paragraph style of the Unused SERDES Quads section.
	• Added the following to Unused SERDES Channels in a Quad section.
	  • Connect to board ground the Rx differential inputs, SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REFRET.
	  • Leave V_{CCSDx} [x= 0-7], $V_{CCPLLSDx}$ [x = 0-7], SDx_REXT, and Tx differential pair outputs open.

Revision 1.4, June 2024

Section	Change Summary
All	• Minor editorial fixes. • Changed *I²C to I2C*. • Changed *Master to Controller*. • Changed *Slave to Target*.
Inclusive Language	Added this section.
CertusPro-NX SerDes and ADC Power Supplies	• Updated the recommended filter of VCCPLLSDx *to 220 Ω FB + 47 µF + 470 nF per pin* in Table 3.1. Recommended Power Filtering Groups and Components. • Updated Figure 3.1. Recommended Power Filters to align with the changes of VCCPLLSDx in Table 3.1. Recommended Power Filtering Groups and Components.

Revision 1.3, April 2024

Section	Change Summary
All	Minor editorial fixes.
CertusPro-NX SerDes and ADC Power Supplies	Updated the Unused ADC Blocks to *Connect VSSADC, ADC_REFx, ADC_DPx, and ADC_DNx pins to board ground. Leave VCCADC18 floating (not connected)*.

Revision 1.2, January 2024

Section	Change Summary
Disclaimer	Updated this section.
Introduction	Added ADC User Guide for Nexus Platform (FPGA-TN-02129).
Power Supplies	Table 2.1. Single-Ended I/O Standards : Updated the nominal voltage value of ADC_REFP[1:0] from 1.2 V to 1.8 V Typical to *1.0 V to 1.8 V Typical*.

CertusPro-NX SerDes and ADC Power Supplies	• Table 3.1. Recommended Power Filtering Groups and Components:
	  • Updated the notes of ADC_REFP[1:0] from 1.2 V to 1.8 V Typical to *1.0 V to 1.8 V Typical.*
	  • Updated the notes of VCCSDCK from If SerDes Block not used, leave open, to *If both SerDes blocks are not used, leave open*.
	• Added Figure 3.1. Recommended Power Filters.
	• Added subsection 3.5 Capacitor Selection.
	• Removed Figure 3.2. Clock Oscillator Bypassing (formerly figure 3.1) under subsection Clock Oscillator Supply Filtering formerly subsection 3.4.
	• Update subsection 3.7 Unused ADC Blocks to: *Connect VSSADC pins to board ground. Leave VCCADC18 and ADC I/O floating (not connected)*.
	• Updated subsection 3.8 Unused SerDes Quads to: *Connect to board ground VSSSDQ, Rx*

Section	Change Summary
	Differential Inputs, SD_EXTx_RefCLKx, SDQx_RefCLKx, SDx_REFRET. Leave open VCCAUXSDQx [x=0,1], VCCSDx [x= 0-7], VCCPLLSDx [x = 0-7], SDx_REXT, and Tx Differential pair outputs. If both SerDes Quads are not used, then leave open VCCSDCK.
Configuration Considerations	• Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins: Updated MCLK pin to 1.0 kΩ to V_{CCIO0}. • Table 6.3. Configuration Pins Needed per Programming Mode2: Added note no.2 – Leave unused configuration ports open. • Added Figure 6.1. Typical Connections for Programming SRAM or External Flash via JTAG/SSPI and Figure 6.2. Typical Connections for Programming SRAM via I2C/I3C.
External SPI Flash	Added this main section.
sysI/O	Added this main section.
Clock Inputs	Reworked section contents.
Layout Recommendations	Added this main section.

Checklist	Added the following items:
	• No. 7 – External Flash
	  • No. 7.1. Flash voltage should match VCCIO0 voltage
	• No. 9 – ADC
	  • No. 9.1 When using ADC function, use the lower right corner PLL.

References	Added this section.

Revision 1.1, April 2023

Section	Change Summary
Checklist	Updated Table 13.1. Hardware Checklist to change row 6 from 'LPDDR3 and DDR3 Interface Requirements' to 'DDR3, DDR3L, LPDDR2, and LPDDR4 Interface Requirements'.
Technical Support Assistance	Added reference link to the Lattice Answer Database.

Revision 1.0, October 2022

Section	Change Summary
All	• Changing document status to Production Release. • Minor adjustments in formatting across the document.
Configuration Considerations	Updated Figure 6.1. Accommodation for Mixed Voltage Across Configuration Banks to change to CertusPro-NX.

Revision 0.83, June 2022

Section	Change Summary
All	Changed SERDES to SerDes across the document.
CertusPro-NX SerDes and ADC Power Supplies	• Added Unused SerDes Quads and Unused SerDes Channels in a Quad sections. • Updated SerDes power filtering for VCCPLLSDx and VCCAUXSDQx in Table 3.1. Recommended Power Filtering Groups and Components.
Configuration Considerations	Updated Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins to add 1.0 kΩ to V_{CCIO1} (not installed by default) for JTAG_EN.
Checklist	• Added $V_{CCPLLSDx}$ and $V_{CCAUXSDQx}$ bypass capacitor ground go only to SDx_REFRET. • Updated item 2.5 in JTAG group to change from TMS to TMS, TDI, and TDO.

Revision 0.82, February 2022

Section	Change Summary
DPHY and SerDes Pin Considerations	• Renamed section 12 SerDes Pin Considerations to DPHY and SerDes Pin Considerations. • Added a line to state that the DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree.
Checklist	Added a row in Table 13.1 to state that the DPHY clock input must use a PCLK pin so that it can be routed directly to the edge clock tree.

Revision 0.81, August 2021

Section	Change Summary
Configuration Considerations	Added note for Table 6.2. Pull-up/Pull-down Recommendations for Configuration Pins.

Revision 0.80, June 2021

Section	Change Summary
All	Preliminary release.

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