Intel® EP80579 Integrated Processor Product Line

Platform Design Guide

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Revision History

Date	Revision	Description
May 2010	005	• Updated Table 100, "Schematic Checklist" - changed Reserved20 pin on page 309 to require a Pulled Up to 3.3V to align with EP80579 External Design Specification.

Date	Revision	Description
June 2009	004	Defeatured LEB Mastering and removed external mastering descriptions related to this in Table 3, "EP80579 Feature List" and in Section 22.0, "Local Expansion Bus (LEB) Interface" Corrected ODT setting for single rank from ODT off to 75 ohms in Table 43, "Write Operation ODT Table" Changed the following signal names: • EX_REQ_GNT# to Reserved 19 • EX_SLAVE_CS# to Reserved 20 • EX_GNT_REQ# to NC57 • EX_WAIT# to NC58 • EX_WDTXFER to NC59 Corrected signal name: • SIU_CST1 to SIU_CST1# • SIU_CST2 to SIU_CST2# **Section 7.0, "Power Management and Reset Interface"** Section 7.4, "Power Sequencing" • Deleted Power Sequencing section. Refer to the *Intel® EP80579 Integrated Processor Product Line Datasheet*, Document Number 320066 for Power Sequencing Timing Diagrams. **Section 8.0, "Platform System Clock"** Section 8.2.1, "HOST_CLK Group" • Added statement to indicate that the Host_Clk_Group Topology and Routing guidelines apply to the routing of two separate 100MHz differential clocks from the CK410 Clock Synthesizer to EP80579 (CLKP100/CLKN100) and the ITP Port (BLKP/BCLKN) • Deleted intra-pair routing specification requirements from Table 18, "HOST_CLK Routing Guidelines" **Section 9.0, "System Memory Interface (DIMM)"** Table 46, "DDR2 Address/Command Signal Group Routing Guidelines" • Deleted the reference of Control (Ctrl) signals from the Routing Rules of CLK-to-CMD/ADD **Section 22.0, "Local Expansion Bus (LEB) Interface"** Added Section 22.2, "LEB Memory Size (LEB_SIZE) Strapping" **Section 25.0, "Sideband Signals"** Table 92, "Sideband Signals" • Changed pull-up resistor on CPURST# signal from 4.7K ohm to 10K ohm • Changed pull-up resistor on IERR# signal from 4.7K ohm to 10K ohm **Section 27.0, "Layout Checklist"** Table 97, "Layout Checklist" • Deleted intra-pair length matching requirements for the following signals: CLKP100/CLKN100 and BCLKP/BCLKN PEA0_Tp[7:0]/PEA0_Tn[7:0] PEA0_Rp[7:0]/PEA0_Rn[7:0] • Changed naming of GBEn_CLKOUT to GBEn_TxCLK • Changed naming of GBEn_CLKIN to GBEn_RxCLK • Changed Characteristic Impedance (Zo) for EX_CLK(CLK33) signal from 50-ohm to 55-ohm **Section 28.0, "Schematics Checklist"** Table 100, "Schematic Checklist" • GP27_IRQ39 - Updated power source to Suspend Power Well • GP33_IRQ33 - Changed backup to bootup for default configuration description • EX_ADDR[24:0] - Included description for strapping EX_ADDR[23:21] to determine LEB Memory Size (LEB_SIZE) • SPKR - Deleted external pull-up requirement on SPKR signal. Signal has a weak internal pull-down

Date	Revision	Description
November 2008	003	Section 7.0, "Power Management and Reset Interface" Updates: • Update to Figure 49 to indicate the delay between PWROK and VRMPWRGD to be 102ms instead of 12ms • Update to Figure 54 to connect GBE_AUX_PWR_GOOD to SYS_PWR_OK in systems without Sustain Power. Section 19.0, "Gigabit Ethernet (GbE) Interface" Updates: • Updates to Table 81, Table 82, and Table 83 to include WOL capability for GbE Port 0. Section 20.0, "IEEE 1588-2008 Hardware Assist Interface" Updates: • Termination of ASMSSIG and AMMSSIG signals changed from pull-ups to pull-down Section 28.0, "Schematics Checklist" Updates: • Updates to indicate signal terminations to Core and Suspend Power Wells • Termination of ASMSSIG and AMMSSIG (IEEE 1588-2008) signals changed from pull-ups to pull-downs.
September 2008	002	Chapter 9.0, "System Memory Interface (DIMM)". Updates to: • Table 27, "Supported DDR2 Device Densities and Widths" on page 111 • Table 28, "Supported DRAM Capacity for 64-bit Mode" on page 112 • Table 29, "Supported DRAM Capacity for 32-bit Mode" on page 112: Termination of unused DDR2 Data Bus Signals in 32-bit mode • Table 33, "256Mb Addressing" on page 114, Supported DDR2 memory addressing configurations • Table 34, "512Mb Addressing" on page 114, Supported DDR2 memory addressing configurations • Table 35, "1Gb Addressing" on page 115, Supported DDR2 memory addressing configurations • Table 36, "2Gb Addressing" on page 115, Supported DDR2 memory addressing configurations Chapter 25.0, "Sideband Signals". Added power-up deactivation pull-ups to sideband signals CPUSLP_OUT#, CPURST#, and IERR# Chapter 28.0, "Schematics Checklist". Termination updates for reserved pins and NC56. Appendix A, "System Memory Interface (SODIMM)". Updated Table A-2, "Supported SODIMM Memory Capacity for 64-bit Mode" on page 317. Appendix B, "System Memory Interface (Memory Down)". Updates to: • Table B-18, "Supported DRAM Capacity for 64-bit Mode" on page 334 • Table B-20, "256Mb Addressing" on page 335, supported DDR2 memory addressing configurations • Table B-21, "512Mb Addressing" on page 335, supported DDR2 memory addressing configurations • Table B-22, "1Gb Addressing" on page 336, supported DDR2 memory addressing configurations • Table B-23, "2Gb Addressing" on page 336, supported DDR2 memory addressing configurations
August 2008	001	Initial version

1.0 Introduction

The Intel® EP80579 Integrated Processor Product Line Platform Design Guide provides design recommendations for system designs based on Intel® EP80579 Integrated Processor or Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology. In addition to providing baseboard design recommendations, such as layout and routing guidelines, this document addresses system design issues.

Carefully follow the design information, schematics and layout checklists provided in this document. These design guidelines ensure maximum flexibility for board designers and reduce the risk of board related issues. Intel performs substantial validation testing based on the design guidelines that are defined in this document. Platforms that do not follow Intel design guidelines require intense scrutiny by designers, in both simulation and validation environments, to ensure different implementations are robust and meet the signal integrity requirements.

Note: The "Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Board" is referred to as "Development Board" throughout this document.

Note: The "Intel® EP80579 Integrated Processor Product Line" is referred to as "EP80579" throughout this document.

1.1 Reference Documentation

Table 1. Reference Documents (Sheet 1 of 2)

Item	Document Number/Source
TPM Specification Rev. 1.1	www.trustedcomputinggroup.org/
ATA Attachment — 6 with Packet Interface (ATA/ATAPI - 6)	http://T13.org *document: T13 1410D*
EPS12V Power Supply Design Guide	http://www.ssiforum.org
Front Panel I/O Connectivity Design Guide	http://www.formfactors.org
Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions Application Note	http://developer.intel.com
Intelligent Platform Management Interface (IPMI) Specification	http://developer.intel.com
The I^2C Bus Specification	http://www.semiconductors.philips.com
Intel® EP80579 Integrated Processor Thermal Product Line Design Guide	Note 1
Intel® EP80579 Integrated Processor Product Line Datasheet	Note 1
Intel® EP80579 Integrated Processor with Intel® QuickAssist Technology Development Kit User's Guide	Note 1
Low Pin Count (LPC) Interface Specification (Rev 1.0)	
PCI Express Base Specification Rev 1.1	http://www.pcisig.com/
System Management Bus (SMBus) Specification	http://www.smbus.org/specs/

Table 1.   Reference Documents (Sheet 2 of 2)

Item	Document Number/Source
Universal Serial Bus Specification	http://www.usb.org/developers/docs.html
High Speed USB Platform Design Guidelines	http://www.usb.org/developers/docs.html
82551QM/82540EM Interchangeable LOM Design Guide Application Note	http://developer.intel.com
82540EM Gigabit Ethernet Controller Datasheet and Hardware Design Guide	http://developer.intel.com

Notes:
1.   For the latest revision and documentation number, contact your local Intel field representative.

1.2   Acronyms and Terminology

Table 2.   Acronyms and Terminology (Sheet 1 of 3)

Acronym	Definition
ACPI	Advanced Configuration and Power Interface Specification, an industry specification of the common interfaces enabling robust operating system (OS)-directed motherboard device configuration and power management of both devices and entire systems.
AHCI	Advanced Host Controller Interface, an industry specification of the interface between memory and SATA devices.
AIOC	Acceleration and I/O Complex
AMC	1. Advanced Mezzanine Card 2. Audio/Modem Codec
ARP	Address Resolution Protocol
BER	Bit Error Rate
BGA	Ball Grid Array
CMC	Common Mode Choke
CM	Coherent Memory
CMI	Core interface, Memory controller hub, I/O controller hub
COTS	Commercial off-the-shelf-: Generally technology or computer products, that are ready-made and available for sale, lease, or license to the general public.
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DDR	DDR SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory), a system memory technology.
DDR2	Double Data Rate Synchronous Dynamic Random Access Memory, second generation.
DED	Double-bit Error Detect
D2D	Digital-to-Digital converter (voltage regulator)
DMA	Direct Memory Access, the hardware function when a peripheral accesses data in the memory in computer system without CPU intervention.
DW	Double Word, a legacy reference to 32 bits of data on a naturally aligned four-byte boundary (i.e. the least significant two bits of the byte address are b00). This is a legacy term used by PCI and must not be used in any other context.
E2E (e2e)	Edge-to-Edge
ECC	Error Checking and Correction

Table 2. **Acronyms and Terminology (Sheet 2 of 3)**

Acronym	Definition
EDMA	Enhanced DMA
EMI	Electro Magnetic Interference
EMTS	Electrical Mechanical Thermal Specification, used for processor specifications.
ESD	Electrostatic Discharge
FRU	Field Replaceable Unit
FS	Full-speed, refers to USB.
FSB	Front Side Bus (a common external interface for Intel® architecture (IA) processors)
FWH	Firmware Hub, a non-volatile memory device used to store the system BIOS.
HBA	Host Bus Adapter, necessary when connecting a peripheral to a computer that doesn't have native support for that peripheral's interface.
HCD	Host Controller Device, a USB interface for programmers
HECBASE	PCI Express Enhanced Configuration Base Register
HSI	High Speed Interface, refers to USB.
IA	Intel® Architecture instruction set commonly known as "x86"
IA-32 core	High performance processor based on the 32-bit embedded Intel® Architecture (IA-32) processor
I^{2}C	Inter-IC Control
I^{2}S	Integrated Interchip-Sound
ICE	In-Circuit-Emulator- JTAG based Emulator to debug software on an embedded system
ICH	I/O Controller Hub
IICH	Integrated I/O Controller Hub
IMCH	Integrated Memory Controller Hub
I/O	1. Input/Output 2. When used as a qualifier to a transaction type, specifies that transaction targets Intel® architecture-specific I/O space (e.g., I/O read).
IP	Internet Protocol
ITP-XDP	In Target Probe - Expanded Debug Port
JEDEC	Joint Electron Device Engineering Council, solid state technology forum
LEB	Local Expansion Bus - EP80579 internal bus to external expansion target devices such as external memory or other physical layer devices.
LPC	Low Pin Count
LS	Low-speed, refers to USB.
LSb	Least Significant Bit
LSB	Least Significant Byte
MCH	Memory Controller Hub
MMIO	Memory Mapped I/O
MSb	Most Significant Bit
MSB	Most Significant Byte
MSI	Message Signaled Interrupt that encodes interrupts as an in-band 32-bit write transaction.
MTBF	Mean Time Between Failures
NCM	Non Coherent Memory
NSI	North South Interface, the designation for the proprietary, internal high-speed serial interconnect between the IMCH and the IICH.

Table 2. **Acronyms and Terminology (Sheet 3 of 3)**

Acronym	Definition
OS	Operating System
P2P	Peer-to-Peer
PCI	Peripheral Component Interconnect Local Bus, a 32- or 64-bit bus with multiplexed address and data lines that is primarily intended for use as an interconnect mechanism within a system between processor/memory and peripheral components or add-in cards.
PCM	Pulse Code Modulation
PEC	Packet Error Checking, this is an SMBus 2.0 feature
PIRQx	Legacy PCI interrupt architecture that encodes interrupts on one of eight side-band signals (PIRQ[H:A]).
PLL	Phase-Locked Loop
POC	Power On Configuration
RDMA	Remote Direct Memory Access
RFL	Receive FIFO Level
RMW	Read-Modify-Write operation
RTC	Real-Time Clock
RTCRESET#	Signal that resets the RTC well (but does not clear the RTC RAM memory contents).
SATA	Serial Advanced Technology Attachment
SATA*	Serial ATA, an industry specification of the interface for storage controllers and devices.
SEC	Single-bit Error Correct
SEC/DED	Single Error Correct/Double Error Detect, a specific data protection algorithm that distributes data and ECC across 144 bits. Enables correction of single bit errors. Allows detection of double bit errors.
SM	M-Unit attached to the System Memory (Convention taken from IA CHAP event definition)
SMBus	System Management Bus
SMM	System Management Mode
SPD	Serial Presence Detect
STR	Suspend To RAM
TAP	Test Access Port used for testability and debug of the component
TCP	Transmission Control Protocol
TDM	Time Division Multiplexed
TDR	Time Domain Reflectometry
TFL	Transit FIFO Level
USB	Universal Serial Bus
VCC	Used to signal circuit logic voltage
VCXO	Voltage Controlled Crystal Oscillator
VDD	Used to signify DIMM logic supply voltage
VREF	Voltage Reference
VSS	Used to signify ground connection
VTT	Used to signify signal termination voltage
WDT	Watch Dog Timer
XDP	eXtended Debug Port

2.0 System Overview

2.1 System Architecture Description

The EP80579 is an System-On-Chip (SOC) device. The EP80579 SOC architecture combines the Intel® Architecture (IA-32) processor, an Integrated Memory Controller Hub (IMCH), an Integrated I/O Controller Hub (IICH), and high speed I/O interfaces (PCI Express* and Gigabit Ethernet). It integrates high-speed communications interfaces and hardware accelerators for high throughput packet and security processing. The architecture is designed to provide high-processing performance, low-power usage, and reasonable cost targets while maintaining IA implementation and providing the required I/O throughput. The EP80579 can be configured to meet many system application and implementation needs.

The EP80579 is manufactured on Intel's advanced 90 nanometer process technology and fully compatible with IA-32 software. This processor is offered in a 1,088 ball, Flip-Chip Ball Grid Array (FCBGA) package technology.

2.1.1 EP80579 Features

Table 3 provides a summary of key EP80579 features.
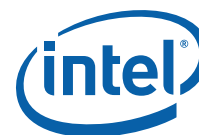
Table 3.   EP80579 Feature List

IA-32 core
- The core is based on the Intel® Pentium M processor and modified for SOC applications.
- Operating frequencies: 600 MHz, 1066 MHz and 1200 MHz
- On-chip FSB operating at 400/533 MHz
- 256 KB L2 cache

DDR2 Memory
- Up to 4 GB total system memory
- Supports DDR2-400, DDR2-553, DDR2-667, DDR2-800 modules
- Optional error protection using ECC bits and error code that supports SEC/DED (single bit error correction/double bit error detection)
- Supports unbuffered and registered DIMMS
- Supports 1 or 2 DIMMs (2 Ranks maximum)

Single DIMM
- 64 or 32 bit
- Single Rank (64 or 32-bit modes)
- Dual Rank (64-bit mode only)

Dual DIMM
- 64 bit only
- Single Rank only
- Both DIMMs must be the same type and technology

PCI Express
- Provides one x8 port, which can be scaled to 1x8 or 2x4 or 2x1

PCI Maximum Theoretical Bandwidth
- 250 MBps / direction for x1
- 1 GBps / direction for x4
- 2 GBps / direction for x8

Serial ATA (SATA)
- Contains two serial ATA ports capable of independent DMA operation
- SATA interface supports data transfer rates up to 3 Gb/s(300 MB/s) per port
- SATA 1.0 or 2.0 used to attached external hard drives

Local Expansion Bus (LEB)
- 25/16-bit 33/80 MHz Local Expansion Bus with 8 programmable chip selects

Universal Serial Bus (USB)
- Two ports supported:
  - One Enhanced Host Controller Interface (EHCI) USB 2.0.
  - One Universal Host Controller Interface (UHCI) USB 1.1
- Both ports support high-speed, full-speed, and low-speed USB devices

SMBus2.0/SMlink
- Two SMBus 2.0-complaint interfaces
- Compatible with most two-wire components that are also I²C compatible

Gigabit Ethernet Controller (GbE)
- Three GbE Media Access Controllers - RGMII/RMII
- Two of the three GbE ports support IEEE 1588-2008 Hardware Assist
- IEEE802.3 compliant
- GbE0 supports Wake-On-LAN
- MDIO interface to support the Ethernet interfaces

IEEE 1588-2008 Hardware Assist
- IEEE 1588-2008 Hardware Assist

GPIO
- Programmable General Purpose I/O (GPIO) pins.

Serial Ports
- Two 16550 compatible asynchronous serial ports that support data rate of up to 115Kbits/sec

Controller Area Network (CAN)
- Two Controller Area Network interfaces:
- Conforms to ISO 11898-1 (high-speed CAN)
- Fully CAN 2.0B compliant
- 40 MHz CAN clock frequency

TDM
- 8.192 MHz high-speed synchronous serial TDM interfaces that support up to 12 T1/E1 links (*with Intel software driver provided for HDLC support*)

SSP
- Synchronous Serial Port (SPI compatible) for TDM Configuration

SPI
- Synchronous Peripheral Interface for System BIOS Flash

2.2 Development Board

The Development Board is designed as a validation vehicle to test and verify the correct functionality of the EP80579 silicon. It also serves as an example of a validated implementation of the EP80579 silicon for external customers.

The Development Board provides interfaces to the extensive peripheral and I/O capabilities (SATA, GbE, USB, PCI Express, etc.) included in the part.

Figure 1 shows a detailed block diagram of the Development Board and Table 4 provides a summary of its features.
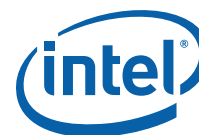
Figure 1.   Development Board Block Diagram
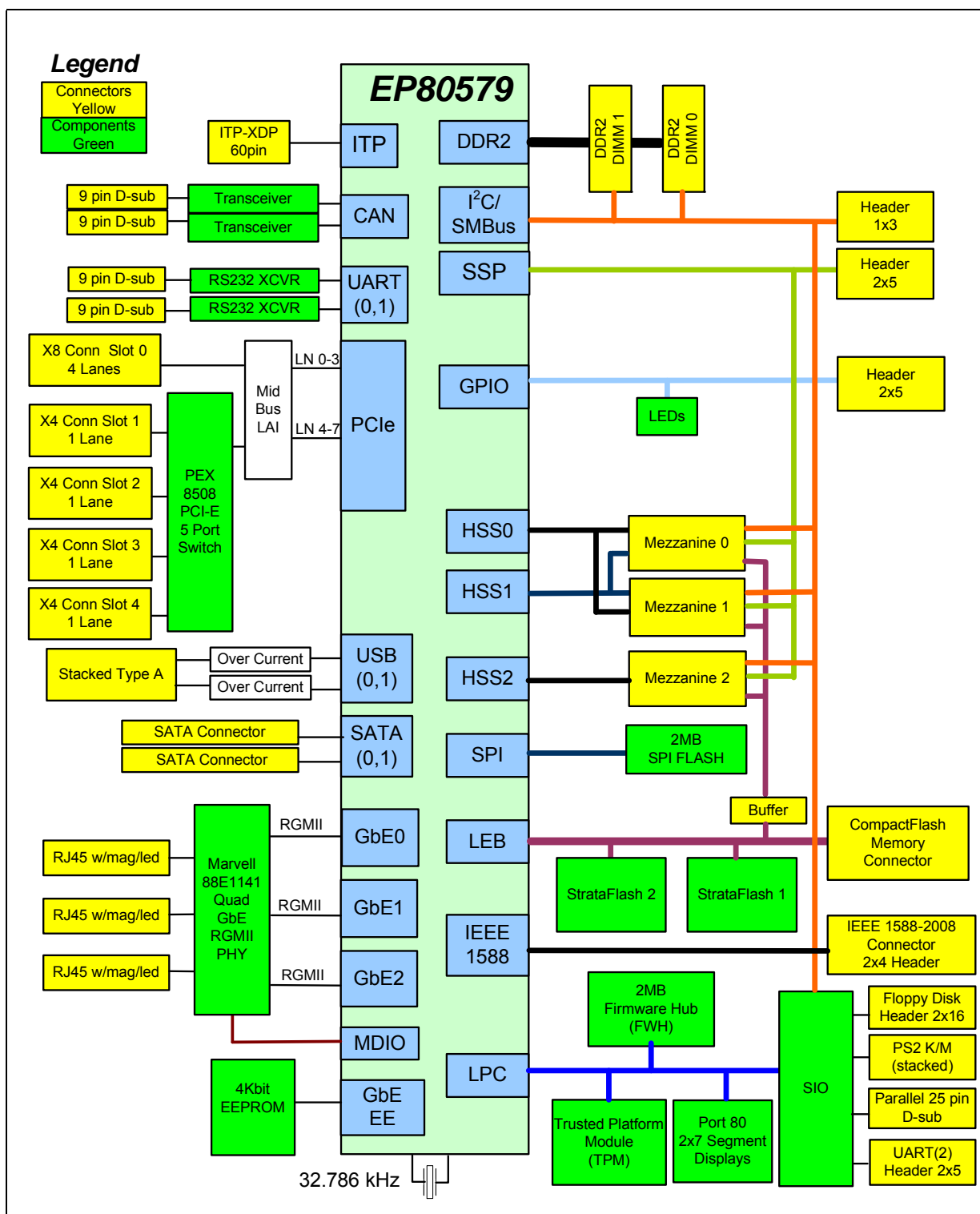
2.2.1 Development Board Features

Table 4. Development Board Feature List (Sheet 1 of 3)

Feature	Board Implementation	Comments
CPU Support		
IA-32 core	EP80579 Processor core	
IA-32 core connector style	Internal bus only	no connector
IA-32 core operating frequency	600 MHz/1066 MHz/1200 MHz	
IA-32 core regulator	Fixed voltage per bus and core frequency	two control pins for 2 voltage selection points, 1.0 V and 1.3 V
Chipset		
Chipset	EP80579 SOC Chip	combination of IMCH and IICH connected together through on-chip North-South Bridge (NSI) Internal Bus Interface
Package	1088-pin FCBGA	
BIOS	FWH TSOP40 16Mb (2 MB)	Socketed
Graphics		
Graphics	None integrated	
PCI Express	x1 PEG supported in PCI Express slots	card only
System Memory		
Memory support	Single channel DDR2	
Frequency	400 / 533 / 667 / 800 MT/s	
Slots	2 DIMMs	
Capacity	4 GB max	CPU limited (32-bit address space)
Ranks	1 or 2 ranks supported	two DIMMs - 1 rank Memory Module per DIMM or one DIMM - Up to 2 rank Memory Module
S3	Suspend to RAM (STR) is supported	
PCI Express		
PCI Express	Rev 1.0a	
x4 lanes	1	x8 connector with bottom four lanes as no-connect
Hot plug	Not implemented	
PCI-E switch	PLX PEX8508	bridge on the lower 4 lanes of the host port from EP80579
PCI-E behind the switch	4 x1 slots	x4 connectors with bottom 3 lanes as no-connect
SATA		
SATA	2 vertical connectors	fully shrouded

Table 4. **Development Board Feature List (Sheet 2 of 3)**

Feature	Board Implementation	Comments
USB		
USB 2.0 connectors	2 on rear panel	vertical stacked
Serial Ports (UART)		
Serial ports	2 - RS232E buffered on ten pin DB9-sub on rear	from EP80579
Synchronous Peripheral Interface (SPI)		
SPI Port	Synchronous Peripheral Interface for System BIOS Flash	
LPC		
Super I/O	SMSC SCH5027	jumper enabled
• Floppy disk connector	Yes	
• Parallel ports	1 25 pin D-sub provided on rear	
• Serial ports	1 Serial, RS232E buffered to 2x5 header with pin10 key	
• Keyboard/ mouse connector	Keyboard/mouse PS2 stacked connector on rear	
• Gluechip	Glue-4 specification	built into SIO
FWH	Firmware Hub for System BIOS	
Port 80	Two nibble 7 segment displays	
Power Management		
ACPI 1.0, 2.0, APM-compliant	Supports S0, S3, S5	
Testability		
On-board ICE tool	ITP-XDP	60 pin, ITP-XDP version 3
Test headers for logic analyzer	PCI Express midbus	on all 8 lanes
System Management Bus (SMBus)		
One Primary SMBus from the EP80579 with three Repeaters (SMBus A/B/C) for voltage translation, fanout, and isolation		
• Primary SMBus Connectivity	SIO, SMLink	
• SMBus A Connectivity	EP80579 (IMCH Slave device), CK410, DB800, ITP-XDP	
• SMBus B Connectivity	DDR2 DIMM0, DDR2 DIMM1	
• SMBus C Connectivity	Mezzanine (0/1/2) Connectors	
LAN Interface		
GbE Controller	EP80579 integrated MAC	
PHYs	One Marvell* Quad PHY	RGMII Mode Configuration

Table 4. **Development Board Feature List (Sheet 3 of 3)**

Feature	Board Implementation	Comments
Physical interface	Copper via 3 RJ-45	connectors include LEDs and magnetics
Thermal Solution		
CPU	Heat sink - COTS per TMAE recommendation	support for Active Cooler
Memory	None	fan header provided
Chassis	None	
Fan headers	Two 3-pin +12V fan headers a) CPU fan - variable speed control and temperature monitoring by SIO b) Optional Misc fan - fixed +12V	
Other		
Power supply	+12V, -12V, +5V, +3.3V, +5VSB	ATX or ATX12V
Power Supply Connectors	10-pin (Insertion Polarity Header)	
Voltage margining	SMA connector for each major on-board voltage regulator	
Clock chip	CK410	
Clock buffer	DB800	
Buttons	Reset, Power, Sleep	
Status LED Indicators	1.2V, 1.8V, 1.8V VSBY, 2.5V, 3.3V, 5.0V, 5.0V VSBY, CPU core, CPU RESET#, CPU THERMRIP#, CPU PROCHOT#, INT33V#, IERR#, HD Activity, SYS RESET. SLP_S3#	
TPM	Trusted Platform Module 1.2	Atmel*
Local Expansion Bus (LEB)	StrataFlash and Compact Flash support	2xStrataFlash (2F128P30) and additional Compact Flash connector
CAN	Two CAN connectors - 2x5 Headers with pin 10 key	
TDM	3x slots TDM Mezzanine slots	

2.3 EP80579 External Clock Requirements

External clocks are supplied to EP80579 internal PLLs as the reference clocks and to other I/O devices. EP80579 has internal PLLs that use these reference clocks to generate internal clocks. Table 5 shows the external clocks requirements for EP80579. These clocks shall always be sourced by the platform to EP80579 in all designs, regardless of whether the referenced interface is implemented or not implemented on the board.

Table 5. **EP80579 External Clock Requirements**

Clock Domain	Frequency	Source	Description
CLKP100/CLKN100	100 MHz (diff)	External	IA-32 core Clock
PEA_CLK(p/n)	100 MHz (diff)	External	PCIe Clock
RTCX1/RTCX2	32.768 MHz	External	RTC Cystal
PCICLK	33 MHz	External	PCI/LPC Reference Clock
UART_CLK	48 MHz	External	Serial Interface (UART) Clock

Table 5.   EP80579 External Clock Requirements

Clock Domain	Frequency	Source	Description
SATA_CLKREF(p/n)	100 MHz	External	SATA Reference Clock
CLK48 (USB)	48 MHz	External	USB Clock
CLK14	14.31818 MHz	External	Timer Oscillator Clock
GBE_REFCLK	125 MHz (RGMII)/ 50 MHz (RMII)	External	GBE Reference Clock
GBE_REFCLK_RMII	100 Ω pull-down (RGMII) / 50 MHz (RMII)	External	RMII Reference Clock
EX_CLK	33/80 MHz	External	Expansion Bus Clock

3.0 Baseboard Requirements

3.1 Development Board Component Placement

Table 6 lists the assumptions used for the component placement of the Development Board. See www.formfactors.org for detailed information on the ATX specification.

Table 6. Assumptions for System Placement Example

System Configuration	Assumptions		
	Form Factor (ATX Specification)	Number of PCB Layers	Assembly
Desktop board	ATX 2.2	Ten layers	Double-Sided
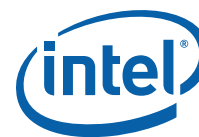
Figure 2.   Development Board Component Placement — Top View
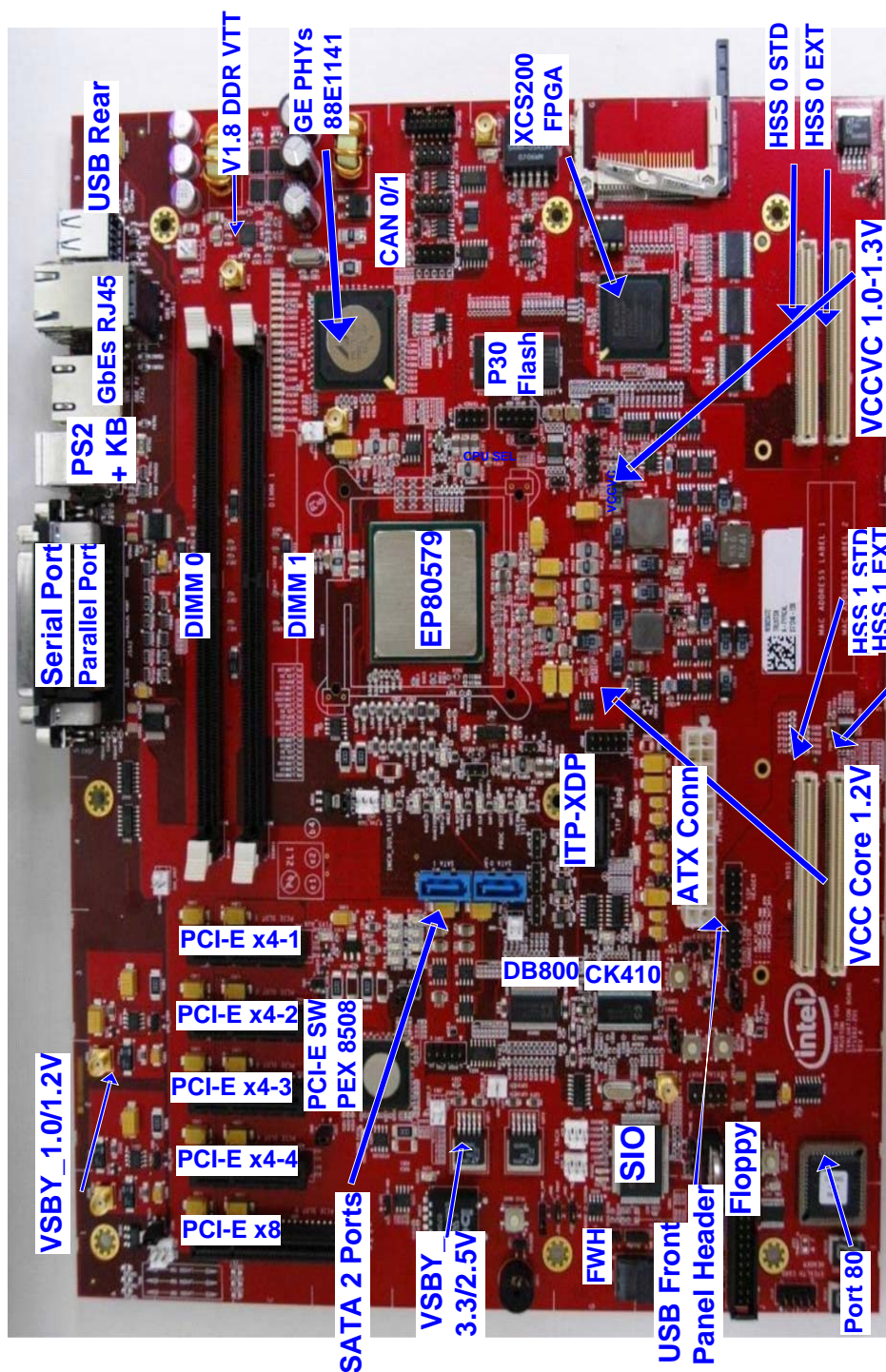
Figure 3.   Development Board Component Placement – Bottom View
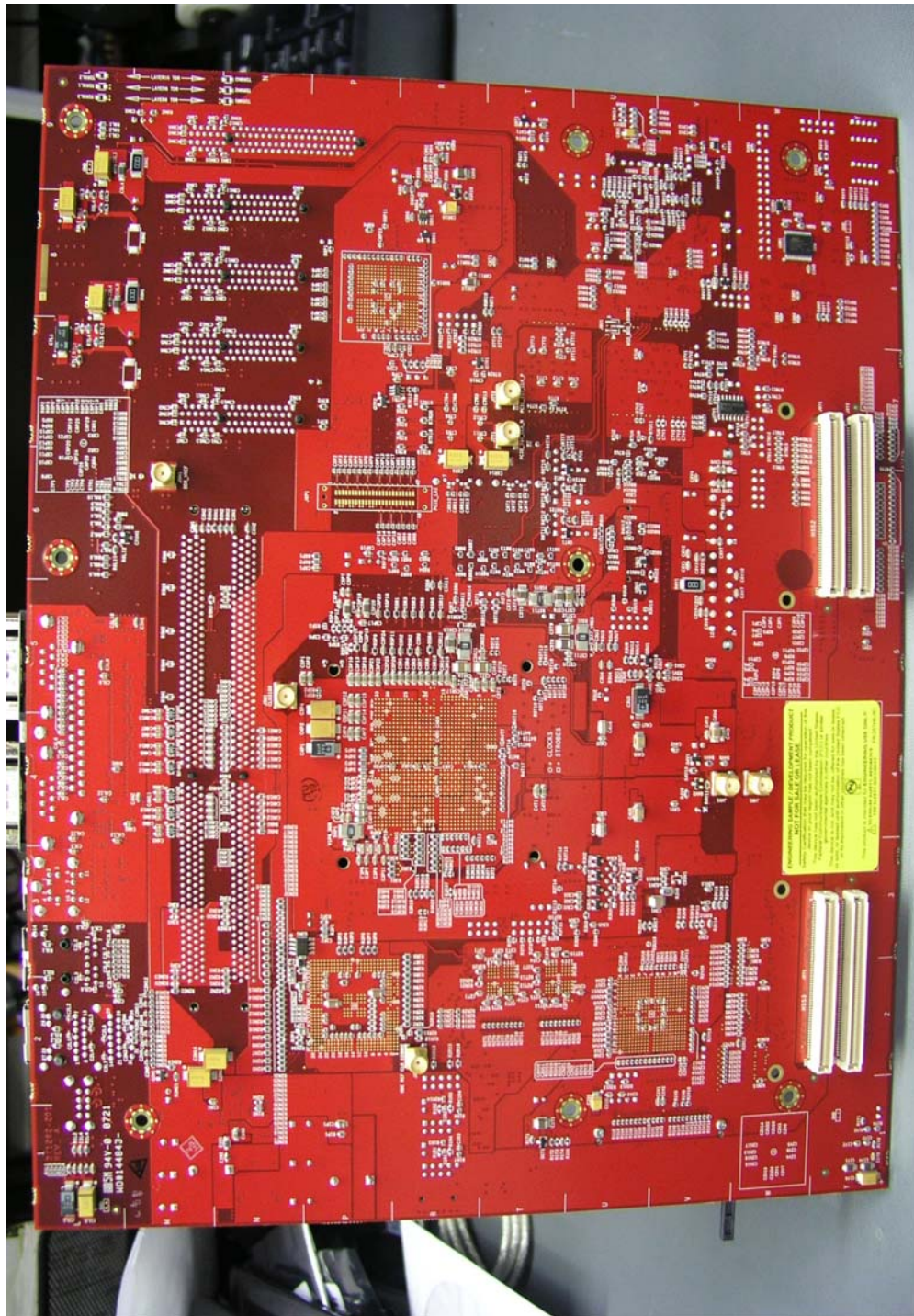
3.2 Platform Stack-Up

Figure 4 shows the recommended platform stack-up.

Signal layers are dual referenced asymmetric stripline on layers 3, 5, 6, and 8 and microstrip on layers 1 and 10. Signal layers 1, 3, 5, 6, 8, and 10 are referenced to ground.

Intel strongly recommends that system designers use the stack-up shown in Figure 4 and recommendations in Table 7 when designing their boards. Intel realizes numerous ways exist to achieve these targeted impedance tolerances; contact your board vendor for these specifics. Intel encourages platform designers to perform comprehensive simulation analysis to ensure all timing specifications are met. This is particularly important if a design deviates from the provided design guidelines.

Figure 4. PCB Recommended 10-Layer Stack-Up

	Thk. (mils)	Er		Single-ended							Edge-coupled differential						Reference Plane
				60 ohms	55 ohms	50 ohms	48 ohms	45 ohms	40 ohms	27.4 ohms	100 ohms	90 ohms	85 ohms	100 ohms	90 ohms	85 ohms	
				Finished Trace Width (mils)							Finished Trace Width (mils)			Trace to Trace Centers (mils)			
Soldermask	0.8	3.60															
Copper Plate	1.3																
Copper Foil	0.6		L1 Top	3.75	4.50	5.50	6.25	6.75	8.50	15.50	4.00	4.75	6.00	10.00	10.00	12.00	L2
Pre-preg	3.6	4.11															
	1.2		L2 Pln														
Core	4	4.10															
	0.6		L3 Sig		3.75	4.50	4.75	5.50	6.50	11.50	3.75	4.50	5.50	10.00	10.00	13.00	L2/L4
Pre-preg	6	4.10															
	1.2		L4 Pln														
Core	4	4.10															
	0.6		L5 Sig	4.25	5.00	6.00	6.50	7.25	9.00	16.00	4.25	5.00	6.00	10.00	10.00	11.00	L4/L7
Pre-preg	25	4.10															
	0.6		L6 Sig	4.25	5.00	6.00	6.50	7.25	9.00	16.00	4.25	5.00	6.00	10.00	10.00	11.00	L4/L7
Core	4	4.10															
	1.2		L7 Pln														
Pre-preg	6	4.10															
	0.6		L8 Sig		3.75	4.50	4.75	5.50	6.50	11.50	3.75	4.50	5.50	10.00	10.00	13.00	L7/L9
Core	4	4.10															
	1.2		L9 Pln														
Pre-preg	3.6	4.11															
Copper Foil	0.6		L10 Bot	3.75	4.50	5.50	6.25	6.75	8.50	15.50	4.00	4.75	6.00	10.00	10.00	12.00	L9
Copper Plate	1.3																
Soldermask	0.8	3.60															

72.80 *Finished board thickness (After plating and solder mask):*

General Routing Guidelines

- All length and matching rules assume pin to pin unless otherwise noted.
- Microstrip or stripline routing is assumed for each interface unless otherwise noted.
- Minimize the number of vias used for each interface.
- Never route signals over plane splits and always try to maintain the same reference plane.
- Avoid 90° bends.
- Although there is a large core thickness between layers 5 & 6, try to minimize the length that traces run parallel on adjacent layers.
- Do not route critical signals under inductors or other noisy components.

Table 7.   Development Board Summary

Board Factor	Recommendation
Material	• Standard FR4 Tg 170 Epoxy • 370HR used for lead free

Impedance requirements[1]	• DDR2:
	   • Varies depending on the layer, the signal, and the topology used.
	• PCI Express*:
	   • 90 Ω ±10% differential with 4.5-mils trace width for stripline layers
	   • 90 Ω ±10% differential with 4.75-mils trace width for microstrip layers

Etch-Etch Spacing	• See the routing guidelines for each interface for this information.
Finished Via Size	• Minimum via size is 10 mils finished hole/21 mils pad/31 mils anti pad
Finish	• Soldermask over bare copper (SMOBC) and immersion gold
Soldermask Type	• SM-840 minimum web 4 mils
Fabrication	• Edge Routed
Component Technology	• Through hole/SMT • QFP, BGA, and discrete 0603, 0805 Front side (Top layer) • Discrete 0603, 0805,7343, 1210 Back side (Bottom layer)

Note:
1.   See the appropriate section in this guide for all possible impedance information. This table is only a general summary.

3.3   Mounting

The Development Board uses non-plated holes for mounting the board. The mounting holes have a spoked ground ring on the top and bottom of the board for all true mounting holes. The hole size for a true mounting hole is 0.125" and the ground ring outer diameter is 0.40". The hole placement follows Extended ATX wherever possible. The Development Board also uses phantom mounting holes. Phantom mounting holes are 0.4" etch keep-out circles on the bottom of the board. The phantom holes can be used for extra board support by aligning a stand off in the center of the phantom hole.

4.0 Component Quadrant Layout

Figure 5 and Figure 6 show only general quadrant information for the EP80579 component, and not exact component pin placement. Designers must use the exact pin assignment to conduct routing analysis. See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for exact ball assignment information.

4.1   Quadrant Layout

Figure 5.   Quadrant Layout (Top View)

Top View
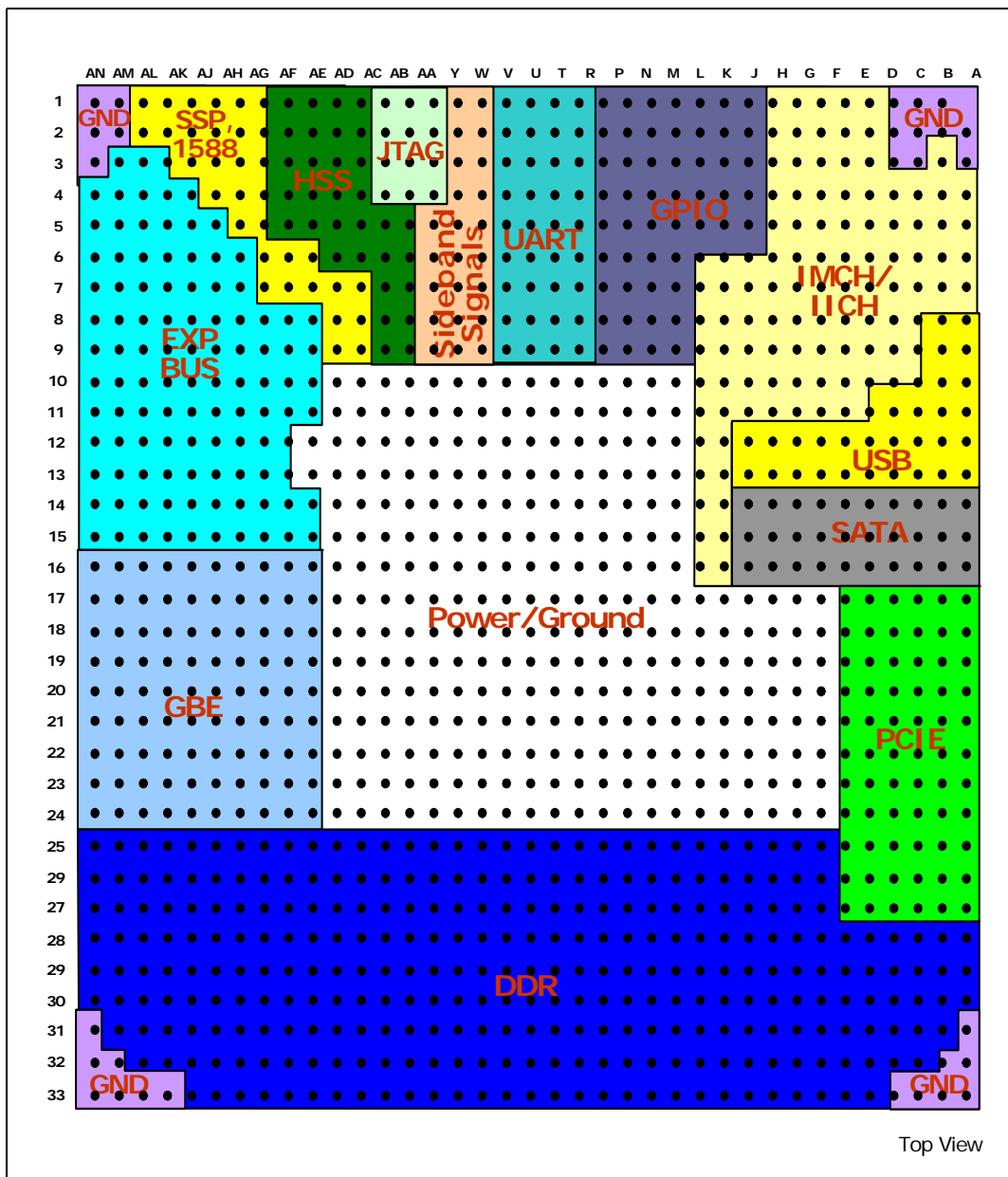
Figure 6.   Quadrant Layout (Bottom View)

Bottom View
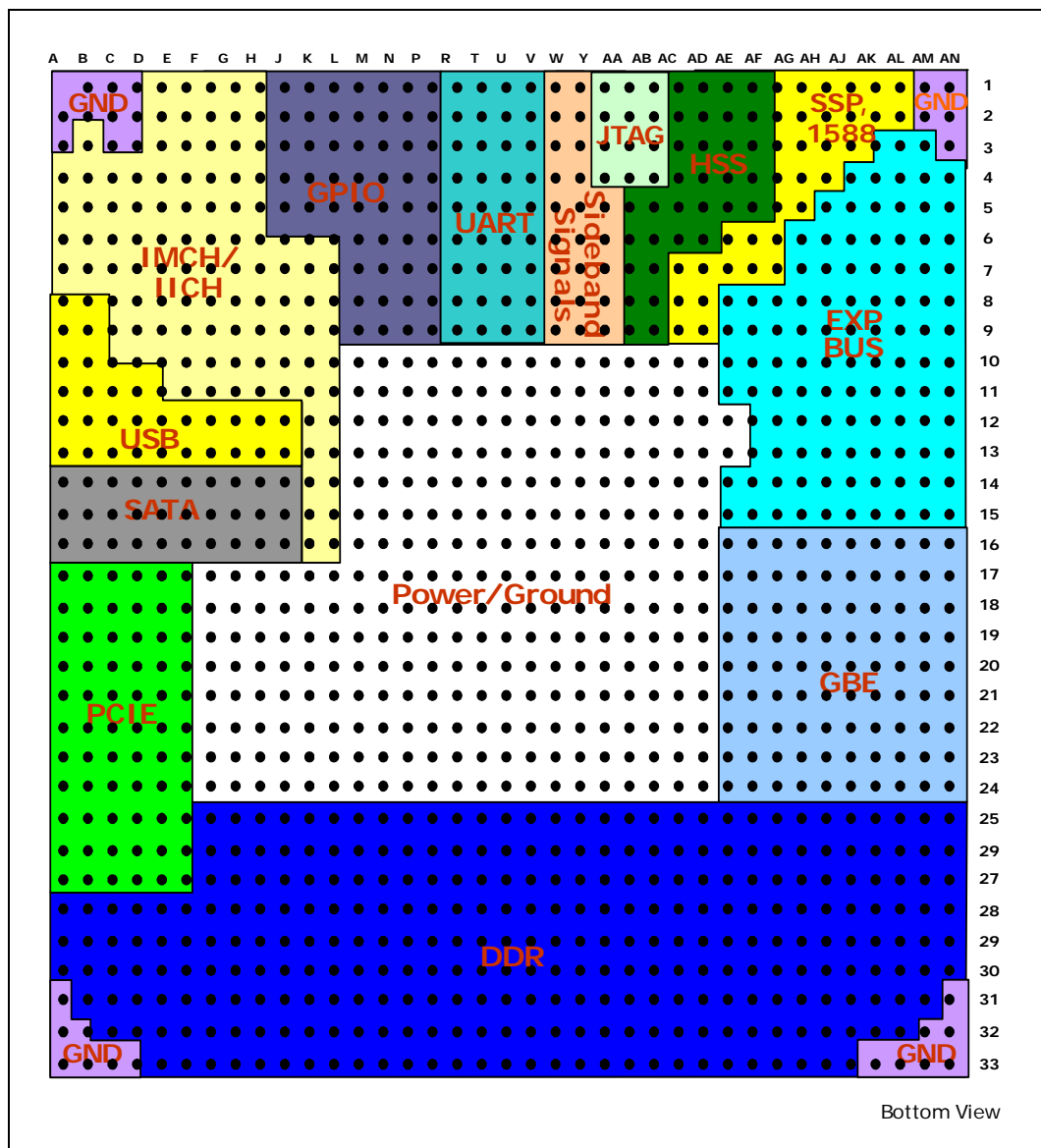
5.0 High-Speed Design Concerns

This chapter describes basic high-speed design practices as they apply to the EP80579.

5.1 Return Path

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, or integrated circuits. The return path is based on electromagnetic field effects. It is useful to think of the return path as the path of least impedance nearest the signal conductor. Discontinuities in the return path often have signal integrity and timing effects similar to the discontinuities in the signal conductor. Therefore, the return paths must be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor, to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance.

The following set of rules for the return path apply to all designs:

- Always trace out the return current path and pay as much attention to the return path as to the path of the signal conductor.
- Do not allow splits in the reference planes in the path of the return current.
- Do not route signals on the reference planes near the system bus signals.
- Do not allow signal layer changes that force the return path to make a reference plane change, even when from one ground layer to another ground layer.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not route over via anti-pads or socket anti-pads.

When reference plane changes must be made:

- Change from a ground reference to a ground reference and place a via that connects the two planes as close as possible to the signal via. This guideline also applies when making a change from VCC to VCC.
- For symmetric stripline, provide return path vias for both ground and VCC.
- Do not switch the reference from VCC to ground or ground to VCC.

5.2 Decoupling Theory

The primary objective of the decoupling guidelines is to minimize the impact of return path discontinuities and to ensure that the I/O has adequate power decoupling. The worst-case return path discontinuity anticipated is for systems that use microstrip structures on the motherboard. When a motherboard uses symmetric stripline with VCC and ground references, a discontinuity does not exist and additional decoupling is not necessary. When the motherboard routing references only a single VCC or ground plane, a return path discontinuity exists.

The inductance of the system caused by cables and power planes slows the power supply's ability to respond quickly to a current transient. Decoupling a power plane may be broken into several independent parts. More inductance is bypassed by placing the capacitors closer to the load. Bypassing the inductance of leads, power planes, etc., requires less capacitance. However, trade-offs must be made since there is less room for capacitance as it is placed closer to the load.

5.2.1 Bulk Decoupling

Larger bulk storage components, such as electrolytic capacitors, are placed across the power input of the board to filter lower frequencies that usually are generated off the board. A suitable capacitance value should be calculated, and many capacitors may be placed in parallel to achieve the value. Maintaining voltage tolerance during changes in current requires high-density bulk capacitors with low Effective Series Resistance (ESR), and low Effective Series Inductance (ESL). Use thorough analysis when choosing these components.

Power bypassing is required due to the relatively slow speed at which a DC-to-DC converter may react. Bulk capacitance supplies energy from the time the high-frequency decoupling capacitors are drained, until the power supply may react to the demand. More correctly, the bulk capacitors in the system slow the transient requirement seen by the power source to a rate it is able to supply, while the high-frequency capacitors slow the transient requirement seen by the bulk capacitors to a rate they may supply

5.2.2 High-Frequency Decoupling

The system boards should place high frequency decoupling as close to the power pins and ground pins of the load as physically possible. Use both sides of the board when necessary for placing load to achieve the optimum proximity to the power pins. This is vital because the inductance of the board's metal plane layers could cancel the usefulness of these low inductance components.

Shorten the path from the capacitor pads to the pins the capacitor is decoupling. When possible, place the vias connecting to the planes within the pad of the capacitor. When not possible, keep the traces as short and wide as is feasible. Possibly one or both ends of the capacitor may be connected directly to the pins of the load without the use of a via. Figure 7 illustrates these concepts.

Better performance can be obtained by minimizing the distance between the chip and capacitor; the connection from the capacitor to the power pin should be kept as short and wide as possible to minimize inductance of the connection. Consider placing the capacitor on the opposite side of the board directly under the chip.

Figure 7. Proper Decoupling Capacitor Placement with Respect to Vias
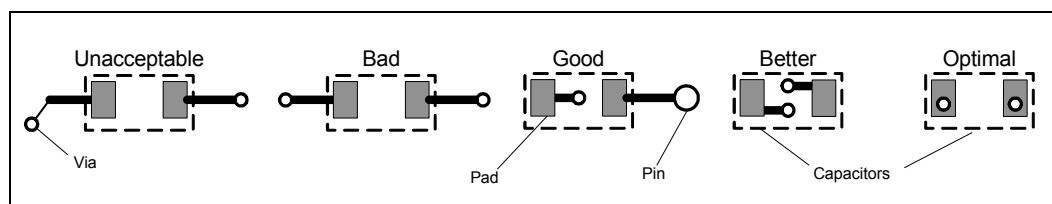
5.3 Serpentine Routing

A serpentine net is a transmission line, routed in such a manner that sections of the net double back and couple to other segments of the same net (see Figure 8).

Figure 8.   Routing in a Serpentine Manner
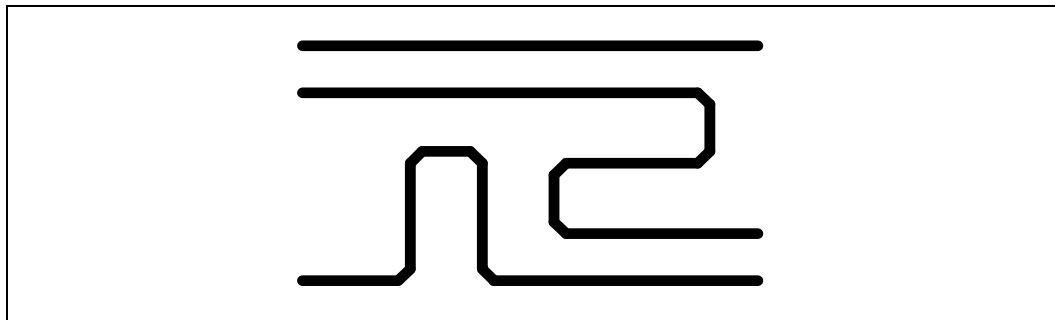
Routing a transmission line in a serpentine manner is sometimes necessary to properly match lengths between nets. It is important to properly control the serpentine to avoid signal integrity and timing problems. The primary impact of a serpentine-routed trace is an observed decrease in the flight time when compared to a straight trace of equal length. This decrease in the flight time is a result of the crosstalk between parallel sections of the serpentined net. As the signal travels down the transmission line, a component of the signal follows the transmission line and behaves as though it were a straight line with no serpentine. However, another portion of the energy propagates perpendicular to the parallel routed portions of the serpentined net via the mutual capacitance and mutual inductance. This creates an extra mode that arrives at the receiver significantly earlier than the other component of the signal. When the coupling between parallel sections is high, significant timing skew may occur when attempting to match trace lengths on a bus. Furthermore, when the coupling is very high, significant signal integrity problems may result.

Serpentine routing requirements are defined using two parameters, as depicted in Figure 9. Parameter "S" is the distance between the two segments of the serpentined trace. Parameter "H" is the distance between the signal and the referenced plane. The ratio is specified as S/H. For the EP80579 stack-up this ratio is typically 3:1. Check the guidelines for each interface to ensure the proper ratio is being used.

Figure 9.   Serpentine Spacing-Spacing to Reference Plane Height Ratio
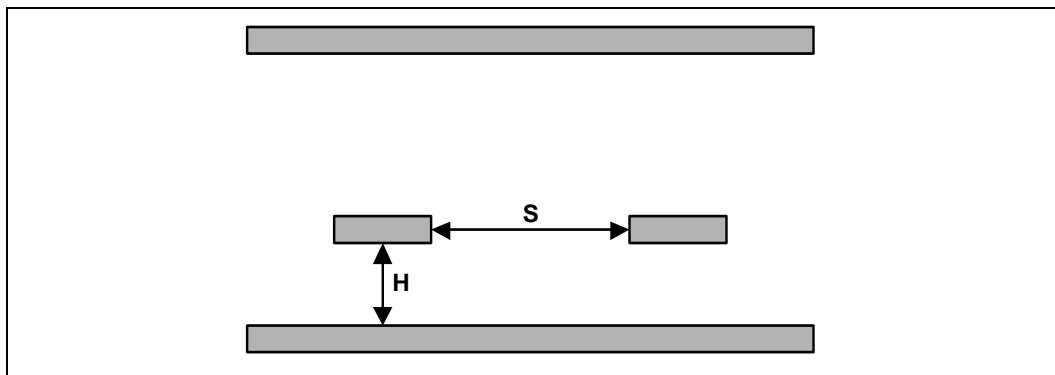
5.4   High Speed Differential Routing Rules

The rules in the following sections pertain to high speed differential signals such as the SATA and the PCI Express* signals.
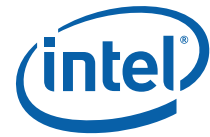
5.4.1 Serpentine Line Rules for Differential Signals

Figure 10. Serpentine Line
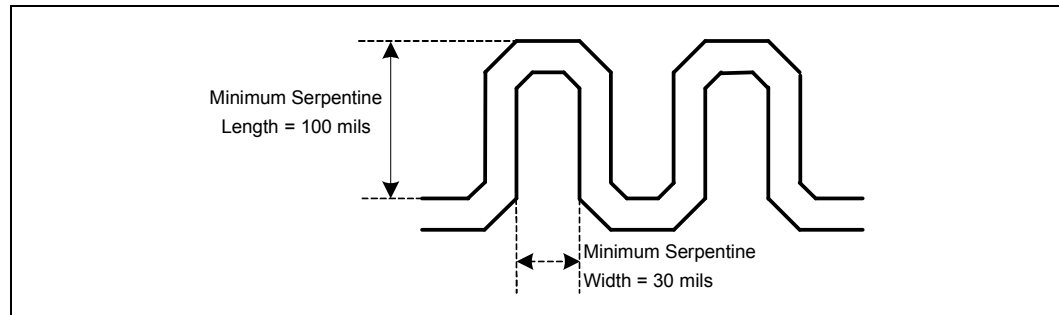
A meander or serpentine line is a transmission line routed in such a manner that segments of the line zigzag and couple to the other segments of the same line. To achieve balanced trace lengths for the critical signals within a group or between the groups, the meander lines can be used to provide fine control of the delay skew requirements. Because of the difference in delays between a straight line and a serpentine line with tight pitch, design rules are needed to guarantee the proper delay skew control for the serpentine lines. When routing matched length lines, the serpentine traces must be at least 100 mils long and 30 mils apart. Meander or serpentine shapes are responsible for a significant reduction in the propagation delay, as compared to the delay in a straight line, as a result of the crosstalk between parallel sections of the serpentine line.

- A sufficient rule of thumb: the edge-to-edge separation of the serpentine line to any other trace must be at least 3x the separation trace width in the stripline structure and 5x when routing in the microstrip structure so that crosstalk is minimal.
- Limit the total number of turns to 15 or fewer for the serpentine traces.
- If the layout permits, make the turns larger and fewer.
- Maintain the spacing, preferably > 10x, both within a meander and between a meander and the other signals.
- Any miter turn must not be greater than 45°.
- No sharp corner or 90° bend is allowed.

5.4.2 Stitching Differential Signals Between Layers

Differential signals must not pass over plane splits if possible. If absolutely necessary, the planes must be stitched together with capacitors where the differential signals cross the plane splits. If such stitching is impractical, the impact is primarily on EMI, not on the signal integrity of the differential signal. If the routing goes from one side to another, vias can be used for multiple signals. Some basic rules when stitching planes together are as follows:

- The signal of a pair may pass through a single reference plane without stitching.
- Vias are presumed to be through-hole. The layers the signal current traverses, not the layers the via traverses, should be considered more important. Use stitching vias when a signal passes through more than one reference plane.
- If the planes are at the same potential, both ground, they must be directly tied together.
- When the stitching vias are used where a signal changes layers, they must be symmetrically placed within ~125 mils of the signal vias. See Figure 13.

- Stitching vias must not include the thermal relief.
- One stitching via between a pair of traces is good. Two stitching vias, one on either side of the signal-via pair, is better.
- The minimum distance of a stitching via anti-pad to the signal trace edge is 5 mils.

Figure 11.   Tied Together for the Same Potential Planes
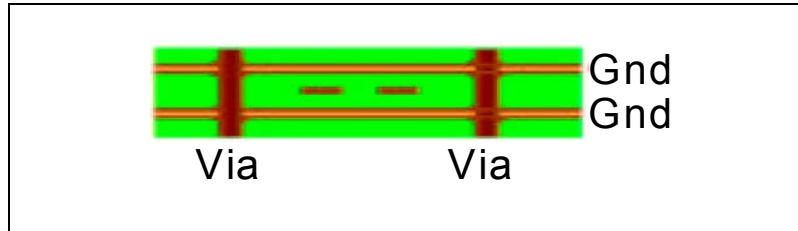
Figure 12.   Series Capacitor for Different Potential Planes
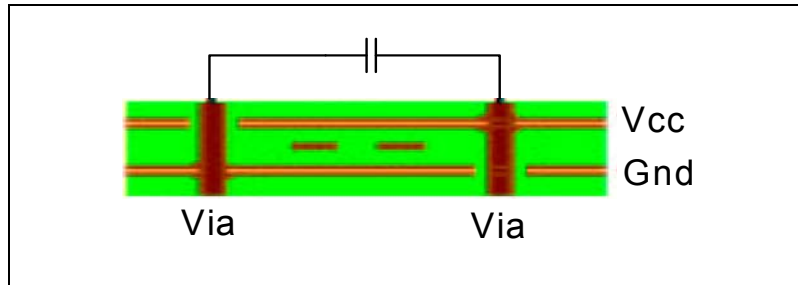
Figure 13.   Stitching Vias Aligned with Signal Vias
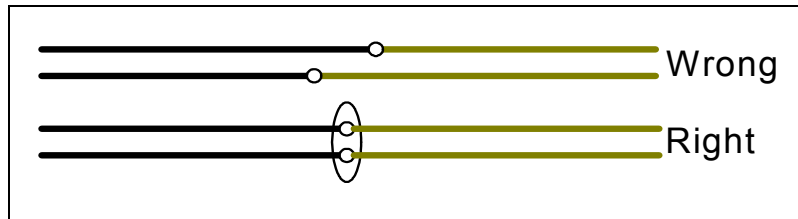
Figure 14.   Stitching for Layer Changes
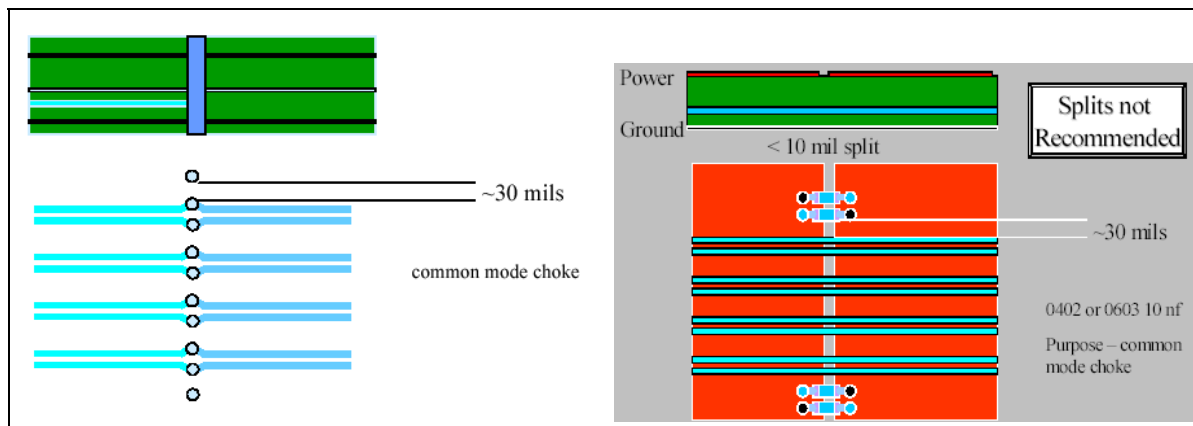
5.4.3 Trace Segment Length Equalization, Bend, and Spacing

The following are several general rules regarding the length matching and other factors when routing high speed differential signal (see Figure 16 when reviewing these rules):

- Trace length matching between pairs is not required due to the embedded clock and the pair-to-pair skew allowance; however, it is desirable to keep the length differences small to minimize the latency.

- Trace segment length matching within the pair is required to ensure the trace lengths are equal on a segment-by-segment basis.

- Examples of the segments could include the breakout areas, routes between the two vias, routes between an AC coupling capacitor, and a connector pin, etc.

- When the ball-outs cause the traces to be staggered in the breakout region, add a trace to equalize the length within the first 0.125 in.

- When a pair turns a corner, add a trace length to the inner side trace to equalize the length within 0.125 inches of the corner.

- Do not equalize the net lengths only at the ends of a differential pair.

- Where a pair changes the layers, do not stagger the vias in the pair.

- Maintain the lateral symmetry between the traces as well as possible.

- When the traces are routed parallel to a plane edge, they must be at least 5x the the dielectric height (5xH). See Figure 15.

- Avoid 90° bends.

Figure 15. Traces Routed Parallel to Plane
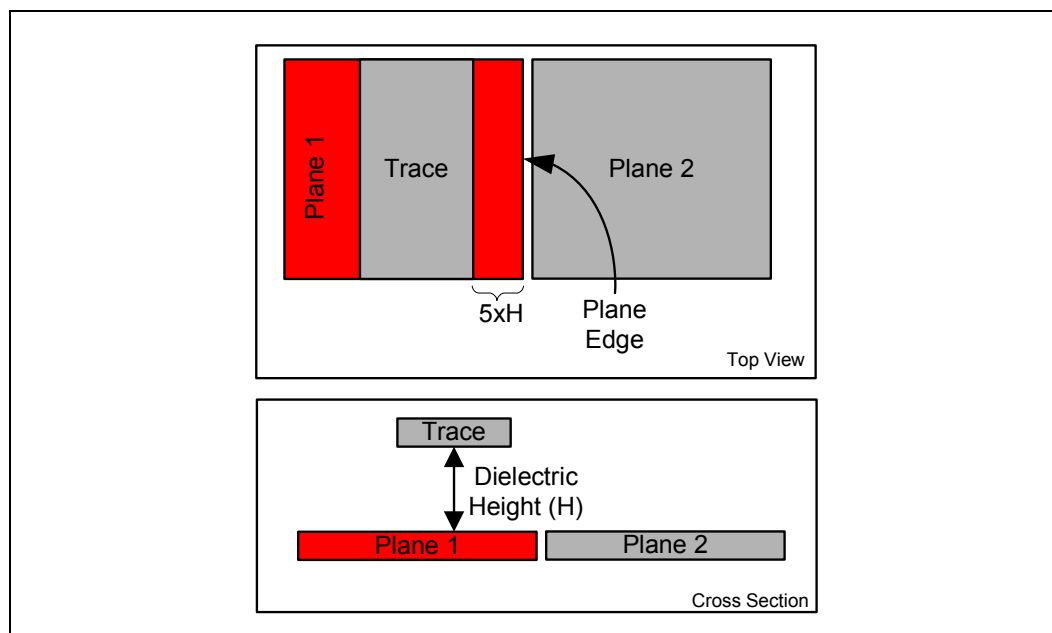
Figure 16.   Trace Segment Length

Equalization Length of Segments

Maintain the Lateral Symmetry for Traces
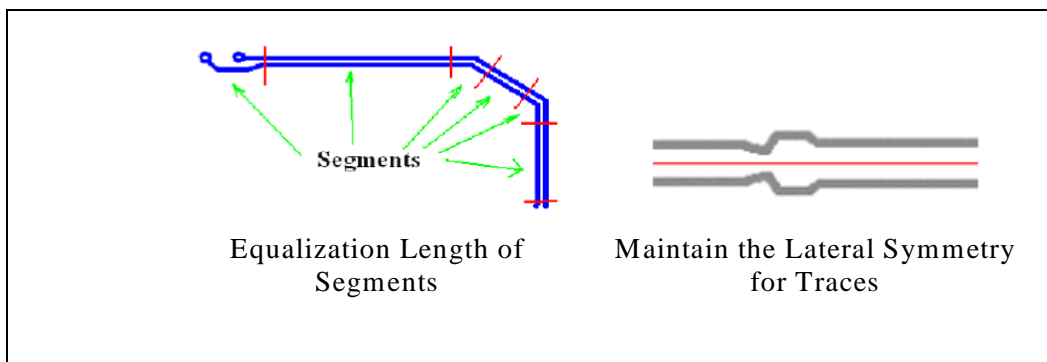
5.4.4   Trace Mismatch and Compensation

The following rules describe how to handle trace mismatch (see Figure 19 and Figure 20 for additional examples):

- If the trace segment between the bend corners is greater than 600 mils, adjust the mismatch to be less than 1 mil. See Figure 18.
- Match the overall length of a differential pair within 5 mils.
- Match the overall length between two adjacent differential pairs within 1000 mils.
- All trace segments must be matched within 2 mils.
- Adjust the trace length near the mismatch. See Figure 17.
- The length compensation must be performed by working on a unified direction (a north to south or south to north, but not both).

Figure 17.   Trace Mismatch

* Watch out for the length reporting issues in Allegro and other routing tools.

Escape Routing   Trace Length Adjusted Near Mismatch
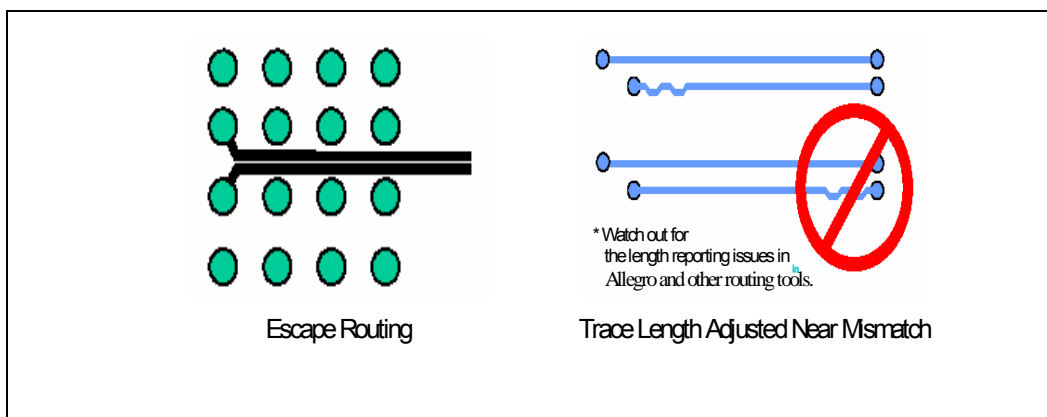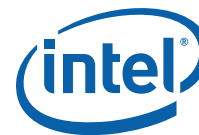
Figure 18.   Trace Length Mismatch Corners
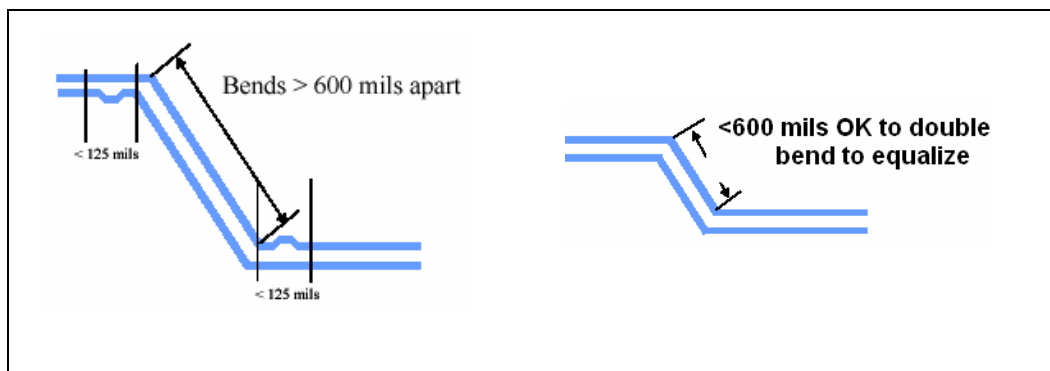
Figure 19.   Routing Examples of the Length Compensation #1
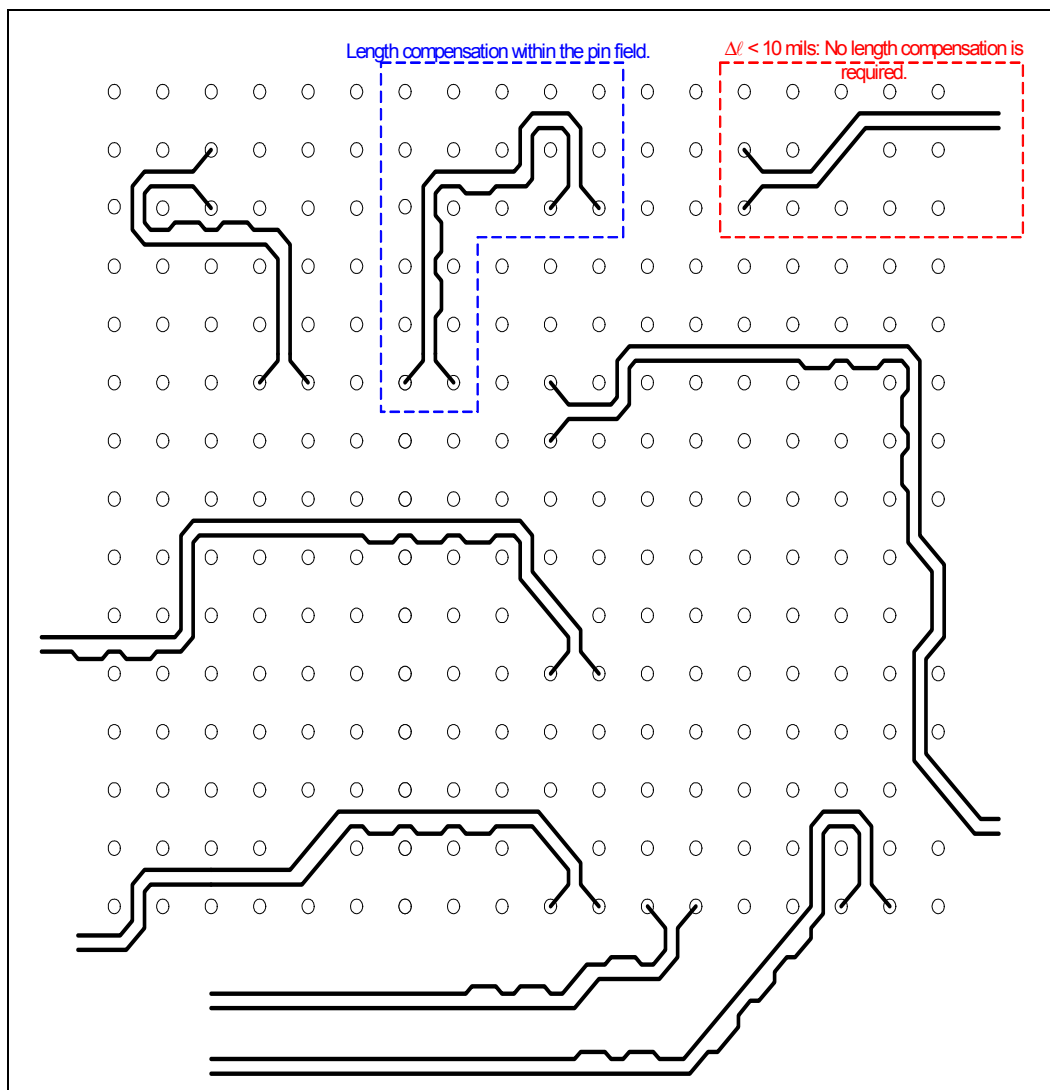
Figure 20. Routing Examples of the Length Compensation #2
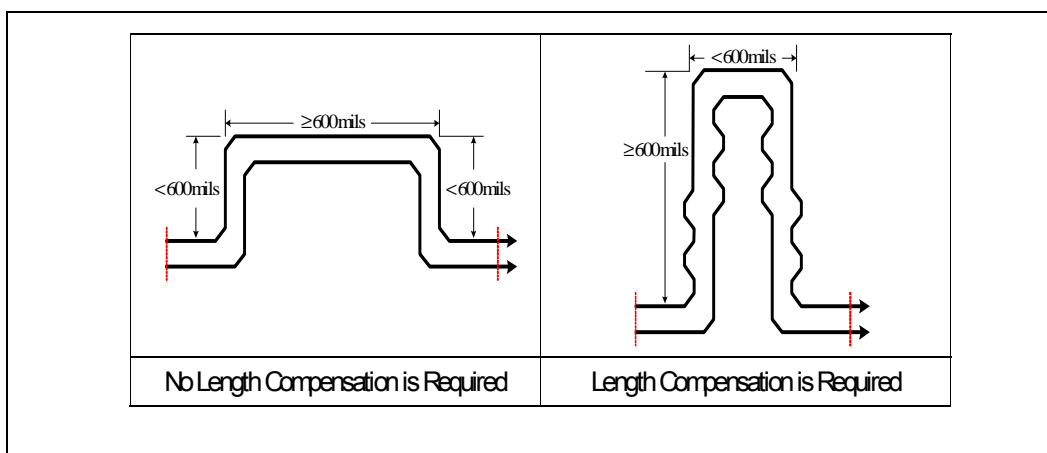
5.4.5 DC Blocking Capacitor

Many differential signals require DC blocking capacitors. In these cases, placement symmetry for the capacitors is recommended, as shown in Figure 21.

Figure 21. DC Blocking Capacitor
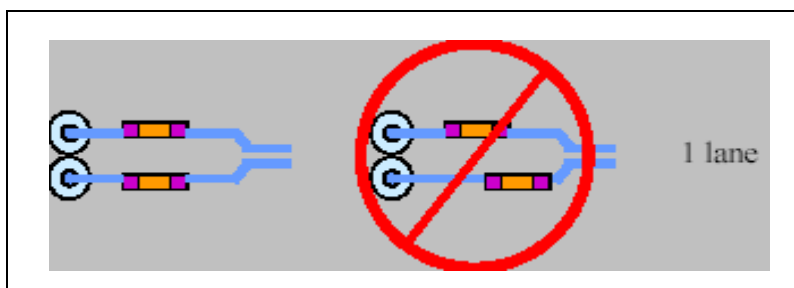
5.5 EMI Design Consideration

As microprocessor power and speeds increase, the ability to contain the corresponding electromagnetic radiation becomes more difficult. Frequencies generated by these processors may be in the low GHz range, which may impact both the system design and the EMI test methodology.

This section provides electrical and mechanical design engineers with information to aid in developing a platform that may meet government EMI regulations. Specifically, the impact of differential clocking, spread spectrum clocking, and the test methodology to the FCC Class B requirements are discussed.

Designers must be aware that implementing all the recommendations in this guideline may not ensure compliance to EMI regulations. Rather, these guidelines may help to reduce the emissions from processors and motherboards and make chassis design easier.

The following sections describe design techniques that may be applied to minimize EMI emissions. Some techniques have been incorporated into Intel-enabled designs (differential clock drivers, selective clock gating, etc.), while others must be implemented by motherboard designers (trace routing, clocking schemes, etc.).
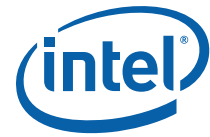
5.5.1 Brief EMI Theory

Electromagnetic energy transfer may be viewed in four ways:

- Radiated emissions
- Radiated susceptibility
- Conducted emissions
- Conducted susceptibility

For system designers, reduction of radiated and conducted emissions is the way to achieve EMC compliance. Susceptibility is typically not a major concern in the server environment, although it may be more important in an industrial environment.

The main component of EMI is a radiated electromagnetic wave, which consists of both electric (E-fields) and magnetic (H-fields) waves traveling together and oriented perpendicular to one another. Although E- and H-fields are intimately tied together, they are generated by different sources. E-fields are created by voltage potentials, while H-fields are created by current flow. In a steady state environment where voltage or current is unchanging, E- and H-fields are also static and of no concern to EMI. Changing voltages and currents are of concern since they contribute to EMI. When a dynamic E-field is present, there must be a corresponding dynamic H-field and vice versa. Motherboards with fast processors generate high-frequency E- and H-fields from currents and voltages present in the component silicon and signal traces.

Two methods exist for minimizing E- and H-field system emissions: prevention and containment. Prevention is achieved by implementing design techniques that minimize the ability of the motherboard to generate EMI fields. Containment is used in a chassis environment to contain radiated energy within the chassis. Careful consideration of board layout, trace routing, and grounding may significantly reduce a motherboard's radiated emissions and make the chassis design easier.

5.5.2 EMI Regulations and Certifications

Original Equipment Manufacturers (OEMs) ensure EMC compliance by meeting EMI regulatory requirements. System designers must ensure that their computer systems do not exceed the emission limit standards set by applicable regulatory agencies. Regulatory requirements referenced in this document include:

- United States Federal Communication Commission (FCC) Part 15 Class B.
- International Electrotechnical Commission's International Special Committee on Radio Interference (CISPR) Publication 22 Class B limits.

The FCC rules require any OEM that sells an "off-the-shelf" motherboard in the United States to pass an open chassis test. Open chassis testing is defined as removing the chassis cover (or top and two sides) and testing for EMI compliance. This test must be completed even though the permitted emission levels on the open chassis are allowed to be higher. Removing the cover greatly reduces the shielding provided by the chassis and increases the amount of EMI radiation. The purpose of this regulation is to ensure that system boards have reasonable emission levels since they are one of the main contributors to EMI.

5.5.3 EMI Test Capabilities

FCC regulations in the United States specify the maximum test frequency for products with clocks in excess of 1 GHz is five times the highest clock frequency or 40 GHz, whichever is lower. OEMs are advised to inquire into the capabilities of their preferred EMC test lab to ensure they are able to scan up to the required frequency range.

Processor performance and frequency double approximately every two years. With this in mind, it is advisable to be prepared for the frequencies that may need to be scanned in the next few years.

Since the FCC rules ultimately require testing to 40 GHz, commercial test equipment has been developed that is capable of making measurements to that frequency. Although it may be some time before processors require testing at this frequency, it may be less expensive to upgrade to 40 GHz test equipment now, rather than making several intermediate steps.

It is also possible to upgrade various parts at different times. The spectrum analyzer may be upgraded to 40 GHz today with only the necessary antennas to support the initial processor frequencies. As processor speed increases, the necessary antennas and cables may be purchased that support testing to the higher levels.

5.5.4 Spread Spectrum Clocking (SSC)

Spread Spectrum Clocking (SSC) is defined as continuously ramping or modulating the processor clock frequency over a predefined range (see Figure 22). SSC reduces radiated emissions by spreading the radiated energy over a wider frequency band (see Figure 23). Thus, instead of maintaining a constant system frequency, SSC modulates the clock frequency along a predetermined path or modulating profile. Figure 22 shows an example of a predetermined modulation frequency. The modulation frequency is usually selected to be larger than 30 KHz (above the audio band) and small enough not to upset system timings (less than 0.8% of the clock frequency). SSC has been demonstrated to reduce peak radiation levels effectively, making EMC compliance easier to achieve.

To conserve the minimum period requirement for bus timing, the SSC clock is modulated between f_{nom} and $(1-\delta)*f_{nom}$, where f_{nom} is the nominal frequency for a constant frequency clock. The 'δ' specifies the total amount of spreading as a relative percentage of f_{nom}. The modulation percentage is always a function of $1-\delta$ and not $1+\delta$, as increasing the clock frequency above the rated speed of the processor may cause unpredictable operation.

Figure 22. Spread Spectrum Modulation Profile
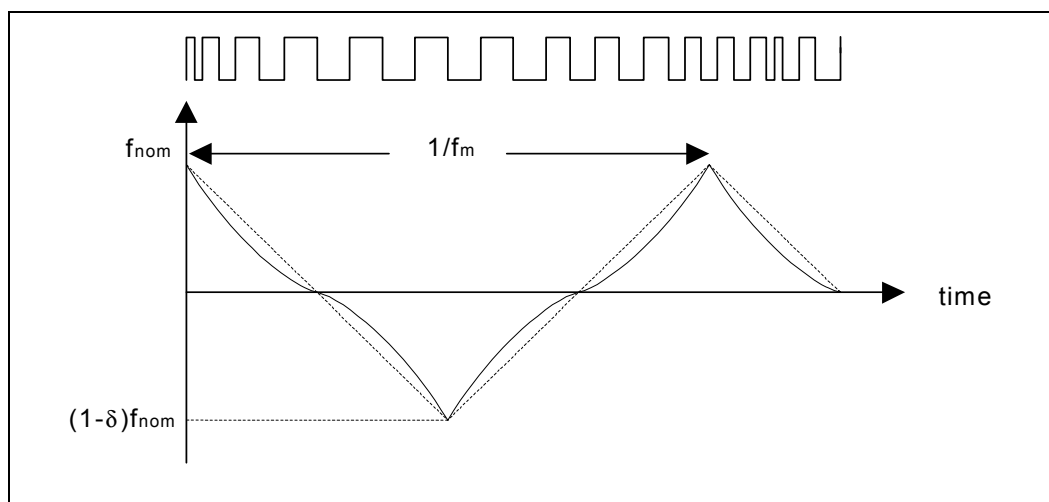
Figure 23. Impact of Spread Spectrum Clocking on Radiated Emissions
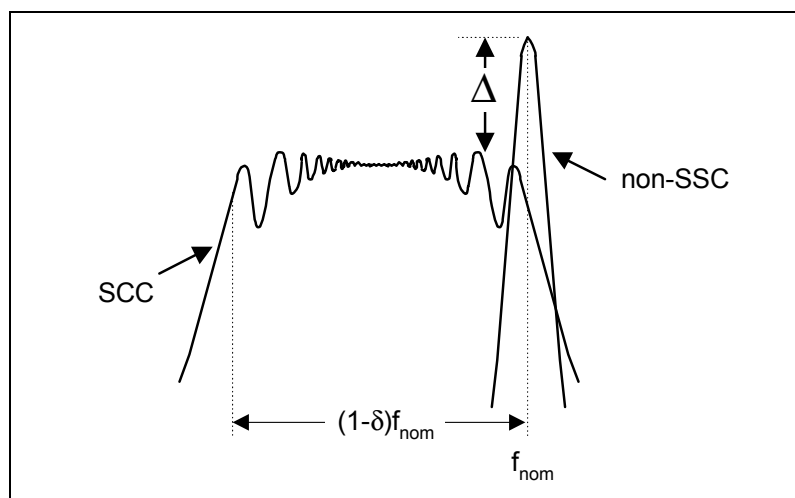
5.5.5   Differential Clocking

Differential clocking requires the clock generator supply both clock and clock-bar traces. Clock-bar has equal and opposite current as the primary clock and is also 180° out of phase. To maximize the benefit of differential clocking, both clock lines must be routed parallel to each other for their entire length. Devices connected to the clock must also be designed to accept both the clock and clock-bar signals.

EMI reduction due to differential clocking is caused by H-field cancellation. Since H-field orientation is generated by and is dependent upon current flow, two equal currents flowing in opposite directions and 180° out of phase may have their H-fields cancelled (see Figure 24). Lower H-fields may result in reduced EMI radiation.

Figure 24. Cancellation of H-fields Through Inverse Currents
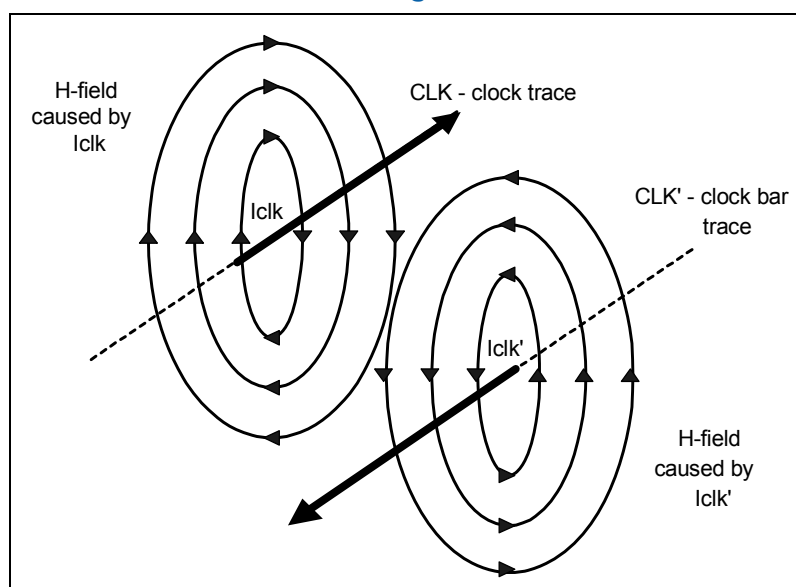
Differential clocking may also reduce the amount of noise coupled to other traces, which improves signal quality and reduces EMI. I/O signals are particularly important, because they often leave the system chassis (serial and parallel ports, keyboards, mouse, etc.) and radiate noise that has been induced onto them. A single-ended clock's return path is usually a reference plane, which is shared by other signals/traces. When noise is created on a single-ended clock, the noise may appear on the reference plane and may be coupled to I/O traces. A differential clock's return path is the clock-bar signal/trace, which is more isolated than the reference plane and minimizes potential I/O trace coupling.

For best results, the trace lengths and routing of the clock lines must be closely matched, and spacing between the two traces must be kept as small as possible. This minimizes loop area and maximizes H-field cancellation. In addition, the real and parasitic terminations of each signal of a differential pair must be the same. Also, the skew between the signal level transitions on the two lines must be small compared to the rise time of the level transitions.

Placing ground traces on the outside of the differential pair may further reduce emissions. Intermediate vias to ground may be needed to reduce the opportunity for re-radiation from the ground traces themselves. Distance between vias must be less than ¼ of a wavelength of the fifth harmonic of the processor core frequency.

5.6　Length Tuning

High-speed source synchronous interfaces have very small setup and hold windows. As a result, the signals as a group are very sensitive to skew. A common way to reduce skew is to tune all of the lengths such that the setup and hold windows have the same positional relationship. Length tuning is the matching of two or more signals' total flight time, within a tolerance, to center the setup and hold windows.

Length tuning has several key parameters: signal to be tuned, absolute minimum flight time, absolute maximum flight time, and tolerance. The absolute minimum and maximum flight times define the flexible solution space within which lengths may fall. For a signal to be properly tuned, it must fall within that solution space and be within the length tuning tolerance. Figure 25 shows the relationship of these parameters.

A tolerance is a value specifying how far off from exact is allowed. Typically, tolerance is specified in a specific direction, such as −1 ps or ± 2 ps.

Figure 25.　Length Tuning Parameters
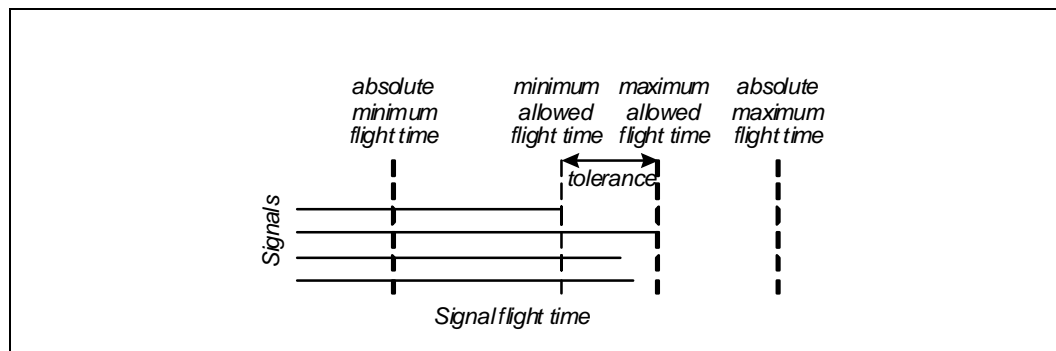
The minimum and maximum allowed flight times are at the end points of the tolerance window. The tolerance window may fall anywhere within the range between absolute minimum flight time and maximum flight time. The remainder of this section may refer to 'minimum allowed flight time' as 'minimum flight time' and may refer to 'maximum allowed flight time' as 'maximum flight time'.

5.6.1 Signal-to-Strobe Flight Time Relationships

High-speed interfaces are commonly latched off a strobe or a clock. Length tuning ensures that the required setup and hold times of the data signal to the strobe signal or clock signal are not violated due to motherboard routing effects. As a result, each data signal is length tuned with respect to the strobe signal or clock signal. This means that the data signals are all within tolerance of the strobe signal:

$$\text{Minimum\_Signal}_{\text{Flight Time}} = \text{Strobe}_{\text{Flight Time}} - \text{Tolerance}$$

$$\text{Maximum\_Signal}_{\text{Flight Time}} = \text{Strobe}_{\text{flight Time}} + \text{Tolerance}$$

Figure 26. Signal Length Solution Space with One Strobe
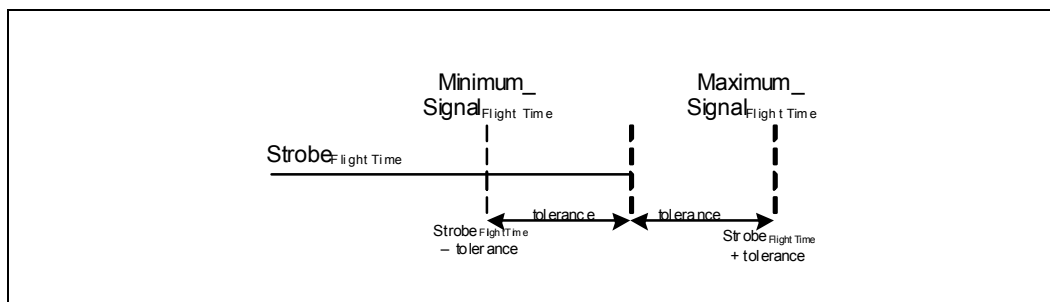
Some groups of high-speed signals need to be length tuned to two strobes or clocks. In this situation, all signals must be length matched to both strobes or clocks and the strobes or clocks must be length matched to each other as well.

$$\text{Minimum\_Signal}_{\text{Flight Time}} = \text{Longer\_Strobe}_{\text{Flight Time}} - \text{Tolerance}$$

$$\text{Maximum\_Signal}_{\text{Flight Time}} = \text{Shorter\_Strobe}_{\text{Flight Time}} + \text{Tolerance}$$

Figure 27. Signal Length Solution with Two Strobes
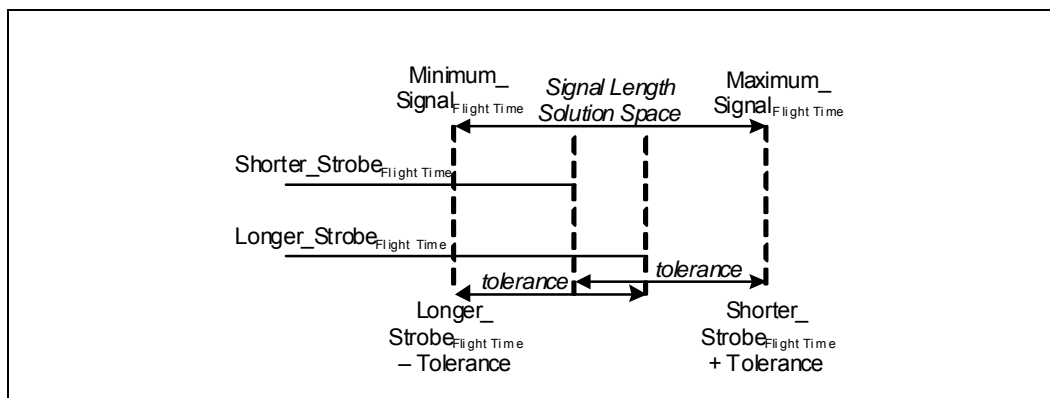
When the strobes are the furthest apart (that is, as far apart as allowed for signals of the same group), then their difference is the total allowed tolerance. This means that all signals must fall between them, or have a solution space, which is "tolerance" wide.

$$Longer\_Strobe_{Flight\ Time} = Shorter\_Strobe_{Flight\ Time} + Tolerance$$

$$Shorter\_Strobe_{Flight\ Time} = Longer\_Strobe_{Flight\ Time} - Tolerance$$

Figure 28.   Signal Length Solution Space with Furthest Apart Strobes
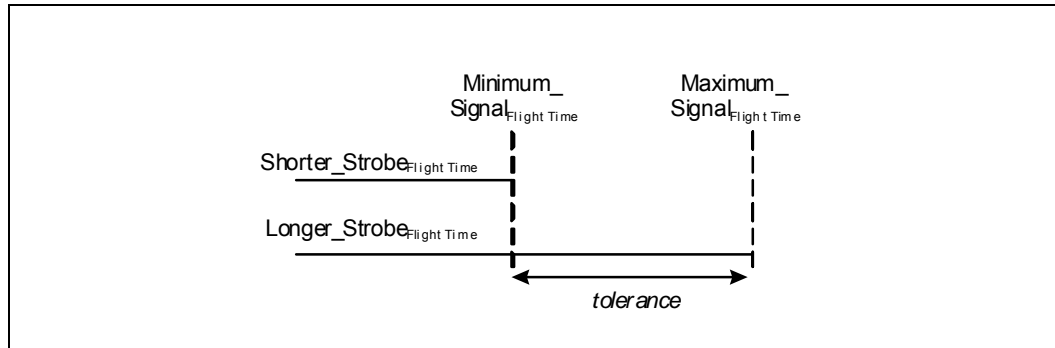
When the strobes have exactly the same flight time, then the signals have a solution space which is *2*tolerance wide*.

$$Strobe_{Flight\ Time} = Longer\_Strobe_{Flight\ Time} = Shorter\_Strobe_{Flight\ Time}$$

$$Minimum\_Signal_{Flight\ Time} = Strobe_{Flight\ Time} - Tolerance$$

$$Maximum\_Signal_{Flight\ Time} = Strobe_{Flight\ Time} + Tolerance$$

Figure 29.   Signal Length Solution Space with Matched Strobes
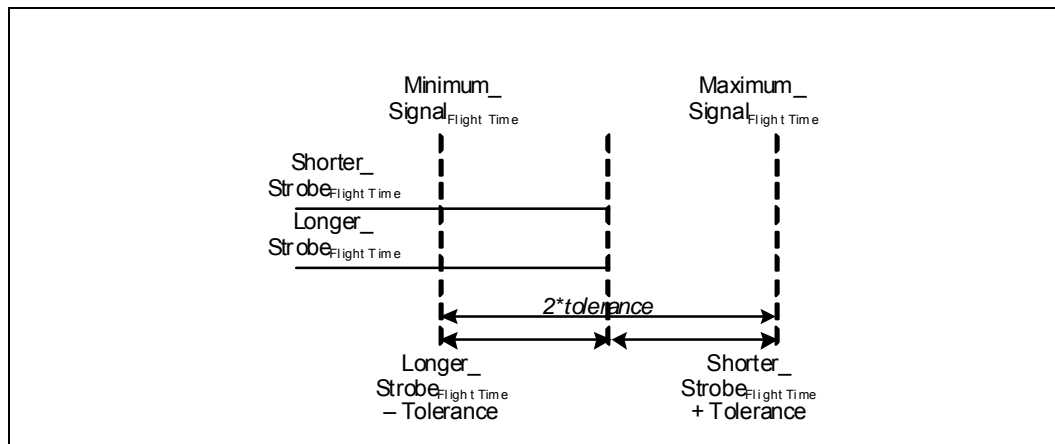
5.6.2   Flight Time Segment Analysis

Length matching often requires package compensating for differences in the package trace lengths of signals within the same strobe group. The "package trace length" is defined as the trace segment between the die pad and component package pin. To

compensate for package-induced skew, the signals lengths in the same group are adjusted by the exact amount of Package Length Compensation (PLC). Equation 1 defines PLC for a particular signal. Signal X is any signal in the group that does not have the longest package length. The PLC is realized by adding equal length PCB trace for signal X.

Equation 1. Package Length Compensation (PLC) Definition

$$SignalX_{PLC} = Maximum\_Signal\_in\_Group_{Package\ Length} - SignalX_{Package\ Length}$$

Every time a signal changes interconnect or layer, there is an effect on flight time. The most effective way to calculate flight time is to break up each signal into segments of constant flight time, analyze those segments, and then add the segments together.

Flight time is trace length divided by a constant trace velocity.

Equation 2. Flight Time

$$flight\_time = \frac{trace\_length}{trace\_velocity}$$

To determine the total flight time, each segment with a constant trace velocity must be identified. These segments are commonly defined at component interconnects. For example, a signal that connects two different components through a PCB would be calculated as follows:

$$Total\_Signal_{Flight\ Time} = Signal_{Component\ Flight\ Time} + Signal_{PCB\ Flight\ Time} +$$
$$Signal_{Component2\ Flight\ Time}$$

Figure 30. Total Signal Length with Two Components
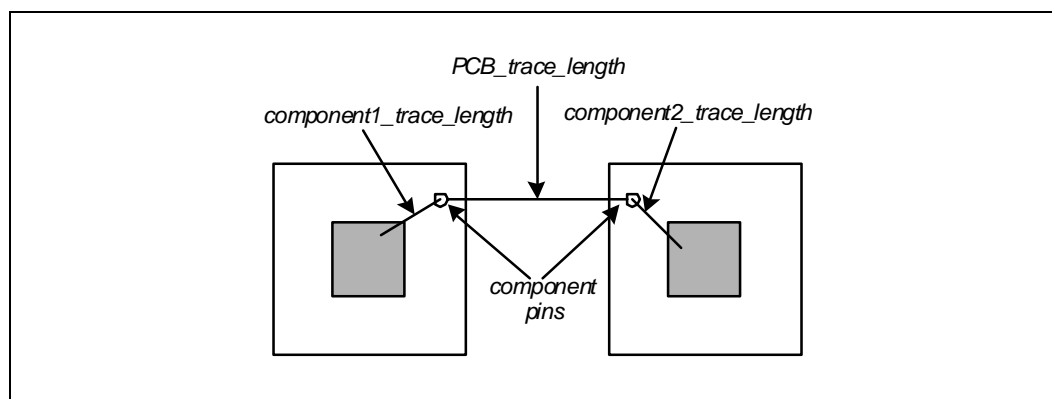
Using the segment lengths and velocities yields:

Equation 3. Total Flight Time

$$flight\_time = \frac{component1\_length}{component1\_velocity} + \frac{PCB\_length}{PCB\_velocity} + \frac{component2\_length}{component2\_velocity}$$

5.6.3   Bus Length Tuning Methodology

Many buses, such as memory and bus, require length tuning a group of signals. A common way to do this is by routing the bus first to determine what the approximate length range is, then picking an arbitrary signal. Sometimes this signal may be the most difficult one to route or adjust to tune. Using the PCB trace length for this signal, the solution space of remainder signals and strobes in the group can be determined.

Intel is able to provide a length tuning calculator spreadsheet. The calculator uses all the specific routing parameters specified in previous section (minimum and maximum lengths, tolerances, signal groups, and so on) to determine the solution space for the bus in question.

5.7   System Bus Tuning

Routing PCB system buses (for example, DDR2 memory bus) requires length matching within source synchronous groups. As a result, propagation-based length matching is used to account for the strobe-to-signal skew effects. Propagation-based length matching is described in the next section, followed by a routing example.

5.7.1   Compensating for Package Trace Length Differences

The first factor in length matching involves compensating for package trace length differences for signals within the same strobe group. The package trace length is defined as the trace segment between the die pad and component package pin. The package lengths on the processor and the EP80579 introduce skew between different signals as illustrated in the example given in Figure 31.

Note: Component A in Figure 31 represents a memory or I/O controller hub. This example uses a strobe and data signal, which happen to have the shortest and longest package trace lengths respectively.

Figure 31.   Package Trace Length Differences
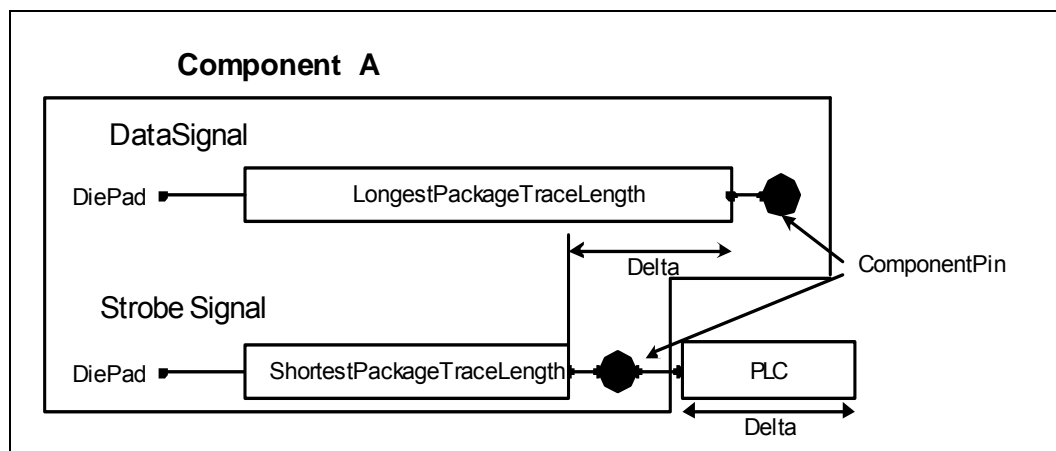
Each of the signals will have varying amounts of package skew. The amount of skew for a particular signal is based on the difference between that signal's package trace length and the longest signal's package trace length in the same signal group. For example, signals with shorter package length will have more package trace length compensation than signals with package lengths closer to the longest package trace.

To compensate for package-induced skew, all source synchronous motherboard trace lengths are adjusted by the exact amount of package length compensation (PLC). Equation 4 defines PLC for a particular signal. SignalX is any signal in the group that does not have the longest package length. This includes the strobe signals.

Equation 4. Package Length Compensation (PLC) Definition

$$\text{SignalX}_{PLC} = \text{Maximum\_Signal\_In\_Group}_{PackageLength} - \text{SignalX}_{PackageLength}$$

The signals with a package length less than the longest package trace in that group will require additional motherboard trace length equal to SignalX$_{PLC}$. Equation 4 yields a zero PLC for the signal with the longest package length, so the signal with the longest package length would require no amount of additional motherboard trace length. Figure 32 illustrates PLC using a data signal as the longest package trace and strobe signal as SignalX.

Figure 32. Example of PLC Compensation on the Motherboard
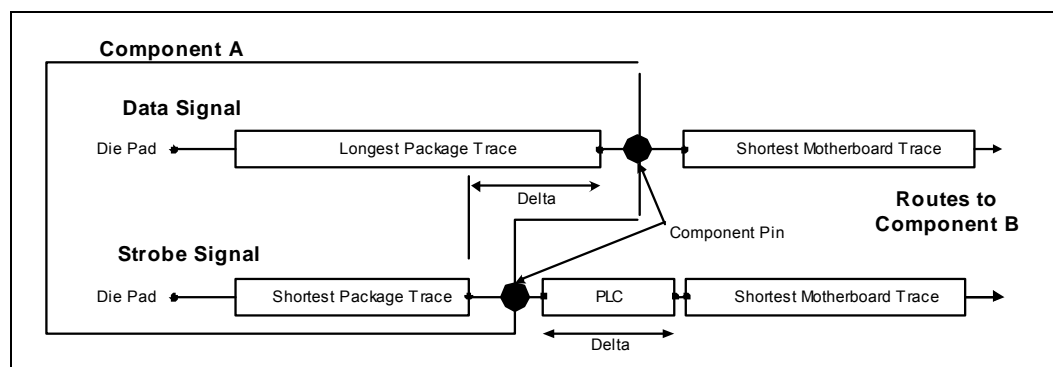
5.8 Common Layout Pit-Falls

This section describes common high speed issues found when laying out a PCB. Examples will be provided to aid the board developer in avoiding these issues. The signals described in this section pertain to high speed signals, such as those found on the system bus, memory bus, etc.

5.8.1 Signal Parallelism

To minimize high-speed signal induced noise or cross-talk, limit or do not route signals on adjacent layers parallel to each other. Figure 33 shows the proper and improper methods for routing signals on adjacent layers.

Figure 33.   Signal Parallelism

Proper adjacent layer signal routing

Improper adjacent signal layer routing
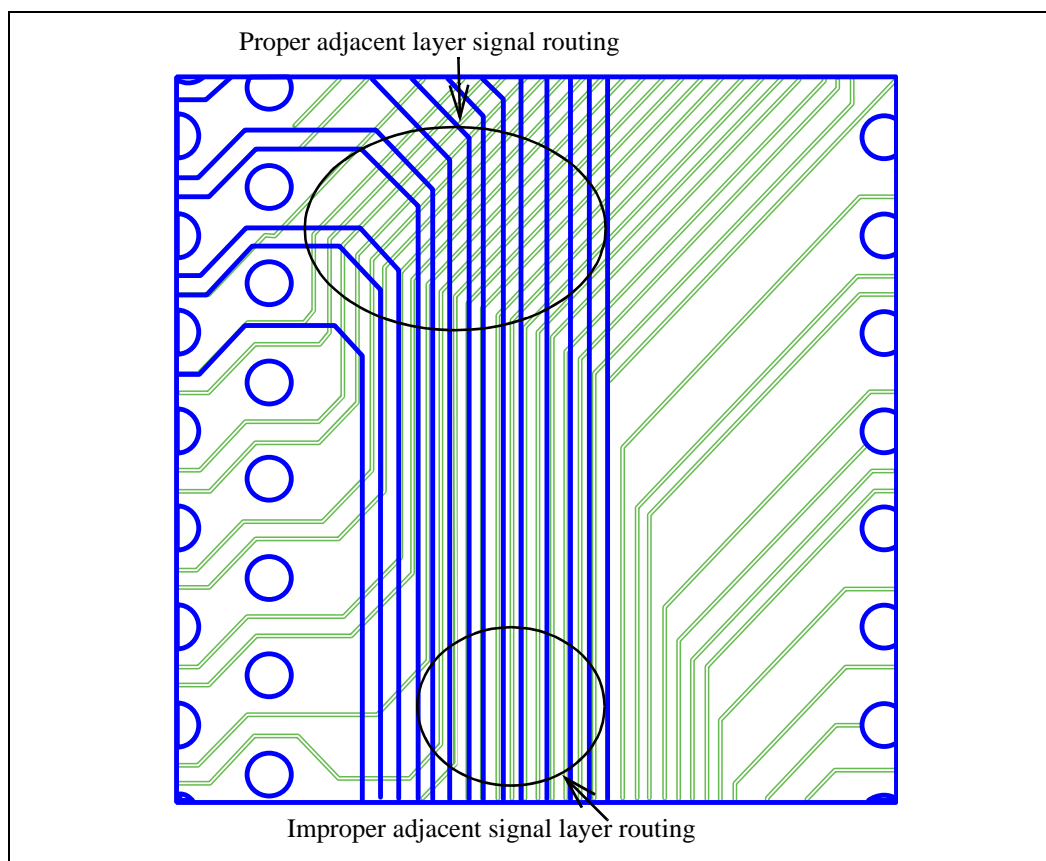
5.8.2 Via Sharing

To minimize inductance/impedance, traces must not share vias. Figure 34 shows the improper method of via sharing. Figure 35 shows an proper method of how to connect the vias.

Figure 34.   Improper Via Sharing

Via shared by C808 and C726
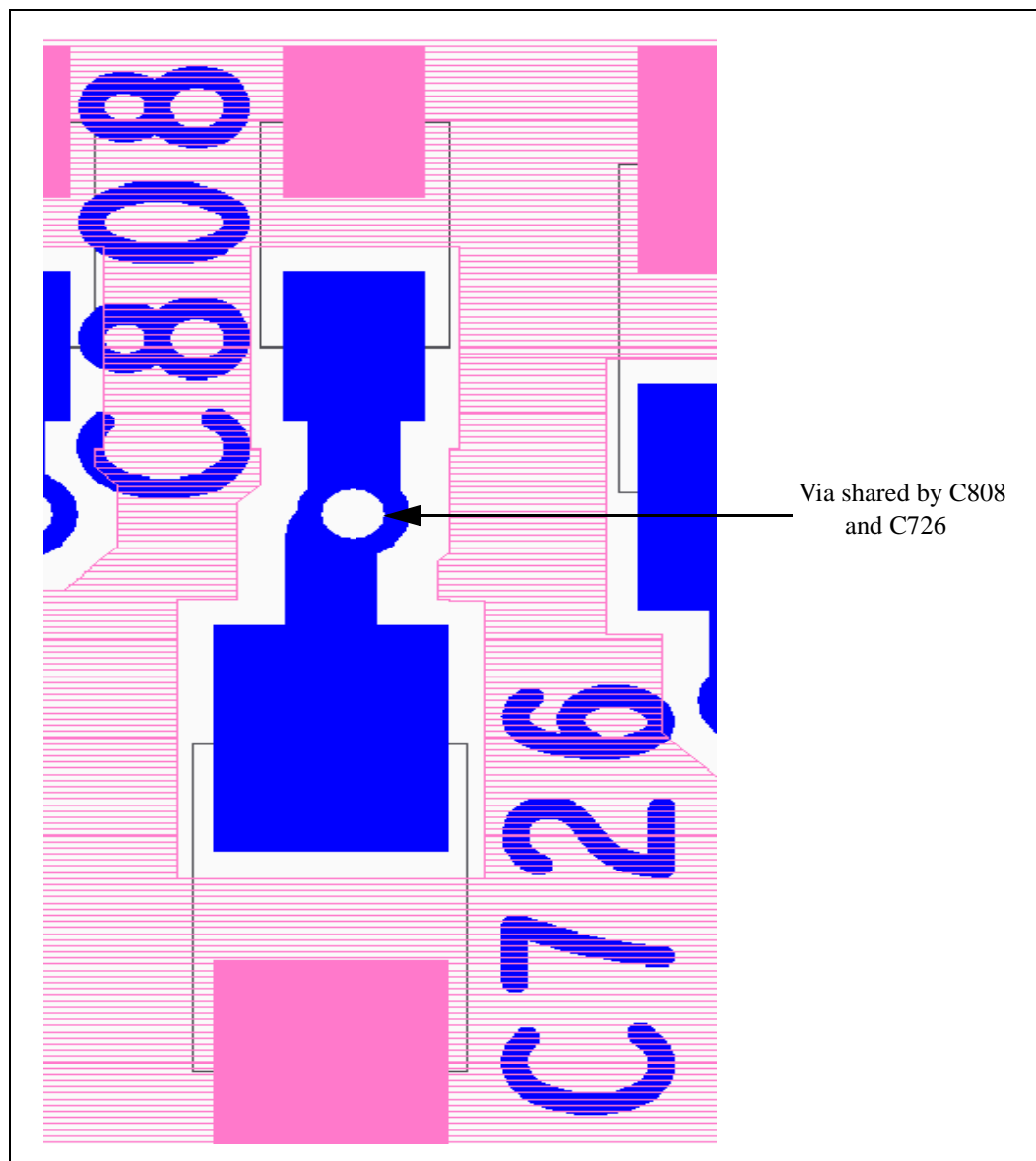
Figure 35. Correct Via Connections

C808 and C726 corrected to have their own vias
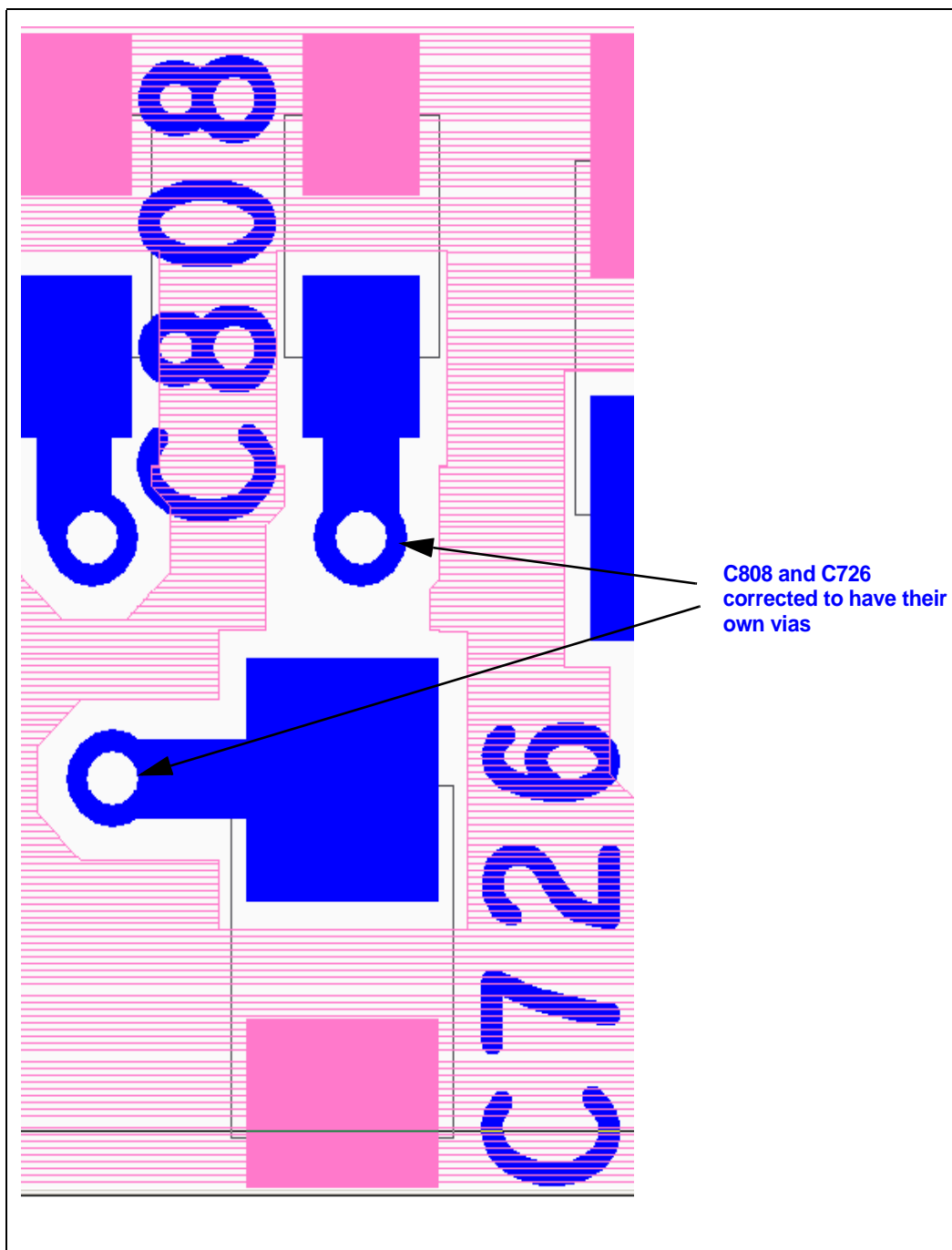
5.8.3 Necking Down

To maintain the current carrying capacity of a thicker power/ground trace, do not neck the trace down. When a trace is necked down, the entire trace essentially takes on the current carrying capacity of the narrowest width, decreasing the current capacity effect

of the thicker traces. Figure 36 shows the improper method of necking down. To correct this issue, the same trace may be routed on several different layers and connected by an adequate amount of vias. A second option is shown in Figure 37. This method doubles the narrow trace to correct the neck down.

Figure 36.   Improper Necking Down

Trace necked down
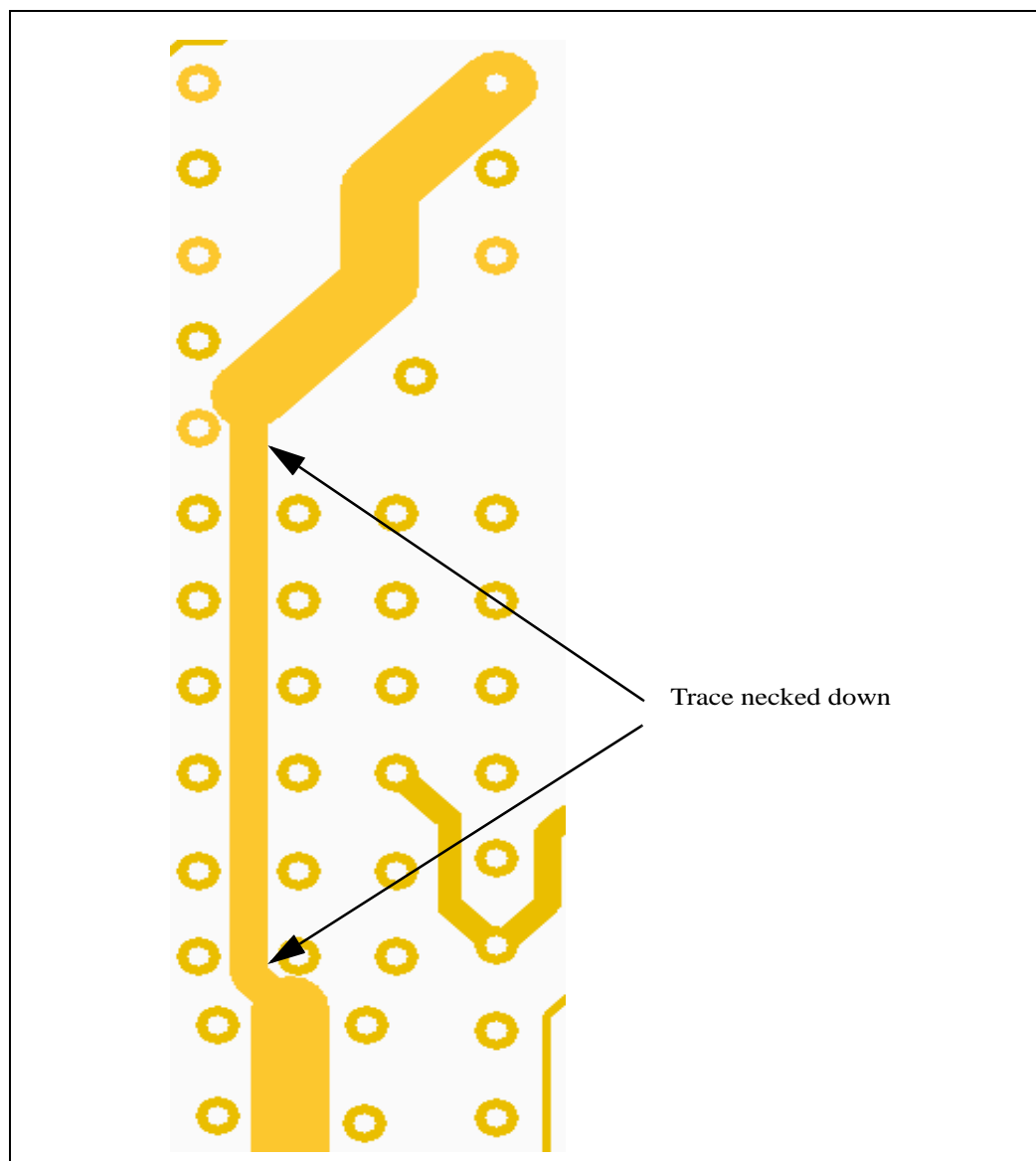
Figure 37.   Correct Necking Down

Neck down corrected by adding additional trace. Traces are equal in length and width.
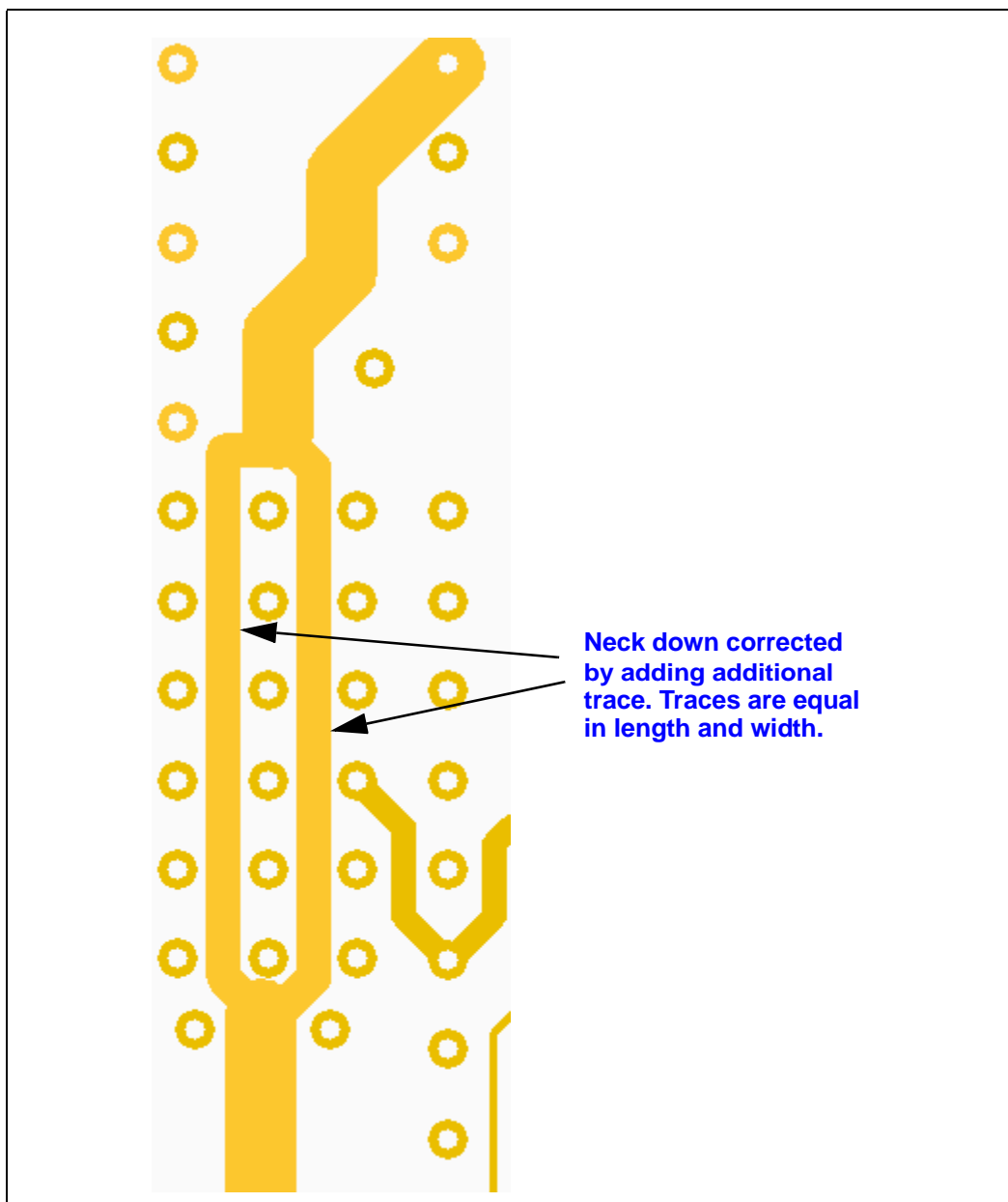
5.8.4 Signals Crossing Plane Splits

Signals that cross an adjacent layer's plane boundary are undesirable for two reasons:

- The return current that runs in the reference plane wants to share its current with the adjacent layer's reference plane it just crossed over. The return current now has to find a return path on the adjacent layer which will cause signal delay.

- The impedance of the trace will change each time it crosses a plane.

Figure 38 shows the improper method of signals crossing the adjacent layer's plane boundaries. Signal routing is done on layer 2, while layer 1 (striped area) contains power and ground. Signals must be routed in a way to avoid this issue, such as routing on a different layer or repositioning the signals to avoid the adjacent layer's plane boundary.

Figure 38. Signal Crossing Plane Splits
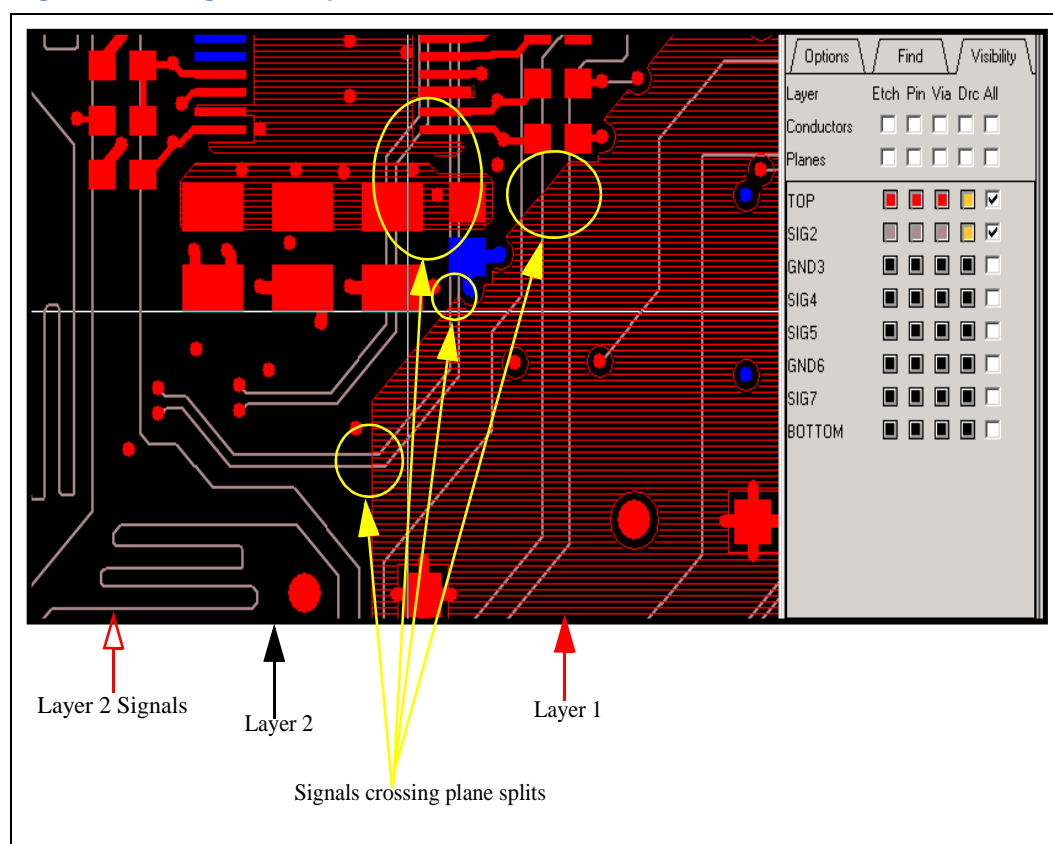
6.0 System Power Delivery Guide

This chapter provides an example for board power delivery of an EP80579-based platform design. It provides the requirements and implemention of power sources for system board designs.

Note: There are many power delivery system implementations other than the example described in this chapter.

6.1 Terminology and Definitions

Table 8.   Terminology

Term	Definition
Full Supply	The external voltages and tolerances required to operate a component.
Full Plane	A group of like voltages connected to a particular power supply
Full Well	Power planes which operate in normal and power management states
Power Rails	An ATX power supply has six power rails: +12V, −12V, +5V, −5V, +3.3V, and +5 VSBY. In addition to these power rails coming off the power supply, several other power rails are created by voltage regulators on the Development Board. The -12V and −5V power rails are unused on the Development Board.
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered. This state is used in the Development Board to satisfy the S3 ACPI power management state. S3 Cold - Classic S3 STR State S3 Hot is not supported.
Full-power	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state (S0) and the S1 (CPU stop-grant state) state.
Suspend Operation	During suspend operation, power is removed from some components on the motherboard.
Core Power	Core power refers to a power rail that is only on during full-power operation. These power rails are on when the active-low PSON# signal is asserted to the ATX power supply. The core power rails that are used directly from the power supply are: +12V, +5V, and 3.3V.
Standby Power Rail	A power rail that is on during suspend operation (these rails are also on during full power operation) is a standby power rail. These rails may be on at all times as soon as the power supply is plugged into AC power. The only standby power rail that is distributed directly from the ATX power supply is +5 VSBY. The other standby rails on the motherboard are created by voltage regulators.
Derived Power	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator.
Dual Power Rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from standby supply during suspend operation and derived from a core supply during full-power operation.
VRM and VRD	VRM stands for Voltage Regulator Module. VRD stands for Voltage Regulator Down.

6.2 Power Supply

Power planes or shapes should be used for the major voltages shown in this section. The functional blocks are powered by the voltages shown in Table 9.

Note: The EP80579 is a large chip and may have interfaces that are not located near each other, although they are powered by the same voltage.

These voltages are not necessarily connected in the package or on the silicon. Their source voltage may be the same voltage plane on the baseboard, but they need to be considered separate for decoupling purposes on the board. The decoupling needs are presented based on these functional blocks.

Table 9.   Power Supply Pins (Sheet 1 of 2)

Well	Development Board Voltage Rail	EP80579 Power Pin Name	Supply Types	Description
Core	1.0V or 1.3V	VCCVC	IA-32 core	VC power
	1.2V	VCCA[1]	IA-32 core	VC PLL1 power
		VCCA[2]	IA-32 core	VC PLL2 power
	1.2V	VCC	CRU, DDR2, Expansion Bus, GbE, IMCH, IICH, PCI Express, SATA	Core logic power
		VCCUSB12	USB2	Digital power
		VCCAUSB12	USB2	Analog power
		VCCAPE0PLL12	PCI Express	PLL digital power
		VCCAPE	PCI Express	Transmitter analog power
		VCCRPE	PCI Express	Receiver digital power
		VCCAPLL	SATA	Analog PLL power
		VCCARX	SATA	Analog receiver power
		VCCATX	SATA	Analog transmitter power
		VCCSATA	SATA	SATA power
		VCCAHPLL	CRU	Analog PLL power
	0.9V (DDR2)	VTTDDR	DDR2	DDR2 reference
	1.8V (DDR2)	VCC18	DDR2	DDR2 IO power
		VCCTMP18	Thermal Sensor	Thermal sensor power
	2.5V	VCC25	GbE	GbE IO
	3.3V	VCC33	CRU, Expansion Bus, IMCH, IICH, MISC IO	I/O power
		VCCGBE33	GbE	3.3V tolerance reference
		VCCSATA33	SATA	SATA power
		VCCABGP033	PCI-Express	Analog bandgap power
		VCCABG3P3_USB	USB2	Analog bandgap power
		VCCASATABG3P3	SATA	Analog bandgap power
	5V	VCC50	N/A	N/A

Table 9.   Power Supply Pins (Sheet 2 of 2)

Well	Development Board Voltage Rail	EP80579 Power Pin Name	Supply Types	Description
Suspend	1.2V	VCC1P2_USBSUS	USB2	1.2V USB sustain power
		VCCSUS1	IMCH_PAD	RTC core sustain power
	2.5V	VCCSUS25	GbE	Sustain GbE power
	3.3V	VCCPSUS	USB2, IMCH	USB sustain power, RTC IO sustain power
		VCCGBEPSUS	GbE	Sustain 3.3V tolerance reference
	5V	VCC50_SUS	N/A	N/A
RTC	3.3V	VCCPRTC	IMCH	Real Time Clock power
GND	Analog Ground	VSSA	Ground	Analog Ground
GND	Ground	VSS	Ground	Ground

6.3   Power Planes

Table 10 summarizes the Development Board power supply interconnect to the EP80579 power pins.

Table 10.   Power and Ground Planes (Sheet 1 of 2)

Development Board Signal Name	EP80579 Power Pin Name	Description
IA-32 core Power Supply Pins		
VCC_CPU	VCCVC	Power Supply (1.0V - 1.3V) for IA-32 core • 1.0V when operating at 600 MHz • 1.3V when operating at 1.066 GHz • 1.3V when operating at 1.2 GHz
VCCA[2:1]	VCCA[2:1]	1.2V CPU core **PLL Analog** Voltage
Core Logic Power Supply Pins		
V1P2	VCC	1.2V supply pins for core logic (CRU, EXP_Bus, GbE, IICH, IMCH, SATA, PCI Express)
VCC3	VCC33	3.3V supply for all 3.3V I/O functions which are not dedicated to their own power rail. The units using this rail include: IMCH, Global Clock/Reset(CRU), USB, CAN, EXP_Bus, SATA, and GbE.
VCC	VCC50	5V power supply for 5V tolerance units. (IICH, CRU, CAN, and EXP_Bus
V2P5	VCC25	2.5V supply for GbE unit.
DDR2 Unit Power Supply Pins		
V1P8_DDR	VCC18	1.8V power supply for DDR2 I/O
DDR2_VTT	VTTDDR	0.9V DDR2 Reference Voltage (Vref)
Suspend/Resume Power Supply Pins		
VSBY1_2	VCCSUS1 VCC1P2_USBSUS	1.2V power pins for the resume well GbE, USB, and IICH core logic. This power is not expected to be shut off unless the system is unplugged.

Table 10.   Power and Ground Planes (Sheet 2 of 2)

Development Board Signal Name	EP80579 Power Pin Name	Description
VSBY3_3	VCCPSUS VCCGBEPSUS	3.3V power pins for the resume well USB, IICH and GbE I/O buffers. This power is not expected to be shut off unless the system is unplugged.
VSBY2_5	VCCSUS25	2.5V power for the resume well GbE core logic. This power is not expected to be shut off unless the system is unplugged
VSBY5	VCC50_SUS	5.0V power for 5V tolerance in the sustain well I/Os. This power is not expected to be shut off unless the system is unplugged
Battery Power (RTC)		
V_3P0_BAT-VREG	VCCPRTC	3.3V Power Supply for the RTC Well. Voltage can drop to 2.0V if all other planes are shut off. This power is not expected to be shut off unless the RTC battery is removed or drained.
Analog Power Supply Pins (All Analog Power Pins should be filtered)		
SATA Analog Voltages		
VCCARX	VCCARX	1.2V Analog Power for SATA AFE Receiver
VCCATX	VCCATX	1.2V Analog Power for SATA AFE Transmitter
VCCSATABG3P3	VCCSATABG3P3	3.3V Bandgap Power for SATA AFE Reference Circuitry
VCCAPLL	VCCAPLL	1.2V Analog Power for SATA PLL. ***Note:*** This supply is required even if the SATA interface is not used.
USB Analog Voltages		
VCCABG3P3_USB	VCCABG3P3_USB	3.3V Bandgap Power for USB AFE Reference Circuitry
USBVCC_1P2_APLL	VCCAUSB12	1.2V Analog Power for USB PLL. *This voltage is required even if USB is not used.*
PCI Express Analog Voltages		
VCCABGP033	VCCABGP033	3.3V PCI Express Bandgap Power supply
VCCAPE0PLL12	VCCAPE0PLL12	1.2V Analog Power for PCI Express PLL.
CRU Analog Voltages		
VCCAHPLL	VCCAHPLL	1.2V Analog Power for CRU PLL

6.4   Power Requirements

This section describes the power requirements for the EP80579. Figure 39 shows a block diagram of the power delivery implementation on the Development Board. Table 11 provides the definitions for the voltages specified in Figure 39. Many other power delivery methods can achieve similar results; however, it is critical to consider the effects if deviating from the example shown below.

Figure 39.   Development Board Power Delivery Implementation

EP80579 Development Board Power Delivery Block Diagram
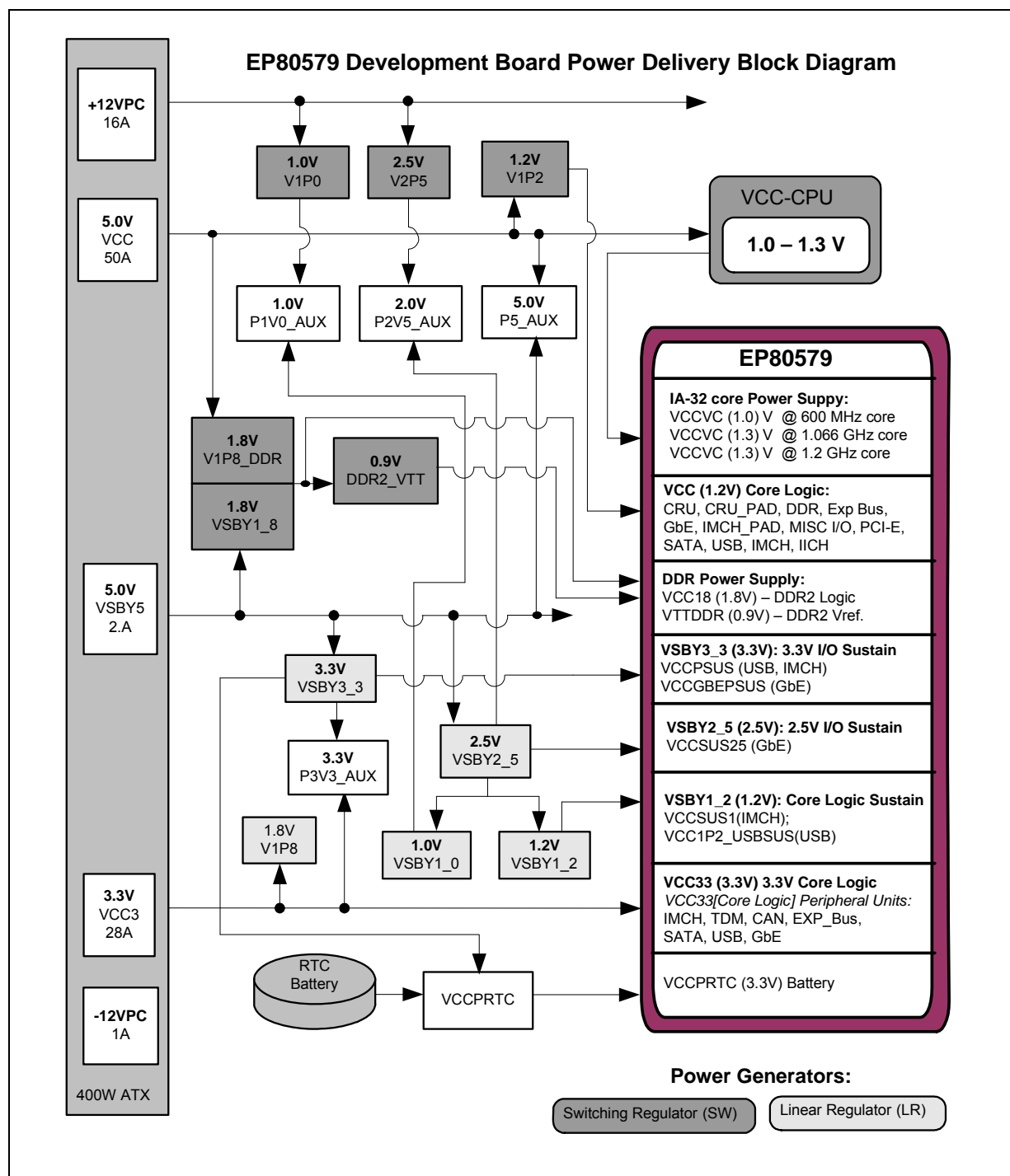
Note: The Development Board power delivery configuration shown is only an example. Many power distribution methods achieve similar results. It is critical, when deviating from these examples in any way, to consider the effects of the change. See Table 11 for Voltage Definitions.

Table 11.   Development Board Power Delivery Voltage Definitions

Development Board Power Rail Signal Name	Definition
VSBY5	5V Standby
VSBY3_3	3.3V Standby
VSBY2_5	2.5V Standby
VSBY1_2	1.2V Standby
VSBY1_0	1.0V Standby
P5_AUX	5V Auxiliary
P3V3_AUX	3.3V Auxiliary
P2V5_AUX	2.5V Auxiliary
P1V0_AUX	1.0V Auxiliary
VCC3	3.3V
VCC	5.0V
V1P0	1.0V
V2P5	2.5V
V1P2	1.2V
V1P8_DDR	1.8V for DDR2
DDR2_VTT	0.9V DDR2 Vref
V1P8	1.8V for on-board devices (HSS, FLASH, etc.)
VCC_CPU	1.0V - 1.3 V for IA-32 core

6.5   Power Delivery Guidelines

The following guidelines are recommended for optimal EP80579 power delivery. The main focus of these guidelines is to minimize power noise and signal integrity quality. The guidelines are not intended to replace thorough system validation of products.

6.5.1   IA-32 core Power (VCC_CPU)

This supply provides the voltage for the IA-32 core. The voltage plane ranges from 1.0V - 1.3V based on the core frequency. The Development Board uses a Pulse Width Modulator (PWM) controller-based switching voltage regulator design to provide the IA-32 core power. The IA-32 core has its own independent voltage regulator and the design is Voltage Regulator-Down on the motherboard (VRD). The VRD is powered by +5V from the ATX power supply.

6.5.1.1   IA-32 core Bus Frequency and Power Select

The IA-32 core voltage is controlled by two signals (BSEL & V_SEL) from the EP80579. The BSEL and V_SEL signals are driven by EP80579 to reflect the internal strapping of the various EP80579 SKUs. The BSEL/V_SEL encodings should be interpreted to generate the required CPU voltage as shown in Table 12. The V_SEL signal is an open-

drain (OD) I/O, hence, it requires an external 10K pull-up. It should be noted that the V_SEL signal can also be pulled down to GND to configure a 1.2GHz SKUed part (BSEL/V_SEL = "11") to operate as a 1.066GHz SKUed part (BSEL/V_SEL = "10").

Table 12. **IA-32 core Frequency and Power Select (BSEL/V_SEL)**

SKU ID	Manufacturing Frequency SKU (FSB/Intel Architecture MHz)	BSEL Value	V_SEL Value	Operating Frequency (FSB/IA-32 core MHz)	IA-32 core Voltage
5/6	533/1200	1	1	533/1200	1.30V
	533/1200	1	0	533/1066	1.30V
3/4/7	533/1066	1	0	533/1066	1.30V
--	--	0	1	Reserved	--
1/2/8	400/600	0	0	400/600	1.0V

6.5.2 Core Logic Voltage (V1P2)

The V1P2 (1.2V) power plane is derived from the 5V power rail delivered by the power supply unit through a switching regulator. It powers the EP80579 core logic and the I/O buffer cells for SATA, PCI Express, and Expansion Bus interfaces.

6.5.3 DDR2 Voltage (V1P8_DDR)

The V1P8_DDR (1.8V) power plane is used to provide power to the DDR2 DRAM core and the DDR2 I/O ring. The V1P8_DDR power plane is created using a combination of a switching and linear regulator. The regulator switches between a switching power supply in S0 state and a linear regulator in S3 state. The switching regulator required for S0 receives its input directly from the 5V power rail from the ATX power supply unit. The linear regulator receives its input directly from the 5V Standby Voltage output (VSBY5) from the ATX power supply unit.

6.5.4 DDR2 Termination Voltage (DDR2_VTT)

The DDR2_VTT (0.9V) is for the DDR2 termination voltage. The input voltage for the DDR2_VTT regulator must come from the 1.8V DDR (V1P8_DDR) core regulator. The VTT voltage regulator is a switching regulator that regulates the 1.8V DDR2 core voltage down to the 0.9V reference voltage +/- 40mV. This provides common mode noise rejection between the DDR2 termination and I/O voltages.

6.5.5 1.8V Voltage (V1P8)

The V1P8 (1.8V) is a 1.8V power supply isolated from the V1P8_DDR. This voltage is used by the on-board components (Flash, HSS) that require 1.8V power supply but cannot be connected to the DDR2 power supply. The V1P8 power plane is derived from the 3.3V power rail delivered by the power supply unit through a linear regulator.

6.5.6 GbE 2.5V (V2P5)

The V2P5 (2.5V) power plane is derived from the +12V power rail delivered by the power supply unit through adjustable shunt regulators. This voltage is used by the GbE controller and LAN transceivers.

6.5.7 3.3V (VCC3)

The VCC3 (3.3V) power plane comes directly from 3.3V power rail delivered by the power supply. This power plane is used for all 3.3V I/O functions that are not dedicated to their own power rail. The plane provides power for the following interfaces:

- VCC3: Used for internal logic (ICH, CAN, SSP, SATA, GbE, Expansion Bus)
- VCCABGP033: Bandgap for internal PCI-Express
- VCCABG3P3_USB: Bandgap for internal USB logic
- VCCSATABG3P3: Bandgap for internal SATA logic

6.5.8 5V Voltage (VCC50)

The 5V power plane is connected directly to the +5.0V power rail delivered by the ATX power supply unit. This plane is responsible for allowing 5V tolerance on some input pins.

6.5.9 VCCRTC Reference

This is the 3.3 VSBY3_3 supply for the RTC well pin. The 3.3V can drop to 2.0V min. in G3 state. This power is not expected to be shut off unless the RTC battery is removed or completely drained.

6.5.10 Standby Voltages

6.5.10.1 2.5V Standby (VSBY2_5)

The VSBY2_5 is derived from the 5V Standby (VSBY5) power rail delivered by the ATX power supply unit through a linear regulator. This rail provides power to the 2.5V resume I/O logic.

6.5.10.2 1.2V Standby (VSBY1_2)

The VSBY1_2 is derived from the VSBY5 power rail delivered by the ATX power supply unit through the VSBY2_5 linear regulator and a 1.2V linear regulator. This rail provides power to the 1.2V resume I/O logic.

6.5.10.3 1.0V Standby (VSBY1_0)

The VSBY1_0 is derived from the VSBY5 power rail delivered by the ATX power supply unit through the VSBY2_5 linear regulator and a 1.0V linear regulator. This rail provides power to the PCI Express switch and GbE LAN resume I/O logic.

6.5.10.4 3.3V Standby (VSBY3_3)

The VSBY3_3 is derived from the 5V Standby (VSBY5) power rail delivered by the ATX power supply unit through a linear regulator. This rail provides power to the 3.3V resume I/O logic.

6.5.10.5 5.0V Standby (VSBY5)

The VSBY5 power plane comes directly off the 5V VSBY power rail from the ATX power supply and has three functions. First, it provides power to component resume logic and wake capable devices (e.g., USB, LAN, etc.). Second, it supplies power to the 1.8V regulator, which supplies power to the memory devices during S3. Third, the VSBY5 is

typically used to derive other stand-by power planes (e.g., 3.3 VSBY, 2.5 VSBY, etc.) on the Development Board. The power supply should be capable of handling at least 2A of continuous standby current and at least 2.5 A of peak standby current.

Note: To ensure that enough power is available during Suspend-to-RAM (STR), a thorough power budget should be completed. The power requirements should include each device's worst case power consumption, both in suspend and in full power modes. The power requirements should be compared with the power budget supplied by the power supply.

6.5.11 Auxiliary Voltages

6.5.11.1 PCI Express 3.3V Vaux Voltage (P3V3_AUX)

The P3V3_AUX power plane is the output of the VSBY5-to-3.3V Auxiliary Power (P3V3_AUX) voltage regulator. The 3.3 Vaux rail powers the PCI Express Switch and PCI Express slots' Vaux pins.

6.5.11.2 GbE LAN 2.5V Vaux Voltage (P2V5_AUX)

The P2V5_AUX power plane is the output of VSBY2_5-to-2.5V Auxiliary Power (P2V5_AUX) voltage regulator. The 2.5 Vaux rail powers the GbE LAN 2.5V Vaux pins.

6.5.11.3 GbE LAN 1.0V Vaux Voltage (P1V0_AUX)

The P1V0_AUX power plane is the output of VSBY1_0-to-1.0V Auxiliary Power (P1V0_AUX) voltage regulator. The 1.0 Vaux rail powers the GbE LAN 1.0V Vaux pins.

6.6 Component Power Distribution Guidelines

Large current swings can cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of capacitance is added to the various power rails. For prototype board designs, the designer should include pads for extra power plane decoupling caps.

6.6.1 IA-32 core Power Distribution Guidelines

6.6.1.1 IA-32 core Power Requirements

The system board designer should properly place high-frequency and bulk-decoupling capacitors as needed between the voltage regulator and processor to ensure the voltage fluctuations remain within the core voltage specifications.

The IA-32 core requires local regulation due to its higher current requirements, and to maintain power supply tolerance. For example, an on-board DC-to-DC converter converts a higher DC voltage to a lower DC voltage using a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R). More importantly however, an on-board regulator regulates the voltage locally, which minimizes DC line losses by reducing motherboard resistance on the core voltage.

6.6.2 General Switching Power Supply Design Recommendations

In a single-phase topology, the duty cycle of the control (top) MOSFET (see Figure 40) is roughly the ratio of the output voltage and the input voltage, and the bottom phase is not implemented. Due to the small ratio between V_{CC} and V_{DC} the duty cycle of the control MOSFET is very small. The main power loss in the control MOSFET is therefore

due to the transition or switching loss as it switches on and off. To minimize the transition loss in the control MOSFET, its transition time must be minimized. This is usually accomplished with the use of a small-size MOSFET. Or similarly, the duty cycle of the Synchronous MOSFET is very large; hence, to minimize the DC loss of the Synchronous MOSFET, its R_{DS-ON} must be small. This is usually accomplished with the use of a large-size MOSFET or several small-size MOSFETs connected in parallel. However, this solution typically leads to shoot-through current as it is quite difficult to minimize the effect of the Gate-Glitch phenomenon in the Synchronous MOSFET due to the C_{GD} charge coupling effect. Therefore, it is necessary to go to a multi-phase topology (Figure 40). In a multi-phase topology, the output load current is sourced from multiple sources or output stages. The term multi-phase implies the phases or stages are out of phase with respect to each other. For example, in a dual-phase topology, the stages are exactly 180° output of phase.

Note: The Development Board implements only the single-phase topology for the switching regulators. Where necessary, multiple MOSFETS are used to increase the output current.

Figure 40. Voltage Regulator Multi-Phase Topology Example
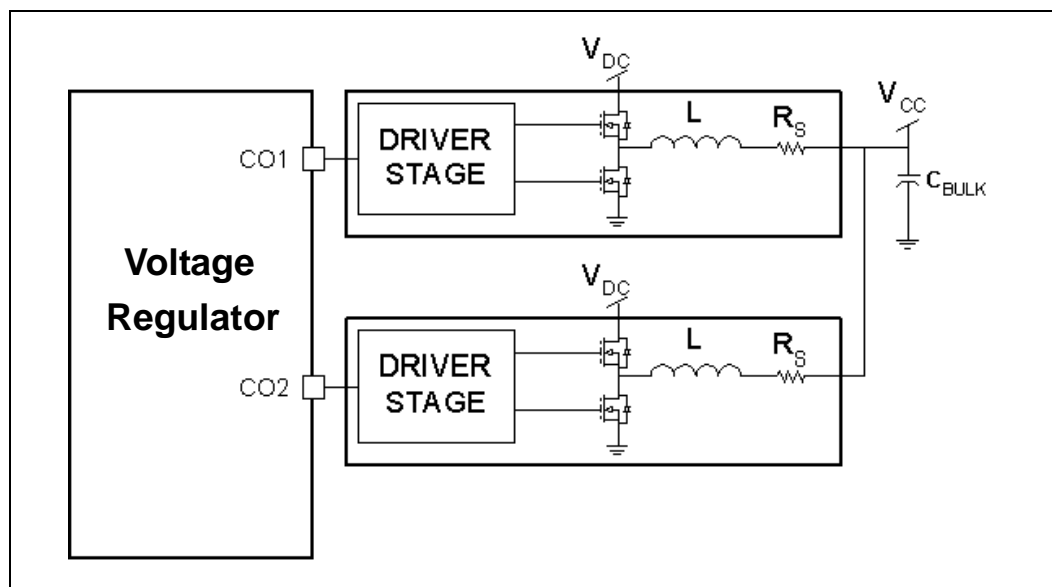
6.6.3 Voltage Regulator Design Recommendations

When laying out the processor power delivery circuit using a traditional Buck Voltage Regulator on a printed circuit board, the example shown in Figure 41 must be followed.

Figure 41. **Buck Voltage Regulator Example**
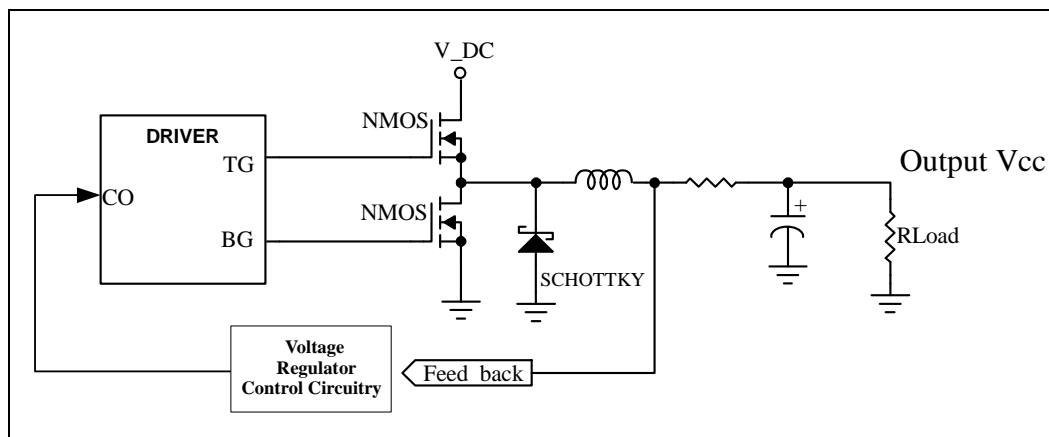
6.6.3.1 High Current Path, Top MOSFET Turned ON

The dashed/arrow line in Figure 42 indicates the high current path when the top MOSFET is ON. Current flows from the V_DC power source through the top MOSFET (there may be more than one of these), the inductor and sense resistor, and finally, the processor, R_{Load}, to ground. The components and current paths shown must be able to not only carry the high current through the processor, but the power source and ground must also be adequate.

Figure 42. **High Current Path With Top MOSFET Turned ON**
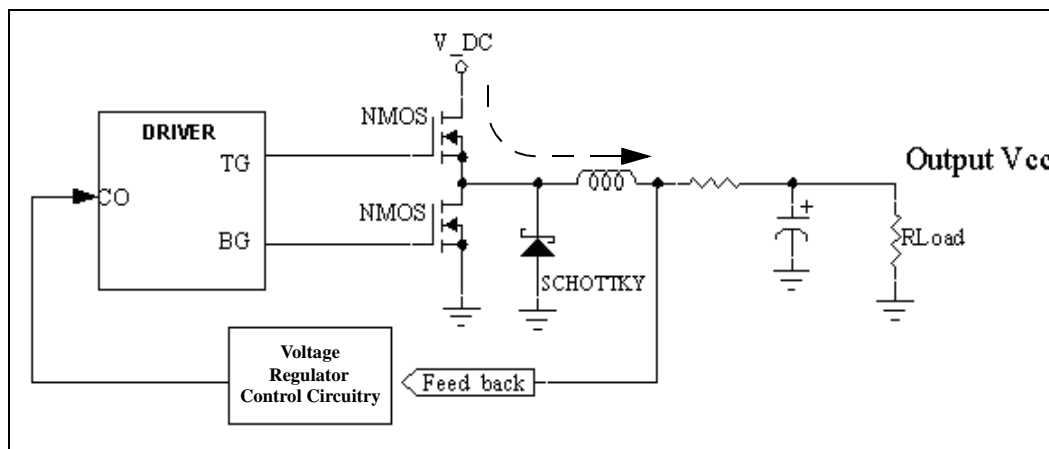
6.6.3.2 High Current Paths During Abrupt Load Current Changes

During abrupt changes in the load current, the bulk and decoupling capacitors must supply current for the brief period before the regulator circuit may respond. The dashed/arrow line in Figure 43 illustrates this current path. Stray inductance and resistance become a major concern and when they are not minimized, as they may compromise the effectiveness of the capacitors. Bulk capacitors for Vcc must be located at the highest current density points. These high-density points are located along the shortest route between the processor core and the sense resistor. Using short, fat traces or planes may minimize both stray inductance and resistance.

Figure 43.   High Current Path During Abrupt Load Current Changes
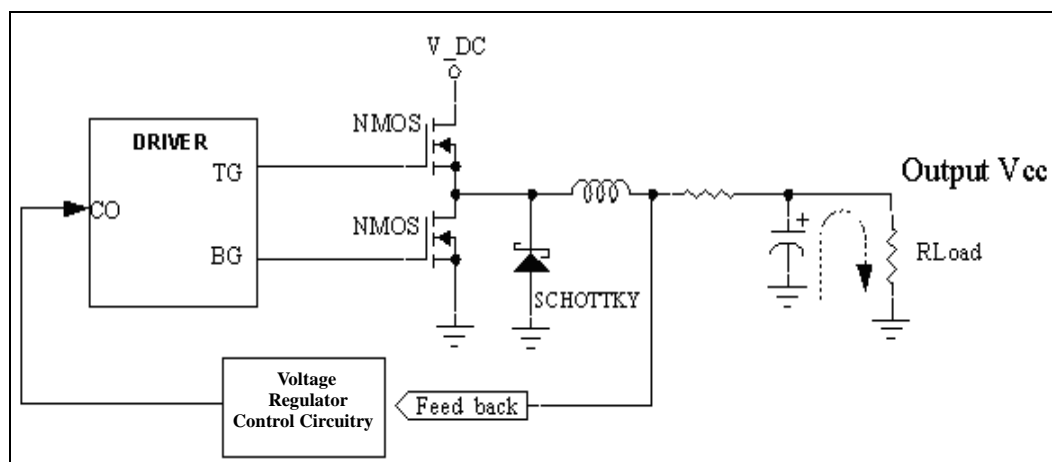
6.6.3.3   High Current Paths During Switching Dead Time

When the top MOSFET turns OFF and before the bottom MOSFET (there may be more than one of these) is turned ON, the pattern of current flow changes. The inductor is no longer being supplied current through the top MOSFET and starts to collapse its magnetic field. The inductor literally becomes a generator at this point. The dashed line in Figure 44 shows the current path during the time that both top and bottom MOSFETs are OFF, also known as dead time. During dead time, there is a high current flow through the inductor, processor, ground, and the Schottky diode. The diode and its traces must be laid out in a way to minimize both stray inductance and resistance with short, fat traces or planes.

Figure 44.   High Current Path With Top and Bottom MOSFETs Turned Off (Dead Time)
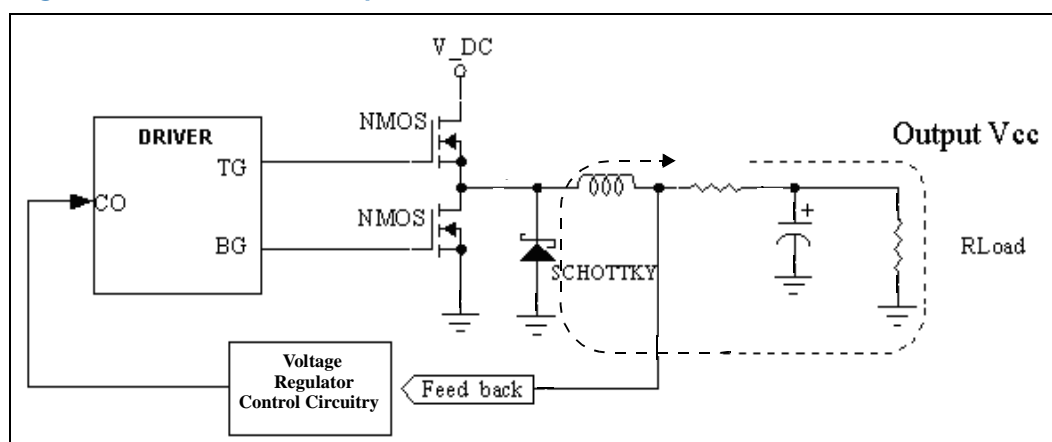
6.6.3.4   High Current Path With Bottom MOSFET(s) Turned ON

A few nanoseconds after the top MOSFET is turned OFF, the bottom MOSFET(s) is turned ON. The high current path now switches from the Schottky diode to the bottom MOSFET(s), the current path shown by the dashed/arrow line in Figure 45. Minimize stray inductance and resistance with short, fat traces or planes.

Figure 45. High Current Path With Bottom MOSFET(s) Turned ON
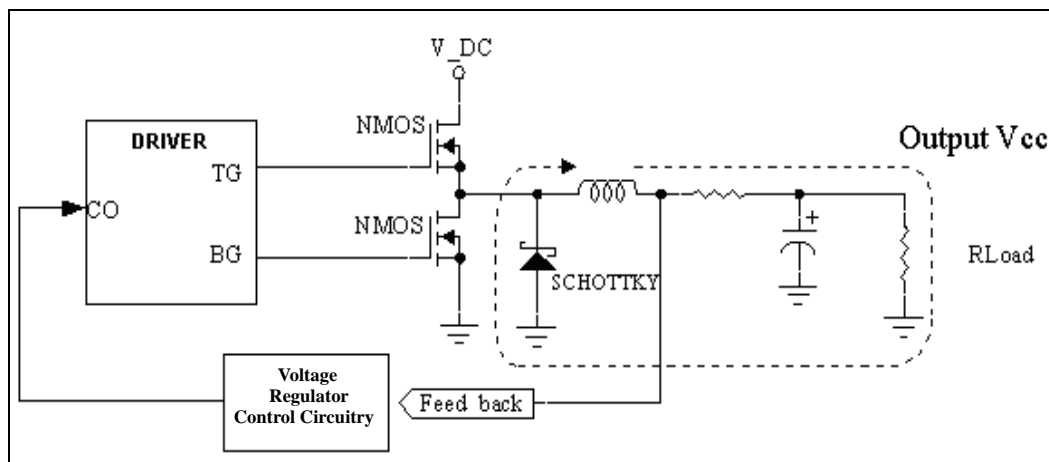
6.6.3.5 General Layout Recommendations

All of the components in the high current paths dissipate some power (i.e., they get warm when current runs through them). To minimize temperature rise and facilitate thermal spreading, use of large copper fill areas connecting the high current components is imperative. For example, the MOSFET manufacturers recommend that each MOSFET be mounted on one square inch of two-ounce copper. While this may not be possible in all environments, this recommendation serves to illustrate the importance of thermal considerations in the switching regulator layout.

- Bulk capacitors for V_{CC} need at least three vias per pad and it is recommended not to share vias. Clusters of bulk and bypass capacitors may be clustered along the high current paths between the sense resistor and the processor. Clusters may have copper fill areas between capacitors. This provides additional opportunities for as many vias as possible.

- Some controllers sense the load on Vcc by monitoring the voltage drop across the sense resistor with a Kelvin connection. The two feedback traces do not handle a high current, but must be of equal lengths to get an accurate load measurement. Connect the feedback signal traces as close as possible to both ends of the sense resistor. While the feedback traces do not handle high current, they are high impedance and susceptible to interference from electrical and magnetic noise. Avoid routing these traces near the power inductor and through vias.

- The sense resistor is to be placed as close to the inductor as possible, followed by the first two bulk capacitors.

- The lead frame in the power MOSFETs is used to dissipate heat. To do this, each of the power MOSFETs requires one square inch of copper.

- Avoid ground loops because they pick up noise. Use star or single point grounding. The source of the lower synchronous bottom MOSFET is an ideal point where the input and output ground planes may be connected.

- Keep the inductor-switching node small by placing the output inductor, switching top MOSFET, and synchronous bottom MOSFET(s) close together on the same copper fill.

- The MOSFET enable/gate traces to the driver must be as short (<1 in.), straight, and wide as possible (20–25 mils). Ideally, the driver has to be placed right next to the MOSFETs. Circuits using multiple top or bottom MOSFETs need to have serpentine gate traces, so all the traces going to the top MOSFET gate(s) and especially the bottom MOSFET gate(s) are the same length.

- Use bulk capacitors for the voltage regulator and multiple layer traces with heavy copper to keep the parasitic resistance low. Use a minimum of three vias per connection on each bulk capacitor.

- Place the top MOSFET drains as close to the VDC-input capacitors as possible.

- The sense resistor has to be wide enough to carry the full load current. A minimum of 1 via per Amp to the Vcc plane must be used. Use more when space permits.

- Use solid 2 oz. copper fill under drain and source connections of the top and bottom MOSFETs.

- The voltage regulator is usually left to the last moment. Often the allocated area is a small, narrow strip and the location is poor. These factors combine so that the design flow, described above, usually cannot be followed.

- General Rule: Copper fill is good. Fill the PCB with metal. There must be no large areas of the board without metal. Increase the width of the grounds, V_{CC}, and other power rails to fill any blank spots. Large metal fill areas allow the voltage regulator to improve its heat radiation and thereby run cooler. Large copper fill areas have other benefits too, including reducing series resistance and inductance and capturing and dissipating RF energy by allowing eddy currents to flow.

6.6.3.6   IA-32 core PLL Power Delivery

6.6.3.6.1   Filter Specifications for VCCA

VCCA is a power source required by the IA-32 Processor core PLL clock generators. Since this PLL is analog in nature, it requires a quiet power supply for minimum jitter. Jitter is detrimental to the system; it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). Traditionally, this supply is low-pass filtered to prevent any performance degradation. The IA-32 processor core has an internal PLL super filter for the external 1.2V supply VCCA pin that dispenses with the need for any external low-pass filtering. However, decoupling capacitors, two 0603 form factor (0.1 µF), and one 1206 form factor (10 µF), must be placed as close as possible to the VCCA pins. The decoupling topology is shown in Figure 46. Parasitics of connecting traces, circuits, and components are not shown in Figure 46

Note: VCCA[1:2] pins are both connected to the Processor VCCA decoupling circuit.

Figure 46.   Processor VCCA Decoupling Circuit Topology
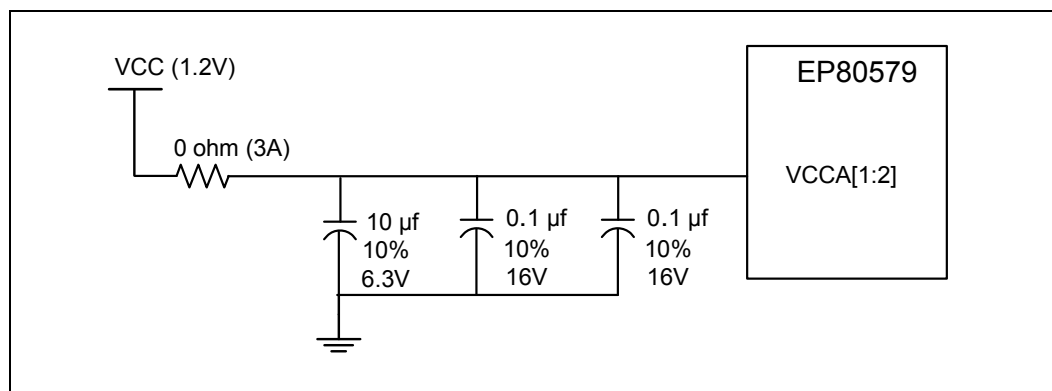
6.6.4   Power Plane Filter Requirements

Several power planes require very quiet supplies and also to generate a minimal amount of noise. These supplies must have a filter to help reduce noise on the source supply. Two types are power supply filtering are required:

- Analog Voltage Filter
- Bandgap Filter

6.6.4.1 Recommended Filter Topologies for Analog (PLL) and Bandgap Filters

Figure 47 shows the recommended filtering for Analog (PLL) and Bandgap supplies, and Table 13 provides the recommended component values for the filters.

6.6.4.1.1 Analog Filtering

The Analog filtering applies to the following signals:

- VCCARX - 1.2V Analog Power for SATA AFE Receiver
- VCCATX - 1.2V Analog Power for SATA AFE Transmitter
- VCCAPLL - 1.2V Analog Power for SATA PLL
- VCCAUSB12 - 1.2V Analog Power for USB PLL
- VCCAPE0PLL12 - 1.2V Analog Power for PCI Express PLL
- VCCAHPLL - 1.2V Analog Power for CRU PLL

6.6.4.1.2 Bandgap Filtering

The Bandgap filtering applies to the following signals:

- VCCSATABG3P3 - 3.3V Band-Gap Power for SATA AFE Reference Circuitry
- VCCABG3P3_USB - 3.3V Band-Gap Power for USB AFE Reference Circuitry
- VCCABGP033 - 3.3V Band-Gap Power for PCI Express Reference Circuitry

Figure 47. Analog/Bandgap Filter Topology
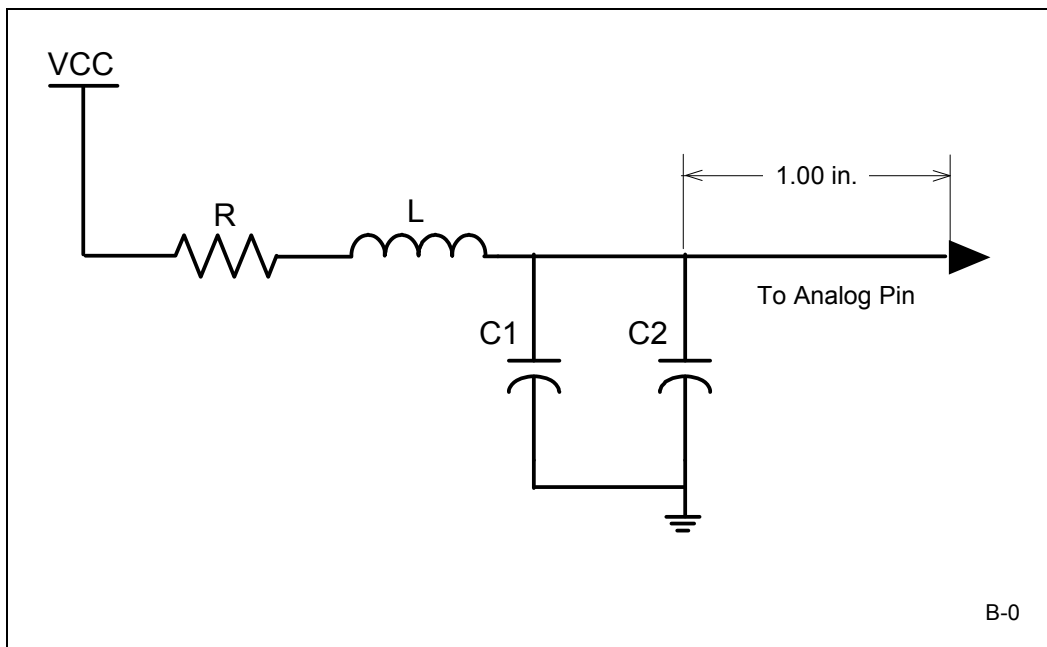
Table 13.   Analog and Bandgap Filter Components

Component	Value
Analog Filter Components	
VCCARX, VCCATX, VCCAHPLL, VCCAUSB12, VCCAPLL, VCCAPE0PLL12	
VCC	V1P2 (1.2V)
R	0 Ω
L[1]	4.7 µH
C1	0.1 µF
C2	10 µF
Bandgap Filter Components	
VCCSATABG3P3, VCCABG3P3_USB, VCCABGP033	
VCC	VCC3 (3.3V)
R	1 Ω
L[1]	4.7 µH
C1	0.1 µF
C2	10 µF

Note:
1.   For the 4.7 uH filter inductors, select inductors with maximum internal resistance of 0.2 ohm and a current rating of 120mA (min). See Table 14 for filter current rating requirements

6.6.5   Analog and Bandgap Filter Layout Guidelines

General board layout guidelines for the Analog filters are as follows:

- Ensure each listed supply has its own filter. Do not share filters between supplies.
- These supplies must have a via directly from the supply plane.
- The filter must be placed as close as possible to the EP80579.
- For filters that call out a distinct VSS, place the 0.1 uF capacitor as close as possible to the filters power and ground pins, even though they are connected to the VSS ground plane.
- Analog traces must be ground referenced.
- Minimum trace width of the analog signals is 12 mils.
- Minimum space to other signals is 20 mils

6.6.6   Analog and Bandgap Filter Frequency Response

The filters need to fall within the acceptable zone of the analog filter frequency response shown in Figure 48:

Figure 48. Filter Frequency Response Specification

B4335-01
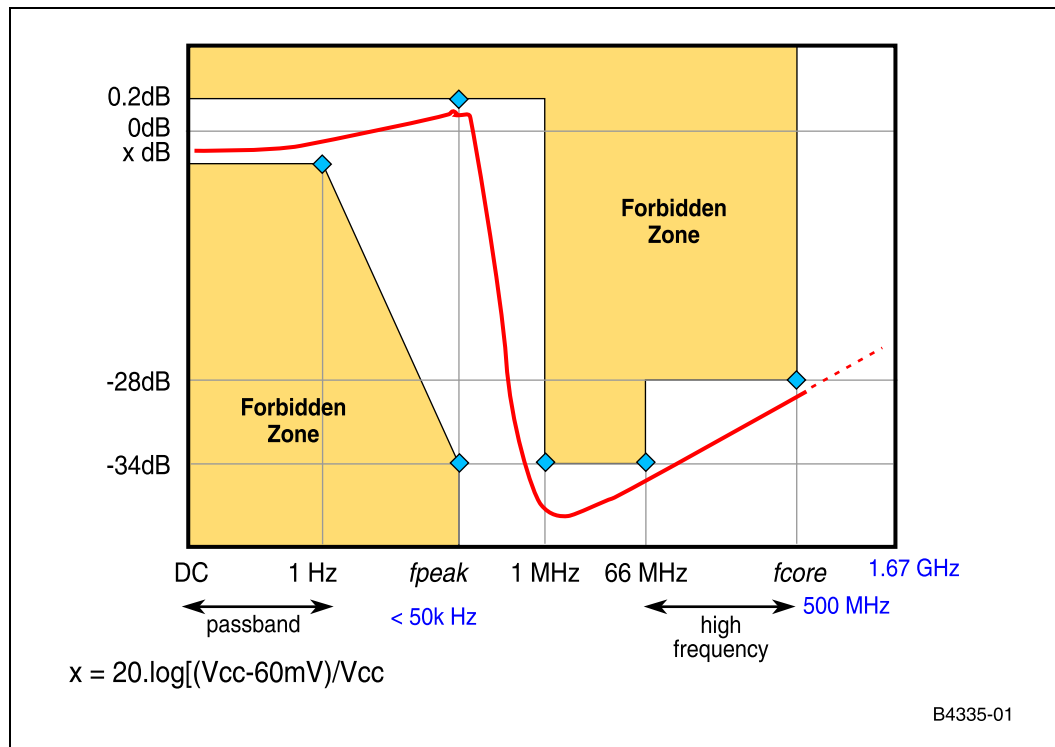
NOTES:
1. Filter DC resistance is the inductor resistance + MB routing resistance.
2. Vout measurement taken as close to (G)MCH package as possible.

6.6.7 Thermal Power Dissipation

Power dissipation has traditionally been a thermal/mechanical challenge for embedded system designers. The amount of current required from the processor power delivery circuit and the heat generated by processors has increased as processor frequencies go up and the silicon process geometry shrinks. The package of any integrated device can dissipate a limited amount of heat into the surrounding environment. The temperature of a device, such as a processor power delivery circuit-switching transistor, is a balance of heat being generated by the device and its ability to shed heat either through radiation into the surrounding air or by conduction into the circuit board. Increased power may effectively raise the temperature of the processor power delivery circuits. Switching transistor die temperatures may exceed the recommended operating value when the heat cannot be removed from the package effectively.

As the current demands for higher frequency and performance processors increases, the amount of power dissipated (i.e., heat generated) in the processor power delivery circuit is starting to become of concern for the applied computing system, thermal, and electrical design engineers. The high input voltage, low duty factor inherent in power supply designs leads to increasing power dissipation losses in the output stage of the traditional buck regulator topology used in the industry today.

These losses may be attributed to three main areas of the processor power delivery circuit.

• The switching MOSFET dissipates a significant amount of power during switching of the top control MOSFET.

- Power dissipation results from drain to source resistance (R_{DS-ON}) DC losses across the bottom synchronous MOSFET.
- Power dissipation occurs through the magnetic core and windings of the main power inductor.

Significant improvement have been made in the switching MOSFET technology to lower gate charge of the control MOSFET, allowing them to switch faster and reduce switching losses. Improvements in lowering the $R_{DS(ON)}$ parametric of the synchronous MOSFET have resulted in reduced DC losses. Also, the direct current resistance (DCR) of the power inductor has been reduced to lower the amount of power dissipation in the circuit's magnetic core and windings.

These technology improvements by themselves are not sufficient to effectively remove the heat generated during the high current demand and tighter voltage regulation required by today's processors. There are several mechanisms for effectively removing heat from the package of these integrated devices. Some of the most common methods are as follows:

- Attach a heat spreader or heat pipe to the package with a low thermal co-efficient bonding material.
- Add and/or increase the copper fill area attached to high current carrying leads.
- Add or re-direct air flow to flow across the device.
- Utilize multiple devices in parallel, as allowed, to reduce package power dissipation.
- Utilize newer/enhanced technology and devices to lower heat generation, with equal or better performance.

For the system designer, these options are not always available or economically feasible. The most effective method of thermal spreading and heat removal, from these devices, is to generate airflow across the package and add copper fill area to the current carrying leads of the package.

6.7 Decoupling Recommendations

This section details the decoupling required by the EP80579.

6.7.1 VCCVC (IA-32 core Power) Decoupling

Care must be taken to reduce the loop inductance for the whole delivery path.
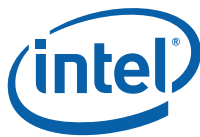
- Two 330 µF±20%, 4V (TANT) capacitors are recommended as bulk decoupling for IA-32 core power plane.
- Two 150 µF±20%, 4V, ESR (45 mΩmax) capacitors are recommended as bulk decoupling for IA-32 core power plane.
- Fifteen 10 µF,±20% 6.3V X5R capacitors are recommended.

6.7.2 VCC (1.2V Core Logic) Decoupling

- Two 150 µF±20%, 4V, ESR (45 mΩmax) capacitors are recommended as bulk decoupling for core logic power plane.
- Twenty 10 µF,±20% 6.3V X5R capacitors are recommended.
- Five 0.1 µF ±10% 16V X7R capacitors are recommended.

6.7.3 VCCA[2:1] (1.2V, IA-32 core PLL Power) Decoupling

- Two 0.1 µF ±10%, 16V X7R capacitors are recommended.

- One 10 µF,±20% 6.3V X7R capacitors are recommended as bulk decoupling.

6.7.4 VCCAPE (1.2V, PCI Express Power) Decoupling

- Three 0.1 µF ±10%, 16V X7R capacitors are recommended.
- One 10 µF,±20% 6.3V X7R capacitors are recommended as bulk decoupling.

6.7.5 VCC18 (1.8V - DDR2) Decoupling

VCC18 power pins are decoupled separately from the DIMMs. These recommendations apply only to the VCC18 power pins. The decoupling of the DIMMs DDR2 power pins are specified below.

- Five 0.1 µF ±10%, 16V X7R capacitors are recommended for the DDR2 power plane (VCC18) for decoupling.
- Three 10 µF,±20% 6.3V X7R capacitors are recommended as bulk decoupling.

6.7.6 VTTDDR (0.9V - DDR2_VTT) Decoupling

VTTDDR power pins are decoupled separately from the DIMMs. These recommendations apply only to the VTTDDR power pins.

- Ten 0.1 µF ±10%, 16V X7R capacitors are recommended for the VTTDDR power plane for decoupling.
- Two 2.2 µF ±10%, 10V X5R capacitors are recommended as bulk decoupling for VTTDDR power plane decoupling.

6.7.7 V1P8_DDR (DIMM) Decoupling (CRB Power Reference)

These recommendations apply to the decoupling of the DIMMs' power pins. All decoupling capacitors should have direct connection to the V1P8_DDR power plane and two vias to ground.

- Six 100 µF ±20%, 6.3V (electrolytic) capacitors are recommended as bulk decoupling for the DIMMs' power pins decoupling.
- Eight 0.1 µF ±10%, 16V X7R capacitors are recommended for the DIMMs' power pins decoupling.

6.7.8 VCC33 (3.3V) Decoupling

- Three 0.1 µF ±10%, 16V X7R capacitors are recommended to be placed near the VCC33 power plane for decoupling. It is recommended that the designer use ceramic capacitor 0603 package type.
- Ten 10 µF,±20% 6.3V X5R capacitors are recommended as bulk decoupling.

6.7.9 VCC25 (2.5V GbE Voltage) Decoupling

- Three 0.1 µF ±10%, 16V X7R capacitors are recommended to be near the VCC25 power plane for decoupling. It is recommended that the designer use ceramic capacitor 0603 package type.
- One 2.2 µF ±10%, 10V X5R capacitor is recommended.
- One 10 µF,±20% 6.3V X5R capacitor is recommended as bulk decoupling.
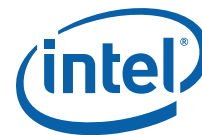
6.7.10 VCC50 (5.0V Reference) Decoupling

- Five 0.1 µF ±10%, 16V X7R capacitors are recommended.
- Two 10 µF ±20% 16V Y5V capacitors are recommended as bulk decoupling.

6.7.11 VCCPRTC (Battery Power) Decoupling

- Two 0.1 µF ±10%, 16V X7R capacitors are recommended.
- One 10 µF ±20% 16V Y5V are recommended as bulk decoupling.

6.7.12 VCC50_SUS (5.0V Standby logic) Decoupling

- Two 0.1 µF ±10%, 16V X7R capacitors are recommended.
- Two 10 µF ±20% 16V Y5V capacitors are recommended as bulk decoupling.

6.7.13 VCCPSUS (3.3V Standby logic) Decoupling

- Two 0.1 µF ±10%, 16V X7R capacitors are recommended.
- Two 10 µF ±20% 16V Y5V capacitors are recommended as bulk decoupling.

6.7.14 VCCSUS25 (2.5V Standby logic) Decoupling

- Two 0.1 µF ±10%, 16V X7R capacitors are recommended.
- Two 10 µF ±20% 16V Y5V are recommended as bulk decoupling.

6.7.15 VCCSUS1 (1.2V Standby logic) Decoupling

- Two 0.1 µF ±10%, 16V X7R capacitors are recommended.
- Two 10 µF ±20% 16V Y5V are recommended as bulk decoupling.

7.0 Power Management and Reset Interface

7.1 Reset and Powergood Distribution

7.1.1 Types of Reset

The EP80579 has four types of reset: Power-good (cold) reset, hard reset, CPU-only reset, and targeted I/O subsystem reset(s). Each of these reset subclasses have unique effects and is described in Table 14.

Table 14.   Types of Reset and Wake-up from Power Saving States

Type	Mechanism	Effect of Reset on following blocks				
		CPU	IMCH/ IICH	AIOC	PCI-E	DDR
Power-good	Input pin	Reset	Reset	Reset	Reset	Reset
Hard	Input pin	Reset	Reset	Reset	Reset	Reset
Software (SW) Controlled	Write to I/O port CF9	Reset	Reset	Reset	Reset	Reset
CPU-only	Internal to EP80579. Generated by IMCH	Reset	-N/A	-N/A	-N/A	-N/A
S3 -> S0	Wake Event	Reset	Reset	Reset	Reset	-N/A
S5->S0	Wake Event	Reset	Reset	Reset	Reset	Reset

7.1.2 Powergood Implementation

The initial boot from when the power supplies are energized are facilitated by the Powergood mechanism. The voltage sources from all platform power supplies are routed to the EP80579 component which tracks them as they ramp-up, and the platform asserts powergood (CPU_VRM_PWR_GD and SYS_PWR_OK) after a fixed interval (nominally 99ms) and after the last voltage reference has stabilized. Powergood signals are propagated asynchronously to dedicated IICH, IMCH, and IA CPU internal blocks. Generally, the components in AIOC fabric including the AIOC reset block do not receive a powergood signal. The exception is the GbE MAC devices.

7.1.3 Hard Reset Implementation

A hard reset is initiated by the IICH via the PLTRST# as a result of various S-state wake events or other reset signal assertions. PLTRST# is driven to the IMCH and is propagated from there to the reset block for AIOC fabric. The reset block in the AIOC fabric is responsible for resetting the individual blocks.

IMCH propagates a hard reset to the FSB and subordinate PCI Express subsystems. The FSB components are reset via an internal reset signal, while the PCI Express subsystems are reset through PCIRST#.

7.1.4 Software Controlled Reset

Software may cause a full system reset through a write to the Reset Control Register located at I/O port CF9.

7.1.5 CPU (IA-32 core) Only Reset

For power management, error conditions, and other reasons, the EP80579 supports a targeted CPU only reset semantic. This mechanism eliminates system reset at large when the CPU function (such as clock gearing selection) must be updated during initialization. It only affects the CPU. Other blocks such as IICH, IMCH, AIOC complex are not reset. It is controlled by IMCH.

7.2 Reset and Powergood Interface Implementation

This section describes the reset and powergood external interfaces for the EP80579.

Figure 49 provides the block diagram for the reset and powergood interface.

Figure 49. Powergood and Reset Interface
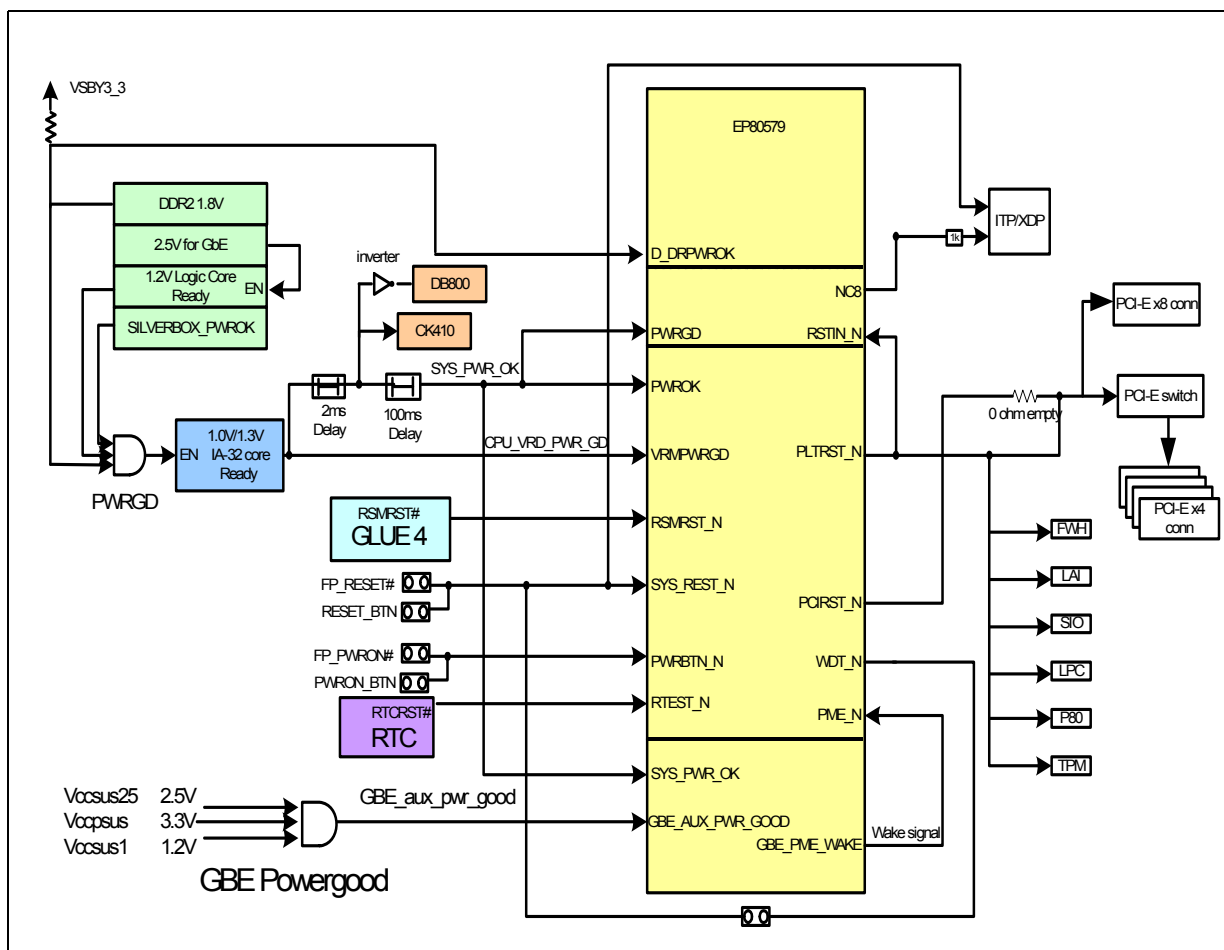
7.2.1 Powergood Interface

The EP80579 receives two external powergood signals. The first is IA-32 core VRMPWRGD and the other is SYS_PWR_OK. SYS_PWR_OK is asserted after at least 102 ms delay from the time that VRMPWRGD goes active and indicates that power has been stable for at least 99 ms. See Figure 49 for the block diagram showing VRMPWRGD and SYS_PWR_OK interfaces.

7.2.2 Reset Interface

The EP80579 receives two reset signals externally.

The first one is the System Reset signal (SYS_RESET#) which can be connected to a reset button. Designers can connect the System Reset signal (SYS_RESET#) on the EP80579 directly to a reset button on the system's front panel provided that the front panel signal is pulled up to 3.3 V standby through a weak pull-up (10 kΩ) resistor. The EP80579 will debounce signals on this pin (16 ms) and allow the SMBus to go idle before resetting the system, helping to prevent a slave device on the SMBus from "hanging" by resetting in the middle of a cycle. See Figure 49.

The second is Resume Reset which is used for resetting the IICH resume well after power is restored from a power failure. See Figure 49.

7.2.2.1 PWRBTN#

The Power Button signal (PWRBTN#) on the EP80579 can be connected directly to the power button on the system's front panel. This signal is internally pulled-up in the EP80579 to Suspend_3.3V (VCCPSUS) through a weak pull-up resistor (15–35 kΩ). EP80579 has a 16 ms internal debounce logic on this pin. See Figure 49.

7.2.2.2 PLTRST# / PCIRST# Usage Model

The EP80579 asserts the platform reset signal (PLTRST#) during power-up and when a hard reset sequence is initiated. This signal must be connected to all devices on the motherboard that require a reset. PLTRST# must also be connected to EP80579's RSTIN# signal. PCIRST# is the secondary PCI Bus reset signal and must only be connected to PCI slots or PCI down devices. See Figure 49.

7.2.2.3 IICH Reset

IICH plays the central role in reset and powergood distribution to the whole chip. IICH receives two powergood signals from platform VRMPWRGD and SYS_PWR_OK. Assertion of these signals start the reset sequence for EP80579.

IICH generates the central reset signal (known as PLTRST#) that initiates the reset of IMCH and the rest of the chip. IICH also generates PCIRST# signal for resetting the PCI device.

7.2.2.4 GbE MAC Reset

There are three GbE MAC devices. Each GbE MAC receives it's reset from internal reset unit and also requires a hardware external reset signal via the EP80579 SYS_PWR_OK input. For "normal" operation, the GBE_AUX_PWR_GOOD pin should also be connected to the SYS_PWR_OK signal. However, since the GbEs also supports Wake-On-LAN and S3-cold, they may actually be connected to a separate auxiliary power supply. To support S3-cold, the GBE_AUX_PWR_GOOD pin should be connected to the platform supplied power good signal from the auxiliary power supply. (see Figure 49)

7.2.3 Reset Sequence

Figure 50 shows the reset sequence executed by EP80579 during power up.

Figure 50.   Reset Sequence
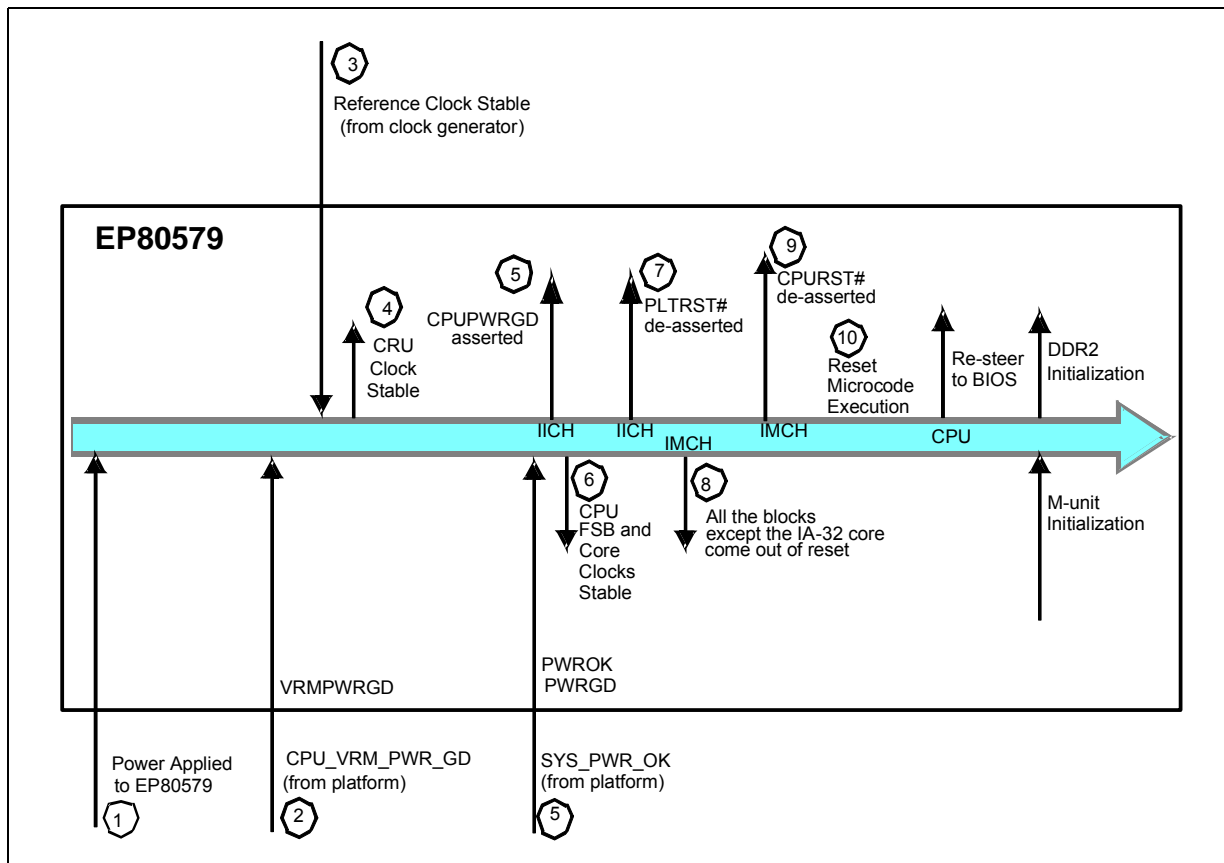
7.2.3.1   Reset Procedure

1. EP80579 receives power and drives its BSEL and V_SEL pins. IA-32 core VRMPWRGD, and SYS_PWR_OK are not asserted. PLTRST# (platform signal) and CPURST# (internal signal) are asserted.

2. VRMPWRGD is asserted (platform signal).

3. Reference Clock provided from platform is stabilized. Voltage regulator output is modified to correspond to BSEL and V_SEL values.

4. CRU PLL locks.

5. SYS_PWR_OK (platform signal) == PWROK/PWRGD internal signal asserted.

6. IO and PLLs are locked to achieve stable IA-32 core Clocking.

7. IICH de-asserts PLTRST#.

8. All EP80579 blocks except the IA-32 core come out of reset.

9. IMCH de-asserts CPURST#.

7.3 Power Management

7.3.1 Supported Power States

EP80579 can be switched to a very low power state during what looks like to the user as "off". The traditional PC power states typically supported by IA-32 core, IMCH and IICH components are employed by the EP80579 for this goal.

Table 15. Three Basic System Power States

Platform Power State	Basic Description	PC equivalent System States	CPU States	Memory States	System Clocks
On	Everything up and running.	S0	C0,C1,C2	Full on	On
Suspend	All systems powered off other than main memory and logic required to wake the system	S3	Powered off	Self Refresh	Off
Soft Off (S5)	All systems powered off and the OS does not save any context. The system is in the "soft" off state and requires a complete boot when it wakes.	Powered off S5	Powered off	Powered off	Off

7.3.1.1 System States

- S0: Full On
- S3: Suspend to RAM (STR).

  Memory is placed into "Self Refresh" before the system enters S3. All power on EP80579 is removed except for the system memory power (VCC18). During this state, no accesses are allowed from any agent and all devices are disabled. Power to the core logic may not be maintained during this state so the internal register contents will not remain valid while in this state. A reset is required during resume from S3.

- S5: Soft Off. All power lost. Total reboot needed.

7.3.1.2 Main Memory States

The main memory is power managed during normal operation and in low power states.

Main memory states are:

- Power up: CKE asserted. Active mode
- Precharge Power down: CKE de-asserted (not self-refresh) with all banks closed
- Active Power down: CKE de-asserted (not self-refresh) with at least one bank active
- Self-Refresh: CKE de-asserted using device self-refresh

7.3.1.3 IA-32 core States

The EP80579 supports the AutoHALT, Stop Grant and Sleep states for optimal power management. See Figure 51 for a visual representation of the IA-32 core low-power states.

Figure 51. Clock Control States
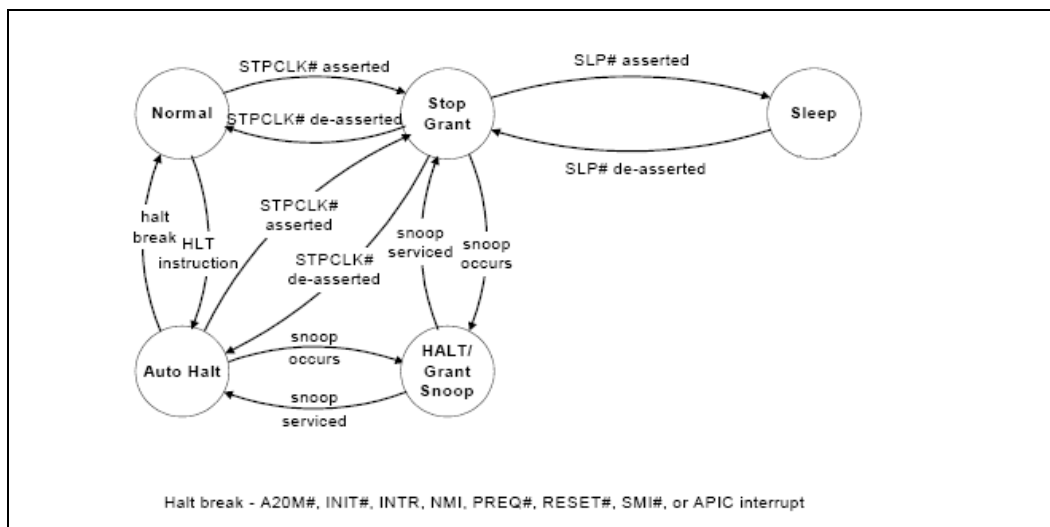
7.3.1.3.1 Normal State (C0)

This is the normal operating state for the IA-32 core.

7.3.1.3.2 AutoHALT Powerdown State (C1)

AutoHALT is a low-power state entered when the IA-32 core executes the HALT instruction. The IA-32 core will transition to the Normal state upon the occurrence of SMI#, INIT#, LINT[1:0](NMI, INTR), or FSB interrupt message. RESET# will cause the IA-32 core to immediately initialize itself.

A system management interrupt (SMI) handler will return execution to either Normal state or the AutoHALT Powerdown state.

The system can generate a STPCLK# while the IA-32 core is in the AutoHALT Powerdown state. When the system deasserts the STPCLK# interrupt, the IA-32 core will return execution to the HALT state.

While in AutoHALT Powerdown state, the IA-32 core will process bus snoops and interrupts.

7.3.1.3.3 Stop-Grant State (C2)

When the STPCLK# pin is asserted, the Stop-Grant state of the IA-32 core is entered 20 bus clocks after the response phase of the IA-32 core-issued Stop Grant Acknowledge special bus cycle.

SYS_RESET# will cause the IA-32 core to immediately initialize itself, but the IA-32 core will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be deasserted ten or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state will occur when the IA-32 core detects a snoop on the FSB (see Section 7.3.1.3.4). A transition to the Sleep state (see Section 7.3.1.3.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT# and LINT[1:0] will be latched by the IA-32 core, and only serviced when the IA-32 core returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the IA-32 core will process snoops on the FSB and it will latch interrupts delivered on the FSB.

7.3.1.3.4 HALT/Grant Snoop State

The IA-32 core will respond to snoop or interrupt transactions on the FSB while in Stop-Grant state or in AutoHALT Power Down state. During a snoop or interrupt transaction, the IA-32 core enters the HALT/Grant Snoop state. The IA-32 core will stay in this state until the snoop on the FSB has been serviced (whether by the IA-32 core or another agent on the FSB) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the IA-32 core will return to the Stop- Grant state or AutoHALT Power Down state, as appropriate.

7.3.1.3.5 Sleep State

The Sleep state is a low power state in which the IA-32 core maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the IA-32 core will enter the Sleep state upon the assertion of the SLP# signal. The SLP# pin should only be asserted when the IA-32 core is in the Stop Grant state. SLP# assertions while the IA-32 core is not in the Stop-Grant state is out of specification and may result in unapproved operation.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the IA-32 core is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or SYS_RESET#) are allowed on the FSB while the IA-32 core is in Sleep state. Any transition on an input signal before the IA-32 core has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the IA-32 core is in the Sleep state, and held active as specified in the SYS_RESET# pin specification, then the IA-32 core will reset itself, ignoring the transition through Stop-Grant State. If SYS_RESET# is driven active while the IA-32 core is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after SYS_RESET# is asserted to ensure the IA-32 core correctly executes the Reset sequence.

7.4 Power Sequencing

Refer to *Intel® EP80579 Integrated Processor Product Line Datasheet* for Power Sequencing Timing Diagrams.

8.0 Platform System Clock

The Development Board uses a single CK410 clock synthesizer, as well as DB800 x8 companion buffer solutions, to minimize jitter, improve routing, and reduce cost.

The CK410 provides three differential CPU host clock pairs and one selectable differential CPU/SRC clock. All host clock pairs are frequency selectable at 100/133/166/200/266/333/400 MHz.

The CK410 also provides six SRC (Serial Reference Clock) differential pairs to the Development Board. The SRC clocks provide 100 MHz differential pair outputs for all of the bus agents, including one for SATA devices and one 100 MHz differential output pair SRC to the DB800. The DB800 companion differential buffer provides the 100 MHz differential clocks for the PCI Express*. Figure 52 shows the implementation of the CK410 bus clocks for the Development Board.

The Development Board design uses a CK410-compliant clock generator to supply the primary clocks. Additional differential clocks are generated with the DB800 clock synthesizer. The Development Board design also has various discrete clocks that are not available in the CK410, such as GbE (25 MHz) and Local Expansion Bus (LEB) clock (33 MHz).

8.1 Platform System Clock Generation

There are several external clock components shown in Figure 52. The first is the CK410 clock generator. This clock generator generates the following:

- Host_CLK: a 100/133 MHz reference clock which is used to generate the internal FSB clock (controlled by the BSEL). This is a spread spectrum clock, so all clocks derived from this will also be spread spectrum.

- CLK100 clock: a fixed 100 MHz reference clock which is used by the PCI Express, SATA interface and DB800 companion differential buffer.

The CK410 also generates a number of other clocks, which are used by the IICH, such as CLK33, CLK14, and CLK48.

The second clock component is the external 25 MHz crystal clock as a reference to the GbE PHY; the GbE PHY uses this clock to generate a 125 MHz reference to the internal GbE MACs. The Local Expansion Bus (LEB) also requires an external clock (33/80 MHz) as reference to the LEB, and The TDM interface requires a 8.192 MHz that provides external T1/E1 plug-on for mezzanines cards.

The CK410 pins require the following stuffing options:

- The series resistor, designated as Rs (33 Ω), and parallel resistor, designated as Rt (49.9 Ω), are required for CK410 output differential clock (Figure 53).

- The series resistor, designated as Rs (33 Ω) is required for CK410 output single-ended clock (Figure 53).

Table 16.   CK410 Clock Groups
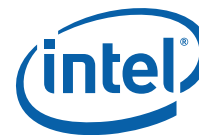
Clock Group Name	Frequency (MHz)	Receiver
Host_CLK	100/133	IA-32 core and ITP (Debug Port)
CLK100	100	PCI Express slot, PCI Express, SATA
CLK33	33	PCI Clock, LPC, Firmware Hub, Port80, TPM, SIO, and ITP Debug
CLK14	14.318	ICH
CLK48	48	USB

Table 17.   Platform System Clock Reference

Clock Group	CK410 Pin	Component	Component Signal Name
Host_CLK	CPU_0	IA-32 core 100/133 MHz Clock	CLKP100
	CPU_0#		CLKN100
	CPU_1	NC (No Connect)	
	CPU_1#		
	CPU_2	ITP - - ITP_BCLK	BCLKP
	CPU_2#		BCLKN
CLK100	SRC	DB800 (SRC Differential Buffer) - PCI Express Slot	SRC_IN(p/n)
		PCI Express	PEA_REFCLK(p/n)
		PCI Express x8 Slot	PCIE_x8_100_MHz_(p/n)
		SATA	SATA_CLKREF(p/n)
CLK14	REF	EP80579 - ICH 14 MHZ Clock	CLK14
		SIO - LPC 14 MHZ Clock	CLOCKI
CLK33	PCI_0	Port80 - PORT80 33 MHz Clock	GCLK
	PCI_1	FWH - FWH 33 MHz Clock	CLK
	PCI_2	SIO - SIO 33 MHz Clock	PCI_CLK
	PCI_3	IICH 33 MHz Clock	PCICLK
	PCI_4	TPM - TPM 33 MHz Clock	LCLK
	PCI_5	ITP - ITP 33 MHz Clock	GCLK
CLK48	USB_48	USB - USB 44 MHz Clock	CLK48

Figure 52. Development Board Clocking Diagram
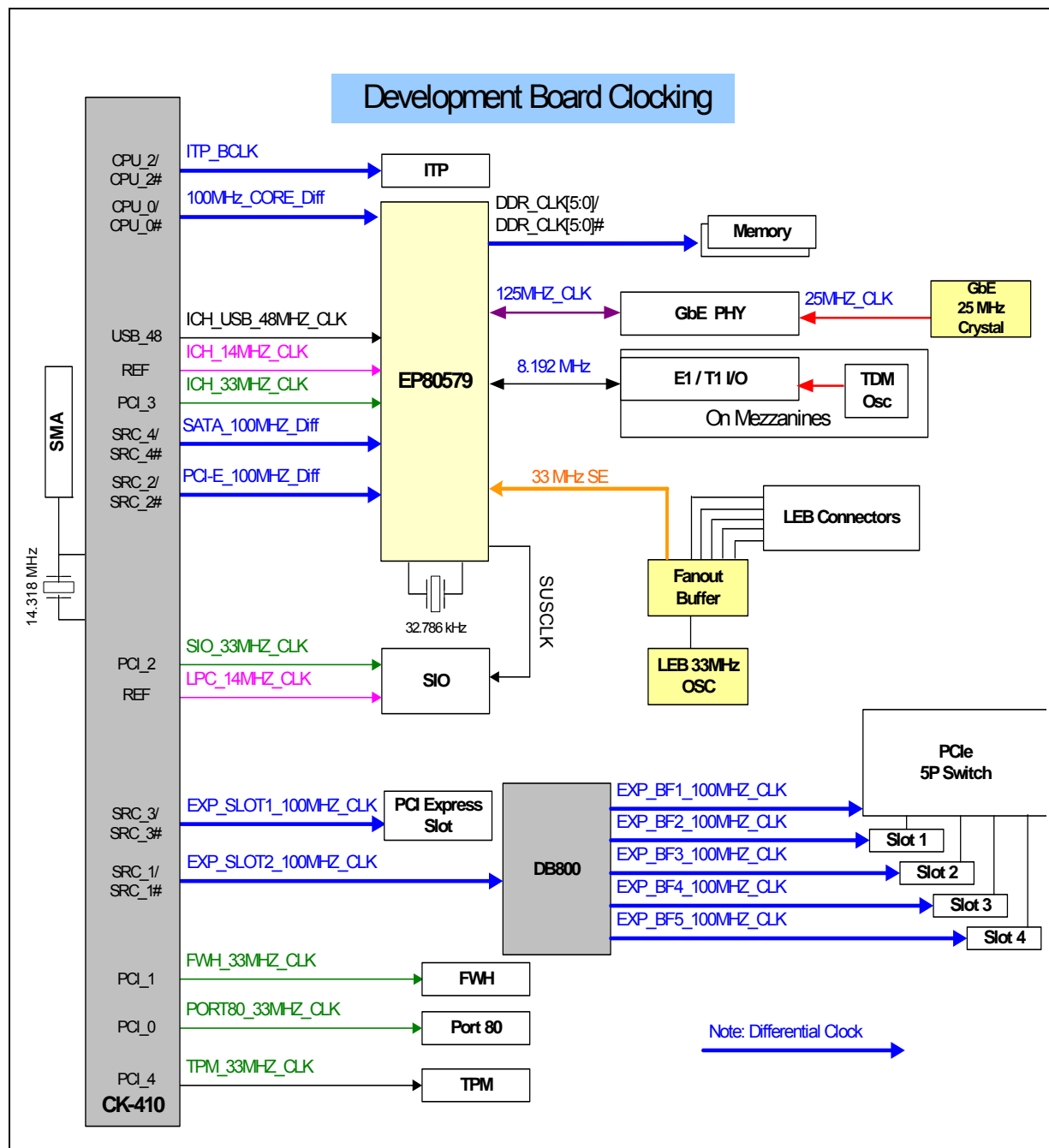
8.2 System Clock Groups

Each of the clock groups mentioned in Table 16 are discussed in the following sections.

8.2.1 HOST_CLK Group

The clock synthesizer provides three sets of 100/133 MHz differential clock outputs. Two of the differential clocks are driven to EP80579 (CLKP100/CLKN100), and to the ITP Debug Port (BCLKP/BCLKN), as shown in Figure 52 . The HOST_CLK Group Topology and Routing guidelines provided in this section applies to the routing of the differential clocks from the clock synthesizer to EP80579 or to the ITP Debug Port

The clock driver differential bus output structure is a "current mode current steering" output, which develops a clock signal by alternately steering a programmable constant current to the external termination resistors, designated as Rt. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor, so the amplitude of the clock signal can be adjusted for different values of resistance to match impedances or to accommodate future load requirements. See the *CK410B Clock Synthesizer/ Driver Specification* for more information.

8.2.1.1 HOST_CLK Topology

The recommended termination for the differential bus clock is a "shunt source termination." See Figure 53 for an illustration of this terminology scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors, designated as Rs, provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with Rt.

Select a value for Rt to match the characteristic impedance of the baseboard.

Figure 53. Source Shunt Termination
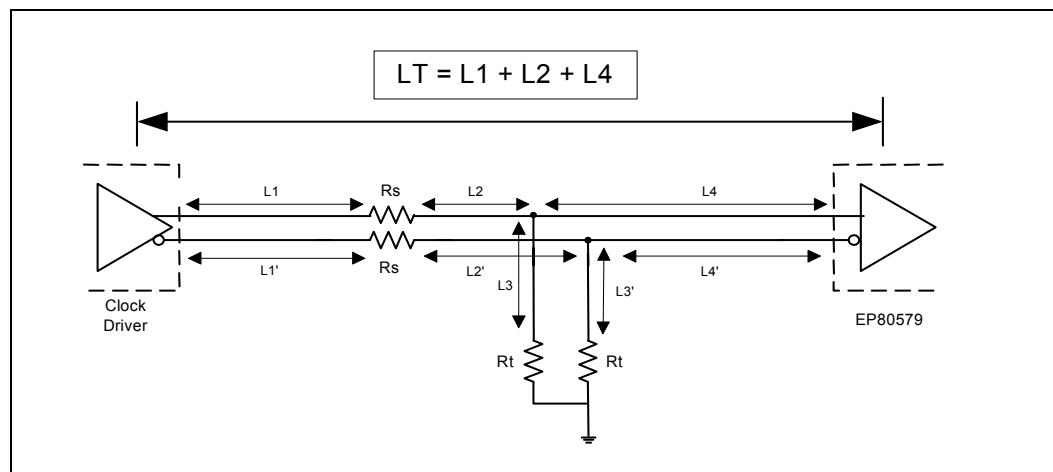
Table 18. **HOST_CLK Routing Guidelines**

Parameter	Routing Guidelines	Figure
Signal Group	Host_CLK: • EP80579 (CLKP100/CLKN100) • ITP Debug Port (BCLKP/BCLKN)	
Reference Plane	Ground Referenced, Microstrip or stripline	
Layer Assignment	Layers 3 or 8	
Characteristic Trace Impedance (Zo)	100 Ω ±10% (differential)	
Trace Width – W	microstrip: 4.5 mils stripline: 4.75 mils	Figure 54
Spacing within HOST_CLK pairs – S	10 mils	Figure 54
HOST_CLK to Signal Spacing – S1	20 mils	Figure 54
Serpentine Spacing	20 mils	Figure 54
Routing Length – L1, L1′: Clock Driver to Rs	0.5 in. max (Differential)	Figure 53
Routing Length – L2, L2′: Rs to Rs-Rt Node	0.2 in. max (Differential)	Figure 53
Routing Length – L3, L3′: Rs-Rt Node to Rt	0.2 in. max (Differential)	Figure 53
Routing Length – L4, L4′[1]	Min: 1 in. Max: 10 in.	Figure 53
Host_CLKn to Host_CLKp Length Matching	±5 mils	
Rs Series Termination Value	33 Ω ±5%	Figure 53
Rt Shunt Termination Value	49.9 Ω ±1%	Figure 53
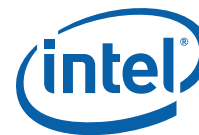
Notes:
1. These traces must not cross any plane splits on adjacent layers. In addition, these must not switch layers for the L4 segment in Figure 53.
2. Routing guidelines are recommended for both 3 and 8 layer.
3. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Maintain uniform spacing along the entire length of the trace. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.

Figure 54. **Trace Spacing for HOST_CLK Clocks**
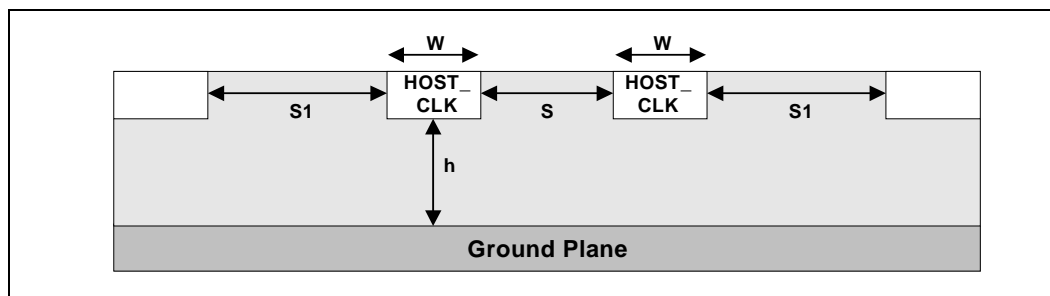
8.2.1.2 Host_CLK General Routing Guidelines

The host bus clocks delivered to the processor can be either microstrip or stripline routing but must be ground referenced to minimize dielectric and impedance variations. Do not split up the two halves of a differential clock pair between layers. Route clocks to agents on the same physical routing layer. See Table 18 for detailed requirements.

8.2.2 CLK100 (SRC Clock) Group

The differential 100 MHz clock synthesizer (SRC) is the source to the PCI Express, SATA and an input to the DB800 differential buffer. The DB800 buffer provides outputs to the PCI Express I/O components.

8.2.2.1 SRC/SRC# General Routing Guidelines

- Do not split up the two halves of a 100 MHz differential clock pair between layers and route to all agents on the same physical routing layer referenced to ground.

- Individual clock pairs must be matched to within ±25 mils, though no length matching is required between different source pairs.

- Do not place vias between adjacent complementary clock traces and avoid layer transitions. Vias placed in one half of a differential pair must be matched by vias in the other half. Differential vias can be placed within length L1, between clock driver and Rs, if needed to shorten length L1.

8.2.2.2 SRC Clock Topology

The CK410 clock synthesizer provides six sets of 100 MHz differential Serial Reference Clock (SRC) outputs. The 100 MHz differential clocks are driven to the SATA and PCI Express ports as well as PCI Express slots or components. See Figure 52.

The clock driver differential bus output structure is a "current mode current steering" output, which develops a clock signal by alternately steering a programmable constant current to the external termination resistors, designated as Rt. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor, so the amplitude of the clock signal can be adjusted for different values of resistance to match impedances or to accommodate future load requirements.

The recommended termination for the differential bus clock is a "shunt source termination." See Figure 55 for an illustration of this terminology scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage and matching the driver output impedance to the transmission line. The series resistors, designated as Rs, provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with Rt.

The value of Rt must be selected to match the characteristic impedance of the baseboard.

8.2.2.3 Source Clock to Down Devices

Figure 55. Source Clock Topology to Down Devices (Except PCI-E)

$$LT = L1 + L2 + L4$$

Clock Driver
CK410

Rs

Rs

SATA, or other
down devices
(Except PCI-E)

L3 L3'

Rt Rt
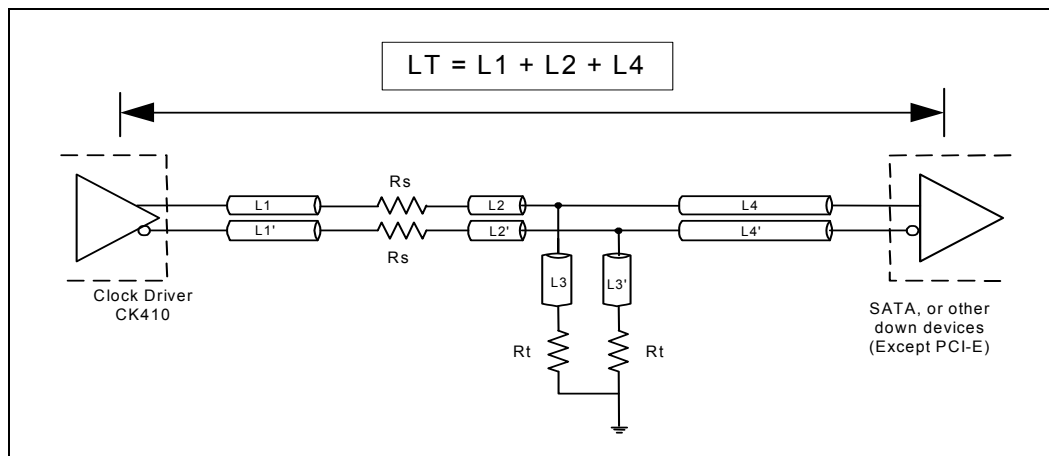
Table 19. 100 MHz SRC/SRC# Clock Routing Guidelines for Down Devices(Except PCI-E)

Layout Guideline	Value	Figure	Notes
Trace Width (W)	microstrip: 4.5 mils stripline: 4.75 mils	Figure 57	1,2
Differential Pair Spacing (S)	10 mils	Figure 57	3,4
Spacing to Other Traces (S1)	20 mils	Figure 57	
Motherboard Impedance – Differential	100 Ω ±10%		3,4
Routing Length (L1, L1'): Clock Driver to Rs	0.5in. max	Figure 55	5
Routing Length (L2, L2'): Rs to Rs-Rt Node	0.2in. max	Figure 55	5
Routing Length (L3, L3'): Rs-Rt Node to Rt	0.2in. max	Figure 55	5
Routing Length (L4, L4'): Rs-Rt Node to Load	Min: 1in. Max: 16in.	Figure 55	
SRC to SRC# Length Matching	within 5 mils		
Resistors	Rs = 22-33 Ω ±5% Rt = 49.9 Ω ±1% (for 100 Ω differential impedance)	Figure 55	

Notes:
1. Routing guidelines are for the width is 4.5 mils with 10 mil spacing on layers 3 & 8. Use 4.5-mil line width and adjust the trace to trace air gap to achieve 100 Ω differential impedance.
2. Trace width and differential spacing is stackup dependent.
3. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Maintain uniform spacing along the entire length of the trace. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
4. The differential impedance of each clock pair is the critical parameter. Single-ended impedance may vary with different geometries.
5. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ringback.

8.2.2.4 Source Clock to PCI Express* Components or Connectors

Figure 56. CLK100 Clock Group (SRC Clock) Topology
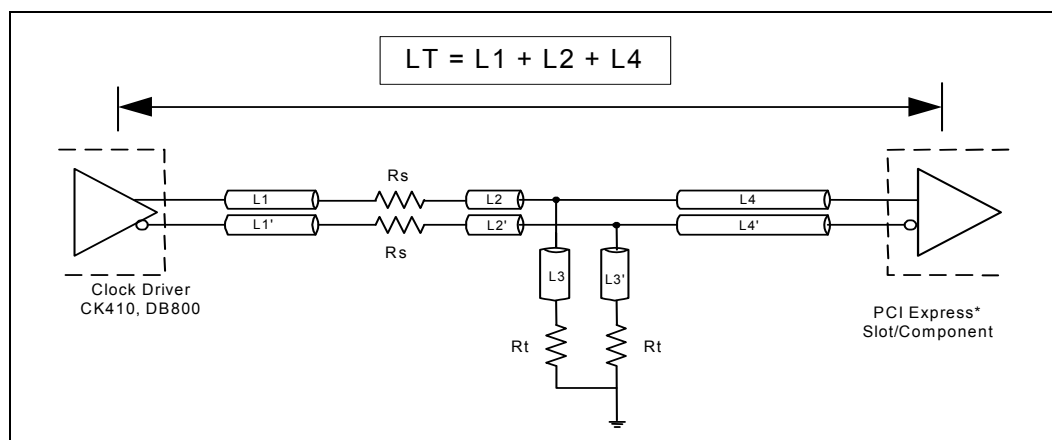
$$LT = L1 + L2 + L4$$

Clock Driver CK410, DB800

PCI Express* Slot/Component

Table 20. 100 MHz SRC/SRC# Clock Routing Guidelines for PCI Express Slot/Component

Parameter	Routing Guidelines	Figure	Notes
Trace Width – W[1]	microstrip: 4.5 mils stripline: 4.75 mils	Figure 57	1
SRC to SRC# spacing – S[1]	10 mils	Figure 57	2,3
SRC to Signal Spacing – S1 (includes spacing between SRC pairs)	20 mils	Figure 57	
Baseboard Impedance – Differential	100 Ω ±10%		2,3
Clock Routing Length (L1, L1'): Clock Driver to Rs	0.5 in max	Figure 56	4
Clock Routing Length (L2, L2'): Rs to Rs-Rt Node	0.1 in max	Figure 56	4
Clock Routing Length (L3, L3'): Rs-Rt Node to Rt	0.1 in max	Figure 56	4
Routing Length (L4, L4'): Any Clock driver (CK410/DB800) to component	Min: 3 in Max: 20 in	Figure 56	5
Routing Length (L4,L4'): Any Clock Driver (CK410/DB800) to PCI Express connector	Min: 3 in Max: 16 in	Figure 56	5
CLKN – CLKP Length Matching	within 5 mils		

Table 20.   100 MHz SRC/SRC# Clock Routing Guidelines for PCI Express Slot/Component

Parameter	Routing Guidelines	Figure	Notes
Rs Series Termination Value	33 Ω ±5%	Figure 56	
Rt Shunt Termination Value	49.9 Ω ±1%	Figure 56	

Notes:
1.   Routing guidelines are for the width is 4.5 mils with 10 mil spacing on layers 3 & 8. Use 4.5-mil line width and adjust the trace to trace air gap to achieve 100 Ω differential impedance.
2.   Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Maintain uniform spacing along the entire length of the trace. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
3.   The differential impedance of each clock pair is the critical parameter. Single-ended impedance may vary with different geometries.
4.   Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ringback.
5.   Single Ended (SE) Absolute Vmax/Vmin (Includes overshoot/undershoot) specs of the transceiver clock (CK410/DB800) 1.15v/-0.3v for some cases (means when the buffer is fast/Max) and differential edge rate Max spec of 4V/ns (receiver clk), the min length is required to 3″.

Figure 57.   Trace Spacing for 100 MHz SRC Clocks
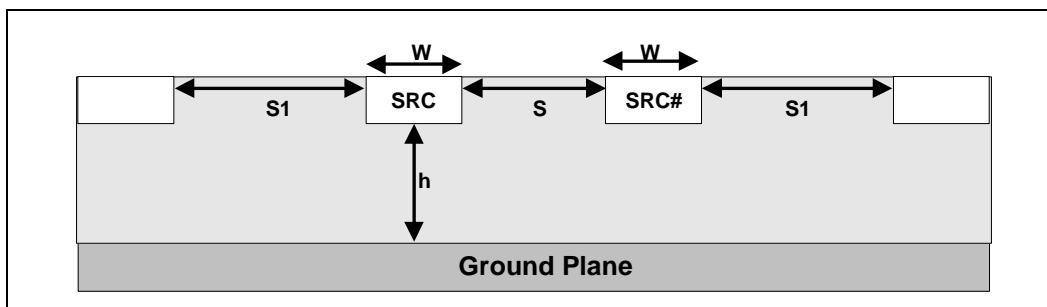
8.2.3   CLK33 Group

The driver in the CLK33 (PCICLK) group is the clock synthesizer 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer to the EP80579, LPC Clock, Port80, Firmware Hub, TPM, and SIO.

Figure 58.   33 MHz Clock Relationships
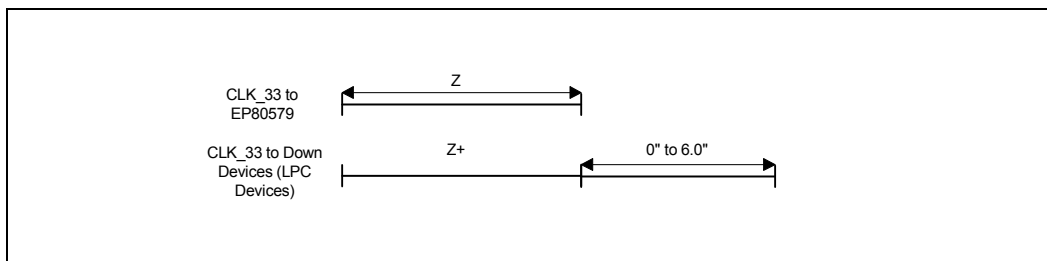
Notes:
1.   The 33 MHz clock to the EP80579 length, "Z", can be 2″ to 20″ long and will dictate the length of all other 33 MHz clock signals.
2.   Figure 58 will be referenced in all subsequent 33 MHz clock routing sections.

Figure 59.   Topology for CLK33 to Down Devices
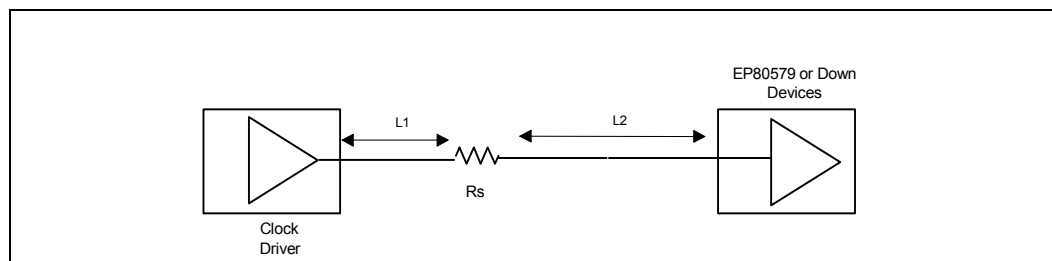
Table 21.   CLK33 Routing Guidelines to EP80579, FWH, and LPC Down Devices

Parameter	Routing Guidelines	Illustrations	Notes
Clock Group	CLK33: 33 MHz clocks - Port80, FWH, LPC, TPM, SIO, ICH_33MHz_CLK, ITP_PCI_CLK_33MHz		
Topology	Point-to-point	Figure 59	
Reference Plane	Ground referenced (contiguous over entire length)		1
Characteristic Trace Impedance (Z_0)	55 Ω ± 10%		
Trace Width (W)	microstrip: 4.5 mils stripline: 4.75 mils	Figure 60	2
Trace Spacing (S1)	20 mils	Figure 60	
EP80579, FWH, and other LPC down devices Trace Length (L1)	0.5" max	Figure 59	
EP80579 (L2)	L2 = Z = 2" to 20"	Figure 59	3, 4
FWH, Port80, TPM, SIO Trace Length (L2)	L2 = [Z + (0" to 6")] = 20" max	Figure 59	3, 4
Resistor	Rs = 43 Ω ±5%	Figure 59	4

Note:
1.   Ground referencing is preferred. However, CLK33 can be routed referenced to other planes if the plane is contiguous from source to destination
2.   Trace width is stackup dependent. Routing guidelines are for the width is 4.5 mils with 6.25 mil spacing on layers 3 & 8.
3.   Length Z = L1 + L2, from Figure 58.
4.   The value of Rs may need to be increased for shorter trace lengths to minimize overshoot / undershoot effects.

Figure 60.   Trace Spacing for CLK33 (PCICLK) Clock
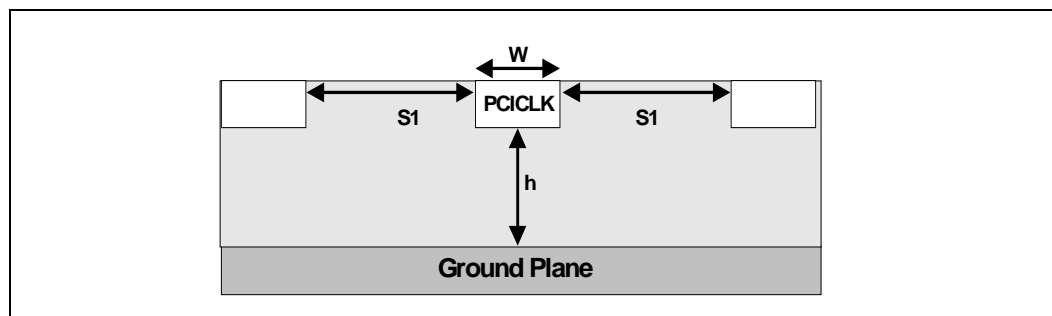
8.2.3.1 Sharing 33 MHz Clocks

In some cases, the designer may have a need to share one 33 MHz clock between two down devices (this is not implemented on the development platform). In this case, the driver is the clock synthesizer 33 MHz clock output buffer and the receivers are the 33 MHz clock input buffers of two separate down devices.

Figure 61. Topology for Sharing CLK33 Between Two Down Devices
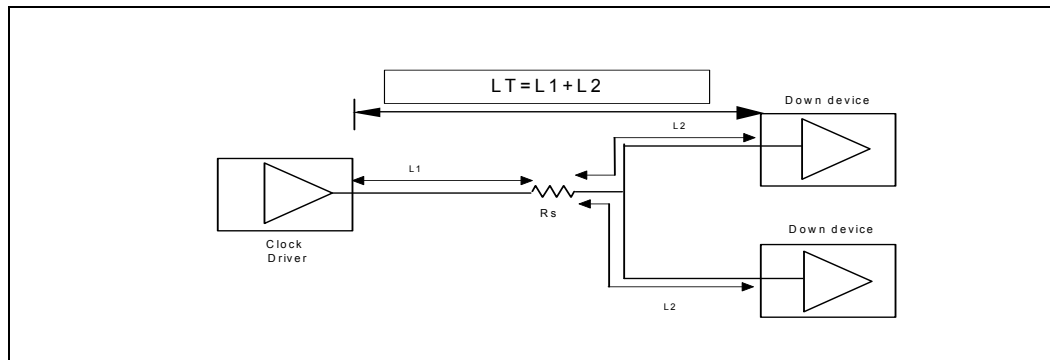
Table 22. CLK33 Routing Guidelines for Two Down Devices

Parameters	Routing Guidelines	Illustrations	Notes
Clock Group	CLK33: 33 MHz clock		
Topology	Balanced T Topology	Figure 61	
Reference Plane	Ground referenced (contiguous over entire length)		1
Characteristic Trace Impedance (Z_0)	55 Ω ± 10%		
Trace Width (W)	4.5 mils (Target Z_0 first)	Figure 60	
Trace Spacing (S1)	20 mils	Figure 60	
Resistor	Rs = 12 Ω ±5%	Figure 61	2
Clk Driver to Rs for PCI Down Devices (L1)	0.5" max	Figure 61	
Rs to Down Device (L2)	L2 = [Z + (0" to 6")] = 20" max. L2 lengths should be matched to within 250 mils of each other.	Figure 61	3

Notes:
1. Ground referencing is preferred. However CLK33 can be routed referenced to other planes assuming that the plane is contiguous from source to destination.
2. The value of Rs may need to be increased for shorter trace lengths to minimize overshoot / undershoot effects.
3. Length "Z" is the distance from the 33 MHz clock driver to the EP80579 33 MHz input buffer. "Z" can be 2" to 20" long.

8.2.4 CLK14 Group

The driver in the CLK14 group is the clock synthesizer 14.318 MHz clock output buffer and the receiver is the 14.318 MHz clock input buffer at the EP80579 and SIO.

Figure 62.   Topology for CLK14
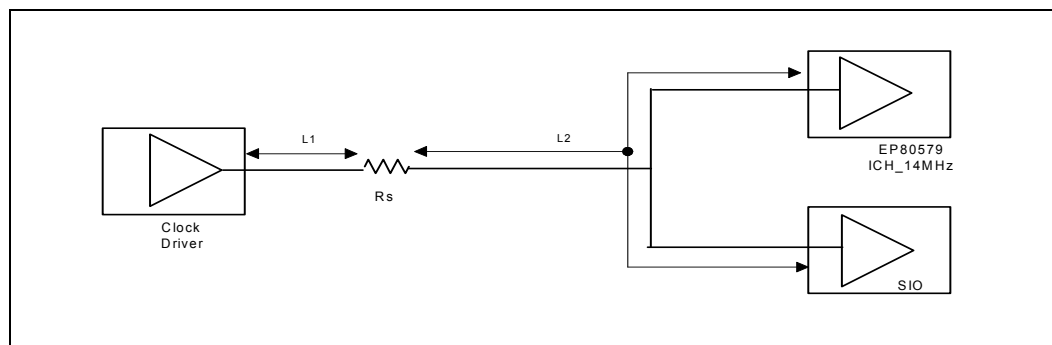
Table 23.   CLK14 Group Routing Guidelines

Parameter	Routing Guidelines	Figure
Signal Group	CLK14: 14 MHz Clock -- LPC_14MHz_CLK, ICH_14MHz_CLK	
Reference Plane	Ground Referenced	
Layer Assignment	Layers 8	
Characteristic Trace Impedance (Zo)	50 Ω ±10% (single ended)	
Nominal Trace Width	4.5 mils	Figure 63
Nominal Trace Spacing	Edge to Edge within CLK14 Group: 10 mils Edge to Edge not in CLK14 Group: 10 mils	Figure 63
Routing Length – L1: Clock Driver to Rs	0.1 in. max	Figure 62
Routing Length – L2: Rs to EP80579 SIO	18 in. max	Figure 62
REFCLK total length (L1+L2)	(L1+L2) to EP80579 must be within 0.500 inches of (L1+L2) to SIO	Figure 62
Resistors	Single Load: Rs = 43 Ω ±5% Double Load: Rs = 33 Ω ±5% Triple Load: Rs = 12 Ω ±5%	Figure 62
Skew Requirements (to other clock groups)	None	Figure 62

Figure 63.   Trace Spacing for CLK14 (REFCLK) Clocks
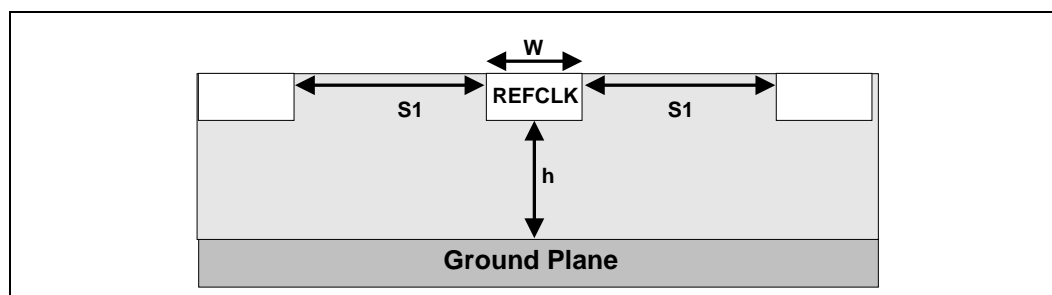
8.2.5   CLK48 Group

The driver in the CLK48 group is the clock synthesizer USB clock output buffer, USB_48. The receivers are the CLK48 input buffers on the EP80579.

Note: These clocks are asynchronous to any other clock on the board.

Figure 64. Topology for CLK48 Group
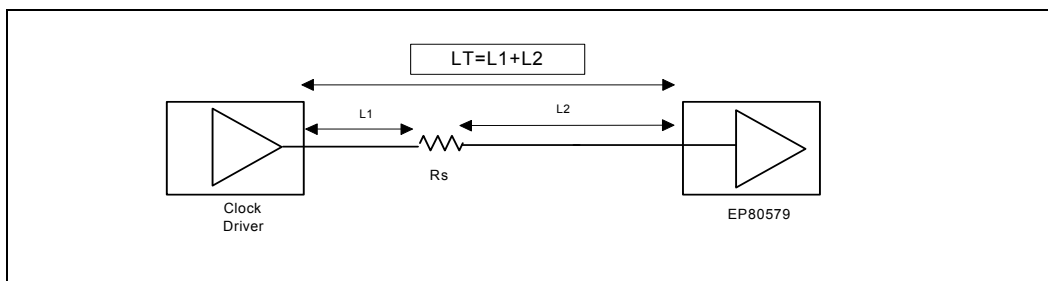
Table 24. CLK48 Routing Guidelines

Parameter	Routing Guidelines	Figure
Signal Group	CKL48 USB	
Reference Plane	Ground Referenced	
Layer Assignment	Layer 3	
Characteristic Trace Impedance (Zo)	50 Ω ±10% (single ended)	
Nominal Trace Width (W)	4.5 mils	Figure 65
Nominal Trace Spacing (S1)	20 mils	Figure 65
Routing Length – L1: Clock Driver to Rs	0.5 in. max	Figure 64
Routing Length – L2: Rs to Device Down or Connector	2 in. to 20 in. max	Figure 64
Resistor	Rs = 43 Ω ± 5%	Figure 64
Skew Requirements (to other clock groups)	None – USBCLK is asynchronous to other clocks on the board	Figure 64
Maximum via Count	2	

Figure 65. Trace Spacing for CLK48 (USBCLK) Clocks
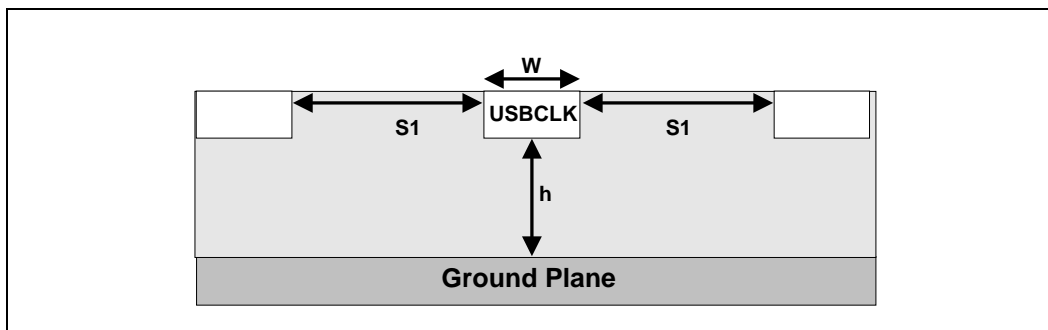
8.3 CK410 General Design Guides

8.3.1 Clock Driver Decoupling

- For all power connection to planes, decoupling caps and vias, the maximum trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.
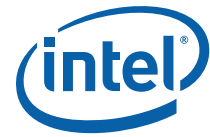
- The VSS pins should not be connected directly to the VSS side of the caps. They should be connected to the ground flood under the part which is via'd to the ground plane in order to avoid VDD glitches propagating out, getting coupled through the decoupling caps to the VSS pins. This method has been shown to provide the best clock performance.

- The ground flood should be via'd through the ground plane with no less than 12 to 16 vias under the part. It should be well connected.

- For all power connections, heavy duty and/or dual vias should be used.

- It is imperative that the standard signal vias and small traces not be used for connecting decoupling caps and ground floods to the power or ground planes.

8.3.2   Clock Power Delivery

Designers must take special care to provide a quiet VDDA supply to the Ref VDD, VDDA and the 48 MHz VDD. These VDDA signals are especially sensitive to switching noise induced by the other VDDs on the clock chip. They are also sensitive to switching noise generated elsewhere in the system such as the processor voltage regulator. It is recommended that a ground flood (Section 8.3.1, "Clock Driver Decoupling" on page 103) be placed directly under the clock chip to provide a low impedance connection for the VSS pins. In addition, power vias should be distributed evenly throughout the ground flood.

Note: For all power connections to planes, decoupling capacitors, and vias, the maximum trace width allowable and shortest possible lengths should be used to ensure the lowest possible inductance.

8.3.3   Decoupling Caps and Ferrite Beads

Figure 66 shows the six different power groupings found on the CK410 and listed in Table 25.

Figure 66.   Clock Power Groupings for Decoupling / Filtering
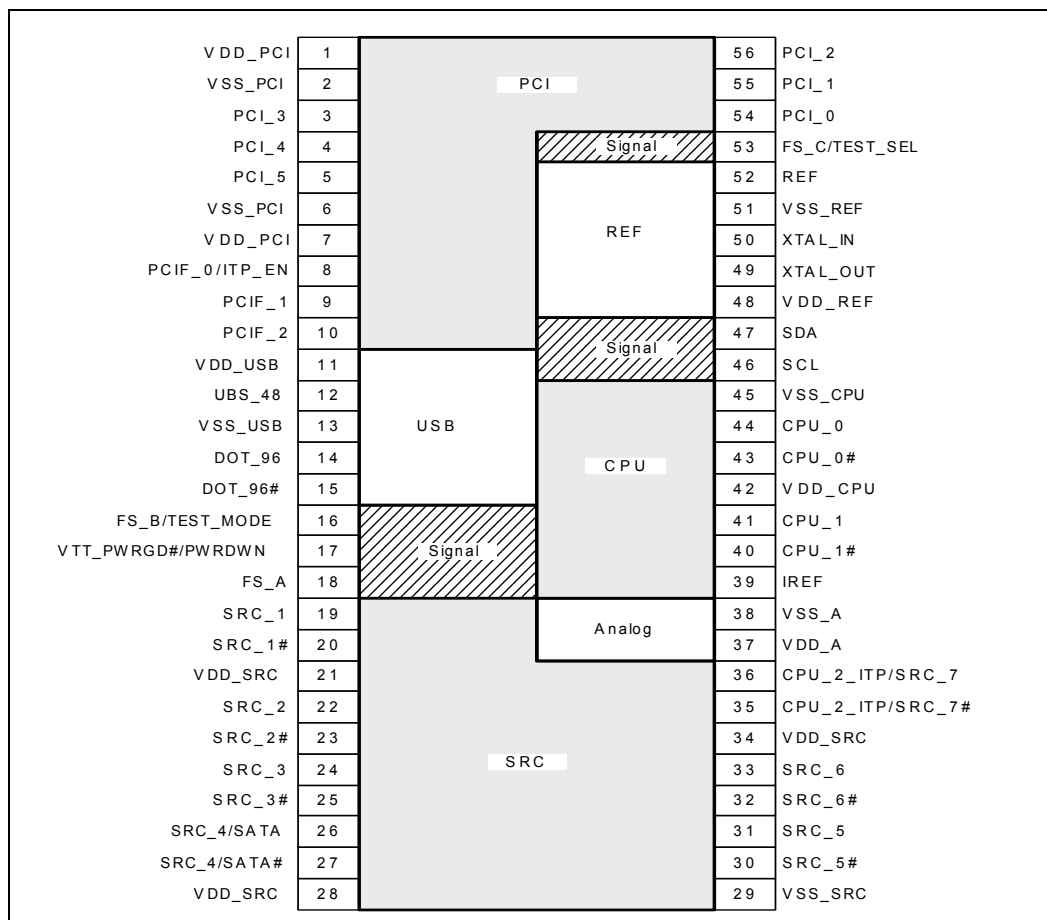
Table 25.   Clock Grouping for Decoupling / Filtering

Clock Group	Signals in Group
Analog	VDD_A, VSS_A
SRC	SRC[7:1], SRC[7:1]#, VDD_SRC, VSS_SRC
CPU	IREF, CPU[1:0], CPU[1:0]#, VSS_CPU, VDD_CPU
PCI	VDD_PCI, VSS_PCI, PCI[5:0], PCIF[2:0]
REF	XTAL_OUT, XTAL_IN, VSS_REF, VDD_REF, REF
USB	VDD_48, USB_48, VSS_48, DOT 96, DOT 96#

Figure 67 shows the CK410 decoupling capacitors and ferrite beads that are associated with the different clock output groupings:
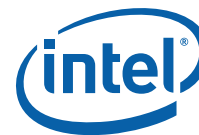
Figure 67. Decoupling and Filtering Per Clock Group
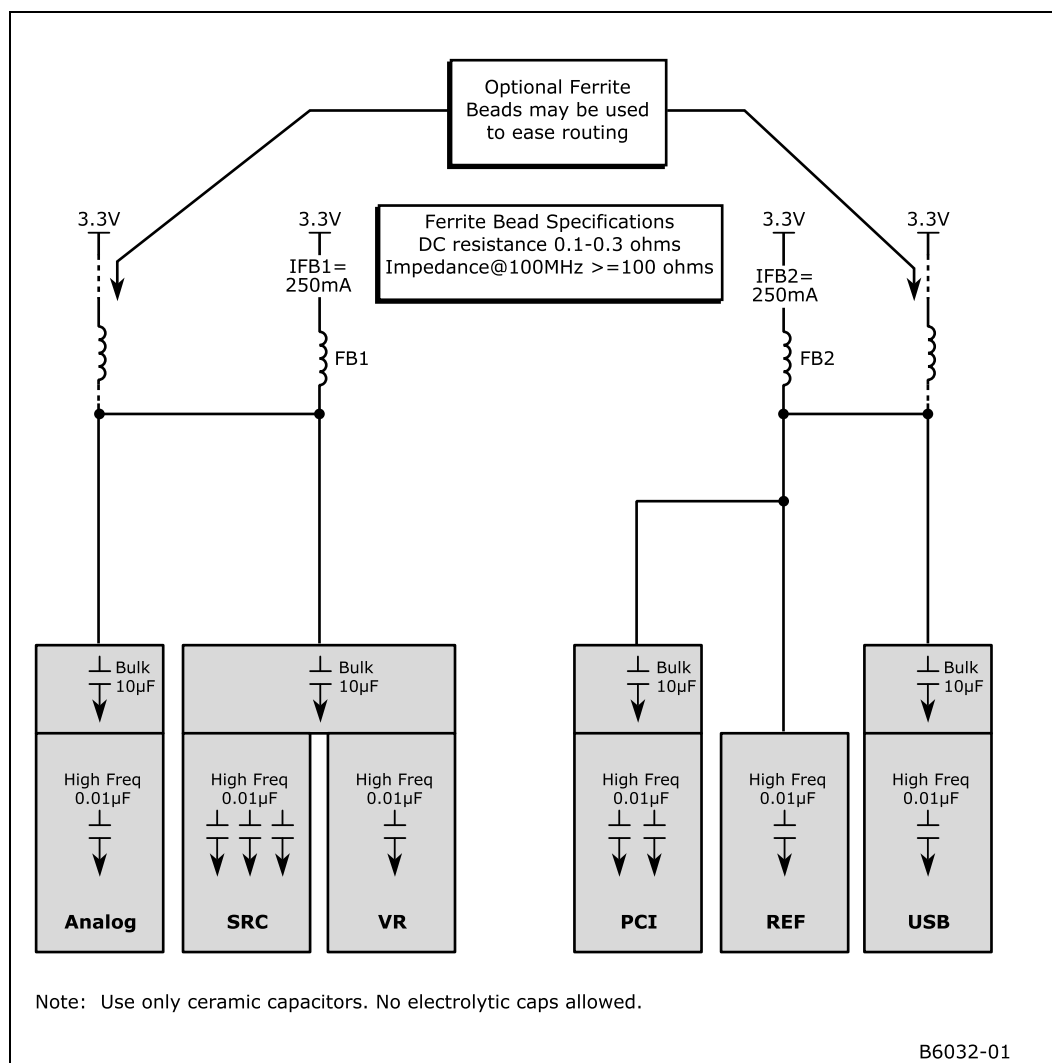
8.3.4 CK410 Power Plane Filtering

8.3.4.1 VDD Plane Filtering

The VDD decoupling requirements for a CK410 compliant clock synthesizer are as follows:

- One 300 Ω (100 MHz) Ferrite Bead is recommended for the VDD plane.
- 10 μF of bulk decoupling cap in a 1206 package placed close to the VDD generation circuitry is recommended for the VDD plane. Two 4.7 μF caps can also be used in place of the 10 μF cap.
- Seven 0.1 μF high-frequency decoupling caps in the 0603 packages should be placed as close to each VDD pin as possible.

8.3.4.2 VDDA Plane Filtering

The VDDA decoupling requirements for a CK410B compliant clock synthesizer are as follows:

- One 300 Ω (100 MHz) Ferrite Bead is recommended for the VDDA plane.
- 10 µF of bulk decoupling cap in a 1210 package placed close to the VDDA generation circuitry is recommended for the VDDA plane. Two 4.7 µF caps can also be used in place of the 10 µF cap.
- One 0.1 µF high-frequency decoupling cap in the 0603 packages should be placed as close to each VDDA pin as possible.

8.3.4.3 VDD_48 Plane Filtering

The VDD_48 decoupling requirements for a CK410B compliant clock synthesizer are as follows:

- One 10 Ω series resistor is recommended for the VDD_48 plane.
- One 10 µF of bulk decoupling cap in a 1210 package placed close to the VDD_48 generation circuitry is recommended for the VDD_48 plane.
- One 0.1 µF high-frequency decoupling cap in the 0603 packages should be placed as close to each VDD_48 pin as possible.

8.3.4.4 Layer 1 Ground Flood

The following drawings show examples of how to create a ground flood underneath the CK410 and connect the decoupling caps in such as way as to minimize noise coupling onto the Layer 1 ground flood.

Figure 68.   Ground Flood on Layer 1 Underneath CK410
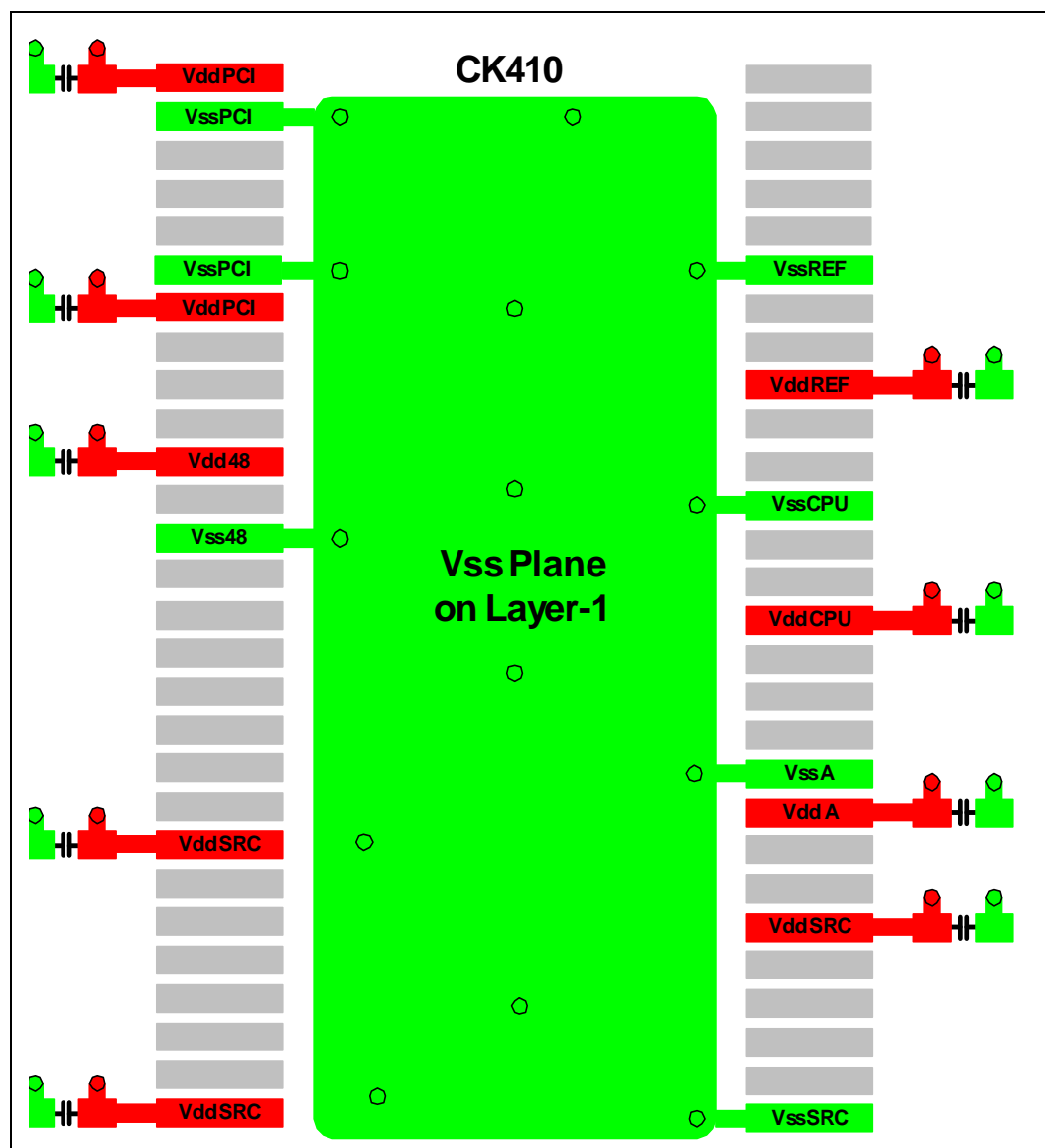
Figure 69. Edge Decoupling Caps – Examples
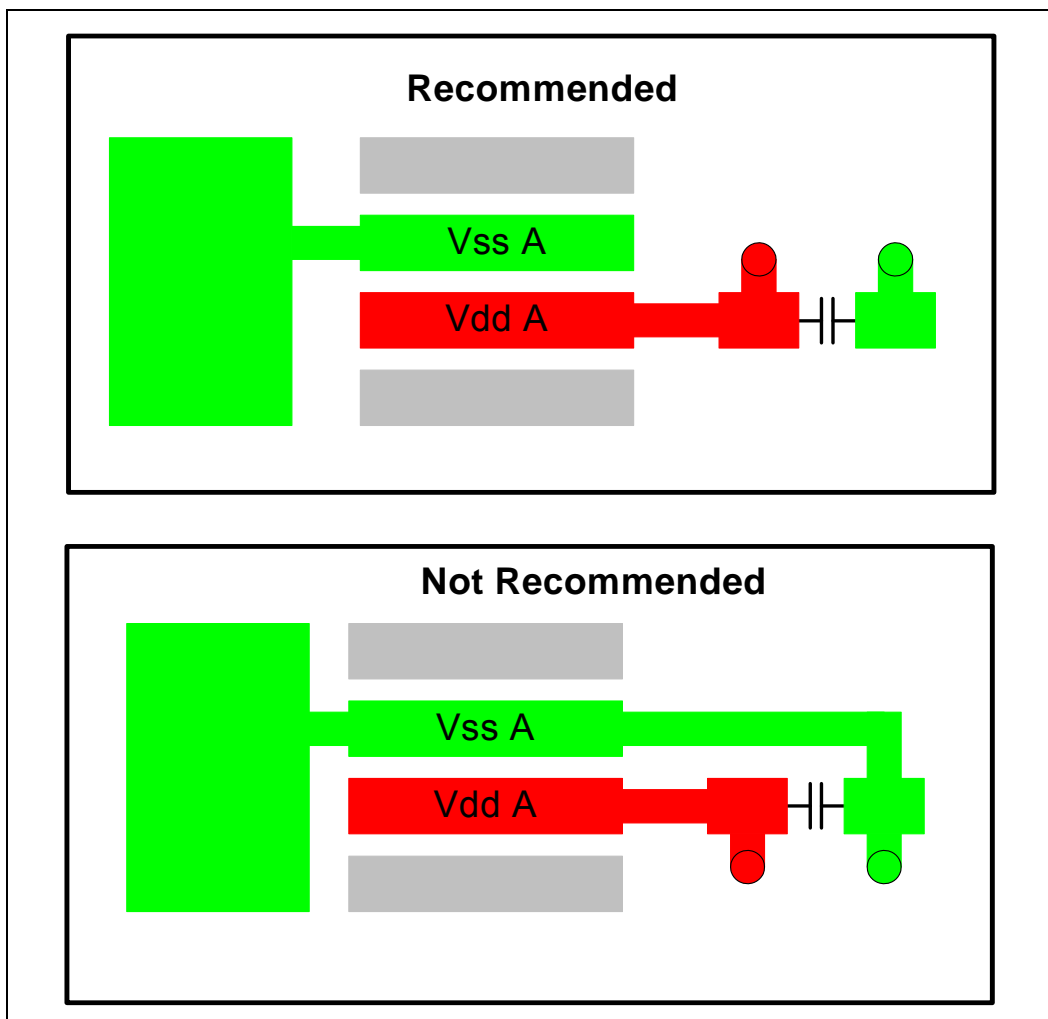
Figure 70. Decoupling Capacitors Placement and Connectivity
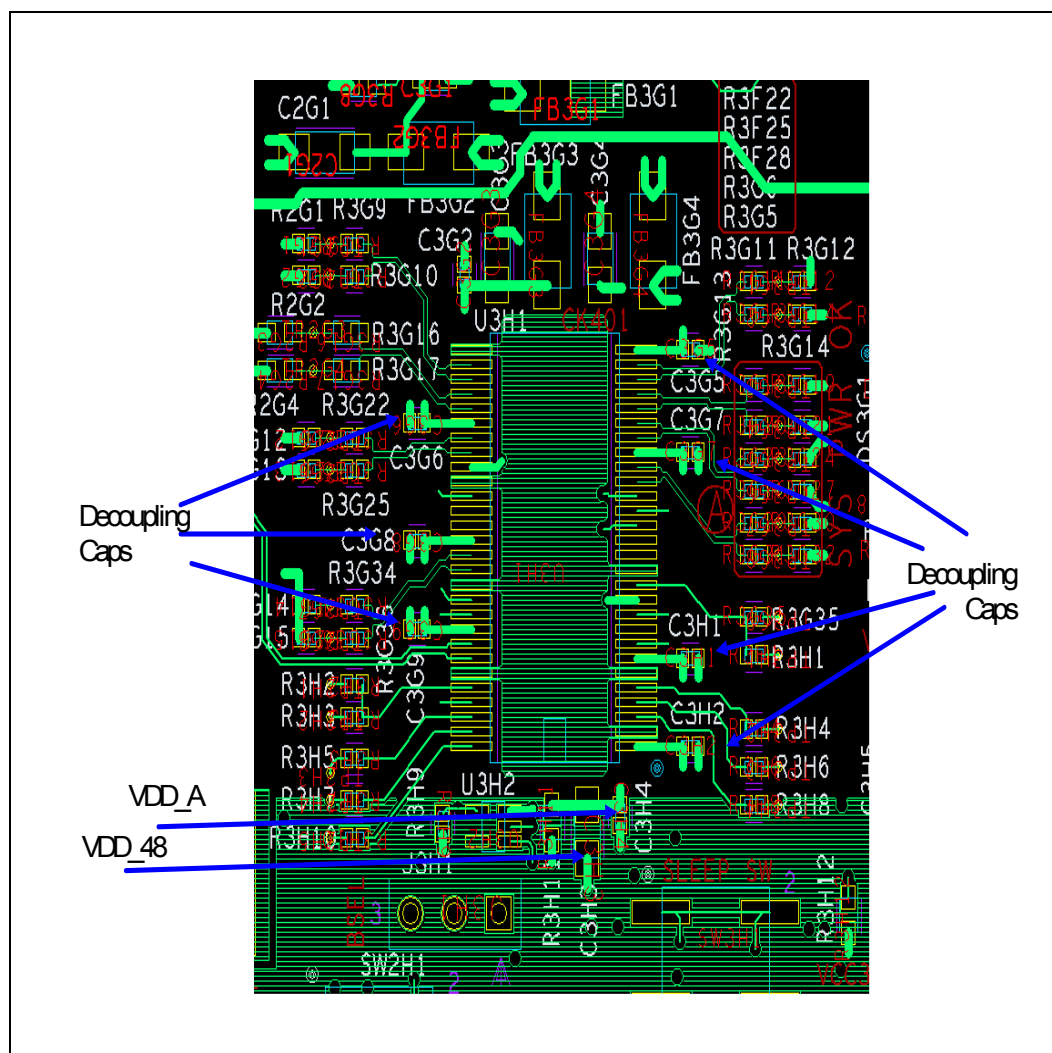
8.3.5 IREF

The IREF pin on the CK410 is connected to ground through a 475 Ω ±1% resistor, making the IREF 2.32 mA.

8.3.6 EMI Constraints

Clocks are a significant contributor to EMI. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two signals of each differential clock pair.
- Route clocks on physical layer adjacent to the VSS reference plane only.
- Use pull-down resistors to pull-down the unused clock signals to ground plane. This prevents signals floating.

9.0 System Memory Interface (DIMM)

This chapter contains topologies and routing guidelines for the EP80579 DDR2 system memory interface. It provides the DDR2 implementation solution for system designs requiring two DIMMs, unbuffered or registered, operating at 400/533/667/800 MT/s speed rates. This chapter **does not** provide guidelines for memory down design implementations.

9.1 Terminology and Definitions

Table 26.   DDR Terminology

Acronym	Description/Comment
Unbuffered memory	Memory that does not contain buffers or registers located on the module. The memory controller directly communicates with the memory devices.
Buffered memory	Memory that contains buffers on the module that re-drive signals from the memory controller to the memory devices. ***Note:*** EP80579 does not support this feature.
Registered memory	Memory that contains registers on the module that register and re-drives the signals from the memory controller to the memory devices.
Self-refresh	Memory technology that is built in the DRAM that refreshes on its own.
Page size	Minimum number of column locations on any row and are accessed by a single ACTIVATE command
DRAM devices	Multiple DRAM devices together make up a DIMM
Rank	Defines a set of DRAM chips (on a module) comprising 8 byte wide (64/32 bits) data, or 9 bytes (72/40 bits) with ECC. All devices in a Rank are connected by a single chip select. The actual memory size is not defined. Single-sided memory modules are always single-rank. Double-sided unbuffered and registered DIMMs are always dual-rank.

9.2 Supported Configurations

Table 27 shows the various DDR2 device technologies supported by the EP80579.

Table 27.   Supported DDR2 Device Densities and Widths

Technology		Support
Device Density	Device Width	
256 Mb	x8	Supported
512 Mb	x8	Supported
1 Gb	x8	Supported
2 Gb	x8	Supported
4 Gb	x8	Not Supported

Table 28 shows the various capacity configurations supported by the memory controller in the 64b mode. The first column shows the total DRAM capacity on the channel. The remaining columns indicate the DRAM devices features, densities and the number of devices required to achieve the given capacity. A single-sided DIMM is indicated by 0 parts populated on side B. A double-sided DIMM has parts populated on both sides.

For each configuration, an additional DRAM part per side is required to support ECC bits. A x8 part provides all the bits required for ECC.

In the 64b configuration, the minimum capacity supported by the memory controller is 256 MB and the maximum capacity supported is 4 GB.

Table 28. Supported DRAM Capacity for 64-bit Mode

Total DRAM Capacity	DRAM Technology		Total # of Parts on Side A (without ECC)	Total # of Parts on Side B (without ECC)
	DRAM Part Density	DRAM Part Width		
256 MB	256 Mb	x8	8	0
512 MB	256 Mb	x8	8	8
	512 Mb	x8	8	0
1 GB	512 Mb	x8	8	8
	1 Gb	x8	8	0
2 GB	1 Gb	x8	8	8
	2 Gb	x8	8	0
4 GB	2 Gb	x8	8	8

Table 29 shows the various configurations supported by the memory controller in the 32b mode.In the 32-bit mode only single rank DDR2 devices are supported. In this mode, the minimum capacity supported by the memory controller is 128 MB and the maximum capacity supported is 1 GB.

Table 29. Supported DRAM Capacity for 32-bit Mode

Total DRAM Capacity	DRAM Technology		Total # of Parts on Side A (without ECC)	Total # of Parts on Side B (without ECC)
	DRAM Density	DRAM Part Width		
128 MB	256 Mb	x8	4	0
256 MB	512 Mb	x8	4	0
512 MB	1 Gb	x8	4	0
1GB	2 Gb	x8	4	0

Note: In the 32b mode, all unused EP80579 DDR2 Data Bus Interface signals should be pulled high to DDR2 1.8V through 10 Kohm resistors.

Table 30 shows the supported DDR2 device speed grades for single and Dual DIMMs. Dual DIMM support uses 2N or 2T command/address timing.

Table 30. Supported DDR2 Data Speeds

DDR Speed	1 DIMM 1 rank	1 DIMM 2 ranks	2 DIMMs 1 rank each
DDR2-400	R = 1T UB = 1T	R = 1T UB = 1T	R = 1T UB = 2T
DDR2-533	R = 1T UB = 1T	R = 1T UB = 1T	R = 1T UB = 2T
DDR2-667	R = 1T UB = 1T	R = 1T UB = 1T	R = 1T UB = 2T
DDR2-800	R = 1T UB = 2T	R = 1T UB = 2T	Not supported
R = Registered UB = Unbuffered 1T = 1T Address/Command Timing 2T = 2T Address/Command Timing			

9.3 Rules for Populating DIMM Slots

Table 31 shows the supported DIMM population of the 2 ranks supported by the EP80579. Configurations not shown in Table 31 are not supported. The rank configurations supported are one or two ranks on a single DIMM or one rank on each of the two DIMMs. Two ranks in each of the two DIMMs (that is, four ranks) is not supported.

Table 31. Supported DIMM Populations

	DIMM1		DIMM0	
	Rank0	Rank1	Rank0	Rank1
1 - Single Rank	Empty	Empty	CS0	Empty
1 - Dual Rank	Empty	Empty	CS0	CS1
2 - Single Rank	CS1	Empty	CS0	Empty
TABLE KEY: CS0/CS1: Chip Selects				

9.3.1 Supported Rank Configurations

Table 32 shows the supported rank configurations when using two ranks for the single and dual DIMM.

Table 32. Supported DDR2 Rank Configurations in Single and Dual DIMM mode (Sheet 1 of 2)

Single DIMM (64 bits - rank 0 & rank 1) (32 bits - rank 0 only)		Dual DIMM (64 bit only)	
Rank 0	Rank 1	Rank 0, DIMM 1	Rank 0, DIMM 0
128 MB (32 bit only)	NA	NA	NA
256 MB	256 MB	256MB	256 MB, 512 MB, 1GB, 2 GB

Table 32. Supported DDR2 Rank Configurations in Single and Dual DIMM mode (Sheet 2 of 2)

Single DIMM (64 bits - rank 0 & rank 1) (32 bits - rank 0 only)		Dual DIMM (64 bit only)	
512 MB	512 MB	512 MB	256 MB, 512 MB, 1 GB, 2 GB
1 GB	1 GB	1 GB	256 MB, 512 MB, 1 GB, 2 GB
2 GB	2 GB	2 GB	256 MB, 512 MB, 1 GB, 2 GB

9.3.2 DRAM Addressing

Table 33, Table 34, Table 35 and Table 36 show the DRAM device addressing for the various DDR2 device technologies and densities supported by the memory controller.

Note that:

- x4 and x 16 devices are not supported.
- 4Gb and higher device density parts are not supported.
- See Table 32 for the supported device densities and widths.

Table 33. 256Mb Addressing

Configuration	DDR2 32 Mb x 8
# of Banks	4
Bank Address	BA0, BA1
Auto Precharge	A10
Row Address	A0-A12
Column Address	A0-A9
Page Size	1KB

Table 34. 512Mb Addressing

Configuration	DDR2 64 Mb x 8
# of Banks	4
Bank Address	BA0, BA1
Auto Precharge	A10
Row Address	A0-A13
Column Address	A0-A9
Page Size	1KB

Table 35.   1Gb Addressing

Configuration	DDR2 128 Mb x 8
# of Banks	8
Bank Address	BA0-BA2
Auto Precharge	A10
Row Address	A0-A13
Column Address	A0-A9
Page Size	1KB

Table 36.   2Gb Addressing

Configuration	DDR2 256 Mb x 8
# of Banks	8
Bank Address	BA0-BA2
Auto Precharge	A10
Row Address	A0-A14
Column Address	A0-A9
Page Size	1KB

9.3.3 DDR2 DIMM Ordering Overview

Figure 71 shows the DIMM ordering and location.

Figure 71. DDR-DIMM- Implementation
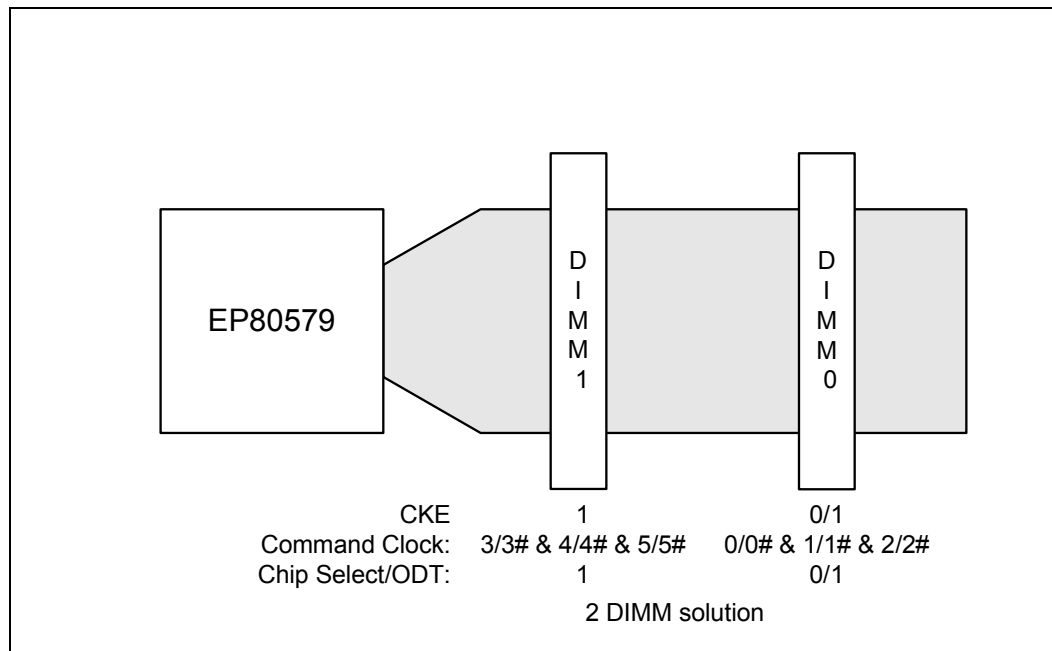
A platform design requires single rank DDR2 DIMMs to be populated in order, starting with the DIMM furthest from EP80579 (DIMM0 - primary DIMM) in a "fill-farthest" approach (see Figure 71). In addition, dual-rank DIMMs must be populated farthest from the EP80579 since only one dual rank DIMM is supported. This recommendation is based on the chip select and on-die termination signals routing requirements of the DDR2 interface. Intel recommends checking for correct DIMM placement during BIOS initialization. Additionally, all designs should follow the DIMM ordering, clock enable routing, command clock routing, and chip select routing documented in Figure 71. This addressing must be maintained to be compliant with the reference BIOS code.

Figure 72. Example of One Single-Rank DIMM Population
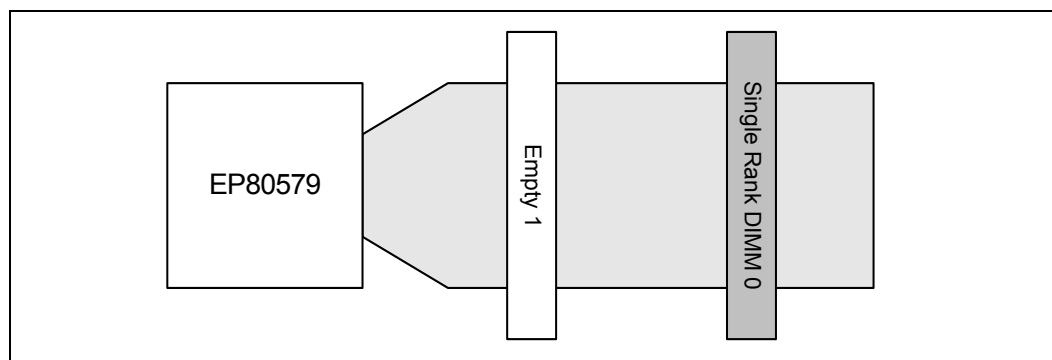
Figure 73.   Example of Two Single-Rank DIMM Population
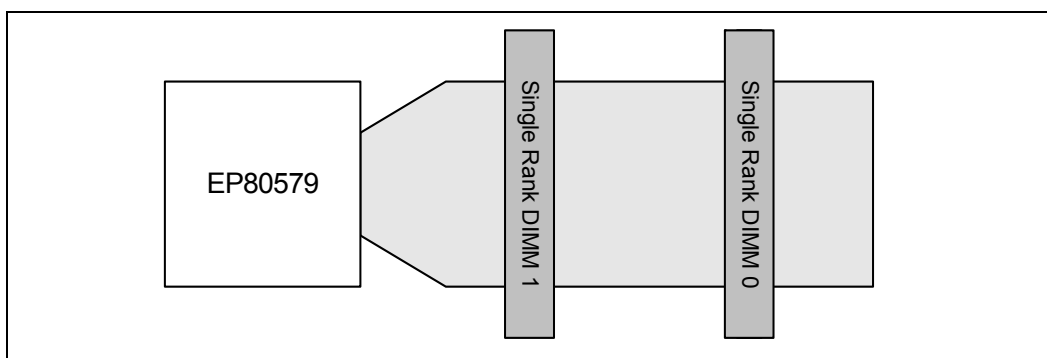
Figure 74.   Example of Dual-Rank DIMM Population
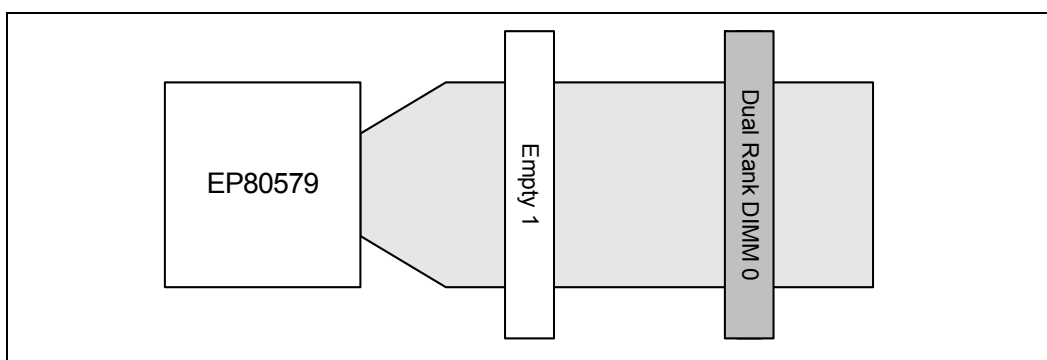
9.4   System Memory Design Guidelines

The EP80579 has a single channel memory interface. The channel consists of 64 data and 8 ECC bits. The pinout for the channel has been optimized for a baseboard design with two DDR2 DIMMs. The DIMM closest to EP80579 is DIMM1, and the farthest is DIMM0.

As stated in Section 9.3.1, in the 64b configuration, the minimum capacity supported by the EP80579 is 256 MB and the maximum capacity supported is 4 GB.

The system memory interface can be divided into five signal groups:

- source synchronous (data)
- address/command
- control
- clocks
- DC bias signals

Table 37 summarizes the different signal groupings.

Table 37.   DDR2 Signal Groups (Sheet 1 of 2)

Group	Signal Name	Description
Data, Mask, & Strobe		
Byte 0	DDR_DQ[0..7], DDR_DM0, & DDR_DQS0/DQS0#	Data Byte Lane0
Byte 1	DDR_DQ[8..15], DDR_DM1, & DQS1/ DDR_DQS1#	Data Byte Lane1
Byte 2	DDR_DQ[16..23], DDR_DM2, & DQS2/ DDR_DQS2#	Data Byte Lane2
Byte 3	DDR_DQ[24..31], DDR_DM3, & DQS3/ DDR_DQS3#	Data Byte Lane3
Byte 4	DDR_DQ[32..39], DDR_DM4, & DDR_DQS4/DQS4#	Data Byte Lane4
Byte 5	DDR_DQ[40..47], DDR_DM5, & DDR_DQS5/DQS5#	Data Byte Lane5
Byte 6	DDR_DQ[48..55], DDR_DM6, & DDR_DQS6/DQS6#	Data Byte Lane6
Byte 7	DDR_DQ[56..63], DDR_DM7, & DDR_DQS7/DQS7#	Data Byte Lane7
Byte 8	DDR_ECC[0..7], DDR_DM8, DDR_DQS8/DQS8#	Data Byte Lane 8 (ECC Check Bits)
Control		
Control	DDR_CKE[1:0]	Clock Enables - One per DIMM Rank
	DDR_CS#[1:0]	Chip Selects – One per DIMM Rank
	DDR_ODT[1:0]	On-Die-Termination – One per DIMM Rank
Address & Command		
Address / Command	DDR_MA[14:0]	Memory Address
	DDR_BA[2:0]	Bank Address (Bank Select)
	DDR_RAS#	Row Address Select
	DDR_CAS#	Column Address Select
	DDR_WE#	Write Enable (Output)
Clocks		
Clocks	DDR_CLK[5:0]/ DDR_CLK#[5:0]	Differential Clocks – Three pairs per DIMM
DC Bias		

Table 37. **DDR2 Signal Groups (Sheet 2 of 2)**

Group	Signal Name	Description
DC Bias (I/O)	DDR_CRES[2:0]	• DDR_CRES[2:1] - Impedance compensation resistors. • DDR_CRES[0] - Common return for DDR2 interface compensation resistors on DDV_CRES, DDR_SLWCRES and DDR_RCOMPX
	DDR_SLWCRES	Slew rate compensation for DDR2 interface (Analog)
	DDR_RCOMPX	Impedance compensation for DDR2 interface
	DDV_CRES	DDR2 resistor
	DDR_VREF	Voltage Reference (Analog)

9.5 Package Length Compensation

Package length compensation is required for total routing length requirements, see the length matching rules listed in Table 38. See the DDR2 Package length information in the *Intel® EP80579 Integrated Processor Product Line Datasheet* for more information.

9.6 Length Matching and Length Formulas

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width, spacing geometries, and absolute minimum and maximum routed lengths for each signal group. These guidelines are recommended to achieve optimal signal integrity and timing.

Table 38. **Length Matching Formulas between EP80579 and DDR2 DIMM**

Source/Destination	Signal Group to matching signal	Total Length Matching Tolerances	Comments
EP80579 Pad to DDR2 DIMM	DQS to DQ/DM	DQS = DQ/DM + 400 mils	1, 2
	DQS to clock	DQS = CLK/CLK# ± 500 mils	2
	CMD/ADD to Clock	CMD/ADD = CLK/CLK# ± 20 mils	2
	CTRL to CMD/ADD	CTRL = CMD/ADD + 2.5 inches	2
	Clock to Clock#	CLK[x] = CLK[x]# ±10 mils	2

Notes:
1. Length matching is only required within each Byte lane. Signal length matching is not required outside the Byte lane. For example, any signal within DQ [0:7] need not be length matched to DQS [3].
2. Total length means - L_{PKG} + L_{BREAK} + L_{ROUTE}

9.7 DDR2 Interface System Interconnect

Figure 75 provides a block diagram of the system interconnect between the EP80579 DDR2 Memory Controller and the two DIMMs for the signal groups provided in Table 37. The Command/Address and Control signals require external terminations. External terminations are not required for DQ and DQS signals since both the EP80579 and the SDRAMs contain internal ODT. The following sections provide the detailed topology and routing guidelines for each of the signal groups.

Figure 75. DDR2 Interfaced System Interconnect
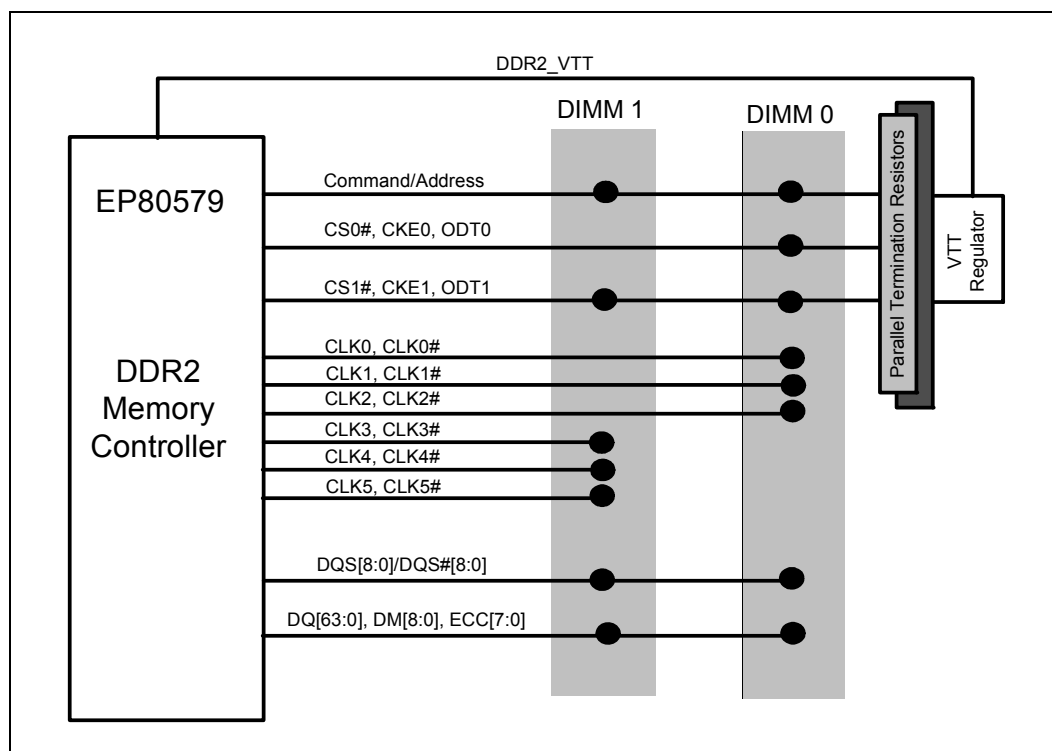
9.7.1 Topologies and Routing Guidelines

9.7.1.1 DDR2 Data and Strobe Signals – DQ/DM/ECC/DQS

The Data and Strobe topology shown in Figure 76 and Figure 77 is the same for each Data Byte Group (See Table 37). The DQS signals must be routed as differential pair with a skew between of ± 10mils. All signals in same byte lane should be matched within 20 mils of each other. (For example, DQS0[+/-], DQ[0..7] and DM0 are in the same byte lane).

All trace impedances should be 40 ohm± 10%. The parameters provided in Table 39 are targeted for 40 ohm.

Figure 76. Data Signal Daisy Chain Routing Topology
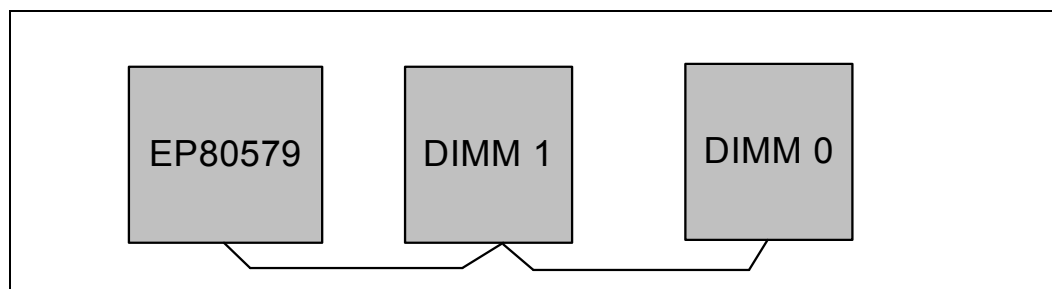
Figure 77. Data/Mask/Strobe Signal Routing Topology Diagram

Table 39. Data and Strobe Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines		Figure
	Data Byte Lane		
	Data & Data Mask	**Strobe**	
Signal Group	Data & Mask (DQ & DM)	Byte Strobe (DQS/DQS#)	
Topology	Daisy Chain		Figure 76
Reference Plane	Ground Referenced		
Characteristic Trace Impedance (Zo)	Single Ended Impedance = 40Ω ±10%		
Layer assignment	• Layers 3/8 • Signals within the same Byte Lane must routed on the same layer		
Nominal Trace Width	A = See Package signal B = 4 mils (Width), 4 mils (Spacing) C = D = 6.5 mils		Figure 77
Trace-to-Trace spacing (e2e)	A = See Package Signals B = 4 mils C = D = 15 mils (min)	• Inter-pair Spacing:-- DQS/DQS# = 6 mils (min) • Pair-to-Pair Spacing: 15 mils (min)	Figure 77
Clearance from other signals	20.0 mils (min)		

Table 39.   Data and Strobe Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guidelines		Figure
	Data Byte Lane		
	Data & Data Mask	**Strobe**	
Board Routing Guidelines			
Total Trace Length (TTL) = (L_{PKG} + L_{BREAK} + L_{ROUTE} + L_{D2D})	2.0 in - 6.0 in	Max TTL (DQS/DQS#) = Min TTL (DQ/DM) + 400 mils	Figure 77
L_{PKG}	See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information.		
L_{BREAK}	B = 0.8 in (max)		
L_{ROUTE}	C = 2.0 in - 4.0 in	Calculate while taking into account Strobe Max Trace Length (Max TTL)	
L_{D2D}	D = 0.8 in (max) (including both DIMMs' break-in fields)		
Length/Skew Matching Rules			
Length Tuning Requirements	• Only length matching is required within each Byte lane. No signal length matching is required outside the Byte lane. For example, any signal within Data Byte Lane 0 (DQ [0...7]) need not be length matched to DQS1 • DQ/DM should match each other to 20 mils or less within the same byte lane. (See Figure 78)	• The trace length difference between DQS and DQS# should not be more than 10 mils. - that is, DQS[x] = DQS[x]#±10 mils, x = 0.. 8 • Length match the data strobes (DQS/DQS#) to the associated data mask and data (DQ/DM) signals for each Data Byte Lane: Max(DQS/DQS#) = Min(DQ/DM[x]) + 400 mils, x = 0.. 8	
	• Length match all DIMM-to-DIMM (D2D) signals (DQ/DM/DQS/DQS#) to 10 mils or less within the same byte lane		
Routing Rules			
Layer Routing Requirements	Signals within a data byte lane must be routed on the same layer.		

Figure 78.   Example Length Matching for a Data Byte Lane
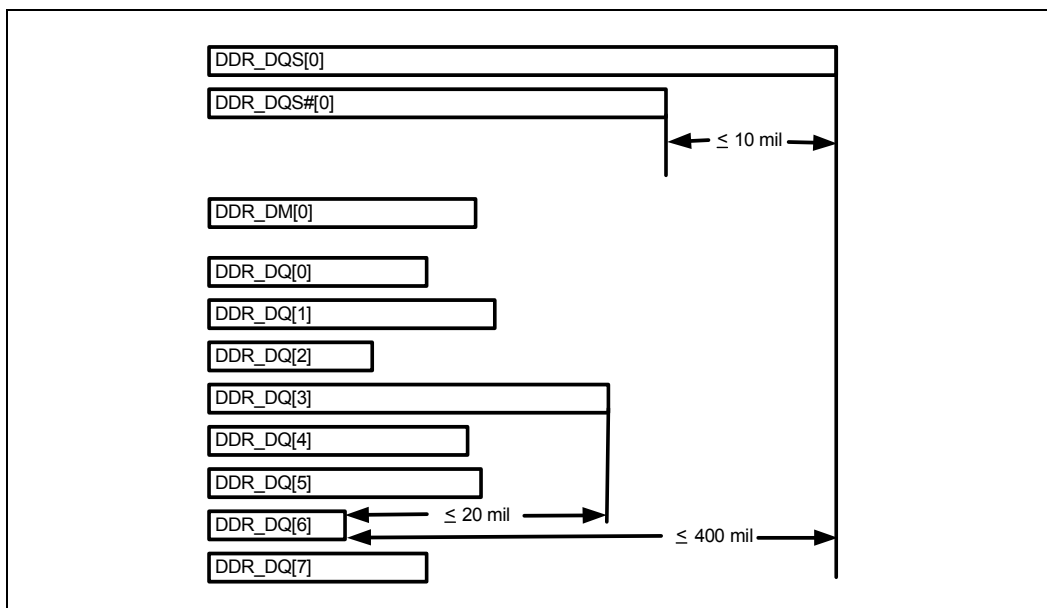
9.7.1.2   DDR2 Clock Group Signals - DDR_CLK[5:0]/DDR_CLK#[5:0]

The clock signal group includes six differential clock pairs per channel. The EP80579 generates and drives these differential clock signals. Since the EP80579 supports both registered and unbuffered DDR2 DIMMs, three separate differential clock pairs are routed to each DIMM connector. Table 40 summarizes the clock signal mapping, and Figure 79 shows the clock interconnect between the EP80579 and the DIMMs.

Table 40.   Differential Clock Signal Mapping

Signal	Relative To
CLK[2:0], CLK#[2:0]	DIMM0
CLK[5:3], CLK#[5:3]	DIMM1

Figure 79. EP80579-to-DIMM Interconnect DDR2 Clock Signals
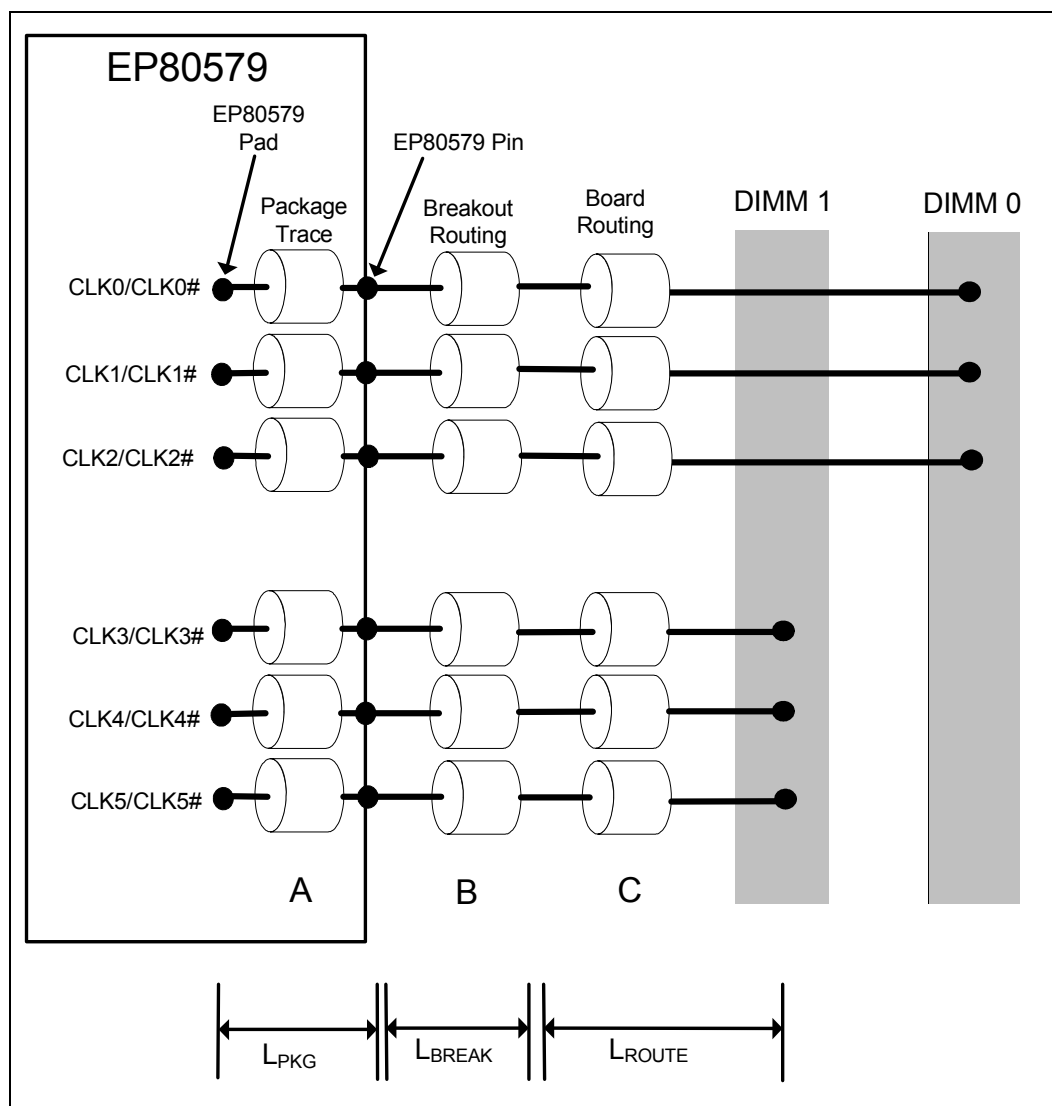
The differential clock pairs must be routed differentially from the EP80579 pin to their associated DIMM pins and must maintain the correct isolation spacing from other signals. Additionally, it is important to maintain the correct spacing and length matching between the pair to protect the differential integrity.

Figure 80 and Table 41 depict the recommended topology and layout routing guidelines for the DDR2 differential clocks. Route differential pair signals on the same layer.

The clocks are routed point-to-point. No external terminations are required for the clock signals because they are terminated on the DIMMs.

Figure 80.   DDR2 Point-to-Point Clock Routing Diagram
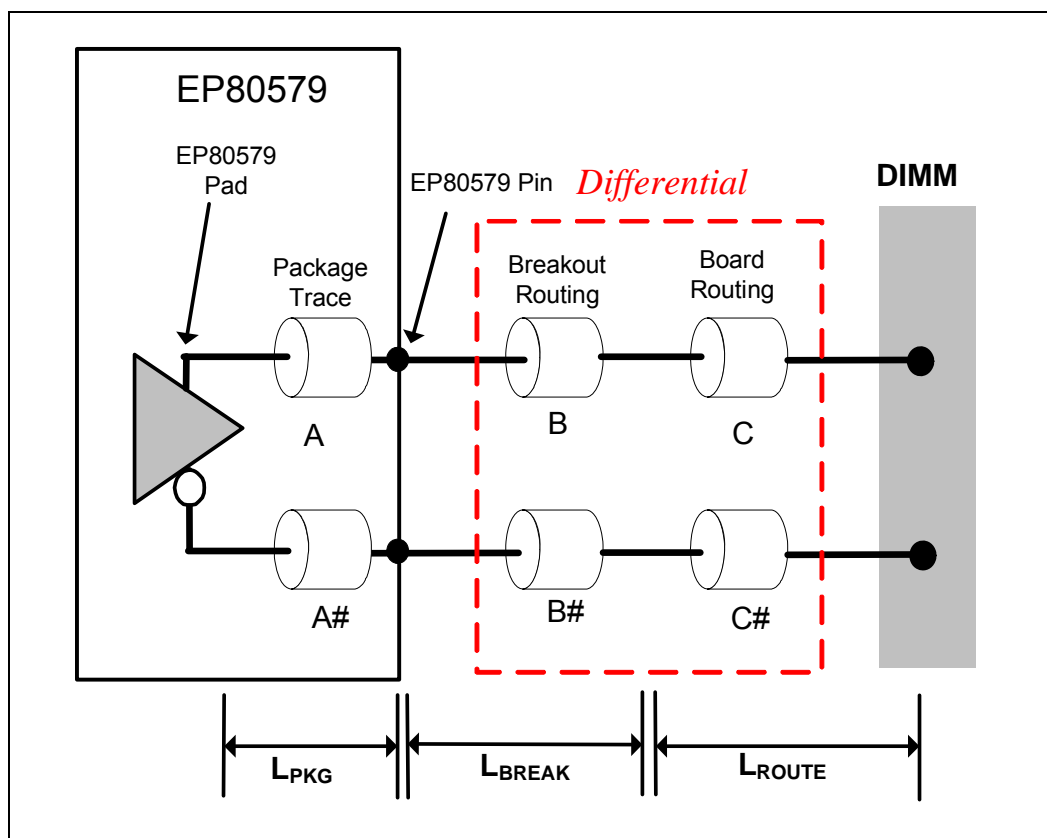
Table 41.   Clock Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines for 2-DIMM Solution	Figure
Signal Group	CLK/CLK#[2:0] - DIMM0; CLK/CLK#[5:3] -DIMM1	Figure 79
Topology	Point-to-Point	Figure 79, Figure 80
Reference Plane	Ground Referenced	
Layer Assignment	Layers 3/8 (Route Clock group on the same layer)	
Characteristic Trace Impedance (Zo)	Single Ended Impedance: 40Ω ±10%	Figure 80
Nominal Trace Width	6.5 mils for L3/L8	Figure 80,
Inter-pair Trace Spacing(e2e) (CLK to CLK# spacing)	6.0 mils	Figure 80
Pair-to-Pair Spacing (e2e)	15.0 mils	
Clearance from other signals groups	20.0 mils	Figure 80
Board Routing Guidelines		
Total Trace Length (TTL) = (L_{PKG} + L_{BREAK} + L_{ROUTE})	2.0 in - 6.0 in	
L_{PKG}	See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information	
L_{BREAK}	Max = 0.8 in	

Table 41. **Clock Signal Group Routing Guidelines (Sheet 2 of 2)**

Parameter	Routing Guidelines for 2-DIMM Solution	Figure
L_{ROUTE}	Max = 4.8 in	
Length/Skew Matching Rules		
	• The clock differential pairs need to match in length within ± 10 mils (CLK[x] = CLK[x]# ± 10 mils, x=0.. 5) • Clock pairs should be matched in length to other clock pairs within ± 20 mils, regardless of DIMM connection. • Clock signals should be matched in length to CMD/ADD within ± 20 mils. (CLK/CLK# = CMD/ADD ± 20 mils)	

9.7.1.3 DDR2 Control Signals – DDR_CS[1:0]#, DDR_ODT[1:0], DDR_CKE[1:0]

In the EP80579 memory configuration, the DDR_CKE, DDR_ODT, and DDR_CS# signals make up the control signal group. EP80579 provides six signals: DDR_CS[1:0]#, DDR_ODT[1:0], and DDR_CKE[1:0] as control signals. In the EP80579 two DIMM configuration, one chip select signal, one ODT control line, and one clock enable signal are required for each rank. Figure 81 provides the inter-connect implementation of the control signals to the DIMMs.

The EP80579 supports two single-rank and one dual-rank DIMMs. Always load the DIMM slot farthest from EP80579 first (DIMM 0). DIMM 0 can be populated with either a single-rank or a dual-rank DIMM. DIMM1 supports only a single-rank DIMM.

- For single-rank DIMMs:
  — DIMM0[rank0] uses DDR_CS0#, DDR_ODT0, and DDR_CKE0
  — DIMM1[rank0] uses DDR_CS1#, DDR_ODT1, and DDR_CKE1
- For dual-rank DIMMs (DIMM0 only):
  — DIMM0 [rank0] uses DDR_CS0#, DDR_ODT0, and DDR_CKE0
  — DIMM0 [rank1] uses DDR_CS1#, DDR_ODT1, and DDR_CKE1
  — DIMM1 should not be populated.

Table 42 and Figure 81 show the recommended topology and layout routing guidelines for the Control signals in a two-DIMM configuration. For designs that use only one DIMM, implement the topology for DIMM0 only, as shown in Figure 81, and eliminate the DIMM-to-DIMM routing guidelines.

Table 43 and Table 44 provide EP80579 controller and DIMM ODT settings for write and read operations to/from the DIMMs.

Figure 81. DDR2 Control Signals- Implementation
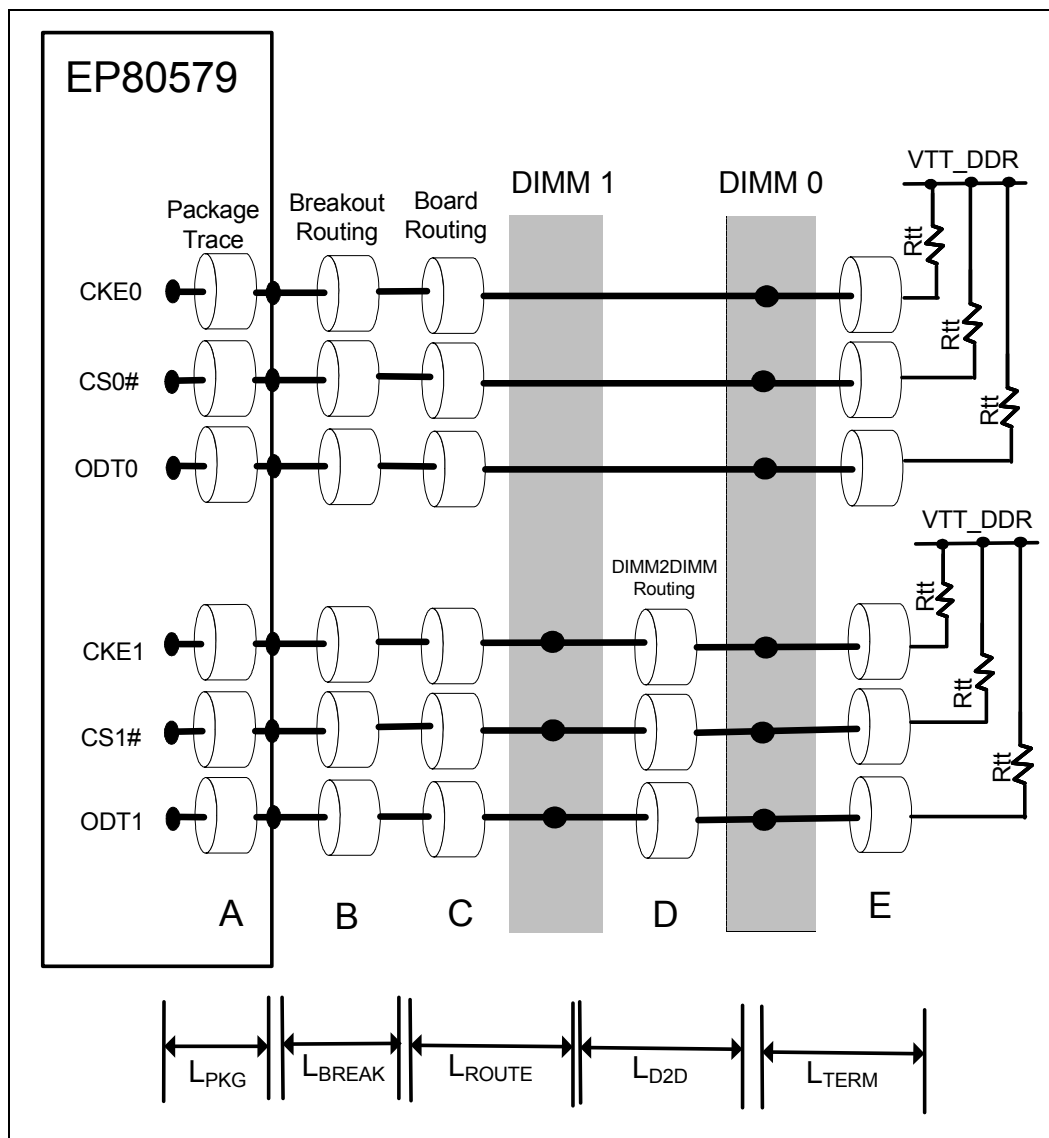
Table 42. DDR2 Control Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines for 2-DIMM Solution with ODT	Figure
Signal Group	Control Signals (CS#/ODT/CKE)	
Topology	Daisy Chain	Figure 76
Reference Plane	Ground Referenced	
Layer Assignment	Layers 3/8	
Characteristic Trace Impedance (Zo)	40 Ω ±10%	Figure 81
Nominal Trace Width	6.5 mils	Figure 81
Nominal Trace Spacing (e2e)	15 mils	Figure 81

Table 42. DDR2 Control Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guidelines for 2-DIMM Solution with ODT	Figure
Clearance from other signals	20 mils (min)	
Board Routing Guidelines		
Total Trace Length (TTL) = (L$_{PKG}$ + L$_{BREAK}$ + L$_{ROUTE}$ + L$_{D2D}$ + L$_{TERM}$)	(TTL of CMD/ADD) + 2.5 in ±5% (See Table 46)	
L$_{PKG}$	See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information.	
L$_{BREAK}$	Max = 0.8 in	
L$_{ROUTE}$	Calculate from Total Trace Length	
L$_{D2D}$	Max = 0.8 in • Trace length skews for the control signal for DIMM-to-DIMM routing should not exceed 10 mils	
L$_{TERM}$	Max = 500 mils • Trace length skews for the control signals to the termination resistors (L$_{TERM}$) should not exceed 200 mils.	
On-Board Termination		
Parallel Termination Resistor (Rtt)	60 Ω ±1%	Figure 81
Length/Skew Matching Rules		
Length Tuning Requirements	• The control signals need to match in length within ± 20 mils of each other.	

9.7.1.3.1   ODT Settings

Table 43 and Table 44 provides the DDR2 Controller and DIMM ODT settings for write and read operations to/from single-rank (SR) and dual-rank (DR) DIMM modules.

Table 43. Write Operation ODT Table

DIMM Module		Write Target	Controller Configuration	DIMM 0 Configuration		DIMM 1 Configuration	
DIMM 0	DIMM 1			Rank0	Rank1	Rank0	Rank1
SR	Empty	Rank0	ODT Off	75 Ω	n/a	n/a	n/a
DR	Empty	Rank0	ODT Off	ODT Off	75 Ω	n/a	n/a
DR	Empty	Rank1	ODT Off	75 Ω	ODT Off	n/a	n/a
SR	SR	Rank0	ODT Off	ODT Off	n/a	75 Ω	n/a
SR	SR	Rank1	ODT Off	75 Ω	n/a	ODT Off	n/a

Table 44.   Read Operation ODT Table

DIMM Module		Read Target	Controller Configuration	DIMM 0 Configuration		DIMM 1 Configuration	
DIMM 0	DIMM 1			Rank0	Rank1	Rank0	Rank1
SR	Empty	Rank0	120 Ω	ODT Off	n/a	n/a	n/a
DR	Empty	Rank0	120 Ω	ODT Off	75 Ω	n/a	n/a
DR	Empty	Rank1	120 Ω	75 Ω	ODT Off	n/a	n/a
SR	SR	Rank0	120 Ω	ODT Off	n/a	75 Ω	n/a
SR	SR	Rank1	120 Ω	75 Ω	n/a	ODT Off	n/a

9.7.1.4   Address and Command Signals – DDR_MA[14:0], DDR_BA[2:0], DDR_RAS#, DDR_CAS#, DDR_WE#

The address/command signals shown in Table 45 are source-clocked signals.

Table 45.   Address and Command Signals

Signal Description	Signal Name
System Memory Address Signals	DDR_MA[14:0]
Bank Addresses	DDR_BA[2:0]
Row Address Select	DDR_RAS#
Column Address Select	DDR_CAS#
Write Enable	DDR_WE#

The address/command signals are source-clocked signals that include 15 system memory address signals (MA[14:0]), 3 bank addresses (BA[2:0]), row address select (RAS#), column address select (CAS#), and write enable (WE#). The address/command signals are "clocked" into the DIMMs using the positive edge of the differential clock signals. The EP80579 drives the address/command and clock signals together.

Resistor packs are acceptable for the parallel (R_{TT}) address/command termination resistors, but address/command signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, or control signals.

Figure 82 and Table 46 show the recommended topology and layout routing guidelines for the DDR2-SDRAM address/command signals. Do not change layers. Place the parallel termination resistors close to the DIMM. Use VTT termination for low power requirement systems.

Figure 82.   Address/Command Daisy Chain With Parallel Termination Topology Diagram

Table 46.   DDR2 Address/Command Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines for 2-DIMM Solution with ODT	Figure
Signal Group	DDR_MA[14:0], DDR_BA[2:0], DDR_RAS#, DDR_CAS#, DDR_WE#	
Topology	Daisy Chain	Figure 76
Reference Plane	Ground Referenced	
Layer Assignment	Layers 3/8	
Characteristic Trace Impedance (Zo)	40 Ω ±10%	Figure 82
Nominal Trace Width	6.5 mils	Figure 82
Nominal Trace Spacing (e2e)	15 mils	Figure 82
Clearance from other signals	20 mils (min)	
Board Routing Guidelines		
Total Trace Length (TTL) = (L_{PKG} + L_{BREAK} + L_{ROUTE} + L_{D2D} + L_{TERM})	2.0 in - 6.0 in	
L_{PKG}	See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information.	
L_{BREAK}	Max = 0.8 in	
L_{ROUTE}	Max = 4.0 in	
L_{D2D}	Max = 0.8 in • Trace length skews for the control signal for DIMM-to-DIMM routing should not exceed 10 mils	
L_{TERM}	Max = 500 mils • Trace length skews for the ADD/CMD signals to the termination resistors (L_{TERM}) should not exceed 200 mils.	

Table 46. **DDR2 Address/Command Signal Group Routing Guidelines (Sheet 2 of 2)**

Parameter	Routing Guidelines for 2-DIMM Solution with ODT	Figure
On-Board Termination		
Parallel Termination Resistor (Rtt)	60 Ω ±1%	Figure 82
DIMM Compensation Capacitor		
DIMM0 Compensation Capacitor (Ccomp)	18pF • One capacitor per ADD/CMD signal to DIMM0 only. Place capacitor as close as possible to DIMM0.	Figure 82
Length/Skew Matching Rules		
Length Tuning Requirements	• ADD/CMD signals should match in length within 20 mils of each other.	
Routing Rules		
CLK-to-ADD/CMD Requirements	Clock signals should match ADD/CMD signals, in length, within 20 mils max.	

9.7.2 Reset Pin Requirement

Board designers must connect the DIMM pin 18 (RESET#) to the PWRGOOD signal from the voltage regulator that provides 1.8 V power to that DIMM. This signal must conform to standard SSTL_18 signaling levels. The DIMM RESET# input must not go low for any reason once the power up sequence is complete. The EP80579 drives all clock enables low by default as it comes out of power up. The timing of the PWRGOOD signal must be such that EP80579 is safely driving DDR_CKE low when PWRGOOD transitions from low to high.

9.7.3 DC Bias Signals

The DC bias signals consist of DDR_SLWCRES, DDR_RCOMPX, DDR_CRES[2:0], DDV_CRES, and DDR_VREF. The routing guidelines for these signals are described in the following sections.

9.7.3.1 DDR_SLWCRES, DDR_RCOMPX, DRV_CRES, & DDR_CRES0

The DDR_SLWCRES, DDR_RCOMPX, DRV_CRES, and DDR_CRES0 signals are compensation resistors for slew rate, impedance, and common return, respectively. Intel recommends 20 mil wide traces with a minimum spacing of 12 mils from other signals. When breaking out from the EP80579, maintain a minimum spacing of 4.5 mils up to a maximum length of 500 mils. For the best signal integrity, minimize this length as much as possible. Figure 83 shows the routing topology for these signals.

Figure 83. **DDR_SLWCRES, DDR_RCOMPX, DDV_CRES, & DDR_CRES0 Routing Topology**

DDR_CRES0

DRV_CRES   249 Ω, 1%

DDR_SLWCRES   825 Ω, 1%

DDR_RCOMPX   825 Ω, 1%
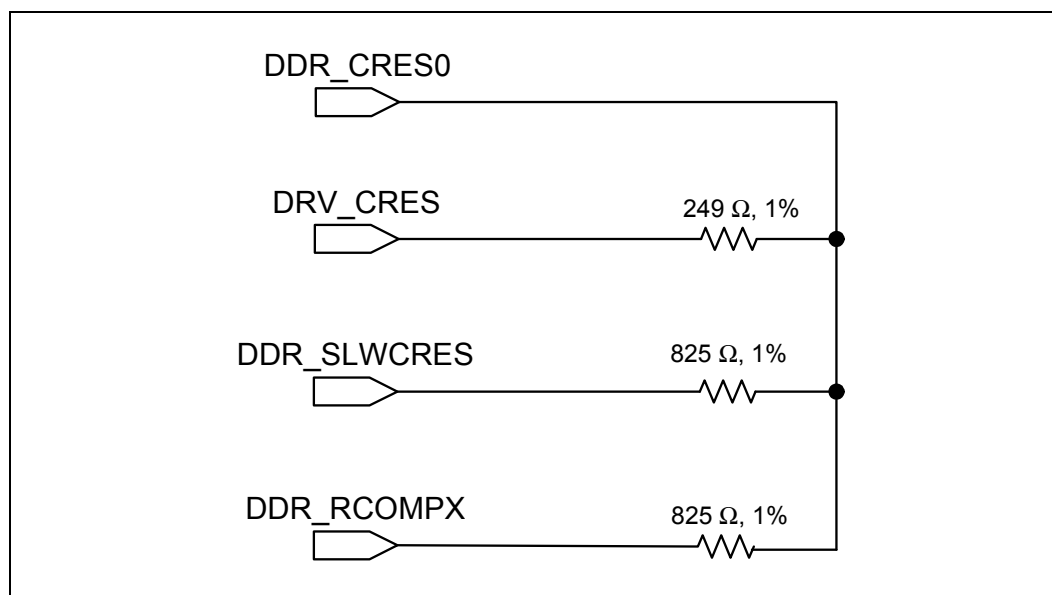
9.7.3.2 DDR_CRES1, DDR_CRES2

The EP80579 provides the DDR_CRES1 and DDR_CRES2 signals as additional compensation resistors (See Figure 84). Intel recommends 20 mil wide traces with a minimum spacing of 12 mils from other signals. When breaking out from the EP80579, maintain a minimum spacing of 4.5 mils spacing up to a maximum length of 500 mils. For the best signal integrity, minimize this length as much as possible.

Figure 84. **DDR_CRES1 and DDR_CRES2 Signal Connections**

VCC18

DDR_CRES2   100 Ω   1 %

0.1uF

DDR_CRES1   100 Ω   1 %
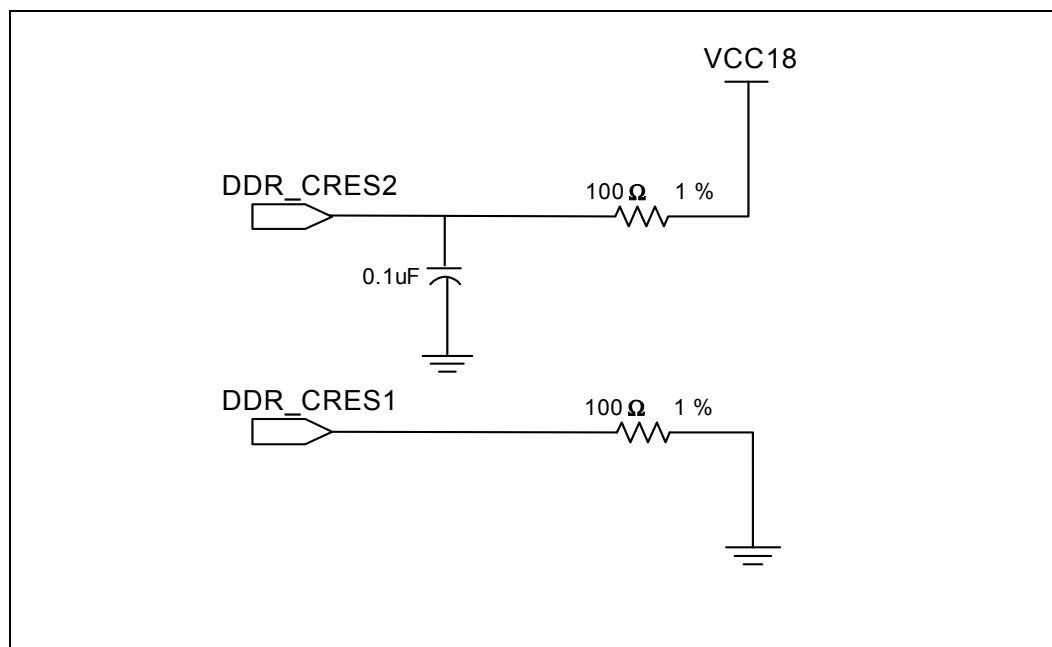
9.7.3.3 DDR2 Reference Voltage, DDR_VREF

The DDR2 system memory reference voltage (DDR_VREF) is used by the DDR2-SDRAM devices to compare the input signal levels of the data, command, and control signals. The DDR2-SDRAM DDR_VREF must be generated as shown in Figure 85. Generate DDR_VREF from a typical resistor divider using 0.1% tolerance resistors, with a 0.01 μF cap tied to DDR_VREF. The DDR_VREF divider resistors must be placed as close to possible to the DIMMs. The DDR_VREF must be decoupled locally at each DIMM connector. Finally, the DDR_VREF signal must be routed with as wide a trace as possible. Table 47 provides the routing and component guidelines for the Vref circuit. Intel recommends at least a 20 mil wide trace with a minimum spacing of 12 mils from other signals. For the best signal integrity, minimize this length as much as possible.

Figure 85. DDR_VREF Generation Example Circuit
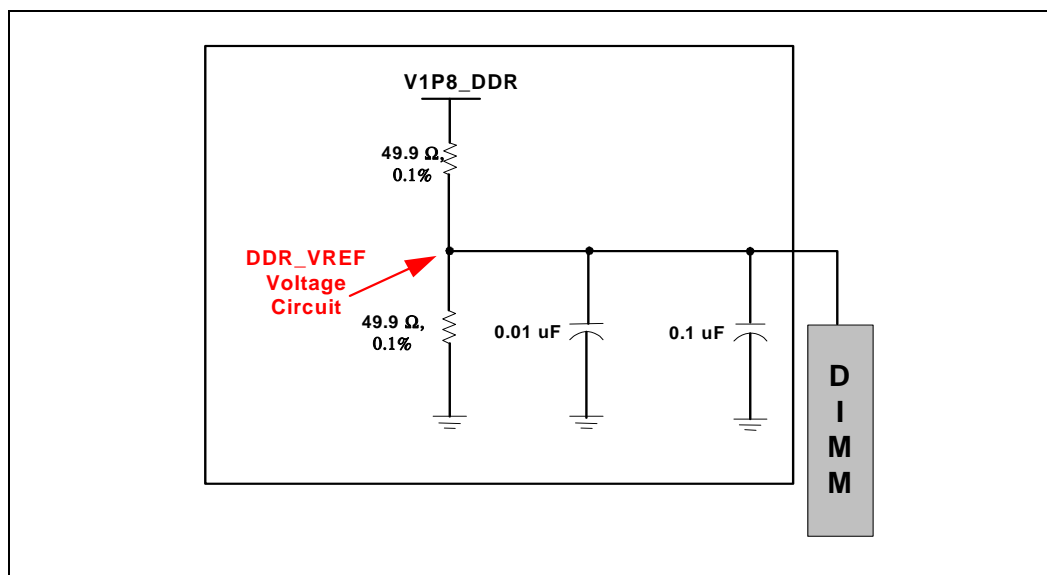
Table 47. DDR V$_{REF}$ Generation Requirements

Parameter	Guideline
Nominal Trace Width	20 mils
Voltage Divider	Place resistor divider consisting of two resistors as close as possible to DIMMs.
Decoupling requirements	0.01 μF and 0.1μF capacitors
Decoupling placement	Place one decoupling cap at each of the DIMM sockets and one decoupling cap at the EP80579 (Figure 85)

9.8 Decoupling Recommendations

When designing a board, the following decoupling recommendations should be followed:

- Capacitors should be mounted as close to the EP80579 as possible. They should be no further than 10 mm from the edge of the EP80579 package for the DDR2 channel.

- Decoupling caps should be placed near any signal reference layer change. This can be done by adding a 0.1μF capacitor between DDR Power and Ground where the Memory Clock traces change reference layers.

Note: These decoupling recommendations are for the EP80579 pins. Place multiple capacitors in parallel to get the desired value for capacitance and ESL.

10.0 PCI Express* Interface

The EP80579 provides one configurable x8 PCI Express interface (Port A or PEA0) with a maximum theoretical bandwidth of 4 GByte/s. Port A may alternatively be configured as a 2x4 or a 2x1 (PEA0 and PEA1). This interface is referred to throughout this document as the PCI Express Port A (PEA). The EP80579 may be configured as x8; in that case the reference is PEA. The EP80579 may also be configured in x4 mode; in which case there are two available x4 ports referred to as PEA0 and PEA1.

PCI Express is a dual-simplex point-to-point serial differential low voltage interconnect. A PCI Express topology can contain a host bridge and several endpoints. The raw bit rate on the data pins is 2.5 Gbit/sec/lane/direction at introduction. Maximum theoretical bandwidth realized on the x8 PCI Express interface of 2 GByte/s in each direction simultaneously, for an aggregate of 4 GByte/s. Each port consists of a group of transmitters and receivers located on the same chip. Each lane consists of a transmitter and a receiver pair. A link between device ports is a collection of lanes (x1, x4, and x8 width). All lanes within a port must transmit data using one frequency.

The point-to-point, serial PCI Express interconnect offers layout advantages over traditional multi-drop parallel interconnects. The lower signal count of PCI Express reduces the number of traces required to route the interconnect.

Each PCI Express packet is 8b/10b encoded with an embedded clock. The embedded clock simplifies routing rules by removing the length matching requirements between signal pairs, which virtually eliminates the serpentine and routing space required to do so. Differential signaling produces lower EMI and crosstalk. The high bit rate for PCI Express requires some design considerations for board designers. See Section 10.1, "PCI Express Layout Design Guidelines" for more details. Intel encourages platform designers to perform simulation and validation testing that is necessary to ensure a successful design.

The PCI Express lane topology consists of a transmitter (Tx) differential pair located on one device connected to a receiver (Rx) differential pair on a second device. One of the devices may be located on the baseboard or an add-in card in which one or more connectors may be present.

Each lane is AC coupled between its corresponding transmitter and receiver. The AC coupling capacitor is located on the board close to the transmitter side. Each end of the link is terminated on-die into nominal 100Ω differential DC impedance. Board termination is not required. The differential signals from the transmitter must be connected to the differential signals at the receiver. Figure 86 shows the PCI Express interconnect.

Figure 86. PCI Express* Interconnect
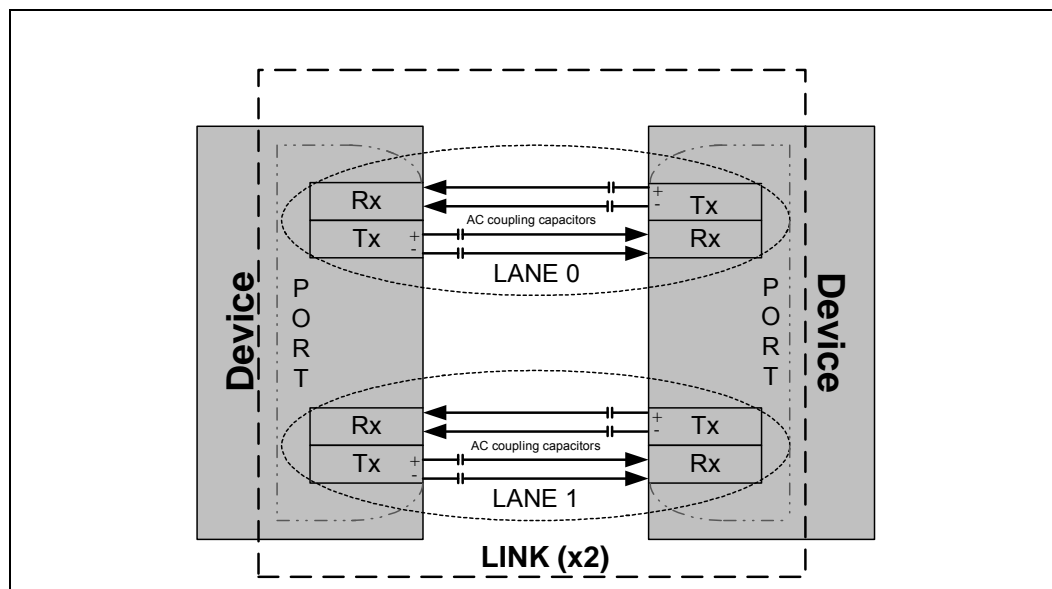
For more information on PCI Express, see the *PCI Express Base Specification*, Rev. 1.1 and *PCI Express Card Electromechanical Specification*, Rev. 1.0 or later.

The EP80579 provides support for x8 port or x4 port. The x8 port can be divided into two x4 ports or two x1 ports.

For the list of PCI Express signals, see the *Intel® EP80579 Integrated Processor Product Line Datasheet*.

10.1 PCI Express Layout Design Guidelines

This section contains information and details for layout and routing guidelines.

One of the key points for PCI Express board design is to follow a set of rules to minimize losses, jitter, crosstalk, and mode conversion for differential traces.

Loss is the differential voltage signal swing attenuation of the trace from transmitter to receiver. The trace is subject to resistive, dielectric, and skin effect losses. Loss increases as trace length or frequency increases. In addition, conductor loss increases as trace width decreases. Vias and connectors that are a part of the interconnect also introduce losses. Total loss allowed on the interconnect is 13.2 dB at 1.25 GHz.

Jitter, including jitter from crosstalk, consists of random and deterministic contributions to signal edge timing that reduce the signal valid time. The total jitter on the interconnect allowable is 120 ps.

Crosstalk is the coupling of energy from one signal trace to the other which results in the signal voltage and phase change. There are two kinds of crosstalk, Far-End (FEXT) and Near-End (NEXT). Whether the transmitter and receiver pairs are interleaved, the Far-End can appear at the transmitter or receiver. Crosstalk within the differential pair is not a concern. Crosstalk between differential pairs can be minimized by keeping a large pair-to-pair spacing compared to spacing within a pair. Stripline traces show far less Far-End crosstalk (FEXT) than microstrip.

Mode conversions are due to imperfections and other trace mismatches on the interconnect which transform differential mode voltage to common mode voltage and vice versa. For example, length mismatch within pairs or an asymmetric via layout could cause mode conversion.

Differential signaling is that in which information is encoded in the difference between the voltage on two nets. The differential receiver is designed to be very sensitive to this difference, while being insensitive to portions of the signal that are similar (the common-mode signal). It is important to equalize the total length of the traces in the pair throughout the trace; each segment of trace length must be equal along the entire length of the pair. The differential trace impedance target of 90 Ω ±10%, unless otherwise specified. Tight coupling within the differential pair and increased spacing to other differential pairs helps to minimize EMI and crosstalk. It is preferable to route Tx and Rx differential pairs alternately on the same layer (i.e., a Tx pair next to an Rx pair rather than another Tx pair) to help minimize FEXT at the receiver on microstrip layers.

For coupled differential pairs, every attempt should be made to match the number of left and right bends as closely as possible to minimize skew due to length differences between each signal of the differential pair.

Alternate left and right turns to minimize skew due to length differences between each signal of the differential pair. Matching the number of right and left turns and alternating such bends helps to minimize the amount of skew between rising or falling edges of a propagating differential signal pair at any point along the length of the pair. For example, a series of left turns adds length to the outside trace that increases the delay of that trace. Although this length could potentially be made up at the end of the trace route, thereby ensuring that the signal pair is in sync at both the beginning and the end of the trace route, the signal pair is actually out of sync in the area around the series of left turns.

Trace segment length matching within pairs is required to ensure trace lengths are equal on a segment-by-segment basis. Overall length must match to +/- 5 mils. Examples of segments could include breakout areas, routes between two vias, routes between an AC coupling capacitor and a connector pin, etc. The points of discontinuity would be the via, the capacitor pad, or the connector pin. In addition, length mismatches must be corrected closely following the mismatch site to minimize common mode conversion effects.

When routing traces, bends must be kept to a minimum. If bends cannot be avoided, they must be at a 45° angle or smaller, do not use 90-degree bends or turns.

10.1.1 Board Stack-Up Consideration

Generally the stack-up depends on the following:

- Signal referencing
- Power-ground plane decoupling requirements
- Routing channel requirements

Due to frequency-dependent loss effects at PCI Express edge rates, the guidelines in this section apply only to the reference stackup. Even if trace widths are adjusted to meet the specified impedance targets, the attenuation of high frequency components of the signal on those traces is a function of the trace width and thickness as well as dielectric characteristics. A design that deviates from the specified stackup will require simulation and validation of the proposed PCI Express implementation. Simulation is highly recommended for all PCI Express implementations.

Follow the specified stackup in Figure TBD to avoid frequency-dependent loss effects that may occur at PCI Express edge rates. If the dielectric characteristics are different from those specified in the stackup (TBD), the solution space presented in this section may not apply. This inaccuracy may happen even if the trace widths are adjusted to meet the specified impedance targets because the attenuation of high frequency components is a function of the trace width, thickness, and dielectric characteristics. Simulate and validate any design that deviates from the specified stackup.

10.1.2 Impedance Requirements

The tables in this section show the required geometry for the stripline and microstrip PCI Express differential signals.

Stripline traces are routed on inner layers. Signals travel slower on stripline traces than on microstrip traces. They have a very low FEXT and very low dispersion. Table 48 indicates the differential impedance and trace width used in routing stripline signals.

Microstrip traces are routed on the outer layers. Signals travel a bit faster on the microstrip traces compared to stripline traces. They have significant FEXT and notable frequency and mode dependence on velocity. Table 48 indicates the differential impedance and trace width used in routing microstrip signals.

Table 48.   Trace Width/Impedance Requirement for Stripline and Microstrip Layers

Trace Width	Nominal Trace Spacing	Nominal Trace Impedance (Zo)
Stripline Layers (3 or 8)		
4.5 mils	5.5 mils edge-to-edge	90 Ω ±10% (Differential)
Microstrip Layers (1 or 10)		
4.75 mils	5.25 mils edge-to-edge	90 Ω ±10% (Differential)

Figure 87.   Recommended PCI Express Stripline Trace Width/Spacing
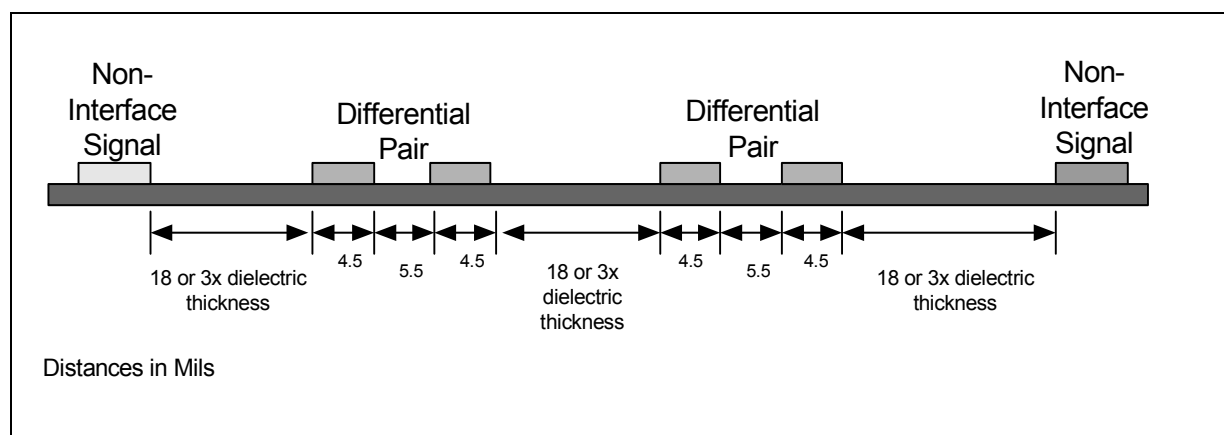
Figure 88.   Recommended PCI Express Microstrip Trace Width/Spacing
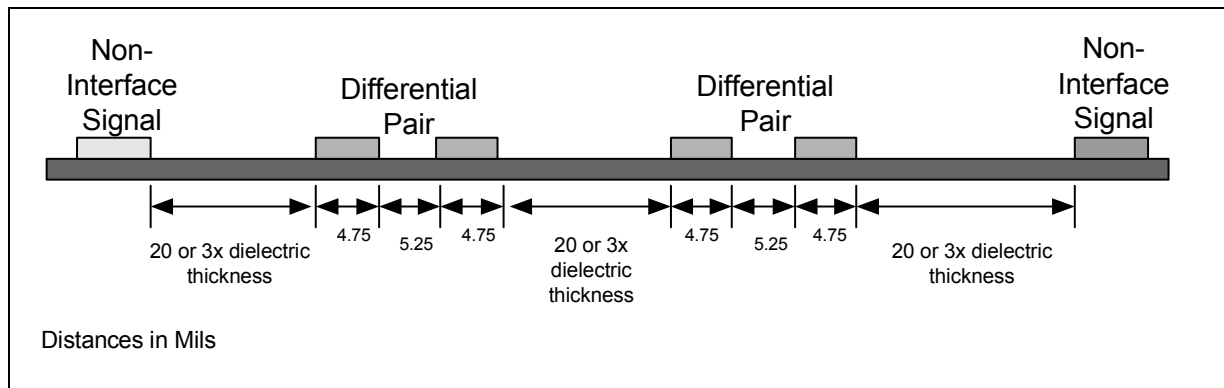
10.1.3   AC Coupling Requirements

Each PCI Express lane is AC coupled between the transmitter and receiver. The AC coupling capacitor is located on the board for baseboard devices.

AC coupling capacitors of 75–200 nF (0.1 µF recommended) must be placed at the same location on the traces within the pair. Size 0603 or smaller capacitors are recommended. C-packs are not allowed for AC coupling capacitors. Also, the same package size of the capacitor must be used for each signal in a differential pair. Pad sizes for each capacitor must be minimized.

10.1.4   Via Requirements

All via geometries are preferred 10 mils finished hole, 21 mils pad or 31 mils antipad. Alternate via geometries will require simulation of the proposed PCI Express implementation, including electrical models of the via geometry being used.

Via requirements for design consideration appear below:

*   Layout recommended that no more than six vias per Tx pair and four vias per Rx pair should be used on each net in a differential pair on the motherboard when routing to a PCI Express connector. For PCI Express graphics down solutions, it is recommended that no more than four(4) vias per Tx pair and four(4) vias per Rx trace be used. The only time to use the six (6) vias in a topology is when the LAI is present. Otherwise the max number of vias is four (4).

*   Each via is expected to contribute 0.25 to 0.5 dB to the loss budget. The number of vias on the differential pair must be the same and in the same relative location on the differential pair to maintain trace symmetry. Avoid placing pads on the inner layers.

*   The number of vias for each signal line within a differential pair - whether or not that pair is tightly coupled - must be matched because each signal within the diff pair must stay on the same layers (3 & 8).

(intel®)

10.1.5   Compensation Resistor Signals Guidelines

Figure 89.   PCI Express Compensation Signal Guidelines
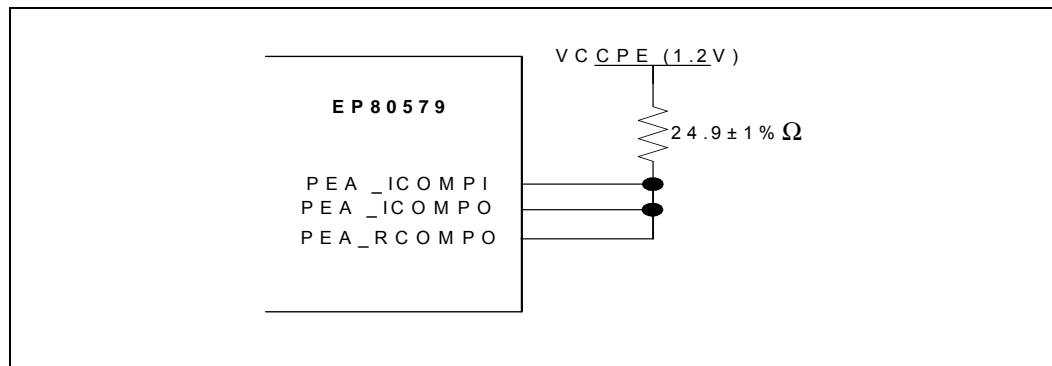
The PCI Express interface has three compensation resistors on the PCI Express port. The following signals are used to calibrate the PCI Express high-speed serial input/ output buffers:

- PEA_RCOMPO
- PEA_ICOMPI
- PEA_ICOMPO

The PEA_RCOMPO, PEA_ICOMPI and PEA_ICOMPO signals must be tied directly to each other at the EP80579 and terminate to VCCPE (1.2V) through a 24.9Ω ±1% resistor, as shown in Figure 89.

10.1.6   PCI Express Clocks Routing Guidelines

PEA_CLKp, and PEA_CLKn are the differential clock pairs for the PCI Express port. These clocks are inputs to the EP80579 and used to derive the internal clock. These clocks are not used for PCI Express devices. Detailed routing information for these signals can be found in Section 8.2.2, "CLK100 (SRC Clock) Group" .

10.1.7   Topology 1 — EP80579 to PCI Express Connector

Table 49 and Figure 90 summarize the layout routing solution space to a PCI Express connector. In this case, the EP80579 is a transmitter and the PCI Express connector is a receiver. L1, L2, and L3 must be routed on the same layer.

- L1 starts from the EP80579 breakout region to the AC blocking capacitor via.
- L2 is the main routing section that is from the AC blocking capacitor via to the PCI Express connector breakout region.
- L3 is the breakout region of the PCI Express connector.
- LT is the main routing section that is from the EP80579 pin to the PCI Express connector.

Table 49.   PCI Express Connector Routing (EP80579 Transmit)

Parameter	Routing Guidelines	Figure
Signal Group	PEA0_Tn[7:0], PEA0_Tp[7:0]	-
Reference Plane	Ground Referenced	-
Layer Assignment	Layers 3 or 8 (stripline) Layers 1 or 10 (microstrip)	-
Characteristic Trace Impedance (Zo)	90 Ω ±10% (Differential)	-
Nominal Trace Width	4.5 mils (stripline) 4.75 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing within a pair from edge to edge	5.5 mils (stripline) 5.25 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing from edge of one differential pair to edge of another differential pair	The greater of: • 18 mils or 3x dielectric thickness (stripline) • 20 mils or 3x dielectric thickness (microstrip)	Figure 87 Figure 88
Trace Length L1, L1'– EP80579 Breakout region and to AC CAP	Min = 0.5 in. Max = 2.5 in.	Figure 90
Trace Length L2, L2' + L3, L3'– AC CAP to PCI Express connector	Min = 4.5 in. Max = 15.5 in. (stripline) Max = 15.0 in. (microstrip)	Figure 90
Trace Length LT– EP80579 pin to PCI Express connector	LT = L1 + L2 + L3	Figure 90
AC Capacitor–AC CAP	0.1 µF	Figure 90
Length Tuning Requirements	Routing must remain on the same layer. Maximum number of vias is 4. LT-LT' = ±5 mils	Figure 90

Figure 90.   PCI Express Connector Routing (EP80579 Transmit)
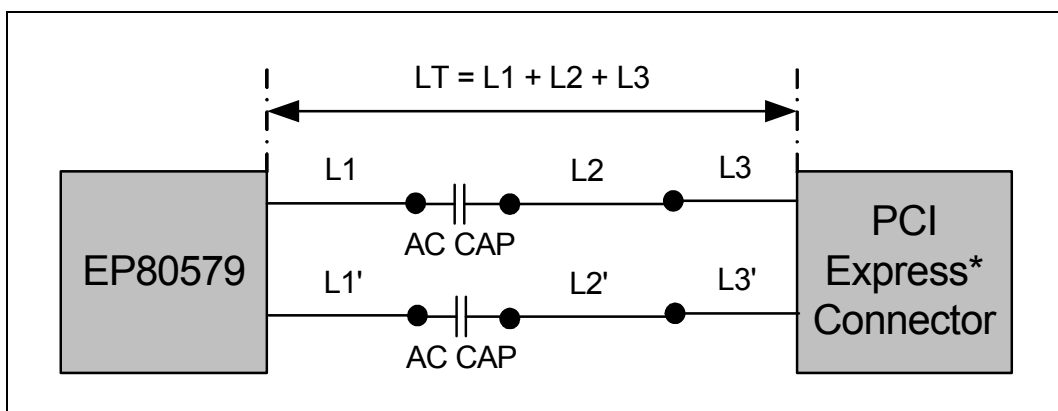
Table 50 and Figure 91 summarize the layout routing solution space to a PCI Express connector. In this case, EP80579 is a receiver and the PCI Express connector is a transmitter. LT must be routed on the same layer.

- L1 is the EP80579 breakout region.
- L2 starts from the edge of the EP80579 breakout region to the PCI Express connector.
- LT is the main routing section that is from the EP80579 pin to the connector.

Table 50.   PCI Express Connector Routing (EP80579 Receive)
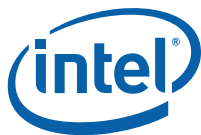
Parameter	Routing Guidelines	Figure
Signal Group	PEA0_Rn[7:0], PEA0_Rp[7:0]	
Reference Plane	Ground Referenced	
Layer Assignment	Layers 3 or 8 (stripline) Layers 1 or 10 (microstrip)	
Characteristic Trace Impedance (Zo)	90 Ω ±10% (Differential)	
Nominal Trace Width	4.5 mils (stripline) 4.75 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing within a pair from edge to edge	5.5 mils (stripline) 5.25 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing from edge of one differential pair to edge of another differential pair	The greater of: • 18 mils or 3x dielectric thickness (stripline) • 20 mils or 5x dielectric thickness (microstrip)	Figure 87 Figure 88
Trace Length L1, L1'– EP80579 Breakout region	Min = 0.5 in. Max = 2.5 in.	Figure 91
Trace Length L2, L2' – PCI Express connector	Min = 4.5 in. Max = 15.5 in. (stripline) Max = 15.0 in. (microstrip)	Figure 91
Trace Length LT– EP80579 pin to PCI Express connector	LT = L1 + L2	Figure 91
Length Tuning Requirements	Routing must remain on the same layer. Maximum number of vias is 4. LT-LT' = ±5 mils	Figure 91

Figure 91.   PCI Express Connector Routing (EP80579 Receive)
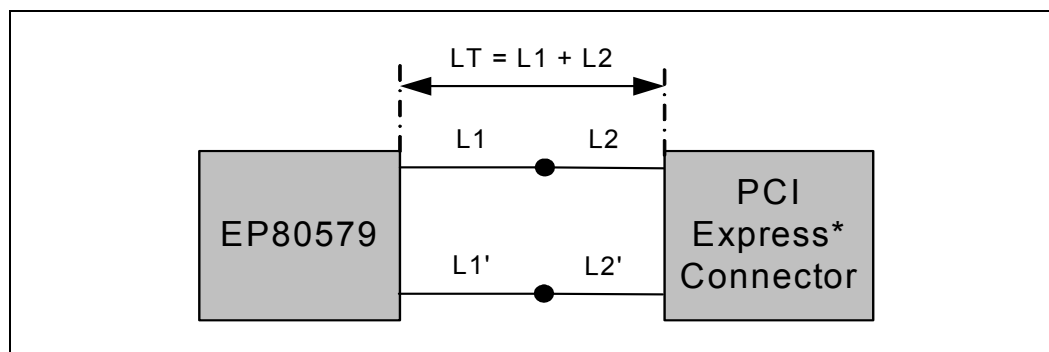
10.1.8   Topology 2 – EP80579 to PCI Express Connector with Logic Analyzer Connector

Table 51 and Figure 92 summarize the layout routing solution space to a PCI Express connector on the board with a logic analyzer connector. In this case, EP80579 is a transmitter and the PCI Express connector is a receiver. All traces must be routed on the same layer.

• L1 starts from the EP80579 breakout region to the AC blocking capacitor via.

• L2 is the main routing section that is from the AC blocking capacitor via to the logic analyzer connector.

- L3 and L4 are the logic analyzer connector breakout regions on each side of the connector.
- L5 is from the logic analyzer connector breakout region to the PCI Express connector.
- LT is the main routing section that is from the EP80579 pin to the PCI Express connector.

Table 51.   PCI Express Connector with LAI Connector Routing (EP80579 Transmit)

Parameter	Routing Guidelines	Figure
Signal Group	PEA0_Tn[7:0], PEA0_Tp[7:0]	-
Reference Plane	Ground Referenced	-
Layer Assignment	Layers 3 or 8 (stripline) Layers 1 or 10 (microstrip)	-
Characteristic Trace Impedance (Zo)	90 Ω ±10% (Differential)	-
Nominal Trace Width	4.5 mils (stripline) 4.75 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing within a pair from edge to edge	5.5 mils (stripline) 5.25 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing from edge of one differential pair to edge of another differential pair	The greater of: • 18 mils or 3x dielectric thickness (stripline) • 20 mils or 3x dielectric thickness (microstrip)	Figure 87 Figure 88
Trace Length L1, L1'– EP80579 Breakout region and to AC CAP via	Min = 0.75 in. Max = 2.5 in.	Figure 92
Trace Length L2, L2' – AC CAP via to logic analyzer breakout region.	Min = 0.5 in. (stripline) Min = 0.5 in. (microstrip) Max = 5.5 in. (stripline) Max = 6.0 in. (microstrip)	Figure 92
Trace Length L3, L3' – Logic analyzer breakout region.	Min = 3.5 in. (microstrip) Max = 0.5 in. (stripline) Max = 7.0 in. (microstrip)	Figure 92
Trace Length L4, L4' – Logic analyzer breakout region.	Max = 0.5 in. (stripline)	Figure 92
Trace Length L5, L5' – Logic analyzer breakout region to PCI Express connector.	Min = 2.5 in. (stripline) Max = 7.0 in. (stripline)	Figure 92
Trace Length LT– EP80579 pin to PCI Express connector	LT = L1 + L2 +L3 + L4 + L5 (stripline) LT = L1 + L2 +L3 (microstrip)	Figure 92
AC Blocking Capacitor–AC CAP	0.1 µF	Figure 92
Length Tuning Requirements	Routing must remain on the same layer. Maximum number of vias is 6 (stripline) and 4 (microstrip). LT-LT' = ±5 mils	Figure 92

Figure 92.   PCI Express Connector with LAI Connector Routing (EP80579 Transmit)
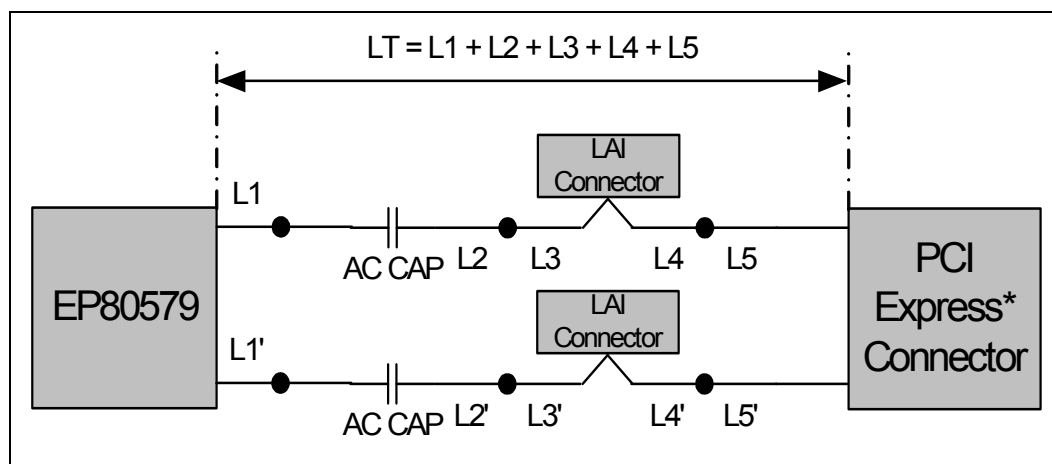
Table 52 and Figure 93 summarize the layout routing solution space to a PCI Express connector. In this case, EP80579 is a receiver and the PCI Express connector is a transmitter. LT must be routed on the same layer.

- L1 is the EP80579 breakout region.
- L2 starts from the EP80579 breakout region to the edge logic analyzer connector.
- L3 and L4 are the logic analyzer connector breakout regions on each side of the connector.
- L5 is from the logic analyzer connector breakout region to the PCI Express connector breakout region.
- LT is the main routing section that is from the EP80579 pin to the PCI Express connector.

Table 52.   PCI Express Connector with LAI Connector Routing (EP80579 Receive) (Sheet 1 of 2)

Parameter	Routing Guidelines	Figure
Signal Group	PEA0_Rn[7:0], PEA0_Rp[7:0]	-
Reference Plane	Ground Referenced	-
Layer Assignment	Layers 3 or 8 (stripline) Layers 1 or 10 (microstrip)	-
Characteristic Trace Impedance (Zo)	90 Ω ±10% (Differential)	-
Nominal Trace Width	4.5 mils (stripline) 4.75 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing within a pair from edge to edge	5.5 mils (stripline) 5.25 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing from edge of one differential pair to edge of another differential pair	The greater of: • 18 mils or 3x dielectric thickness (stripline) • 20 mils or 3x dielectric thickness (microstrip)	Figure 87 Figure 88
Trace Length L1, L1'— EP80579 Breakout region	Min = 0.5 in. Max = 2.5 in.	Figure 93

Table 52. **PCI Express Connector with LAI Connector Routing (EP80579 Receive) (Sheet 2 of 2)**

Parameter	Routing Guidelines	Figure
Trace Length L2, L2′ – to edge of logic analyzer breakout region.	Min = 0.5 in. (stripline) Min = 0.5 in. (microstrip) Max = 5.5 in. (stripline) Max = 6.0 in. (microstrip)	Figure 93
Trace Length L3, L3′ – Logic analyzer breakout region.	Min = 3.5 in. (microstrip) Max = 0.5 in. (stripline) Max = 7.0 in. (microstrip)	Figure 93
Trace Length L4, L4′ – Logic analyzer breakout region.	Max = 0.5 in. (stripline)	Figure 93
Trace Length L5, L5′ – Logic analyzer breakout region to PCI Express connector.	Min = 2.5 in. (stripline) Max = 7.0 in. (stripline)	Figure 93
Trace Length LT– EP80579 pin to PCI Express connector	LT = L1 + L2 +L3 + L4 + L5 (stripline) LT = L1 + L2 +L3 (microstrip)	Figure 93
AC Blocking Capacitor–AC CAP	0.1 μF	Figure 93
Length Tuning Requirements	Routing must remain on the same layer. Maximum number of vias is 6 (stripline) and 4 (microstrip). LT-LT′ = ±5 mils	Figure 93

Figure 93. **PCI Express Connector With LAI Connector Routing (EP80579 Receive)**
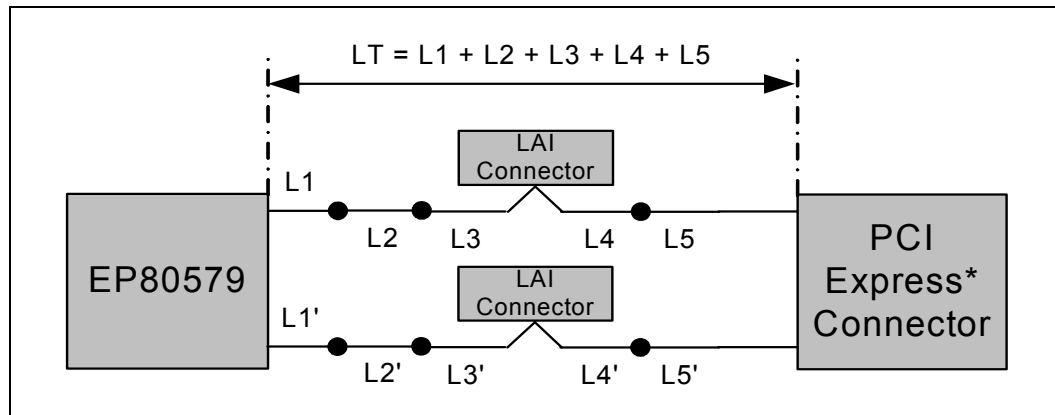
10.1.9 Topology 3 – EP80579 to PCI Express Down Device

Table 53 and Figure 94 summarize the layout routing solution space to a PCI Express device on the board. In this case, EP80579 is a transmitter and the PCI Express device is a receiver. All traces must be routed on the same layer.

- L1 starts from the EP80579 breakout region to the AC blocking capacitor via.
- L2 is the main routing section that is from the AC blocking capacitor via to the PCI Express device breakout region.
- L3 is the breakout region of the PCI Express device.
- LT is the main routing section that is from the EP80579 pin to the PCI Express device.

Table 53.   PCI Express Down Device Routing (EP80579 Transmit)

Parameter	Routing Guidelines	Figure
Signal Group	PEA0_Tn[7:0], PEA0_Tp[7:0]	-
Reference Plane	Ground Referenced	-
Layer Assignment	Layers 3 or 8 (stripline) Layers 1 or 10 (microstrip)	-
Characteristic Trace Impedance (Zo)	90 Ω ±10% (Differential)	-
Nominal Trace Width	4.5 mils (stripline) 4.75 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing within a pair from edge to edge	5.5 mils (stripline) 5.25 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing from edge of one differential pair to edge of another differential pair	The greater of: • 18 mils or 3x dielectric thickness (stripline) • 20 mils or 3x dielectric thickness (microstrip)	Figure 87 Figure 88
Trace Length L1, L1'– EP80579 Breakout region and to AC CAP	Min = 0.75 in. Max = 2.5 in.	Figure 94
Trace Length L2, L2' – AC CAP to PCI Express Device breakout region	Min = 4.0 in (stripline) Min = 2.5 in (microstrip) Max = 14.5 in. (stripline) Max = 13.0 in. (microstrip)	Figure 94
Trace Length L3, L3'– Express Device breakout region	Min = 0.75 in. Max = 2.0 in.	Figure 94
Trace Length LT– EP80579 pin to PCI Express Device	LT = L1 + L2 + L3	Figure 94
AC Blocking Capacitor–AC CAP	0.1 µF	Figure 94
Length Tuning Requirements	Routing must remain on the same layer. Maximum number of vias is 4. LT-LT' = ±5 mils	Figure 94

Figure 94.   PCI Express Down Device Routing (EP80579 Transmit)
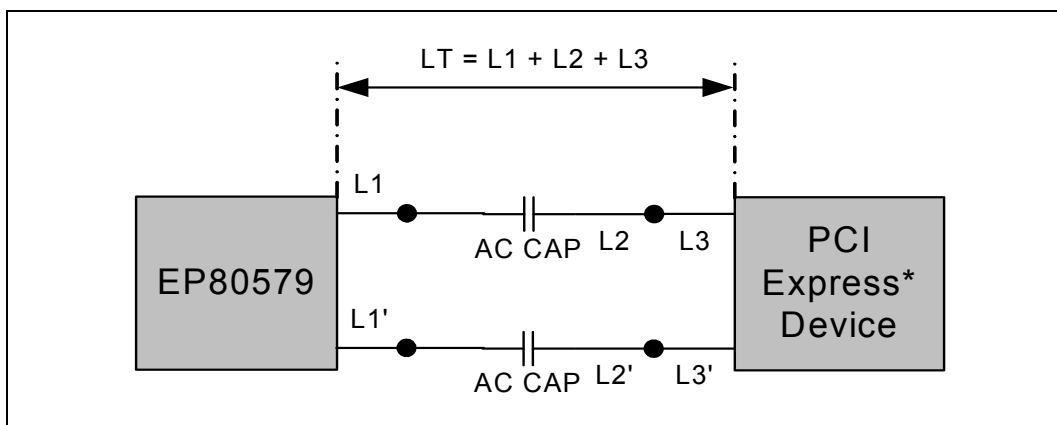
Table 54 and Figure 95 summarize the layout routing solution space to a PCI Express on board device. In this case, EP80579 is a receiver and the PCI Express device is a transmitter. LT must be routed on the same layer and the signals must reference one continuous plane.

• L1 is the EP80579 breakout region.

- L2 starts from the EP80579 breakout region to the PCI Express device breakout region.
- L3 is the breakout region of the PCI Express device.
- LT is the main routing section that is from the EP80579 pin to the PCI Express device.

Table 54.   PCI Express Down Device Routing (EP80579 Receive)

Parameter	Routing Guidelines	Figure
Signal Group	PEA0_Tn[7:0], PEA0_Tp[7:0]	-
Reference Plane	Ground Referenced	-
Layer Assignment	Layers 3 or 8 (stripline) Layers 1 or 10 (microstrip)	-
Characteristic Trace Impedance (Zo)	90 Ω ±10% (Differential)	-
Nominal Trace Width	4.5 mils (stripline) 4.75 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing within a pair from edge to edge	5.5 mils (stripline) 5.25 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing from edge of one differential pair to edge of another differential pair	The greater of: • 18 mils or 3x dielectric thickness (stripline) • 20 mils or 3x dielectric thickness (microstrip)	Figure 87 Figure 88
Trace Length L1, L1'– EP80579 Breakout region	Min = 0.75 in. Max = 2.5 in.	Figure 95
Trace Length L2, L2' – edge of EP80579 Breakout region to edge PCI Express Device breakout region.	Min = 4.0 in (stripline) Min = 2.5 in (microstrip) Max = 14.5 in. (stripline) Max = 13.0 in. (microstrip)	Figure 95
Trace Length L3, L3' – PCI Express breakout region.	Min = 0.75 in. Max = 2.0 in.	Figure 95
Trace Length LT– EP80579 pin to PCI Express connector	LT = L1 + L2 +L3	Figure 95
Length Tuning Requirements	Routing must remain on the same layer. Maximum number of vias is 4. LT-LT' = ±5 mils	Figure 95

Figure 95.   PCI Express Down Device Routing (EP80579 Receive)
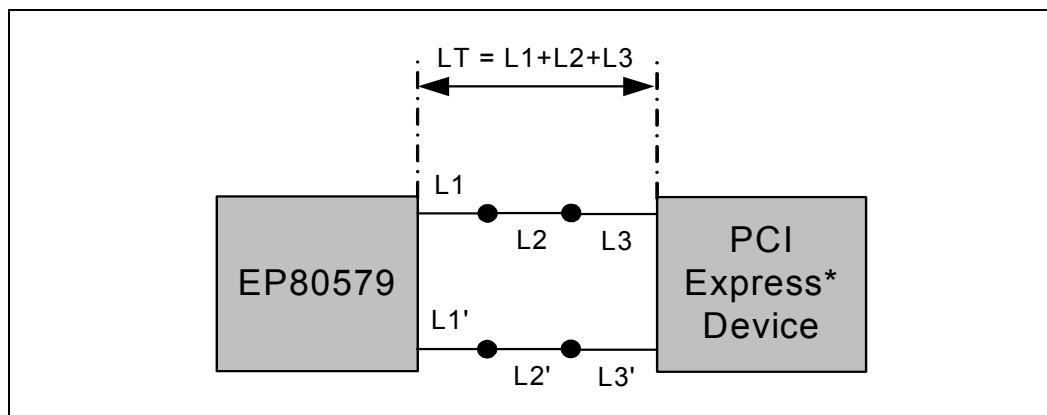
10.1.10 Topology 4 – EP80579 to PCI Express Down Device with Logic Analyzer Connector

Table 55 and Figure 96 summarize the layout routing solution space to a PCI Express device on the board with a logic analyzer connector between the EP80579 and PCI Express device. In this case, the EP80579 is a transmitter and the PCI Express device is a receiver. All traces must be routed on the same layer.

- L1 starts from the EP80579 breakout region to the AC blocking capacitor via.
- L2 is the main routing section that is from the AC blocking capacitor via to the logic analyzer connector.
- L3 and L4 are the logic analyzer connector breakout regions on each side of the connector.
- L5 is from the logic analyzer connector breakout region to the PCI Express device break-in region.
- L6 is the break-in region of the PCI Express device.
- LT is the main routing section that is from the EP80579 pin to the PCI Express device.

Table 55. PCI Express Down Device with LAI Connector Routing (EP80579 Transmit)

Parameter	Routing Guidelines	Figure
Signal Group	PEA0_Tn[7:0], PEA0_Tp[7:0]	-
Reference Plane	Ground Referenced	-
Layer Assignment	Layers 3 or 8 (stripline) Layers 1 or 10 (microstrip)	-
Characteristic Trace Impedance (Zo)	90 Ω ±10% (Differential)	-
Nominal Trace Width	4.5 mils (stripline) 4.75 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing within a pair from edge to edge	5.5 mils (stripline) 5.25 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing from edge of one differential pair to edge of another differential pair	The greater of: • 18 mils or 3x dielectric thickness (stripline) • 20 mils or 3x dielectric thickness (microstrip)	Figure 87 Figure 88
Trace Length L1, L1'– EP80579 Breakout region and to AC CAP	Min = 0.5 in. Max = 2.5 in.	Figure 96
Trace Length L2, L2' – AC CAP to logic analyzer breakout region.	Min = 0.5 in. Max = 5.5 in.	Figure 96
Trace Length L3, L3', L4, L4' – Logic analyzer breakout region.	0.5 in. (stripline)	Figure 96
Trace Length L5, L5' – Logic analyzer breakout region to PCI Express device breakout region.	Min = 2.5 in., Max = 6.5 in.	Figure 96
Trace Length L6, L6' – PCI Express breakout region.	Min = 0.75 in. Max = 2.0 in.	Figure 96
Trace Length LT– EP80579 pin to PCI Express Device	LT = L1+L2+L3+L4+L5+L6 (stripline) LT = L1+L2+L5+L6 (microstrip)	Figure 96
AC Blocking Capacitor–AC CAP	0.1 µF	Figure 96
Length Tuning Requirements	Routing must remain on the same layer. Maximum number of vias is 6 (stripline) and 4 (microstrip). LT-LT' = ±5 mils	Figure 96

Figure 96. PCI Express Down Device with LAI Connector Routing (EP80579 Transmit)
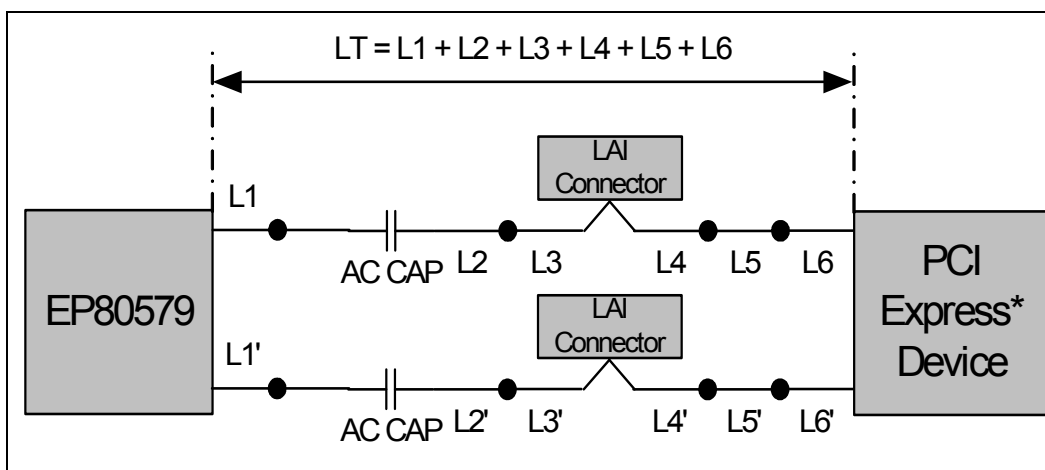
Table 56 and Figure 97 summarize the layout routing solution space to a PCI Express Device. In this case, EP80579 is a receiver and the PCI Express connector is a transmitter. LT must be routed on the same layer.

- L1 starts from the EP80579 breakout region to the AC blocking capacitor via.

- L2 is the main routing section that is from the AC blocking capacitor via to the logic analyzer connector.

- L3 and L4 are the logic analyzer connector breakout regions on each side of the connector.

- L5 is from the logic analyzer connector breakout region to the PCI Express device break-in region.

- L6 is the break-in region of the PCI Express device.

- LT is the main routing section that is from the EP80579 pin to the PCI Express device.

Table 56. PCI Express Down Device with LAI Connector Routing (EP80579 Receive)

Parameter	Routing Guidelines	Figure
Signal Group	PEA0_Rn[7:0], PEA0_Rp[7:0]	-
Reference Plane	Ground Referenced	-
Layer Assignment	Layers 3 or 8 (stripline) Layers 1 or 10 (microstrip)	-
Characteristic Trace Impedance (Zo)	90 Ω ±10% (Differential)	-
Nominal Trace Width	4.5 mils (stripline) 4.75 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing within a pair from edge to edge	5.5 mils (stripline) 5.25 mils (microstrip)	Figure 87 Figure 88
Nominal Trace Spacing from edge of one differential pair to edge of another differential pair	The greater of: • 18 mils or 3x dielectric thickness (stripline) • 20 mils or 3x dielectric thickness (microstrip)	Figure 87 Figure 88
Trace Length L1, L1'— EP80579 Breakout region and to AC CAP	Min = 0.75 in. Max = 2.5 in.	Figure 97

Table 56. **PCI Express Down Device with LAI Connector Routing (EP80579 Receive)**

Parameter	Routing Guidelines	Figure
Trace Length L2, L2′ – AC CAP to logic analyzer breakout region.	Min = 0.5 in. Max = 5.5 in.	Figure 97
Trace Length L3, L3′, L4, L4′ – Logic analyzer breakout region.	0.5 in. (stripline)	Figure 97
Trace Length L5, L5′ – Logic analyzer breakout region to PCI Express device breakout region.	Min = 2.5 in. Max = 6.5 in.	Figure 97
Trace Length L6, L6′ – PCI Express breakout region.	Min = 0.75 in. Max = 2.0 in.	Figure 97
Trace Length LT– EP80579 pin to PCI Express Device	LT = L1+L2+L3+L4+L5+L6 (stripline) LT = L1+L2+L5+L6 (microstrip)	Figure 97
Length Tuning Requirements	Routing must remain on the same layer. Maximum number of vias is 6 (stripline) and 4 (microstrip). LT-LT′ = ±5 mils	Figure 97

Figure 97. **PCI Express Down Device With LAI Connector Routing (EP80579 Receive)**
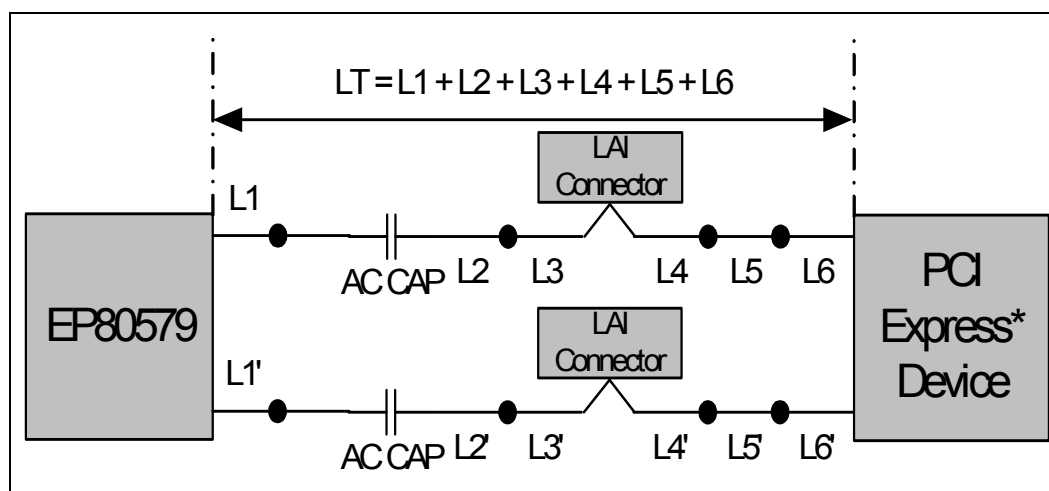
10.2 Additional Considerations for PCI Express

10.2.1 PCI Express I/O Devices

Baseboard down PCI Express I/O devices typically require special layout techniques on other data interfaces as well. Keep the considerations in this section in mind and reference the appropriate design guides while performing the PCI Express layout.

10.2.2 EMI

As data is transmitted at higher frequencies, the spectrum of high-speed signals has significant energy as the speed reaches several GHz. Minimizing and containing EMI is challenging for wide band signals. There are two general principles for EMI reduction in a system:

- Suppression of noise generation

- Containment of generated noise

Suppression is generally accomplished at the board level through component placement, trace routing, etc. Containment is achieved at the system level through inter-board connection, enclosure, etc. Non-linear distortion of the PCI Express signals may increase the EMI and should be minimized. The spread spectrum clocking may be used with the limitation in the modulation range (0 to -5000 ppm) and rate (30 - 33 KHz).

Many electromagnetic compatibility problems can be avoided by following EMI design guidelines.

10.2.3 PCI Express (JTAG) Boundary Scan Pins

If boundary scan is not implemented on the system board, TMS and TDI must be independently bused and pulled up, each with ~5 kΩ resistors. TRST# and TCK must be independently bused and pulled down, each with ~5 kΩ resistors. TDO must be left open.

10.2.4 Terminating Unused PCI Express Ports

If the PCI Express port is not implemented on the system, leave the signals shown in Table 57 as no connects.

Table 57.   No Connect Signals for Unused PCI Express Ports

PCI Express Port
PEA0_Tn[x]
PEA0_Tp[x]
PEA0_Rn[x]
PEA0_Rp[x]

Note: 'x' is the port number left unconnected.

If PCI Express ports will not be implemented on the platform, leave all PCI Express transmit and receive signals disconnected. This includes the following signals:

- PEA0_Tn[7:0]
- PEA0_Tp[7:0]
- PEA0_Rn[7:0]
- PEA0_Rp[7:0]

10.2.5 Probing Differential Pairs

Be aware of limitations when probing the PCI Express Tx pairs on EP80579. There may be a mismatch in impedance caused by the grid pitch and general routing in the breakout region if the Tx probing is done close to the breakout region. In this case, localized reflections may be misread as poor signal integrity. These reflections do not propagate to the receive end of the transmission line, where most measurements should be taken. Only Unit Interval width measurements should be taken on the transmit side of the transmission line.

11.0 Serial ATA (SATA) Interface

11.1 SATA Interface

The EP80579 contains two SATA ports capable of independent DMA operation. The SATA interface supports data transfer rates up to 1.5 Gb/s or 3.0 Gb/s per port.

11.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design (see Figure 98):

- Serial ATA signals must be ground referenced, preferred routing on layers 3 and 8. If changing reference plane is completely unavoidable (i.e. ground reference to power reference), proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by reference plan change. Stitching capacitors are small-valued capacitors (1uF or lower in value) that bridge the power and ground planes close to where a high-speed signal changes layers. Stitching caps provide a high frequency current return path between different reference planes. They minimize the impedance discontinuity and current loop area that crossing different reference planes created. Max number allowable for SATA to change reference plane is one.

- Route all traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane can cause signal reflections and must be avoided.

- Minimize layer changes. Use a maximum of 2 vias per SATA trace for microstrip or a maximum of 2 vias for stripline. Via count includes thru-hole connector as an effective via. Use a maximum of six vias for stripline in order to connect to the AC decoupling capacitors. If a layer change is necessary, ensure that trace matching for either the transmit or receive pair occurs within the same layer. Recommend to use SATA vias as small as possible.

- Do not route SATA traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks.

- Avoid stubs (e.g., usually introduced by test points) whenever possible. Utilize vias and connector pads as test points instead.

- It can be helpful for testability to route the Tx and Rx pairs for a given port on the same layer and close to each other to help ensure the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of Rx pair layout quality can be approximated by using the results from actively testing the Tx pair's signal quality.

- Do not serpentine to match Rx and Tx traces; there is NO requirement to match Rx and Tx traces. In addition, DO NOT serpentine to meet minimum length guidelines on Rx and Tx.

Note: The minimum length must be met. That minimizes our Max peak to peak differential voltage (for Gen 2). Properly placing a SATA connector (not too close to the EP80579)

so that serpentining is not necessary would be the approach to meeting the minimum requirement and not serpentining.

- Keep SATA traces 20 mils from any vias on the motherboard whenever possible.

- In certain systems, such as a closed-box small form factor system, where a short, very low loss cable is to be exclusively used, it may be desirable to use longer trace lengths to optimize SATA signal quality at the device receiver. See the Rx connector specification for more information. Careful simulation and/or studies on prototypes of signal quality are required to balance this trade off effectively.

Figure 98.   SATA Layout and Routing Example
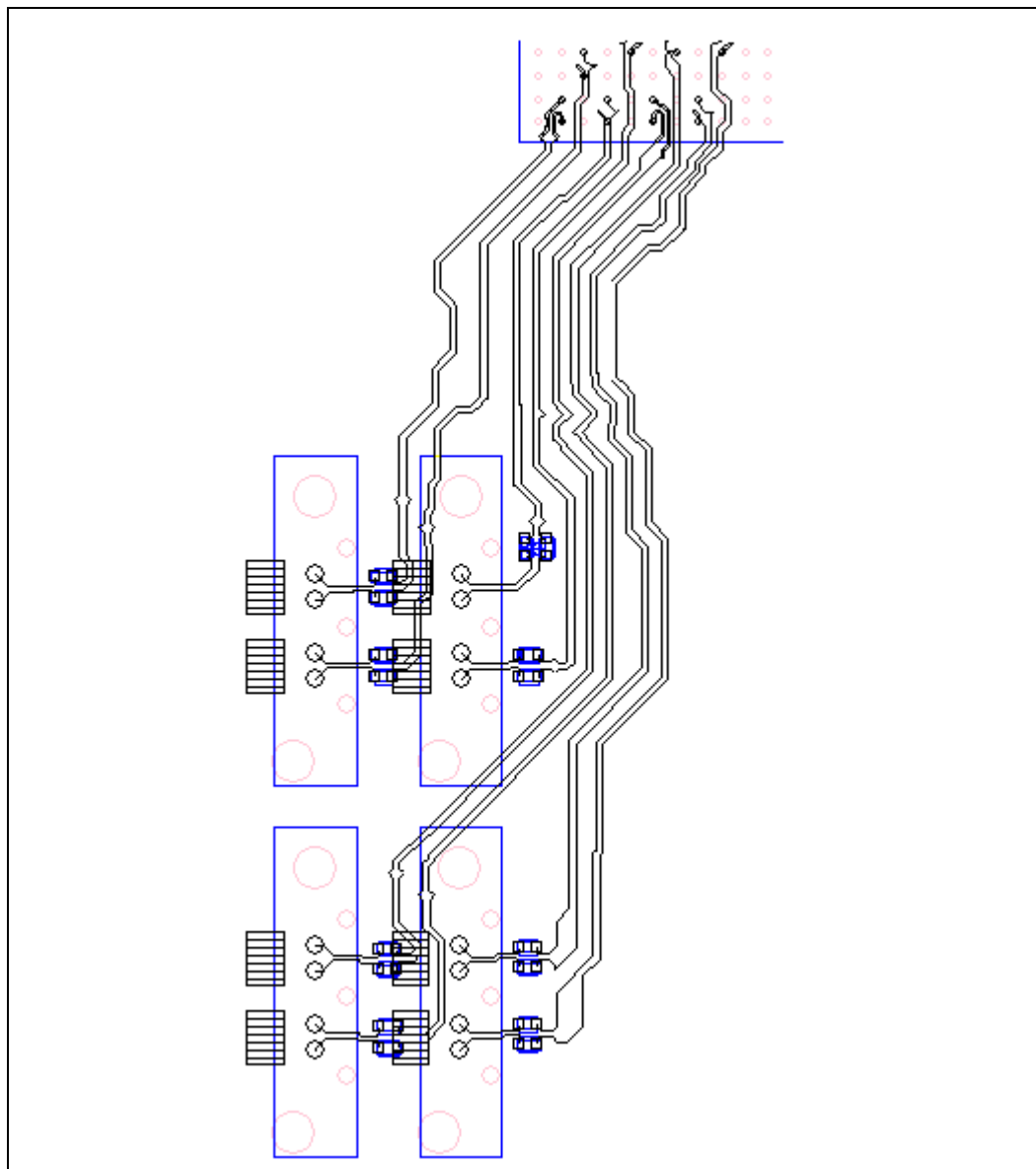
Notes:
1.   Some manufacturing processes have difficulties with the fine-pitched SATA thru-hole connector. In some cases, solder bridging can occur between the connector pins. Solder wicking pads, as shown in Figure 98, can be used to minimize this effect by wicking solder away from the pins.
2.   The AC Caps are required on the SATA interface.

11.2 SATA Transmit and Receive Signals – SATA_TXp[1:0], SATA_TXn[1:0], SATA_RXp[1:0], SATA_RXn[1:0]

The SATA interface has two differential transmit and receive pairs for a total of 8 signals. Route each pair differentially as microstrip or stripline. Table 58 summarizes the SATA_TX and SATA_RX routing guidelines.

Table 58. Transmit and Receive Routing Guidelines

Parameter	Routing Guidelines	Figure
Signal Group	SATA_TXp[1:0], SATA_TXn[1:0], SATA_RXp[1:0], SATA_RXn[1:0]	
Reference Plane	Ground Referenced, Stripline or Microstrip	
Layer Assignment	Layer 1 or 10 (microstrip) Layers 3 or 8 (stripline)	
Characteristic Trace Impedance (Zo)	90 Ω ±10% (differential)	
Nominal Trace Width	4.75 mils (microstrip) 4.5 mils (stripline)	Figure 101

Nominal Trace Spacing	Trace Spacing, edge-to-edge:
	    5.25 mils–microstrip
	    5.5 mils–stripline
	Pair to Pair Spacing, edge-to-edge:
	    25 mils –microstrip
	    20 mils –stripline
		Figure 101

Nominal Trace Length	L1 max = 0.400 in.
	L2 =
	    Stripline –> min = 1.150 in., max = 4.750 in.
	    Microstrip –> min = 1.500 in., max = 5.750 in.
	L3 max = (L-ac1 + L_ac_2) = 0.350 in.
		Figure 99 and Figure 100

Length Tuning Requirements	LTpos = LTneg within 5 mils (LT = L1+L2+L3)	Figure 99 and Figure 100
EP80579 Breakout	4 mils width with 4 mils spacing for maximum of 400 mils, minimize this length.	Figure 99 and Figure 100
Vias	2 Vias max, recommended to remove unused internal pads to improve the signal quality.	Figure 99 and Figure 100
AC CAP	10 nf	Figure 99 and Figure 100
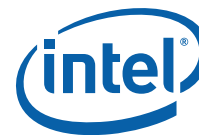
Figure 99. SATA Tx and Rx Signal Routing Topology
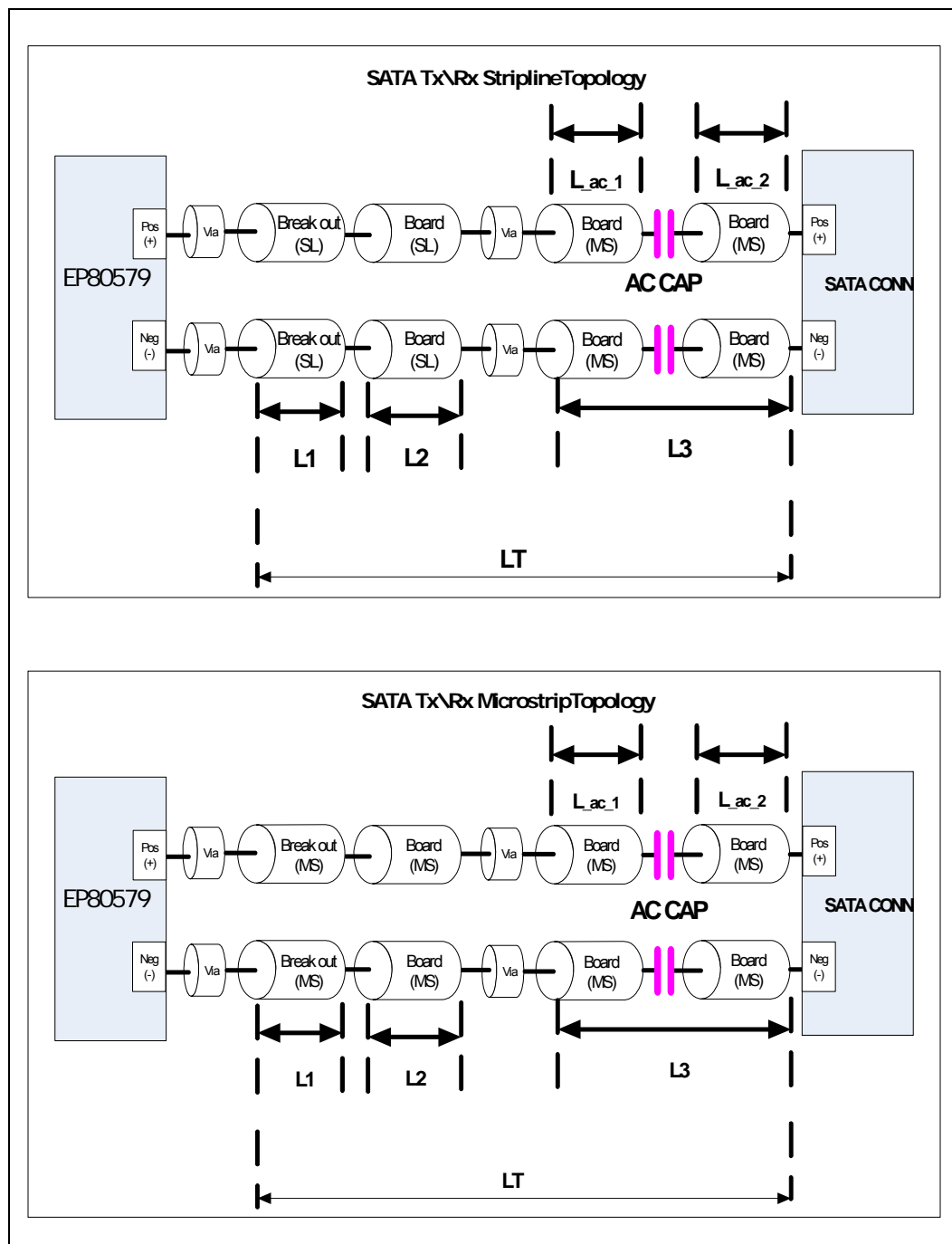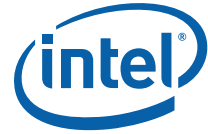
Figure 100. SATA PCB Routing
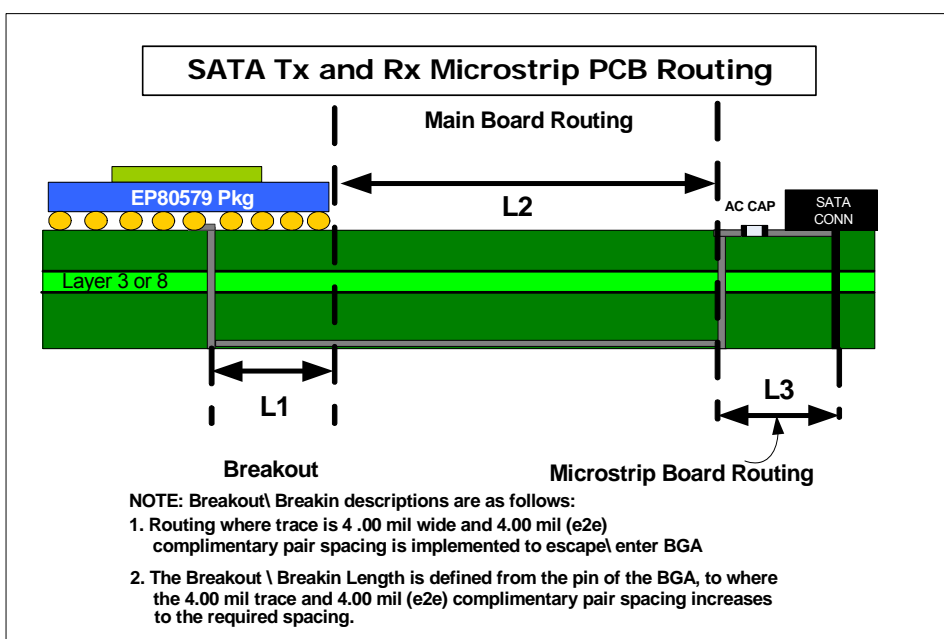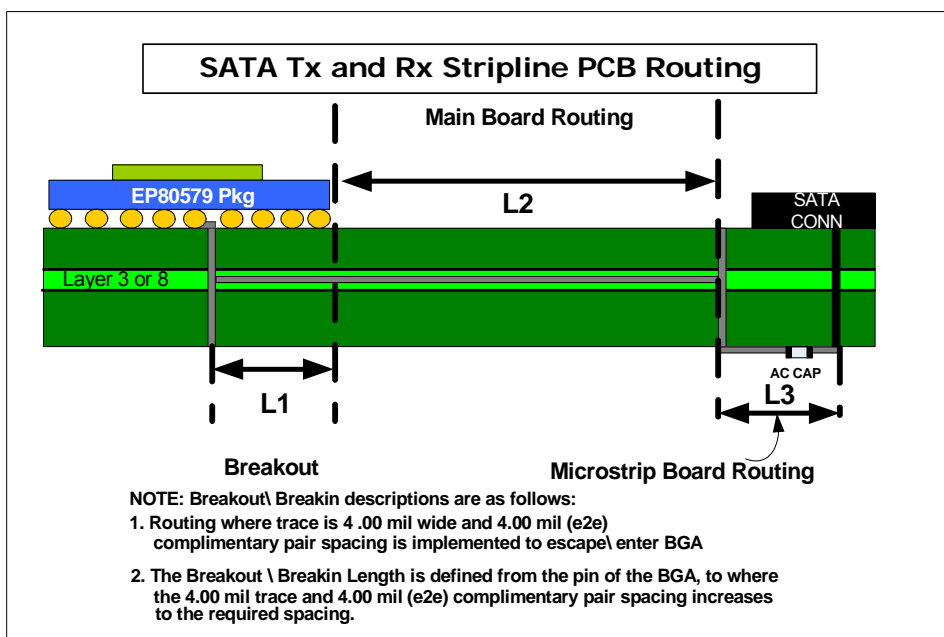
11.2.1 SATA Trace Separation

Figure 101 provides an illustration of the recommended trace spacing. Use the following separation guidelines for the SATA interface:

- Maintain parallelism between SATA differential signals with the trace spacing needed to achieve 90 Ω ±10% differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Ensure the amount and length of the deviations are kept as small as possible.

- Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used, keeping in mind that the target is a 90 Ω ±10% differential impedance. For the recommended board stackup parameters, 4.5 mil traces with 5.5 mil spacing in stripline, or 4.75 mil traces with 5.25 mil spacing in microstrip, the results are in approximately 90 Ω ±10% differential trace impedance.

- Based on simulation data, use 20 mil (stripline) minimum, or 25 mil (microstrip) minimum spacing between the SATA signal pairs and other signal traces for optimal signal quality. This helps prevent crosstalk.

Figure 101. SATA Trace Spacing
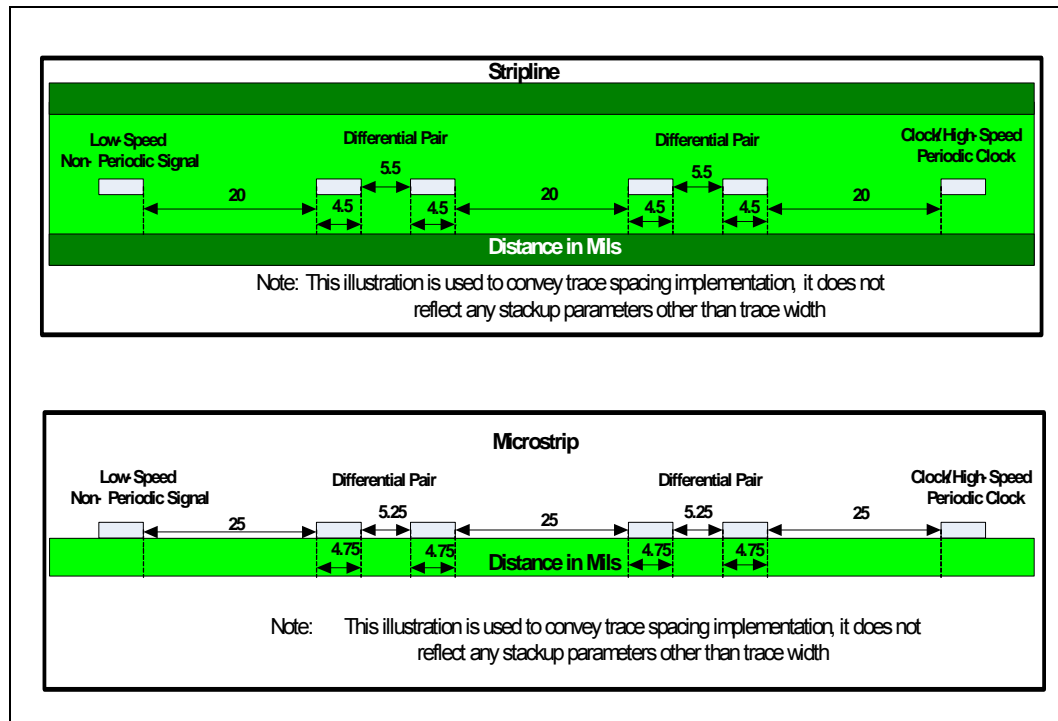
11.2.2 SATA Trace Length Guidelines and Pair Matching

If the trace length of the differential pair is longer than recommended, the high frequency differential signal will suffer signal attenuation and an increase of rise/fall time.

SATA signal pair traces must be trace length matched. The difference of two line traces in a differential pair must be restricted to below 20 mils, but less trace mismatch is recommended.

11.2.3 SATA AC Coupling Requirements

EP80579 requires AC coupling capacitors (10 nf) for both the SATA_TX and SATA_RX differential pairs. The series capacitors may be placed at any point on the traces between EP80579 and the SATA connector. However, it is recommended that they should be closed to the connector for optimal signal quality. Layouts must minimize the placement mismatch within a differential pair between the capacitors as much as possible; in other words, the distance between EP80579 and the capacitor on the 'P' signal must be identical to the distance between EP80579 and the capacitor on the 'N' signal for the same pair.

11.3 SATA General Purpose Signals — SATA1_GP, SATA0_GP

EP80579 has two SATA General Purpose input signals, SATAx_GP. These signals can be configured as interlock switch inputs corresponding to a given SATA port. When used as an interlock switch status indication, drive this signal to '0' to indicate the switch is closed and to a '1' to indicate the switch is open.

If interlock switches will not be used on the platform, these signals can be configured as GPIs.

Note: All SATAx_GP pins must be configured with the same function, either SATAx_GP signals or GPI signals.

Note: Each SATAx_GP pin that is not used must be terminated using an 8.2–10 kΩ pull-up resistor to VCC33.

11.4 SATA Clock Signals — SATA_CLKREFp, SATA_CLKREFn

These 100 MHz differential clock signals are discussed in Section 8.2.2, "CLK100 (SRC Clock) Group" on page 96.

11.5 SATA_RBIAS/SATA_RBIAS# Connection

It is recommended that the SATA_RBIAS and the SATA_RBIAS# pins be shorted at the package and then routed to one end of a 24.9 Ω ±1% resistor to ground. Place the resistor within 0.0″ to 0.5″ of EP80579. Avoid routing next to clock pins.

Figure 102.   SATA_RBIASp/SATA_RBIASn Connection
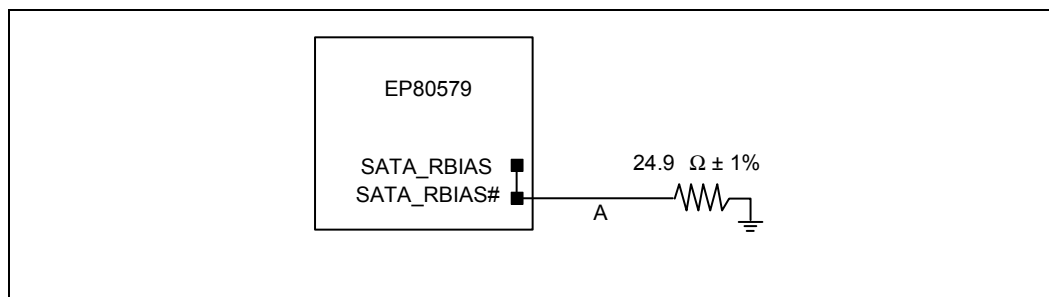
Table 59.   SATA_RBIAS/SATA_RBIAS# Routing Summary

Trace Impedance	SATA_RBIAS/ SATA_RBIAS# Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
50 Ω ±15% (single ended)	Short SATA_RBIAS and SATA_RBIAS# pins at the package.	A = 0.0" - 0.5" (EP80579 to Resistor)	N/A	N/A

11.6   SATALED# Implementation

EP80579 provides a signal (SATALED#) to indicate SATA device activity. In order for this signal to work in conjunction with Parallel ATA hard drives, it is recommended that designers implement similar glue logic as illustrated in Figure 103.

When low, SATALED# indicates SATA device activity and must activate the hard drive's LED. When tristated, the signal will not activate the LED. The hard drive LED is active low.

Figure 103. SATALED# Circuitry Example
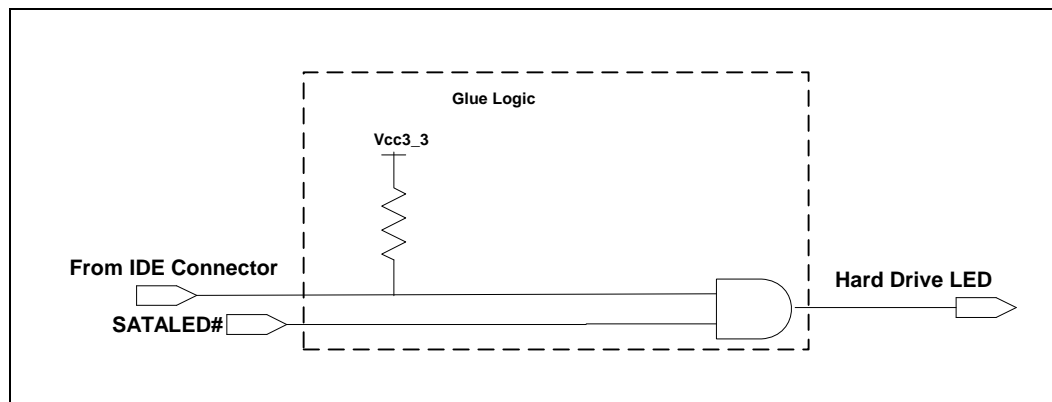
11.7   SATA Host Connector Placement Considerations

When placing SATA host connectors, applicable keep-out regions must be comprehended in the layout of the board. Figure 104 shows an example cable and the height required for bending the cable to a 90° bend. This can be used as an example when considering height obstruction regions.

Figure 104. SATA Cable 90° Bend Height Example
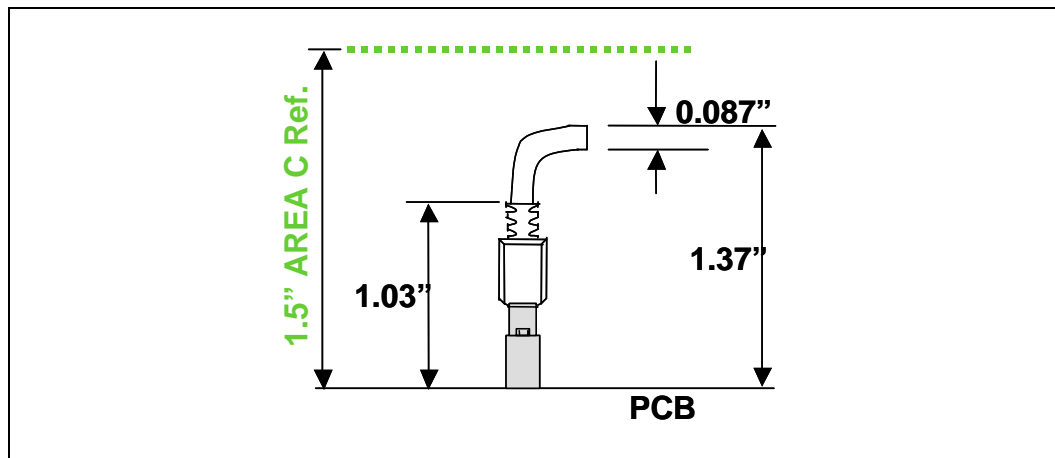
Figure 105 shows the ATX Specification rev 2.1 height restriction regions. With the example cable, Area C (near the traditional parallel ATA connector sites) is the recommended placement region to allow the cable to fully bend and avoid any obstructions.

Figure 105. SATA Host Connector Placement Region Recommendations
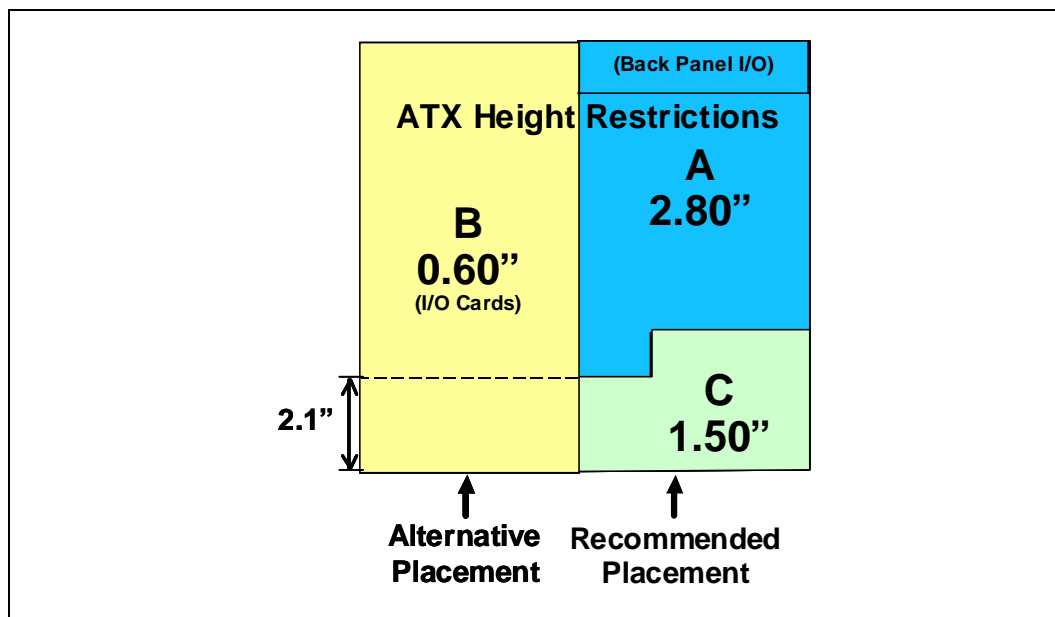
Designers must exercise great care to minimize conflicts with I/O cards (e.g., PCI cards) if Area B must be used. As noted in Figure 105, the lower 2.1" can reduce conflicts with short PCI cards.

Also, designers can optimize horizontal placement relative to the I/O cards to minimize conflicts with protrusions from the I/O card. Figure 106 shows an example implementation that places the host connector to left edge of the PCI card keep-out region.

Figure 106. SATA Host Connector Placement ATX Area B
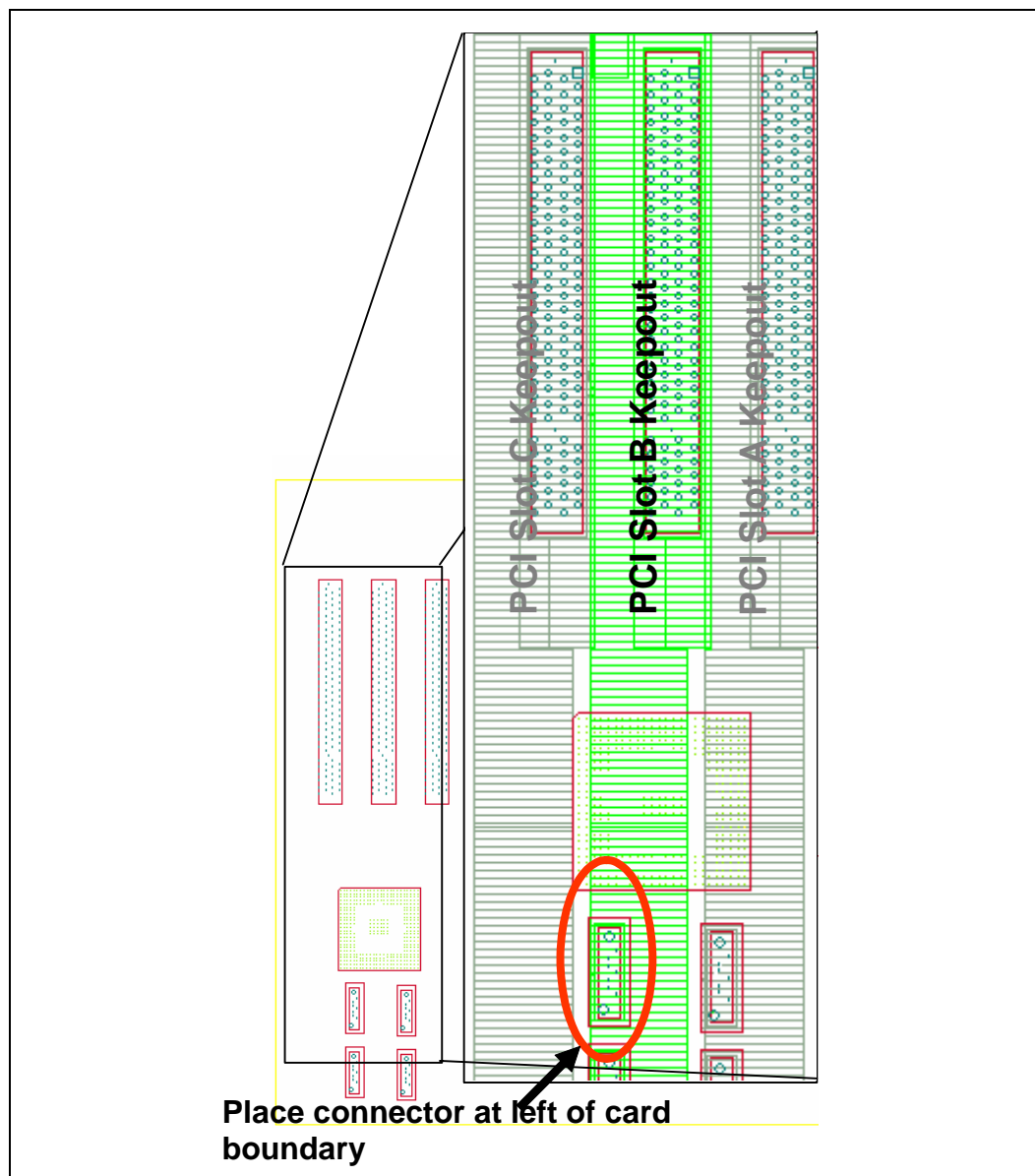
An additional consideration is the relative placement to other SATA host connectors as well as other neighboring parts and devices on the motherboard. Figure 107 shows an example of a case where two adjacent SATA host connectors were placed too close to one another. Figure 108 shows the minimum host connector spacings recommended in the SATA specification.

Figure 107. Example of Poor Host Connector Placement
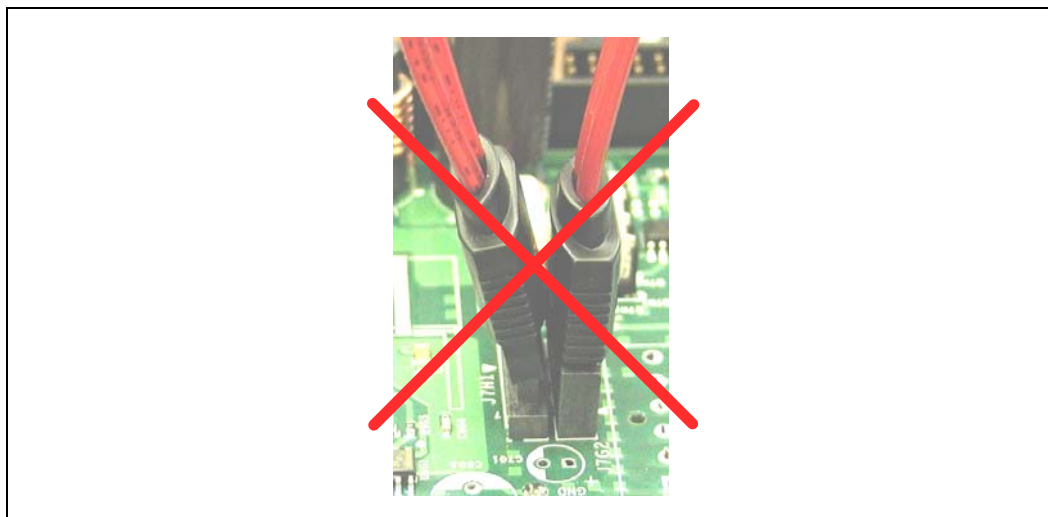
Figure 108. Minimum Host Connector Placement Spacing (From SATA Specification)
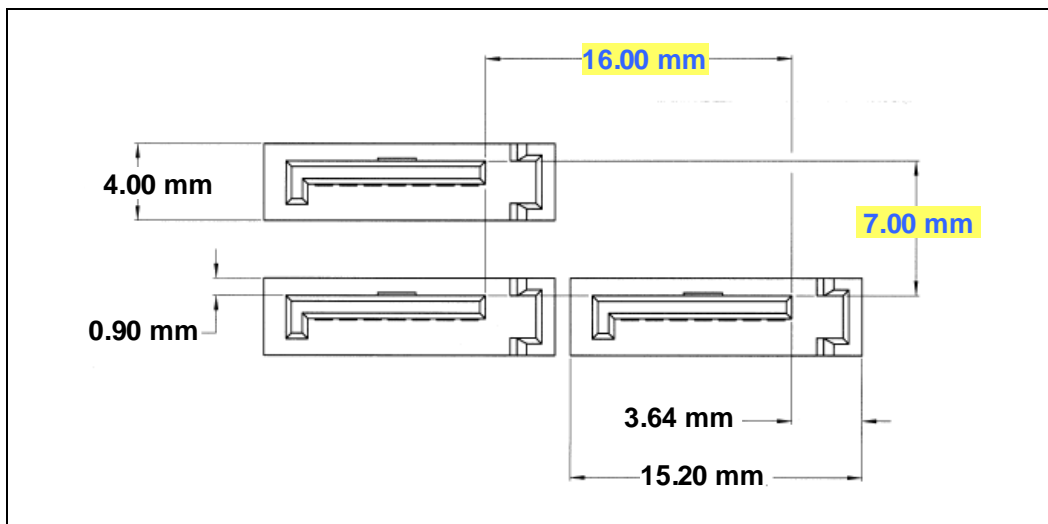
11.8   Terminating Unused SATA Interface

If an SATA port will not be implemented on the platform, the SATA_RXp[x], SATA_RXn[x], SATA_TXp[x], and SATA_TXn[x] signals may be left unconnected. 'x' is the port number not being used.

If the SATA interface will not be implemented on the platform (i.e., no ports will be used), designers must take the following actions:

• Terminate SATA Bias and clocks as follows:
    — Tie SATA_RBIAS and SATA_RBIAS# together and connect through a 24.9Ω ±1% resistor to ground.
    — Connect SATA_CLKREFp/SATA_CLKREFn to a 100 MHz clock source.
• The following signals can be left as no connects:

— SATA_RXp[1:0], SATA_RXn[1:0], SATA_TXp[1:0], SATA_TXn[1:0], and SATA_LED#.

• VCCAPLL must be connected directly to VCC1_2, but the filter caps are not required.

• Disable the SATA function via the system BIOS. See the description for the Function Disable Register in the *Intel® EP80579 Integrated Processor Product Line Datasheet*.

12.0 Universal Serial Bus (USB) Interface

12.1 USB Interface

The EP80579 contains one Enhanced Host Controller Interface (EHCI) USB 2.0 and one Universal Host Controller Interface (UHCI). The EP80579 supports a maximum of two USB ports, which can be configured independtly as either EHCI or UHCI. The connection to either a UHCI or the EHCI port is dynamic and dependent on the USB device capability, meaning that all ports support high-speed, full-speed, and low-speed USB devices.

The USB ports support a debug port at USB 2.0 transfer rates and also support wakeup from sleeping states S3 and S5. The USB 2.0 interfaces can be configured as master only.

12.2 Layout Guidelines

12.2.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design to help maximize signal quality and minimize EMI problems:

- Place EP80579 and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain the maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).

- Ensure the USB 2.0 signals are ground referenced. Based on recommended stack-up, this would mean signals routed on signal layer 3 and 8.

- Route USB 2.0 signals using a minimum number of vias and corners. This reduces reflections and impedance changes.

- When a 90° turn becomes necessary, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.

- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use and/or duplicate clocks.

- Avoid stubs on high-speed USB signals, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line must not be greater than 200 mils.

- Route all traces over continuous planes, with no interruptions. Avoid crossing over an anti-etch, plane split if possible. Crossing over anti-etch, plane splits, increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0 traces as much as practical. Changing layers to avoid crossing a plane split is preferable. See Section 12.3, "Plane Splits, Voids, and Cut-Outs (Anti-Etch)" on page 170 for further details.

- Separate signal traces into similar categories and route similar signal traces together, such as routing differential pairs together.

- Keep USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.

- Follow the 20*h general guideline by keeping traces at least 20*(height above the plane) away from the edge of the plane (Vcc or GND, depending on the plane the trace is over).

  For an example, the stackup height above the plane is 4.5 mils. This calculates to a spacing requirement of 90 mils from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

12.2.2 USB Differential Signals – USBp[1:0], USBn[1:0]

The USB interface has two differential pairs for a total of four signals. Route each pair differentially as microstrip or stripline. Table 60, Table 61, and Table 62 summarize the USBp and USBn routing guidelines for three cases:

- Case 1: Table 60 gives the routing guidelines for the USB controller to a connector on the board. See Figure 109.

- Case 2: Table 61 gives the routing guidelines to implement a front panel option that uses a cable to a daughter card panel for the USB connector. The choke is on the main board rather than on the daughter card panel. See Figure 110.

- Case 3: Table 62 gives the routing guidelines to implement a front panel option that uses a cable to a daughter card panel for the USB connector. In this case, the choke is on the daughter card panel. See Figure 111.

The front panel design option, Case 2, is made on the board using a 0 Ω resistor. Putting this resistor on the board required a layer change for the USB signals, which required simulation. The rear panel design option is similar to Case 1 in that it goes directly to a connector on the board. The front panel option is more stringent since the header will be connected to a front panel daughter card through a cable. See Section 12.7, "Front Panel Solutions" on page 173 for more information about front panel solutions.

Table 60. Case 1, USB Routing Guidelines – EP80579 to Connector (Sheet 1 of 2)

Parameter	Routing Guidelines	Figure
Signal Group	USBp[1:0], USBn[1:0]	-
Reference Plane	Ground Referenced, Stripline or Microstrip	-
Layer Assignment	Layers 1 or 10 (microstrip) Layers 3 or 8 (stripline)	-
Characteristic Trace Impedance (Zo)[1]	90 Ω ±10% (differential)	-
Nominal Trace Width	4.75 mils – microstrip 4.5 mils – stripline	Figure 112 Figure 113

Nominal Trace Spacing	Trace Spacing, edge-to-edge:
	    5.25 mils– microstrip
	    5.5 mils– stripline
	Pair-to-pair spacing, edge to edge: 45 mils minimum
	Spacing to clock signals: 45 mils minimum
	Spacing to non-clock signals: 45 mils minimum
		Figure 112
		Figure 113

Nominal Trace Length	Keep all lengths as short as possible. Length L2 must be as short as possible to keep the choke as close to the connector as possible. LT = 2–11 in. – microstrip (differential) 2–10 in. – stripline (differential)	Figure 109

Table 60.   Case 1, USB Routing Guidelines — EP80579 to Connector (Sheet 2 of 2)

Parameter	Routing Guidelines	Figure
Length Tuning Requirements	Length matching over LT within a pair is 60 mils or less.	-
EP80579 Breakout	4 mils width with 4 mils spacing for maximum of 500 mils, minimize this length.	-

Note:
1.   Strictly observe the characteristic trace impedance. In this regard, requirements for the layers, trace width, and trace spacing are secondary.

Figure 109. USB Trace Lengths From Controller to Connector
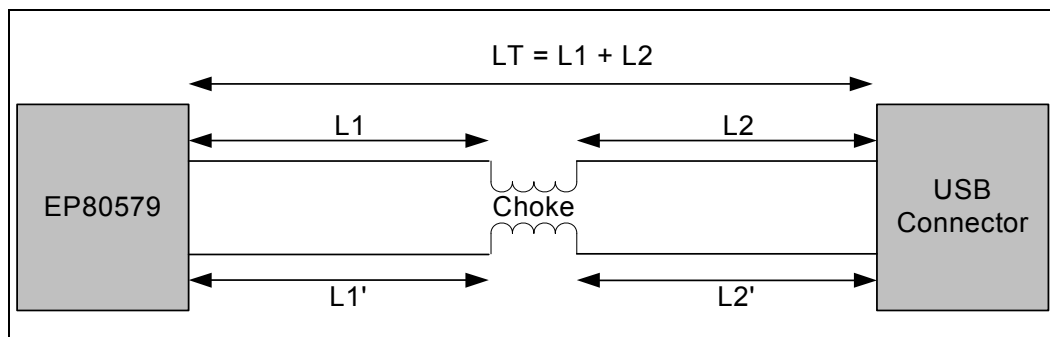
Table 61.   Case 2, USB Routing Guidelines — EP80579 Front Panel Option (Sheet 1 of 2)

Parameter	Routing Guidelines	Figure
Signal Group	USBp[1:0], USBn[1:0]	-
Reference Plane	Ground Referenced, Stripline or Microstrip	-
Layer Assignment	Layers 3 or 8	-
Characteristic Trace Impedance (Zo)[1]	90 Ω ±10% (differential)	-
Nominal Trace Width	4.75 mils – microstrip 4.5 mils – stripline	Figure 112 Figure 113

Nominal Trace Spacing	Trace Spacing, edge-to-edge:
	     5.25 mils–microstrip
	     5.5 mils– stripline
	Pair-to-pair spacing, edge to edge: 45 mils minimum
	Spacing to clock signals: 45 mils minimum
	Spacing to non-clock signals: 45 mils minimum
		Figure 112
		Figure 113

Nominal Trace Length[2]	Keep all lengths as short as possible.
	L1 = 1500 mils maximum
	L2 = LT - L1 - L3
	L3 = 1000 mils maximum
	LT (to connector =
	     2–11 in. – microstrip (differential)
	     2–10 in. – stripline (differential)
	LT to a header is dependent on the length of the cable connecting the header to the front panel daughter card. See Table 63 for detailed trace length requirements.
		Figure 110

Table 61. **Case 2, USB Routing Guidelines — EP80579 Front Panel Option (Sheet 2 of 2)**

Parameter	Routing Guidelines	Figure
Length Tuning Requirements	Length matching over LT within a pair is 60 mils or less Segment length matching, L1 to L1', L2 to L2', and L3 to L3' is 20 mils or less	-
EP80579 Breakout	4 mils width with 4 mils spacing for maximum of 500 mils, minimize this length	-

Note:
1.   Strictly observe the characteristic trace impedance. In this regard, requirements for the layers, trace width, and trace spacing are secondary.
2.   See Section 12.2.2.3 for more information on possible cable lengths for front panel headers.

Figure 110. **USB Trace Lengths For EP80579 Front Panel Solution**
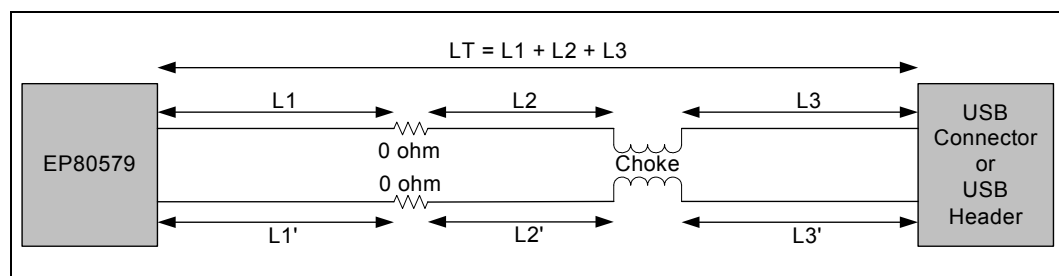
Table 62. **Case 3, USB Routing Guidelines — Optional Front Panel Solution**

Parameter	Routing Guidelines	Figure
Signal Group	USBp[1:0], USBn[1:0]	-
Reference Plane	Ground Referenced, Stripline, or Microstrip	-
Layer Assignment	Layers 3 or 8	-
Characteristic Trace Impedance (Zo)[1]	90 Ω ±10% (differential)	-
Nominal Trace Width	4.75 mils – microstrip 4.5 mils – stripline	Figure 112 Figure 113

Nominal Trace Spacing	Trace Spacing, edge-to-edge:
	    5.25 mils–microstrip
	    5.5 mils–stripline
	Pair-to-pair spacing, edge to edge: 45 mils minimum
	Spacing to clock signals: 45 mils minimum
	Spacing to non-clock signals: 45 mils minimum
		Figure 112
		Figure 113

Nominal Trace Length[2]	Keep all lengths as short as possible. L1 to a header is dependent on the length of the cable connecting the header to the front panel daughter card. See Table 63 for detailed trace length requirements.	Figure 111
Length Tuning Requirements	Length matching over LT within a pair is 60 mils or less Segment length matching, L1 to L1', L2 to L2', and L3 to L3' is 20 mils or less	-
EP80579 Breakout	4 mils width with 4 mils spacing for maximum of 500 mils, minimize this length	-

Note:
1.   Strictly observe the characteristic trace impedance. In this regard, requirements for the layers, trace width, and trace spacing are secondary.
2.   See Section 12.2.2.3 for more information on possible cable lengths for front panel headers.

Figure 111. USB Trace Lengths For Optional Front Panel Option
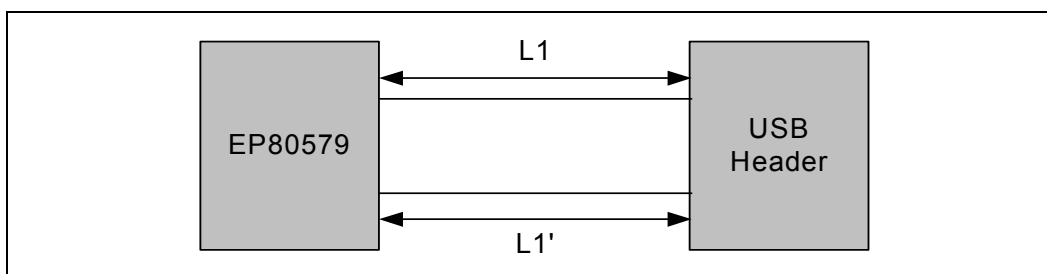
12.2.2.1 USB 2.0 Trace Separation

Use the following separation guidelines (Figure 112 and Figure 113 show the recommended trace spacing):

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω ±10% differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Ensure the amount and length of the deviations are kept to the minimum possible.

- Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used, keeping in mind that the target is a 90 Ω ±10% differential impedance. The recommended board stackup parameters for microstrip are 4.75 mil wide traces with 5.25 mil trace spacing, which results in approximately 90 Ω ±10% differential trace impedance. The recommended board stackup parameters for stripline are 4.5 mil wide traces with 5.5 mil trace spacing, which results in approximately 90 Ω ±10% differential trace impedance. See Figure 112 and Figure 113.

- Minimize the length of high-speed clock and periodic signal traces that run parallel to the high-speed USB signal lines to minimize crosstalk. The minimum recommended spacing to any clock signal is 0.050 inch.

Figure 112. (Microstrip) Recommended USB Trace Spacing
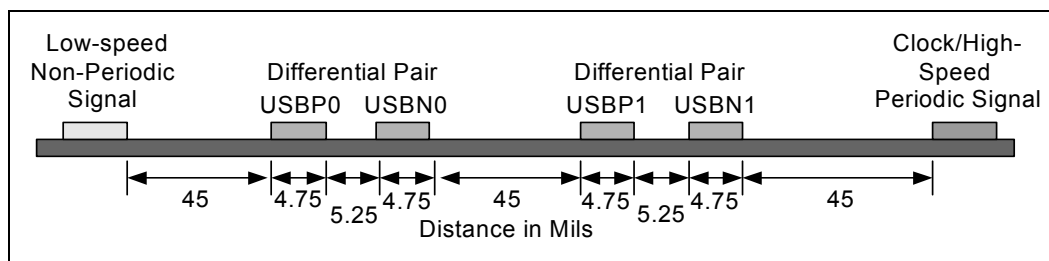
Figure 113. (Stripline) Recommended USB Trace Spacing
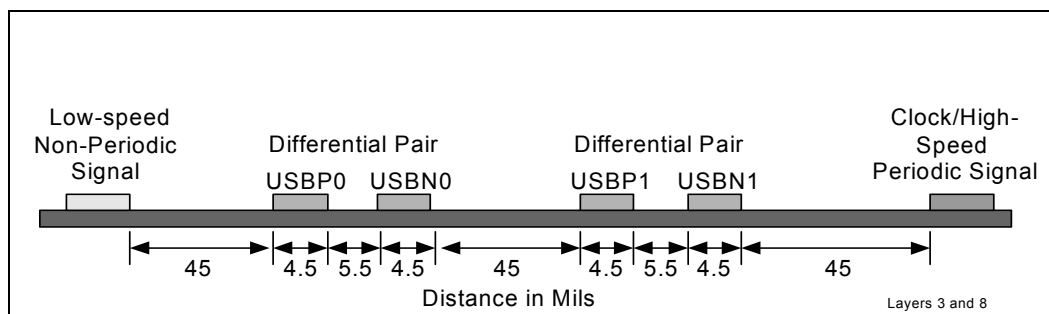
12.2.2.2 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces must be trace length matched. The maximum trace length mismatch within a USB 2.0 signal pair must be no greater than 60 mils.

12.2.2.3 USB 2.0 Trace Length Guidelines

Use the following trace length guidelines.

Table 63. USB 2.0 Trace Length Guidelines

Topology	Cable Length (inches)	Motherboard Trace Length Microstrip (inches)	Motherboard Trace Length Stripline (inches)	Card Trace Length (inches)	Signal Matching
Back Panel	N/A	2–11	2–10	N/A	Keep the maximum mismatch within data pairs to less than 60 mils. This is over the entire routing space.
Front Panel	6	7	7	1.5–2	
	7.5	6	6	1.5–2	
	9	5	4	1.5–2	
	10.5	4	3	1.5–2	
	11	N/A	2	1.5–2	
	12	2	N/A	1.5–2	

Notes:
1. The numbers in Table 63 are based on the following simulation assumptions:
   a. An approximate 1:1 trade-off can be assumed for the motherboard trace length vs. the daughter card trace length (e.g., trade 1 inch of daughter card trace length for 1 inch of motherboard trace length).
   b. The trace length on front panel daughter card has a maximum trace length of 2 inches.
   c. USB twisted-pair shielded cable as specified in the USB 2.0 Specification was used.
2. For front panel solutions, signal matching is considered from EP80579 to the front panel header.

12.2.3 USB_RBIASp/USB_RBIASn Connection

Intel recommends designers short the USB_RBIASp and the USB_RBIASn pins at the package and then route to one end of a 22.6 Ω ±1% resistor to ground. Place the resistor within 0.50 inch of EP80579. Avoid routing next to clock pins. The following are the general recommendation for the USB_RBIAS:

- Route on top layer (recommended, not required).
- 50 Ω+/-15% single ended impedance/impedance defines trace width.
- Signals must be Ground referenced.
- Spacing requirements may be reduced to 4mil through the pin/via field.

Figure 114. USB_RBIASp/USB_RBIASn Connection
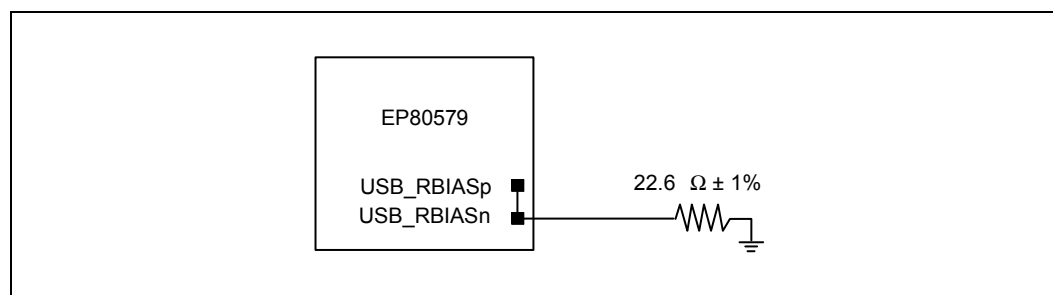
Table 64. **USB_RBIASp/USB_RBIASn Routing Summary**

Trace Impedance	USB_RBIASp/USB_RBIASn Routing Requirements	Maximum Trace Length	Signal Length Matching	Signal Referencing
50 Ω ±15%	Short USB_RBIASp and USB_RBIASn pins at the package.	A = 0.50 inch (EP80579 to Resistor)	N/A	N/A

12.2.4 Clock signal -- USB CLK48

The USB Clock 48 MHz is discussed in Section 8.2.5, "CLK48 Group" on page 102.

12.2.5 USB Over Current protection — OC[1:0]#

Each USB port has an input to indicate when there is an over current condition. These inputs can be connected to the over current signal of a current limited power distribution switch. When an over current condition occurs, the switch will drive these signals low to indicate the condition to the USB controller. If these signals are not used, pull them up to VCCPSUS with an 10 kΩ resistor.

12.3 Plane Splits, Voids, and Cut-Outs (Anti-Etch)

The guidelines in the following sections apply to the use of plane splits, voids, and cut-outs.

12.3.1 Vcc Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the Vcc plane:

- Traces must not cross anti-etch since it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e., the Full-Speed Single Ended Zero is common mode).

- Avoid routing USB 2.0 signals within 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages, it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in environments that use several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors, 1 µF or lower in value, that bridge voltage plane splits close to where high-speed signals or clocks cross the plane split. The capacitor ends must tie to each plane separated by the split. They are also used to bridge or bypass power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates V5REF and VCC33 planes must have a stitching cap placed near any high-speed signal crossing. One side of the cap must tie to V5REF, and the other side must tie to VCC33. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.
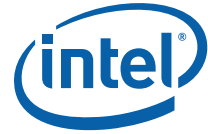
12.3.2   GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

12.4   USB Power Line Layout Topology

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this kind provide two types of protection during dynamic attach and detach situations on the bus:

- inrush current limiting (droop)
- dynamic detach flyback protection

These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. Designers must place capacitors as close as possible to the port and the power-carrying traces must be as wide as possible, preferably, a plane. A good general guideline is to make the power-carrying traces wide enough that the system fuse will blow on an over current event. If the system fuse is rated at 1 amp, the power-carrying traces must be wide enough to carry at least 1.5 amps.

The USB power traces should be at least .050" wide to ensure adequate current carrying capability. This requirement is implemented in the rule set by identifying USB power nets and applying a minimum .050" line width to the entire net. Not all segments of all of these nets will carry high current therefore the requirement built into the rule set should be reconsidered as the design progresses.

Figure 115.   Good Downstream Power Connection
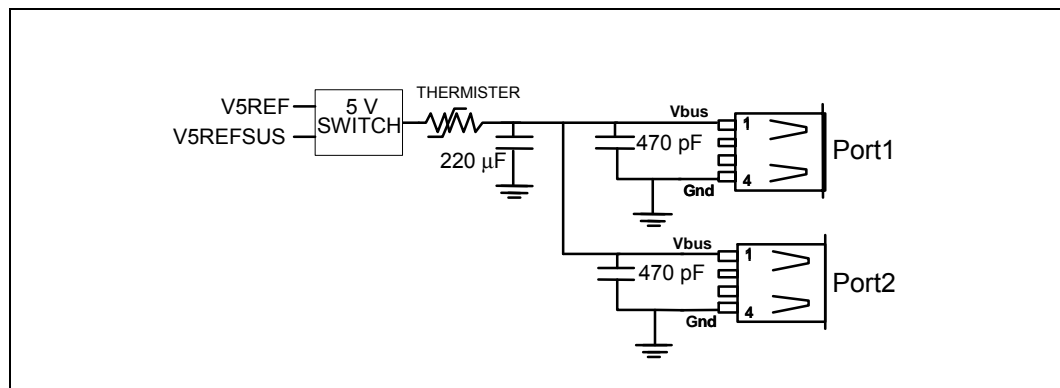
12.5   EMI Considerations

The guidelines in the following sections apply to the selection and placement of common mode chokes and ESD protection devices.

12.5.1   Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design must include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Figure 116 shows the schematic of a typical common mode choke and ESD suppression components. Place the choke as close as possible to the USB connector signal pins. In systems that route USB to a front panel header, the choke must be placed on the front panel card. See Section 12.7.3, "Front Panel Daughter Card" on page 176.

Figure 116. A Common Mode Choke
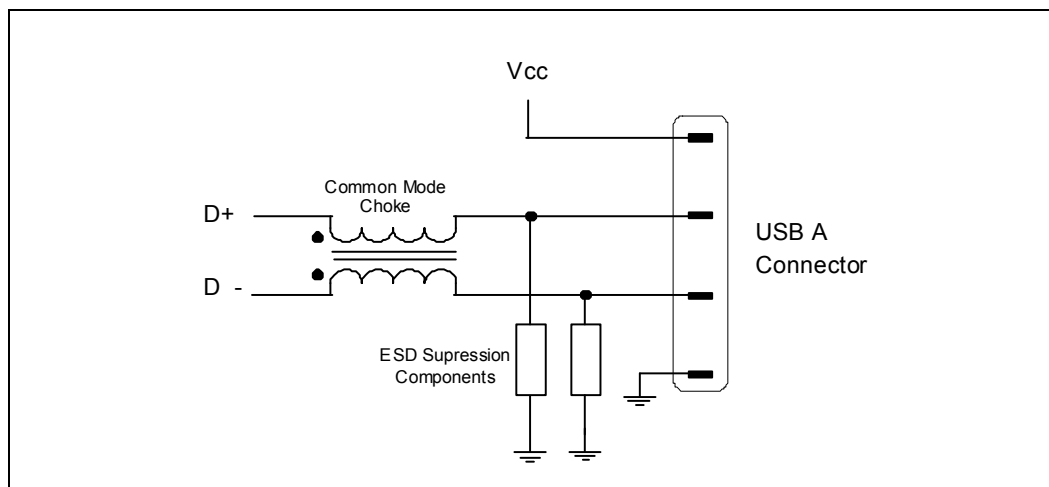
Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so you must test the effects of the common mode choke on full-speed and high-speed signal quality. Common mode chokes with a target impedance of 80–90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process:

- Choose a part with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that must be suppressed.

- After obtaining a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality, so use care when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed, and high-speed USB operation.

12.6 ESD

Classic USB (1.0/1.1) provided ESD suppression by using in-line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 because of the higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common mode choke and the USB connector data pins as shown in Figure 116. Other types of low-capacitance ESD protection devices may work as well, but were not investigated. As with the common mode choke solution, Intel recommends designers include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

Recommended proper placement of any ESD protection device is "on the data lines between the common mode choke and the USB connector signal pin". Constraints to control these placements are not included in this rule set. Stubs caused by these components must be less than 0.200".

12.7 Front Panel Solutions

12.7.1 Internal USB Cables

The front panel internal cable solution must meet all the requirements of Chapter 6 in the *USB 2.0 Specification* for high/full-speed cabling for each port with the exceptions described in Section 12.7.1.2, "Internal Cable Option 2" on page 173.

12.7.1.1 Internal Cable Option 1

Use standard high/full-speed compatible USB cables.

These must meet all cabling requirements called out in Chapter 6 of the *USB 2.0 Specification*. The recommended motherboard mating connector pin-out is covered in Section 12.7.2, "Motherboard/PCB Mating Connector" on page 174.

12.7.1.2 Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 in the *USB 2.0 Specification* with the following additions/exceptions:

- The cables can share a common jacket, shield, and drain wire.
- Two ports with signal pairs that share a common jacket may combine Vbus and ground wires into a single wire, provided the following conditions are met:
  - The bypass capacitance required by Section 7.2.4.1 of the *USB 2.0 Specification* is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughter card). See Section 12.7.3, "Front Panel Daughter Card" on page 176 for details.
  - Selecting the proper wire size. A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the USB 2.0 Specification that has equal or less than half the resistance of either of the two wires being combined. The data is provided for reference in Table 65.

Table 65.   Conductor Resistance (Table 6-6 from *USB 2.0 Specification*)

American Wire Gauge (AWG)	Ohm/100 Meters Maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

Example: Two 24-gauge (AWG) power or ground wires can be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the *USB 2.0 Specification* at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port can usually meet droop requirements by providing adequate capacitance near the motherboard mating connector since droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients will be seen/dampened by the capacitance at the motherboard mating connector before they can cause problems with the adjacent port sharing the same cable. See Sections 7.2.2 and 7.2.4.1 of the *USB 2.0 Specification* for more details.

Cables that contain more than two signal pairs are not recommended due to unpredictable impedance characteristics.

12.7.2   Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure signal quality is not adversely affected due to a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the *USB 2.0 Specification*.

12.7.2.1   Pin-out

A ten pin, 0.1-inch pitch stake pin assembly is recommended with the schematic shown in Figure 117 and the pin-out listed in Table 66.

Figure 117. Front Panel Header Schematic
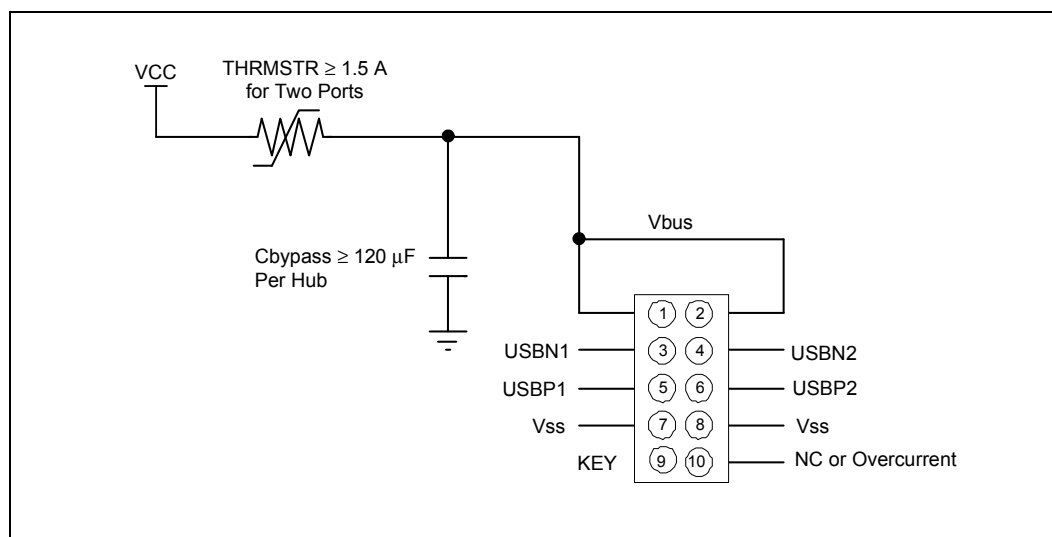
Table 66. Front Panel Header Pin-Out

Pin	Description
1	Vbus
2	Vbus
3	DM1
4	DM2
5	DP1
6	DP2
7	Vss
8	Vss
9	KEY
10	No connect or over-current sense

Intel highly recommends that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage, for the following reasons:

- protects the motherboard from damage in the case where an un-fused front panel cable solution is used.

- provides protection from damage if an un-keyed cable is inadvertently plugged onto the front panel USB connector.

- provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between Vbus and ground.

12.7.2.2 Routing Considerations

Keep the following routing considerations in mind:

- Traces or surface shapes from Vcc to the thermistor, to C_{BYPASS}, and to the connector power and ground pins must be at least 50 mils wide to ensure adequate current carrying capability.

- Power and ground nets must have double vias.

- Trace lengths must be kept as short as possible.

12.7.3 Front Panel Daughter Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 118 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card.

Figure 118. Motherboard Front Panel USB Support

Front Panel USB Ports
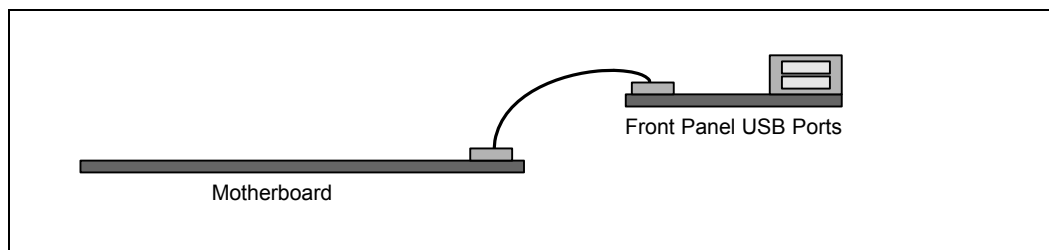
Motherboard

When designing the motherboard with front/side panel support, the system integrator must know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure there are not duplicate EMI/ESD/thermistor components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure.

12.7.3.1 Front Panel Daughter Card Design Guidelines

Keep the following front panel daughter card design guidelines in mind:

- Place the Vbus bypass capacitance, CMC, and ESD suppression components on the daughter card as close as possible to the connector pins.

- Follow the same layout, routing, and impedance control guidelines as specified for motherboards.

- Minimize the trace length on the front panel connector card. Less than a 2 inch trace length is recommended.

- Use the same mating connector pin-out as outlined for the motherboard in Section 12.7.2, "Motherboard/PCB Mating Connector" on page 174.

- Use the same routing guidelines as described in Section 12.2, "Layout Guidelines" on page 164.

- Follow trace length guidelines given in Table 63.

12.8 Terminating Unused USB Interface

If the USB interface is not used, the termination is recommended to the interface.
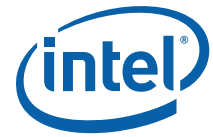
- USBp[1:0], USBn[1:0] - These signals have integrated 15kW pull-down resistors. Unused USB ports can be left as no connect.

- OC[1:0]# - If these signals are not used, pull them up to VCCPSUS with an 10 kΩ resistor.

- USB_RBIASn, USB_RBIASp - See Section 12.2.3

- CLK48 - The USB Clock 48 MHz is referenced in Section 8.2.5, "CLK48 Group" on page 102.

13.0 System Management Bus (SMBus) Interface

13.1 SMBus 2.0/SMLink Interface

The EP80579 integrates two SMBus 2.0 controllers. The SMBus provides an interface to manage peripherals, such as serial presence detection (SPD) on RAM, thermal sensors, etc. The slave interface allows an external microcontroller to access system resources.

The EP80579 consists of a host/slave controller and a slave controller, both of which are I^{2}C compliant. These interfaces use signals SMBCLK, SMBDATA, SMBSDA, and SMBSCL, respectively, to send and receive data from components residing on these buses.

The host/I^{2}C bus has a flexible SMBus/SMLink architecture to optimize for Alert Specification Format (ASF) and eliminate board requirements. The host interface allows the processor to communicate via the SMBus. The SMB slave can access internal configuration registers, allowing a server management card to control system configuration and read various error and status information.

Figure 119. SMBus 2.0 / SMLink Interface
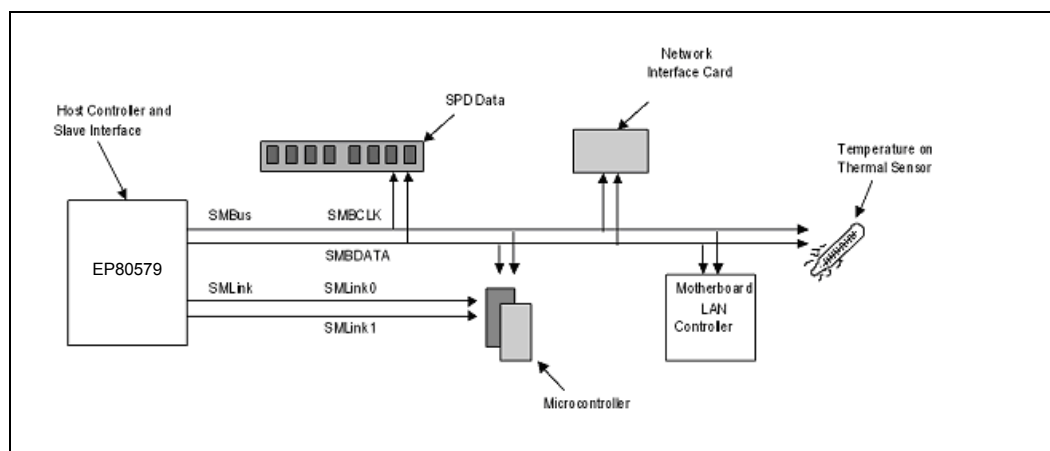
13.1.1 SMBus Design Considerations

No single SMBus design solution will work for all platforms. Designers must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process more challenging, since they add extra capacitance to the bus. This extra capacitance has a large effect on the bus time constant, which in turn affects the bus rise and fall times.

Primary considerations in the design process are as follows:

• Device class (High/Low power—most designs use primarily High Power Devices)
• Devices that must run in S3

- Amount of current available in the suspend power well (i.e., minimizing the load of the suspend power well)

13.1.2 General Design Considerations

The following are general design considerations:

- The pull-up resistor size for the SMBus data (SMBDATA) and clock (SMBCLK) signals is dependent on the bus load, which includes leakage currents for all devices. Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant ($\mathrm{Resistance} \times \mathrm{Capacitance}$) does not meet the SMBus rise and time specification.

- The maximum bus capacitance that a physical segment can reach is 400 pF.

- SMBus devices that can operate in STR (Suspend-to-RAM) must be powered by the suspend power well.

- SMBus address contention as a design consideration.

- I^{2}C devices should be powered by the appropriate core power well voltage. During an I^{2}C transaction, in which the device is sending information to EP80579, the device may not release the SMBus if EP80579 receives an asynchronous reset. By using the core power, the BIOS is able to reset the device if necessary. SMBus 2.0-compliant devices have a time-out capability that makes them insusceptible to this I^{2}C issue, allowing flexibility in choosing a voltage supply.

- If SMBus is connected to PCI Express, it must be connected to all PCI Express slots.

13.1.3 High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices while also allowing SMBus devices to communicate while in S3. Leakage in the suspend power well is minimized by keeping non-essential devices connected to the core power well. This is accomplished by the use of a FET to isolate the devices powered by the core and suspend power wells. See Figure 120.

Figure 120. High Power/Low Power Mixed Suspend/Core Power Well Architecture
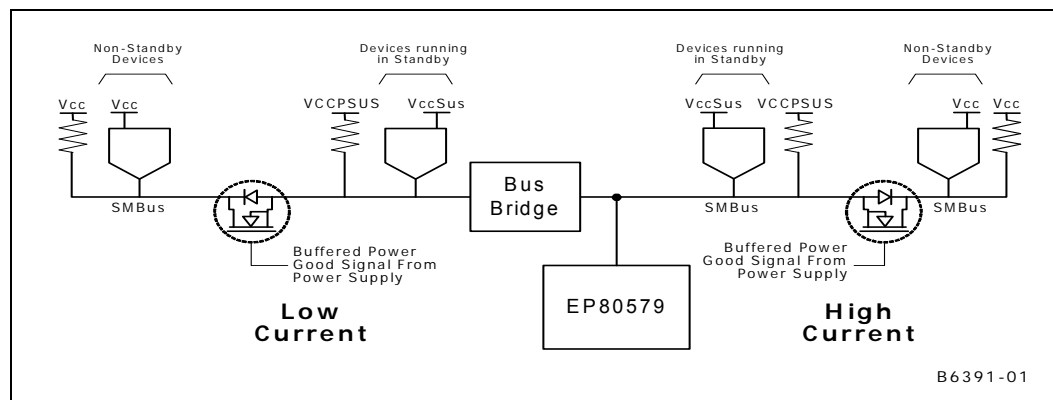
Additional considerations for mixed architecture are shown below:

- The bus bridge must be powered by a voltage from the suspend power well.

- Devices that are powered by the suspend power well must not drive into other devices that are powered off. This is accomplished with the "bus switch."

- The bus bridge can be a device similar to the Phillips* PCA9515, used on the Development Board.

13.1.4 Calculating the Physical Segment Pull-Up Resistor

The following tables are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, a bus bridge device similar to the Phillips PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 67.   Bus Capacitance Reference Chart

Device	No. of Devices/ Trace Length	Capacitance Includes	Cap (pF)
EP80579	1	Pin Capacitance	12
CK410	1	Pin Capacitance	10
DIMMs	2	Pin Capacitance (5 pF) + 4" worth of trace capacitance (2 pF/inch)	28
PCI Express Slots	2	Each add-in card is allowed up to 40 pF + 3 pF per each connector	86
SMBus Trace Length in inches	24	2 pF per inch of trace length	48
	36		72
	48		96

Table 68.   Bus Capacitance/Pull-Up Resistor Relationship

Physical Bus Segment Capacitance	Pull-Up Range (For Vcc = 3.3V)
0 to 100 pF	8.2 kΩ to 1.2 kΩ
100 pF to 200 pF	4.7 kΩ to 1.2 kΩ
200 pF to 300 pF	3.3 kΩ to 1.2 kΩ
300 pF to 400 pF	2.2 kΩ to 1.2 kΩ

13.2 Enabled System Management Features (Optional)

System management features for EP80579 allow a system platform to administer and monitor the system, such as processor temperature monitoring, power failure, etc. System management feature can be implemented by using a separate controller commonly referred to as a bus management controller (BMC), See Table 69. The Development Board does not support this feature. This feature can be custom design to consider add the BMC connector for an add in the BMC card. Intel did not validate this solution on the Development Board.

A list of system management features appears below

Note: Most of these features are theoretical implementations, they are not presented in the Development Board implementation and have not been simulated.

- Monitor processor temperature
  The processor has a thermal diode connected to the THERMDA and THERMDC pins. The LM93 uses its A/D converter to determine the processor temperature. When the processor temperature reaches its threshold, the system management sends an alert to the administrator.

- Adjust processor temperature
  Power consumption can be adjusted by controlling the PWM fan speed. The system management can adjust the fan speed depending on the processor temperature. If
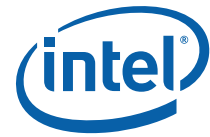
a system gets too hot, an alert is sent to the system management controller. The administrator can then turn the system off.

• Monitor EP80579 device registers

During normal run time, the system management can poll all error registers in the device. When an error condition occurs, the event can log in the system management event log. If the system crashes, the administrator can review the system management error log to find out what caused the crash.

• Monitoring in the out-of-band operation

When the system is in standby or is powered down, some system management capabilities are still available, such as power on, access to the IPMI system event log (SEL), Field Replacement Unit log (FRU), and pre-boot/BIOS boot process.

• Power failure

The system management can monitor the powergood signals on EP80579 to detect power subsystem failure.

• System reset

The reset button on the front panel is routed through the BMC, allowing the BMC to monitor and control reset to possibly prevent reset from occurring. Also, the BMC can detect system live lock using a timer for monitoring the system. This remote management is used to reset the system.

• Monitor processor events

System management monitors the processor's THERMTRIP#, PROCHOT#, IERR#, and other signals and takes appropriate action when necessary. This action includes logging the event, sending a warning to the administrator and shutting the system down (if necessary).

• Clear CMOS

If the CMOS needs to be cleared, the administrator can clear it remotely via the BMC.

• Emergency management port

The emergency management port (EMP) provides serial port access to the BMC, which may be accessed while the system is powered down. It provides the user with a command line interface (CLI) that can be used to access the SEL, FRU, and service boot partition.

• Platform event paging

The BMC performs platform event paging (PEP) to alert system administrators of system events and reduce server downtime. The administrator can get an alert by pager or over a network about the system events using a UART or external serial modem.

• System event log

The BMC supports system event log, FRU, and SDR. The BMC logs all events detected by the hardware sensors. The system event log is synchronized with the BIOS real-time clock to provide an accurate timestamp for logged events.

13.3 Enabled System Management Vendors (Optional)

Several system management vendors listed below can be consider for the system management feature design. See Table 69.

Table 69.   Enabled System Management Vendors

Vendor Info
Agilent Technologies*   N2523A, N2532A, N2531A   http://www.agilent.com/find/rmc
American Megatrends*   http://www.ami.com/
National Semiconductor*   NSC PC87431, PC87435, PC87436   http://www.national.com/
OSA Technologies*   http://www.osatechnologies.com/
Phoenix Technologies Ltd.*   http://www.phoenix.com/
QLogic*   Zircon UL   http://www.qlogic.com/
Renesas Technology, Inc.*   H8S 2100 /216x Series   http://www.renesas.com/

13.4   Development Board System Management Implementation

EP80579 provides SMBus connectivity and provides system management communication. Figure 121 shows the implementation as a single bus with three repeaters used for voltage translation, fan out and isolation. Since the Development Board is a reference board, several system management features are not implemented.

Figure 121. Development Board System Management - SMBus Block Diagram
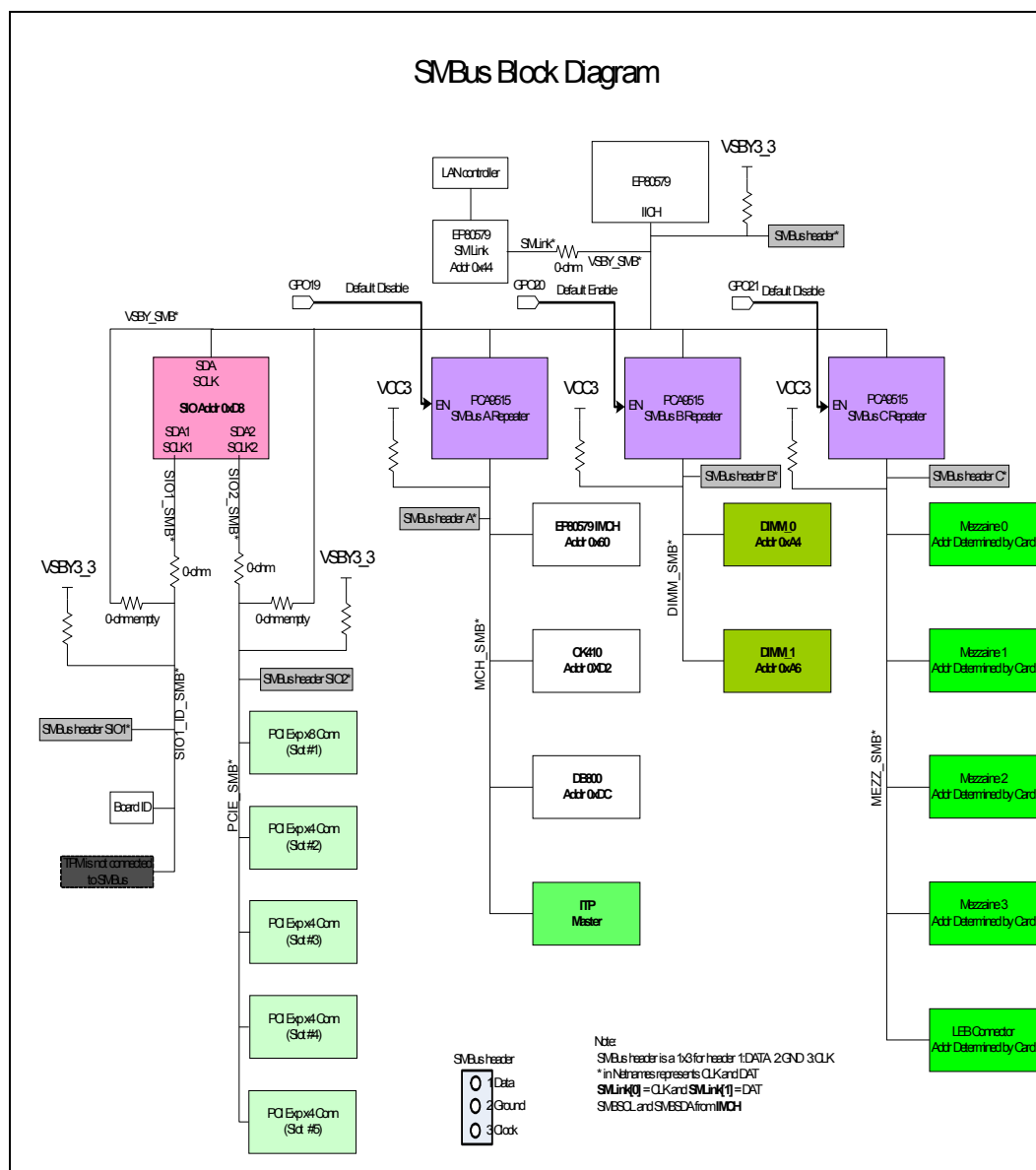
EP80579's SMBus has many features for system management. The following sections show an example implementation of system management portions of EP80579 in the Development Board. The system platform may use a BMC on a separate system management card, although this is not part of the Development Board implementation. This card is used for enabling and validating multiple system management vendors. Intel highly recommends an embedded solution with the BMC of choice. Any controller can serve this function. This section provides an example of what was implemented in the Development Board. The example below is one of the possible system management solutions for the EP80579.

13.4.1   SIO Implementation

The System Management interface requires access to a serial port for out-of-band operation and for alerts. The SMC can have its own dedicated UART and COM port on the baseboard or it can be wired to share system resources. An SIO can be chosen with the option of a serial port master, reducing parts and board real estate. In the circuit depicted in Figure 122, the SIO must be on standby power for out-of-band operation. The Development Board uses an SMSC SCH5027 SIO.

Figure 122. System Management SIO Implementation

Notes:

1. This is an example for the EP80579 SMBus interface implementation in the EP80579 Development Board. This diagram idoes not present every signal. See the EP80579 Development Board schematics for more details.

2. The Optional BMC connection is not implemented in the EP80579 Development Board.

14.0 Low Pin Count (LPC) Interface

14.1 LPC Interface

The EP80579 provides a Low Pin Count (LPC) interface that is compliant with the *Low Pin Count Interface Specification,* Revision 1.0. The general design of the EP80579 LPC interface is shown in Figure 123.

This section provides design guidelines for interfacing properly with the LPC bus. These guidelines help minimize signal integrity issues and maintain conformance to LPC specifications. Figure 123 shows a general design connection to a typical LPC interface. The EP80579 implements all of the signals that are shown as optional; peripherals are not a required part of the implementation.

- LAD[3:0] are shared address and data lines with device components.
- LCLK (clock) must be connected to a 33 MHz clock (EP80579 PCICLK is recommended).
- LRESET# (reset) must be connected to EP80579's PLTRST# or PCIRST# signal.
- LFRAME# (cycle termination) is shared with FWH and the SIO.
- SERIRQ is the serialized IRQ line.
- LPCPD# (suspend status and LPC power down) is connected to the EP80579 SUS_STAT#.
- LSMI# may be connected to any of the EP80579 GPIO signals, as they may be configured as inputs to generate an SMI#.
- Connecting the Super I/O PME# to the PME# signal is possible. A better choice is to connect it to one of the GPIO signals, as they may be configured to generate an SCI.
- All other signals have the same name on the EP80579 and on the LPC interface.

Figure 123. LPC Interface Diagram
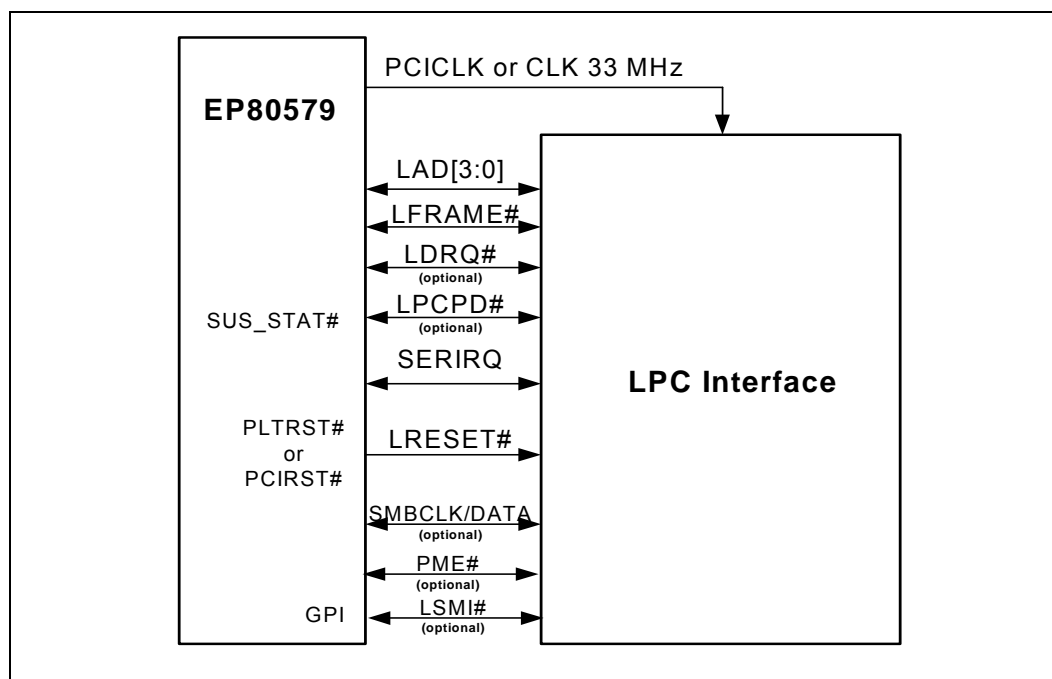
14.2 LPC Layout

14.2.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design:

- LPC signals should be ground referenced.
- Route all traces using microstrip or stripline over continuous planes (Vcc or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane may cause signal reflections and should be avoided.
- Route LPC signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- No 90-degree bends or stubs.

14.2.2 LPC Interface Routing and Topology

This section provides guidelines for topology routing. The Development Board provides four basic component devices connected to the EP80579's LPC interface. These devices include:

- port 80
- Firmware Hub
- Trusted Platform Module
- Super IO

Figure 124 provides a block diagram:

Figure 124. Development Board LPC Interface Block Diagram
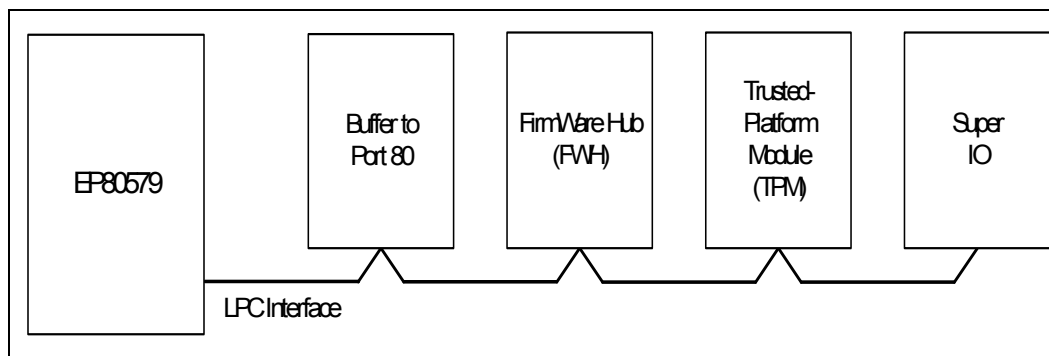
The routine and topology guidelines in Figure 125 are based on the following:

- Ten layer stack up
- LPC routing used layer 8
- Trace impedance 50 Ω ±10%
- LPC clock traces should be trace length matched. Maximum trace length mismatch between clocks coming from the clock driver should be no greater that 250 mils.

Figure 125. Topology of LPC Interface
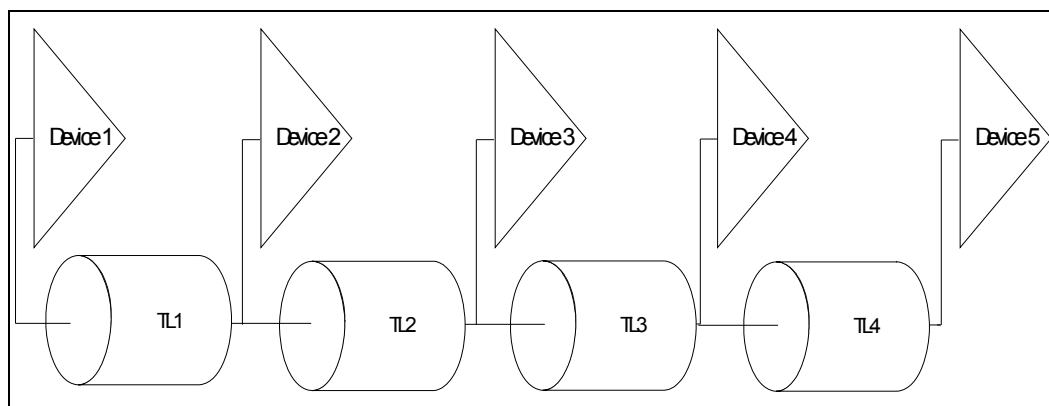
Figure 126 and Table 70 show the EP80579's LPC interface design recommendation routing for all signals except clock:

- Daisy chain all signals to every device on the bus
- Use a total of five or fewer devices on the LPC bus
- The EP80579 can be placed anywhere in the bus daisy chain (can be in the middle or at the end of the chain)
- There is no length matching requirement among the signals, as long as each signal meets the length target

Table 70. **Routing Recommendations**

Parameter	Routing Guideline
Signal Group	All signals, except clock
Routing	Route over unbroken reference plane (Ground or Power) microstrip or stripline
Minimum Trace Spacing (edge-to-edge) with any other signals	4 times the reference plane height (which ever reference plane is closest. For instance (only as an example): • stripline: Reference plane at 4 mils on one side and 12 mils on other side. Spacing needs to be 16 mils • microstrip: Reference plane at 4 mils. Spacing needs to be 16 mils
Trace Length - applies to TL1, TL2, TL3, and TL4 (Trace Length from one device to other device)	1 inch min to 12 inch max (referred to total length restriction)
Total length of the traces from Device1 to Device 5 (or last device from the chain)	16.0" maximum (maximum distance between the end devices in the daisy chain)
Vias	2 vias on each segment (TL1, TL2…)

14.2.3 Clock Signals -- CLK33

The 33 MHz clock is discussed in Section 8.2.3, "CLK33 Group" on page 99.

14.3 Trusted Platform Module (TPM) Guidelines

Trusted Platform Module(s) (TPM) are a Trusted Computing Platform Alliance* (TCPA) low cost security solution to increase confidence on system security. The TPM is a device that resides on the motherboard and is connected to EP80579 using the Low Pin Count (LPC) bus to communicate with the rest of the board.

14.3.1 TPM Design Considerations

See the *TPM Specification*, Rev. 1.1 for TPM specific design considerations.

14.3.2 TPM Design Considerations

Routing requirements for the TPM LPC interface are as follows:

• LAD[3:0] (address/data lines) are shared with the Firmware Hub (FWH) component and the Super I/O (SIO) device.

• LCLK (clock) must be connected to a 33 MHz clock (PCICLK).

• LRESET# (reset) must be connected to PLTRST#.

• LFRAME# (cycle termination) is shared with FWH and the SIO.

• SERIRQ (serialized IRQ) is shared with the SIO.

• LPCPD# (suspend status and LPC power down) is shared with SIO connected to SUS_STAT#.

Figure 126 and Figure 127 are block diagrams showing the TPM interconnect to the EP80579. Some of the LPC signals shown in the block diagram are shared with other LPC components that reside on the LPC interconnect, such as the SIO and the FWH.

Figure 126. TPM 1.1/EP80579 Block Diagram
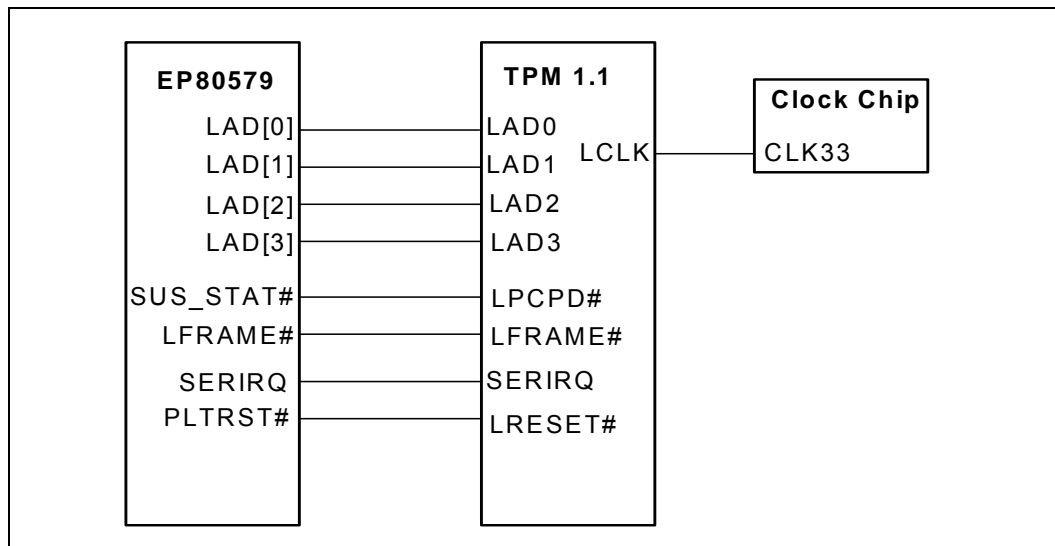
Figure 127. TPM 1.2/EP80579 Block Diagram
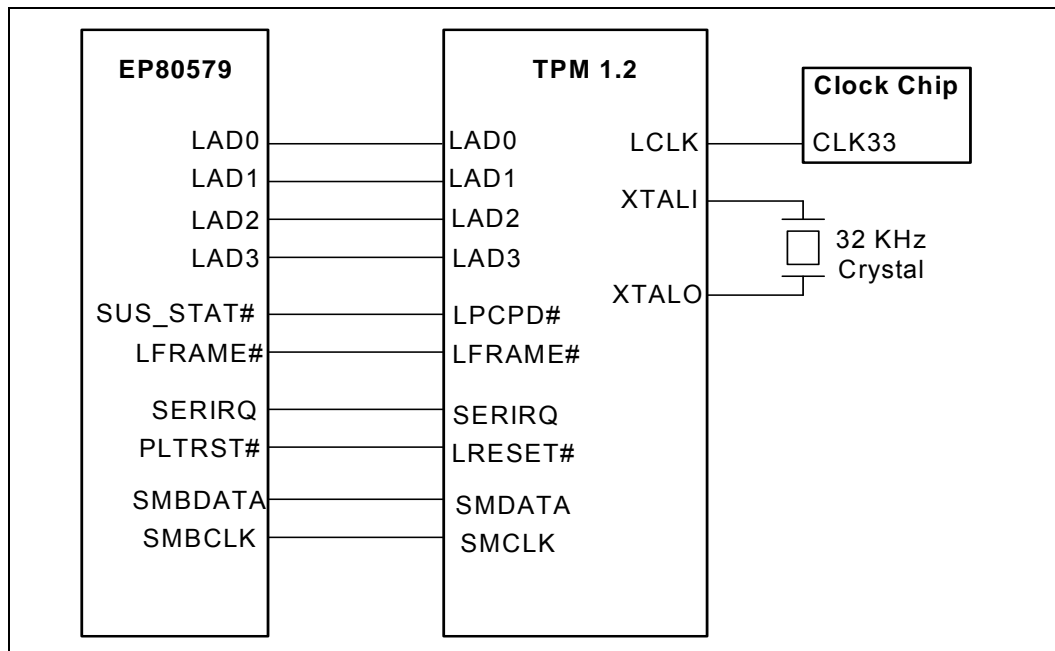
14.3.3 Motherboard Placement Consideration

Optimum routing can typically be achieved by placing the TPM close to the EP80579 or other LPC peripherals (e.g., Firmware Hub, Super I/O).

The TPM is a security device that must be shielded as much as possible from physical access. In high-security implementations, there are a number of mechanisms that can be used to detect or prevent physical system intrusion, but such mechanisms are beyond the scope of this design guide. However, convenience of physical access to the TPM can be minimized by placing the TPM behind the memory DIMMs. In an ATX or

µATX chassis, the area behind the memory is positioned behind the disk drives when installed in a tower chassis. Drive bays or cables will make physical access to the TPM more difficult than if it was left out in the open portions of the motherboard.

14.4 Firmware Hub (FWH) Guidelines

The following sections provide general guidelines for compatibility and design when supporting the FWH device. The majority of the changes will be incorporated in the BIOS.

14.4.1 FWH and Flash BIOS Vendors

The following vendors manufacture firmware hubs that meet Intel requirements:

SST*:   http://www.ssti.com

STM*:   http://us.st.com/stonline

ATMEL*: http://www.atmel.com

Note: Contact the vendor directly for information on packaging and density.

14.4.2 FWH Decoupling

A 0.1 µF capacitor must be placed between the VCC supply pins and the VSS ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor must be placed between the VCC supply pins and the VSS ground pins to decouple low frequency noise. The capacitors must be placed no further than 390 mils from the VCC supply pins.

14.4.3 FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active-low. Therefore, the inactive state of the EP80579 INIT33V# signal needs to be at a slightly higher value than the V_{IH} min FWH INIT# pin specification. The EP80579 inactive state for this signal is typically governed by the following formula:

$$\text{I/O power well minimum} - \text{noise margin}$$

For example, if the minimum voltage in the I/O power well of the processor is 1.6V, the noise margin is 200 mV and the V_{IH} min spec of the FWH INIT# input signal is 1.35V, there would be no compatibility issue (because 1.6V − 0.2V = 1.40V, which is greater than the 1.35V minimum of the FWH). If the V_{IH} min of the FWH was 1.45V, there would be an incompatibility and logic translation (see Section 14.4.4) would need to be used.

Note: These examples do not take into account actual noise that may be encountered on INIT#. Care must be taken to ensure that the V_{IH} min specification is met with ample noise margin.

14.4.4 FWH V_{PP} Design Guidelines (Optional)

The V_{PP} pin on the FWH is used for programming the flash cells. The FWH supports V_{PP} of 3.3V or 12V. If V_{PP} is 12V, the flash cells will program about 50% faster than at 3.3V. However, the FWH only supports a V_{PP} of 12V for 80 hours (3.3V on Vpp does not affect

the life of the device). The V_{PP} of 12V would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V_{PP} pin must be connected to 3.3V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. To decrease programming time, it becomes necessary to apply 12V to the V_{PP} pin. The circuit in Figure 128 allows testers to put 12V on the V_{PP} pin while keeping this voltage separated from the 3.3V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3V on this pin during normal operation.

Figure 128. FWH VPP Isolation Circuitry
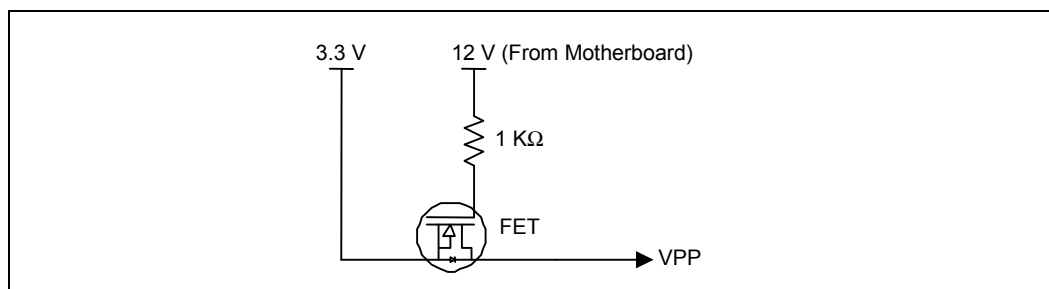
Note: This is an example only. See the specification for the FWH being used for more details.

15.0 Real Time Clock (RTC) Interface

15.1 RTC Interface

The EP80579 contains a Real Time Clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions:

- keeping the date and time
- storing system data in its RAM when the system is powered down

The RTC module uses a crystal circuit to generate a low-swing 32 KHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the EP80579, the RTCX1 signal is amplified to drive internal logic as well as generate a free-running, full-swing clock output for system use. This output signal of the EP80579 is called SUSCLK, as illustrated in Figure 129.

Figure 129. RTCX1 and SUSCLK Relationship in EP80579
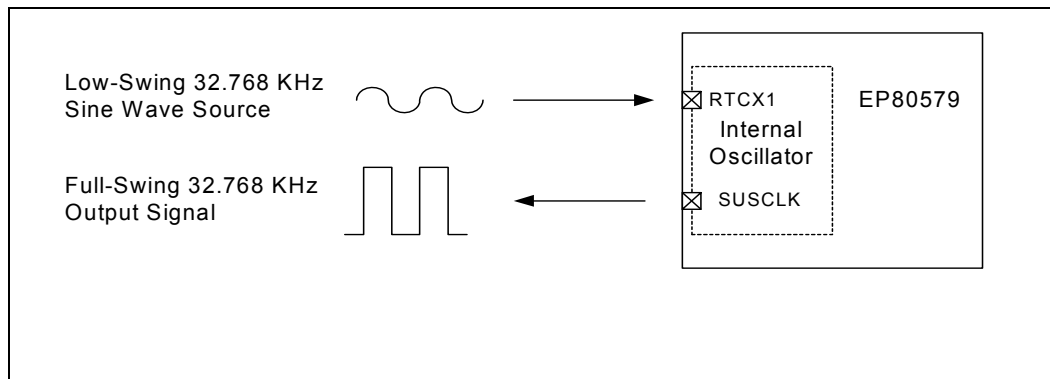
15.1.1 RTC Crystal

The RTC module requires an external oscillating source of 32.768 KHz connected to the RTCX1 and RTCX2 signals. Figure 130 shows the external circuitry that comprises the oscillator of the RTC:

Figure 130. External Circuitry for the RTC
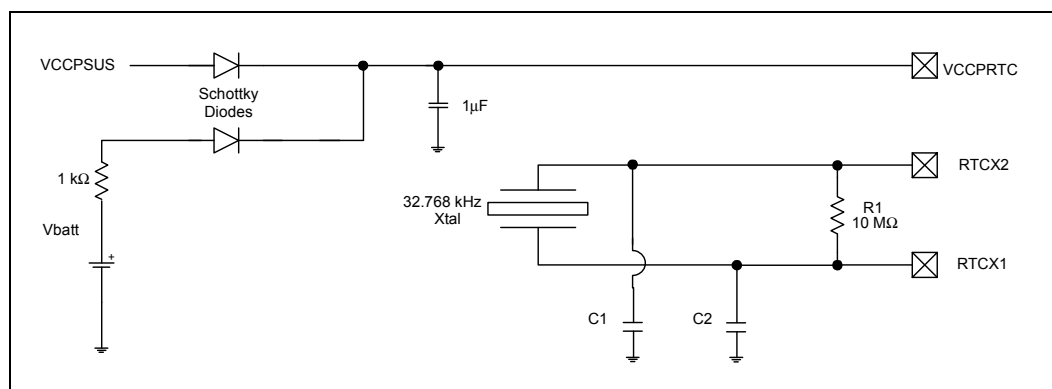
Notes:
1.   The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations.
     Typical values for C1 and C2 are 15 pF, based on crystal load of 12.5 pF.
2.   Reference designators are arbitrarily assigned.
3.   VCCPSUS is active whenever the system is plugged in.
4.   Vbatt is voltage provided by the battery.
5.   VCCPRTC, RTCX1, and RTCX2 are EP80579 pins.
6.   VCCPRTC powers the EP80579 RTC well.
7.   RTCX1 is the input to the internal oscillator.
8.   RTCX2 is the feedback for the external crystal.

Table 71.   RTC Routing Summary

Trace Impedance	RTC Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, C1, and C2 Tolerances	Signal Referencing
50 Ω ±10%	5 mil trace width (results in ~2 pF/in.)	1.2 in. (the total net length including caps is 1.5 inches)	N/A	R1 = 10 MΩ ±5% C1 = C2 = (NPO class) See Section 15.1.2 for calculating a specific capacitance value for C1 and C2	Ground

15.1.2   External Capacitors

To maintain the RTC accuracy, the external capacitor values C1 and C2 must be chosen to provide the manufacturer-specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})^2 (C_2 + C_{in2} + C_{trace2})] / [C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2}] + C_{parasitic}$$

where:

- C_{load} = crystal's load capacitance. This value can be obtained from the crystal specification.

- C_{in1}, C_{in2} = input capacitances at the RTCX1 and RTCX2 signals of EP80579. These values can be obtained from the *Intel® EP80579 Integrated Processor Product Line Datasheet*.

- C_{trace1}, C_{trace2} = trace length capacitances measured from the crystal terminals to the RTCX1 and RTCX2 signals. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mils wide trace and a ½ ounce copper pour, is approximately equal to:

C_{trace} = trace length • 2 pf per inch

- $C_{parasitic}$ = crystal's parasitic capacitance. This capacitance is created by the existence of two electrode plates and the dielectric constant of the crystal blank inside the crystal part. See the crystal's specification to obtain this value.

Ideally, C1 and C2 can be chosen such that C1 = C2. Using the equation of C_{load} above, the values of C1 and C2 can be calculated to give the best accuracy (closest to 32.768 KHz) of the RTC circuit at room temperature. However, C2 can be chosen such that C2 > C1, and then C1 can be trimmed to obtain the 32.768 KHz.

In certain conditions, both the C1 and C2 values can be shifted away from the theoretical values calculated from the above equation to obtain the closest oscillation frequency to 32.768 KHz. When C1 and C2 are smaller than the theoretical values, the RTC oscillation frequency will be higher.

The following example illustrates the use of practical values of C1 and C2 in the case that theoretical values cannot guarantee the accuracy of the RTC in a low temperature condition:

Example:

According to the required 12.5 pF load capacitance of a typical crystal that is used with EP80579, the calculated values of C1 = C2 is 15 pF at room temperature (25$^°$ C) yields a 32.768KHz oscillation.

At 0$^°$ C, the frequency stability of the crystal gives −23 ppm (assuming the circuit has 0 ppm at 25$^°$ C). This makes the RTC circuit oscillate at 32.767246 KHz instead of 32.768 KHz.

If the values of C1 and C2 are chosen as 6.8 pF instead of 10 pF, the RTC will oscillate at a higher frequency at room temperature (+23 ppm), but this configuration of C1 and C2 makes the circuit oscillate closer to 32.768 KHz at 0$^°$ C. The 6.8 pF value of C1 and C2 is the practical value.

Note: The temperature dependency of the crystal frequency is a parabolic relationship (ppm/degree squared). The effect of changing the crystal's frequency when operating at 0° C (25° C below room temperature) is the same when operating at 50° C (25° C above room temperature). See the crystal's datasheet for more details.

15.1.3 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires highly accurate oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. A trace length of less than 1 in. on each branch (from the crystal's terminal to the RTCXn signals) is recommended. Keep routing on the RTC circuit basic to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-406, a trace of 5 mils has approximately 2 pF per inch.

- Reduce trace signal coupling by avoiding routing of adjacent PCI signals close to RTCX1 and RTCX2.

- Use of a ground guard plane is highly recommended.

- The oscillator's Vcc must be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

15.1.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while EP80579 is not powered by the system.

Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 6 µA, the battery life will be at least:

$$170,000 \text{ µAh} / 6 \text{ µA} = 28,333 \text{ h} = 3.2 \text{ years}$$

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy may be obtained when the RTC voltage is in the range of 3.0V to 3.3V.

The battery must be connected to EP80579 via an isolation Schottky diode circuit. The Schottky diode circuit allows the RTC well to be powered by the battery when the system power is not available and the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 131 is an example of a diode circuit that is used.

Figure 131. A Schottky Diode Circuit to Connect RTC External Battery
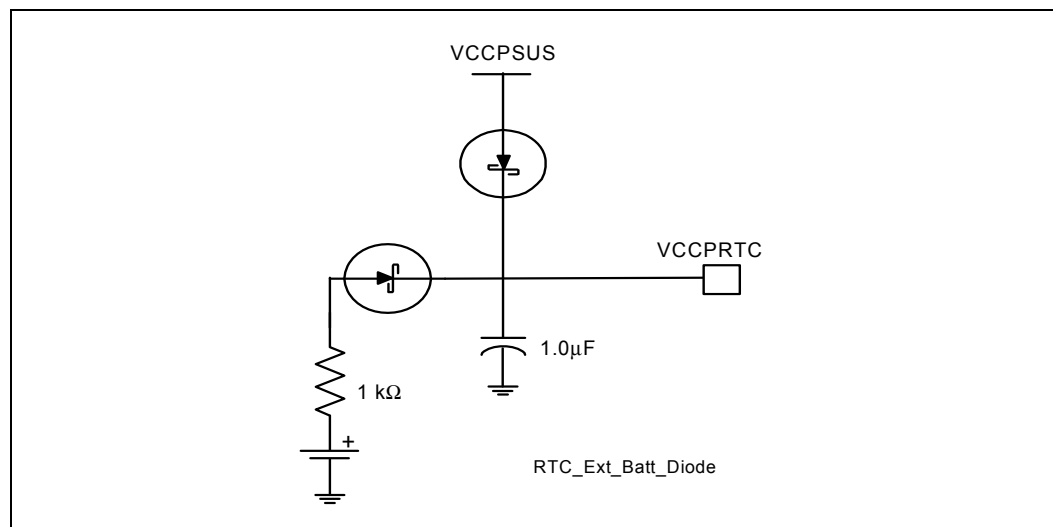
Use a standby power supply to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

15.1.5 Internal only RTC External RTEST# Circuit

Figure 132. RTEST# External Circuit for the RTC
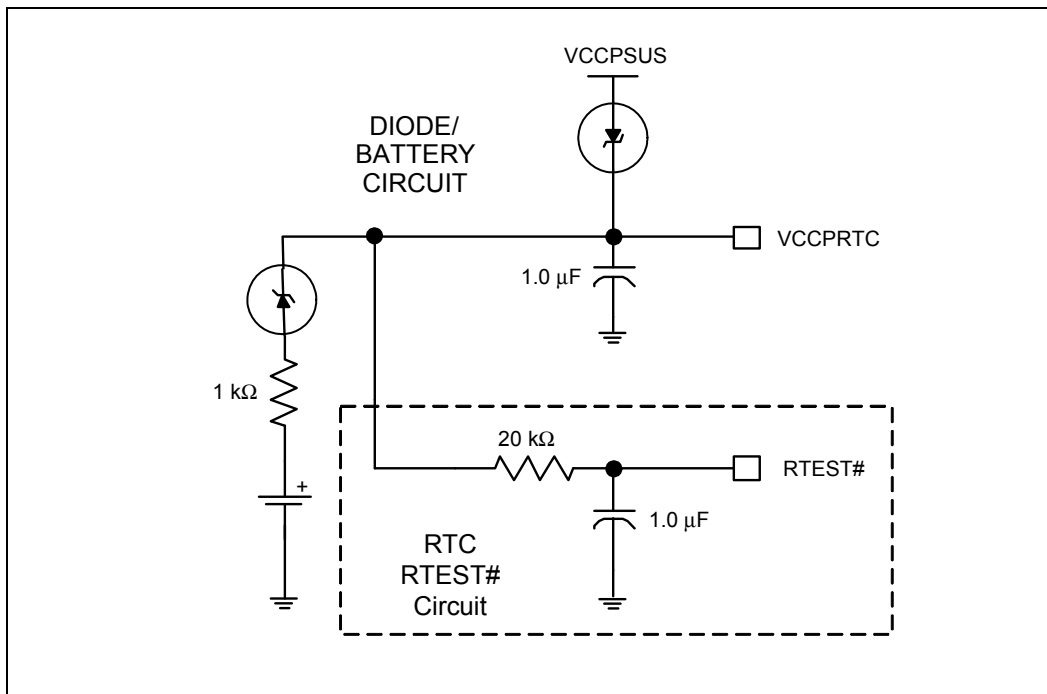
The RTC requires some additional external circuitry. The RTEST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTEST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTEST# will go high some time after the battery voltage is valid. The RC time delay must be in the range of 18–25 ms. When RTEST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1 and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

The RTEST# signal may also be used to detect a low battery voltage. RTEST# will be asserted during a power up from the G3 state if the battery voltage is below 2V. This will set the RTC_PWR_STS bit as described above. If desired, BIOS may request that the user replace the battery.

This RTEST# circuit is combined with the diode circuit (shown in Figure 131), whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 132 is an example of this circuitry that is used in conjunction with the external diode circuit.

15.1.6 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), the SUSCLK duty cycle can be between 30%–70%. If the SUSCLK duty cycle is beyond the 30%–70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using a normal probe (50 Ω input impedance probe) and is an appropriate signal to check the RTC frequency to determine the accuracy of the RTC Clock.

15.1.7   RTC Well Input Strap Requirements

All RTC-well inputs (RTEST#, INTRUDER#) recommend be either pulled up to VCCPRTC or pulled down to ground while in the G3 state. RTEST#, when configured as shown in Figure 132 meets this requirement. INTRUDER# recommend have a weak external pull-up to VCCPRTC. This will prevent these nodes from floating in the G3 state and correspondingly will prevent I_{CC}RTC leakage that can cause excessive coin-cell drain. It is recommended that the PWROK input signal also be configured with an external weak pull-down.

16.0 Synchronous Peripheral Interface (SPI)

The EP80579's Serial Peripheral Interface (SPI) is a 4-pin interface that provides a potentially lower-cost alternative for system flash versus the Firmware Hub on the LPC bus. The Serial Peripheral Interface is used to support only one SPI compatible flash device - only one chip select is available. The SPI flash device can be up to 16 MB (128 Mbits). The SPI interface operates at 20 MHz clock frequency. See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for additional SPI compatibility requirements.

Table 72. Serial Peripheral Interface Signal Description

Group	Signal Name	Description
Data	SPI_MOSI	SPI serial output data from EP80579 to SPI flash device
Data	SPI_MISO	SPI serial input data from the SPI Flash Device to EP80579
Clock	SPI_CLK	SPI Clock output from EP80579 to SPI Flash Device (20 MHz)
Chip Select	SPI_CS#	SPI chip select from EP80579 to SPI Flash Device **Note:** If SPI interface is used, pull-up with 10 K-ohm resistor for signal stabilty during power up.

16.1 Terminating Unused SPI Port

If the SPI port is not implemented on the system, terminate the signals as follows:

— SPI_MOSI - Leave as no connect (NC)

— SPI_MIS0 - Pull-up with a 10 K-ohm resistor

— SPI_CLK - Leave as no connect (NC)

— SPI_CS# - Leave as no connect (NC)

16.2 SPI Interface General Routing Guidelines

This section contains preliminary information and details for layout and routing guidelines for the SPI BIOS Flash interface. Also, see the Serial Flash vendor documentation for additional Serial Flash specific design considerations.

16.2.1 SPI Routing Guidelines

Figure 133. SPI Topology (System BIOS Only)
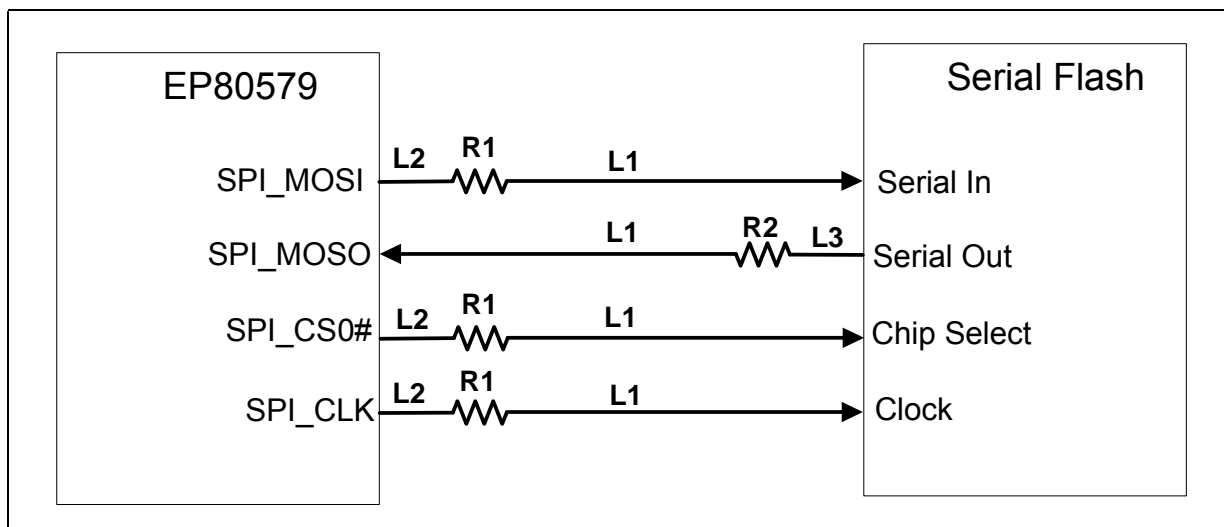
Table 73. SPI Single Flash Device Routing Summary

Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Length	Breakout	Figure	Notes
SPI_MOSI SPI_MISO SPI_CS0# SPI_CLK	50Ω ±10%	W = 4.5 mils S = 7 mils	Microstrip	L1 = 1"-11" L2 = 0.1"-0.5" L3 = 0.1"-0.5"	W = 4 mils S = 4 mils L = <1"	Figure 133	1, 2, 3
SPI_MOSI SPI_MISO SPI_CS0# SPI_CLK	50Ω ±10%	W = 3.75mils S = 7 mils	Stripline	L1 = 1"-11" L2 = 0.1"-0.5" L3 = 0.1"-0.5"	W = 4 mils S = 4 mils L = <1"	Figure 133	1,2,3

1. W represents width of signal; S represents spacing to any other signal.
2. R1 = 15Ω and should be placed 0.1-1" from the EP80579.
3. R2 = 15Ω and should be placed 0.1-1" from the serial flash device.

16.2.2 Boot BIOS Selection

GPIO[17] and GPIO[33] have internal 50 KΩ pull-ups which set the default bootup to the FWH. The SPI boot option is implemented by strapping GPIO[17] and GPIO[33] to ground (GND) through 1KΩ pull-down resistors. See Table 74 for strapping options.

Table 74.   Boot-up Strapping Options (Flash)

GPIO[17]	GPIO[33]	BIOS Bootup Option
0	0	Boot BIOS from SPI Flash
0	1	Reserved
1	0	Reserved
1	1	Boot BIOS from LPC FWH **(default)**

16.2.3   Serial Flash Vendors

The following vendors manufacture serial flash devices that conform to Intel's specific requirements. For additional details on the compatibility requirements for SPI devices see the *Intel® EP80579 Integrated Processor Product Line Datasheet*. Contact the flash vendor directly for information on packaging and density.

ATMEL: http://www.atmel.com/

INTEL: http://www.intel.com/design/flcomp/prodbref/s33.htm

MACRONIX: http://www.macronix.com/

PMC: http://www.pmcflash.com/

SST: http://www.ssti.com/

STM: http://us.st.com/stonline/

WINBOND: http://us.winbond-usa.com/

Note: OEMs must fully validate any SPI flash device to ensure compatibility with their platforms. This list should not be considered as a complete list of SPI vendors and is not an indication of Intel approved devices or vendors. Contact your preferred flash vendor directly to determine if they have a compatible device.
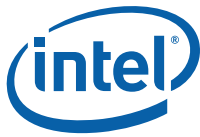
17.0 General Purpose I/O (GPIO) and Interrupt Interface

17.1 GPIO Signals

The EP80579 provides 36 general-purpose input/output (GPIO) pins for use in generating and capturing application-specific input and output signals. By design, each GPIO pin is hard-wired as input (GPI), output (GPO), or input/output (GPIO). Only the Input/Output (GPIO) pins can be re-programmed as an input or output. Some of the GPIO signals are multiplexed and can be reconfigured to provide alternate functionality, such as IOAPIC interrupts. All GPIO pins which are configured as IRQ inputs do not require any external pull-up resistors. Additionally, SIU_TXD2 (UART_TXD2) should be pulled-down with a 510 ohm resistor to enable the configuration of the GPIOs to function as IOAPIC Interrupts. When a GPIO pin is configured as an IOAPIC IRQ, the pin direction is automatically set as an input (I). Table 75 provides the functional definitions for the GPIO pins, Table 76 shows how the GPIOs are used in the Development Board and Table 77 shows how the GPIOs are used as external interrupt pins.

Table 75. GPIO Pin Definitions (Sheet 1 of 2)

Signal(s)	I/O Type (Default Mode)	Function (Default Mode)	Alternate Mode	Description
GPIO[1:0]	I	GPI	N/A	Unmultiplexed
GP2_PIRQE#	I	GPI	PIRQE#	GPIO[2] multiplexed with PIRQE#
GP3_PIRQF#	I	GPI	PIRQF#	GPIO[3] multiplexed with PIRQF#
GP4_PIRQG#	I	GPI	PIRQG#	GPIO[4] multiplexed with PIRQG#
GP5_PIRQH#	I	GPI	PIRQH#	GPIO[5] multiplexed with PIRQH#
GPIO[10:6]	I	GPI	N/A	Unmultiplexed
GP11_SMBALERT#	I	SMBALERT#	GPIO[11]	SMBALERT# multiplexed with GPIO[11]
GPIO[15:12]	I	GPI	N/A	Unmultiplexed
GPIO[16]	I/O	GPIO	IRQ24	Multiplexed with IOAPIC IRQ24
GPIO[17]	I/O	GPIO	IRQ25	Multiplexed with IOAPIC IRQ25
GPIO[18]	I/O	GPIO	IRQ36	Multiplexed with IOAPIC IRQ36
GPIO[19]	I/O	GPIO	IRQ37	Multiplexed with IOAPIC IRQ37
GPIO[20]	I/O	GPIO	IRQ26	Multiplexed with IOAPIC IRQ26
GPIO[21]	I/O	GPIO	IRQ27	Multiplexed with IOAPIC IRQ27
GPIO[23]	I/O	GPIO	IRQ28	Multiplexed with IOAPIC IRQ28
GPIO[24]	I/O	GPIO	IRQ29	Multiplexed with IOAPIC IRQ29
GPIO[25]	I/O	GPIO	IRQ38	Multiplexed with IOAPIC IRQ38
GP26_SATA0GP	I	GPI	SATA0GP	Multiplexed with SATA0GP

Table 75.   GPIO Pin Definitions (Sheet 2 of 2)

Signal(s)	I/O Type (Default Mode)	Function (Default Mode)	Alternate Mode	Description
GPIO[27]	I/O	GPIO	IRQ39	Multiplexed with IOAPIC IRQ39
GPIO[28]	I/O	GPIO	IRQ30	Multiplexed with IOAPIC IRQ30
GP29_SATA1GP	I	GPI	SATA1GP	Multiplexed with SATA1GP
GPIO[30]	I	GPI	IRQ31	Multiplexed with IOAPIC IRQ31.
GPIO[31]	I	GPI	IRQ32	Multiplexed with IOAPIC IRQ32.
GPIO[33]	I/O	GPIO	IRQ33	Multiplexed with IOAPIC IRQ33.
GPIO[34]	I/O	GPIO	IRQ34	Multiplexed with IOAPIC IRQ34.
GPIO[40]	I	GPI	IRQ35	Multiplexed with IOAPIC IRQ35.
GP41_LDRQ[1]#	I	LDRQ[1]#	GPIO[41]	LDRQ[1]# multiplexed with GPIO[41]
GPIO[48]	O	GPO	N/A	Unmultiplexed

17.1.1   Development Board GPIO Usage

The Development Board has all unused GPIO signals connected to headers. Some multiplexed GPIO signals may not be connected to the headers if they are used for alternate functions.

Table 76 provides a list of how the GPIO signals are used in the Development Board.

Table 76.   Development Board GPIO Usage (Sheet 1 of 2)

Pin Name	I/O (Default Mode)	Signal Name	Mode of Operation	Function
GPIO[0]	I	T_GPIO[0]	GPI	Header
GPIO[1]	I	T_GPIO[1]	GPI	Header
GP2_PIRQE_N	I	T_GPIO[2]	GPI	Header
GP3_PIRQF_N	I	T_GPIO[3]	GPI	Header
GP4_PIRQG_N	I	T_GPIO[4	GPI	Header
GP5_PIRQH_N	I	T_GPIO_5_FPGA_IN_5	GPI	FPGA_IN_5
GPIO[6]	I	T_GPIO_6_FPGA_IN_6	GPI	FPGA_IN_6
GPIO[7]	I	T_GPIO_7_FPGA_IN_7	GPI	FPGA_IN_7
GPIO[8]	I	T_GPI8_SLEEP_WAKE_N	GPI	Sleep Wake
GPIO[9]	I	T_GPIO_9_FPGA_IN_9	GPI	FPGA_IN_9
GPIO[10]	I	T_GPIO_10_FPGA_IN_10	GPI	FPGA_IN_10
SMBALERT_N	I	IMCH_SMBALERT_N	GPI	SMBus Alert
GPIO[12]	I	T_GPIO_12_FPGA_IN_12	GPI	FPGA_IN_12
GPIO[13]	I	T_GPIO_13_FPGA_IN_13	GPI	FPGA_IN_13
GPIO[14]	I	T_GPIO_14_FPGA_IN_14	GPI	FPGA_IN_14
GPIO[15]	I	T_GPIO_15_FPGA_IN_15	GPI	FPGA_IN_15
GP16_IRQ24	I	T_GPO16_HSS0_INT_N	IRQ24	HSS0_INT_N
GP17_IRQ25	I/O	T_GP017	GPIO	T_GP017_HSS1/SPI Boot Select

Table 76.   Development Board GPIO Usage (Sheet 2 of 2)

Pin Name	I/O (Default Mode)	Signal Name	Mode of Operation	Function
GP18_IRQ36	I	T_GPO18_HSS2_INT_N	IRQ36	HSS2_INT_N
GP19_IRQ37	I	T_GPO19_HSS1_INT_N	IRQ37	HSS1_INT_N
GP20_IRQ26	O	T_GPO20_SMB_C	GPO	SMBus_C Enable
GP21_IRQ27	O	T_GPO21_SMB_B	GPO	SMBus_B Enable
GP23_IRQ28	O	T_GPO23_SMB_A	GPO	SMBus_A Enable
GP24_IRQ29	I/O	T_GPIO24_FPGA_IO_0	GPIO	FPGA_I/O_0
GP25_IRQ38	I/O	T_GPIO25_FPGA_IO_1	GPIO	FPGA_I/O_1
GP26_SATA0GP	I	T_GPIO_26_FPGA_IN_11	GPIO	FPGA_IN_11
GP27_IRQ39	I/O	T_GPIO27_FPGA_IO_2	GPIO	FPGA_I/O_2
GP28_IRQ30	I/O	T_GPIO28_FPGA_IO_3	GPIO	FPGA_I/O_3
GP29_SATA1GP	I	T_GPIO_29_FPGA_IN_8	GPIO	FPGA_IN_8
GP30_IRQ31	I	IMCH_SLP_N	IRQ31	Sleep signal by External Jumper
GP31_IRQ32	I	T_GPI31	GPI	Header
GP33_IRQ33	I/O	T_GPIO33_FPGA_IO_4	GPIO	FPGA_I/O_4/SPI Boot Select
GP34_IRQ34	I/O	HPI_GPIO_34	GPIO	HSS1 EXT
GP40_IRQ35	I	IERR_GPI40	GPI	IERR Signal)
LDRQ[1]_N	I	L_DRQ1_N	GPI	LPC DMA Request
GPIO[48]	O	T_GPO_48_FPGA_OUT_5	GPO	FPGA_OUT_5

17.2   Interrupts

EP80579 provides support for up to four PCI interrupt pins (PIRQ[E:H]) and PCI 2.3 message-based interrupts. EP80579 also maintains support for ISA (legacy)-style interrupts via the serial interrupt protocol (SERIRQ). PCI Interrupts (PIRQ[A:D]) are not pinned out on EP80579, but supported via SERIRQ. When IOAPIC is active, IRQ[39:24] are externally driven interrupts through GPIO pins, enabled if SIU_TXD2 is pulled low on power-up.

Table 77 shows the mapping of the various interrupts when the IOAPIC is active.

Table 77.   Interrupt Configurations - APIC Mode (Sheet 1 of 2)

IRQ #	Interrupt Name	Source	Pin Name
16	PIRQA	SERIRQ	N/A
17	PIRQB	SERIRQ	N/A
18	PIRQC	SERIRQ	N/A
19	PIRQD	SERIRQ	N/A
20	PIRQE	External	PIRQE
21	PIRQF	External	PIRQF
22	PIRQG	External	PIRQG
23	PIRQH	External	PIRQH
24		External	GPIO[16]

Table 77.   Interrupt Configurations - APIC Mode (Sheet 2 of 2)

IRQ #	Interrupt Name	Source	Pin Name
25		External	GPIO[17]
26		External	GPIO[20]
27		External	GPIO[21]
28		External	GPIO[23]
29		External	GPIO[24]
30		External	GPIO[28]
31		External	GPIO[30]
32		External	GPIO[31]
33		External	GPIO[33]
34		External	GPIO[34]
35		External	GPIO[40]
36		External	GPIO[18]
37		External	GPIO[19]
38		External	GPIO[25]
39		External	GPIO[27]

18.0   Serial Interface Unit (SIU/UART)

18.1   SIU (UART) Interface

The EP80579 provides two asynchronous Serial I/O Unit (SIU/UART) ports. These SIUs are 16550-compliant with 16-byte transmit and receive buffers.

Both SIUs are full-function and can be used for debug purposes or connected to an external modem. The ports have programmable Baud Rate generators. The maximum baud rate supported by the SIUs is 115 Kbps. The SIUs can be connected point-to-point. To ensure proper implementation, see the individual device design guide for the peripheral to be connected.

18.1.1   SIU Interface Signals

Table 78.   SIU Interface Signals (Sheet 1 of 2)

Signal Name	I/O Direction	Description
UART_CLK	I	48 MHz input clock to the SIU: This clock is passed to the baud clock generation logic of each UART in the SIU. **Note:** • UART_CLK must be connected even when the ports are not used.
SIU_RXD[2:1]	I/O	SERIAL INPUT for UART1 and UART2: Serial data input from device pin to the receive port. **Note:** • Must be pulled high through a 10 KΩ resistor when the port is not connected to an interfacing device
SIU_TXD[2:1]	I/O	SERIAL OUTPUT for UART1 and UART2: Serial data output to the communication peripheral/modem or data set. Upon reset, the TXD pins are set to MARKING condition (logic 1). **Note:** • Can be left as NC when the port is not connected to an interfacing device
SIU_CTS[2:1]#	I/O	CLEAR TO SEND for UART1 and UART2: [Active low]. This pin indicates that data can be exchanged between EP80579 and the external interface. These pins have no effect on the transmitter. These pins could be used as Modem Status Input whose condition can be tested by the processor. **Note:** • Must be pulled high through a 10 KΩ resistor when the port is not connected to an interfacing device
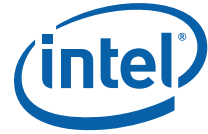
Table 78. **SIU Interface Signals (Sheet 2 of 2)**

Signal Name	I/O Direction	Description
SIU_DSR[2:1]#	I/O	DATA SET READY for UART1 and UART2: [Active low]. This pin indicates that the external agent is ready to communicate with UART. These pins have no effect on the transmitter. These pins could be used as Modem Status Input whose condition can be tested by the processor. ***Note:*** • Must be pulled high through a 10 KΩ resistor when the port is not connected to an interfacing device
SIU_DCD[2:1]#	I/O	DATA CARRIER DETECT for UART1 and UART2: [Active low]. This pin indicates that data carrier has been detected by the external agent. These pins are Modem Status Input whose condition can be tested by the processor. ***Note:*** • Must be pulled high through a 10 KΩ resistor when the port is not connected to an interfacing device
SIU_RI[2:1]#	I/O	RING INDICATOR for UART1 and UART2: [Active low]. This pin indicates that a telephone ringing signal has been received by the external agent. These pins are Modem Status Input whose condition can be tested by the processor. ***Note:*** • Must be pulled high through a 10 KΩ resistor when the port is not connected to an interfacing device
SIU_DTR[2:1]#	I/O	DATA TERMINAL READY for UART1 and UART2: When low these pins informs the modem or data set that UART 1, 2 are ready to establish a communication link. The DTR#x(x=0,1) output signals can be set to an active low by programming the DTRx (x-0,1) (bit0) of the Modem control register to a logic 1. A Reset operation sets this signal to its inactive state (logic 1). LOOP mode operation holds this signal in its inactive state. ***Note:*** • Can be left as NC when the port is not connected to an interfacing device
SIU_RTS[2:1]#	I/O	REQUEST TO SEND for UART1 and UART2: When low these pins informs the modem or data set that UART 1, 2 are ready to establish a communication link. The RTS#x(x=0,1) output signals can be set to an active low by programming the RTSx (x-0,1) (bit1) of the Modem control register to a logic 1. A Reset operation sets this signal to its inactive state (logic 1). LOOP mode operation holds this signal in its inactive state. ***Note:*** • Can be left as NC when the port is not connected to an interfacing device

18.1.2   SIU Interface Interconnect

The High-Speed SIU interface can be configured to support speeds from 300 baud to 115 Kbaud. This interface supports five, six, seven, or eight data bit transfers, one or two stop bits, as well as even-, odd-, or no-parity configurations.

Figure 134 illustrates how the SIU signals are connected to the RS-232 transceiver. This RS-232 transceiver has five transmit and three receive signals to handle all modem control signals. To ensure proper implementation, see the transceiver component design guide for the Transceiver-to-DB9 Connector interface filter requirements.

Figure 134. SIU Interface Interconnect
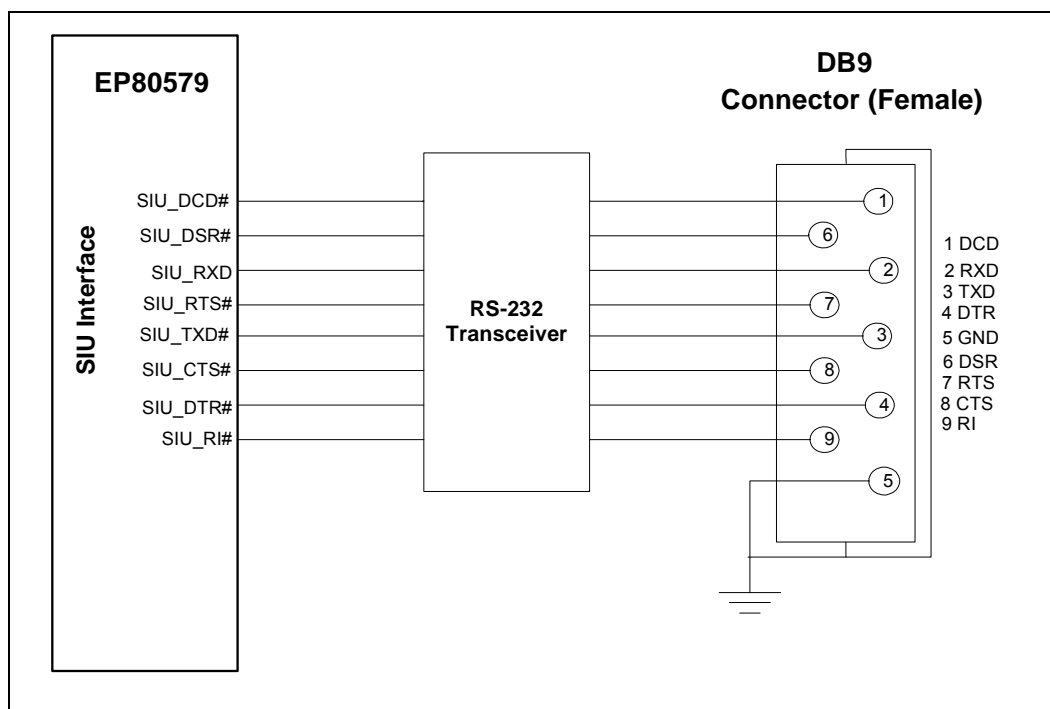
19.0 Gigabit Ethernet (GbE) Interface

The EP80579 Gigabit Ethernet Media Access Controller (GbE MAC) is based on Intel's fourth generation gigabit MAC. The GbE MAC provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications. The controller is capable of transmitting and receiving data rates of 10/100/1000 Mbps.

Through the GbE MAC interface, EP80579 can be connected to an external PHY, which can support Reduced Ethernet (RMII) and Reduced GMII (RGMII).

The GbE MAC includes a single Management Data Interface (MDI)- Management Data Input/Output (MDIO) and Management Data Clock (MDC). The single Management Data Interface is used to communicate, control, and configure the PHY devices interfacing to the GbE ports.

Finally, each GbE MAC is capable of self-configuration via an optional, external serial EEPROM. A single EEPROM is used for all the GbE MACs.

Note: The EP80579 can support both 3.3V and 2.5V PHY for the GbE interface. The media outputs will use 2.5V drivers that are 3.3V-tolerant. This is a violation of the RMII specification, which calls for TTL level outputs (not LVTTL) and 5V input level tolerance. We expect all major PHY devices that may be used in a EP80579 system will drive a maximum voltage of 3.3V.

RGMII version 1.3 is specified as a 2.5V CMOS level I/O interface and as such, EP80579 is fully compliant. RGMII version 2.0 is specified as a 1.5V HSTL I/O interface and the EP80579 is **NOT** compliant with this standard. All PHY devices that the EP80579 may be used with are expected to support RGMII version 1.3 standard. The MDIO, MDC, and serial EEPROM bus will be implemented with 2.5V I/O drivers.

19.1 GbE MAC/LAN Interface Interconnect

The GbE MAC connects to an external LAN component to provide the GbE LAN capabilities. The GbE MAC bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers IA-32 core utilization by offloading communication tasks from the IA-32 core.

The GbE MAC supports several PHY components, depending on the target market. This chapter's design guidelines are provided using the Marvell* GbE Transceivers (e.g., Marvell Alaska Quad* 88E1141/88E1145 (Quad-Port) Transceiver) as the LAN PHY component. Figure 135 and Figure 137 provide the interface interconnect between the EP80579 GbE MAC and the LAN PHY component.

Note: **Intel recommends that you consult the EP80579 Software Documents in the "Technical Documents" section at the Intel website (**http://www.intel.com/go/soc**) to determine if the Ethernet Physical Layer device (PHY) you intend to use in your design has software driver support. Utilyzing Physical Layer devices already supported by the software driver set will alleviate additional code for PHY configuration and management**.

19.2 GbE MAC Interface Guidelines

The GbE design guidelines provided in this chapter apply only to the interface between the GbE MAC interface and the LAN PHY component. See the LAN component's documentation for design guidelines, magnetics module and the Physical Interface Connector (See Figure 135).

Figure 135. GbE Controller/LAN Interface Interconnect
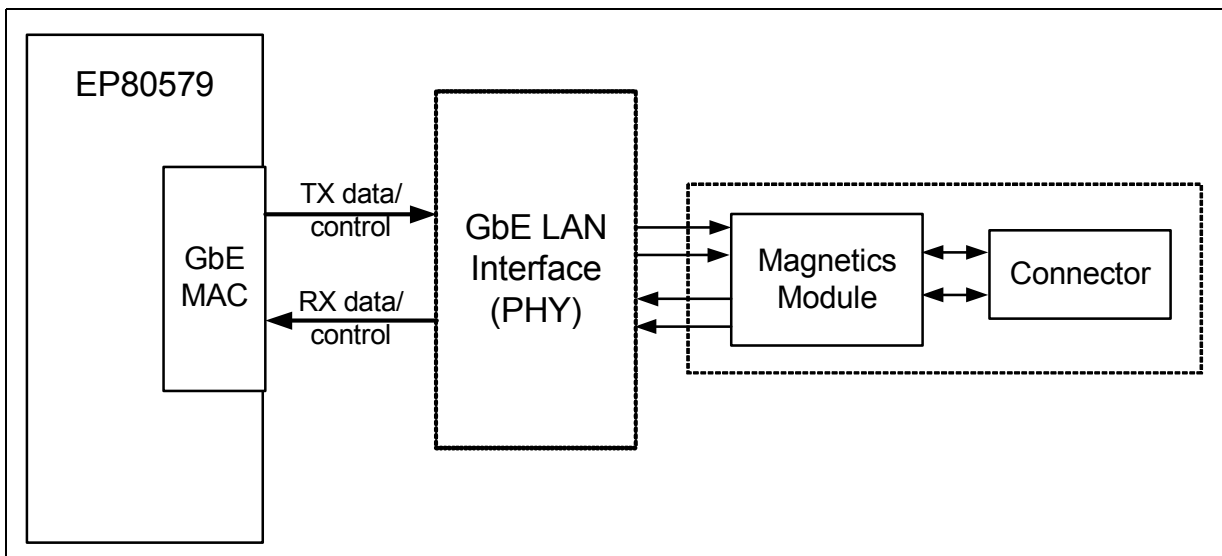
19.3 Frequency Requirements

Table 79 provides the frequency of all input clocks in the different modes of operation:

Table 79. Frequencies of All Input Clocks

Model	Clock Name	Frequency
RMII	GBE_REFCLK	50 MHz ± 50 ppm
	GBE_REFCLK_RMII	50 MHz ± 50 ppm
RGMII	GBEn_RxCLK	2.5/25/125 MHz
	GBE_REFCLK	125 MHz± 50 ppm

19.4 Gigabit Ethernet Interface Signals

GbE Port0 supports Wake-On-LAN (WOL) hence the GbE Port0 block resides in the Sustain Voltage rail within EP80579. It is required that all GbE Port0 (Transmit/Receive) interface signals on the platform be powered with GbE Standby Voltage. GbE Port 1&2 signals are to be powered with the GbE core power voltages.

Table 80.   GBEn Pin Table (Sheet 1 of 4)

GBEn Signal Name	Pin Type	Pin Count	Description
Note:			
• GBE Port 0 supports Wake-On-LAN (WOL); hence GBE Port 0 Block resides in the Sustain Power Well within EP80579. It is required that all GBE Port 0 (Transmit/Receive) interface signals on the platform be powered by GBE Standby Voltage. GBE Port 1&2 should be powered by GBE core power.			

GBEn_TxCLK	O	1	**RGMII Mode of Operation:**
			• The signal name is GBEn_TxCLK.
			• This signal is the transmit reference clock and will be 125 MHz, 25 MHz, or 2.5 MHz +- 50ppm depending on speed. GBEn_TxCLK is connected to the PHY GTXn_CLK input
			  — 125 MHz when operating at 1000Base-X speeds
			  — 25 MHz when operating at 100Base-X speeds
			  — 2.5 MHz when operating at 10Base-X speeds
			• Pull up GBE Port 0 Transmit Clock signal to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistor.
			• Pull up GBE Port 1&2 Transmit Clock signals to GBE 2.5V using a 1.2KΩ ± 5% resistors.
			• Leave signals of any unused Port as no connect.

	N/A	N/A	**RMII Mode of Operation:** • Not used in RMII mode of operation and is a no connect.
GBEn_TxCTL	O	1	**RGMII Mode of Operation:** • The signal name is GBEn_TXEN when the interface is configured to operate in RGMII mode of operation. • GBEn_TXEN indicates that the MAC has valid data being transmitted on the GBEn_TXDATA[3:0] signals. GBEn_TXEN shall be asserted synchronously with the first nibble of the preamble and shall remain asserted until all data bits are presented on the GBEn_TXDATA[3:0] signals. GBEn_TXEN shall be negated prior to the first GBEn_REFCLK rising edge following the final nibble of a frame. GBEn_TXEN shall transition synchronously with respect to GBEn_REFCLK. • Pull up GBE Port 0 Transmit Control signal to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistor. • Pull up GBE Port 1&2 Transmit Control signals to GBE 2.5V using a 1.2KΩ ± 5% resistors. • Leave signals of any unused Port as no connect.
	O	1	**RMII Mode of Operation:** • The signal name is GBEn_TXEN when the interface is configured to operate in RMII mode of operation. • GBEn_TXEN indicates that the MAC has valid data being transmitted on the GBEn_TXDATA[1:0] signals. GBEn_TXEN shall be asserted synchronously with the first two bits of the preamble and shall remain asserted until all data bits are presented on the GBEn_TXDATA[1:0] signals. GBEn_TXEN shall be negated prior to the first GBEn_REFCLK rising edge following the final two bits of a frame. GBEn_TXEN shall transition synchronously with respect to GBEn_REFCLK. • Pull up GBE Port 0 Transmit Control signal to EP80579 3.3V Standby Voltage (VCCGBEPSUS) using a 1.2KΩ ± 5% resistor. • Pull up GBE Port 1&2 Transmit Control signals to GBE 3.3V using a 1.2KΩ ± 5% resistors. • Leave signals of any unused Port as no connect.

Table 80.   GBEn Pin Table (Sheet 2 of 4)

GBEn Signal Name	Pin Type	Pin Count	Description
GBEn_TxDATA[3:0]	O	4	**RGMII Mode of Operation** • GBEn_TxDATA[3:0] signal name is GBEn_TxDATA[3:0] on the rising edge of GBEn_TxCLK when GBEn_TxCTL is active • GBEn_TxDATA[3:0] signal name is GBEn_TxDATA[7:4] on the falling edge of GBEn_TxCLK when GBEn_TxCTL is active. • Pull up GBE Port 0 Receive Data signals to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistors. • Pull up GBE Port 1&2 Receive Data signals to GBE 2.5V using a 1.2KΩ ± 5% resistors. • Leave signals of any unused Port as no connect.
	O	2	**RMII Mode of Operation:** • GBEn_TxDATA[1:0] signal name is GBEn_ TxDATA[1:0] on the rising edge of the 50 MHz GBEn_REFCLK when GBEn_TxCTL is active. • Pull up GBE Port 0 Receive Data signals to EP80579 3.3V Standby Voltage (VCCGBEPSUS) using a 1.2KΩ ± 5% resistors. • Pull up GBE Port 1&2 Receive Data signals to GBE 3.3V using a 1.2KΩ ± 5% resistors. • Leave signals of any unused Port as no connect

GBEn_RxCLK	I	1	**RGMII Mode of Operation:**
			• The signal name is GBEn_RxCLK.
			• This signal is the continuous receive clock and will be 125 MHz, 25 MHz, or 2.5 MHz +- 50ppm depending on data link speed. This clock shall be derived at the PHY and supplied by the PHY to the MAC from the received data stream.
			  — 125 MHz when operating at 1000Base-X speeds
			  — 25 MHz when operating at 100Base-X speeds
			  — 2.5 MHz when operating at 10Base-X speeds
			• Pull up GBE Port 0 Receive Clock signal to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistor.
			• Pull up GBE Port 1&2 Receive Clock signals to GBE 2.5V using a 1.2KΩ ± 5% resistors.
			• Pull-down all unused Receive Clock signals to GND using 10 KΩ resistors

	I	1	**RMII Mode of Operation:** • GBEn_RxCLK should be connected to GND with a 10 KΩ pull-down resistor when the interface is configured in this mode.

Table 80.   GBEn Pin Table (Sheet 3 of 4)

GBEn Signal Name	Pin Type	Pin Count	Description
GBEn_RxCTL	I	1	**RGMII Mode of Operation:** • The signal name is GBEn_RxCTL and connected to the PHY RX_DV when operating in RGMII mode of operation. • GBEn_RxCTL (PHY RX_DV) is driven by the PHY to indicate that the PHY is presenting recovered and decoded data on the GBEn_RXDATA[3:0] bundle. GBEn_RxCTL transitions synchronously with respect to the GBEn_RxCLK. GBEn_RxCTL shall be asserted continuously from the first recovered nibble of the frame through the final recovered nibble and shall be negated prior to the first rising edge of GBEn_RxCLK that follows the final nibble. In order for a received frame to be correctly interpreted by the MAC and the MAC sublayer, GBEn_RxCTL must encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End-of-Frame delimiter. • Pull up GBE Port 0 Receive Control signal to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistor. • Pull up GBE Port 1&2 Receive Control signals to GBE 2.5V using a 1.2KΩ ± 5% resistors. • Pull-down all unused Receive Control signals to GND using 10 KΩ resistors.
	I	1	**RMII Mode of Operation:** • The signal name is GBEn_RxCTL and connected to the PHY CRS_DV when operating in RMII mode of operation. • GBEn_RxCTL (PHY CRS_DV) shall be asserted by the PHY when the receive medium is non-idle. Loss of carrier shall result in the deassertion of GBEn_RxCTL synchronous to the cycle of REF_CLK which presents the first two-bits of a nibble onto GBEn_RxDATA[1:0] (i.e. GBEn_RxCTL is deasserted only on nibble boundaries). During a false carrier event, GBEn_RxCTL shall remain asserted for the duration of carrier activity. The data on GBEn_RxDATA[1:0] is considered valid once GBEn_RxCTL is asserted. However, since the assertion of GBEn_RxCTL is asynchronous relative to REFCLK, the data on GBEn_RxDATA[1:0] shall be "00" until proper receive signal decoding takes place. • Pull up GBE Port 0 Receive Control signal to EP80579 3.3V Standby Voltage (VCCGBEPSUS) using a 1.2KΩ ± 5% resistor. • Pull up GBE Port 1&2 Receive Control signals to GBE 3.3V using a 1.2KΩ ± 5% resistors. • Pull-down all unused Receive Control signals to GND using 10 KΩ resistors.

Table 80.   GBEn Pin Table (Sheet 4 of 4)

GBEn Signal Name	Pin Type	Pin Count	Description
GBEn_RxDATA[3:0]	I	4	**RGMII Mode of Operation at 1000Base-X-speeds** • GBEn_RxDATA[3:0] signal name is GBEn_RxDATA[3:0] on the rising edge of GBEn_RxCLK when GBEn_RxCTL is active • GBEn_RxDATA[3:0] signal name is GBEn_RxDATA[7:4] on the falling edge of GBEn_RxCLK when GBEn_RxCTL is active • Pull up GBE Port 0 Receive Data signals to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistors. • Pull up GBE Port 1&2 Receive Data signals to GBE 2.5V using a 1.2KΩ ± 5% resistors. • Pull-down all unused Receive Data signals to GND using 10 KΩ resistors
	I	4	**RMII Mode of Operation:** • The signal names GBEn_RxDATA[1:0] are mapped to PHY_RxDATA[1:0] when the interface is configured to operate in RMII mode of operation. • GBEn_RxDATA[1:0] is valid on the rising edge of GBE_REFCLK on every clock where GBEn_RxCTL is asserted, When GBEn_RxCTL is de-asserted, GBEn_RxDATA[1:0] being equal to "00" indicates the interface is idle. • GBEn_RXDATA[3] signal is connected to PHY RX_ERR when operating in RMII mode of operation. • PHY RX_ERR (Receive Error) is driven by the PHY and asserted for one or more GBE_REFCLK periods to indicate to the MAC that an error (e.g., a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY to the MAC. PHY RX_ERR shall transition synchronously with respect to GBE_REFCLK. While GBEn_RxCTL is de-asserted, PHY RX_ERR shall have no effect on the MAC. • Pull up GBE Port 0 Receive Data signals to EP80579 3.3V Standby Voltage (VCCGBEPSUS) using a 1.2KΩ ± 5% resistors. • Pull up GBE Port 1&2 Receive Data signals to GBE 3.3V using a 1.2KΩ ± 5% resistors. • Pull-down all unused Receive Data signals to GND using 10 KΩ resistors
GBE_REFCLK	I	1	**RGMII Mode of Operation:** • GBE_REFCLK is a continuous clock used for internal operation of the interface when configured in RGMII mode of operation and the interface is operating at 1000 Mb/s. This clock can be sourced from either an external clock or from the PHY. This clock is used to produce the GBEn_TxCLK clock. • The GBE_REFCLK frequency is nominally 125 MHz ± 50 ppm in this mode of operation.
	I	1	**RMII Mode of Operation:** • GBE_REFCLK is a continuous clock used for the internal operation of the interface when configured in RMII mode of operation. This clock is sourced external to both the EP80579 MAC and PHY. • The GBE_REFCLK frequency is nominally 50 MHz ± 50 ppm in this mode of operation.
GBE_REFCLK_RMII	I	1	**RGMII Mode of Operation:** • GBE_REFCLK_RMII is unused and connected via a 100Ω +/- 1% tolerance resistor to ground when the interface is configured in RGMII mode of operation.
	I	1	**RMII Mode of Operation:** • GBE_REFCLK_RMII is connected to the same clock source as the GBE_REFCLK when the interface is configured in RMII mode of operation. • The GBE_REFCLK/GBE_REFCLK_RMII frequency is nominally 50 MHz ± 50 ppm in this mode of operation.
GbE RCOMP[P/N]	I/O	2	• Signal used to control Gigabit Ethernet (RMII/RGMII mode) drive strength characteristics. Drive strength is varied on GbE Ethernet signals depending upon temperature. • GbE RCOMPP requires 50Ω +/- 1% tolerance resistor to ground. • GbE RCOMPN requires 50Ω +/- 1% tolerance resistor to EP80579 GbE 2.5V Standby Voltage (VCCSUS25).

Table 81. **GbE MAC Management Data Interface Signals**

Name	Input/ Output	Pull Up/ Down	Recommendations
MDIO	IO	Yes	• Management Data Input/Output. • Pull-up signal to EP80579 GbE 2.5V Standby (VCCSUS25) using a 1.5 KΩ ± 5% resistor. **Note:** • Must be pulled high through a 10 KΩ resistor to EP80579 GbE 2.5V Standby (VCCSUS25) the interface is not used.
MDC	O	No	• Management Data Clock. • Provide termination if signal is connected to multiple receivers • Resides in GbE Standby Power Well **Note:** • Can be left as no connect if the interface is not used.

Table 82. **GbE MAC Serial EEPROM Interface Signals**

Name	Input/ Output	Pull Up/ Down	Recommendations
EEDO	I	Yes	• EEPROM Output Data. Data from EEPROM to EP80579 • An external **pull-up** resistor of 4.7 KΩ is required. • Resides in GbE Standby Power Well.
EEDI	O	Yes	• EEPROM Input Data. Data from EP80579 to EEPROM • **Requires a 20KΩ pull-up resistor to GbE Standby Power, if GbE Standby power is generated on the platform; otherwise pull-down with 4.7 KΩ**
EECS	O	Yes	• EEPROM Chip Select. Used to enable EEPROM device • An external **pull-down** resistor of 4.7 KΩ is required. • Resides in GbE Standby Power Well.
EESK	O	Yes	• EEPROM Shift Clock. Clock for the EEPROM Interface (~ 1 MHz) • An external **pull-down** resistor of 4.7 KΩ is required. • Resides in GbE Standby Power Well.

19.5 GbE Interface - LAN Connect Interface Guidelines

The following sections contain guidelines on implementing a platform LAN connect device on a system motherboard. These sections should treated as a guideline and not as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings.

19.5.1 GbE Ethernet Interface — RGMII Mode

This section describes the GbE Ethernet reference clock transmit and receive timings when operating in RGMII mode. RGMII works in source synchronous mode, where transmit and receive data are synchronized with respect to TxCLK and RxCLK. In RGMII mode, TxCLK and RxCLK run at 2.5/25/125 MHz. In 2.5/25 MHz mode, both transmission and receive occurs on rising edges of the clock. At 125 MHz, data transfer (both Tx and Rx) occurs on both edges of the clock.

The RGMII interface gets Rx clock from the PHY and Tx clock from the MAC. The PHY receives a 25 MHz reference clock from the board, and the PHY sources the 125 MHz reference clock to the MAC. The RGMII outputs use 2.5V drivers that are 3.3V-tolerant. Figure 136 shows the GbE block diagram with the signal connections in RGMII mode:

Figure 136. GbE RGMII Mode Signal Connection Block Diagram
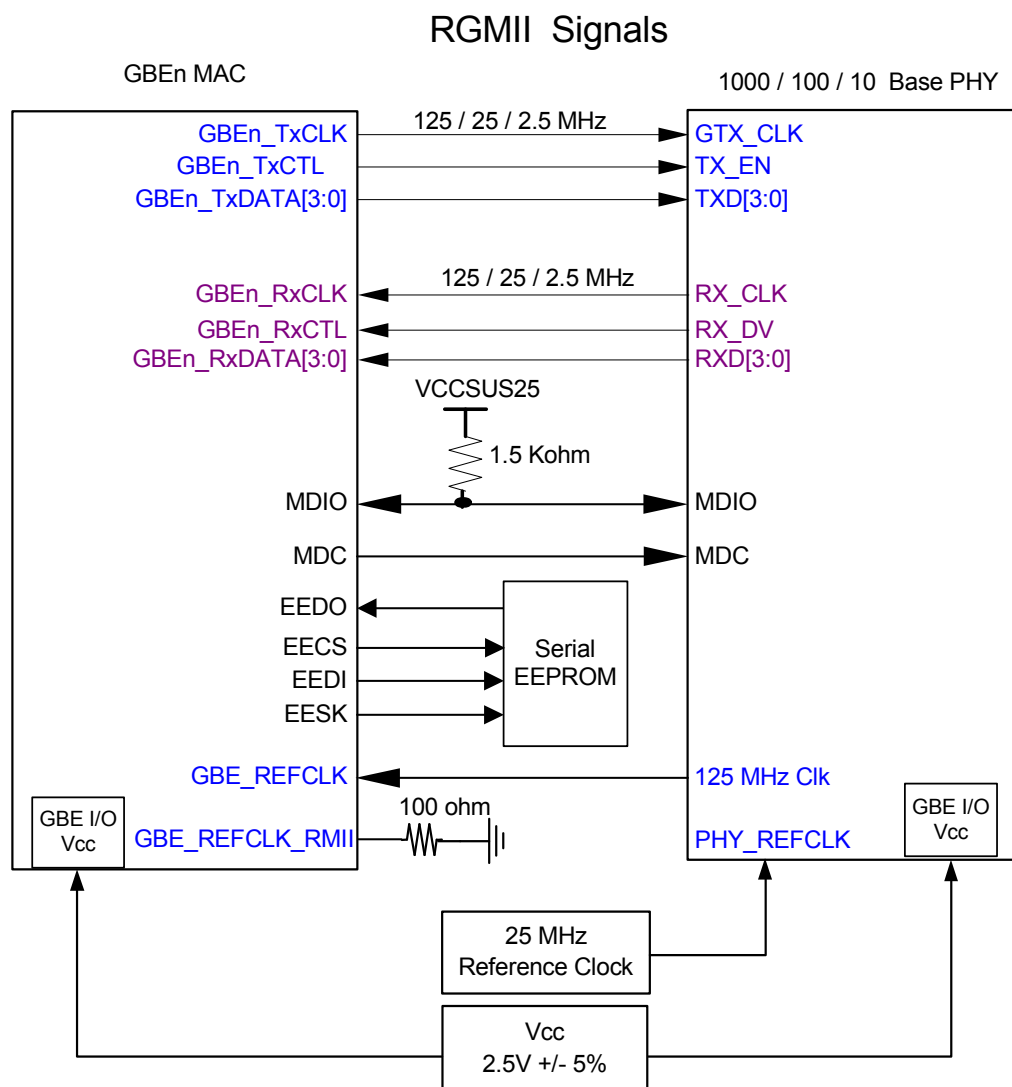
19.5.2 GbE Ethernet Interface — RMII Mode

This section describes the GbE interface when the interconnect is designed for a RMII interface.

In RMII mode, data is transmitted and received (TXDATA and RXDATA) with respect to the MAC and PHY reference clock inputs, which in 10/100 Base T is 50 MHz.

Figure 137 shows the GbE signal connections used in RMII mode for 10/100 Base connections. A 50 MHz external clock sources both the MAC and PHY reference clocks.

Figure 137. GbE RMII Mode Signal Connection Block Diagram
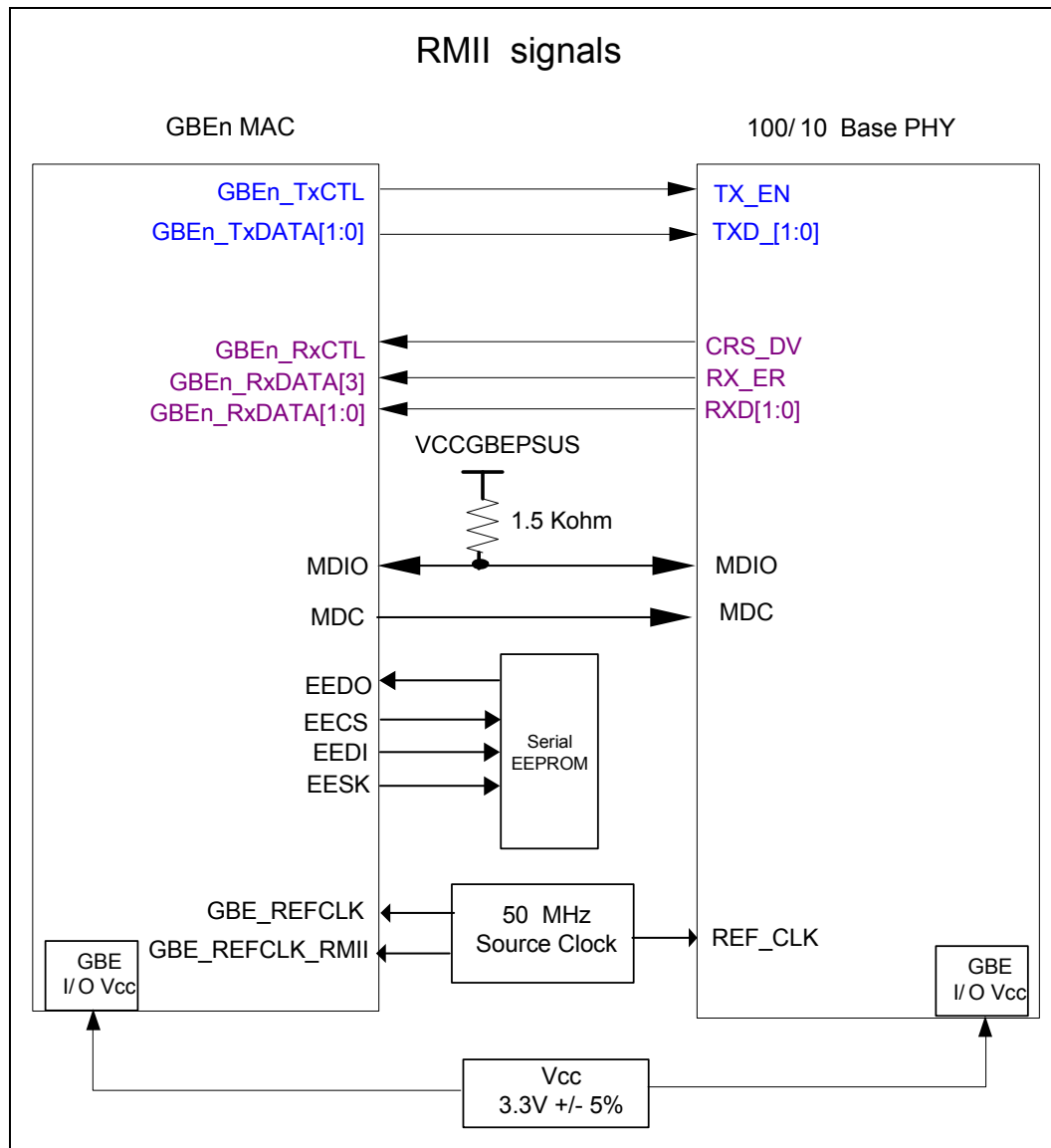
19.6 GbE Transmit and Receive Topology

19.6.1 GbE Transmit Topology

19.6.1.1 GbE Transmit Clock Topology

Figure 138 shows the routing topology of the GbE Transmit clock. The transmit clock topology is for the routing of GbEn_TxCLK (RGMII) or GbEn_CLK (RMII). The routing guidelines for the Transmit Data and Transmit Control signals in section Section 19.6.1.2 are referenced to the to the Transmit clock. Table 83 provides routing guidelines for the Transmit Clock signals.

Figure 138. GbE RGMII Transmit Path Clock Topology

RGMII Transmit Path Clock Topology
(EP80579 → PHY)

LCLK_Total_tx = LCLK_Brk_out_tx + LCLK_Brd_route_tx + LCLK_Brk_in_tx

NOTE: Breakout\ Breakin descriptions are as follows:

1. Routing where trace is 3.75 mil wide and 4mil spacing is implemented to escape\ enter BGA
2. The Breakout \ Breakin Length is defined from the pin of the BGA, to where 4 mil spacing increases to the required spacing per SI recommendations.
   a). Clock = 20 mil edge-to-edge (e2e) for Stripline
   b). Clock = 25 mil edge-to-edge (e2e) for Microstrip

Table 83. **GbE RGMII Transmit Path Clock Routing Guidelines**

Parameter	Routing Constraints	
Routing Layer	**Stripline**	**Microstrip**
Reference Plane	Ground Reference	
Board Trace Impedance	55 Ω	55 Ω
Trace Width	3.75mils (L3/L8)	4.5mils (L1/L10)
Clock Spacing (e2e)	20 mils (min)	25 mils (min)
EP80579 Clock Tx Breakout Length (LClk_Brk_out_tx)	0.5 inch (max)	0.5 inch (max)
Clock Tx Board Length (LClk_Brd_route_tx)	min =1.0 inch max = 7.0 inch	min =1.5 inch max = 8.0 inch
PHY Clock Tx Breakin Length (LClk_Brk_in_tx)	0.3 inch (max)	0.3 inch (max)
Total Tx Clock Routing (LClk_total_tx)	min =1.0 inch max = 7.8 inch	min =1.5 inch max = 7.8 inch
Pull Up Resistor T-Line (Lpull_up)	0.4 inch (max)	0.4 inch (max)
Pull Up Resistor (Rpull_up)	1.2 KΩ (5%)	1.2 KΩ (5%)
Breakout\Breakin Spacing (e2e)	4 mils (min)	4 mils (min)

19.6.1.2 GbE Transmit Data\Control Topology

The transmit Data and control signals included in the GbE transmit path topology shown in Figure 139 are:

— GBEn_TXDATA[3:0]

— GBEn_TXCTL

All the transmit path Data and Control signals in a channel (see Figure 139) should be length matched, routed on the same layer, and referenced to the Transmit Clock in section Section 19.6.1.1. The transmit data and control signals do not need to be length matched between channels, only within a channel. Table 84 provides routing guidelines for the Transmit Data and Control signals.

Figure 139. GbE RGMII Transmit Path Data\Control Topology

RGMII Transmit Path Data\Control Topology
(EP80579 ⟶ PHY)

L_{Pull_up}

V2P5

Rpull_up

Pull_Up
TL (µs)

EP80579

Via

Break out

Board

Break in

Via

PHY

Transmitter
(Data\Ctrl)

Receiver
(Data\Ctrl)

LD\C_Brk_out_tx   LD\C_Brd_route_tx   LD\C_Brk_in_tx

$L_{D\backslash C\_Total\_tx} = L_{D\backslash C\_Brk\_out\_tx} + L_{D\backslash C\_Brd\_route\_tx} + L_{D\backslash C\_Brk\_in\_tx}$

NOTE: Breakout\ Breakin descriptions are as follows:

1. Routing where trace is 3.75 mil wide and 4mil spacing is implemented to escape\ enter BGA
2. The Breakout \ Breakin Length is defined from the pin of the BGA, to where 4 mil spacing
   increases to the required spacing per SI recommendations.

a). Data\Ctrl = 12 mil edge-to-edge (e2e) for Stripline
b). Data\Ctrl = 18 mil edge-to-edge (e2e) for Microstrip

Table 84.   GbE RGMII Transmit Path Data\Control Routing Guidelines

Parameter	Routing Constraints	
Routing Layer	**Stripline**	**Microstrip**
Reference Plane	Ground Reference	
Board Trace Impedance	55 Ω	55 Ω
Trace Width	3.75mils (L3/L8)	4.5mils (L1/L10)
Data\Control Spacing (e2e)	12 mils (min)	18 mils (min)
EP80579 Data\Control Tx Breakout Length (LD\C_Brk_out_tx)	0.5 inch (max)	0.5 inch (max)
Data\Control Tx Board Length (LD\C_Brd_route_tx)	min =1.0 inch max = 7.0 inch	min =1.5 inch max = 8.0 inch
PHY Data\Control Tx Breakin Length (LD\C_Brk_in_tx)	0.3 inch (max)	0.3 inch (max)
Total Data\Control Tx Routing (LD\C_total_tx)	LClk_total_tx ± 50 mils (See Table 83)	LClk_total_tx ± 50 mils (See Table 83)
Pull Up Resistor T-Line (Lpull_up)	0.4 inch (max)	0.4 inch (max)
Pull Up Resistor (Rpull_up)	1.2 KΩ (5%))	1.2 KΩ (5%)
Breakout\Breakin Spacing (e2e)	4 mils (min)	4 mils (min)

19.6.2   GbE Receive Topology

19.6.2.1   GbE Receive Clock Topology

Figure 140 shows the routing topology of the GbE Receive clock. The receive clock topology is for the routing of GbEn_RxCLK (RGMII) or GbEn_CLK (RMII). The routing guidelines for the Receive Data and Control signals in section Section 19.6.2.2 are referenced to the Receive clock. Table 85 provides routing guidelines for the Receive Clock signals.

Figure 140. GbE RGMII Receive Path Clock Topology

RGMII Receive Path Clock Topology
(EP80579 ←——— PHY)

L_{Pull_up}

V2P5

Rpull up

Pull Up
TL (μs)

EP80579

PHY

Via

Break in

Board

Break out

Via

Receiver
Clock

Transmitter
Clock

LCLK_Brk_in_rx   LCLK_Brd_route_rx   LCLK_Brk_out_rx

LCLK_Total_rx = LCLK_Brk_out_rx + LCLK_Brd_route_rx + LCLK_Brk_in_rx

NOTE: Breakout\ Breakin descriptions are as follows:

1. Routing where trace is 3.75 mil wide and 4mil spacing is implemented to escape\ enter BGA
2. The Breakout \ Breakin Length is defined from the pin of the BGA, to where 4 mil spacing
   increases to the required spacing per SI recommendations.
   a). Clock = 20 mil edge-to-edge (e2e) for Stripline
   b). Clock = 25 mil edge-to-edge (e2e) for Microstrip

Table 85. GbE RGMII Receive Path Clock Routing Guidelines

Parameter	Routing Constraints	
Routing Layer	**Stripline**	**Microstrip**
Reference Plane	Ground Reference	
Board Trace Impedance	50 Ω	50 Ω
Trace Width	4.5mils (L3/L8)	5.5mils (L1/L10)
Clock Spacing (e2e)	20 mils (min)	25 mils (min)
PHY Clock Rx Breakout Length (LClk_Brk_out_rx)	0.5 inch (max)	0.5 inch (max)
Clock Rx Board Length (LClk_Brd_route_rx)	min =1.0 inch max = 7.0 inch	min =1.0 inch max = 7.0 inch
EP80579 Clock Tx Breakin Length (LClk_Brk_in_rx)	0.3 inch (max)	0.3 inch (max)
Total Tx Clock Routing (LClk_total_rx)	min =1.0 inch max = 7.8 inch	min =1.0 inch max = 7.8 inch
Pull Up Resistor T-Line (Lpull_up)	0.625 inch (max)	0.625 inch (max)
Pull Up Resistor (Rpull_up)	1.2 KΩ (5%)	1.2 KΩ (5%)
Breakout\Breakin Spacing (e2e)	4 mils (min)	4 mils (min)

19.6.2.2 GbE Receive Data\Control Topology

The receive signals included in the GbE receive Data and Control topology (Figure 141) are:

— GBEn_RXCTL

— GBEn_RXDATA[3:0]

All the receive path Data and Control signals in a channel (see Figure 141) should be length matched, routed on the same layer, and referenced to the Receive Clock in section Section 19.6.2.1. The signals do not need to be length matched between channels, only within a channel. Table 86 provides routing guidelines for the Receive Interface signals.

Figure 141. GbE RGMII Receive Path Data/Clock/Control Topology

RGMII Receive Path Data\Control Topology
(EP80579 ⟵ PHY)

L_{Pull_up}

V2P5

Rpull up

Pull Up
TL (µs)

EP80579

PHY

Via   Break in   Board   Break out   Via

Receiver
(Data\Ctrl)

Transmitter
(Data\Ctrl)

LD/C_Brk_in_rx   LD\C_Brd_route_rx   LD\C_Brk_out_rx

LD\C_Total_rx = LD\C_Brk_out_rx +   LD\C_Brd_route_rx +   LD\C_Brk_in_rx

NOTE: Breakout\ Breakin descriptions are as follows:

1. Routing where trace is 3.75 mil wide and 4mil spacing is implemented to escape\ enter BGA
2. The Breakout \ Breakin Length is defined from the pin of the BGA, to where 4 mil spacing increases to the required spacing per SI recommendations.
   a). Data\Ctrl = 12 mil edge-to-edge (e2e) for Stripline
   b). Data\Ctrl = 18 mil edge-to-edge (e2e) for Microstrip

Table 86. **GbE RGMII Receive Path Data\Control Routing Guidelines**

Parameter	Routing Constraints	
Routing Layer	Stripline	Microstrip
Reference Plane	Ground Reference	
Board Trace Impedance	50 Ω	50 Ω
Trace Width	4.5mils (L3/L8)	5.5mils (L1/L10)
Data\Control Spacing (e2e)	12 mils (min)	18 mils (min)
PHY Data\Control Rx Breakout Length (LD\C_Brk_out_tx)	0.5 inch (max)	0.5 inch (max)
Data\Control Rx Board Length (LD\C_Brd_route_rx)	min =1.0 inch max = 7.0 inch	min =1.0 inch max = 7.0 inch
EP80579 Data\Control Tx Breakin Length (LD\C_Brk_in_rx)	0.3 inch (max)	0.3 inch (max)
Total Data\Control Rx Routing (LD\C_total_rx)	LClk_total_rx ± 50 mils (See Table 85)	LClk_total_rx ± 50 mils (See Table 85)
Pull Up Resistor T-Line (Lpull_up)	0.625 inch (max)	0.625 inch (max)
Pull Up Resistor (Rpull_up)	1.2 KΩ (5%))	1.2 KΩ (5%)
Breakout\Breakin Spacing (e2e)	4 mils (min)	4 mils (min)

19.7 GbE Serial EEPROM

The GbE MACs use a 4K- bit (256 x 16 bits each) serial EEPROM device for storing product configuration information. Several EEPROM words are automatically accessed by the GbE controller after reset to provide pre-boot configuration data before it is accessed by the host software. The remainder of the stored information is available to software for storing the MAC addresses and additional configuration information for three GbE MACs. The EEPROM algorithm programmed into the GbE controllers is compatible with most commercially available 3.3V Microwire* interfaces, serial EEPROM devices, with a 256 x 16 organization and a 1 MHz speed rating.

All three controllers share the same EEPROM. A fixed priority arbiter controls access to the EEPROM where highest priority is given to GbE 0 then GbE 1 and finally GbE 2.

19.8 Wake on LAN

Two types of wake-up mechanisms are supported:

• Advanced Power Management (APM) Wake-up

• ACPI Power Management Wake-up

When so configured, if a wake-up packet is received, the GBE_PME_WAKE signal will be asserted. The GBE_PME_WAKE signal of all three GbE MACs are wired-or together and brought to the external pin GBE_PME_WAKE. The user must externally connect this pin to the PME_N input pin.

19.9 GbE RComp

The GbE RCOMP (Resistive COMPensation) circuitry dynamically compensates the GbE I/O output drivers for variations in operating conditions due to process, temperature, voltage and PCB layout. These variations are measured through a resistive mechanism in two special I/O pads.

The resistive mechanism on those I/O pads references external resistors that the user provides to optimize the signal impedance termination. Thus the output driver impedance can be tuned specifically to the application PCB characteristics for nominal signal transfer into the transmission lines formed by the PCB traces. The RCOMP design is nominally set to operate at 50 ohm, but the user is free to set the impedance in the range 45 ohm to 55 ohm.

Two RCOMP pins (GbE RCOMPP and GbE RCOMPN) are provided to establish the GbE output driver impedance, one to control the drive high strength and one to control the drive low strength. These RCOMP outputs drive into external resistors. For the Development Board, the GbE RCOMPP is connected via a 50 ohm resistor to ground, while GbE RCOMPN is connected through a 50 ohm resistor to the GbE auxiliary power supply. The drivers form a resistor divider and the voltages developed in these dividers are compared to a reference voltage. The RCOMP state machine independently adjusts the strength of the drivers making them stronger or weaker until the comparator signals that the voltage is greater than or less than the reference. The state machine will continue making adjustments causing the comparators to oscillate between two strength settings just above and just below the comparator trip point. Logic in the RCOMP state machine recognizes when this "dithering" between the two values has begun and holds the strength output for the GbE outputs fixed at one of the two settings. Note this algorithm is independently and concurrently applied to the drive high strength and to the drive low strength.

The GbE RCOMP controller starts operation when the GBE_AUX_PWR_GOOD input is asserted. This condition indicates the power supplies are stable; the condition also indicates that the GBE_REFCLK input is being driven with a 125 MHz clock. The GBE_REFCLK input is divided by either 4 or 16 and then used to drive the RCOMP state machine. Software accessible registers that provide options to monitor/overwrite internal bias and comparator output are also present.

19.10 Crosstalk Considerations

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the tRMATCH skew parameter. tRMATCH is the sum of the trace length mismatch between GbE Clock and Data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the clock trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-GbE signals.

19.11 Pull-up Termination

For the Development Board, signal pull-up termination is implemented at the receiver side of the interface to achieve acceptable signal integrity by controlling signal reflection, overshoot/undershoot, and ringback. Table 85 and Table 86 provide the recommended pull-up termination value at the receiver endpoint. The system designer should ensure through simulations or other techniques that the pull-up termination is required and fulfils their specific LAN interface signal integrity requirements.

19.12 General Gigabit Ethernet Design Guidelines

The platform GbE Connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of the interface specification. Some general guidelines appear below. The board designer should simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk.

Use the following general routing and placement guidelines when laying out a new design (see Figure 139 and Figure 140):

- Gigabit Ethernet signals must be ground referenced.

- Route all traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane can cause signal reflections and must be avoided.

- Minimize layer changes. Use a maximum of 4 vias per GbE trace for microstrip or a maximum of 6 vias for stripline. Via count includes thru-hole connector as an effective via. Use a maximum of six vias for stripline in order to connect to the AC decoupling capacitors. If a layer change is necessary, ensure that trace matching for either the transmit or receive pair occurs within the same layer.

- Do not route GbE traces under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use and/or duplicate clocks.

20.0   IEEE 1588-2008 Hardware Assist Interface

IEEE 1588-2008 is a precision clock synchronization standard for network measurement and control systems. IEEE 1588-2008 was intended to be used in full-duplex LAN (Local Area Network) topologies, for applications such as industrial automation in factories and processing plants within a single building.

The main objective of IEEE 1588-2008 is to accurately synchronize independent clocks, running on separate nodes of a network, to a grandmaster clock.

The EP80579 provides hardware assist for GbE0, GbE1, CAN0, CAN1 and the two auxiliary input signals, master and slave mode. The master device holds the grandmaster clock and the slaves synchronize to the master. The hardware also supports the following outputs:

- transmit trigger
- received trigger
- pulse per second
- test signal

The accuracy of the system depends on the topology of the network and the software architecture. Microseconds to sub-microsecond accuracy is possible in real applications.

The topology consists of assigning one of the nodes to become a master. The master holds the grandmaster clock, and the other nodes become slaves within the network. The slaves attempt to synchronize to the grandmaster. The main objective of the slaves is to be in sync with the master, via the IEEE 1588-2008 protocol.

A classic example of IEEE 1588-2008 is to synchronize clocks in a school to the main grandmaster clock. Figure 142 shows an example of a system with clocks running in a network that supports IEEE 1588-2008 and another school network that does not support IEEE 1588-2008.

Figure 142. Classic Clock Synchronization Example
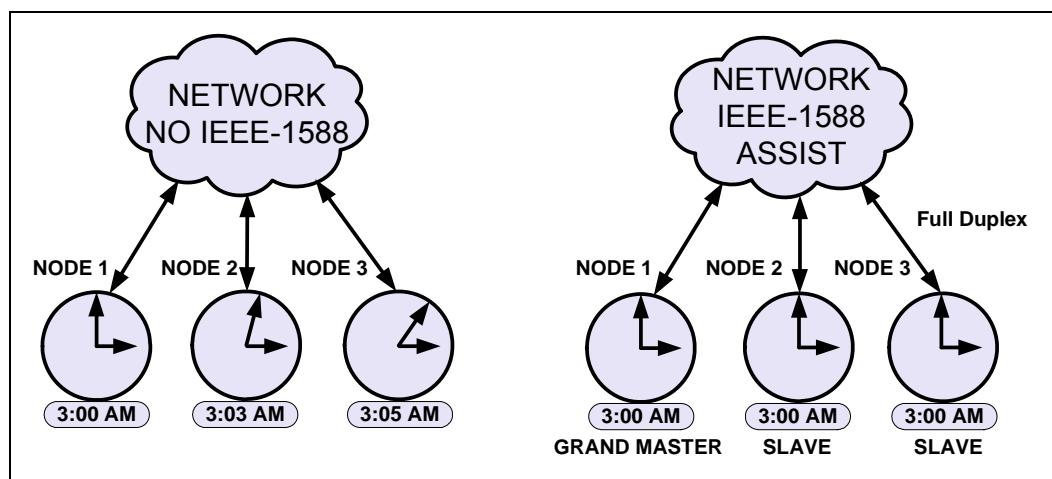
20.1   Input/Output Signal Application

The IEEE 1588-2008 hardware assist has a total of six input/output signals, as described in the following tables.

Inputs	
ASMSSIG	• Auxiliary Slave Mode Snapshot • Must be pulled down with a 10K ohm resistor when the port is not connected to an interfacing device.
AMMSSIG	• Auxiliary Master Mode Snapshot • Must be pulled down with a 10K ohm resistor when the port is not connected to an interfacing device.

Outputs	
1588_TESTMODE_DATA	• Test Mode Data • Can be left NC when the port is not connected to an interfacing device.
1588_PPS	• Test Pulse Per Second • Can be left NC when the port is not connected to an interfacing device.
1588_RX_SNAP	• Receive Snapshot Taken • Can be left NC when the port is not connected to an interfacing device.
1588_TX_SNAP	• Transmit Snapshot Taken • Can be left NC when the port is not connected to an interfacing device.

This section describes how the signals shown in the tables above can be used for debugging, event capture, and event trigger. The usage of the input/output signals can vary from application-to-application and software implementation.

All of the above signals can be accessed on the Development Board via the IEEE 1588 Hardware Assist Interface Connector J53.

Figure 143 shows the internal architecture of IEEE 1588-2008 hardware assist implementation in the EP80579. It also shows the various internal registers within the block, such as the System Time Clock register, which contains the system time used for time stamping and triggering events that can be used to drive outputs. Examples of these conditions are:

- expiration of the Target Time or Auxiliary Target Time register
- PPS Compare register greater or equal to the system time clock
- Ethernet or CAN message detect
- edge detect of Auxiliary Master/Slave inputs

All of the conditions shown above generate interrupts, which can be serviced immediately for time-critical applications.

The above features require software support, if you intend to use these features, see the *Intel® EP80579 Integrated Processor Product Line Programmer's Guide* for implementation and support.
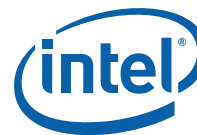
Figure 143. EP80579 IEEE 1588-2008 Hardware Assist Block Diagram
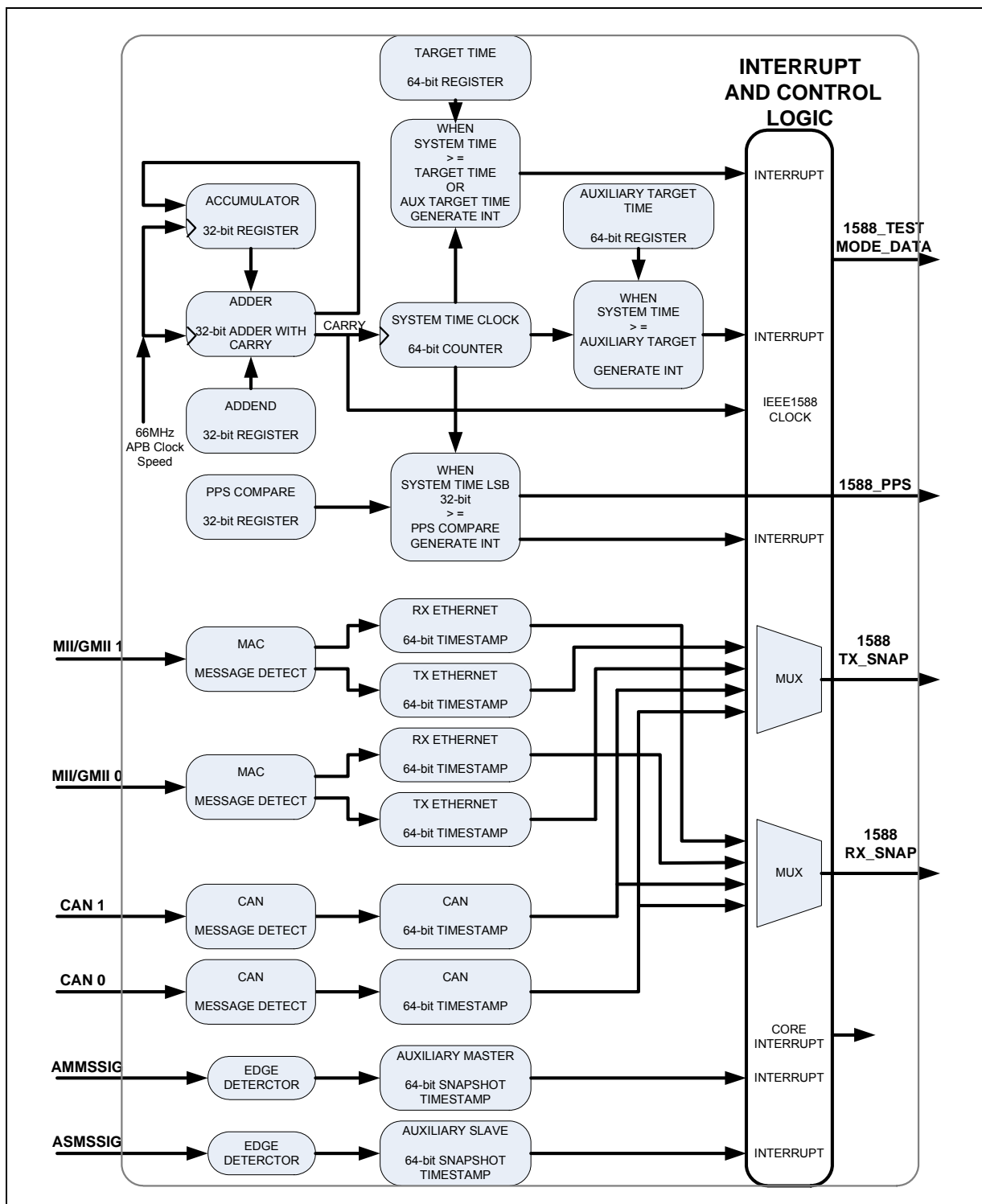
20.1.1   Input

Two input pins, AMMSSIG and ASMSSIG, connect to the IEEE 1588-2008 hardware module. These signals can be used to detect status change of events that will require a timestamp for tracking purpose. A typical example can be to adjust gain in a close loop system using servo motors to control the mechanism of a fast moving robotic arm.

The hardware detects signal status changes by detecting positive edges. Once a positive edge is detected, the hardware will timestamp the event and store the timestamp information in either the Auxiliary Master or Auxiliary Slave register, depending on what signal is being detected. The hardware will then generate an interrupt to the processor that indicates a snapshot event has been captured and it needs to be serviced. The processor can choose to ignore the event or service it. An output can be generated to trigger additional external hardware as part of a close loop system or simply for debug purposes.

20.1.2   Outputs

There is a total of four programmable output pins:

- 1588_TESTMODE_DATA
- 1588_PPS
- 1588_RX_SNAP
- 1588_TX_SNAP

These signals can be used to trigger external hardware or signal out the detections of messaging timestamp of any of the two Ethernet or CAN network interfaces. The maximum frequency of these signals is 66 MHz, which is derived from the APB bus clock frequency.

1588_RX_SNAP and 1588_TX_SNAP are programmable signals that can be used to generate triggering pulses when receiving or generating timestamps from GbE0/GbE1 and CAN0/CAN1.

TP_PPS pulse per second signal can be programmed to generate sequential pulses, which can be used to generate a clock for the synchronization purposes of external hardware. The duty cycle of the signal is 50% and is ideal for clocking external devices.

1588_TESTMODE_DATA will be used on future applications.

20.1.3   Board Design Tips

Implement standard board design rules for 66 MHz signal speed.

Signals that are not being used can be left floating. For the signals being used, board impedance can be anywhere from 45 to 65 ohm.

21.0 Controller Area Network (CAN) Interface

Controller Area Network (CAN) is a serial communication protocol that can efficiently transfer distributed real-time control commands and small data streams with very high levels of security. CAN fulfils the communication needs of a wide range of applications from high-speed networks to low-cost multiplex wiring.

The hardware interface is done via two wire differential pair, transmitting and receiving in a half duplex mode. The interface is capable of transmitting bit rates of up to 1Mbps to a maximum transmission line of 30 meters over a typical twisted pair. Networks with longer transmission lines can be implemented at lower bit rates. Signal delay on the transmission lines, as well as the number of nodes connected to the network, will have an impact to the bit rate. As the distance and number of devices increases, the bit rate will need to be decreased. This is done to overcome the signal delay in the network topology as the signals move through the twisted pair and experience delays.

The EP80579 supports two CAN controllers with IEEE 1588-2008 Hardware Assist. The controller requires an external physical interface (CAN driver), therefore this section provides an example of how to connect an external CAN driver.

As stated earlier, this is a two wire physical interface that requires differential signal routing guideline for board design.

Figure 144 shows one of the standard connectors used to interface to the outside world. The CAN protocol does not specify or recommend a mechanical connector, however, industry uses various connectors with a number of pin definitions. The example shown in Figure 144 shows a DB9 connector, which is one of the most common connectors used in industry.

The value of resistor R1 is selected to adjust the rise/fall time of the differential signals; as the value of R1 is incrementing, so will the rise/fall time. See the datasheet for the CAN Transceiver for the resistor ratio that affects the proportion of the rise/fall time.

Figure 144. CAN Physical Interface Example
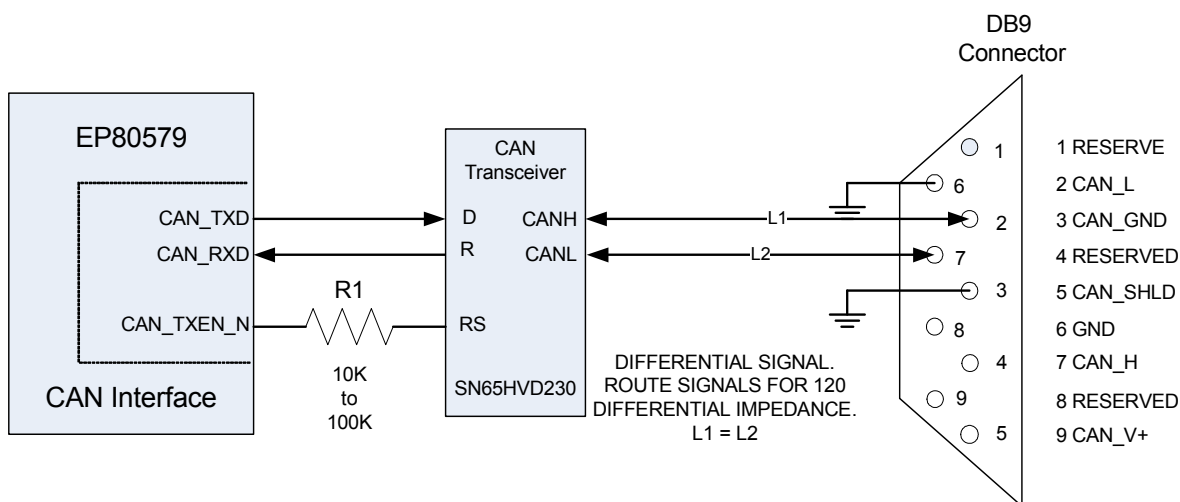
BXXXX-001

21.1 Input/Output Signal Application

The CAN controller has a total of three input/output signals per CAN port, as described in the following tables.

Inputs	
CN0RXD	• Receive Data, Channel 0 • Must be tied high to a 10K ohm resistor when the port is not connected to an interfacing device.
CN1RXD	• Receive Data, Channel 1 • Must be tied high to a 10K ohm resistor when the port is not connected to an interfacing device.

Outputs	
CN0TXD	• Transmit Data, Channel 0 • Can be left NC when the port is not connected to an interfacing device.
CN1TXD	• Transmit Data, Channel 1 • Can be left NC when the port is not connected to an interfacing device.
CN0TXEN	• Transmit Data Enable, Channel 0 • Can be left NC when the port is not connected to an interfacing device.
CN1TXEN	• Transmit Data Enable, Channel 1 • Can be left NC when the port is not connected to an interfacing device.

All of the signals shown in the above two tables are single ended LVTTL 3.3V logic, and they are NOT 5V tolerant.

CNTXD and CNRXD are used to transmit and receive signals, which are relatively low speed, up to 1 MHz. The only signal that requires special attention is CNTXEN; this signal requires a series damping resistor. It is required to control the rise or fall time the differential pair in the CAN Driver. Use the table provided in the data sheet for the CAN Driver to determine the value of resistor R1.

21.2 Multipoint Topology

CAN networks can implement multipoint topologies. The interconnect between nodes is typically done with a simple twisted pair of 120 ohm impedance as shown in Figure 145. The transmission line must be terminated at both ends of the line with a 120 ohm resistor. This is done to minimize reflections at the end of the line. The energy sent by the transmitting node needs to be absorbed at the end of the transmission line so that pulses are not reflected back and forth, and the energy is absorbed by the 120 ohm resistor.

Figure 145. CAN Multipoint Topology
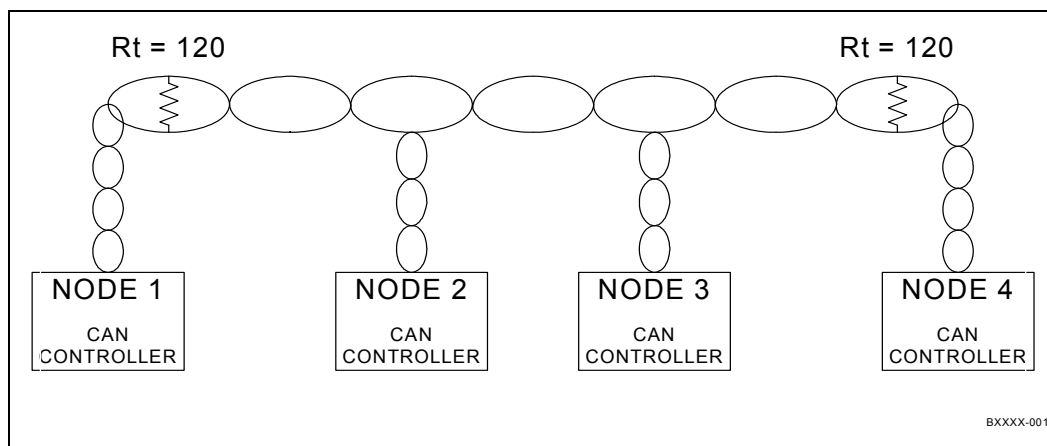
Each of the messages sent by the transmitting node are received by every node in the network, including the transmitting node. The transmitting node checks for errors or collisions in the message send. If an error is sensed, the transmitting node will attempt to retransmit. If two nodes attempt to transmit at the same time, the node sending the highest priority message will win and the node sending the lower priority message will stop transmitting immediately. All nodes on the network receive and process the message send if it is identified to be for them. Multiple nodes can identify the message to be for them, and process it at the same time. For example, in the case where there are temperature sensors in the network and a broadcast message is sent to all devices to read and send their respective temperature readings to the requesting node. Each one of the temperature sensing devices will process the requesting message and start sending their reading one by one.

21.2.1 Board Design Tips

- Implement standard board design routing rules for differential pairs signal.
- LVTTL signals can be routed to maintain impedance anywhere from 45 to 65 ohm.
- Follow design guides described by the PHY CAN transceiver used in your design.

22.0 Local Expansion Bus (LEB) Interface

The EP80579 Local Expansion Bus (LEB) is a flexible, general purpose communication interface between the EP80579 and external peripherals. LEB is specifically designed for compatibility with Intel and Motorola*-style microprocessor interfaces, as well as Texas Instruments* DSP standard Host-Port Interfaces* (HPI).

The LEB controller supports 25-bit address bus and 16-bit data bus, running at a maximum speed of 80 MHz feed in from an external clock oscillator. At 80 MHz, the maximum load on the bus is limited to a max of two devices. At lower speeds the number of devices can be increased as shown in the Development Board, which runs at 33 MHz.

The LEB is a flexible and multifunction bus, which can support various modes of operation, such as target devices shown in the following table:

Intel multiplexed	Intel non-multiplexed
Intel StrataFlash®	Synchronous Intel StrataFlash® Memory
Micron* Flow-Through ZBT	Motorola multiplexed
Motorola non multiplexed	Texas Instruments* Host Port Interface (HPI)

The LEB controller has an address decoder, which can generate up to 8 programmable Chip Selects (CS); each one of them able to support up to 32Mbyte of address space.

All supported modes are seamless and no additional glue logic is required. Other cycles, such as 8-bit access or 16-bit types, may be supported by configuring the Timing and Control Register for Chip Select. There is no support for 32-bit or wider transaction accesses.

22.1 LEB Chip Select Assignment

Each Chip Select is connected to a device that can be independently mapped into a contiguous IA-32 address space in blocks of 1 K to 32 MB. The eight Chip Selects can address up to 256 MB of contiguous IA-32 address space. The start address of these blocks is hard-coded on the 32 MB boundaries and no other device may be inserted into the address space occupied by the particular CS.

The Development Board makes full use of all eight CS signals EX_CS[7:0]#. The assignment of all CS signals to the various peripherals on board appears below.

Chip Select Signal	Peripheral
EX_CS[7:0]#	FPGA
EX_CS0#	Flash 1, Intel StrataFlash® P30
EX_CS[2:1]#	Compact Flash
EX_CS3#	Flash 2, Intel StrataFlash® P30

Chip Select Signal	Peripheral
EX_CS4#	Mezzanine Connector 1
EX_CS5#	Mezzanine Connector 2
EX_CS6#	Mezzanine Connector 3

22.2 LEB Memory Size (LEB_SIZE) Strapping

As stated above, the LEB controller allocates up to 256 MB of memory space to support up to 8 devices on the LEB Bus. At power-up or whenever RESET_IN# is asserted, EX_ADDR[23:21] bits are captured and stored by the LEB controller to detemine the LEB memory size (LEB_SIZE) and the number of devices supported on the bus. The EX_ADDR[23:21] should be externally strapped with 1K ohm pull-ups and pull-downs to determine the LEB_SIZE as shown in Table 87.

Table 87.   LEB Memory Size (LEB_SIZE) Strapping

LEB_SIZE [23 : 21]	MMBAR Size	# of CS "+ 16 MB" mode	# of CS "+ 32 MB" mode
000	0 MB	None	None
001	32 MB	2	1
010	64 MB	4	2
011	128 MB	8	4
1xx	256 MB	16 (See Note)	8

Note: Only 8 chip selects are supported; the other 8 are alias of the first 8 chip selects. Refer to the *Utilizing the Local Expansion Bus on the Intel® EP80579 Integrated Processor Product Line Application Note*, Document Number 321096 for details.

22.3 LEB Interface Topologies

There are three groups of signals that require careful routing when designing with the LEB interface. These groups are split into Chip Select, Address, and Data/Control signals. The following sections recommend guidelines to help design a working system that will minimize signal integrity issues. The recommendations are based on the Development Board routing with the LEB clock rate at 33 MHz.

22.3.1 LEB Interface Topology at 33 MHz

The Development Board has been designed to interface with up to 7 devices, which are split in two bridges. The primary bridge interconnects with the first four peripherals and a buffer, while the secondary bridge interconnects with three mezzanine connectors. The connectors are to be used to interface with existing line cards and future develop cards. With careful routing and following the guidelines in this chapter, this topology can run at a maximum speed of 33 MHz.

Figure 146. Multi-drop Topology Diagram
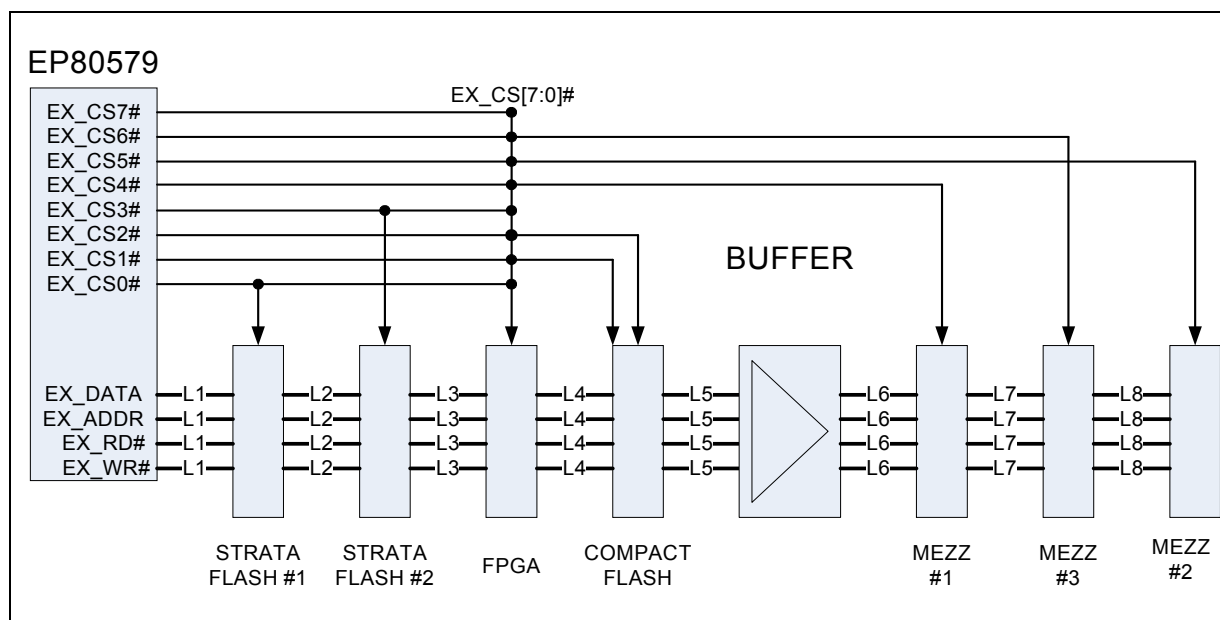
Table 88 contains information for trace length measurements that came from the Development Board. Use this information as a reference when designing similar topologies. It is strongly recommended to perform simulations for your specific applications.

Table 88.   Multi-drop Topology Trace Lengths for the Development Board

Trace	Average Length
L1	2.5 inch
L2	1.0 inch
L3	2.5 inch
L4	2.0 inch
L5	1.0 inch
L6	1.5 inch
L7	1.0 inch
L8	5.0inch

22.3.2   Chip Select Topologies

Chip Select is a point-to-point signal that must be closely routed to match the Address, Data, and Control signal trace lengths. In order for signals to arrive at the same time through the bus and avoid timing issues, all three groups must tightly match to +/- 500 mil.

External board pull-ups are required on EX_CS_N to ensure the signal remains deasserted, so that a spurious transfer does not start due to board noise. Additionally, the system designer is responsible for ensuring that all the tri-stated signals do not become indeterminate. It is recommended to terminate the EX_CS_N signal with a 10K ohm pull-up resistor.

Figure 147 and Table 89 indicate min and max trace lengths that can be used when routing chip select signals.

Figure 147. Chip Select Point-to-Point Topology Diagram
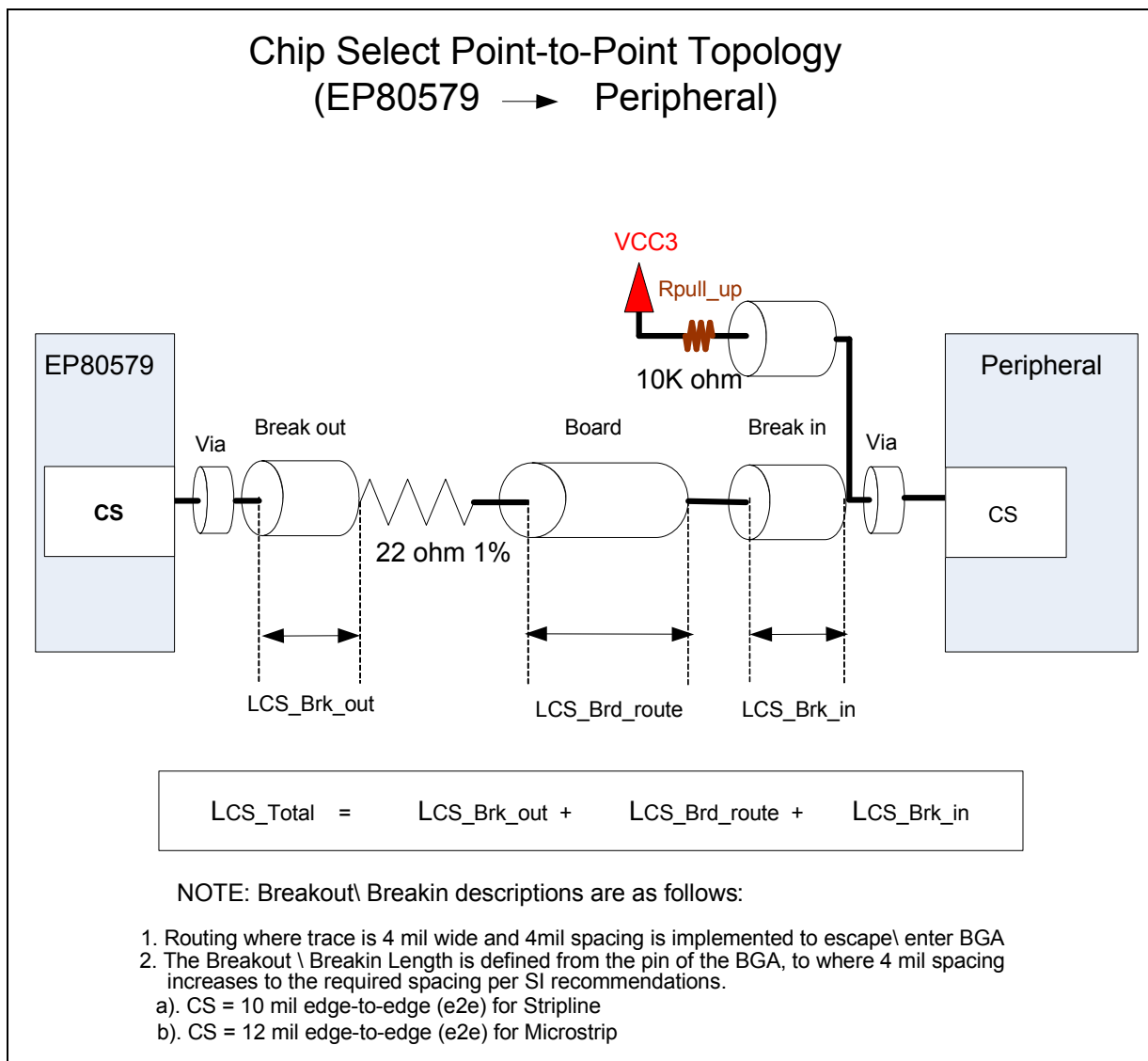
Chip Select Point-to-Point Topology (EP80579 → Peripheral)

$$LCS\_Total = LCS\_Brk\_out + LCS\_Brd\_route + LCS\_Brk\_in$$

NOTE: Breakout\ Breakin descriptions are as follows:

1. Routing where trace is 4 mil wide and 4mil spacing is implemented to escape\ enter BGA
2. The Breakout \ Breakin Length is defined from the pin of the BGA, to where 4 mil spacing increases to the required spacing per SI recommendations.
   a). CS = 10 mil edge-to-edge (e2e) for Stripline
   b). CS = 12 mil edge-to-edge (e2e) for Microstrip

Table 89.   Chip Select Point-to-Point Topology Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Constraints	
Routing Layer	Stripline	Microstrip
Reference Plane	Ground Referenced	
Board Trace Impedance	50 Ω	50 Ω
Trace Width	4.5mils (L3/L8)	5.5mils (L1/L10)
Chip Select to Other Signals Spacing	10 mils (min)	12 mils (min)

Table 89. **Chip Select Point-to-Point Topology Routing Guidelines (Sheet 2 of 2)**

Parameter	Routing Constraints	
EP80579 Chip Select Breakout Length (LCS_Brk_out)	1 inch (max)	1 inch (max)
Chip Select Board Length (LCS_Brd_route)	max = 16 inch	max = 16 inch
EP80579 Chip Select Breakin Length (LCS_Brk_in)	1.5 inch (max)	1.5 inch (max)
Pull Up Resistor (Rpull_up)	10 KΩ (5%))	10 KΩ (5%)
Breakout\Breakin Spacing (e2e)	4 mils (min)	4 mils (min)

22.3.2.1 Chip Select Address Allocation

The LEB occupies 256 MB of address space in the EP80579 Memory Map. Each of the eight chip selects in the LEB has been allocated 32 MB of addressing space which can be individually programmed through the Timing and Control register. For a complete description of the chip select functionality, see the Local Expansion Bus Controller in the *Intel® EP80579 Integrated Processor Product Line Datasheet.*

22.3.3 Address Star Topologies

Address signals are normally routed in a multi-point topology; the main reason for this is due to the nature of the bus. The bus is meant to interface with multiple devices which interconnect in a parallel fashion; usually there being more than one device, connected to the interface. The group signals are required to be matched with each other, a conservative matching value could be within 500 mils. The matching number will go down as the speed of the bus is increased. Each of the address, data, chip selects and control signal groups must also match with each other. Attempt to math the signals as close as possible. This will help avoid potential timing issues. Notice that for the address signals, it is not required to use dumping series resistors. However depending on your design configuration, it might be required to place pull-down resistors for strapping purpose at boot time. Make sure proper pull-down resistors are in place for you system configuration. It is recommended to use 1K ohm pull-down resistor. Pull-ups are not required, as there is an internal weak resistor already that pulls the signal high.

Figure 148 shows the star topology used in the Development Board design to interconnect the data bus to the various peripherals in the LEB bus. Table 90 provides the general routing rules such as impedance, min and max trace lengths.

22.3.4 Data and Control Star Topology

Figure 148. Address Signals Star Topology Diagram
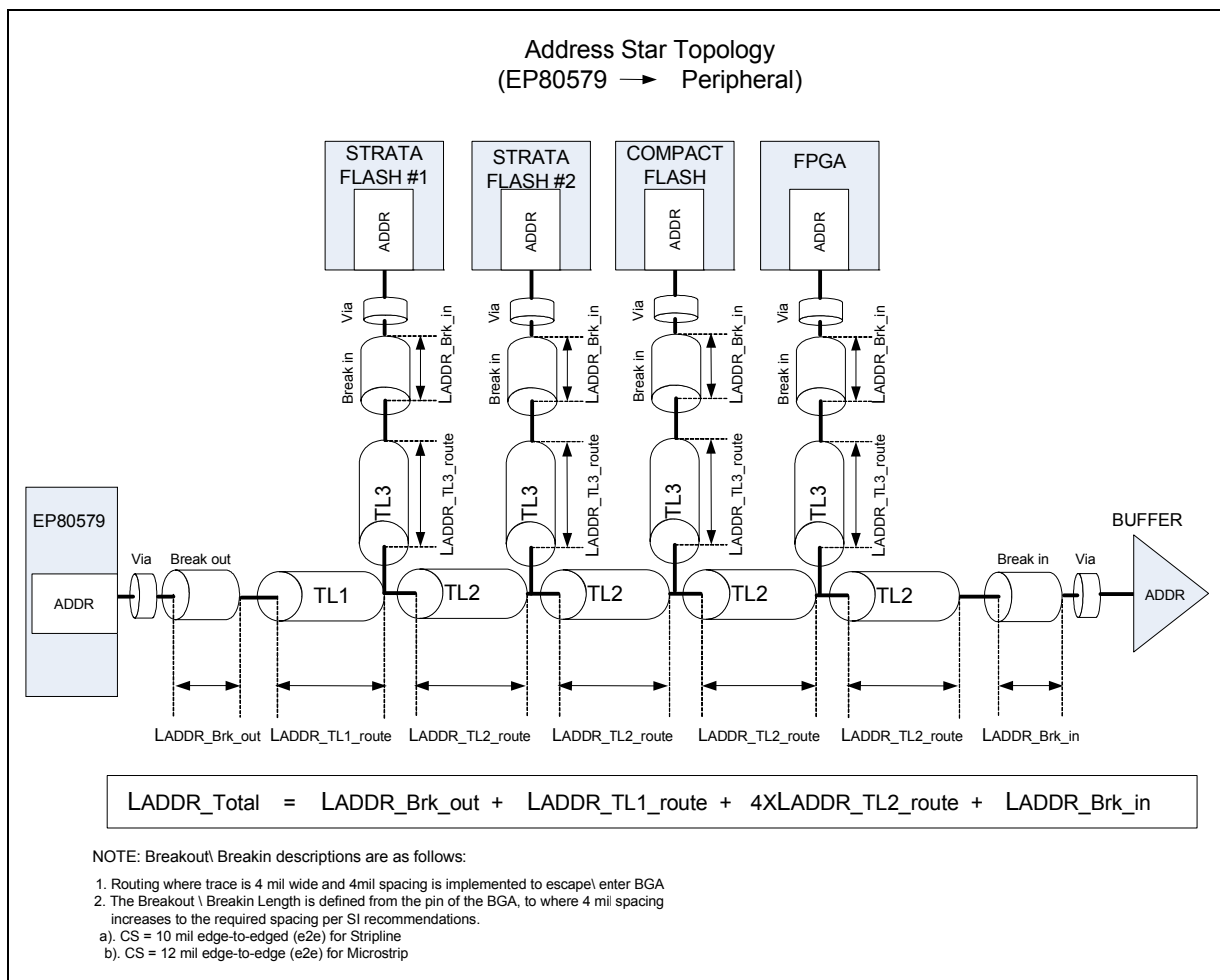
Data and control signals require very similar guidelines as stated in the above Section 22.3.3, "Address Star Topologies" on page 241, but with a very important key difference, it is required to place a series 22 ohm damping resistor at the destination end of the transmission line. This will help damp the over shoot of signals when the data logic levels are generated by the peripherals. The overshoot can be generated when reading the devices and the signals are propagated on the bus. Match signals groups as stated in the above section to approximately 500 mils.

Figure 149 shows the star topology used in the Development Board design to interconnect the data and control signals to the various peripherals in the LEB bus. Table 90 provides the general routing rules such as impedance, min and max trace lengths.

22.3.4.1 Adding Delay to EX_RD#

The EP80579 requires a 2nSec (min) read hold time (Trdhold) on the data bus when reading external devices connecting to the LEB interface. Some of the external devices are able to meet the requirement but many of them do not.
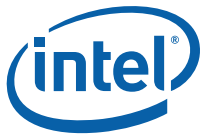
One easy way to check this is to look at the specification of the device being used in the design and look for the hold time on data during reads. In many occasions you will see a few nanoseconds for Thold, but in some other cases the Thold = 0 nSec. This is the case in which it is required to do something externally to meet this timing. A simple solution that will resolve the hold time requirement would be to delay the EX_RD# signal with a chip multilayer delay line. The Development Board design uses LDH32 2.5 nSec delay line to meet the EP80579 requirement of Trdhold=2nSec.

Note: By delaying the EX_RD#, you also must ensure that the Trdsetup still is valid. Normally this is not a problem since the data becomes valid and is available early in time to allow the to met setup.

Figure 149. Data, and Control Signals Star Topology Diagram
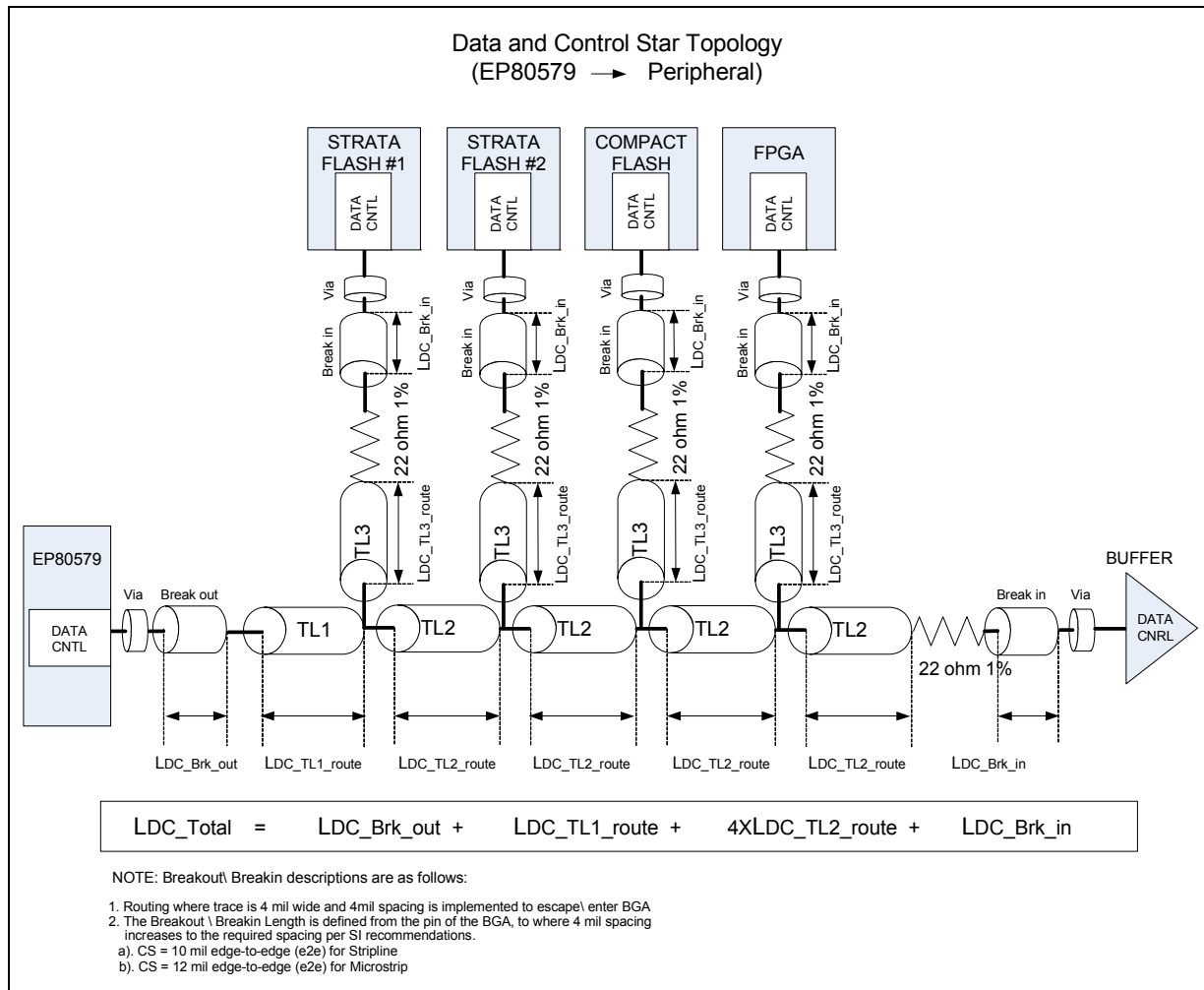
Table 90.   Address, Data and Control Star Topology Routing Guidelines

Parameter	Routing Constraints	
Routing Layer	Stripline	Microstrip
Reference Plane	Ground Referenced	
Board Trace Impedance	50 Ω	50 Ω
Trace Width	4.5mils (L3/L8)	5.5mils (L1/L10)
Address\Data\Control to Other Signals Spacing	10 mils (min)	12 mils (min)
EP80579 Address\Data\Control Breakout Length (LADDR_Brk_out\LDC_Brk_out)	1 inch (max)	1 inch (max)
EP80579 Address\Data\Control (LADDR_Total\LDC_Total)	max = 14 inch	max = 14 inch
EP80579 Address\Data\Control Breakin Length (LADDR_Brk_out\LDC_Brk_out)	1.5 inch (max)	1.5 inch (max)
Address Pull Down Strapping Resistor (as required for your specific design)	1 KΩ (5%))	1 KΩ (5%)
Breakout\Breakin Spacing (e2e)	4 mils (min)	4 mils (min)
TL1	5 inch (max)	5 inch (max)
TL2	4 inch (max)	4 inch (max)
TL3	1.5 inch (max)	1.5 inch (max)

22.3.5   Mezzanine Card Interconnect

In order to isolate external plug-in cards and to relieve the loading to the LEB bus, it is recommended to make use of bidirectional buffers. The buffers do not support hot-plug however this is a feature that can be implemented in other designs with some additional logic. Depending of the buffers used, it might or might not be required to use series damping resistors. The Development Board uses the 74LVC16245 bidirectional buffers, which do not required series damping resistor. However other application might vary, specially if customers are designing new cards or the drive strength of the peripherals used might vary, or simply if the speed of the LEB bus is increased.

Figure 150 and Table 91 are very similar to those above, except that the secondary bridge is isolated through the buffers.

Figure 150. Address, Data, and Control Signals Mezzanine Star Topology Diagram
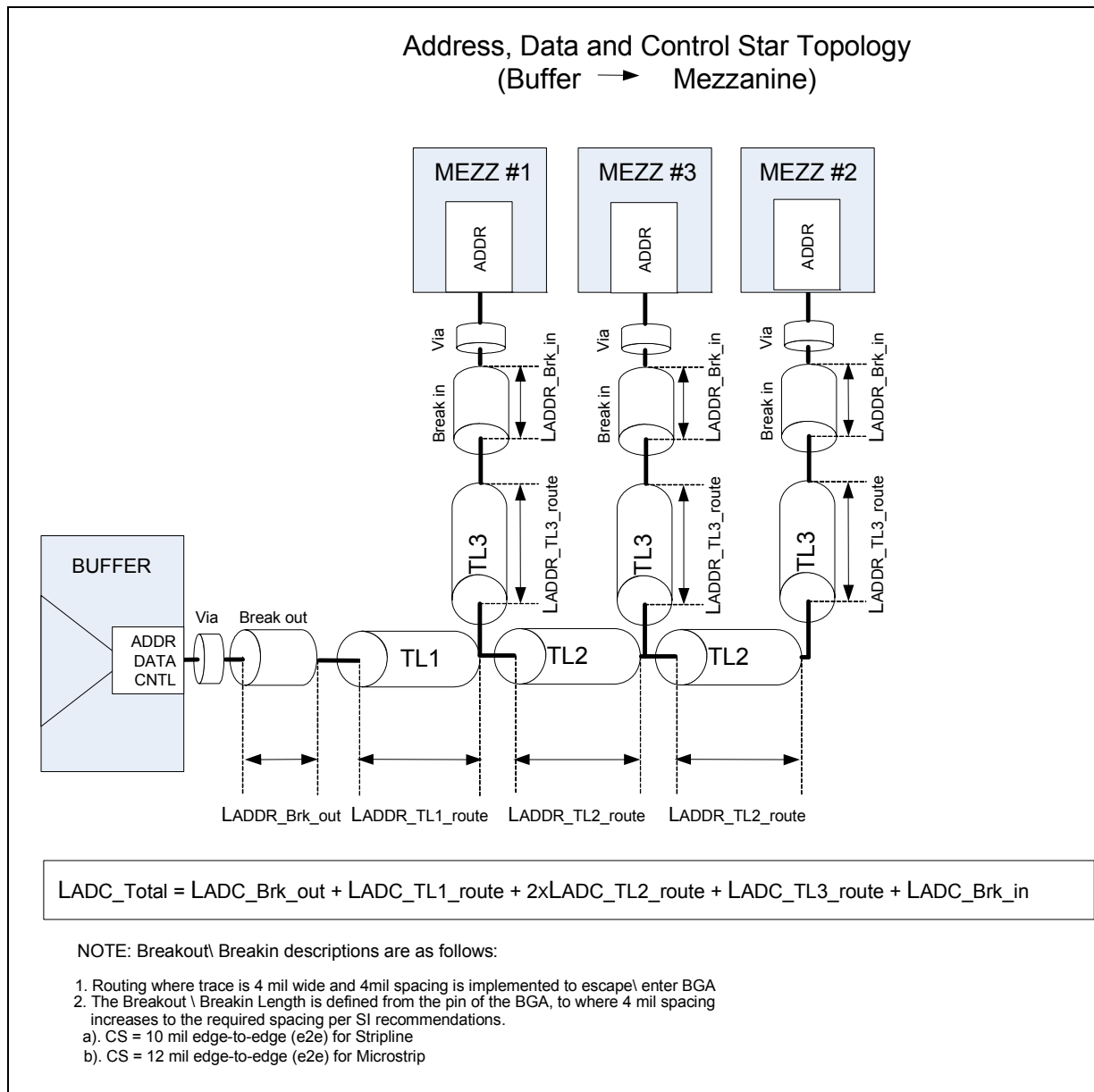
Address, Data and Control Star Topology
(Buffer → Mezzanine)

$LADC\_Total = LADC\_Brk\_out + LADC\_TL1\_route + 2xLADC\_TL2\_route + LADC\_TL3\_route + LADC\_Brk\_in$

NOTE: Breakout\ Breakin descriptions are as follows:

1. Routing where trace is 4 mil wide and 4mil spacing is implemented to escape\ enter BGA
2. The Breakout \ Breakin Length is defined from the pin of the BGA, to where 4 mil spacing increases to the required spacing per SI recommendations.
   a). CS = 10 mil edge-to-edge (e2e) for Stripline
   b). CS = 12 mil edge-to-edge (e2e) for Microstrip

Table 91. Address, Data and Control Star Topology Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Constraints	
Routing Layer	Stripline	Microstrip
Reference Plane	Ground Referenced	
Board Trace Impedance	50 Ω	50 Ω
Trace Width	4.5mils (L3/L8)	5.5mils (L1/L10)

Table 91. Address, Data and Control Star Topology Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Constraints	
Address\Data\Control to Other Signals Spacing	10 mils (min)	12 mils (min)
Buffer Address\Data\Control Breakout Length (LADC_Brk_out)	1 inch (max)	1 inch (max)
EP80579 Address\Data\Control (LADC_Total)	max = 8 inch	max = 8 inch
EP80579 Address\Data\Control Breakin Length (LADC_Brk_out)	1 inch (max)	1 inch (max)
Breakout\Breakin Spacing (e2e)	4 mils (min)	4 mils (min)
TL1	5 inch(max)	5 inch(max)
TL2	4 inch(max)	4 inch(max)
TL3	1.5 inch(max)	1.5 inch(max)

22.3.6 Input/Output Signal Application

The LEB controller has a total of 17 input/output interfacing signals, which might required special pull-up resistors. This can occur when the interface is not connected to a devices or simply not being used.

Input/Output	
EX_ADDR[24:0]	• Address Bus • Can be left NC when the interface is not connected to an interfacing device or not used.
EX_DATA[15:0]	• Data Bus • Can be left NC when the interface is not connected to an interfacing device or not used.
EX_BE[1:0]#	• Bus Byte Enable • Can be left NC when the interface is not connected to an interfacing device or not used.
EX_PARITY[1:0]	• Bus Parity • Can be left NC when the interface is not connected to an interfacing device or not used.
EX_RD#	• Bus Read *Note:* The EP80579 requires a 2 nSec hold time during read accesses. Requires to delay EX_RD# signal if the interfacing device cannot meet the Thold=2nSec time required by the EP80579. • Can be left NC when the interface is not connected to an interfacing device or not used.
EX_WR#	• Bus Write • Can be left NC when the interface is not connected to an interfacing device or not used.

Output	
EX_ALE	• Address Latch Enable • Can be left NC when the interface is not connected to an interfacing device or not used.
EX_CS[7:0]#	• Chip Selects 0 to 7 • External 10K ohm resistor board pull-ups are required to ensure this signal remains deasserted. • EX_CS[7:4]# can be configured for HPI mode of operation. While in HPI mode, each chip select has a corresponding EX_RDY#: EX_CS[7]# corresponds to EX_RDY[3]# in HPI Mode EX_CS[6]# corresponds to EX_RDY[2]# in HPI Mode EX_CS[5]# corresponds to EX_RDY[1]# in HPI Mode EX_CS[4]# corresponds to EX_RDY[0]# in HPI Mode • Intel and Motorola* mode share EX_IOWAIT for all chip selects EX_CS[7:0]#.

Input	
EX_CLK	• 33/80 MHz Expansion Bus Clock • Must be sourced even when the interface is not used or connected to other devices.
EX_IOWAIT#	• Target Wait • Must be tied high to a 10K ohm resistor when the interface is not connected to an interfacing device or not used.
EX_RDY[3:0]#	• Bus Ready • Must be tied high to a 10K ohm resistor when the interface is not connected to an interfacing device or not used.
EX_BURST	• Burst Size • Must be tied high to a 10K ohm resistor when the interface is not connected to an interfacing device or not used.

All of the signals shown in the above two tables are single ended LVTTL 3.3V logic, and they are NOT 5V tolerant.

22.3.7 Design Notes

Care must be taken when loading the bus with too many devices. As more devices are added, the loading capacity adds up, to the point where timing can become critical.

To account for this, timing on the expansion bus may be adjusted in the Timing and Control Register for Chip Select. If an edge rises slowly due to low drive strength, the processors should wait an extra cycle before the value is read. For more information, see the documentation on Timing and Control Register for Chip Select bits [29:16] in the *Intel® EP80579 Integrated Processor Product Line Datasheet*.

Note: The recommendations made in this chapter is based on using a 33 MHz clock for the LEB interface in the Development Board. If it is required to increase the clock frequency, proper timing calculations or simulations need to be implemented to ensure there will not be a timing issue in the design.

23.0 Time Division Multiplex (TDM) Interface

Time Division Multiplex (TDM), also referred to as High-Speed Serial (HSS), is a hardware module whose primary function is to provide connectivity between EP80579 and external devices such as SLICs and CODECs. There is a total of three TDM ports, which can support a total of 12-T1/E1 or 4-T1/E1 per port. Typical applications include voice/data through voice-over broadband systems for CODECs and DSL framers. TDM ports are software configured to support various serial protocols, such as T1/ E1/J1, and MVIP.

23.1 Development Board TDM Support

The Development Board supports a total of three mezzanine card connectors. Each connector supports two TDM ports. This was done to maintain compatibility with previous voice mezzanine cards such as the Intel® EPAVM80579 Analog Voice Card and future mezzanine cards which might require two TDM ports. Currently the Intel® EPAVM80579 card only makes use of a single TDM port, the second port is not used.

23.2 SLIC/CODEC Interface

One of the most common devices used in voice applications, such as telephony, are SLIC/CODEC modules which are used to encode voice analog signals to digital signals in a very common mode called TDM encoding. Data moves through the TDM port, in both directions from the SLIC/CODEC to the EP80579 TDM or from the EP80579 to the SLIC/CODEC. The device also requires configuration and control service, which is normally done via the Synchronous Serial Port (SSP) interface.

23.3 Device Connection

Figure 151 shows a typical interconnect between the EP80579 and four SLIC/CODEC devices. The diagram does not represent the interconnect of SLIC/CODECs in the Development Board design. The diagram is meant to show how to interface in a simple manner, bypassing CPLDs and FPGAs in a platform design. To avoid software changes, you must follow the design guidelines provided by the Development Board.

The SLIC/CODEC devices used for this example are from Silicon Laboratories* and have been used in a number of evaluation platforms. See the Intel® EPAVM80579 Analog 4x1 Card design for details on the components used.
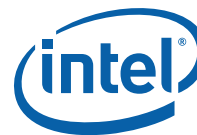
Figure 151. TDM to SLIC/CODEC Interface Example
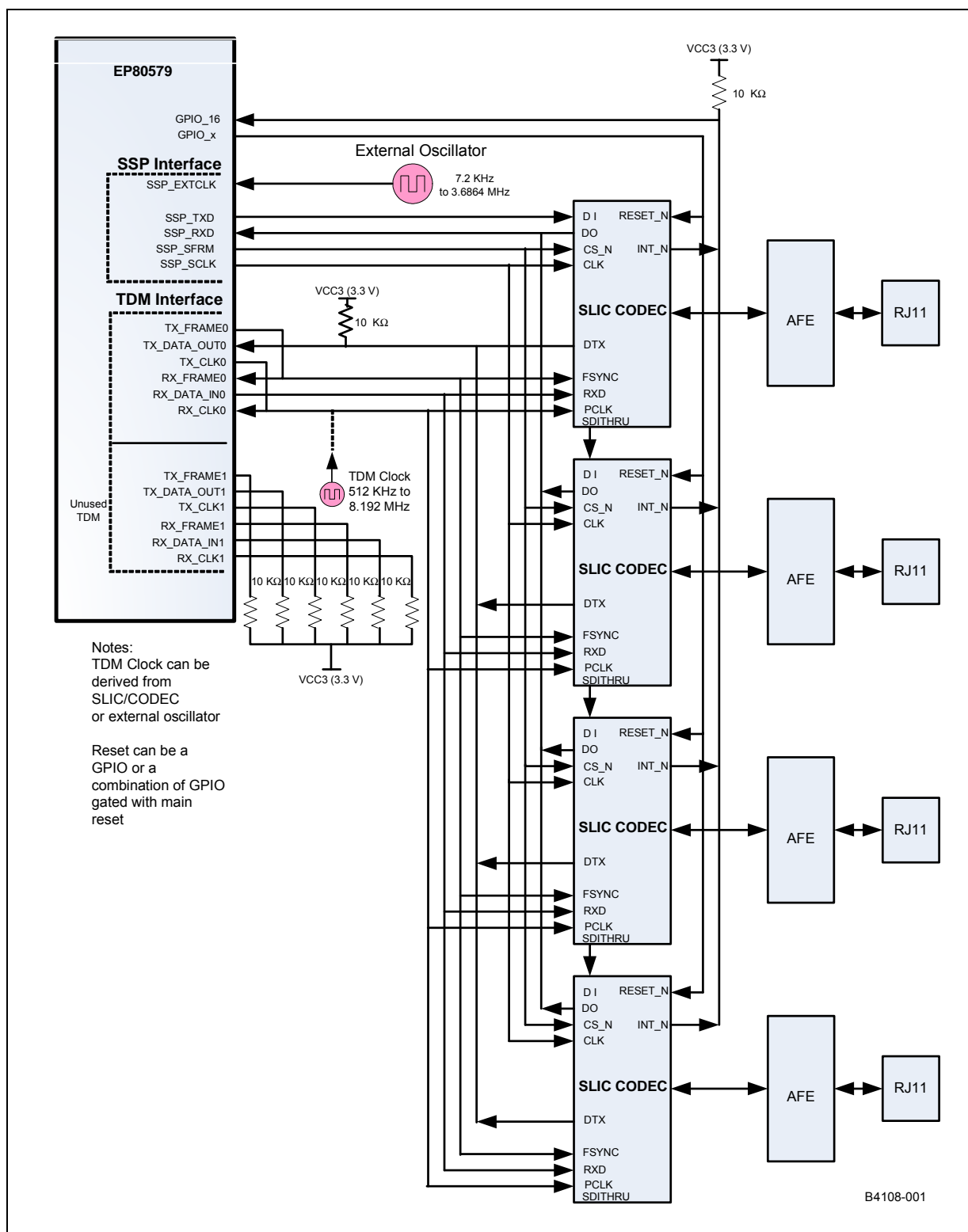
23.3.1   Input/Output Signal Application

The TDM controller has a total of 6 input/output signals per TDM port, as shown in the following tables:

Inputs/Output	
TX_FRAME[2:0]	• Transmit Frame Channel 0, 1 and 2 • Must be tied high to a 10K ohm resistor when the port is not connected to an interfacing device.
RX_FRAME[2:0]	• Receive Frame, Channel 0, 1 and 2 • Must be tied high to a 10K ohm resistor when the port is not connected to an interfacing device.
TX_CLK[2:0]	• Transmit Clock Channel 0, 1 and 2 • Must be tied high to a 10K ohm resistor when the port is not connected to an interfacing device.
RX_CLK[2:0]	• Receive Clock, Channel 0, 1 and 2 • Must be tied high to a 10K ohm resistor when the port is not connected to an interfacing device.

Output	
TX_DATA_OUT[2:0]	• Transmit Data Channel 0, 1 and 2 • Must be tied high to a 10K ohm resistor when the port is not connected to an interfacing device.

Input	
RX_DATA_IN[2:0]	• Receive Data Channel 0, 1 and 2 • Must be tied high to a 10K ohm resistor when the port is not connected to an interfacing device.

Note: The signals shown in the tables are single ended LVTTL 3.3V logic, and they are NOT 5V tolerant.

23.3.2   Design Notes

The TDM interface does not fall into the high speed design category and therefore high speed design rules are not required. When designing hardware for the TDM interface, use routing and signal integrity rules that apply to the 10 MHz signals speeds. If the use of LEB is required to control SLIC/CODECs, see the design rules for that particular peripheral and design for the speed at which the bus will be running.

24.0 Synchronous Serial Port (SSP) Interface

Synchronous Serial Port (SSP), is a hardware module whose primary function is to provide connectivity between the EP80579 and external devices. The EP80579 supports a single SSP port, however the port can be multiplexed to various devices. Each device can be selected with a dedicated chip select. Only one device can be accessed at a time. The SSP module supports National Microwire*, Texas Instruments* Synchronous Serial Port (SSP) and Motorola* Serial Peripheral Interface (SPI).

Two of the most common port configuration modes to access external devices are SPI and Microwire. Such interfaces can connect with RTC (Real-Time Clock), LCD (Liquid Crystal Display), Digital Thermal Sensors, EPROM, Flash, etc.

Clocking can be derived internally or from an external source. The internal clock can be selected from an internal, 3.6864 MHz source and divided down to the desired standard frequency (for applications that require usage of the external input pin SSP_EXTCLK). The input clock frequency is also 3.6864 MHz as well as the internal source clock, the frequency can be divided down anywhere from 7.2 KHz to 1.84 MHz.

24.1 Development Board SSP Support

The Development Board provides SSP interface to all three mezzanine card connectors. The SSP port, as well as a number of GPIO signals, are routed to all mezzanine connectors. GPIO signals can be configured for input interrupts or outputs that can be used to gate the chip select to access multiple devices with a single HSS port.

24.2 EP80579 SSP Interface

The EP80579 SSP interface has a total of five input/output signals. These signals can be configured to the various hardware protocols supported by the SSP port. The following tables show the five pins supported:

Inputs	
SSP_RXD	• Receive Data • Must be tied high to a 10K ohm resistor when the port is not connected to an interfacing device.
SSP_EXTCLK	• External Clock • Must be tied high to a 10K ohm resistor when the port is not connected to an interfacing device.

Outputs	
SSP_SCLK	• Serial Clock • Can be left NC when the port is not connected to an interfacing device.
SSP_TXD	• Transmit Data • Can be left NC when the port is not connected to an interfacing device.
SSP_SFRM	• Serial Frame • Can be left NC when the port is not connected to an interfacing device.

24.2.1 Serial Peripheral Interface (SPI)

Serial Peripheral Interface (SPI) is a widely use serial interconnect. Many products are available specifically to interface to SPI. One of the most common uses of SPI is to store boot code or data storage. Some other common applications store board revision, serial numbers, or assembly information. Figure 152 provides an example of a Serial Flash device interface to the SSP port.

The following table shows how the SSP signals can be mapped when operating in SPI mode.

Motorola SPI	
SSP_SCLK	SCLK - Serial Shift Clock
SSP_TXD	MOSI - Master Out Slave In
SSP_RXD	MISO - Master In Slave Out
SSP_SFRN	/SS - Slave Select

Figure 152. SSP to Serial Flash Interface Example
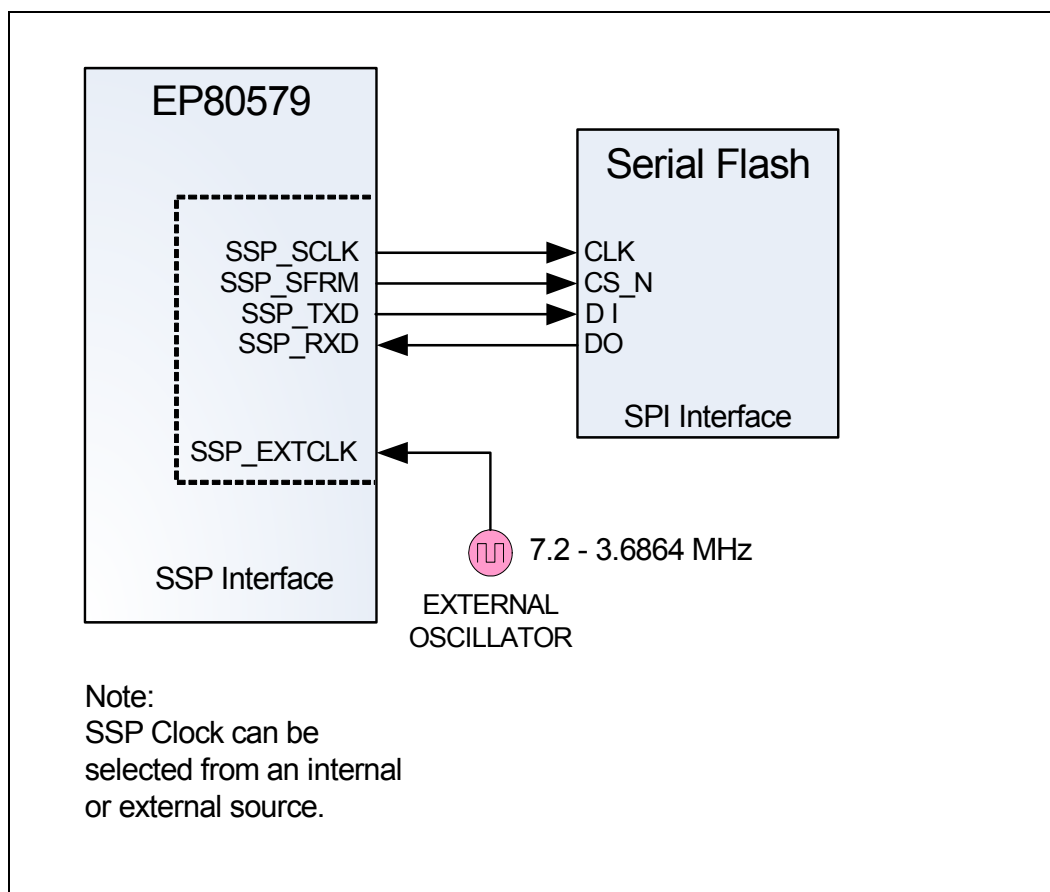
24.2.2 Microwire* Interface

Microwire is another common serial interface that is widely used to interconnect with serial devices. The following table shows how the SSP signals can be mapped when operating in Microwire mode.

National Microwire	
SSP_SCLK	SK - Serial Shift Clock
SSP_TXD	SO - Serial Out (Master and Slave)
SSP_RXD	SI - Serial In (Master and Slave)
SSP_SFRN	CS - Chip Select

24.2.3 Board Design Tip

Implement standard board design rules for low speed signals. When designing a board, specify board impedances to match anywhere between 45 to 65 ohm.

25.0 Sideband Signals

Table 92 describes the EP80579's IA-32 core legacy and miscellaneous signals.

Table 92. Sideband Signals (Sheet 1 of 4)

Signal Name	Group	Description
CPUSLP_OUT#	CPU Sideband Output	**CPU Sleep:** • This EP80579 output signal is made visible to the platform for debug purposes only. This internal EP80579 signal places the processor into a state that saves substantial power compared to the Stop-Grant state. When EP80579 is in this state, it does not recognize snoops or interrupts. The processor will only respond to deassertion of CPUSLP_OUT# or a system reset while in Sleep state. If CPUSLP_OUT# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. • This signal can be monitored via a LED. • Pull up signal to Platform 3.3V (VCC3) power supply using 4.7KΩ ± 5% resistor if used. **Note:** • This signal can be left as a no connect (NC) if not used.
INIT33V_OUT#	FWH Reset	**CPU Initialization:** • This 3.3V EP80579 output signal is made visible to the platform to reset the Firmware Hub. Internal EP80579 signal that when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT_N assertion. INIT_N is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. • Connect to FWH INT# pin. • Pull up signal to Platform 3.3V (VCC3) power supply using 4.7KΩ ± 5% resistor if used. **Note:** • This signal can be left as a no connect (NC) if not used.

Table 92.   Sideband Signals (Sheet 2 of 4)

Signal Name	Group	Description
NMI	CPU Sideband Output	**Non-Maskable Interrupt:** • NMI forces a non-maskable interrupt to the IA-32 core CPU if configured. The CPU detects an NMI as a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register (I/O Register 61h), except when an external platform agent is driving the NMI pin. • This signal should be pulled-down to GND using 10KΩ ± 5% resistor.
SMI_OUT#	CPU Sideband Output	**System Management Interrupt:** • This EP80579 output signal is made visible to the platform for debug purposes only. This internal EP80579 signal is active low output synchronous to PCICLK that is asserted in response to one of many enabled hardware or software events. On accepting a System Management Interrupt, the processor saves the current state and enter System Management mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. • Pull-up to EP80579 3.3V (VCC33) power supply using 10KΩ ± 5% resistor if used. *Note:* • This signal can be left as a no connect (NC) if not used.
STPCLK_OUT#	CPU Sideband Output	**Stop Clock Request:** • This EP80579 output signal is made visible to the platform for debug purposes only. This internal EP80579 signal is an active-low output synchronous to PCICLK that is asserted in response to one of many hardware or software events. When the processor samples STPCLK_OUT# asserted, it causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the CPU FSB and CPU APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK_OUT# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK_OUT# has no effect on the bus clock; STPCLK_OUT# is an asynchronous CPU input generated by the EP80579 IICH. • Pull-up to EP80579 3.3V (VCC33) power supply using 10KΩ ± 5% resistor if used. *Note:* • This signal can be left as a no connect (NC) if not used.

Table 92. Sideband Signals (Sheet 3 of 4)

Signal Name	Group	Description
RCIN#	CPU Sideband Input	**Keyboard Controller Reset Processor:** • The keyboard controller can generate INIT# to the CPU. This saves the external OR gate of other sources of INIT#. When EP80579 detects the assertion of this signal, INIT# is generated for 16 PCICLK clocks. • EP80579 ignores RCIN# assertion during transitions to the S3, S4 and S5 states. • Connect to Keyboard Reset (KBDRST#) pin of the Keyboard Controller provided by the Super I/O device. ***Note:*** • This signal should be pulled-up to VCC3 (3.3V) using a 10KΩ ± 5% resistor.
A20GATE	CPU Sideband Input	**A20 Gate:** • A signal from the keyboard controller. Acts as an alternative method to force the A20M# signal active. Saves the external OR gate needed with various other chipsets. • Connect to A20M pin of the Keyboard Controller provided by the Super I/O device. • Pull up signal to Platform 3.3V (VCC3) power supply using 10KΩ ± 5% resistor ***Note:*** • This signal should be pulled-up to VCC3 (3.3V) using a 10KΩ ± 5% resistor if not used
CPURST#	CPU Sideband Output	**Processor Bus Reset:** • The IMCH assets CPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is deasserted. The CPURST# allows the processor to begin execution in a known state. • Processor reset output signal that can be used by a debug tool. • Pull up signal to Platform 3.3V (VCC3) power supply using 10KΩ ± 5% resistor if used. ***Note:*** • This signal can be left as a no connect (NC) if not used
CPUPWRGD_OUT	CPU Sideband Output	**CPU Power Good:** • This EP80579 output signal is made visible to the platform for debug purposes only. This signal is an open drain signal, and requires an external pull-up resistor. CPUPWRGD monitors an internal signal connected directly form the IICH to the processor and represents a logical AND of PWROK and VRMPWRGD signals • Pull up signal to Platform 3.3V (VCC3) power supply using 10KΩ ± 5% resistor

Table 92. Sideband Signals (Sheet 4 of 4)

Signal Name	Group	Description
IERR#	CPU Sideband Output	**EP80579 Internal Error:** • Asserted by the CPU as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (for example, NMI) by EP80579. The CPU keeps IERR# asserted until the assertion of INIT33V_OUT# or EP80579 is reset using SYS_RESET#. • Connect to GPIO[40] to be used as IOAPIC IRQ35 • Pull up signal to Platform 3.3V (VCC3) power supply using 10KΩ ± 5% resistor if used. ***Note:*** • This signal can be left as a no connect (NC) if not used

25.1 CPUSLP_OUT#, INIT33V_OUT#, NMI, SMI_OUT#, STPCLK_OUT, RCIN#, A20GATE, IERR#

These signals are asynchronous and adhere to the routing recommendations and topology recommended in Table 93.

Table 93. Routing Recommendations for Sideband Signals

Signal Name	Impedance	Width (W) / Spacing (S)	Layer	Notes
CPUSLP_OUT# INIT33V_OUT#, NMI, SMI_OUT#, STPCLK_OUT, RCIN#, A20GATE, CPURST#, CPUPWRGD_OUT, IERR#	50Ω	Stripline: W = 4.5 mils S = 15.0 mils Microstrip: W = 6.0 mils S = 15.0 mils	Stripline or Microstrip	1, 2
Routing Guidelines				
• The Sideband Signals are asynchronous signals and may be routed on either the stripline or microstrip layers • These signals may change layers, but this should be minimized as much as possible				

Notes:
1. W represents width of signal;
2. S represents spacing to any other signal.

26.0 Debug Port Design Guide

26.1 Overview

This chapter provides information about the design of an eXtended Debug Port (XDP). The details of this chapter are requirements for debug port design, unless the text explicitly states that a design rule or connection is optional.

Note: The ITP-XDP and ITP-XDP2 are run-control tools created by Intel® Corporation. They are not sold publicly by Intel. In this document, the term ITP and ITP-XDP can be interchanged with "run-control tool." Intel works with several run-control tool vendors to create tools that can be used for design (the guidelines presented within this document must also be followed). These vendors include:

- American Arium*
- International Test Technologies*
- Antron Electronics*

26.2 Terms and Definitions

Table 94. Terms and Definitions

Term	Definition
BPM	Break Point Monitor - Processor pins used by run-control tools to monitor and influence the internal state of the processor
Debug Port	Connection into a processor/chipset/platform environment used to provide control during debug and validation.
EMTS	Electrical Mechanical Thermal Specification
I²C	Inter-IC Bus. A two-wire serial interface.
ITP	In-Target Probe. An ITP is a run-control tool as produced by Intel as well as third party vendors. This specification is not meant to imply that any vendor's debug tool is preferred over any other. Contact your Intel representative for alternative vendors supporting the XDP.
ITP-XDP	A specific ITP for the eXtended Debug Port
ITP-XDP2	Functionally identical to ITP-XDP with the single added feature. of a built in USB power assist module.
JTAG	Joint Test Access Group. IEEE Standard 1149.1 style scan chain.
Local Tap Master	A device other than the ITP that is designed to control accesses into an IEEE Standard 1149.1 style scan chain and all TAP agents contained within that scan chain.
OCP	Observation Control Port
Power	Detection of and response to the system powergood state.
Reset	Detection and control of reset state for elements within the system.

Table 94.   Terms and Definitions

Term	Definition
Scan Chain	Collection of TAP devices with concurrent TAP state control and serial data connection. Note that the XDP definition permits more than one scan chain to be controlled.
TAP	IEEE Standard 1149.1 defined Test Access Port.
TAP Master	A device that is designed to control accesses into an IEEE Standard 1149.1 style scan chain and all TAP agents contained within that scan chain. The ITP is an example of a TAP master.
UP	Uni-processor.
VTAP	Operating voltage for the system TAP and TAP Master. For most systems this voltage is VTT. For systems with out VTT, this will be Vcc.
XDP	eXtended Debug Port - A specific implementation that provides additional interfaces useful for debug and validation above other debug port implementations.
XDP-SSA	XDP Second-Side Attach - alternate connector and debug capability for ITP-XDP, ITP-XDP2.

26.2.1   General Debug Port Overview

The debug port is a connection into a target-system environment that provides access to JTAG, run control, system control, and observation resources.

The XDP is a 60-pin, small form-factor connector, that provides for additional silicon / system debug resources compared to other debug-port implementations and provides for expansion for future capabilities.

The EP80579 also provided a consistent, IEEE 1149.1 compliant JTAG Boundary Scan Chain (BSC) for most interfaces. There are three high-speed interfaces, PCI Express*, SATA and USB, is not implemented in JTAG boundary scan. These interfaces are used the XOR Chains. See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for a detailed signal pin list for BSC and XOR chain.

26.2.2   Debug Port Design Reviews

Intel would be pleased to review your system for debug port design accuracy. Please contact your Intel field sales representative or Field Applications Engineer (FAE) for a formal design review of the debug port implementation on your system.

26.2.3   Depopulating XDP for Production Units

At some point there may be a desire to remove the XDP from production units. Intel recommends that the debug-port real estate and pads remain in place if they need to be populated for a future problem.

Depopulate all physical devices (connector, termination resistors, jumpers) except:

* Termination of OBSFN_x[0:1] / BPM[4:5]# / PREQ#, PRDY#
* Termination of TCK
* Termination of TDI
* Termination of TMS
* Termination of TRSTn

It is acceptable to replace the standard resistor values with any resistor value between 51 ohm to 1k ohm to reduce bill-of-material items.

26.2.4   General Guidelines

For some signals, the existence of on-die termination (ODT) within the processor or chipset will remove parts from the platform design. The processor or chipset-specific Thermal Design Specification will clarify if ODT exists on signals for this guideline.

Electrical lengths are provided in units of flight time. Conversion of flight time to board-trace lengths is dependent on what layer routing occurs on and the dielectric constant of the board materials for a specific design. Rule-of-thumb numbers can be derived by using 140 to 180ps/inch for outer layers of an FR4 product and 180ps/inch for inner layers.

Signals must be routed using 45 to 65 ohm +/-10% impedance traces. The length of any unterminated stub on any TCK (1:0) or observation-port pin nets must be less than 200ps unless otherwise stated. The 51 +/- 5% ohm recommendation in this document for signal termination has been proven to work on all recommended board impedances. JTAG and observation-port signals my optionally be terminated using the nominal-board impedance.

Debug port signals that are not discussed within this document may be assumed to be left floating, thus no termination is required.

TCK1, TCK0, system clocks, and all of the observation pins should be routed with high-speed design rules in mind, in particular:

- An effort should be made to minimize the number of layer transitions and plane split crossings imposed on each trace (ideally this will be zero). If return paths are well kept then the number of vias are nearly immaterial.

- Keep the critical signals referenced to GND whenever possible.

- Include ground-stitching vias near every layer transition. This is important even when referencing the same voltage on the new layer because the stitching via may reduce return current loops on the trace.

- For situations where these signals are routed referenced to one or more power planes, include a bypass capacitor near every layer transition or plane split between the two referenced planes.

- An effort should be made not to share XDP bypass capacitors with other high-speed signals.

- For all signals, pull-up termination resistors should be located above a solid-power plane. If a solid-power plane does not exist at the required termination location, add a 0.1uF ceramic capacitor to GND on the pull-up voltage within 0.5 inches of termination resistor.

26.2.5   Termination Resistors

Termination resistances are given, with tolerances, whenever appropriate. Tolerances are within +/- of the percentage.

With few exceptions (noted specifically in their description), termination resistors must be close to the receiver. The topology, at the end of the chain, must be terminated in one of the following ways (in all cases) except those noted in their specific description.

In the case of Figure 153, where there is a termination after the last receiver, (A) must be smaller than any noted maximum routing length. This is the typical way of showing terminations in this document. There is no restriction for the length of (B) unless otherwise noted.

Figure 153. Termination After Last Receiver
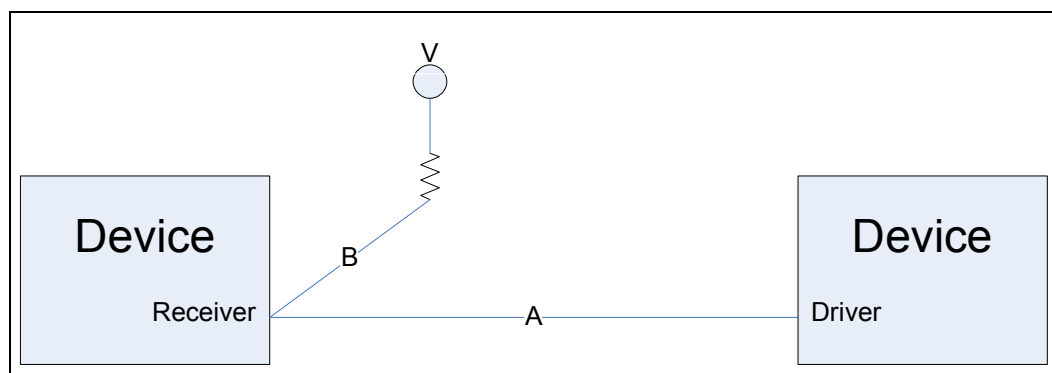
Figure 154 shows another method for termination that is equally valid. This is a termination prior to the end receiver where the maximum routing length of the signal must be less than the length of (D) + (C). (C) must be less than 200ps.

Figure 154. Termination Prior to Last Receiver
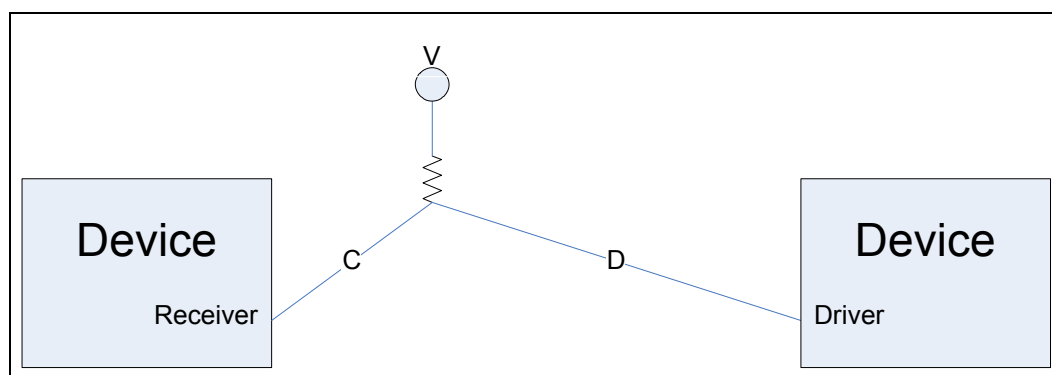
In both Figure 153 and Figure 154, there may be other devices on the (A) or (D) routing of the signal (if called for within this document).

26.3 Routing Guidelines

This section provides implementation details specific to these designs only and takes priority over any discrepancies existing between this document and any other Debug Port Design Guide.

For EP80579 systems, VTAP refers (within this section) to the 1.2V EP80579 core voltage.

26.3.1 JTAG Routing Guidelines

26.3.1.1 TDI-TDO Routing Guidelines

Route TDI and TDO as shown in Figure 155.

Figure 155. TDI-TDO Routing
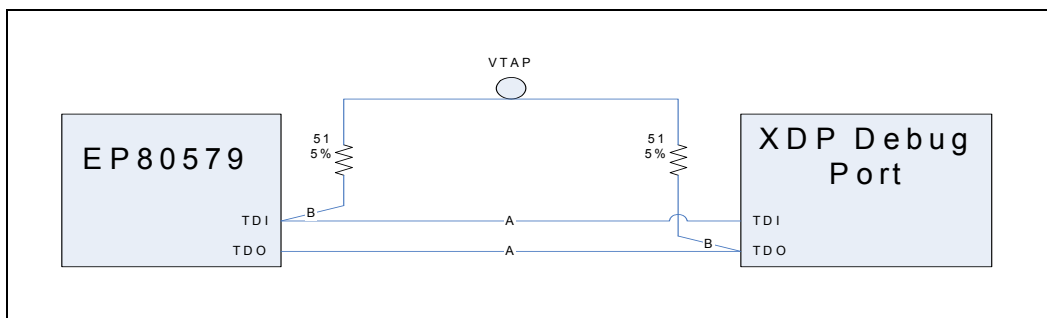
Notes:
>   (A) - These traces have no specific routing requirements.
>   (B) - This routing has no length requirements.

26.3.1.2 TCK0 and TCK1 Routing

Route TCK0 to the EP80579 TCK with a 51 ohm 5% resistor to GND at the EP80579 end. The trace length must be a maximum of 1.5ns. Any stub on this net must be shorter than 200ps.

Note: Leave TCK1 as a NO CONNECT.

26.3.1.3 TMS Routing Guidelines

This JTAG signal is routed as a daisy chain to all devices. There should be a 51 ohm 5% resistor to VTAP placed at the last load on the trace.

There is no trace-length requirement for this signal.

26.3.1.4 TRSTn Routing Guidelines

This JTAG signal is routed as a daisy chain to all devices on all chains. There should be a 51 ohm 5% pull-down resistor on the trace. The location of this resistor is recommended to be near the last device in the chain, but can be placed in other positions if necessary for platform layout. The trace length of this signal is unimportant.

26.3.2 Observation Port Routing Guidelines

There are four observation ports on the XDP labeled A through D. Each observation port is made up of four OBS Data lines and two OBSFN control/strobe lines. The observation ports of this debug port are used to support the following features:

26.3.2.1 Pilot Bus (NOA) Routing Guidelines

This signal is reserved. No connection to this signal are required.

26.3.2.2 BPM4_PRDY_OUT (BPM4) Routing Guidelines

Route point-to-point from EP80579 to the XDP debug port. Stubs on these nets must be no longer than 200ps. There are no specific routing lengths required for these nets.

Note: This signal may also be referred to as PRDY#. No termination is required on the platform for this signal.

26.3.2.3 BPM5_PREQ_IN (BPM5) and BPM3_IN (BPM3) Routing Guidelines

These nets have a board level circuit required to shift the VOH of the signal from the VCCOBS_AB/CD voltage level of 1.8V down to the 1.2V EP80579 core voltage of the input buffer. Route point-to-point from the XDP debug port to a 100 ohm resistor on the platform located within 1 inch of the EP80579 input pin. The other side of the 100 ohm resistor is connected to an active LOW enable quickswitch such as the SN75CBTLV1G125 or equivalent. When the quickswitch is enabled, the 100 ohm resistor provides a path to GND. the quickswitch is controlled by the XDP_PRESENT# signal described later in this document. There are no specific routing lengths required for these nets.

Figure 156. BPM5 and BPM3_in Platform Circuit
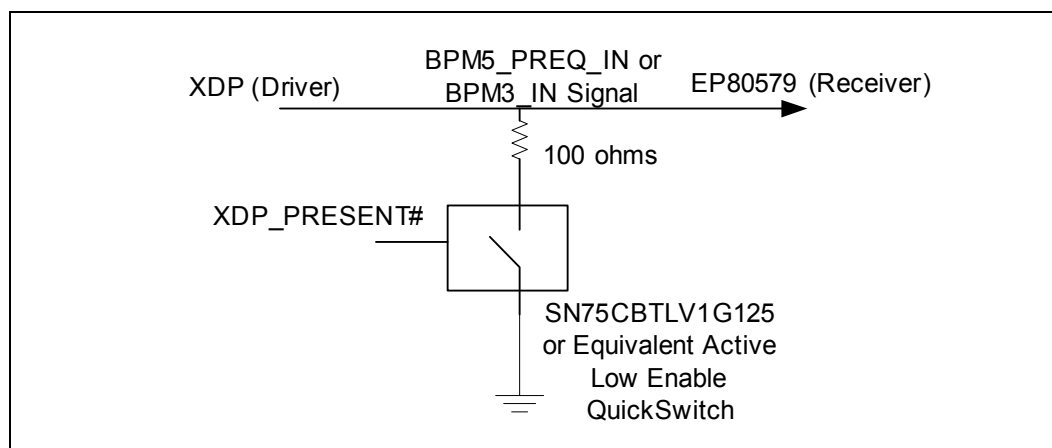
26.3.3 Hook Pins Routing Guidelines

The Hook [7:0] pins are used by the ITP-XDP to manage the system power, scan, and reset states of the target system. The pins are also used to support debug interfaces that are not common to all platforms.

26.3.3.1 PWRGOOD (HOOK0) Routing Guidelines

Route a system PWRGOOD (CPUPWRGD pin) signal directly to the XDP HOOK0 pin. This signal is used to indicate that the system's power delivery subsystem has reached stability. This signal must be asserted before the run-control tool will attempt operations. The run-control tool will not drive PWRGOOD. The run-control tool will use transitions on this signal as triggering events. Please consult the system's Platform Design Guidelines (PDG) for termination information. If edge integrity of PWRGOOD is critical to the operation of the target system, it is acceptable to place a 1k ohm isolation resistor, in series, between the target system PWRGOOD signal and the trace to the XDP HOOK0 pin. If there is no PWRGOOD on the system, pull this signal up to a voltage between 1.0V to 3.3V through a 1k to 10k ohm resistor.

There are no trace length requirements for this signal.

26.3.3.2 Reserved (HOOK[1])

This signal is reserved. No connection to this signal are required.

26.3.3.3 Reserved (HOOK[2])

This signal is reserved. No connection to this signal are required.

26.3.3.4 Reserved (HOOK[3])

This signal is reserved. No connection to this signal are required.

26.3.3.5 ITPCLK/ITPCLK# (HOOK[4:5]) Routing Guidelines

A copy of the system clock (BCLK) needs to be delivered to the XDP by a system-clock component. ITPCLK (BCLK) and ITPCLK# (BCLK#) are used for:

- noise and synchronizer fault survivability
- as a frequency reference for some observation-port protocols
- as a frequency reference for run-control operations when enabled by the run-control tool.

These operations may be disabled if ITPCLK is not connected or unavailable.

Route the reference clock differentially from the system-clock distribution component to the HOOK[4:5] pins of the debug-port connector. Provide adequate source termination of the clock traces at the clock driver. Route the signals using the specification of the driver. There are no length-matching requirements for this clock pair compared to any other signals in the target system.

Due to the variations in nomenclature, BCLK[0:1] is sometimes denoted as BCLK[p/n] respectively. Thus, BCLK[0] = BCLK[p] = ITPCLK = ITP_BCLK_P = HOOK4 is the rising edge for the beginning of every transaction. Conversely, BCLK[1] = BCLK[n] = ITPCLK# = ITP_BCLK_N = HOOK5.

26.3.3.6 RESET# (HOOK6) Routing Guidelines

The RESET# signal is an input to the run-control tool. Run-control tools will not drive RESET#. The run-control tool uses this signal to sense when a system reset has occurred.

Route the EP80579 RESET# signal to the XDP RESET# pin through a 1k ohm isolation resistor. Routing of this signal, before the isolation resistor, is left to the system designers as part of the system design guides. On the debug-port side of the isolation resistor, this signal has no length requirement.

The isolation resistor should be placed to remove any stub from the reset line by placing the isolation-resistance pad directly, at any point, on the RESET# signal line. There is no requirement from the point of view of the run-control tool, but the target system will have signal-integrity issues with greater than a minimum stub on the system RESET# line.

26.3.3.7 DBR# (HOOK7) Routing Guidelines

The DBR# signal is an output from the run-control tool to the system-reset control logic. The run-control tool uses this signal to initiate a system reset. This reset assertion must not cycle any power supplies on the target system nor may it alter the PWRGOOD signal. The run-control tool will drive this signal with a silicon switch closure to ground when a debug reset is requested.

Route this signal to any point within the system-reset topology that would initiate the appropriate reset. Typical implementations route the DBR# signal to a reset controller FPGA and a wire-OR function within the front-panel reset circuit

The pull-up value and location is not critical to the run-control tool but may be to the receiver or other drivers if this signal is wire-ORed.

26.3.3.8 XDP_Present

This optional steady-state output from the run-control hardware indicates the presence of an ITP-XDP-style tool at the debug port. To use this tool, the target system must provide a pull-up termination of 1k to 10k ohm to this signal. Termination voltage for this signal can be to any voltage that is compatible with the receiver chosen by the platform design.

When the ITP-XDP tool is present, the ITP-XDP tool will short this pin to ground.

26.3.4 I^{2}C (SDA/SCL) Routing Guidelines

The I^{2}C interface from the ITP-XDP includes two pins – SDA and SCL. Route the debug-port SDA pin to the SDA signal of the I^{2}C on the system. Route the debug port SCL pin to the SCL signal of the I^{2}C on the system. The I^{2}C ITP-XDP interface is master only and cannot be slave addressed. The I^{2}C ITP-XDP master can be connected to any multiple-master I^{2}C bus within the target system that provides access to the hooks required for validation and debug. The ITP-XDP conforms to the multi-master rules of the I^{2}C bus. The debug port has no additional requirements for termination on these signals beyond the I^{2}C specifications. The I^{2}C ITP-XDP is compatible with I^{2}C and SM Bus protocols.

There are no additional requirements for termination on these signals beyond the I^{2}C specifications.

26.3.5 Power

26.3.5.1 VCC_OBS Pins

The VCC_OBS_AB and VCC_OBS_CD pins are used by the ITP-XDP hardware to provide termination voltage to the OBS interface. Connect VCC_OBS_AB and VCC_OBS_CD to the voltage listed in the system-connection table. Decoupling capacitors are not required for these signals.

Each of these pins draws ~200mA of current.

26.3.5.2 Ground

All XDP ground signals must be tied directly to the system ground with little to no trace from the debug port.

26.4 System Connection

The XDP connector placed on the target system is a Samtec* 60-pin BSH-030-01 series connector. Specific plating types, locking clips, and alignment pins versions of this connector can be obtained from Samtec*. Table 95 documents the pinout for ITP-XDP connector.

Table 95.   XDP To EP80579 Signal Connections (Sheet 1 of 2)

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		2	GND	GND	NA	System
3	OBSFN_A0	BPM5_PREQ _IN	I/O	EP80579	4	OBSFN_C0	Open	NA	
5	OBSFN_A1	BPM4_PRDY _OUT	I/O	EP80579	6	OBSFN_C1	Open	NA	

Table 95.   XDP To EP80579 Signal Connections (Sheet 2 of 2)

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
7	GND	GND	NA	System	8	GND	GND	NA	System
9	OBSDATA_A[0]	BPM3	I	EP80579	10	OBSDATA_C[0]	Open	NA	
11	OBSDATA_A[1]	BPM2	I	EP80579	12	OBSDATA_C[1]	Open	NA	
13	GND	GND	NA	System	14	GND	GND	NA	System
15	OBSDATA_A[2]	BPM1	I	EP80579	16	OBSDATA_C[2]	Open	NA	
17	OBSDATA_A[3]	BPM0	I	EP80579	18	OBSDATA_C[3]	Open	NA	
19	GND	GND	NA	System	20	GND	GND	NA	System
21	OBSFN_B0	Open	NA		22	OBSFN_D0	BPM3_IN	O	EP80579
23	OBSFN_B1	Open	NA		24	OBSFN_D1	Open	NA	
25	GND	GND	NA	System	26	GND	GND	NA	System
27	OBSDATA_B[0]	Open	NA		28	OBSDATA_D[0]	Open	NA	
29	OBSDATA_B[1]	Open	NA		30	OBSDATA_D[1]	Open	NA	
31	GND	GND	NA	System	32	GND	GND	NA	System
33	OBSDATA_B[2]	Open	NA		34	OBSDATA_D[2]	Open	NA	
35	OBSDATA_B[3]	Open	NA		36	OBSDATA_D[3]	Open	NA	
37	GND	GND	NA		38	GND	GND	NA	System
39	PWRGOOD/HOOK0	PWRGOOD	I	System	40	ITPCLK/HOOK4	BCLK	I	System
41	TESTINb/HOOK1	Open	NA		42	ITPCLK#/HOOK5	BCLK#	I	System
43	VCC_OBS_AB	1.8V	NA	System	44	VCC_OBS_CD	1.8V	NA	System
45	HOOK2	PCICLK	I	System	46	RESET#/HOOK6	RESET#	I	System
47	HOOK3	CLK REF	I	System	48	DBR#/HOOK7	DBR#	O	System
49	GND	GND	NA	System	50	GND	GND	NA	System
51	SDA	SDA	I/O	System	52	TDO	TDO	I	EP80579
53	SCL	SCL	O	System	54	TRSTn	TRST#	O	EP80579
55	TCK1	Open	NA		56	TDI	TDI	O	EP80579
57	TCK0	TCK	O	EP80579	58	TMS	TMS	O	EP80579
59	GND	GND	NA	System	60	GND	XDP_PRESENT#	O	System

26.5   Mechanical Specifications

Figure 157 illustrates the target system volume that must be reserved for the ITP-XDP to attach to the target system. It is recommended that the main ITP-XDP enclosure be securely attached to the target system to avoid damage to the ITP-XDP and the target system. Four 1/8 inch mounting holes are provided on the ITP-XDP to facilitate attachment with screws or cable ties.

Figure 157. XDP Connector System Keep-Out Diagram
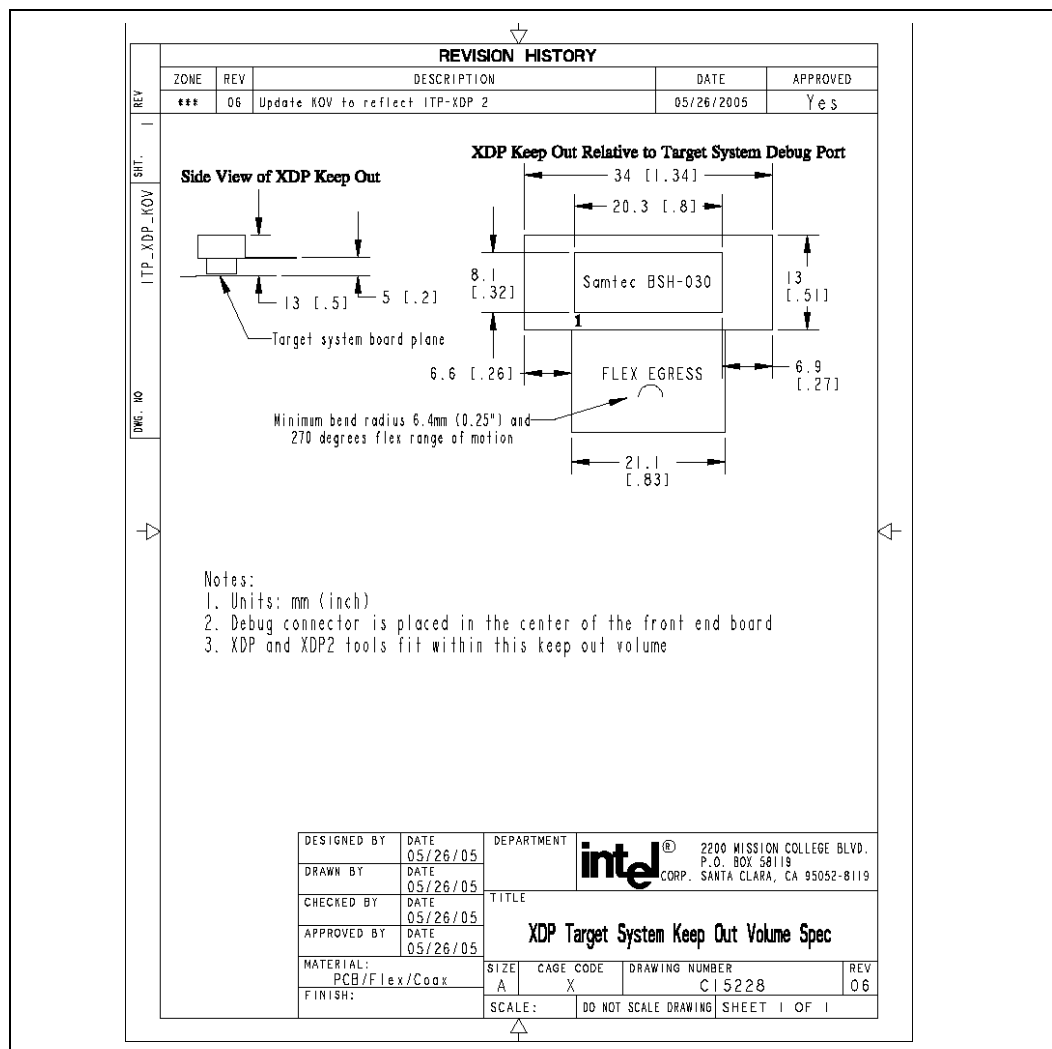
The placement of the XDP connector on the secondary side should be avoided if possible. Among other reasons, it should be avoided due to the complexity of hand placing and soldering the device. Cap all vias near the XDP-connector pads in compliance with the Intel DFM Guidelines for capped vias.

27.0 Layout Checklist

The layout checklist provides design considerations that should be reviewed prior to completing the layout and routing of EP80579-based platform designs. See the individual peripheral interface chapters in this document for more detailed routing guidelines for the platform board.

27.1 Functional Signal Definitions

Table 96 provides the legend for interpreting the IO Type field that appears throughout the tables in this section.

Table 96. Signal Type Definitions

Symbol	Description
#	Active low signal
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or output
OD	Open Drain pin
PWR	Power pin
GND	Ground pin
Reserved	Pin must be connected as described, where n is the reserved pin number
NCn	No Connection, where n is the NC pin number

27.2 Layout Checklist

Table 97. Layout Checklist (Sheet 1 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
IA-32 core Interface			
Global Clock Unit (CRU)			
CLKP100/CLKN100 or BCLKP/BCLKN	Zdiff = 100 Ω +/- 10% Trace Width – W Brakeout Trace Width 4 mils Microstrip: 4 mils Stripline: 3.75 mils(L3/L8) Stripline: 4.25 mils(L5/L6) Brakeout Trace Width 4 mils Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 6 mils Stripline: 9 mils Spacing between Pairs 20mils Spacing to other signals 20 mils Serpentine Spacing 20 mils	Routing Length LT: Min = 1 in. Max = 10 in. Inter-Pair length matching: +/- 5 mils	See Section 8.2.1.1, "HOST_CLK Topology".
Thermal Diode			
THERMDA THERMDC	Recommended Trace Width: Trace width = 10 mils. Spacing to other signals 1 X trace width.		Remote sensor should place as close as possible to THERMDA and THERMDC, approximately 4 to 8" away from the noise sources. Route the THERMDA and THERMDC lines parallel and close together with ground guards enclosing them.
Sideband Miscellaneous Signals			
CPUSLP_OUT#	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
INIT33V_OUT#	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
NMI	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
SMI_OUT#	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
STPCLK_OUT#	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
RCIN#	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
A20GATE	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		

Table 97.   Layout Checklist (Sheet 2 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
CPURST#	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
CPUPWRGD_OUT	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
BSEL	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
V_SEL	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
Integrated Memory Controller Hub (IMCH) Interface			
IMCH Reset			
RSTIN#	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
PWRGD	Zo = 50 Ω +/- 10% Spacing to other signals 3 X trace width.		
DDR2 SDRAM			
DDR_DQ[63:0], DDR_ECC[7:0], DDR_DM[8:0], DDR_DQS[8:0], DDR_ DQS[8:0]#	Zo = 40 Ω +/- 10% single ended Trace Width: Brakeout Trace Width 4 mils Stripline: 6.5 mils(L3/L8) Airgap Spacing: Brakeout spacing Min=4mils DDR_DQ/DDR_ECC/DDR_DM Min=15 mils DDR_DQS to DDR_DQS# 6 mils DDR_DQS Pair to Pair Min=20mils To any other signals Min=20mils	EP80579 to First DIMM 2.0 in to 4.0 in Max First to Second DIMM Max=0.8 in Total Trace Length (TTL) 2.0 in - 6.0 in DDR_DQS to DDR_DQS# Match within 10 mils Skew: Match all group signals within 20 mils for the same byte group. The shortest signal of the group must not exceed the longest signal of the byte group by 20 mils. This requirement is for the complete length from EP80579 to the farthest DIMM connector.	See Section 9.7, "DDR2 Interface System Interconnect". Topology Daisy Chain Reference Plane: Ground and Power reference plane Route groups of signals on the same layer from EP80579 to the farthest DIMM. No vias, except were required to breakout. Direct connection from EP80579 to each DIMM with no termination.

Table 97.   Layout Checklist (Sheet 3 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
DDR_A[14:0], DDR_BA[2:0], DDR_RAS#, DDR_CAS#, DDR_WE#	Zo = 40 Ω +/- 10% single ended Trace Width: Brakeout Trace Width 4 mils Stripline: 6.5 mils(L3/L8) Airgap Spacing: Brakeout spacing Min=4 mils Between group signals Min=15mils To any other signals Min=20mils	EP80579 to First DIMM 2.0 in to 4.0 in Max First to Second DIMM Max=0.8 in Total Trace Length (TTL) 2.0 in - 6.0 in Termination Trace Length Max = 0.5 in. Skew between Termination Trace Length should not exceed 200 mils. Skew: Match all group signals within 20 mils. The shortest signal of the group must not exceed the longest signal of the group by 20 mils. This requirement is for the complete length from EP80579 to the farthest DIMM connector.	See Section 9.7, "DDR2 Interface System Interconnect". Topology Daisy Chain Reference Plane: Ground and Power reference plane Route groups of signals on the same layer from EP80579 to the farthest DIMM. No vias, except were required to breakout. Place Ccomp caps as close as possible to the DIMM
DDR_CS[1:0]#, DDR_CKE[1:0], DDR_ODT[1:0]	Zo = 40 Ω +/- 10% single ended Trace Width: Brakeout Trace Width 4 mils Stripline: 6.5 mils(L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Between group signals Min=15mils To any other signals Min=20mils	EP80579 to First DIMM 2.0 in to 4.0 in Max First to Second DIMM Max=0.8 in Total Trace Length (TTL) 2.0 in - 6.0 in Termination Trace Length Max = 0.5 in. Skew between Termination Trace Length should not exceed 200 mils. Skew: Match all group signals within 20 mils. The shortest signal of the group must not exceed the longest signal of the group by 20 mils. This requirement is for the complete length from EP80579 to the farthest DIMM connector.	See Section 9.7, "DDR2 Interface System Interconnect". Topology Daisy Chain Reference Plane: Ground and Power reference plane Route groups of signals on the same layer from EP80579 to the farthest DIMM. No vias, except were required to breakout.

Table 97.   Layout Checklist (Sheet 4 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
DDR_CK[5:0], DDR_CK[5:0]#	Zo = 40 Ω +/- 10% single ended Trace Width: Brakeout Trace Width 4 mils Stripline: 6.5 mils(L3/L8) Airgap Spacing: Brakeout spacing Min=4mils DDR_CK to DDR_CK# 6mils Pair to Pair Min=15mils To any other signals Min=20mils	EP80579 to First DIMM 2.0 in to 4.0 in Max Total Trace Length (TTL) 2.0 in - 6.0 in DDR_CK to DDR_CK# Match within 10 mils Skew: Match all pair to pair group within 20 mils. The shortest pair of the group must not exceed the longest pair of the group by 20 mils. This requirement is for the complete length from EP80579 to the farthest DIMM connector. DDR_CK/DDR_CK# Clock pairs should be match in length to CMD/ADDR within 20 mils	See Section 9.7, "DDR2 Interface System Interconnect". Topology Point to Point Groups are defined as follow: First group CLK/CLK#[2:0] Second group CLK/CLK#[5:3] Reference Plane: Ground and Power reference plane. Route Clock group on the same layer from EP80579 to the farthest DIMM. No vias, except were required to breakout.
DDR_CRES[0], DDR_SLWCRES, DDR_DRVCRES DDR_RCOMPX	Trace Width: Brakeout Trace Width 4 mils Other routing 20 mils Airgap Spacing: Brakeout spacing Min=4mils To any other signals Min=12mils	Total Trace Length (TTL) Max=500mils	Keep traces as short as possible.
DDR_CRES[1], DDR_CRES[2]	Trace Width: Brakeout Trace Width 4 mils Other routing 20 mils Airgap Spacing: Brakeout spacing Min=4mils To any other signals Min=12mils	Total Trace Length (TTL) Max=500mils	Keep traces as short as possible. Place the RC circuit as close as possible to EP80579.
PCI Express Interface			
PEA0_Tp[7:0], PEA0_Tn[7:0]	Zdiff = 90 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 4.75 mils Stripline: 4.5 mils (L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 5.25 mils Stripline: 5.5 mils Spacing between Pairs, the greater of the two Microstrip: 20 mils or 3X dielectric thickness. Stripline: 18 mils or 3X dielectric thickness.	Inter-pair length matching: +/-5 mils. Within a link, the lane-to-lane skew should meet the PCIe transmit skew (tx-skew) specification.	See Section 10.1.7, "Topology 1 – EP80579 to PCI Express Connector". Interface System Interconnect. Maximum number of vias per signal is 4.

Table 97.   Layout Checklist (Sheet 5 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
PEA0_Rp[7:0], PEA0_Rn[7:0]	Zdiff = 90 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 4.75 mils Stripline: 4.5 mils (L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 5.25 mils Stripline: 5.5 mils Spacing between Pairs, the greater of the two Microstrip: 20 mils or 3X dielectric thickness. Stripline: 18 mils or 3X dielectric thickness.	Inter-pair length matching: +/-5 mils. Within a link, the lane-to-lane skew should meet the PCIe receive skew (rx-skew) specification.	See Section 10.1.7, "Topology 1 – EP80579 to PCI Express Connector". Maximum number of vias per signal is 4.
PEA_CLKp, PEA_CLKn	Zdiff = 100 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 4 mils Stripline: 3.75 mils(L3/L8) Stripline: 4.25 mils(L5/L6) Airgap Spacing: Brakeout spacing Min=4mils PEA_CLKp to PEA_CLKn Microstrip: 6 mils Stripline: 9 mils Spacing to other signals 20 mils Serpentine Spacing 20 mils	Inter-pair length matching: +/- 5 mils	See Section 8.2.2, "CLK100 (SRC Clock) Group". Maximum number of vias per signal is 4.
PEA_ICOMPI, PEA_ICOMPO, PEA_RCOMPO	Zo = 50 Ω +/- 10%		
PE_HPINTR#	Zo = 50 Ω +/- 10%		
Integrated I/O Controller Hub (IICH) Interface			
Real Time Clock (RTC)			
RTCX1, RTCX2	Zo = 50 Ω +/- 10% Trace Width: Microstrip: 5.5 mils Airgap Spacing Microstrip: 9 mils Spacing to other signals 2 X	Routing Length LT: Max = 1.2 in.	See Section 15.1.1, "RTC Crystal". Avoiding routing of adjacent PCI signals close to RTCX1 and RTCX2. Use of a ground guard plane is highly recommended. Put GND plane underneath Crystal components. Minimize capacitance between RTCX1 and RTCX2. Don't route switching signals under the external components (unless on other side of board).
RTEST#	Zo = 50 Ω +/- 10%		
General Purpose I/O (GPIO) and Interrupts Interface			
GPIO[1:0]	Zo = 50 Ω +/- 10%		
GP2_PIRQE#	Zo = 50 Ω +/- 10%		

Table 97.   Layout Checklist (Sheet 6 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
GP3_PIRQF#	Zo = 50 Ω +/- 10%		
GP4_PIRQG#	Zo = 50 Ω +/- 10%		
GP5_PIRQH#	Zo = 50 Ω +/- 10%		
GPIO[10:6]	Zo = 50 Ω +/- 10%		
GP11_SMBALERT#	Zo = 50 Ω +/- 10%		
GPIO[21:12]	Zo = 50 Ω +/- 10%		
GPIO[25:23]	Zo = 50 Ω +/- 10%		
GP26_SATA0GP	Zo = 50 Ω +/- 10%		
GPIO[28:27]	Zo = 50 Ω +/- 10%		
GP29_SATA1GP	Zo = 50 Ω +/- 10%		
GPIO[31:30]	Zo = 50 Ω +/- 10%		
GPIO[34:33]	Zo = 50 Ω +/- 10%		
GPIO[40]	Zo = 50 Ω +/- 10%		
GP41_LDRQ[1]#	Zo = 50 Ω +/- 10%		
GPIO[48]	Zo = 50 Ω +/- 10%		
IICH Interrupts			
SERIRQ	Zo = 50 Ω +/- 10%		
Low Pin Count (LPC) Interface			
LAD[3:0], LFRAME#	Zo = 50 Ω +/- 10%		
LDRQ[0]# GP41_LDRQ[1]#	Zo = 50 Ω +/- 10%		
PCICLK	Zo = 55 Ω +/- 10% Trace Width: Microstrip: 4.5 mils Stripline: 3.75 mils (L3/L8) Airgap Spacing: Spacing to other signals 20 mils	Routing Length LT: LT = 2 in - 20 in.	
Serial Peripheral Interface (SPI) - System BIOS Topology			
SPI_MOSI	Zo = 50 Ω +/- 10% Trace Width: Microstrip: 4.5 mils Stripline: 3.75 mils (L3/L8) Airgap Spacing: Spacing to other signals 7 mils	Routing Length LT: Max = 16 in.	See Section 16.2.1, "SPI Routing Guidelines". Place pull resistor close to the SPI Flash device.
SPI_MISO	Zo = 50 Ω +/- 10% Trace Width: Microstrip: 4.5 mils Stripline: 3.75 mils (L3/L8) Airgap Spacing: Spacing to other signals 7 mils	Routing Length LT: Max = 16 in.	See Section 16.2.1, "SPI Routing Guidelines". Place pull resistor close to the SPI Flash device.

Table 97.   Layout Checklist (Sheet 7 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
SPI_CS#	Zo = 50 Ω +/- 10% Trace Width: Microstrip: 4.5 mils Stripline: 3.75 mils (L3/L8) Airgap Spacing: Spacing to other signals 7 mils	Routing Length LT: Max = 16 in.	See Section 16.2.1, "SPI Routing Guidelines". Place pull resistor close to the SPI Flash device.
SPI_CLK	Zo = 50 Ω +/- 10% Trace Width: Microstrip: 4.5 mils Stripline: 3.75 mils (L3/L8) Airgap Spacing: Spacing to other signals 7 mils	Routing Length LT: Max = 16 in.	See Section 16.2.1, "SPI Routing Guidelines". Place pull resistor close to the SPI Flash device.
System Management Bus (SMBus) Interface			
SMBSDA, SMBSCL	Zo = 50 Ω +/- 10%		
INTRUDER#	Zo = 50 Ω +/- 10%		
SMLINK[1:O]	Zo = 50 Ω +/- 10%		
SMBALERT#	Zo = 50 Ω +/- 10%		
Serial Interface Unit (UART) Interface			
SIU_RXD[2:1] SIU_TXD[2:1] SIU_CTS[2:1]# SIU_DSR[2:1]# SIU_DCD[2:1]# SIU_RI[2:1]# SIU_DTR[2:1]# SIU_RTS[2:1]#	Zo = 50 Ω +/- 10%		
UART_CLK	Zo = 50 Ω +/- 10%	Place the 33 Ω ± series resistor as close as possible to the source.	Isolate UART_CLK from USB_CLK (CLK48) through the series resistors
Serial ATA (SATA) Interface			
SATA_TXp[1:0] SATA_TXn[1:0] SATA_RXp[1:0] SATA_RXn[1:0]	Zdiff = 90 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 4.75 mils Stripline: 4.5 mils (L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 5.25 mils Stripline: 5.5 mils Spacing between Pairs, the greater of the two Microstrip: 25 mils Stripline: 20 mils	Breakout L1: Max = 0.40 in. Length L2: Microstrip Min=1.5 in, Max=5.75 in Strip Line Min=1.15 in, Max=4.75 in Length L3 Max=0.350 in Inter-pair length matching: +/- 5 mils	See Section 11.2, "SATA Transmit and Receive Signals – SATA_TXp[1:0], SATA_TXn[1:0], SATA_RXp[1:0], SATA_RXn[1:0]". It is recommended to place the AC coupling capacitors close to the connector for optimal signal quality. 2 Vias Max
SATA_RBIAS SATA_RBIAS#	Zo = 50 Ω +/- 10%	Routing Length LT: Max = 0.5 in.	Place the RBIAS (resistor bias) as close as possible to EP80579.

Table 97. Layout Checklist (Sheet 8 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
SATA_CLKREFp, SATA_CLKREFn	Zdiff = 100 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 4 mils Stripline: 3.75 mils (L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 6 mils Stripline: 9 mils Spacing between Pairs 20mils Spacing to other signals 20 mils Serpentine Spacing 20 mils	Routing Length LT: Min = 1 in. Max = 16 in. Inter-pair length matching: +/- 5 mils	See Section 8.2.2, "CLK100 (SRC Clock) Group". 2 Vias Max
SATALED#	Zo = 50Ω +/- 10%		
SATA0GP (GP26_SATA0GP) See General Purpose I/O (GPIO) Interface			
SATA1GP (GP29_SATA1GP) See General Purpose I/O (GPIO) Interface			
Universal Serial Bus (USB) Interface			
USBp[1:0], USBn[1:0]	Zdiff = 90 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 4.75 mils Stripline: 4.5 mils Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 5.25 mils Stripline: 5.5 mils Spacing between Pairs Min = 45mils Spacing to clock signals Min = 45mils Spacing to non clock signals Min = 45mils	Breakout: Max = 400mils. Board Length: Microstrip 2-11 in. Strip Line 2-10 in. Inter-pair length matching Max = 60 mils skew	See Section 12.2.2, "USB Differential Signals – USBp[1:0], USBn[1:0]". Keep all traces as short as possible. Choke must be placed as close as possible to the connector.
OC[1:0]#	Zo = 50 Ω +/- 10%		• See Section 12.2.5, "USB Over Current protection – OC[1:0]#".
USB_RBIASp USB_RBIASn	Zo = 50 Ω +/- 10%	Length LT: Max = 0.5 in.	• See Section 12.2.3, "USB_RBIASp/USB_RBIASn Connection". • Place the 22.6 Ω resistor within 0.5 in. of the EP80579.
CLK48	Zo = 50 Ω +/- 10% Trace Width Microstrip: 5.5 mils Stripline: 4.5 mils (L3) Airgap Spacing: Spacing to other signals Min = 20mils Spacing to non clock signals Min = 45mils	Length LT: 2 to 20 in	Place damping resistor as close as possible to the source.
Power Management Interface			
PLTRST#	Zo = 50 Ω +/- 10%		
PROCHOT#	Zo = 50 Ω +/- 10%		

Table 97.   Layout Checklist (Sheet 9 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
THRMTRIP#	Zo = 50 Ω +/- 10%		
SLP_S3#	Zo = 50 Ω +/- 10%		
SLP_S4#	Zo = 50 Ω +/- 10%		
SLP_S5#	Zo = 50 Ω +/- 10%		
PWROK	Zo = 50 Ω +/- 10%		
PWRBTN#	Zo = 50 Ω +/- 10%		
RI#	Zo = 50 Ω +/- 10%		
SYS_RESET#	Zo = 50 Ω +/- 10%		
RSMRST#	Zo = 50 Ω +/- 10%		
SUS_STAT#	Zo = 50 Ω +/- 10%		
SUSCLK	Zo = 50 Ω +/- 10%		
VRMPWRGD	Zo = 50 Ω +/- 10%		
IERR#	Zo = 50 Ω +/- 10%		
IICH Miscellaneous Signals			
CLK14	Zo = 50 Ω +/- 10% Trace Width: Microstrip: 5.5 mils Stripline: 4.5 mils (L8) Airgap Spacing: Spacing to other signals Min = 10mils Spacing to non clock signals Min = 10mils	Breakout: Max = 500mils. Length LT: Max = 18 in.	Place damping resistor as close as possible to the source.
WDT#	Zo = 50 Ω +/- 10%		
Acceleration and I/O Complex (AIOC)			
Controller Area Network (CAN) Interface			
CAN0TXD, CAN1TXD	Zo = 50 Ω +/- 10%		
CAN0TXEN, CAN1TXEN	Zo = 50 Ω +/- 10%		
CAN0RXD, CAN1RXD	Zo = 50 Ω +/- 10%		
Gigabit Ethernet (GbE) Interface			
GBE0_TxCLK, GBE1_TxCLK, GBE2_TxCLK	Zo = 55 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 4.5 mils Stripline: 3.75 mils (L3/L8) 5 mils (L5/L6) Airgap Spacing: Brakeout spacing Min=4mils Spacing to other clock signals Stripline Min = 20mils Microstrip Min = 25mils	Breakout: EP80579 Max = 500mils. PHY Max = 300mils. Total Clock Routing: Microstrip 1.5 to 7.8 in Stripline 1 to 7.8 in. Pull Up Trace Length Max=0.4 in.	See Section 19.6.1.1, "GbE Transmit Clock Topology". Place pull-up resistors close to PHY device

Table 97.   Layout Checklist (Sheet 10 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
GBE0_TxDATA[3:0] GBE1_TxDATA[3:0] GBE2_TxDATA[3:0], GBE0_TxCTL, GBE1_TxCTL, GBE2_TxCTL	Zo = 55 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 4.5 mils Stripline: 3.75 mils (L3/L8) 5 mils (L5/L6) Airgap Spacing: Brakeout spacing Min=4mils Spacing between Data\Control Stripline Min = 12mils Microstrip Min = 18mils	Breakout: EP80579 Max = 500mils. PHY Max = 300mils. Total Data Routing: +/- 50 mils of Total Clock Routing. Pull Up Trace Length Max=0.4 in.	See Section 19.6.1.2, "GbE Transmit Data\Control Topology". Place pull-up resistors close to PHY device.
GBE0_RxCLK, GBE1_RxCLK, GBE2_RxCLK	Zo = 50 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 5.5 mils Stripline: 4.5 mils (L3/L8) 6 mils (L5/L6) Airgap Spacing: Brakeout spacing Min=4mils Spacing to other clock signals Stripline Min = 20mils Microstrip Min = 25mils	Breakout: EP80579 Max = 500mils. PHY Max = 300mils. Total Clock Routing: Microstrip 1 to 7.8 in Stripline 1 to 7.8 in. Pull Up Trace Length Max=0.625 in.	See Section 19.6.2.1, "GbE Receive Clock Topology". Place pull-up resistors close to EP80579 device.
GBE0_RxDATA[3:0] GBE1_RxDATA[3:0] GBE2_RxDATA[3:0] GBE0_RxCTL, GBE1_RxCTL, GBE2_RxCTL	Zo = 50 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 5.5 mils Stripline: 4.5 mils (L3/L8) 6 mils (L5/L6) Airgap Spacing: Brakeout spacing Min=4mils Spacing between Data\Control Stipline Min = 12mils Microstrip Min = 18mils	Breakout: EP80579 Max = 500mils. PHY Max = 300mils. Total Data Routing: +/- 50 mils of Total Clock Routing. Pull Up Trace Length Max=0.625 in.	See Section 19.6.2.2, "GbE Receive Data\Control Topology". Place pull-up resistors close to EP80579 device.
MDC	Zo = 50 Ω +/- 10%		
MDIO	Zo = 50 Ω +/- 10%		• See Section 19.5.1, "GbE Ethernet Interface — RGMII Mode".
GBE_REFCLK	Zo = 50 Ω +/- 10%		
GBE_REFCLK_RMII	Zo = 50 Ω +/- 10%		
GBE_RCOMPP	Zo = 50 Ω +/- 10%		Place the RCOMPP resistor as close as possible EP80579.
GBE_RCOMPN	Zo = 50 Ω +/- 10%		Place the RCOMPN resistor as close as possible EP80579.
EEDO	Zo = 50 Ω +/- 10%		
EEDI	Zo = 50 Ω +/- 10%		
EECS	Zo = 50 Ω +/- 10%		
EESK	Zo = 50 Ω +/- 10%		
GBE_PME_WAKE	Zo = 50 Ω +/- 10%		

Table 97.   Layout Checklist (Sheet 11 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
SYS_PWR_OK	Zo = 50 Ω +/- 10%		
GBE_AUX_PWR_GOOD	Zo = 50 Ω +/- 10%		
Time Division Multiplexing (TDM) Interface			
Note: Certain EP80579 SKUs may not contain this feature. Feature must be enabled with EP80579 Software. See EP80579 "SKU Features" in the EP80579 Software Documentation for detailed Information			
Rx_CLK[2:0]	Zo = 50 Ω +/- 10%		
Tx_CLK[2:0]	Zo = 50 Ω +/- 10%		
Tx_FRAME[2:0]	Zo = 50 Ω +/- 10%		
Tx_DATA_OUT[2:0]	Zo = 50 Ω +/- 10%		
Rx_FRAME[2:0]	Zo = 50 Ω +/- 10%		
Rx_DATA_IN[2:0]	Zo = 50 Ω +/- 10%		
Local Expansion Bus (LEB) Interface			
EX_ADDR[24:0]	Zo = 50 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 5.5 mils Stripline: 4.5 mils (L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 12 mils Stripline: 10 mils	Breakout: Max = 1 in. Breakin: Max = 1 in. Length: LADDR_Total = LCS_Total +/-500mils, Not to exceed 16 inch at 33 MHz	See Section 22.3.3, "Address Star Topologies".
EX_CLK	Zo = 55 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 5.5 mils Stripline: 4.5 mils (L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 12 mils Stripline: 10 mils	Breakout: Max = 1 in. Breakin: Max = 1 in.	See Section 8.2.3, "CLK33 Group".
EX_CS[7:0]#	Zo = 50 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 5.5 mils Stripline: 4.5 mils (L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 12 mils Stripline: 10 mils	Breakout: Max = 1 in. Breakin: Max = 1 in. Length: LCS_Total = 16 in. (Max)	See Section 22.3.2, "Chip Select Topologies".

Table 97. Layout Checklist (Sheet 12 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
EX_DATA[15:0]	Zo = 50 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 5.5 mils Stripline: 4.5 mils (L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 12 mils Stripline: 10 mils	Breakout: Max = 1 in. Breakin: Max = 1 in. Length: LDC_Total = LCS_Total +/-500mils, Not to exceed 16 inch at 33 MHz	See Section 22.3.4, "Data and Control Star Topology".
EX_RD# EX_WR# EX_BE[1:0]# EX_RDY[3:0]# EX_PARITY[1:0]	Zo = 50 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 5.5 mils Stripline: 4.5 mils (L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 12 mils Stripline: 10 mils	Breakout: Max = 1 in. Breakin: Max = 1 in. Length: LDC_Total = LCS_Total +/-500mils, Not to exceed 16 inch at 33 MHz	See Section 22.3.4, "Data and Control Star Topology".
EX_ALE EX_BURST EX_IOWAIT#	Zo = 50 Ω +/- 10% Trace Width: Brakeout Trace Width 4 mils Microstrip: 5.5 mils Stripline: 4.5 mils (L3/L8) Airgap Spacing: Brakeout spacing Min=4mils Microstrip: 12 mils Stripline: 10 mils	Breakout: Max = 1 in. Breakin: Max = 1 in. Length: Not to exceed 16 inch at 33 MHz	See Section 22.3.4, "Data and Control Star Topology".
EX_RCOMPP	Zo = 50 Ω +/- 10%	Routing Length LT: Max = 0.5 in.	Place the RCOMPP (compensation resistor) as close as possible to EP80579.
EX_RCOMPN	Zo = 50 Ω +/- 10%	Routing Length LT: Max = 0.5 in.	Place the RCOMPN (compensation resistor) as close as possible to EP80579.
Synchronous Serial Port (SSP) Interface			
SSP_SCLK	Zo = 50 Ω +/- 10%		
SSP_SFRM	Zo = 50 Ω +/- 10%		
SSP_TXD	Zo = 50 Ω +/- 10%		
SSP_RXD	Zo = 50 Ω +/- 10%		
SSP_EXTCLK	Zo = 50 Ω +/- 10%		
IEEE 1588 Hardware-Assist Interface			
TS_TESTMODE_DATA	Zo = 50 Ω +/- 10%		
TS_PPS	Zo = 50 Ω +/- 10%		
ASMSSIG	Zo = 50 Ω +/- 10%		
AMMSSIG	Zo = 50 Ω +/- 10%		
TSYNC_RX_SNAP	Zo = 50 Ω +/- 10%		

Table 97.   Layout Checklist (Sheet 13 of 13)

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
TSYNC_TX_SNAP	Zo = 50 Ω +/- 10%		
Miscellaneous I/O Interface			
JTAG			
TMS	Zo = 50 Ω +/- 10%		See Section 26.3.1, "JTAG Routing Guidelines".
TDI	Zo = 50 Ω +/- 10%		See Section 26.3.1, "JTAG Routing Guidelines".
TDO	Zo = 50 Ω +/- 10%		See Section 26.3.1, "JTAG Routing Guidelines".
TCK	Zo = 50 Ω +/- 10%		See Section 26.3.1, "JTAG Routing Guidelines".
TRST#	Zo = 50 Ω +/- 10%		See Section 26.3.1, "JTAG Routing Guidelines".
BPM3_IN	Zo = 50 Ω +/- 10%		See Section 26.3.1, "JTAG Routing Guidelines".
BPM4_PRDY_OUT	Zo = 50 Ω +/- 10%		See Section 26.3.1, "JTAG Routing Guidelines".
BPM5_PREQ_IN	Zo = 50 Ω +/- 10%		See Section 26.3.1, "JTAG Routing Guidelines".
BPM[3:0]	Zo = 50 Ω +/- 10%		See Section 26.3.1, "JTAG Routing Guidelines".
Miscellaneous Pins			
PME#	Zo = 50 Ω +/- 10%		
PCIRST#	Zo = 50 Ω +/- 10%		
SPKR	Zo = 50 Ω +/- 10%		
Reserved Pins			
Reserved[20:0]	Zo = 50 Ω +/- 10%		
No Connect Pins **Note:** (All No Connect Pins should be left un-connected)			
NC_SUS_TWO	Zo = 50 Ω +/- 10%		
NC_TWO	Zo = 50 Ω +/- 10%		
NC7	Zo = 50 Ω +/- 10%		
NC[22:9]	Zo = 50 Ω +/- 10%		
NC[38:34]	Zo = 50 Ω +/- 10%		
NC[48:40]	Zo = 50 Ω +/- 10%		
NC[57:50]	Zo = 50 Ω +/- 10%		

27.3   CK410 Layout Checklist

For additional information, see the *CK410 Clock Synthesizer/Driver Specification* and the component's datasheet.

Table 98. **CK410 Schematic Checklist**

Signal Name	Trace Geometry and Impedance	Length Requirements	Comments
Note: See CK410 Clock Synthesizer/Driver Specification for more details			
PCIF_0/ITP_EN	Zo = 50 Ω +/- 10%		
PCIF_1, PCIF_2	Zo = 50 Ω +/- 10%		
SRC[6:1]/ SRC[6:1]#	Zo = 50 Ω +/- 10%		
DOT96/DOT96#	Zo = 50 Ω +/- 10%		
PCI[5:0]	Zo = 50 Ω +/- 10%		
CPU[1:0]/ CPU[1:0]#	Zo = 50 Ω +/- 10%		
CPU_2/SRC_7, CPU_2#/SRC_7#	Zo = 50 Ω +/- 10%		
FS_A	Zo = 50 Ω +/- 10%		
FS_B/ TEST_MODE	Zo = 50 Ω +/- 10%		
FS_C/TEST_SEL	Zo = 50 Ω +/- 10%		
REF	Zo = 50 Ω +/- 10%		
IREF	Zo = 50 Ω +/- 10%		
XTAL_IN/ XTAL_OUT	Zo = 50 Ω +/- 10%		• Connect to a 14.318-MHz crystal, placed within 500 mils of CK410 device.
VTT_PWRGD#/ PD	Zo = 50 Ω +/- 10%		• Connect to Platform VRMPWRGD signal after a 2ms delay. • VTT_PWRGD# is a 3.3V LVTTL input. It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs. After VTT_PWRGD# assertiion, it becomes a real time input for asserting power down.
VDD_PCI[1:0], VDD_CPU, VDD_SRC[3:1], VDD_REF, VDD_48, VDD_A			CK410 Power Pins • Connect to VCC3 • See Section 8.3.4, "CK410 Power Plane Filtering" for Power Filtering and Decoupling guidelines.
VSS_48, VSS_SRC, VSS_CPU, VSS_PCI[1:0], VSS_REF VSS_A			CK410 Ground Pins • Connect to GND • See Section 8.3.4, "CK410 Power Plane Filtering" for Ground Filtering and Decoupling guidelines.

28.0 Schematics Checklist

The schematic checklist provides design recommendations and guidance for the development of EP80579-based platform designs. See the individual peripheral interface chapters in this document for further details.

Note: Some of the information in this document may not be applicable if a customer design implementation deviates from what was implemented in the Development Board.

28.1 Functional Signal Definitions

Table 99 provides the legend for interpreting the I/O Type field that appears throughout the tables in this section.

Table 99. Signal Type Definitions

Symbol	Description
#	Active low signal
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or output
OD	Open Drain pin
PWR	Power pin
GND	Ground pin
Reserved	Pin must be connected as described, where n is the reserved pin number
NCn	No Connection, where n is the NC pin number

28.2   Schematic Checklist

Table 100.   Schematic Checklist (Sheet 1 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
IA-32 core Interface			
Global Clock Unit (CRU)			
CLKP100	I	Differential positive 100 MHz IA-32 core clock input. • Connect from CK410 Clock Generator CPU_0 output through a 33 Ω ±5% series resistor. • Terminate to GND through a 49.9 Ω ±1% resistor.	Differential (Positive) System Bus Clock Signal
CLKN100	I	Differential negative 100 MHz IA-32 core clock input. • Connect from CK410 Clock Generator CPU_0# output through a 33 Ω ±5% series resistor. • Terminate to GND through a 49.9Ω ±1% resistor	Differential (Negative) System Bus Clock Signal
Thermal Diode			
THERMDA	I	• Connect to Anode of Thermal Diode of temperature monitoring circuitry if used.	• The Development Board monitors the temperature of the EP80579 device via the SuperIO chip. • Couple THERMDA and THERMDC signals together using 100 pF 5% 50V capacitor. • Route signals as differential pairs. ***Note:*** • These signals are used to monitor and control the EP80579 CPU temperature. It is used to control the fan speeds of the EP80579 heat sink. If this feature is not used, the heat sink fan can be connected to operate at a constant speed, and these signals can be left as no connect (NC)
THERMDC	O	• Connect to Cathode of Thermal Diode of temperature monitoring circuitry if used.	
Sideband Miscellaneous Signals			
CPUSLP_OUT#	O	• Can monitor signal using an LED • Pull up signal to Platform 3.3V (VCC3) power supply using 4.7KΩ ± 5% resistor if used.	***Note:*** • This signal can be left as a no connect (NC) if not used. • This signal can be exposed via a testpoint for debug purposes if not used.
INIT33V_OUT#	O	• Connect to FWH INT# pin. • Pull up signal to Platform 3.3V (VCC3) power supply using 4.7KΩ ± 5% resistor if used. • This signal can be monitored via an LED	***Note:*** • This signal can be left as a no connect (NC) if not used. • This signal can be exposed via a testpoint for debug purposes if not used.

Table 100.   Schematic Checklist (Sheet 2 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
NMI	I/O	• Terminate to GND using 10KΩ ± 5% resistor if used.	*Note:* • This signal should be pulled-down to GND with a 10KΩ resistor if not used
SMI_OUT#	O	• Pull up signal to Platform 3.3V (VCC3) using a 10KΩ ± 5% resistor if used	*Note:* • This signal can be left as a no connect (NC) if not used. • This signal can be exposed via a testpoint for debug purposes if not used.
STPCLK_OUT#	O	• Can monitor signal using an LED • Pull up signal to Platform 3.3V (VCC3) using a 10KΩ ± 5% resistor if used	*Note:* • This signal can be left as a no connect (NC) if not used. • This signal can be exposed via a testpoint for debug purposes if not used.
RCIN#	I	• Connect to Keyboard Reset (KBDRST#) pin of the Keyboard Controller provided by the Super I/O device. • Pull up signal to Platform 3.3V (VCC3) using a 10KΩ ± 5% resistor.	*Note:* • This signal should be pull-up to 3.3V with a 10KΩ resistor if not used
A20GATE	I	• Connect to A20M pin of the Keyboard Controller provided by the Super I/O device. • Pull up signal to Platform 3.3V (VCC3) power supply using 10KΩ ± 5% resistor	• Provides an alternative method to assert A20M#. *Note:* • This signal should be pull-up to 3.3V with a 10KΩ resistor if not used.
CPURST#	O	• Processor reset output signal that can be used by a debug tool. • Pull up signal to Platform 3.3V (VCC3) using a 10KΩ ± 5% resistor if used	• Processor Bus Reset: The IMCH asserts CPURST# while RSTIN# is asserted and for approximately 1ms after RSTIN# is deasserted. The CPURST# allows the processor to begin execution in a known state. *Note:* • This signal can be left as a no connect (NC) if not used. • This signal can be exposed via a testpoint for debug purposes if not used.
CPUPWRGD_OUT	O (OD)	• Processor Internal Power Good output signal that can be used by a debug tool. • Pull up signal to EP80579 3.3V (VCC33) using a 10KΩ ± 5% resistor.	• CPU Power Good: This EP80579 output signal is made visible to the platform for debug purposes only. This signal is an open drain signal, and requires an external pull-up resistor. CPUPWRGD monitors an internal signal connected directly form the IICH to the processor and represents a logical AND of PWROK and VRMPWRGD signals. *Note:* • Pull up signal to EP80579 3.3V (VCC33) using a 10KΩ ± 5% resistor if not used. • This signal can be exposed via a testpoint for debug purposes if not used.

Table 100. Schematic Checklist (Sheet 3 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
IERR#	O	• Connect to GPIO[40] to be used as IOAPIC IRQ35 • Pull-up to EP80579 3.3V (VCC33) power supply using 10KΩ ± 5% if used. • Can monitor signal using an LED	IERR# (EP80579 Internal Error) is asserted by the IA-32 core as a result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (for example, NMI) by EP80579. The IA-32 core keeps IERR# asserted until the assertion of INIT33V_OUT# or EP80579 is reset using SYS_RESET#. *Note:* • This signal can be left as a no connect (NC) if not used. • This signal can be exposed via a testpoint for debug purposes if not used.
Integrated Memory Controller Hub (IMCH) Interface			
IMCH Reset			
RSTIN#	I	• Connects to EP80579 PLTRST# output	• 50KΩ internal pull-up.
PWRGD	I	• Connects to Platform SYS_PWR_OK	
DDR2 SDRAM			
DDR_DQ[63:0], DDR_ECC[7:0], DDR_DM[8:0], DDR_DQS[8:0], DDR_ DQS[8:0]#	I/O	• Directly connect from EP80579 to each DIMM with no termination. • For 32-bit mode, all unused EP80579 DDR2 Data Bus Interface Signals should be pulled high to 1.8V (VCC18) with 10KΩ pull-up resistors	• See **Figure 75**
DDR_A[14:0] DDR_BA[2:0] DDR_RAS# DDR_CAS# DDR_WE#	O	• Connect to each DIMM • Use 18 pF 5% 50V compensation capacitor on each signal. • Use 60 Ω ±1%, 0.25W, pull-up resistor to DDR Termination voltage (DDR2_VTT) on each signal.	• Use one capacitor per signal to DIMM0 only • Place capacitor as close as possible to DIMM0 • See **Figure 82**
DDR_CS[1:0]#, DDR_CKE[1:0], DDR_ODT[1:0]	O	• Use 60 Ω ±1%, 0.25W, pull-up resistor to DDR Termination voltage (DDR2_VTT) on each signal. • Connect DDR_CS[0]#/DDR_CKE[0]/DDR_ODT[0] to DIMM0 Rank 0 • Connect DDR_CS[1]#/DDR_CKE[1]/DDR_ODT[1] to DIMM0 Rank 1 • Connect DDR_CS[1]#/DDR_CKE[1]/DDR_ODT[1] to DIMM1 Rank 0	• DIMM0 supports both single and dual rank memory modules • DIMM1 supports only single rank memory modules • See **Figure 81**

Table 100.   Schematic Checklist (Sheet 4 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
DDR_CK[5:0], DDR_CK[5:0]#	O	• Connect DDR_CK[2:0]/ DDR_CK[2:0]# from EP80579 to DIMM0. • Connect DDR_CK[5:3]/ DDR_CK[5:3]# from EP80579 to DIMM1	• See **Figure 79** and **Figure 80** • Route clocks as differential signals
DDR_CRES[0], DDR_SLWCRES, DDR_DRVCRES DDR_RCOMPX	I/O	• Connect DDR_SLWCRES to DDR_CRES[0] with 825Ω ±1% resistor. • Connect DDR_DRVCRES to DDR_CRES[0] with 249Ω ±1% resistor. • Connect DDR_RCOMPX to DDR_CRES[0] with 825Ω ±1% resistor.	• See **Figure 83**
DDR_CRES[1], DDR_CRES[2]	I/O	• Connect DDR_CRES[1] to ground with 100 Ω ±1%. • Connect DDR_CRES[2] to EP80579 1.8V (VCC18) with 100 Ω ±1%. • Decouple DDR_CRES[2] with 0.1 μF ±10%, 16V, capacitor to GND.	• See **Figure 84**
PCI Express Interface			
PEA0_Tp[7:0], PEA0_Tn[7:0]	O	• Connect from EP80579 transmit outputs to PCI Express Device receive input pins through 0.1 μF ±10% AC blocking capacitors.	• Signals should be routed as differential pairs • See **Figure 94** • See Section 10.1.7 for Transmit guidelines for EP80579 interface to the PCI-E Connector *Note:* If a PCI-E port is not used or not connected to an interfacing device, terminate the transmit signals as follows: • PEA0_Tp[x]/PEA0_Tn[x] signals may be left as no connect (NC) (where 'x' is the PCIE port number left unconnected)
PEA0_Rp[7:0], PEA0_Rn[7:0]	I	• Connect from PCI Express Device transmit outputs to EP80579 receive inputs. • Require external 0.1 μF ±10% AC blocking capacitors on Receive signals if the Transmitting Device do not have the suppression capacitors built in at the transmitter.	• Signals should be routed as differential pairs • See **Figure 95** • See Section 10.1.7 for Receive guidelines for EP80579 interface to PCI-E Connector *Note:* If a PCI-E port is not used or not connected to an interfacing device, terminate the receive signals as follows: • PEA0_Rp[x]/PEA0_Rn[x] signals may be left as no connect (NC) (where 'x' is the PCI-E port number left unconnected)

Table 100. Schematic Checklist (Sheet 5 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
PEA_CLKp, PEA_CLKn	I	• Connect to one of 100 MHz differential clock outputs from CK410 Clock device through a 33 Ω ±5% series resistor. • Terminate to GND through a 49.9Ω ±1% resistor	**Note:** • Connect PEA_CLK(p/n) to a 100 MHz differential clock source even if the PCI-E port is not used or not connected to an interfacing device. • See Section 2.3
PEA_ICOMPI, PEA_ICOMPO, PEA_RCOMPO	I	• Tie these signals together and connect to EP80579 1.2V (VCC) supply through a 24.9 Ω ±1% resistor.	
Integrated I/O Controller Hub (IICH) Interface			
Real Time Clock (RTC)			
RTCX1, RTCX2	I/O	RTC Crystal I/O • Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 MΩ resistor. • Decouple both RTCX1 and RTCX2 with 15 pF ±5%, 50V capacitors to GND.	**Note:** • The capacitor and resistor values in this document is based on the crystal selected for the Development Board. • The exact capacitor and resistor values for any design must be based on the recommendations provided by the crystal maker for the crystal selected for the design • See Figure 130 for further guidelines
RTEST#	I	RTC Test Enable • Connect pin to a 20KΩ ± 5% resistor to VCCRTC. • Connect to a 1.0µF ± 5% capacitor to GND.	See Section 15.1.5.
General Purpose I/O (GPIO) and Interrupts Interface			
GPIO[1:0]	I	• Input Only (GPI)	• Must be pulled high through a 10 KΩ resistor if not used • Resides in Core Power Well
GP2_PIRQE#	I	• Input Only if used as GPI. • Can be used as PIRQE#.	• Must be pulled high through a 10 KΩ resistor if not used or used in PIRQ mode. • Resides in Core Power Well
GP3_PIRQF#	I	• Input Only if used as GPI. • Can be used as PIRQF#.	• Must be pulled high through a 10 KΩ resistor if not used or used in PIRQ mode. • Resides in Core Power Well
GP4_PIRQG#	I	• Input Only if used as GPI. • Can be used as PIRQG#.	• Must be pulled high through a 10 KΩ resistor if not used or used in PIRQ mode • Resides in Core Power Well
GP5_PIRQH#	I	• Input Only if used as GPI. • Can be used as PIRQH#.	• Must be pulled high through a 10 KΩ resistor if not used or used in PIRQ mode • Resides in Core Power Well
GPIO[7:6]	I	• Input Only (GPI)	• Must be pulled high through a 10 KΩ resistor if not used • Resides in Core Power Well

Table 100. Schematic Checklist (Sheet 6 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
GPIO[10:8]	I	• Input Only (GPI).	• Must be pulled high through a 10 KΩ resistor if not used. • Resides in Suspend Power Well
GP11_SMBALERT#	I	• Input Only if used as GPI. • Can be used as SMBus Alert: Wake System or generate SMI#	• Must be pulled high through a 10 KΩ resistor if used for SMBALERT# or if not used • Resides in Suspend Power Well
GPIO[13:12]	I	• Input Only GPI.	• Must be pulled high through a 10 KΩ resistor if not used. • Resides in Core Power Well
GPIO[15:14]	I	• Input Only (GPI).	• Must be pulled high through a 10 KΩ resistor if not used. • Resides in Suspend Power Well
GP16_IRQ24	I/O	• Input/Output configurable if used as GPIO[16]. **Strapping Options:** **A16 Overide Strap** • This strap selects the treatment of A16 for cycles going to BIOS space (but not feature space) in the FWH. EP80579 interprets this strap as follows: • 0 = EP80579 does not invert A16 • 1 = EP80579 inverts A16 on some BIOS cycles (**default = 1**) *Note:* • Since there is an internal pull-up, there is no need for an external pull-up for the system to operate in the default state. • Pull to GND with 1KΩ ± 5% resistor to overide the inversion.	• This signal can function as either GPIO[16] or IRQ[24]. • Resides in Core Power Well • 50KΩ internal pull-up.
GP17_IRQ25	I/O	• Input/Output configurable if used as GPIO[17]. • Can be strapped for SPI Boot-up • Can be used as IRQ[25] • This pin, in conjuction with GP33_IRQ33, can be strapped to select the source of BIOS during boot-up. • Since GP17 and GP33 have internal pull-ups, the default boot up is set to FWH. GP17 and GP33 should be strapped to ground through 1KΩ pull-down resistors to configure the boot source to the SPI Flash	• This signal can function as either GPIO[17] or IRQ[25]. • 50KΩ internal pull-up Boot BIOS Selection Strap: This strap selects the source of the BIOS during boot. EP80579 interprets GP17 & GP33 strappings as follows: **GP17 GP33 (Boot Options)** 0 0 Boot BIOS from SPI 0 1 Reserved 1 0 Reserved 1 1 (Default) Boot BIOS from LPC • See Table 74 for more details

Table 100.   Schematic Checklist (Sheet 7 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
GP18_IRQ36	I/O	• Input/Output configurable if used as GPIO[18]. • Can be used as IRQ[36]	• 50KΩ internal pull-up • No external Pullup Required • ***Note:*** • Do not strap or drive this signal low during power-up until the CPURST# signal is de-asserted.
GP19_IRQ37	I/O	• Input/Output configurable if used as GPIO[19]. • Can be used as IRQ[37]	• 50KΩ internal pull-up • No external Pullup Required ***Note:*** • Do not strap or drive this signal low during power-up until the CPURST# signal is de-asserted.
GP20_IRQ26	I/O	• Input/Output configurable if used as GPIO[20]. • Can be used as IRQ[26]	• No external pull-up required if used in IRQ mode. ***Note:*** • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Core Power Well
GP21_IRQ27	I/O	• Input/Output configurable if used as GPIO[21]. • Can be used as IRQ[27]	• 50KΩ internal pull-up • No external Pullup Required ***Note:*** • Do not strap or drive this signal low during power-up until the CPURST# signal is de-asserted.
GP23_IRQ28	I/O	• Input/Output configurable if used as GPIO[23]. • Can be used as IRQ[28]	• 50KΩ internal pull-up • No external Pullup Required ***Note:*** • Do not strap or drive this signal low during power-up until the CPURST# signal is de-asserted.
GP24_IRQ29	I/O	• Input/Output configurable if used as GPIO[24]. • Can be used as IRQ[29]	• No external pull-up required if used in IRQ mode. ***Note:*** • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Suspend Power Well
GP25_IRQ38	I/O	• Input/Output configurable if used as GPIO[25]. • Can be used as IRQ[38]	• No external pull-up required if used in IRQ mode. ***Note:*** • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Suspend Power Well
GP26_SATA0GP	I	• Input Only if used as GPI. • Can be used as SATA Port 0 Interlock switch Status Input depending on the platform	• SATAOGP: Interlock Switch Status Port0: 0 = Closed 1 = Open • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Core Power Well

Table 100.   Schematic Checklist (Sheet 8 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
GP27_IRQ39	I/O	• Input/Output configurable if used as GPIO[27]. • Can be used as IRQ[39]	• No external pull-up required if used in IRQ mode. ***Note:*** • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Suspend Power Well
GP28_IRQ30	I/O	• Input/Output configurable if used as GPIO[28]. • Can be used as IRQ[30]	• No external pull-up required if used in IRQ mode. ***Note:*** • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Suspend Power Well
GP29_SATA1GP	I	• Input Only if used as GPIO[29] • Can be used as SATA Port 1 Interlock switch Status Input depending on the platform	• SATA1GP: Interlock Switch Status Port1: 0 = Closed 1 = Open • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Core Power Well
GP30_IRQ31	I	• Input only if used as GPIO[30]. • Can be used as IRQ[31]	• No external pull-up required if used in IRQ mode. ***Note:*** • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Core Power Well
GP31_IRQ32	I	• Input only if used as GPIO[31]. • Can be used as IRQ[32]	• No external pull-up required if used in IRQ mode. ***Note:*** • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Core Power Well
GP33_IRQ33	I/O	• Input/Output configurable if used as GPIO[33]. • Can be strapped for SPI Boot-up • Can be used as IRQ[33] • This pin, in conjuction with GP17_IRQ25, can be strapped to select the source of BIOS during boot-up. • Since GP17 and GP33 have internal pull-ups, the default bootup is set to FWH. GP17 and GP33 should be strapped to ground through 1KΩ pull-down resistors to configure the boot source to the SPI Flash.	• This signal can function as either GPIO[33] or IRQ[33]. • 50KΩ internal pull-up Boot BIOS Selection Strap: This strap selects the source of the BIOS for system boot. EP80579 interprets GP17 & GP33 strappings as follows: **GP17 GP33 (Boot Options)** 0 0 Boot BIOS from SPI 0 1 Reserved 1 0 Reserved 1 1 (Default) Boot BIOS from LPC • See Table 74 for more details

Table 100. Schematic Checklist (Sheet 9 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
GP34_IRQ34	I/O	• Input/Output configurable if used as GPIO[34]. • Can be used as IRQ[34]	• No external pull-up required if used in IRQ mode. ***Note:*** • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Core Power Well
GP40_IRQ35	I	• Input only if used as GPIO[40]. • Can be used as IRQ[35]	• No external pull-up required if used in IRQ mode. ***Note:*** • Must be pulled high through a 10 KΩ resistor if not used. • Resides in Core Power Well
GP41_LDRQ[1]#	I	• Input only if used as GPIO[41]. • Can be used as LPC DMA Request input (LDRQ[1])	• 50KΩ internal pull-up • No external Pullup Required
GPIO[48]	O	• Output Only (GPO).	• 50KΩ internal pull-up • No external Pullup Required • Should **not** be pulled down.
IICH Interrupts			
SERIRQ	I	• Connect to SuperIO (SIO) SER_IRQ pin	• Serial Interrupt Request. This signal implements the serial interrupt protocol. ***Note:*** • Must be pulled high through a 10 KΩ resistor if used in PIRQ mode. • Resides in Core Power Well
Firmware Hub/Low Pin Count (FWH/LPC) Interface			
LAD[3:0], LFRAME#,	I/O	• No external pull-ups required. • Connect straight to FWH/TPM/ SuperIO/Port80 Display	
LDRQ[0]#	I	• Connect to SuperIO LDRQ# output	• 50KΩ internal pull-up • No external Pullup Required • Should **not** be pulled down.
LDRQ[1]# (GPIO[41]) See General Purpose I/O (GPIO) Interface			
PCICLK	I	• Connect to one of six sets of 33 MHz clock outputs from CK410 Clock Synthesizer • Connect clocks through 33 Ω ±5% series resistor	***Note:*** • See Section 2.3
Serial Peripheral Interface (SPI) - System BIOS Topology			
SPI_MOSI	O	• Connect to the serial data input pin of the flash device. • Connect signal **through a 15Ω ±1% series resistor** • Place resistor close to EP80579	***Note:*** • Can be left as NC when the port is not connected to an interfacing device.
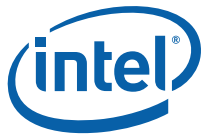
Table 100. Schematic Checklist (Sheet 10 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
SPI_MISO	I	• Connect to the serial data output pin of the flash device • Connect signal through a 15Ω ±1% series resistor • Place resistor close to flash device	*Note:* • Must be pulled high to 3.3V through a 10 KΩ resistor when the port is not used.
SPI_CS#	O	• Connect to the chip select (CS#) pin of the flash device • Connect signal through a 15Ω ±1% series resistor • Place series resistor close to EP80579 • Pull-up to 3.3V through a 10 KΩ resistor for signal stability during power-up	*Note:* • Can be left as NC when the port is not connected to an interfacing device.
SPI_CLK	O	• Connect to the clock input pin of the flash device • Connect signal through a 15Ω ±1% series resistor • Place series resistor close to EP80579.	*Note:* • Can be left as NC when the port is not connected to an interfacing device.
System Management Bus (SMBus) Interface			
SMBDATA/SMBCLK	OD I/O	• Primary SMBus from EP80579 • Primary SMBus requires external 8.2 kΩ pull-up resistors to EP80579 3.3V Standby voltage (VCCPSUS) on both data and clock • Connect Primary SMBus to SuperIO and EP80579 IMCH SMLINK • Use Primary SMBus and Repeaters to generate three secondary SMBuses - (for voltage translation, fanout, and isolation)- • • SMBus_A - IMCH_SMBus • SMBus_B - DIMM SMBus • SMBus_C - MEZZ_SMBus	**SMBus_A (IMCH_SMBus):** • Connects to EP80579 IMCH SMBus (SMBSDA/SMBSCL) • Connects to CK410 and clock buffer DB800 • Connects to ITP-XDP Connector. • Requires external 8.2 kΩ pull-up resistors to platform VCC3 on both data and clock. **SMBus_B (DIMM SMBus):** • Connects to DDR_DIMM0 and DDR_DIMM1 • Requires external 8.2 kΩ pull-up resistors to platform VCC3 on both data and clock. **SMBus_C (MEZZ_SMBus):** • Connects to Mezzanine (0/1/2) Connectors • Requires external 8.2 kΩ pull-up resistors to platform VCC3 on both data and clock.
SMBSDA/SMBSCL	OD I/O	• Connect to SMBus_A (IMCH_SMBus)	*Note:* • See the row above for SMBus_A guidelines.
SMLINK[1:O]	OD I/O	Connect to Primary SMBus: • Connect SMLINK[0] to SMBCLK • Connect SMLINK[1] to SMBDATA	• SMBus System Management Link: SMBus link to optional external system management ASIC or LAN controller • Connect to Primary SMBus from EP80579 (SMBDATA/SMBCLK) • Primary SMBus requires external 8.2 kW pull-up resistors to EP80579 VCCPSUS power supply (3.3V sustain power) on both data and clock.

Table 100. Schematic Checklist (Sheet 11 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
INTRUDER#	I	• Connect to EP80579 VCCPRTC (VBAT) through a 1MΩ resistor	• SMBus Intruder Detect: Detects if the system case has been opened. Can be set to disables the system if the box is detected open. This input signal is in the RTC well. This pin's status is readable, so it can be used like a GPI if the Intruder switch is not needed
SMBALERT# (GPIO[11]) See General Purpose I/O (GPIO) Interface			
Serial Interface Unit (SIU or UART) Interface			
SIU_CTS[2:1]#	I/O	• Connect signals appropriately to RS-232 Transceiver	• UART Port[2:1] Clear to Send: Active low, these pins indicate that data can be exchanged between UARTs and the external interfaces. *Note:* • Must be pulled high through a 10 KΩ resistor when the port is not connected to an interfacing device
SIU_DCD[2:1]#	I/O	• Connect signals appropriately to RS-232 Transceiver	• UART Port[2:1] Data Carrier Detect: Active low, these pins indicate that data carrier has been detected by the external agents for UART port[2:1]. *Note:* • Must be pulled high through a 10 KΩ resistor when the port is not connected to an interfacing device
SIU_DSR[2:1]#	I/O	• Connect signals appropriately to RS-232 Transceiver	• UART Port[2:1] Data Set Ready: Active low, these pins indicate that the external agents are ready to communicate with UART port[2:1]. *Note:* • Must be pulled high through a 10 KΩ resistor when the port is not connected to an interfacing device

Table 100. Schematic Checklist (Sheet 12 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
SIU_DTR[2:1]#	I/O	• Connect signals appropriately to RS-232 Transceiver **Strapping Options:** **SIU_DTR[1]# -** **(SIW Config Port Address Select)** • 0 = SIW IO Addresses are 20Eh and 20Fh • 1 = SIW IO Addresses are 04Eh and 04Fh (**default**)	• UART Port[2:1] Data Terminal Ready: When low, these pins inform the modem or data set that the UART ports are ready to establish a communication link. *Note:* • SIU_DRT[1]# is sampled on Power-up to select SIW Configuration Port Address. This strap selects the IO Address for the Serial I/O Unit and Watchdog Time • Signals have 50KΩ internal pull-ups *Note:* • SIU_DTR[1] need to be strapped appropriately even if the port is not used or not connected to an interfacing device. • SIU_DTR[2] can be left as no connect (NC) if the port is not used. • Do not strap or drive SIU_DTR[2] signal low during power-up until the CPURST# signal is de-asserted.
SIU_RI[2:1]#	I/O	• Connect signals appropriately to RS-232 Transceiver	• UART Port[2:1] Ring Indicator: Active low, these pins indicate that a telephone ringing signal has been received by the external agents for UART port [2:1]. *Note:* • Must be pulled high through a 10 KΩ resistor when the port is not connected to an interfacing device
SIU_RTS[2:1]#	I/O	• Connect signals appropriately to RS-232 Transceiver	• UART Port[2:1] Request To Send: When low these pins inform the modem or data set that UART ports want to send data on an established communication link. The RTS# output signal can be set to an active low by programming the RTS (bit 1) of the Modem Control Register to a logic '1'. A Reset operation sets this signal to its inactive state (logic '1'). LOOP mode operation holds this signal in its inactive state • Signals have 50KΩ internal pull-ups *Note:* • Signal can be left as NC when the port is not connected to an interfacing device • Do not strap or drive SIU_RTS[1] or SIU_RTS[2] signal low during power-up until the CPURST# signal is de-asserted.

Table 100.   Schematic Checklist (Sheet 13 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
SIU_RXD[2:1]	I/O	• Connect signals appropriately to RS-232 Transceiver	• UART Port[2:1]Serial Data Input: Serial data input form external devices to the receive UART port [2:1]. ***Note:*** • Must be pulled high through a 10 KΩ resistor when the port is not connected to an interfacing device
SIU_TXD[2:1]	I/O	• Connect signals appropriately to RS-232 Transceiver **Strapping Options**: **SIU_TXD[2] -** **(GPIO IRQ Capability Strap)** • 0 = GPIO IRQ Capability enabled • 1 = GPIO IRQ Capability disabled ***Note:*** **(default = 0)** Connect SIU_TXD[2] through a 510 Ω pull-down resistor to ground to enable IRQ capability	• UART Port[2:1] Serial Data Output: Serial data output to the communication peripheral/modem or data set for UART port [2:1]. Upon reset, the TXD pins will be set to MARKING condition (logic '1' state). • Signals have 50KΩ internal pull-ups ***Note:*** • SIU_TXD[2] needs to be strapped appropriately even if the port is not used or not connected to an interfacing device. • SIU_TXD[1] can be left as no connect (NC) if the port is not used.
UART_CLK	I	• Connect to 48 MHz clock (USB_48) from the CK410 Clock Synthesizer • Connect clock through a 33 Ω ±5% series resistor.	***Note:*** • Both UART_CLK and USB_CLK (CLK48) use the same clock output (USB_48) from the CK410 Clock Synthesizer. • Isolate UART_CLK from USB_CLK (CLK48) through 33 Ω ±5% series resistors • Connect UART_CLK to a 48 MHz clock source even when the SIU ports are not connected to any interfacing device. • See Section 2.3
Serial ATA (SATA) Interface			
SATA_TXp[1:0], SATA_TXn[1:0], SATA_RXp[1:0], SATA_RXn[1:0]	I/O	Requires series AC coupling capacitors: • Connect 0.01µF ±10% capacitor on each data line between EP80579 and SATA connector.	***Note:*** If a SATA port is not used or connected to an interfacing device, terminate the signals as follows: • SATA_RXp/SATA_RXn, SATA_TXp/SATA_TXn signals may be left as no connect (NC)
SATA_RBIAS SATA_RBIAS#	I	SATA Bias Resistor • Short signals SATA_RBIAS to SATA_RBIAS# at package. • Pull down shorted signal through a 24.9Ω ±1% resistor to ground.	***Note:*** • Tie SATA_RBIAS and SATA_RBIAS# together and connect to GND through a 24.9Ω ±1% resistor even when the SATA port is not used or connected to an interfacing device.
SATA_CLKREFp, SATA_CLKREFn	I	• Connect to SRC_4_SATAp/n (100 MHz) clock outputs of the CK410 Clock Synthesizer. • Connect clocks through 33 Ω ±5% series resistors • Connect clocks through 49.9Ω ±1% resistors to ground	***Note:*** • Connect SATA_CLKREFp/ SATA_CLKREFn to a 100 MHz clock source even if the SATA port is not used or connected to an interfacing device. • See Section 2.3

Table 100. Schematic Checklist (Sheet 14 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
SATALED#	OD O	• Can monitor using an LED to indicate SATA activity. • Requires an external 10KΩ pull-up to EP80579 VCC33 (3.3V) power supply if used	Serial ATA LED: This is an open-collector/open-drain output signal driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tristated, the LED is off. An external pull-up resistor is required. ***Note:*** • If all SATA ports are not used, this signal can be left as no connect (NC)
SATA0GP (GPIO[26]) See General Purpose I/O (GPIO) Interface			
SATA1GP (GPIO[29]) See General Purpose I/O (GPIO) Interface			
Universal Serial Bus (USB) Interface			
USBp[1:0], USBn[1:0]	I/O	• No external resistors are required. • Connect USBp/n[0] and USBp/n[1] differential signal pins through Common Mode Chokes to USB connector for ESD and EMI suppression.	• Common mode chokes with a target impedance of 80-90 Ω at 100 MHz generally provide adequate noise suppression. • See Section 12.2.2 for more details. ***Note:*** • Can be left as no connect (NC) when the port is not used.
OC[1:0]#	I	• Connect to OC[2:1]# outputs of a USB current limiter power distribution switch. • Pull up signals to P3V3_AUX using a 10KΩ ± 5% resistors	• See Section 12.2.5 ***Note:*** • If these signals are not used, pull up to EP80579 3.3V Standby voltage (VCCPSUS) with an 10 kΩ resistor.
USB_RBIASp USB_RBIASn	I/O	• Short signals USB_RBIASp to USB_RBIASn at package. • Connect shorted signal to a 22.6 Ω ±1% pull-down resistor to ground	• See Section 12.2.3 • Bias connection is required even if the USB ports are not used.
CLK48	I	• Connect to 48 MHz clock (USB_48) from the CK410 Clock Synthesizer • Connect clock through a 33 Ω ±5% series resistor.	***Note:*** • Both UART_CLK and USB_CLK (CLK48) use the same clock output (USB_48) from the CK410 Clock Synthesizer. • Isolate UART_CLK from USB_CLK (CLK48) through series resistors. • Connect CLK48 to a 48 MHz clock source even if the USB ports are not used. • See Section 2.3 • See Section 8.2.5, "CLK48 Group" on page 102.
Power Management Interface			
PLTRST#	O	• Connect to EP80579 RSTIN# input. • Connect to all Platform devices that require reset.	Platform Reset: IICH asserts PLTRST# to reset Platform devices.

Table 100. Schematic Checklist (Sheet 15 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
PROCHOT#	O	• Can monitor using an LED to indicate IA-32 core Thermal Status. • Pull up signal to EP80579 VCC33 (3.3V) using a 10KΩ ± 5% resistors	Thermal Alarm. Driven out by EP80579. Monitored by Platform.
THRMTRIP#	OD I/O	• Monitor using an LED to indicate IA-32 core Thermal Status. • Pull up signal to EP80579 VCC33 (3.3V) using a 10KΩ ± 5% resistors	Thermal Trip. When Low, immediately transitions IICH to S5 State
SLP_S3# SLP_S4#, SLP_S5#	O	• Signals are driven by EP80579 to Platform Sleep logic. • Can monitor any or all the signals using LEDs to indicate IA-32 core Sleep Status	• S3 Sleep Control (Power Down): Suspend-To_RAM (STR) • S4 Sleep Control (Power Down): Suspend-To-DISK • S5 Sleep Control (Power Down): S5-Soft Off
PWROK	I	• Connect to Platform SYS_PWR_OK	Indicates EP80579 core power (VRMPWRGD) has been stable for a minimum of 99ms.
SYS_PWR_OK	I	• Connect to Platform SYS_PWR_OK	Indicates EP80579 core power (VRMPWRGD) has been stable for a minimum of 99ms.
PWRBTN#	I	• Direct connect to front panel power button on system	• Power Button: Causes system to go to a sleep state. If already in sleep state, will cause a wake event. If PWRBTN# is pressed for more than four seconds, will cause unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S3 or S4 state. • This signal has a 50 KΩ internal pullup resistor and has an internal 16 ms de-bounce on the input
RI#	I	• This signal is not implemented. • Pull-up to EP80579 3.3V Standby (VCCPSUS) power supply using 10KΩ ± 5% resistor.	• Ring Indicate: From the modem interface. Can be enabled as a wake event and is preserved during power failures
SYS_RESET#	I	• Connect to front panel Reset Button on system. • Pull-up to Platform 3.3V Standby (VSBY3_3) power supply using 10KΩ ± 5% resistor.	• System Reset: Forces internal reset. • Signal should not float. • Requires external pull-up.
RSMRST#	I	• Connect to SuperIO (SIO) RSMRST# output and must go high no sooner than 10 ms after VSBY3_3 has reached their nominal voltages. • Connect through 8.2 kΩ ± 5% resistor to GND.	• Resume Well Reset. This signal is used to reset the Suspend power plane logic. • If the SIO device is not used in the design, an external RC circuit is required to guarantee that the resume well power is valid prior to RSMRST# going high.

Table 100. Schematic Checklist (Sheet 16 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
SUS_STAT#	O	• Can monitor using an LED.	• Suspend State Status: Asserted to indicate that the system is entering into a low power state. **Note:** • This signal can be left as a no connect (NC) if not used
SUSCLK	O	• Connect to SuperIO (SIO) CLKI32 (32.768 kHz) input.	• Suspend Clock. Output clock from RTC clock generator circuit. **Note:** • This signal can be left as a no connect (NC) if not used. • This signal can be exposed via a testpoint for debug purposes if not used.
VRMPWRGD	I	• This signal is connected to the IA-32 core Voltage Regulator power good output signal.	• IA-32 core Voltage Regulator Power Good.
IICH Miscellaneous Signals			
CLK14	I	• Connect to REF clock (14 MHz) from the CK410 Clock Synthesizer • Connect clock through a 33 Ω ±5% series resistor.	• Timer Oscillator Clock: Used for 8254 timers and HPET (High Precision Event Timer). Runs at 14.31818 MHz. This clock stops (and should be low) during S3 and S5 state. CLK14 must be accurate to within 500ppm over 100usecs (and longer periods) in order to meet HPET accuracy requirements • See Section 2.3
PE_HPINTR#	I	• On platforms that support PCI Express Hot-Plug, pull this pin up to EP80579 3.3 V (VCC33) with 1 kΩ ±5% resistor. Connect to an output of the Hot-Plug I/O expander logic. • On platforms that do not support PCI Express Hot-Plug, pull up to EP80579 3.3V (VCC33) supply through a 10 KΩ ±5% resistor.	**Note:** Because PCI Express Hot Plug is not supported in EP80579, this pin must be pulled up to EP80579 3.3V (VCC33) supply through a 10 KΩ ±5% resistor
BSEL	O	FSB Frequency Indicator. • Driven by CPU to indicated FSB Frequency. • See Section 6.2 for more details.	• The BSEL and V_SEL signals are outputs from EP80579 to reflect the internal strapping of the various EP80579 SKUs. The BSEL and V_SEL signals are interpreted to indicate the FSB frequency and CPU power requirements for the various SKUs.
V_SEL	I/OD	IA-32 core Voltage Select Indicator: • Driven by EP80579 to indicate CPU SKU voltage requirements. • Requires an external 10K pull-up to Platform 3.3V • See Section 6.2 for more details.	• See Section 6.2 for more details. **Note:** • The V_SEL signal is an open drain (OD) I/O signal that requires an external 10K pull-up. It can also be pulled to GND on the Platform to configure a EP80579 1.2GHz SKUed part to operate at 1.066GHz frequency.
WDT_TOUT#	O	• Can be monitored using an LED	WatchDog Timer Output. Used by Platform Management Controller to reset EP80579

Table 100. Schematic Checklist (Sheet 17 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
**Acceleration and I/O Complex (AIOC)**
**Controller Area Network (CAN) Interface**
CN0TXD, CN1TXD	O	• Connect directly to the Driver (D) inputs of CAN Transceivers • One CAN Transceiver per channel	• Connect CAN Low/High (CANL/ CANH) outputs to CAN Connector *Note:* • Can be left as NC when the port is not connected to an interfacing device.
CN0TXEN, CN1TXEN	O	• Connect to Standby/Slope Control (Rs) inputs of CAN Transceivers	• Driver is switched off and the receiver is activated if a high logic is applied to Rs and remains in sleep mode until the circuit is activated by a low logic level on Rs *Note:* • Can be left as NC when the port is not connected to an interfacing device.
CN0RXD, CN1RXD	I	• Connect directly to the Receive (R) outputs of CAN Transceivers	*Note:* • Must be pulled high through a 10 KΩ resistor when the interface is not used or connected to an interfacing device
**Gigabit Ethernet (GbE) Interface** *Note:* • GBE Port 0 supports Wake-On-LAN (WOL); hence GBE Port 0 Block resides in the Sustain Power Well within EP80579. It is required that all GBE Port 0 (Transmit/Receive) interface signals on the platform be powered by GBE Standby Voltage. GBE Port 1&2 should be powered by GBE core power.
GBEn_TxDATA[3:0]	O	**RGMII Mode** • Interconnect each Port Transmit Data (GBEn_TxDATA[3:0]) to the corresponding Port Transmit Data of the RGMII PHY Device • Pull up GBE Port 0 Transmit Data signals to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistors. • Pull up GBE Port 1&2 Transmit Data signals to GBE 2.5V using a 1.2KΩ ± 5% resistors. • Leave signals for any unused Port as no connect.	**RMII Mode** • Interconnect the lower two bits of each Port Transmit Data (GBEn_TxDATA[1:0]) to the corresponding Port Transmit Data of the RMII PHY Device. • Pull up GBE Port 0 Transmit Data signals to EP80579 3.3V Standby Voltage (VCCGBEPSUS) using a 1.2KΩ ± 5% resistors. • Pull up GBE Port 1&2 Transmit Data signals to GBE 3.3V using a 1.2KΩ ± 5% resistors • Leave all unused Transmit Data signals as no connect.
		*Note:* • Can be left as NC when the port is not used in either mode.

Table 100. Schematic Checklist (Sheet 18 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
GBEn_TxCLK	O	**RGMII Mode** • Interconnect each Port Transmit Clock (GBEn_TxCLK) to the corresponding Port Transmit Clock of the RGMII PHY Device • Pull up GBE Port 0 Transmit Clock signal to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistor. • Pull up GBE Port 1&2 Transmit Clock signals to GBE 2.5V using a 1.2KΩ ± 5% resistors. • Leave the clock of any unused Port as no connect.	**RMII Mode** • Not used in this mode. • Leave all Transmit clock signals as no connect.
		Note: • Can be left as NC when the port is not used in either mode.	
GBEn_TxCTL	O	**RGMII Mode** • Interconnect each Port Transmit Control (GBEn_TxCTL) to the corresponding Port Transmit Enable (TX_EN) of the RGMII PHY Device • Pull up GBE Port 0 Transmit Control signal to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistor. • Pull up GBE Port 1&2 Transmit Control signals to GBE 2.5V using a 1.2KΩ ± 5% resistors. • Leave the control signal of any unused Port as no connect.	**RMII Mode** • Interconnect each Port Transmit Control (GBEn_TxCTL) to the corresponding Port Transmit Enable (TX_EN) of the RMII PHY Device • Pull up GBE Port 0 Transmit Control signal to EP80579 3.3V Standby Voltage (VCCGBEPSUS) using a 1.2KΩ ± 5% resistor. • Pull up GBE Port 1&2 Transmit Control signals to GBE 3.3V using a 1.2KΩ ± 5% resistors • Leave the control signal of any unused Port as no connect
		Note: • Can be left as NC when the port is not used in either mode.	
GBEn_RxDATA[3:0]	I	**RGMII Mode** • Interconnect each Port Receive Data (GBEn_RxDATA[3:0]) to the corresponding Port Receive Data of the RGMII PHY Device • Pull up GBE Port 0 Receive Data signals to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistors. • Pull up GBE Port 1&2 Receive Data signals to GBE 2.5V using a 1.2KΩ ± 5% resistors. • Pull-down all unused Receive Data signals to GND using 10 KΩ resistors	**RMII Mode** • Interconnect the lower two bits of each Port Receive Data (GBEn_RxDATA[1:0]) to the corresponding Port Receive Data of the RMII PHY Device. • Connect each Port Receive Data bit3 (GBEn_RxDATA[3]) to the corresponding Port Receive Error signal (RX_ER) of the RMII PHY Device • Pull up GBE Port 0 Receive Data signals to EP80579 3.3V Standby Voltage (VCCGBEPSUS) using a 1.2KΩ ± 5% resistors. • Pull up GBE Port 1&2 Receive Data signals to GBE 3.3V using a 1.2KΩ ± 5% resistors • Pull-down all unused Receive Data signals to GND using 10 KΩ resistors
		Note: • Pull-down all Receive Data signals to GND using 10 KΩ resistors when the port is not used in either mode	

Table 100.   Schematic Checklist (Sheet 19 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
GBEn_RxCLK	I	**RGMII Mode** • Interconnect each Port Receive Clock (GBEn_RxCLK) to the corresponding Port Receive Clock of the RGMII PHY Device • Pull up GBE Port 0 Receive Clock signal to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistor. • Pull up GBE Port 1&2 Receive Clock signals to GBE 2.5V using a 1.2KΩ ± 5% resistors. • Pull-down all unused Receive Clock signals to GND using 10 KΩ resistors.	**RMII Mode** • No used in this mode • Pull-down all Receive Clock signals to GND using 10 KΩ resistors
		Note: • Pull-down all Receive Clock signals to GND using 10 KΩ resistors when the port is not used in either mode	
GBEn_RxCTL	I	**RGMII Mode** • Interconnect each Port Receive Control (GBEn_RxCTL) to the corresponding Port Receive Data Valid (RX_DV) of the RGMII PHY Device • Pull up GBE Port 0 Receive Control signal to EP80579 2.5V Standby Voltage (VCCSUS25) using a 1.2KΩ ± 5% resistor. • Pull up GBE Port 1&2 Receive Control signals to GBE 2.5V using a 1.2KΩ ± 5% resistors. • Pull-down all unused Receive Control signals to GND using 10 KΩ resistors.	**RMII Mode** • Interconnect each Port Receive Control (GBEn_RxCTL) to the corresponding Port Receive Data Valid (CRS_DV) of the RMII PHY Device • Pull up GBE Port 0 Receive Control signal to EP80579 3.3V Standby Voltage (VCCGBEPSUS) using a 1.2KΩ ± 5% resistor. • Pull up GBE Port 1&2 Receive Control signals to GBE 3.3V using a 1.2KΩ ± 5% resistors • Pull-down all unused Receive Control signals to GND using 10 KΩ resistors.t
		Note: • Pull-down all Receive Control signals to GND using 10 KΩ resistors when the port is not used in either mode	
GBE_REFCLK	I	**RGMII Mode** • 125 MHz Reference clock • Sourced from an external clock or from the RGMII PHY Device.	**RMII Mode** • 50 MHz Reference clock. • External clock to both the MAC and RMII PHY Device
		Note: • Connect to 125 MHz clock source when the ports are not used in either mode. • See Section 2.3	

Table 100.   Schematic Checklist (Sheet 20 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
GBE_REFCLK_RMII	I	**RGMII Mode** • Not used in this mode • Connect through a 100Ω ±1% resistor to Ground. **Note:** • Pull-down RMII Reference CLock (RMII) signal to GND using 100Ω resistor when the port is not used in either mode. • See Section 2.3	**RMII Mode** • 50 MHz RMII Reference clock. • Sourced from the same external clock as GBE_REFCLK **Note:** • In RMII Mode, the GBE_REFCLK, GBE_REFCLK_RMII, and PHY_REFCLK are sourced by the same external 50 MHz clock, hence, use a no-delay clock buffer to distribute the clocks to the three receivers. • Route clock signals exactly same length from clock buffer to receivers.
GBE_RCOMPP	I/O	• Connect through a 50Ω ±1% resistor to Ground.	
GBE_RCOMPN	I/O	• Pull up to EP80579 GbE 2.5V Standby (VCCSUS25) supply through a 50Ω ±1% resistor	
MDC	O	• Connect to the MDC signal of the PHY device. • Provide termination if signal is connected to multiple receivers. • Resides in GbE Standby Power Well **Note:** • Can be left as NC when none of GBE ports is connected to an interfacing device	
MDIO	I/O	• Connect to the MDIO signal of the PHY device. • Pull-up signal to EP80579 GbE 2.5V Standby (VCCSUS25) using a 1.5 KΩ ± 5% resistor **Note:** • Must be pulled high through a 10 KΩ resistor to EP80579 GbE 2.5V Standby (VCCSUS25) when none of GBE ports is connected to an interfacing device	
EEDO	I	• Connect to EEPROM Serial Data Output signal (DO) • Pull-up to corresponding GbE Standby power supply through a 4.7KΩ ±5% resistor. **Note:** • Must be pulled high through a 10 KΩ resistor to EP80579 GbE 2.5V Standby (VCCSUS25) when none of GBE ports is connected to an interfacing device	
EEDI	O	• Connect to EEPROM Serial Data Input signal (DI) • Requires a 20KΩ pull-up to GbE Standby power if GbE Standby power is generated on the platform; otherwise pull-down with 4.7 KΩ	
EECS	O	• Connect to EEPROM Chip Select input (CS) • Connect through a 4.7KΩ ±5% resistor to Ground. **Note:** • Can be left as NC when none of GBE ports is connected to an interfacing device	

Table 100. Schematic Checklist (Sheet 21 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
EESK	O	• Connect to EEPROM Shift Clock input (SK) • Connect through a 4.7KΩ ±5% resistor to Ground. ***Note:*** • Can be left as NC when none of GBE ports is connected to an interfacing device	
GBE_PME_WAKE	OD O	• Connect to EP80579 PME# Input • Pull-up to EP80579 3.3V Standby (VCCPSUS) supply through a 10 KΩ ±5% resistor	
GBE_AUX_PWR_GOOD	I	• Connect to Platform GBE_AUX_PWR_GOOD ***Note:*** • Connect to SYS_PWR_OK if standby voltages are not generated.	
3-Port Time Division Multiplexing (TDM) Interface			
Note: Certain EP80579 SKUs may not contain this feature. Feature must be enabled with EP80579 software. See EP80579 "SKU Features" in the EP80579 Software Documentation for detailed information.			
Rx_CLK[2:0], Rx_FRAME[2:0], Rx_DATA_IN[2:0], Tx_CLK[2:0], Tx_FRAME[2:0], Tx_DATA_OUT[2:0]	I/O	• Connect appropriately to the three mezzanine card connectors. • Each connector supports two TDM (HSS) ports to be compatible with previous voice mezzanine cards.	***Note:*** • If an interface is not used or connected to a device, each interface signal should be pulled high through 10 KΩ resistors.
Local Expansion Bus (LEB) Interface (See **Section 22.3.3** for more details)			
EX_ALE	O	• Address Latch Enable • Used for multiplexed address/data bus accesses	• Used in Intel, Motorola, and HSS multiplexed modes of operation ***Note:*** • Can be left as no connect (NC) when the interface is not connected to an interfacing device or not used

Table 100.   Schematic Checklist (Sheet 22 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
EX_ADDR[24:0]		• Expansion Bus Address. • Connect to Expansion Bus on-board devices and inbound/outbound buffer • Strap EX_ADDR[23:21] as shown below to determine LEB Bus memory size. *Note:* • **BIOS** can also be used to configure the LEB_SIZE through the MMBAR (Expansion Bus Base Address Register) instead of external strapping. (Refer to *EP80579 Datasheet*)	• The LEB controller allocates up to 256 MB of memory space to support up to 8 devices on the LEB Bus. At power-up or whenever RESET_IN# is asserted, EX_ADDR[23:21] bits are captured and stored by the LEB controller to detemine the LEB memory size (LEB_SIZE) and the number of devices on the bus, which also controls the active LEB chip selects. The EX_ADDR[23:21] should be externally strapped with 1KΩ pull-ups and pull-downs to determine the LEB_SIZE. *Note:* • Can be left as no connect (NC) when the LEB Bus is not connected to an interfacing device or not used
		LEB_SIZE Strapping Options: | EX_ADDR [23:21] Strapping	LEB Memory Size (LEB_SIZE)	# of Devices Supported
---	---	---
000	0 MB	0
001	32 MB	1
010	64 MB	2
011	128 MB	4
1XX	256 MB	8 | *Note:* Strap EX_ADDR[23:21] = 000 or use **BIOS** to configure LEB_SIZE = 0 MB if the LEB Bus is not used.	
EX_BE[1:0]	I/O	• Expansion Bus Byte Enables. • Used to select the particular bytes that will be written or read when executing inbound/outbound HSS transfers.	*Note:* • Can be left as no connect (NC) when the interface is not connected to an interfacing device or not used
EX_CLK	I	• 33 MHz Expansion Clock • Use an External 33 MHz Clock with a clock buffer • Connected to one of the outputs from the Expansion Clock Fanout Buffer. • Connect clock **through a 33 Ω ±5% series resistor.**	The EP80579 Expansion Bus connects to several devices on the Platform. • Flash (2) • FPGA • HSS [3:0] Each device should be connected to one of the outputs from the clock fanout buffer. *Note:* • Connect EX_CLK to a 33 MHz clock source when the interface is not used or connected to other devices. • See Section 2.3

Table 100.   Schematic Checklist (Sheet 23 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
EX_CS[7:0]#	I/O	• External Chip Selects for the Expansion Bus Peripheral Devices • Pull-up to Platform 3.3V (VCC3) supply through a 10 KΩ ±5% resistor	Expansion Bus Target Chip Selects: Chip selects to select Expansion Bus devices. • Devices using EX_CS[3:0]# indicate Data Ready with EX_IOWAIT# during EP80579 Read accesses • Devices using EX_CS[7:4]# indicate Data Ready with EX_RDY[3:0]# during EP80579 Read accesses *Note:* • Must be pulled high through a 10 KΩ resistor when the interface is not used or connected to an interfacing device.
EX_DATA[15:0], EX_WR# EX_RD#	I/O	• Bi-directional Expansion Bus data/ Expansion Write Command/ Expansion Bus Read Command. • Isolate DATA/ WR#/RD# to Platform on-board devices from inbound/outbound devices using an external data buffer. • Buses to all on-board devices are isolated from each other using 22Ω ±5% series resistors.	• See Section 22.3.4 for more details. *Note:* EP80579 requires a 2nSec hold time during read accesses. Requires to delay EX_RD# signal **by 2ns(min)** if the interfacing device cannot meet the Thold=2nSec time required by EP80579. *Note:* • Can be left as no connect (NC) when the interface is not connected to an interfacing device or not used
EX_IOWAIT#	I	• Data ready/acknowledge from expansion bus devices • Pull-up to Platform 3.3V (VCC3) supply through a 10 KΩ ±5% resistor	• An expansion bus access is halted when an external device asserts EX_IOWAIT# and resumes access from the halted location once the external device de-asserts EX_IOWAIT# • Expansion Bus Devices using EX_CS[3:0]# indicate Data Ready with EX_IOWAIT# during EP80579 Read Accesses. *Note:* • Must be pulled high through a 10 KΩ resistor when the interface is not used or connected to an interfacing device
EX_PARITY[1:0]	I/O	• Byte wide parity protection on inbound/outbound transfers.	*Note:* • Can be left as no connect (NC) when the interface is not connected to an interfacing device or not used

Table 100. Schematic Checklist (Sheet 24 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
EX_RDY[3:0]#	I	• HPI Interface ready signals • Pull-up to Platform 3.3V (VCC3) supply through a 10 KΩ ±5% resistor	• These signals are used to halt accesses using expansion bus chip selects 7 through 4 when the chip selects are configured to operate in HPI mode. • There is one EX_RDY# signal per chip select. • The signals only affects accesses that use EX_CS[7:4]# ***Note:*** • Must be pulled high through a 10 KΩ resistor when the interface is not used or connected to an interfacing device
EX_BURST	I	• Expansion bus burst transfer operation	• For inbound transfers, this signal is used to signify that a burst operation is being requested ***Note:*** • Must be pulled high through a 10 KΩ resistor when the interface is not used or connected to an interfacing device
EX_RCOMPP	I/O	• Connect through a 50Ω ±1% resistor to Ground.	Resistive compensation (Positive)
EX_RCOMPN	I/O	• Pull up to EP80579 3.3V (VCC33) supply through a 50Ω ±1% resistor	Resistive compensation (Negative)
Synchronous Serial Port (SSP) Interface			
SSP_SCLK, SSP_SFRM, SSP_TXD, SSP_RXD, SSP_EXTCLK	I/O	Synchronous Serial Port Interface signals • Connect appropriately to the HSS or TDM (Mezzanine) port connectors. • Used for HSS (TDM) port configuration	***Note:*** IF the port is not used, the interface signals should be terminated as follows • SSP_RXD and SSP_EXTCLK must each be pulled high through a 10 KΩ resistor. • SSP_SCLK, SSP_TXD, SSP_SFRM can be left as no connect (NC)
IEEE 1588 Hardware-Assist Interface			
1588_TX_SNAP, 1588_RX_SNAP, 1588_PPS, 1588_TESTMODE_DATA, ASMSSIG, AMMSSIG	I/O	• Connect appropriately 1588 Hardware Assist signals from/to EP80579 and connector or header.	***Note:*** IF the port is not used, the interface signals should be terminated as follows • ASMSSIG and AMMSSIGG must each be pulled down through a 10 KΩ resistor. • 1588_TX_SNAP, 1588_RX_SNAP, 1588_PPS, and 1588_TESTMODE_DATA can be left as no connect (NC)
Miscellaneous I/O Interface			
JTAG ***Note:*** See the application debug port design guide for information.			
TCK		Pull-down to ground through a 51Ω ±5% resistor	
TDI		Pull-up to Platform 1.2V (V1P2) supply through a 51Ω ±5% resistor	

Table 100.   Schematic Checklist (Sheet 25 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
TDO		Pull-up to Platform 1.2V (V1P2) supply through a 51Ω ±5% resistor	
TMS		Pull-up to Platform 1.2V (V1P2) supply through a 51Ω ±5% resistor	
TRST#		Pull-down to ground through a 51Ω ±5% resistor	
BPM3_IN	I	No connect	
BPM4_PRDY_OUT	OD	No external pull-up required	• See Section 26.3.2.2 for more details.
BPM5_PREQ_IN	I	No connect	
BPM[3:0]	I/O	No connect	
Miscellaneous Pins			
PME#	I/O OD	Connect to EP80579 GBE_WAKE output	• 50KΩ internal pull-up
PCIRST#	O	• Leave as no connect. • Use PLTRST# for system reset	See Section 7.2 and Figure 49 for more details
SPKR	O	**No Reboot Strap:** The SPKR signal is sampled at Platform Reset as a functional strap: • This strap controls the re-boot behavior of timeouts in the TCO Timer • 0 = Reboot on second timeout of TCO timer (default) • 1 = No re-boot on second timeout of TCO Timer	SPKR: • This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST#, its output state is 0. • Weak internal pull-down
Reserved Pins			
Reserved0		Must have external 10KΩ pull-down to VSS	
Reserved1		Must have external 10KΩ pull-down to VSS	
Reserved2		Must have external 10KΩ pull-down to VSS	
Reserved3		Must have external 10KΩ pull-down to VSS	
Reserved4		Must have external 10KΩ pull-down to VSS	
Reserved5		Must have external 10KΩ pull-down to VSS	
Reserved6		Must have external 10KΩ pull-down to VSS	
Reserved7		Must be connected to VSS	
Reserved8		Must have external 10KΩ pull-down to VSS	
Reserved9		Must be connected to VSS	

Table 100.   Schematic Checklist (Sheet 26 of 26)

Checklist Items	I/O Type (Default)	Recommendations	Comments
Reserved10		• Must have a 330Ω pull-up to VCCPSUS (EP80579 3.3V sustain power) if used to connect to TESTIN# signal on the ITP Debug Port. • Must have a 10KΩ pull-up to VCCPSUS (EP80579 3.3V sustain power) if not used	
Reserved11		Must be connected to VSS	
Reserved12		Must have external 10KΩ pull-down to VSS	
Reserved13		Must have external 10KΩ pull-down to VSS	
Reserved14		Must have external 10KΩ pull-down to VSS	
Reserved15		Must be connected to VSS	
Reserved16		Must have external 10KΩ pull-up to 3.3V (EP80579 3.3V power)	
Reserved17		Must be connected to VSS	
Reserved18		Must have external 10KΩ pull-down to VSS	
Reserved19 Reserved20		Must have external 10KΩ pull-up to 3.3V (EP80579 3.3V power)	
No Connect Pins *Note:* **(Except for NC56 Pull-down termination, all other No Connect (NC) Pins must be left unconnected)**			
NC_SUS_TWO			
NC_TWO			
NC7			
NC9 - NC22			
NC34 - NC38			
NC40 - NC48			
NC50 - NC55			
NC56		Must have external 10KΩ pull-down to VSS	
NC57-NC59			

28.3 Power Supply Decoupling

Table 101. Decoupling Recommendations (Sheet 1 of 3)

Power/Ground Pin Name	Type	Configuration	Decap	Qty	Component Layout Notes
IA-32 core and Logic Power					
VCC	PWR	1.2V core logic power supply	150 µF	2	
			10 µF	20	
			0.1 µF	5	
VCC33	PWR	3.3V power supply	10 µF	10	
			0.1 µF	3	
VCCPRTC	PWR	3.3V RTC power supply	10 µF	1	
			0.1 µF	2	
VCC50	PWR	5.0V power supply	10 µF	2	
			0.1 µF	5	
VCC25	PWR	2.5V GbE power supply	2.2 µF	1	
			10 µF	1	
			0.1 µF	3	
VCCVC	PWR	IA-32 core -- 1.0V - 1.3V CPU power supply	330 µF	2	
			150 µF	2	
			10 µF	15	
VCC18	PWR	1.8V - DDR2 power supply	10 µF	3	
			0.1 µF	5	
VTTDDR	PWR	0.9V - DDR2 Termination power supply	2.2 µF	2	
			0.1 µF	10	
VCCA[2:1]	PWR	IA-32 core Logic-- 1.2V PLL power supply • Connect to VCC power supply	10 µF	1	
			0.1 µF	2	
VCCTMP18	PWR	1.8V power supply for thermal sensor • Connect to VCC18 power supply (1.8V)			
VCCUSB12	PWR	1.2V USB power supply • Connect to VCC power supply (1.2V)			
VCCAPE	PWR	1.2V PCI Express power supply • Connect to VCC power supply(1.2V)	10 µF	1	
			0.1 µF	3	
VCCRPE	PWR	1.2V PCI Express power supply • Connect to VCC power supply(1.2V)			
VCCSATA	PWR	1.2V SATA power supply • Connect to VCC power supply(1.2V)			

Table 101.   Decoupling Recommendations (Sheet 2 of 3)

Power/Ground Pin Name	Type	Configuration	Decap	Qty	Component Layout Notes
VCCSATA33	PWR	3.3V SATA power supply • Connect to VCC33 power supply(3.3V)			
VCCGBE33	PWR	3.3V GbE power supply • Connect to VCC33 power supply(3.3V)			
Suspend/Resume Power Pins					
VCCSUS1	PWR	1.2V sustain supply for both I/O and core logic	10 µF	2	
			0.1 µF	2	
VCC1P2_USBSUS	PWR	1.2V USB sustain power supply • Connect to VCCSUS1 power supply			
VCCPSUS	PWR	3.3V sustain power supply for I/O logic	10 µF	2	
			0.1 µF	2	
VCCGBEPSUS	PWR	3.3V GbE sustain power supply • Connect to VCCPSUS power supply			
VCCSUS25	PWR	2.5V GbE sustain power supply	10 µF	2	
			0.1 µF	2	
VCC50_SUS	PWR	5.0V sustain power supply	10 µF	2	
			0.1 µF	2	
Analog Power Pins with Filter					
Note: See Section 6.6.5 and Table 13 for Analog Filter guidelines					
VCCARX	PWR	1.2V SATA Analog Power: • connect to VCC (1.2V) with analog filter			
VCCATX	PWR	1.2V SATA Analog Power: • connect to VCC (1.2V) with analog filter			
VCCAPLL	PWR	1.2V SATA Analog Power: • connect to VCC (1.2V) with analog filter			
VCCAUSB12	PWR	1.2V USB Analog Power: • connect to VCC (1.2V) with analog filter			
VCCAHPLL	PWR	1.2V CRU PLL Analog Power • connect to VCC (1.2V) with analog filter			
VCCAPE0PLL12	PWR	1.2V PCI Express Analog power supply • connect to VCC (1.2V) with analog filter			

Table 101. Decoupling Recommendations (Sheet 3 of 3)

Power/Ground Pin Name	Type	Configuration	Decap	Qty	Component Layout Notes
Bandgap Power Pins with Filter					
Note: See Section 6.6.5 and Table 13 for Bandgap Filter guidelines					
VCCASATABG3P3	PWR	3.3V SATA Bandgap power supply • connect to 3.3V (VCC33) with bandgap filter			
VCCABG3P3_USB	PWR	3.3V USB Bandgap power supply • connect to 3.3V (VCC33) with bandgap filter			
VCCABGPO33	PWR	3.3V PCI Express Bandgap power supply • connect to 3.3V (VCC33) with bandgap filter			
Ground Pins					
VSSA	GND	Analog Ground			• The Analog Ground (VSSA) should be isolated from the normal Ground (VSS) on the Platform
VSS	GND	Ground			• The Analog Ground (VSSA) should be referenced to CRU PLL Power supply (VCCAHPLL). • VSSA and VSS are connected together internally in the device

28.4 CK410 Schematic Checklist

For additional information, see the *CK410 Clock Synthesizer/Driver Specification* and the component's datasheet.

Table 102. CK410 Schematic Checklist (Sheet 1 of 3)

Pin Name	System Pull-up/Pull-down	Series Resistor	Recommendations
Note: See the *CK410 Clock Synthesizer/Driver Specification* for more details			
PCIF_0/ITP_EN	• 4.7 KΩ pull-up to Platform 3.3V (VCC3) for ITPCLK • 4.7 KΩ pull-down to GND for SRC_7	33 Ω±1%	• On the Development Board, this pin is pulled high using a 4.7 KΩ resistor to VCC3 to select pins 35 and 36 as ITPCLK. • Customer can use this pin as a PCIF as well. • If used as a PCIF clock as well use multiple 33 Ω±1% series resistors for isolation if the clock signal is shared between multiple devices.
PCIF_1, PCIF_2		33 Ω±1%	Free running PCI Clock Outputs • If not used, can be left as NC. • If used as a PCIF clock use multiple 33 Ω±1% series resistor if the clock signal is shared between multiple devices.

Table 102. CK410 Schematic Checklist (Sheet 2 of 3)

Pin Name	System Pull-up/Pull-down	Series Resistor	Recommendations
SRC[6:1]/SRC[6:1]#	49.9 Ω±1% pull-down to GND	33 Ω±5%	100 MHz Differential Clocks Outputs • Connect to various differential serial reference clocks (PCI-E, SATA, etc.) • If not used, can be left as NC.
DOT96/DOT96#	49.9 Ω±1% pull-down to GND	33 Ω±5%	96 MHz Differential Clock Output • If not used, can be left as NC
PCI[5:0]		33 Ω±1%	33 MHz single-ended PCI Clock Outputs • If not used, can be left as NC. • Use multiple 33 Ω±1% series resistor if the clock signal is shared between multiple devices.
CPU[1:0]/CPU[1:0]#	49.9 Ω±1% pull-down to GND	33 Ω±5%	100/133 MHz EP80579 Core Differential Clock • Connect CPU_0 to EP80579 CLKP100 • Connect CPU_0# to EP80579 CLKN100 • Leave unused clocks as NC
CPU_2/SRC_7, CPU_2#/SRC_7#	49.9 Ω±1% pull-down to GND	33 Ω±5%	Selectable Differential CPU or SRC output • If on-board XDP/ITP is implemented, this pair of clock signals is used for the XDP/ITP connector. Otherwise, it can be routed to the dedicated XDP/ITP clock pins on the processor socket. If no on-board ITP, then this can be used for SRC7. • If not used, can be left as NC
FS_A	1KΩ ±1% pull-up to VCC3		• This pin works in conjunction with FS_B and FS_C to select the CPU clock frequency *Note:* See the *CK410 Clock Synthesizer/Driver Specification* for more details
FS_B/TEST_MODE	1KΩ ±1% pull-down to GND		• This pin works in conjunction with FS_A and FS_C to select the CPU clock frequency *Note:* See the *CK410 Clock Synthesizer/Driver Specification* for more details
FS_C/TEST_SEL	Clk Frequency Strapping Options: • If BSEL = 0 (FSB = 400MTS), connect to VCC3 through 1KΩ ±1% resistor • If BSEL = 1 (FSB = 533MTS), connect to GND through 1KΩ ±1% resistor		• This pin works in conjunction with FS_A and FS_B to select the CPU clock frequency. • Connect using EP80579 BSEL signal to select EP80579 FSB frequency *Note:* See the *CK410 Clock Synthesizer/Driver Specification* for more details
REF		33 Ω±5%	14.318 MHz reference clock output • Can connect to various reference clock devices (ICH, SIO, LPC, etc.) • The REF signal can support 1-3 devices, • Use multiple 33 Ω±1% series resistors to isolate clocks if the clock signal is shared between multiple devices. • Use a clock buffer if the clock signal connects to four or more devices.
IREF	475 Ω ±1% pull-down to GND		• A precision resistor (internal) is attached to this pin, which is connected to the internal current reference. • Connect a 475 Ω ±1% pull-down resistor to this pin

Table 102.   CK410 Schematic Checklist (Sheet 3 of 3)

Pin Name	System Pull-up/Pull-down	Series Resistor	Recommendations
XTAL_IN/XTAL_OUT			• Connect to a 14.318-MHz crystal, placed within 500 mils of CK410 device. • It is recommended to use 33 pF external load capacitors
VTT_PWRGD#/PD			• Connect to Platform VRMPWRGD signal after a 2ms delay. • VTT_PWRGD# is a 3.3V LVTTL input. It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs. After VTT_PWRGD# assertion, it becomes a real time input for asserting power down.
VDD_PCI[1:0], VDD_CPU, VDD_SRC[3:1], VDD_REF, VDD_48, VDD_A			CK410 Power Pins • Connect to VCC3 • See Section 8.3.4 for Power Filtering and Decoupling guidelines
VSS_48, VSS_SRC, VSS_CPU, VSS_PCI[1:0], VSS_REF VSS_A			CK410 Ground Pins • Connect to GND • See Section 8.3.4 for Ground Filtering and Decoupling guidelines

29.0 Reference Design

The EP80579 reference design includes the Development Board schematics, BOMs (Bill Of Materials), and other CAD board files. Contact your Intel field representative to obtain these documents.

Appendix A System Memory Interface (SODIMM)

The EP80579, utilizing next-generation dual-processor server chipset technology, enables reduced power consumption with improved platform reliability and system manageability compared to previous generation server platforms.

EP80579-based platforms can be designed to support various memory speeds, including DDR2-400/533/667/800 MT/s. Certain applications, including those associated with embedded communications market segments, may require smaller form factor memory module solutions, such as SODIMM designs, to benefit from the revolutionary features offered by the EP80579, such as PCI Express*1 serial I/O technology and next generation DDR2 memory technology, which helps increase I/O bandwidth and reduces system latency for data-intensive applications.

The purpose of this chapter is to provide basic board design guidance to customers who are interested in enabling SODIMM DDR2-400/533/667/800 MT/s memory for the EP80579-based platform designs.

The EP80579 has been validated to work with unbuffered DDR2-400/533/667/800 DIMMs. However, the challenges involved with enabling Unbuffered SODIMM DDR2-400/533/667/800 have not been fully explored. These guidelines address some of the possible challenges and best known methods for overcoming the potential issues.

These guidelines do not include the software code necessary for BIOS modification. Although the intention of these guidelines are to cover all aspects relating to implementing a design with unbuffered SODIMM DDR2- 400/533/667/800 with EP80579, it does not guarantee that every possibility has been identified.

Note: Usage of any of the simulation models, topology, and guidelines described in this document should be accompanied with simulations in your own environment to ensure that your implementation will be successful.

The targeted specification for the unbuffered SODIMM DDR2- 400/533/667/800 with EP80579 will be based on 256 MB, 512 MB, 1 GB, and 2 GB memory technology.

Unbuffered SODIMM DDR2-400/533/667/800 design on EP80579 has NOT been validated by Intel and the data provided in these guidelines are the results from simulation only.

Note: The simulation results and guidelines provided in this document are based on simulation topologies composed of EP80579 Memory Controller interfacing to simulation models from SODIMM Memory Modules with Micron devices. To date, there have been no reported SODIMM issues with Samsung or Micron memory devices. Customers that report instability with certain SODIMMs have reported that Samsung and Micron devices are stable. Intel is not specifically recommending either of these two SODIMM options, just sharing information gathered from customer feedback. However, customers are reminded to simulate and validate their EP80579-based platform designs when using SODIMM Modules with other vendor devices.

A.1 Terminology and Definitions

Table A-1. DDR Terminology

Acronym	Description/Comment
Unbuffered memory	Memory that does not contain buffers or registers located on the module. The memory controller directly communicates with the memory devices.
Buffered memory	Memory that contains buffers on the module that re-drive signals from the memory controller to the memory devices. ***Note:*** EP80579 does not support this feature.
Registered memory	Memory that contains registers on the module that register and re-drives the signals from the memory controller to the memory devices.
Self-refresh	Memory technology that is built in the DRAM that refreshes on its own.
Page size	Minimum number of column locations on any row and are accessed by a single ACTIVATE command
DRAM devices	Multiple DRAM devices together make up a DIMM
DIMM	Dual Inline Memory Module
SODIMM	Small Outline Dual Inline Memory Module
Rank	Defines a set of DRAM chips (on a module) comprising 8 byte wide (64/32 bits) data, or 9 bytes (72/40 bits) with ECC. All devices in a Rank are connected by a single chip select. The actual memory size is not defined. Single-sided memory modules are always single-rank. Double-sided unbuffered and registered DIMMs are always dual-rank.

A.2 Supported Configurations

Table A-2 shows the various DDR2 SODIMM memory configurations, including capacities and technologies, supported by the EP80579.

Table A-2. Supported SODIMM Memory Capacity for 64-bit Mode

Total DRAM Capacity	Technology		Total # of parts (without ECC)
	DRAM Density	DRAM Part Width	
256 MB	256 Mb	x8	8
512 MB	512 Mb	x8	8
1 GB	1 Gb	x8	8
2 GB	2 Gb	x8	8

A.3 Differences between Unbuffered SODIMM and Unbuffered DIMM

The main difference between Unbuffered SODIMM and Unbuffered DIMMs is that an unbuffered non-ECC DIMM requires three input clocks, whereas an Unbuffered SODIMM only requires two input clocks, with no support for ECC. Typical DIMM pins include the place holder pins for ECC functions.

Table A-3. DDR2 Unbuffered SODIMM and Unbuffered DIMM Pin Comparison Table

	SODIMM (200 pins)	DIMM (240 pins)
Signal	**# of pins**	**# of pins**
VDD (SDRAM Core Power Supply)	12	12
VDDQ (SDRAM I/O Driver Power Supply)	0	10
VREF (SDRAM I/O Reference Power Supply)	1	1
VSS (Ground)	57	64
DQ (SDRAM Memory Data Bus)	64	64
DQS/DQS# (SDRAM Data Strobes)	16	18
DM (SDRAM Data Masks)	8	9
ECC (SDRAM ECC Check Bits)	0	8
CK/CK# (SDRAM Clocks)	4	6
Address (SDRAM Address Bus)	19	19
CMD (SDRAM Command Signals)	3	3
CS#/CKE (Chip Select and Clock Enable)	4	4
ODT (On die Termination)	2	2
SPD (Serial Presence Detect)	5	6
NC/RC/TEST	5	21
Total	**200**	**240**

A.4 SODIMM System Memory Design Guidelines

This section provides an example of the solution space as a result from simulation. These simulation results *have not been physically validated by Intel and is to be used for reference purposes only*. The values suggested in this section (resistor, trace length, breakout length, etc.) may not provide the only possible solution space. There can be different setups that may be equally feasible. Thorough simulations, careful layout implementation, and vigorous stress testing and validation must be performed to ensure that the design is robust if other design options are considered.

A.4.1 SODIMM DDR2 Signal Groups

The EP80579 has a single channel memory interface. The channel consists of 64 data bits with no ECC support. The pinout for the channel has been optimized for a baseboard design with one SODIMM.

The system memory interface can be divided into five signal groups:

- source synchronous (data)
- address/command
- control
- clocks
- DC bias signals

Table A-4 summarizes the different signal groupings:

Table A-4. DDR2 Signal Groups

Group	Signal Name	Description
Data, Mask, & Strobe		
Byte 0	DDR_DQ[0..7], DDR_DM0, & DDR_DQS0/DQS0#	Data Byte Lane0
Byte 1	DDR_DQ[8..15], DDR_DM1, & DQS1/ DDR_DQS1#	Data Byte Lane1
Byte 2	DDR_DQ[16..23], DDR_DM2, & DQS2/ DDR_DQS2#	Data Byte Lane2
Byte 3	DDR_DQ[24..31], DDR_DM3, & DQS3/ DDR_DQS3#	Data Byte Lane3
Byte 4	DDR_DQ[32..39], DDR_DM4, & DDR_DQS4/DQS4#	Data Byte Lane4
Byte 5	DDR_DQ[40..47], DDR_DM5, & DDR_DQS5/DQS5#	Data Byte Lane5
Byte 6	DDR_DQ[48..55], DDR_DM6, & DDR_DQS6/DQS6#	Data Byte Lane6
Byte 7	DDR_DQ[56..63], DDR_DM7, & DDR_DQS7/DQS7#	Data Byte Lane7
Control		
Control	DDR_CKE[1:0]	Clock Enables
	DDR_CS#[1:0]	Chip Selects
	DDR_ODT[1:0]	On-Die-Termination
Address & Command		
Address / Command	DDR_MA[14:0]	Memory Address
	DDR_BA[2:0]	Bank Address (Bank Select)
	DDR_RAS#	Row Address Select
	DDR_CAS#	Column Address Select
	DDR_WE#	Write Enable
Clocks		
Clocks	DDR_CLK[1:0]/ DDR_CLK#[1:0]	Differential Clocks
DC Bias		
DC Bias (I/O)	DDR_CRES[2:0]	• DDR_CRES[2:1] - Impedance compensation resistors. • DDR_CRES[0] - Common return for DDR2 interface compensation resistors on DDV_CRES, DDR_SLWCRES and DDR_RCOMPX
	DDR_SLWCRES	Slew rate compensation for DDR2 interface (Analog)
	DDR_RCOMPX	Impedance compensation for DDR2 interface
	DDV_CRES	DDR2 resistor
	DDR_VREF	Voltage Reference (Analog)

A.4.2 Package Length Compensation

Package length compensation is required for total routing length requirements, see the length matching rules listed in Table A-5, "Length Matching Formulas between EP80579 and DDR2 SODIMM" on page 320. See the DDR2 package length information in the *Intel® EP80579 Integrated Processor Product Line Datasheet*.

A.4.3 Length Matching and Length Formulas

The routing guidelines presented in the following subsections define the recommended routing topologies, trace width, spacing geometries, and absolute minimum and maximum routed lengths for each signal group. These guidelines are recommended to achieve optimal signal integrity and timing.

Table A-5. Length Matching Formulas between EP80579 and DDR2 SODIMM

Source/ Destination	Signal Group to matching signal	Total Length Matching Tolerances	Notes
EP80579 Pad to DDR2 SODIMM	DQS to DQ/DM	Min DQS = Min(DQ/DM) - 200 mils Max DQS = Max(DQ/DM) - 200 mils	1, 2
	DQS to clock	DQS = CLK/CLK# ± 500 mils	2
	CMD/ADD to Clock	CMD/ADD = CLK/CLK# ± 20 mils	2
	CTRL to CMD/ADD	Total CTRL Length = Total (CMD/ADD Length) + 3.0 inches	2
	Clock to Clock#	CLK[x] = CLK[x]# ±10 mils	2

Notes:
1. Length matching is only required within each Byte lane. Signal length matching is not required outside the Byte lane. For example, any signal within DQ [0:7] need not be length matched to DQS [3].
2. Total length means - L_{PKG} + L_{BREAK} + L_{ROUTE}

A.4.4 DDR2 Interface System Interconnect

Figure A-1 provides a block diagram of the system interconnect between the EP80579 DDR2 Memory Controller and the SODIMM for the signal groups provided in Table A-4. The Command/Address and Control signals require external terminations. External terminations are not required for DQ and DQS signals since both the EP80579 and the SDRAMs contain internal ODT. The following sections provide the detailed topology and routing guidelines for each of the signal groups.

Figure A-1. DDR2 Interfaced System Interconnect
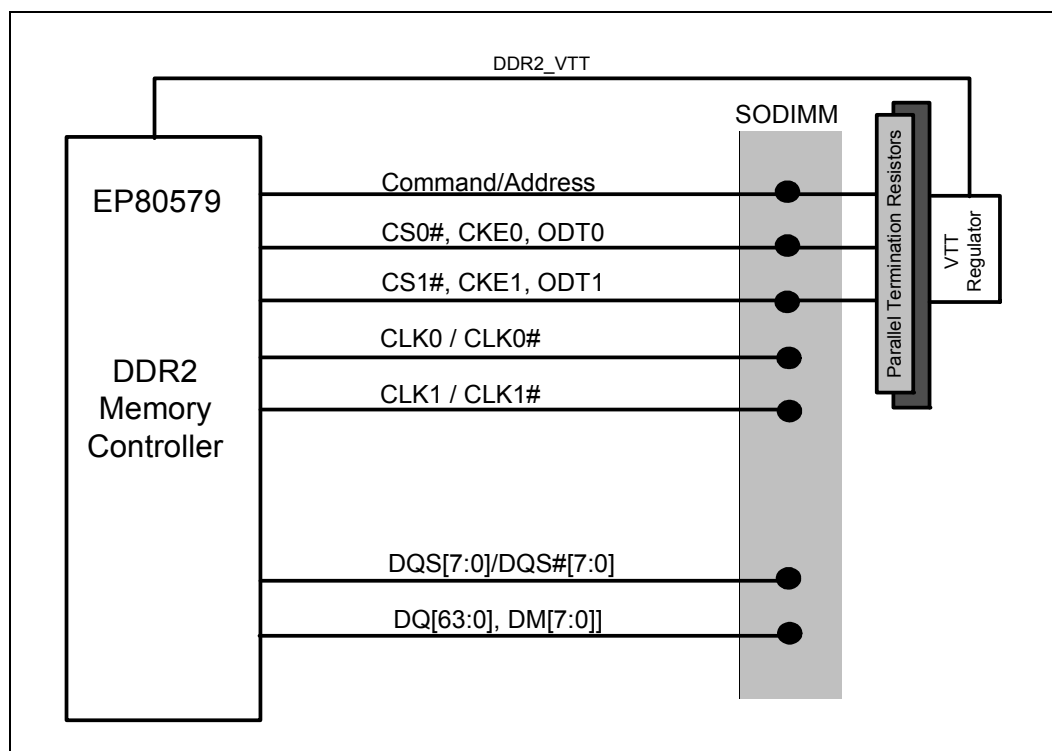
A.4.5 Topologies and Routing Guidelines

A.4.5.1 DDR2 Data and Strobe Signals – DQ/DM/DQS

The Data and Strobe topology shown in Figure A-2 is the same for each Data Byte Group (See Table A-4). The DQS signals must be routed as differential pair within inter-pair skew of ± 10mils. All signals in same byte lane should be matched within 20 mils of each other. (For example, DQS0[+/-], DQ[0..7] and DM0 are in the same byte lane).

All trace impedances should be 40 ohm± 10%. The parameters provided in Table A-6 are targeted for 40 ohm.

Figure A-2. Data/Mask/Strobe Signal Routing Topology Diagram

Table A-6. Data and Strobe Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines		Figure
	Data Byte Lane		
	Data & Data Mask	**Strobe**	
Signal Group	Data & Mask (DQ & DM)	Byte Strobe (DQS/DQS#)	
Topology	Point-to-Point		
Reference Plane	Ground Referenced		
Characteristic Trace Impedance (Zo)	Single Ended Impedance: 40Ω ±10%		
Layer assignment	• Layers 3/8 • Signals within the same Byte Lane must routed on the same layer		
Nominal Trace Width	B= C = D = 6.5 mils		Figure A-2
Trace-to-Trace spacing (e2e)	B = C = D = 3 x Trace Width (min)	• Inter-pair Spacing:-- DQS/DQS# = 6 mils (min) • Pair-to-Pair Spacing: 20 mils (min)	Figure A-2
Clearance from other signals	20.0 mils (min)		

Table A-6.   Data and Strobe Signal Group Routing Guidelines (Sheet 2 of 2)

| Parameter	Routing Guidelines		Figure
	Data Byte Lane		
	Data & Data Mask	**Strobe**	
Board Routing Guidelines			
Total Trace Length (TTL) = (L_{PKG} + $L_{BREAKOUT}$ + L_{ROUTE} + $L_{BREAKIN}$)	2.0 in - 5.0 in	• Min TTL (DQS/DQS#) = Min TTL (DQ/DM) - 200 mils • Max TTL (DQS/DQS#) = Max TTL (DQ/DM) - 200 mils	Figure A-2
L_{PKG}	See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information.		
$L_{BREAKOUT}$	B = 0.8 in (max)		
L_{ROUTE}	C = 1.0 in - 4.0 in		
$L_{BREAKIN}$	D = 0.8 in (max)		
Length/Skew Matching Rules			
Length Tuning Requirements	• Only length matching is required within each Byte lane. No signal length matching is required outside the Byte lane. For example, any signal within Data Byte Lane 0 (DQ [0...7]) need not be length matched to DQS1 • DQ/DM should match each other to 20 mils or less within the same byte lane.	• The trace length difference between DQS and DQS# should not be more than 10 mils. - that is, DQS[x] = DQS[x]#±10 mils, x = 0.. 7 • Length match the data strobes (DQS/DQS#) to the associated data mask and data (DQ/DM) signals for each Data Byte Lane: • Min TTL (DQS/DQS#) = Min TTL (DQ/DM) - 200 mils • Max TTL (DQS/DQS#) = Max TTL (DQ/DM) - 200 mils	
Routing Rules			
Layer Routing Requirements	Signals within a data byte lane must be routed on the same layer.		
DQS-to-Clock		Length match Strobe (DQS/DQS#) to Clock (CLK/CLK#) to within 500 mils: • DQS/DQS# = CLK/ CLK# ± 500 mils	

A.4.5.2 DDR2 Clock Group Signals - DDR_CLK[1:0]/DDR_CLK#[1:0]

The clock signal group for the SODIMM comprises of two differential clock pairs. The differential clock pairs must be point-to-point routed from the EP80579 to the SODIMM and must maintain the correct isolation spacing from other signals. Additionally, it is important to maintain the correct spacing and length matching between the pair to protect the differential integrity.

Figure A-3 and Table A-7 depict the recommended topology and layout routing guidelines for the DDR2 differential clocks. Route differential pair signals on the same layer. No external terminations are required for the clock signals because they are terminated on the SODIMM.

Figure A-3. DDR2 Point-to-Point Clock Routing Diagram
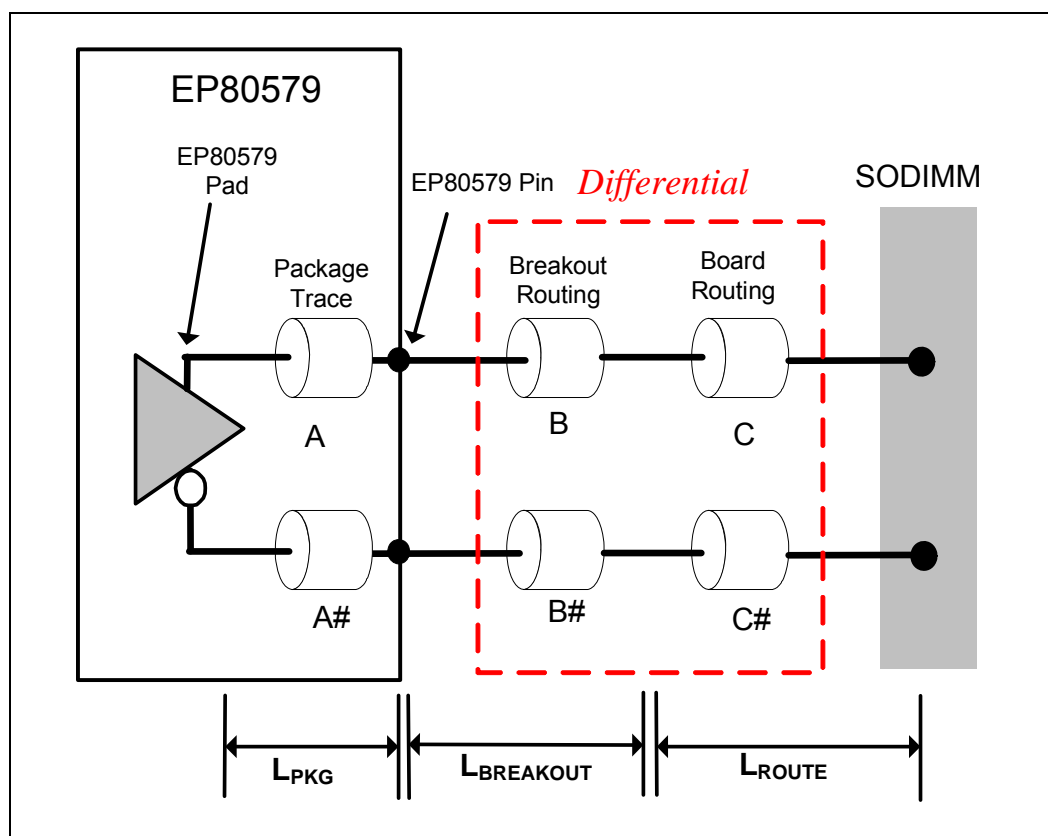
Table A-7. Clock Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines for SODIMM	Figure
Signal Group	CLK/CLK#[1:0] - SODIMM	
Topology	Point-to-Point (Differential)	Figure A-3
Reference Plane	Ground Referenced	
Layer Assignment	Layers 3/8 (Route Clock group on the same layer)	
Characteristic Trace Impedance (Zo)	Single Ended Impedance: 40Ω ±10%	Figure A-3
Nominal Trace Width	6.5 mils for L3/L8	Figure A-3

Table A-7.   Clock Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guidelines for SODIMM	Figure
Inter-pair Trace Spacing(e2e) (CLK to CLK# spacing)	6.0 mils	Figure A-3
Pair-to-Pair Spacing (e2e)	20.0 mils	
Clearance from other signals groups	20.0 mils	Figure A-3
Board Routing Guidelines		
Total Trace Length (TTL) = (L_{PKG} + $L_{BREAKOUT}$ + L_{ROUTE})	1.0 in - 5.0 in	
L_{PKG}	See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information.	
$L_{BREAKOUT}$	Max = 0.8 in	
L_{ROUTE}	Max = 4.0 in	
Length/Skew Matching Rules		
	• The clock differential pairs need to match in length within ± 10 mils (CLK[x] = CLK[x]# ± 10 mils, x= 0.. 1) • Clock pairs should be matched in length to other clock pairs within ± 20 mils • Clock signals should be matched in length to CMD/ADD within ± 20 mils. (CLK/CLK# = CMD/ADD ± 20 mils)	

A.4.5.3   DDR2 Control Signals – DDR_CS[1:0]#, DDR_ODT[1:0], DDR_CKE[1:0]

In the EP80579 memory configuration, the DDR_CKE, DDR_ODT, and DDR_CS# signals make up the control signal group. EP80579 provides six signals: DDR_CS[1:0]#, DDR_ODT[1:0], and DDR_CKE[1:0] as control signals for two-rank memory support. On the SODIMM, one chip select signal, one ODT control line, and one clock enable signal are required for each rank. Figure A-4 provides the inter-connect implementation of the control signals to the SODIMM.

A.4.5.3.1   ODT Settings

Table A-8 and Table A-9 provides the DDR2 Controller and SODIMM ODT settings for write and read operations to/from single-rank and dual-rank SODIMM modules.

Table A-8.   Write Operation ODT Table

SODIMM Module	Write Target	Controller Configuration	SODIMM Configuration	
			Rank0	Rank1
1-Rank (SR)	Rank0	ODT Off	ODT Off	n/a
2-Rank (DR)	Rank0	ODT Off	ODT Off	150 Ω
2-Rank (DR)	Rank1	ODT Off	150 Ω	ODT Off

Table A-9.   Read Operation ODT Table

SODIMM Module	Write Target	Controller Configuration	SODIMM Configuration	
			Rank0	Rank1
1-Rank (SR)	Rank0	120 Ω	ODT Off	n/a
2-Rank (DR)	Rank0	120 Ω	ODT Off	150 Ω
2-Rank (DR)	Rank1	120 Ω	150 Ω	ODT Off

Figure A-4.   DDR2 Control Signals- Implementation
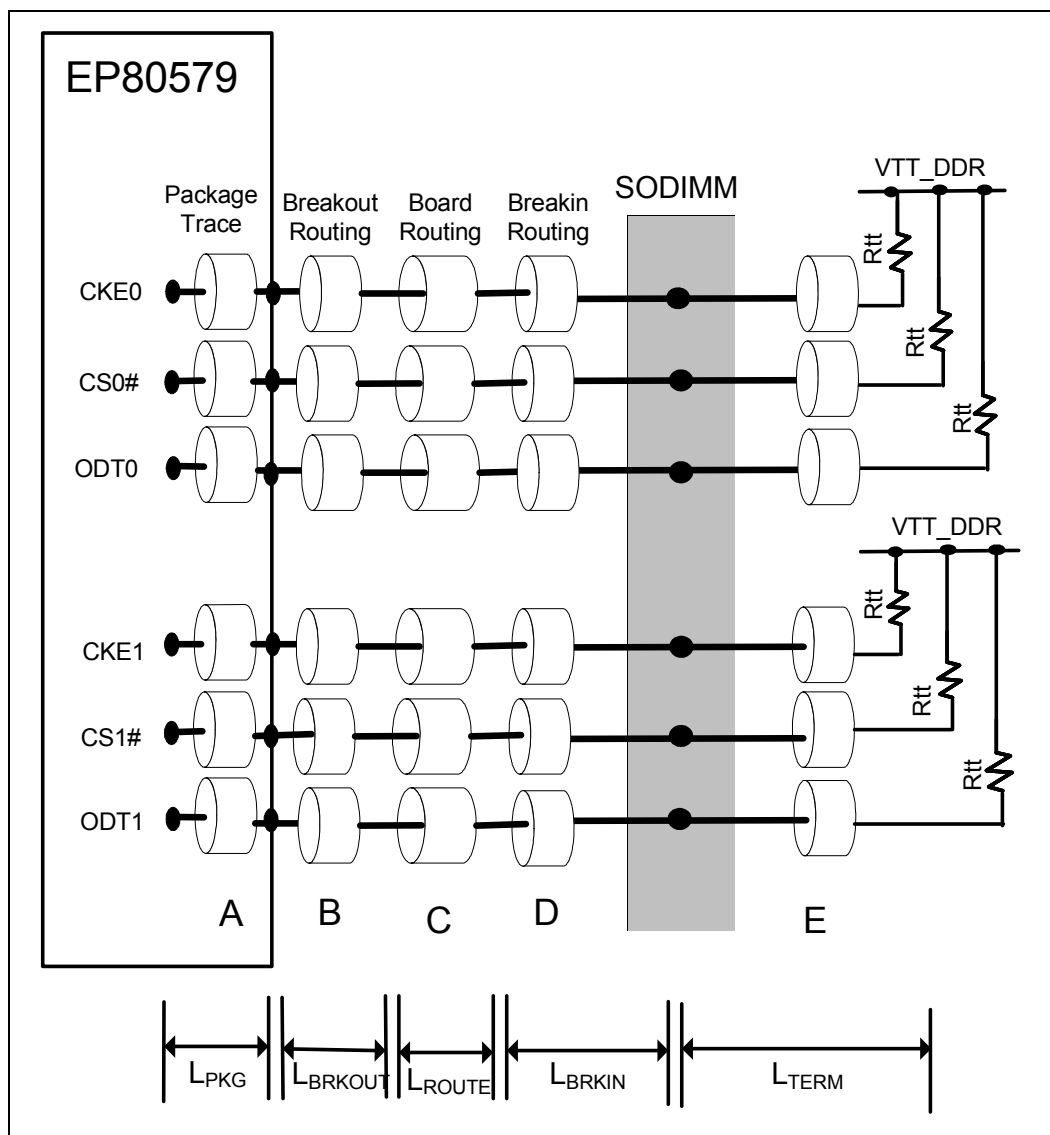
Table A-10. DDR2 Control Signal Group Routing Guidelines

Parameter	Routing Guidelines for SODIMM	Figure
Signal Group	Control Signals (CS#/ODT/CKE)	
Topology	Point-to-Point	
Reference Plane	Ground Referenced	
Layer Assignment	Layers 3/8	
Characteristic Trace Impedance (Zo)	40 Ω ±10%	Figure A-4
Nominal Trace Width	6.5 mils	Figure A-4
Nominal Trace Spacing (e2e)	3X Trace Width	Figure A-4
Clearance from other signals	20 mils (min)	
Board Routing Guidelines		
Total Trace Length (TTL) = (L_{PKG} + $L_{BREAKOUT}$ + L_{ROUTE} + $L_{BREAKIN}$)	• TTL (CTRL) = 1.0 in - 7.5 in • TTL (CTRL) = TTL (CMD/ADD) + 3 in	
L_{PKG}	See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information.	
$L_{BREAKOUT}$	Max = 0.8 in	
L_{ROUTE}	Max = 6.5 in	
$L_{BREAKIN}$	Max = 0.8 in	
L_{TERM}	Max = 500 mils • Trace length skews for the control signals to the termination resistors (L_{TERM}) should not exceed 200 mils.	
On-Board Termination		
Parallel Termination Resistor (Rtt)	75 Ω ±1%	Figure A-4
Length/Skew Matching Rules		
Length Tuning Requirements	• The control signals need to match in length within ± 20 mils of each other.	

A.4.5.4 Address and Command Signals – DDR_MA[14:0], DDR_BA[2:0], DDR_RAS#, DDR_CAS#, DDR_WE#

The address/command signals shown in Table A-11 are source-clocked signals.

Table A-11. Address and Command Signals

Signal Description	Signal Name
System Memory Address Signals	DDR_MA[14:0]
Bank Addresses	DDR_BA[2:0]
Row Address Select	DDR_RAS#
Column Address Select	DDR_CAS#
Write Enable	DDR_WE#

The address/command signals are source-clocked signals that include 15 system memory address signals (MA[14:0]), 3 bank addresses (BA[2:0]), row address select (RAS#), column address select (CAS#), and write enable (WE#). The address/command signals are "clocked" into the SODIMM using the positive edge of the differential clock signals. The EP80579 drives the address/command and clock signals together.

Resistor packs are acceptable for the parallel (R_{TT}) address/command termination resistors, but address/command signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, or control signals.

Figure A-5, and Table A-12 show the recommended topology and layout routing guidelines for the DDR2-SDRAM address/command signals. Do not change layers. Place the parallel termination resistors close to the SODIMM.

Figure A-5. Address/Command With Parallel Termination Topology Diagram

Table A-12. DDR2 Address/Command Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines for SODIMM	Figure
Signal Group	DDR_MA[14:0], DDR_BA[2:0], DDR_RAS#, DDR_CAS#, DDR_WE#	
Topology	Point-to-Point	
Reference Plane	Ground Referenced	
Layer Assignment	Layers 3/8	
Characteristic Trace Impedance (Zo)	40 Ω ±10%	Figure A-5
Nominal Trace Width	6.5 mils	Figure A-5
Nominal Trace Spacing (e2e)	3X Trace Width	Figure A-5
Clearance from other signals	20 mils (min)	
Board Routing Guidelines		
Total Trace Length (TTL) = (L_{PKG} + $L_{BREAKOUT}$ + L_{ROUTE} + $L_{BREAKIN}$)	1.0 in - 4.5 in	
L_{PKG}	See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information.	

Table A-12. DDR2 Address/Command Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guidelines for SODIMM	Figure
L$_{BREAKOUT}$	Max = 0.8 in	
L$_{ROUTE}$	Max = 4.0 in	
L$_{BREAKIN}$	Max = 0.8 in	
L$_{TERM}$	Max = 500 mils • Trace length skews for the ADD/CMD signals to the termination resistors (L$_{TERM}$) should not exceed 200 mils.	
On-Board Termination		
Parallel Termination Resistor (Rtt)	100 Ω ±5%	Figure A-5
Length/Skew Matching Rules		
Length Tuning Requirements	• ADD/CMD signals should match in length within 20 mils of each other.	
Routing Rules		
CLK-to-CMD/ADD Requirements	• Clock signals should match CMD/ADD signals in length within 20 mils max.	

A.4.6 DC Bias Signals

The DC bias signals consist of DDR_SLWCRES, DDR_RCOMPX, DDR_CRES[2:0], DDV_CRES, and DDR_VREF. The routing guidelines for these signals are described in the following sections.

A.4.6.1 DDR_SLWCRES, DDR_RCOMPX, DRV_CRES, & DDR_CRES0

The DDR_SLWCRES, DDR_RCOMPX, DRV_CRES, and DDR_CRES0 signals are compensation resistors for slew rate, impedance, and common return, respectively. Intel recommends 20 mil wide traces with a minimum spacing of 12 mils from other signals. When breaking out from the EP80579, maintain a minimum spacing of 4.5 mils up to a maximum length of 500 mils. For the best signal integrity, minimize this length as much as possible. Figure A-6 shows the routing topology for these signals.

Figure A-6. DDR_SLWCRES, DDR_RCOMPX, DDV_CRES, & DDR_CRES0 Routing Topology
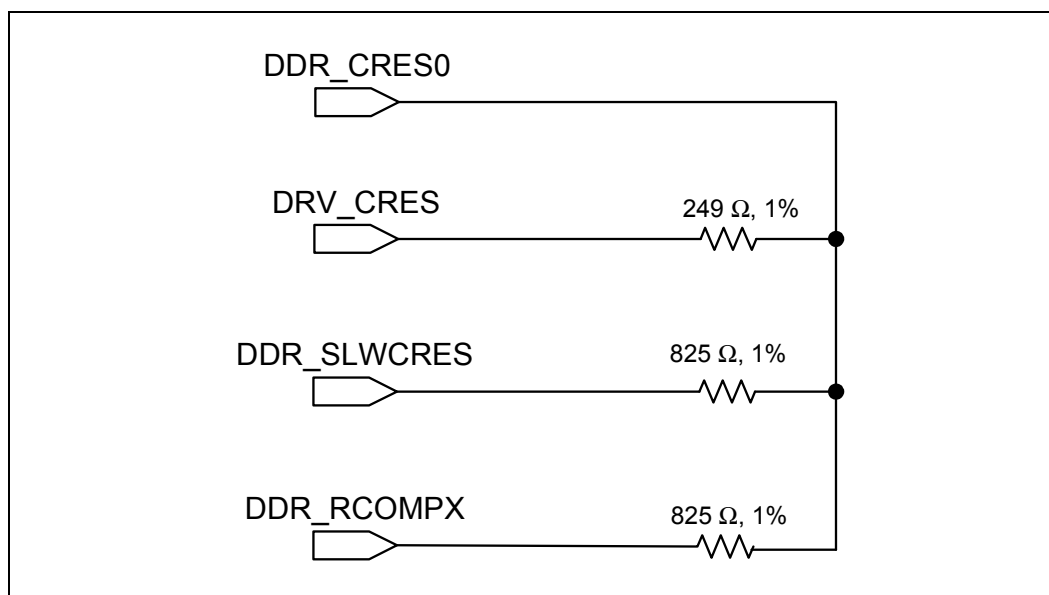
A.4.6.2 DDR_CRES1, DDR_CRES2

The EP80579 provides the DDR_CRES1 and DDR_CRES2 signals as additional compensation resistors (See Figure A-7). Intel recommends 20 mil wide traces with a minimum spacing of 12 mils from other signals. When breaking out from the EP80579, maintain a minimum spacing of 4.5 mils spacing up to a maximum length of 500 mils. For the best signal integrity, minimize this length as much as possible.

Figure A-7. DDR_CRES1 and DDR_CRES2 Signal Connections
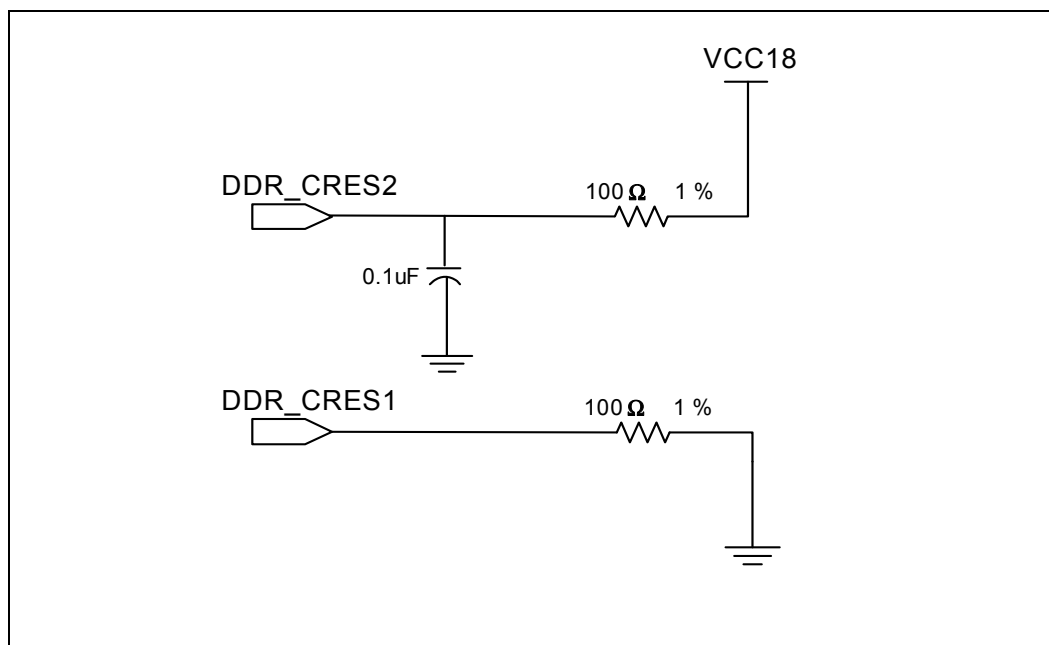
A.4.6.3 DDR2 Reference Voltage, DDR_VREF

The DDR2 system memory reference voltage (DDR_VREF) is used by the DDR2-SDRAM devices to compare the input signal levels of the data, command, and control signals. The DDR2-SDRAM DDR_VREF must be generated as shown in Figure A-8. Generate DDR_VREF from a typical resistor divider using 0.1% tolerance resistors, with a 0.01 µF cap tied to DDR_VREF. The DDR_VREF divider resistors must be placed as close to possible to the SODIMM. The DDR_VREF must be decoupled locally at the SODIMM connector. Finally, the DDR_VREF signal must be routed with as wide a trace as possible. Table A-13 provides the routing and component guidelines for the Vref circuit. Intel recommends at least a 20 mil wide trace with a minimum spacing of 12 mils from other signals.

Figure A-8. DDR_VREF Generation Example Circuit
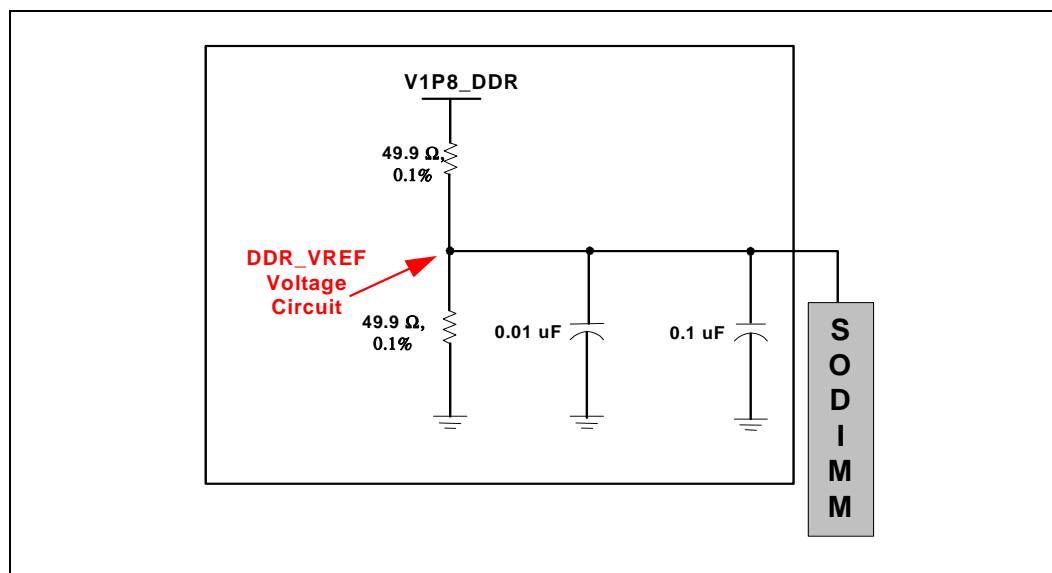
Table A-13. DDR V$_{REF}$ Generation Requirements

Parameter	Guideline
Nominal Trace Width	20 mils
Voltage Divider	Place resistor divider consisting of two resistors as close as possible to SODIMM.
Decoupling requirements	0.01 µF and 0.1µF capacitors
Decoupling placement	Place decoupling caps as close as possible to SODIMM (Figure A-8)

A.5 Decoupling Recommendations

When designing a board, the following decoupling recommendations should be followed:

- Capacitors should be mounted as close to the EP80579 as possible. They should be no further than 10mm from the edge of the EP80579 package for the DDR2 channel.
- Decoupling caps should be placed near any signal reference layer change. This can be done by adding a 0.1µF capacitor between DDR Power and Ground where the Memory Clock traces change reference layers.

Note: These decoupling recommendations are for the EP80579 pins. Place multiple capacitors in parallel to get the desired value for capacitance and ESL.

A.6 Clock Delay Programming and Write Levelization

The EP80579 primary memory clocks CK[1:0]/CK[1:0]# have write levelization circuitry, WDLL.

Because of difference in loading between CTRL signals and CMD/ADD signals, flight time skew between these two signal groups could be substantial. This is more pronounced in the case of raw cards E and F where Control signals have 8 SDRAM loads respectively and CMD/ADD signals have 16 loads respectively.

Since both signals (CTRL and CMD) are latched on the same clock crossing, therefore clock needs to be positioned as close as possible to the middle of both CTRL and CMD valid windows. Positioning the clock into the optimal window is enabled by controlled push out of clock WDLL.

The clock WDLL can be pushed out up to one clock cycle in a 32 incremental steps. Because relative position of valid CTRL and Valid CMD center may vary depending on memory speed and silicon and board skews, this value could be different for different raw cards, and different speeds.

In the case where this is not possible, and CTRL requirement conflicts with CMD requirement with respect to positioning the clock crossing point, priority goes to the Ctrl signal, CMD signals are then switched to the 2T timing mode. The priority is dictated by the architectural requirement that the Chip Select (CS#) has always to toggle in 1T and can not be scaled down to 2T. In other words, we have to satisfy CS# 1T timing first, then try to tune the Clock WDLL to accommodate the CMD signals whenever possible, or switch the CMD signals to 2T timing.

A.6.1 SODIMM Write Levelization Values

Table A-14 andTable A-15 provide the Write Levelization settings for single-rank and dual-rank SODIMM modules.

Table A-14. Write Levelization for Single Rank Configuration

Data Rate	Number of Clock Push Out
400 MT/s	20
533 MT/s	12
667 MT/s	11
800 MT/s	8

Table A-15. Write Levelization for Dual Rank Configuration

Data Rate	Number of Clock Push Out
400 MT/s	7
533 MT/s	8
667 MT/s	13
800 MT/s	14

Appendix B System Memory Interface (Memory Down)

This chapter contains topologies and routing guidelines for the system memory interface signal group of the DDR2 interface. It provides the DDR2 implementation solution for system designs requiring memory down topologies, unbuffered or registered, operating at 400/533/667/800 MT/s speed rates.

The EP80579 integrates a single-channel DDR2 system memory controller with a single, 64-bit wide interface. The memory controller buffers support the SSTL_18 (1.8 V) logic switching range only. The memory controller interface is fully configurable through a set of control registers.

The EP80579 has been validated to work with unbuffered and registered DDR2-400/533/667/800 DIMMs. However, memory down configurations enabling unbuffered or registered DR2-400/533/667/800 have not been fully explored. Memory down configurations involve designs in which the memory devices are soldered onto the motherboard. These guidelines address some of the possible challenges and best known methods for designs using memory down configurations.

Note: Although these guidelines are intended are to cover all aspects relating to implementing a design with unbuffered or registered memory down DDR2- 400/533/667/800 configurations with EP80579, it does not guarantee that every possibility has been identified.

Note: Unbuffered or registered memory down DDR2-400/533/667/800 design configurations on EP80579 has NOT been validated by Intel and the data provided in these guidelines are the results from simulation for single rank topologies only. Usage of any of the simulation models, topology, and guidelines described in this document should be accompanied with simulations in your own environment to ensure that your implementation will be successful.

B.1 Terminology and Definitions

Table B-16. DDR Terminology (Sheet 1 of 2)

Acronym	Description/Comment
Unbuffered memory	Memory that does not contain buffers or registers located on the module. The memory controller directly communicates with the memory devices.
Buffered memory	Memory that contains buffers on the module that re-drive signals from the memory controller to the memory devices. *Note:* The EP80579 does not support this feature.
Registered memory	Memory that contains registers on the module that register and re-drives the signals from the memory controller to the memory devices.
Self-refresh	Memory technology that is built into the DRAM that refreshes on its own.

Table B-16. DDR Terminology (Sheet 2 of 2)

Acronym	Description/Comment
Page size	Minimum number of column locations on any row and are accessed by a single ACTIVATE command
DRAM devices	Multiple DRAM devices together make up a DIMM.
Rank	Defines a set of DRAM chips (on a module) comprising 8-byte wide (64/32 bits) data, or 9-bytes (72/40 bits) with ECC. All devices in a Rank are connected by a single chip select. The actual memory size is not defined. Single-sided memory modules are always single-rank. Double-sided unbuffered and registered DIMMs are always dual-rank.

B.2 Supported Configurations

Table B-17 shows the various DDR2 device density technologies supported by the EP80579.

Table B-17. Supported DDR2 Device Densities and Widths

Technology		Support
Device Density	**Device Width**	
256 Mb	x8	Supported
512 Mb	x8	Supported
1 Gb	x8	Supported
2 Gb	x8	Supported
4 Gb	x8	Not Supported

B.2.1 Supported DRAM Capacities

Table B-18 shows the various capacity configurations supported by the memory controller in the 64b mode. The first column shows the total DRAM capacity on the channel. The remaining columns indicate the DRAM devices features, densities, width, and the number of devices required to achieve the given capacity. Table B-18 assumes single rank configurations only because dual-rank memory down configurations are not supported by the EP80579.

Table B-18. Supported DRAM Capacity for 64-bit Mode

Total DRAM Capacity	DRAM Technology		Total # of parts (without ECC)
	DRAM Part Density	**DRAM Part Width**	
256 MB	256 Mb	x8	8
512 MB	512 Mb	x8	8
1 GB	1 Gb	x8	8
2 GB	2 Gb	x8	8

Table B-19 shows the various configurations supported by the memory controller in the 32b mode.In the 32-bit mode only single rank DDR2 devices are supported. In this mode, the minimum capacity supported by the memory controller is 128 MB and the maximum capacity supported is 1 GB.

Table B-19. Supported DRAM Capacity for 32-bit Mode

Total DRAM Capacity	DRAM Technology		Total # of parts (without ECC)
	DRAM Density	DRAM Part Width	
128 MB	256 Mb	x8	4
256 MB	512 Mb	x8	4
512 MB	1 Gb	x8	4
1GB	2 Gb	x8	4

Note: In the 32b mode, all EP80579 unused data bus bits (DQ[63:33]/DQS[7:4]/DM[7:4]) should be pulled high through 10 Kohm resistors.

B.3 DRAM Addressing

Table B-20, Table B-21, Table B-22 and Table B-23 show the DRAM device addressing for the various DDR2 device technologies and densities supported by the memory controller.

Note that:

- x4 and x 16 devices are not supported.
- 4Gb and higher device density parts are not supported.
- See Table B-17 for the supported device technologies.

Table B-20. 256Mb Addressing

Configuration	DDR2 32 Mb x 8
# of Banks	4
Bank Address	BA0, BA1
Auto Precharge	A10
Row Address	A0-A12
Column Address	A0-A9
Page Size	1KB

Table B-21. 512Mb Addressing

Configuration	DDR2 64 Mb x 8
# of Banks	4
Bank Address	BA0, BA1
Auto Precharge	A10
Row Address	A0-A13
Column Address	A0-A9
Page Size	1KB

Table B-22. 1Gb Addressing

Configuration	DDR2 128 Mb x 8
# of Banks	8
Bank Address	BA0-BA2
Auto Precharge	A10
Row Address	A0-A13
Column Address	A0-A9
Page Size	1KB

Table B-23. 2Gb Addressing

Configuration	DDR2 256 Mb x 8
# of Banks	8
Bank Address	BA0-BA2
Auto Precharge	A10
Row Address	A0-A14
Column Address	A0-A9
Page Size	1KB

B.4 DDR2 Signal Groups

Table B-24 summarizes the different signal groupings of the DDR interface. See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for more details on specific pin functionality.

Table B-24. DDR2 Signal Groups (Sheet 1 of 2)

Group	Signal Name	Description
Data, Mask, & Strobe		
Byte 0	DDR_DQ[0..7], DDR_DM0, & DDR_DQS0/DQS0#	Data Byte Lane0
Byte 1	DDR_DQ[8..15], DDR_DM1, & DQS1/ DDR_DQS1#	Data Byte Lane1
Byte 2	DDR_DQ[16..23], DDR_DM2, & DQS2/ DDR_DQS2#	Data Byte Lane2
Byte 3	DDR_DQ[24..31], DDR_DM3, & DQS3/ DDR_DQS3#	Data Byte Lane3
Byte 4	DDR_DQ[32..39], DDR_DM4, & DDR_DQS4/DQS4#	Data Byte Lane4

Table B-24. DDR2 Signal Groups (Sheet 2 of 2)

Group	Signal Name	Description
Byte 5	DDR_DQ[40..47], DDR_DM5, & DDR_DQS5/DQS5#	Data Byte Lane5
Byte 6	DDR_DQ[48..55], DDR_DM6, & DDR_DQS6/DQS6#	Data Byte Lane6
Byte 7	DDR_DQ[56..63], DDR_DM7, & DDR_DQS7/DQS7#	Data Byte Lane7
Byte 8	DDR_ECC[0..7], DDR_DM8, DDR_DQS8/DQS8#	Data Byte Lane 8 (ECC Check Bits)
Control		
Control (CTRL)	DDR_CKE[1:0]	Clock Enables
	DDR_CS#[1:0]	Chip Selects - One chip select per rank
	DDR_ODT[1:0]	On-Die-Termination
Address & Command		
Address / Command (ADDR/CMD)	DDR_MA[14:0]	Memory Address
	DDR_BA[2:0]	Bank Address (Bank Select)
	DDR_RAS#	Row Address Select
	DDR_CAS#	Column Address Select
	DDR_WE#	Write Enable (Output)
Clocks		
Clocks	DDR_CLK[5:0]/ DDR_CLK#[5:0]	Differential Clocks – Three pairs per rank
DC Bias		
DC Bias (I/O)	DDR_CRES[2:0]	• DDR_CRES[2:1] - Impedance compensation resistors. • DDR_CRES[0] - Common return for DDR2 interface compensation resistors on DDV_CRES, DDR_SLWCRES and DDR_RCOMPX
	DDR_SLWCRES	Slew rate compensation for DDR2 interface (Analog)
	DDR_RCOMPX	Impedance compensation for DDR2 interface
	DDV_CRES	DDR2 resistor
	DDR_VREF	Voltage Reference (Analog)

B.5 Supported Memory Configurations

The EP80579 Memory Controller supports up to 4 GB of 400/533/667/800 MT/s memory in a one-rank (2 GB) or two-rank (4 GB) configuration. However, since 9 (8 Data +1 ECC) x8 devices are required for each rank, only single rank designs are reasonably feasible in the memory down implementations. These guidelines support only one rank memory configurations as listed in Table B-25.

Table B-25. Memory Configurations Supported by the EP80579

Config No.	Topology	Ranks	Memory Down (x8) Device Placement	Memory Device Width	Figures
1	Memory Down on PCB (1 chip select)	One	8 on Top **or** 8 on Bottom	8	
2	Memory Down on PCB (1 chip select)	One	4 on Top **and** 4 on Bottom	8	

B.6 Overview and Design Considerations

There are two length constraints placed on each signal group within the DDR2 interface:

- Absolute length: These constraints define the length range over which the signals will meet signal integrity rules.
- Clock and strobe length matching: These constraints ensure that clock-relative AC timing margins are met.

Intel recommends following a preliminary test route to establish the natural bounds on all signal groups. This route defines the target lengths for each signal group, and provides an acceptable solution space when the length matching formulas are applied. Use the EP80579 *Memory Down Trace Length Calculator (TLC)* to ensure that the length and matching requirements are properly met.

B.6.1 Length Matching and Length Formulas

The routing guidelines provided in the following subsections define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal signal integrity and timing. In addition to the absolute length limits provided in the individual guideline tables, more restrictive length matching formulas are also provided that further restrict the minimum and maximum length range of each signal group with respect to clock, within the overall boundaries defined in the guidelines tables, as required to guarantee timing margins. These secondary constraints are referred to as length matching constraints and the formulas used are referred to as length matching formulas.

All signal groups are length matched to the DDR2 clocks, with the clocks themselves length tuned to a fixed length across the Memory Down devices. The amount of minimum to maximum length variance allowed for each signal group around the clock reference length varies from signal group to signal group depending on the amount of timing variance that can be tolerated. A simplified summary of the length matching formulas from the EP80579 to the Memory Down devices for each signal group is provided in Table B-26.

Table B-26. Length Matching Formulas for Memory Down Configuration

Source to Destination	Signal Group	Minimum Length	Maximum Length
EP80579 to Memory Down Pin	ADDR/CMD/CTRL to Clock	Clock - 0 mils	Clock + 30 mils
	Strobe to Clock	Clock - 500 mils	Clock + 500 mils
	Data to Strobe	Strobe - 20 mils	Strobe + 20 mils

Note: All length matching formulas are based on the EP80579 die-pad to Memory Down pin total length.

Package length tables are provided for all signals to facilitate the pad to pin matching. Length formulas should be applied to Memory Down independently. The full geometry and routing guidelines along with the exact length matching formulas and associated diagrams are provided in the individual signal group guidelines sections.

DDR2 System Memory Topologies for Memory Down configurations for all signal groups have a relatively high via usage. This must be considered for the board layout as the vias and the anti-pads for the vias may restrict power delivery to the memory.

B.6.2 Optimizing Memory Signal Integrity

For all configurations in Table B-25, the following recommendations should be followed:

- Branch topologies benefit when the length of each branch is as short as possible and equal to other branches.

- All branch segments should be on the same layer. For example, if there are four L2 segments, then all L2 segments should be the same length and on the same layer.

- If surface mount components are needed (such as a series resistor) for stripline traces, the signal should return to the same internal layer after completing the short external layer route.

  — Transition layer segment length should be minimized.

- For optimal signal integrity and adequate timing margins, have a continuous reference return plane, preferably ground, above and below the routing layer.

- Exceptions to the trace width and spacing geometries are allowed in the break-out region in order to fan out the interconnect pattern. Reduced spacing should be avoided as much as possible.

B.6.2.1 Stack-Up and Layer Utilization

These guidelines are targeted for platforms that use the stack-up dimensions used by the Development Board.

While other stack-ups and layer utilization schemes are possible, ensure that the impedance, velocity, and coupling assumptions used in verifying the signal integrity and timing of the interface are not compromised.

- The data and data strobe signals should be routed completely on one external layer, except as required to break out of the EP80579 package.

- When multiple external layers are used, individual byte lanes should be routed as a group on the same layer.
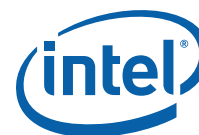
B.6.2.2 Return Path Continuity for Memory Down Topologies

The DDR2 control signals are ground-referenced on the SDRAM devices. This implies that the majority of return current will be flowing through the GND pins on the SDRAM pin and will need to have a contiguous return path back to EP80579. If a power plane is referenced instead, ensure that a minimum of four AC stitching capacitors are used near the SDRAM devices' control pins.

B.6.3 Topologies and Routing Guidelines

B.6.3.1 DDR2 Clock Group Signals - DDR_CLK[2:0]/DDR_CLK[2:0]#

The EP80579 clock signal group includes three differential clock pairs per rank. The following guidelines assume a one-rank design topology. The EP80579 generates and drives these differential clock signals. Each clock pair is routed to three memory devices. Table B-27 summarizes the clock to memory mapping, Figure B-9 shows the

clock interconnect between the EP80579 and the memory devices. Table B-27 provides the clock distribution among the memory devices, and Table B-28 provides the clock routing guidelines.

Table B-27. Clock to Memory Device Mapping

Signal	Connection To
CLK[0], CLK[0]#	SDRAM[2:0]
CLK[1], CLK[1]#	SDRAM[5:3]
CLK[2], CLK[2]#	SDRAM[7:6] + ECC_SDRAM

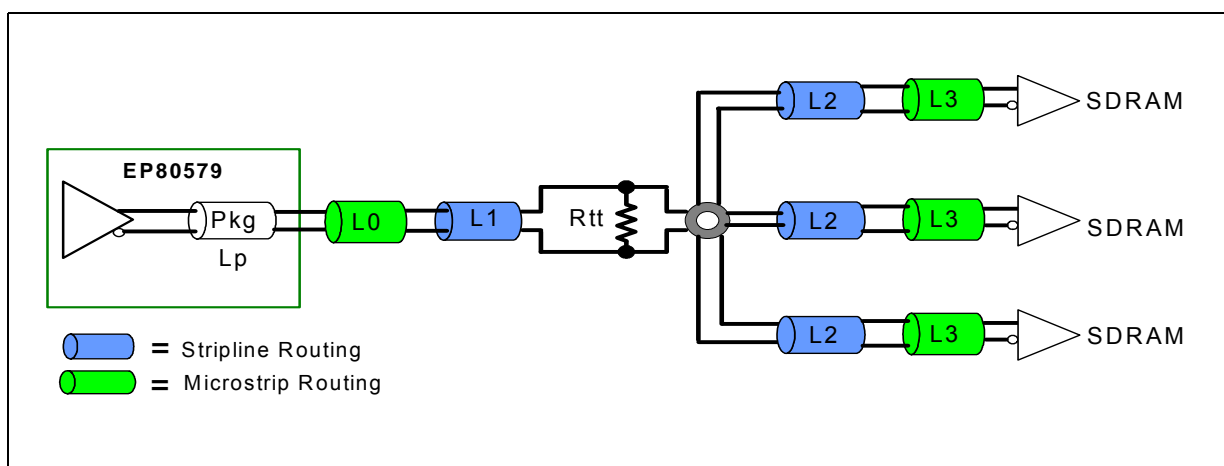**Figure B-9. DDR2 Clock Signal Routing Topology (One Clock for Three Devices)**

Table B-28. Clock Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines	Figure
Signal Group	CLK[2:0]/CLK[2:0]#	
Reference Plane	Ground Referenced	
Layer Assignment	All clock signals must be routed on the same layer	
Characteristic Trace Impedance (Zo)	Single Ended Impedance: 45Ω ±10%	
Nominal Trace Width	See Stackup	
Inter-pair Trace Spacing(e2e) (CLK to CLK# spacing)	6.0 mils	
Pair-to-Pair Spacing (e2e)	15.0 mils	
Clearance from other signals groups	20.0 mils	
Board Routing Guidelines		
Total Trace Length (TTL) = (Lp + L0 + L1 + L2 + L3)	Total Trace Length = 2.0 in - 5.0 in	
Lp	Package Length: See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information.	
L0	Microstrip Break-out • Trace Length = 0.5 in (max)	

Table B-28. Clock Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guidelines	Figure
L1	Stripline Board Route • Trace Length = 1.5 in (min) - 4.0 in (max)	
L2	Stripline Board Route • Trace Length = 0.8 in (max)	
L3	Microstrip Board Route • Trace Length = 0.5 in (max)	
Resistor Coupling		
Rtt	120 Ω ±1%	
Routing Length Matching Rules		
CLK-to-CLK# Length Matching	Match clock pairs to within 10 mils	
Pair-to-Pair Length Matching	Clock pairs should be matched in length to other clock pairs within 20 mils of each other	
Clock-to-DQS Length Matching	Match total length of DQS to clocks to within ±500 mils • DQS/DQS# minimum Length = Clock - 500 mils DQS/DQS# maximum Length = Clock + 500 mils	
Clock-to-ADDR/CMD/CTRL	Match total length of ADD/CMD/CTRL to Clocks to within 20 mils • ADD/CMD/CTRL minimum Length = Clock - 0 mils ADD/CMD/CTRL maximum Length = Clock + 20 mils	

B.6.4 DDR2 Data Group Signals — DQ/DM/ECC/DQS/DQS#

The DDR2 Data Group consists of the following signals:

- Data - DQ[63:0]
- ECC - ECC[7:0]
- Data Mask - DM[8:0]
- Data Strobe - DQS/DQS#[8:0]

The Data/DM and Strobe topologies shown in Figure B-10 and Figure B-11 are the same for each Data Byte Lane (see Table B-24). All signals in the same data byte lane should be routed on the same layer. The Data Strobe (DQS/DQS#) signals must be routed as differential pairs with inter-pair skew of ± 6 mils. This topology assumes that ODT is enabled for both the controller and SDRAM during write operations. Set Controller ODT = 120 ohms, and SDRAM ODT = 150 ohms.
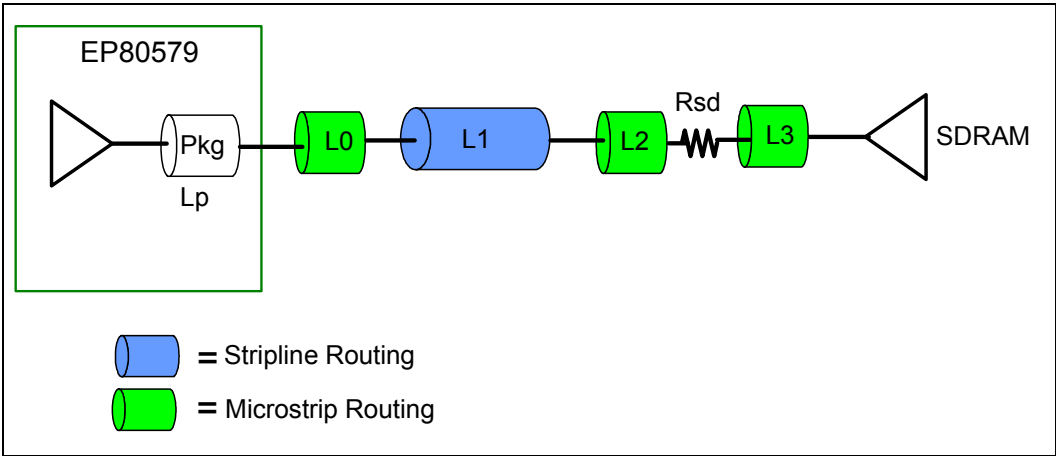
Figure B-10. DDR2 Data/DM/ECC Byte Lane Topology

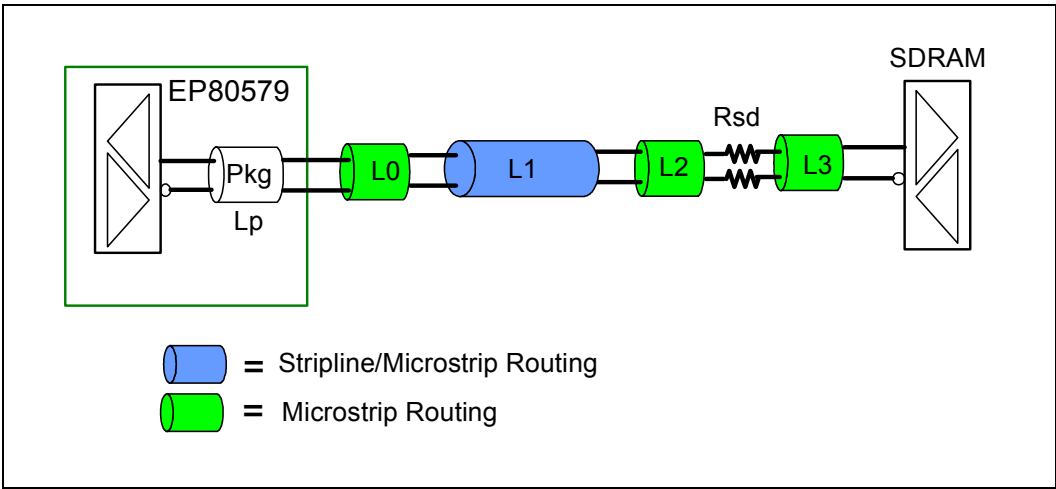**Figure B-11. DDR2 Data Strobe Routing (DQS/DQS#) Topology (One Strobe per Byte Lane)**

Table B-29. Data and Strobe Signal Group Routing Guidelines (Sheet 1 of 2)

Parameter	Routing Guidelines		Figure
	Data Byte Lane		
	Data & Data Mask	**Strobe**	
Signal Group	Data & Mask (DQ & DM)	Byte Strobe (DQS/DQS#)	
Reference Plane	Ground Referenced		
Characteristic Trace Impedance (Zo)	Single Ended Impedance • 50Ω ±10% for L1/L10 (Microstrip routing (e2e)) • 45Ω ±10% for L3/L5/L6/L8 (Stripline routing (e2e))		
Layer assignment	• Signals within the same Byte Lane must be routed on the same layer		
Nominal Trace Width	See Stackup		

Table B-29. Data and Strobe Signal Group Routing Guidelines (Sheet 2 of 2)

Parameter	Routing Guidelines		Figure
	Data Byte Lane		
	Data & Data Mask	**Strobe**	
Trace-to-Trace spacing (e2e)	15 mils (min)	• Inter-pair Spacing:-- DQS/DQS# = 6 mils (min) • Pair-to-Pair Spacing: 15 mils (min)	
Clearance from other signals	20.0 mils (min)		
Board Routing Guidelines			
Total Trace Length (TTL) = (Lp + L0 + L1 + L2 + L3)	Total Trace Length = 2.0 in - 6.0 in		
Lp	Package Length: • See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information.		
L0	Microstrip Break-out: • Trace Length = 0.5 in (max)		
L1	Board Route (Microstrip or Stripline) • Trace Length = 1.5 in (min) - 4.0 in (max)		
L2	Microstrip Board Route: • Trace Length = 0.3 in(max) if L1 is Stripline routed on L3/L5/L6/L8		
L3	Microstrip Break-in • Trace Length = 0.5 in (max)		
Break-out/Break-in Trace Width	4.0 mils		
Break-out/Break-in Trace-to-Trace Spacing	4.0 mils		
Series Termination			
Series Resistor (Rsd)	22Ω ±1%		
Routing Length Matching Rules			
DQS-to-DQS# Inter-pair Length Matching		• Match total length of DQS to DQS# to within ±10 mils • DQS = DQS# ±10 mils	
DQ/DM Data Byte Lane Length Matching	Match total Length of data byte lane signals (DQ/DM) to within 20 mils • Max(DQ/DM) - Min(DQ/DM) </= 20 mils		
DQS-to-DQ/DM Length Matching	Match total length of DQ/DM to DQS to within ±20 mils • DQ/DM minimum Length = DQS - 20 mils • DQ/DM maximum Length = DQS + 20 mils		
DQS-to-Clock Length Matching	Match total length of DQS to clocks to within ±500 mils • DQS/DQS# minimum Length = Clock - 500 mils • DQS/DQS# maximum Length = Clock + 500 mils		
ODT Settings			
Enable ODT	• Controller ODT = 120Ω • SDRAM ODT = 150Ω		

B.6.5 Address, Command and Control Signals

The address, command and control signals shown in Table B-30 are source-clocked signals.

Table B-30. Address and Command Signals

Signal Description	Signal Name
System Memory Address Signals	DDR_MA[14:0]
Bank Addresses	DDR_BA[2:0]
Row Address Select	DDR_RAS#
Column Address Select	DDR_CAS#
Write Enable	DDR_WE#
Chip Select	DDR_CS[0]#
Clock Enable	DDR_CKE[0]
On-Die-Termination (ODT)	DDR_ODT[0]

The address, command and control signals are source-clocked signals. The signals are "clocked" into the SDRAM devices using the positive edge of the clock signals. The EP80579 drives the address/command and clock signals together.

Figure B-26, and Table B-31 show the recommended topology and layout routing guidelines for the DDR2-SDRAM address, command and control signals. A maximum of 6 vias should be used for layer changes over the entire route from the EP80579 pin to SDRAM pin.

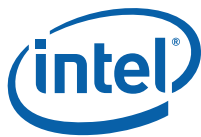**Figure B-12. DDR2 Address, Command and Control Signal Routing Topology**
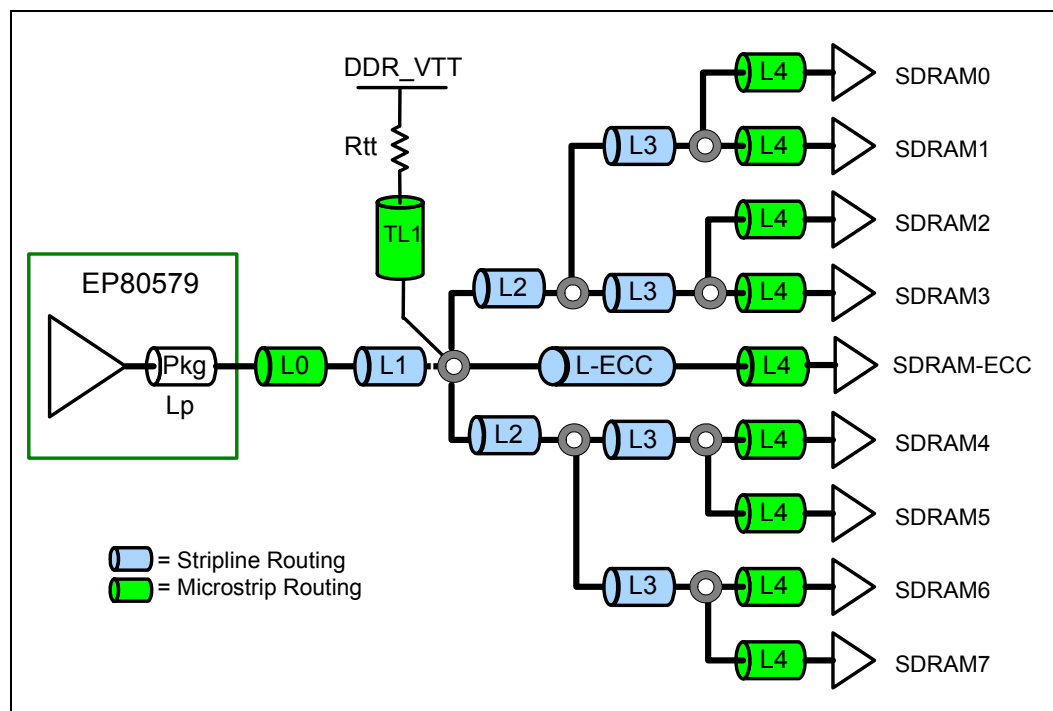
Table B-31. DDR2 Address/Command Signal Group Routing Guidelines

| Parameter	Routing Guidelines	Figure
Signal Group	DDR_MA[14:0], DDR_BA[2:0], DDR_RAS#, DDR_CAS#, DDR_WE#, DDR_CS[0]#, DDR_CKE[0], DDR_ODT[0]	
Reference Plane	Ground Referenced	
Layer Assignment	• Signals must be routed on the same layer	
Characteristic Trace Impedance (Zo)	45 Ω ±10%	
Nominal Trace Width	See Stackup	
Nominal Trace Spacing (e2e)	15 mils	
Clearance from other signals	20 mils (min)	
Board Routing Guidelines		
Total Trace Length (TTL) = (Lp + L0 + L1 + L2 + L3 + L4)	Total Trace Length = 2.0 in - 6.0 in	
Lp	Package Length: • See the *Intel® EP80579 Integrated Processor Product Line Datasheet* for package length information.	
L0	Microstrip Break-out: • Trace Length = 0.5 in (max)	
L1	Stripline Board Route • Trace Length = 1.5 in (min) - 4.0 in (max)	
L2	Stripline Board Route: • Trace Length = 0.8 in(max)	
L3	Stripline Board Route: • Trace Length = 0.8 in(max)	
L4	Microstrip Break-in • Trace Length = 0.5 in (max)	
L-ECC	ECC Stripline Board Route: • Trace Length = L2 + L3	
TL1 (Stub to Rtt)	Microstrip Route • Trace Length = 0.4 in (max)	
On-Board Termination		
Termination Resistor (Rtt)	60 Ω ±1%	Figure B-27
Routing Length Matching Rules		
Inter group signal length matching	Match total length of ADD, CMD, and CTRL signals to within 20 mils of each other.	
(ADD/CMD/CTRL) - to - Clock	Match total length of ADD/CMD/CTRL to Clocks to within 20 mils • ADD/CMD/CTRL minimum Length = Clock - 0 mils • ADD/CMD/CTRL maximum Length = Clock + 20 mils	

B.6.6 DC Bias Signals

The DC bias signals consist of DDR_SLWCRES, DDR_RCOMPX, DDR_CRES[2:0], DDV_CRES, and DDR_VREF. The routing guidelines for these signals are described in Section B.6.6.1 and Section B.6.6.2.

B.6.6.1 DDR_SLWCRES, DDR_RCOMPX, DRV_CRES, & DDR_CRES0

The DDR_SLWCRES, DDR_RCOMPX, DRV_CRES, and DDR_CRES0 signals are compensation resistors for slew rate, impedance, and common return, respectively. Intel recommends 20 mil wide traces with a minimum spacing of 12 mils from other signals. When breaking out from the EP80579, maintain a minimum spacing of 4.5 mils up to a maximum length of 500 mils. For the best signal integrity, minimize this length as much as possible. Figure B-13 shows the routing topology for these signals.

Figure B-13. DDR_SLWCRES, DDR_RCOMPX, DDV_CRES, & DDR_CRES0 Routing Topology
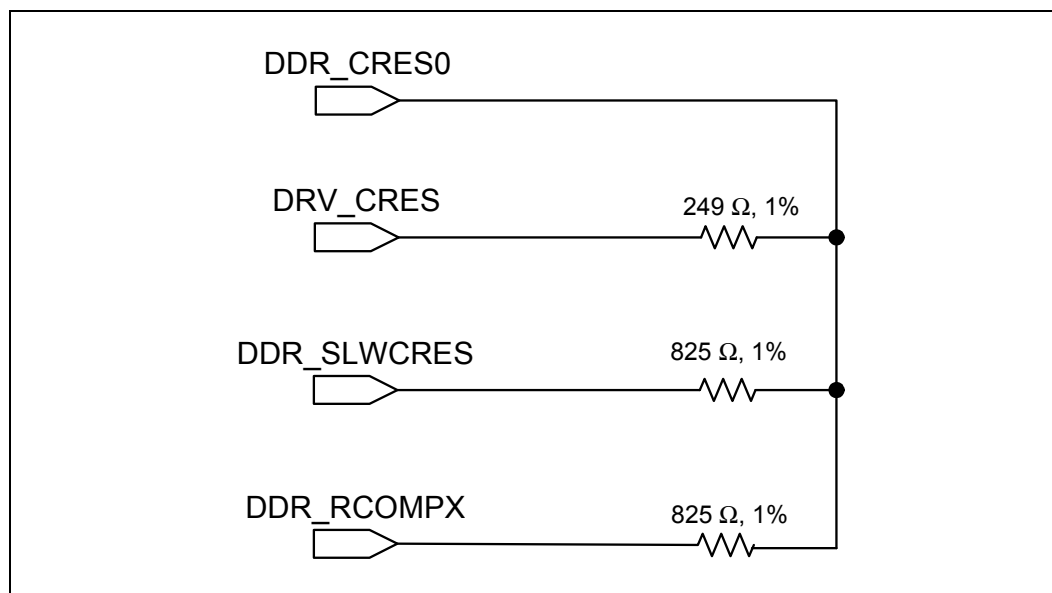
B.6.6.2 DDR_CRES1, DDR_CRES2

The EP80579 provides the DDR_CRES1 and DDR_CRES2 signals as additional compensation resistors (See Figure B-14). Route the signal as microstrip, with a maximum length of 500 mils and minimized DC resistance.
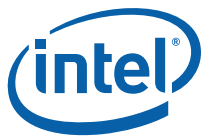
Figure B-14. DDR_CRES1 and DDR_CRES2 Signal Connections