
STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32_Demo
Board Name	NUCLEO-F103RB
Generated with:	STM32CubeMX 6.1.2
Date	03/04/2021

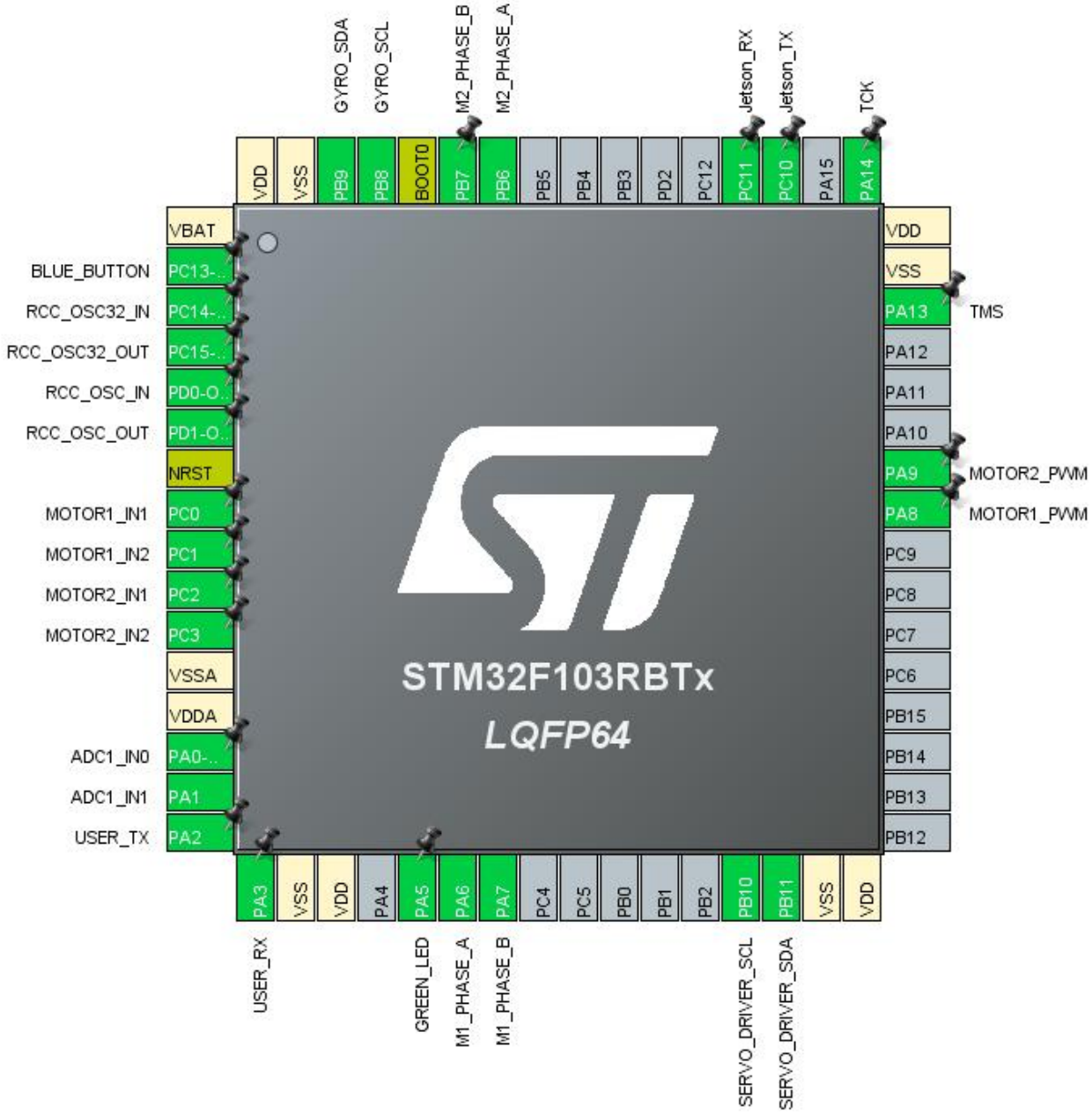
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103RBTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M3

2. Pinout Configuration



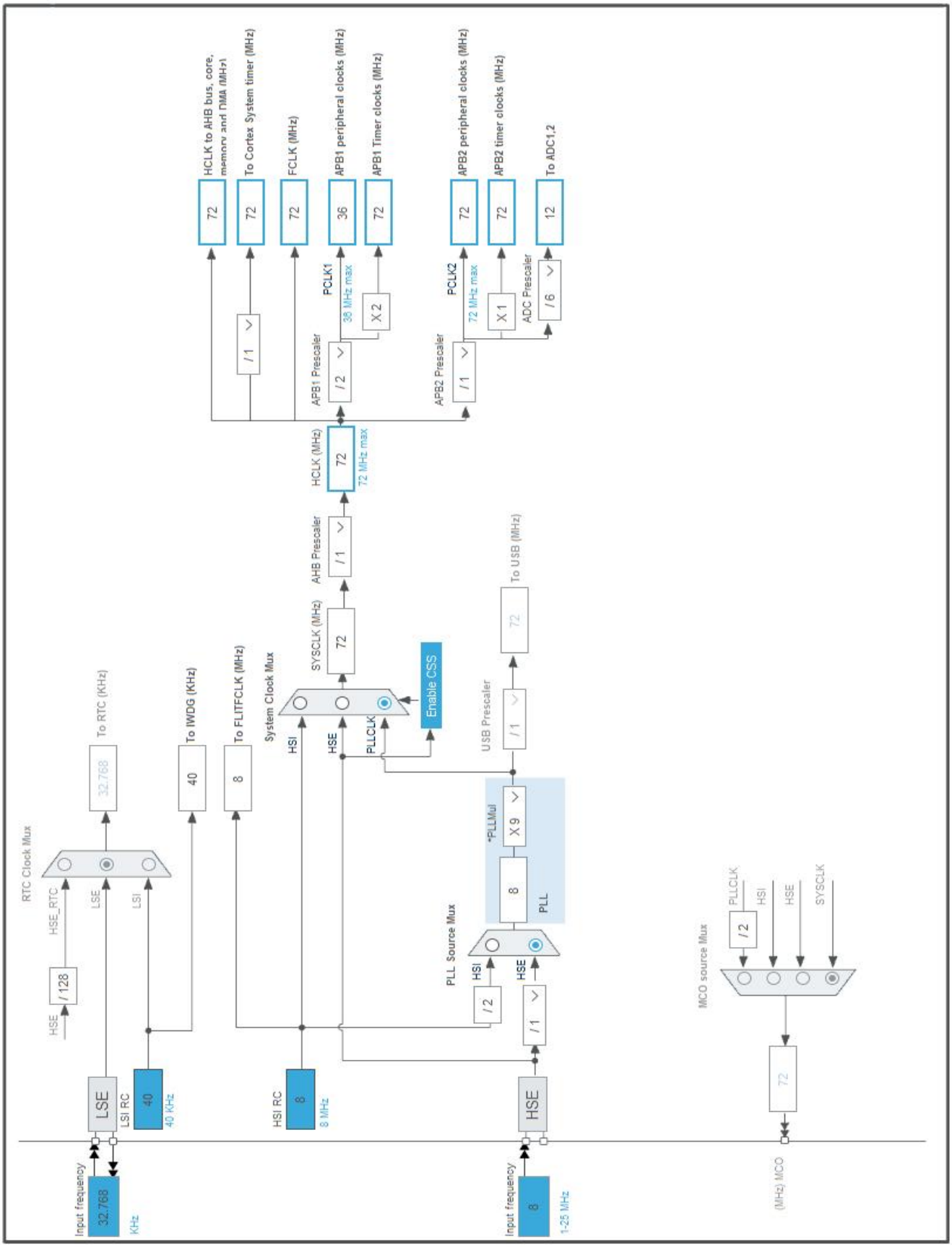
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC	I/O	GPIO_EXTI13	BLUE_BUTTON
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	MOTOR1_IN1
9	PC1 *	I/O	GPIO_Output	MOTOR1_IN2
10	PC2 *	I/O	GPIO_Output	MOTOR2_IN1
11	PC3 *	I/O	GPIO_Output	MOTOR2_IN2
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	
15	PA1	I/O	ADC1_IN1	
16	PA2	I/O	USART2_TX	USER_TX
17	PA3	I/O	USART2_RX	USER_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	GREEN_LED
22	PA6	I/O	TIM3_CH1	M1_PHASE_A
23	PA7	I/O	TIM3_CH2	M1_PHASE_B
29	PB10	I/O	I2C2_SCL	SERVO_DRIVER_SCL
30	PB11	I/O	I2C2_SDA	SERVO_DRIVER_SDA
31	VSS	Power		
32	VDD	Power		
41	PA8	I/O	TIM1_CH1	MOTOR1_PWM
42	PA9	I/O	TIM1_CH2	MOTOR2_PWM
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
51	PC10	I/O	USART3_TX	Jetson_TX
52	PC11	I/O	USART3_RX	Jetson_RX
58	PB6	I/O	TIM4_CH1	M2_PHASE_A
59	PB7	I/O	TIM4_CH2	M2_PHASE_B

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
60	BOOT0	Boot		
61	PB8	I/O	I2C1_SCL	GYRO_SCL
62	PB9	I/O	I2C1_SDA	GYRO_SDA
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32_Demo
Project Folder	C:\Users\VincentChan\Desktop\Humane_Controller
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.3
Application Structure	Basic
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_USART2_UART_Init	USART2
5	MX_I2C2_Init	I2C2
6	MX_TIM2_Init	TIM2
7	MX_TIM3_Init	TIM3
8	MX_TIM4_Init	TIM4
9	MX_USART3_UART_Init	USART3
10	MX_TIM1_Init	TIM1
11	MX_IWDG_Init	IWDG

Rank	Function Name	Peripheral Instance Name
12	MX_ADC1_Init	ADC1
13	MX_I2C1_Init	I2C1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103RBTx
Datasheet	DS5319_Rev17

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

6.4. Sequence

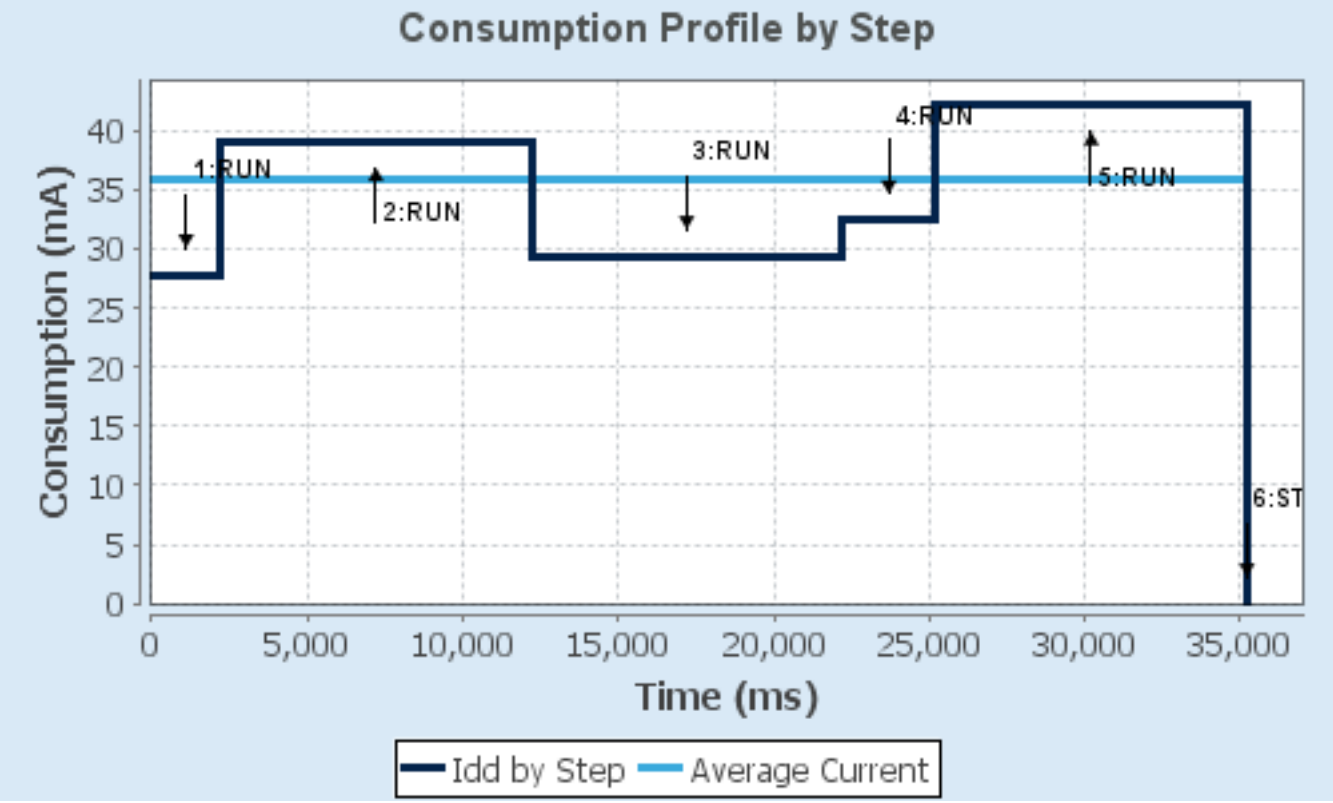
Step	Step1	Step2	Step3	Step4	Step5	Step6
Mode	RUN	RUN	RUN	RUN	RUN	STANDBY
Vdd	3.3	3.3	3.3	3.3	3.3	3.3
Voltage Source	Battery	Battery	Battery	Battery	Battery	Battery
Range	No Scale	No Scale	No Scale	No Scale	No Scale	No Scale
Fetch Type	FLASH	FLASH	FLASH	FLASH	FLASH	n/a
CPU Frequency	72 MHz	72 MHz	72 MHz	72 MHz	72 MHz	0 Hz
Clock Configuration	HSE PLL	HSE PLL	HSE PLL	HSE PLL	HSE PLL	LSI IWDG
Clock Source Frequency	8 MHz	8 MHz	8 MHz	8 MHz	8 MHz	37 kHz
Peripherals	USART2	GPIOA GPIOB GPIOC GPIOD IWDG TIM1 TIM2 TIM3 TIM4 USART2	I2C2 IWDG USART2	ADC1 IWDG TIM4 USART2	ADC1 GPIOA GPIOB GPIOC GPIOD I2C2 IWDG TIM1 TIM2 TIM3 TIM4 USART2 USART3	IWDG*
Additional Cons.	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
Average Current	27.88 mA	39.19 mA	29.44 mA	32.44 mA	42.21 mA	3.4 µA
Duration	2200 ms	10 s	10 s	3 s	10 s	20 ms
DMIPS	61.0	61.0	61.0	61.0	61.0	0.0
Ta Max	100.86	99.18	100.63	100.18	98.73	105
Category	In DS Table	In DS Table	In DS Table	In DS Table	In DS Table	In DS Table

6.5. Results

Sequence Time	35.22 s	Average Current	35.98 mA

Battery Life	3 days, 22 hours	Average DMIPS	61.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN0

mode: IN1

7.1.1. Parameter Settings:

ADCs_Common_Settings:	
Mode	Independent mode
ADC_Settings:	
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
ADC_Regular_ConversionMode:	
Enable Regular Conversions	Enable
Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 0
Sampling Time	1.5 Cycles
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	1.5 Cycles
ADC_Injected_ConversionMode:	
Enable Injected Conversions	Disable
WatchDog:	
Enable Analog WatchDog Mode	false

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Master Features:	
I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000
Slave Features:	
Clock No Stretch Mode	Disabled

Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.3. I2C2

I2C: I2C

7.3.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.4. IWDG

mode: Activated

7.4.1. Parameter Settings:

Clocking:

IWDG counter clock prescaler	**32 ***
IWDG down-counter reload value	4095

7.5. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled

Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.6. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.7. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**20 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**3600 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.8. TIM2

Clock Source : Internal Clock

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1024 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**709 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.9. TIM3

Combined Channels: Encoder Mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**10 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**10 ***

7.10. TIM4

Combined Channels: Encoder Mode

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.11. USART2

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.12. USART3

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	
	PA1	ADC1_IN1	Analog mode	n/a	n/a	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	n/a	**High ***	GYRO_SCL
	PB9	I2C1_SDA	Alternate Function Open Drain	n/a	**High ***	GYRO_SDA
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	n/a	**High ***	SERVO_DRIVER_SCL
	PB11	I2C2_SDA	Alternate Function Open Drain	n/a	**High ***	SERVO_DRIVER_SDA
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	MOTOR1_PWM
	PA9	TIM1_CH2	Alternate Function Push Pull	n/a	Low	MOTOR2_PWM
TIM3	PA6	TIM3_CH1	Input mode	No pull-up and no pull-down	n/a	M1_PHASE_A
	PA7	TIM3_CH2	Input mode	No pull-up and no pull-down	n/a	M1_PHASE_B
TIM4	PB6	TIM4_CH1	Input mode	No pull-up and no pull-down	n/a	M2_PHASE_A
	PB7	TIM4_CH2	Input mode	No pull-up and no pull-down	n/a	M2_PHASE_B
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	Low	USER_TX
	PA3	USART2_RX	*	No pull-up and no pull-down	n/a	USER_RX
USART3	PC10	USART3_TX	Alternate Function Push Pull	n/a	**High ***	Jetson_TX
	PC11	USART3_RX	Input mode	No pull-up and no pull-down	**n/a**	Jetson_RX
GPIO	PC13-TAMPER-RTC	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	BLUE_BUTTON
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR1_IN1
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR1_IN2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR2_IN1
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR2_IN2
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GREEN_LED

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
USART3_RX	DMA1_Channel3	Peripheral To Memory	**Very High ***

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

USART3_RX: DMA1_Channel3 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
TIM2 global interrupt	true	0	0
USART3 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART2 global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false

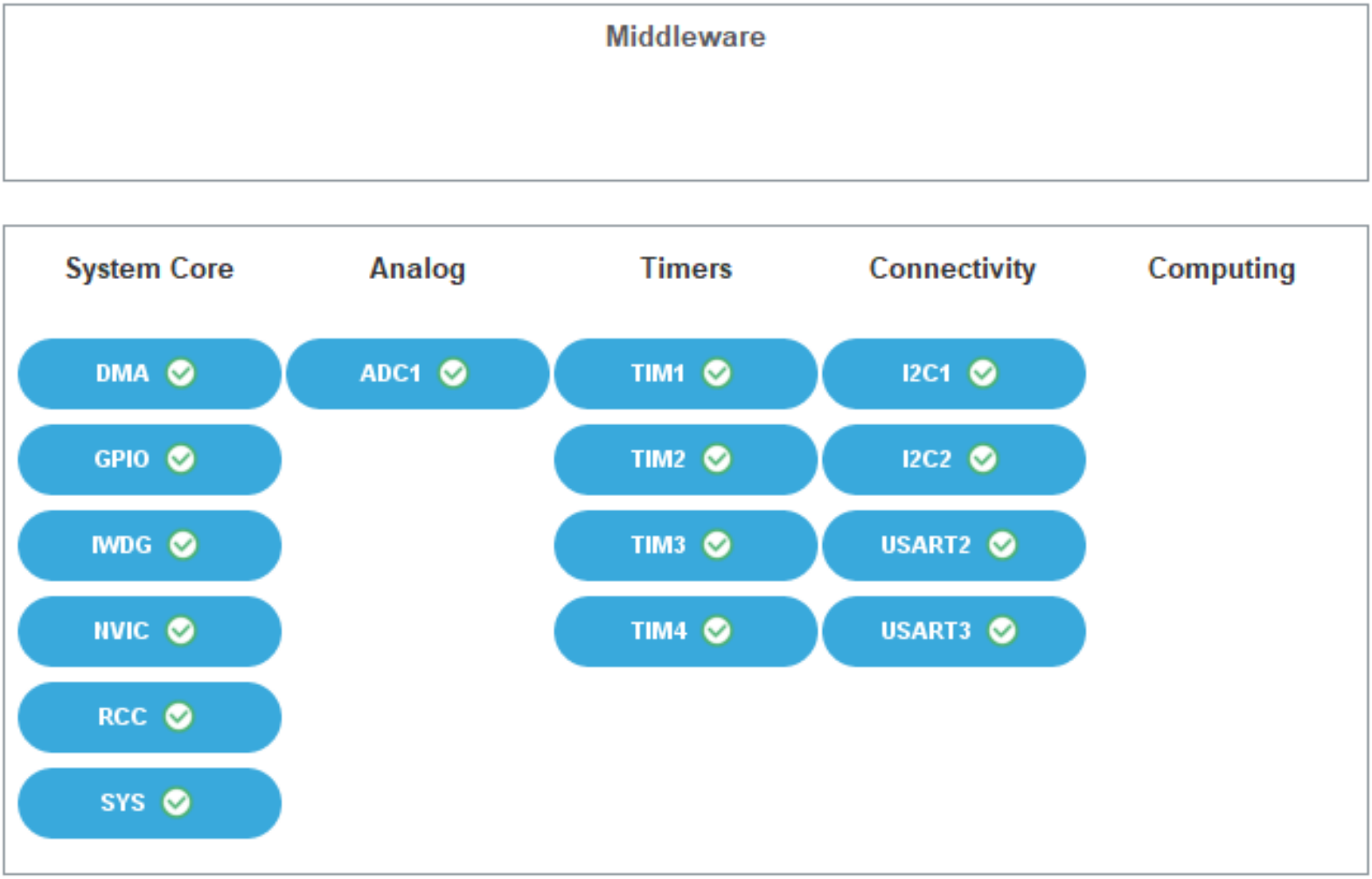
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel3 global interrupt	false	true	true
TIM2 global interrupt	false	true	true
USART3 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/CD00161566.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/CD00171190.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/CD00228163.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/CD00283419.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/CD00190234.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00156964.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00325582.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf