Christopher Torng

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Research Interests

I am interested in all aspects of computer architecture, especially specialized systems that are co-designed across software, architecture, and VLSI to unify emerging applications with emerging technologies. In the future, I hope to engage experts across software (e.g., AR, VR, intelligence on the edge, smart healthcare) and technology (e.g., TFETs, emerging memories, energy harvesting) to continue a track of cross-stack research.

Education

- **Cornell University**, Ithaca, NY 2012 – Present
  Ph.D. Candidate in Electrical and Computer Engineering
  Advisor: Professor Christopher Batten, Expected Graduation: Spring 2019
  Tentative Thesis: Software, Architecture, and VLSI/Circuit Co-Design for Task-Based Parallel Runtimes
- **Cornell University**, Ithaca, NY 2008 – 2012
  B.S. - Electrical Engineering and Computer Science

Awards and Honors

- Rising Stars in Computer Architecture (RISC-A) 2018
- IEEE Micro Top Pick from Hot Chips (for Hot Chips '17 paper) 2018
- NSF GRFP Honorable Mention 2014
- Finalist for Qualcomm Innovation Fellowship (QInF) 2013
- H.C. Torng Fellowship – Cornell one-semester graduate fellowship (no familial relation) 2012

Research Experience

- **Software, Architecture, and VLSI Co-Design for Task-Based Parallel Runtimes** 2016 – Present
  Computer Systems Laboratory, Cornell University, Ithaca, NY
  Advisor: Professor Christopher Batten
- **Methodologies for Rapid ASIC Design** 2016 – Present
  Computer Systems Laboratory, Cornell University, Ithaca, NY
  Advisors/Mentors: Professor Christopher Batten (Cornell University)
  Advisors/Mentors: Professor Michael B. Taylor (University of Washington)
  Advisors/Mentors: Professor Ronald G. Dreslinski (University of Michigan)
  Advisors/Mentors: Brucek Khailany (NVIDIA Research)
- **Architecture and Circuit Co-Design for Integrated Voltage Regulation** 2012 – Present
  Computer Systems Laboratory, Cornell University, Ithaca, NY
  Advisors/Mentors: Professor Christopher Batten
  Advisors/Mentors: Professor Alyssa B. Apsel

Teaching Experience

- **Cornell ECE 2400 – Computer Systems Programming** 2017
  Lead Graduate Teaching Assistant
- **Cornell ECE 4750 – Computer Architecture** 2014
  Lead Graduate Teaching Assistant
- **Cornell CURIE Academy** 2014
  Lead Graduate Teaching Assistant
- **Cornell ENGRG 1060 – Explorations in Engineering** 2013
  Graduate Teaching Assistant
- **Cornell ECE 4750 – Computer Architecture** 2011
  Undergraduate Teaching Assistant

Industry Experience

- **NVIDIA ASIC/VLSI Research Group**, Austin, TX — 2017
  Graduate Research Intern
- **Intel Many Integrated Core**, Hillsboro, OR — 2012
  Graduate Design and Validation Intern
- **Intel Many Integrated Core**, Hillsboro, OR — 2011
  Undergraduate Validation Intern

Test Chips and Prototyping

See my research website for photos and details: `http://www.csl.cornell.edu/~ctorng`


Batten Research Group Test Chip 2 (BRGTC2) — 2018
Task-Based Parallel Runtimes


Pulse-Coupled Oscillator Synchronizer (PCOSYNC) — 2018
Baseband Synchronizers for Internet of Things


The Celerity RISC-V Tiered Accelerator Fabric (Celerity) — 2017
Methodologies for Rapid ASIC Design


Batten Research Group Test Chip 1 (BRGTC1) — 2016
Python-Based Hardware Modeling


Dynamic Capacitance Sharing (DCS) — 2014
Integrated Voltage Regulation

Media Coverage

- EETimes: 16 Views of Hot Chips '17, ASIC done in nine months for $1.3M
  - `https://www.eetimes.com/document.asp?doc_id=1332192&page_number=10`

Journal Publications

Top-tier architecture journals in this list	**IEEE MICRO**
Top-tier circuits journals in this list	**IEEE TCAS I**

- Scott Davidson, Shaolin Xie, **Christopher Torng**, Khalid Al-Hawaj, Austin Rovinski, Tutu Ajayi, Luis Vega, Chun Zhao, Ritchie Zhao, Steve Dai, Aporva Amarnath, Bandhav Veluri, Paul Gao, Anuj Rao, Gai Liu, Rajesh K. Gupta, Zhiru Zhang, Ronald G. Dreslinski, Christopher Batten, and Michael B. Taylor. "The Celerity Open-Source 511-Core RISC-V Tiered Accelerator Fabric: Fast Architectures and Design Methodologies for Fast Chips". *IEEE Micro Volume 38(2):30–41, Mar/Apr. 2018 (**IEEE MICRO**)*. Special issue for top picks from Hot Chips 29.
- Ivan Bukreyev, **Christopher Torng**, Waclaw Godycki, Christopher Batten, and Alyssa Apsel. "Four Monolithically Integrated Switched-Capacitor DC-DC Converters with Dynamic Capacitance Sharing in 65-nm CMOS". *IEEE Transactions on Circuits and Systems I* (**IEEE TCAS I**), PP(99):1-13. November 2017.

Conference Publications

Top-tier architecture conferences in this list	**ISCA**, **MICRO**
Top-tier chip / design automation conferences in this list	**DAC**, **HotChips**

- Shunning Jiang, **Christopher Torng**, and Christopher Batten . "An Open-Source Python-Based Hardware Generation, Simulation, and Verification Framework". First Workshop on Open-Source EDA Technology held in conjunction with ICCAD-37 (**WOSET**). San Diego, CA. November 2018.

- **Christopher Torng**, Shunning Jiang, Khalid Al-Hawaj, Ivan Bukreyev, Berkin Ilbeyi, Tuan Ta, Lin Cheng, Julian Puscar, Ian Galton, and Christopher Batten. "A New Era of Silicon Prototyping in Computer Architecture Research". *RISC-V Day Workshop held in conjunction with MICRO-51* (**RISC-V Day**). Fukuoka, Japan. October 2018.
- Brucek Khailany, Evgeni Krimer, Rangharajan Venkatesan, Jason Clemons, Joel Emer, Matthew Fojtik, Alicia Klinefelter, Michael Pellauer, Nathaniel Pinckney, Yakun Sophia Shao, Shreesha Srinath, **Christopher Torng**, Sam (Likun) Xi, Yanqing Zhang, Brian Zimmer. "A Modular Digital VLSI Flow for High-Productivity SoC Design". *55th ACM/IEEE Design Automation Conference* (**DAC**). San Francisco, CA. June 2018.
- Ji Kim, Shunning Jiang, **Christopher Torng**, Moyang Wang, Shreesha Srinath, Berkin Ilbeyi, Khalid Al-Hawaj, Christopher Batten. "Using Intra-Core Loop-Task Accelerators to Improve the Productivity and Performance of Task-Based Parallel Programs". *50th IEEE/ACM Int'l Symposium on Microarchitecture* (**MICRO**). Boston, MA. October 2017.
- Tutu Ajayi, Khalid Al-Hawaj, Aporva Amarnath, Steve Dai, Scott Davidson, Paul Gao, Gai Liu, Anuj Rao, Austin Rovinski, Ningxiao Sun, **Christopher Torng**, Luis Vega, Bandhav Veluri, Shaolin Xie, Chun Zhao, Ritchie Zhao, Christopher Batten, Ronald G. Dreslinski, Rajesh K. Gupta, Michael B. Taylor, Zhiru Zhang. "Experiences Using the RISC-V Ecosystem to Design an Accelerator-Centric SoC in TSMC 16nm". *First Workshop on Computer Architecture Research with RISC-V* (**CARRV**). Boston, MA. October 2017.
- Tutu Ajayi, Khalid Al-Hawaj, Aporva Amarnath, Steve Dai, Scott Davidson, Paul Gao, Gai Liu, Atieh Lotfi, Julian Puscar, Anuj Rao, Austin Rovinski, Loai Salem, Ningxiao Sun, **Christopher Torng**, Luis Vega, Bandhav Veluri, Xiaoyang Wang, Shaolin Xie, Chun Zhao, Ritchie Zhao, Christopher Batten, Ronald G. Dreslinski, Ian Galton, Rajesh K. Gupta, Patrick P. Mercier, Mani Srivastava, Michael B. Taylor, Zhiru Zhang. "Celerity: An Open Source RISC-V Tiered Accelerator Fabric". *29th Symposium on High Performance Chips* (**HotChips**). Cupertino, CA. August 2017.
- **Christopher Torng**, Moyang Wang, Bharath Sudheendra, Nagaraj Murali, Suren Jayasuriya, Shreesha Srinath, Taylor Pritchard, Robin Ying, and Christopher Batten. "Experiences Using A Novel Python-Based Hardware Modeling Framework For Computer Architecture Test Chips". *Poster at the 28th Symposium on High Performance Chips* (**HotChips Poster**). Cupertino, CA. August 2016.
- **Christopher Torng**, Moyang Wang, and Christopher Batten. "Asymmetry-Aware Work-Stealing Runtimes". *43rd ACM/IEEE Int'l Symp. on Computer Architecture* (**ISCA**). Seoul, Korea. June 2016.
- Waclaw Godycki*, **Christopher Torng***, Ivan Bukreyev, Alyssa Apsel, and Christopher Batten. "Enabling Realistic Fine-Grain Voltage Scaling with Reconfigurable Power Distribution Networks". *47th IEEE/ACM Int'l Symposium on Microarchitecture* (**MICRO**). Cambridge, UK. December 2014. (* = equally contributing co-first authors)
- Ji Kim, **Christopher Torng**, Shreesha Srinath, Derek Lockhart, and Christopher Batten. "Microarchitectural Mechanisms to Exploit Value Structure in SIMT Architectures". *40th ACM/IEEE Int'l Symposium on Computer Architecture* (**ISCA**). Tel Aviv, Israel. June 2013.

Talks

- "A New Era of Silicon Prototyping in Computer Architecture Research" October 2018
  RISC-V Day Workshop held in conjunction with MICRO-51. Fukuoka, Japan.
- "Software, Architecture, and VLSI Co-Design for Task-Based Parallel Runtimes" October 2018
  Rising Stars in Computer Architecture (RISC-A) Workshop
  Georgia Institute of Technology. Atlanta, GA.
- "Towards Rapid Chip Development with Celerity and BRGTC1" April 2018
  Invited talk at CMU Computer Architecture Lab (CALCM)
  Carnegie Mellon University. Pittsburgh, PA.

- "Experiences Using the RISC-V Ecosystem to Design an Accelerator-Centric SoC in TSMC 16nm" October 2017
  CARRV: First Workshop on Computer Architecture Research with RISC-V. Boston, MA.
- "Celerity: An Open Source RISC-V Tiered Accelerator Fabric" September 2017
  Cornell Electron Devices Society. Ithaca, NY.
- "Asymmetry-Aware Work-Stealing Runtimes" June 2016
  ISCA: 43rd ACM/IEEE Int'l Symp. on Computer Architecture (ISCA-43). Seoul, Korea.
- "Enabling Realistic Fine-Grain Voltage Scaling with Reconfigurable Power Distribution Networks" December 2014
  MICRO: 47th IEEE/ACM Int'l Symposium on Microarchitecture (MICRO-47). Cambridge, UK.
- "On-Chip Reconfigurable Power Distribution Networks" July 2013
  Cornell STEM Graduate Student Summer Colloquium. Ithaca, NY.
- "Reconfigurable Power Distribution Networks for Embedded Multicore Processors" March 2013
  QInF: Qualcomm Innovation Fellowship Finals. Bridgewater, NJ.

Outreach

- **Cornell CURIE Academy** 2014

  Lead Graduate Teaching Assistant

  The CURIE Academy is a one-week summer residential program organized by the Cornell Diversity Programs in Engineering for high school girls who excel in math and science, enjoy solving problems, and want to learn more about careers in engineering.

Professional Activities

- Shadow PC Member for ASPLOS 2018 2018
- Reviewer for IEEE TCAS I 2016

My Open-Source Projects

- The Modular VLSI Build System 2018
  `https://github.com/cornell-brg/alloy-asic`

Miscellaneous

- Music Director for *FantAsia A Cappella* at Cornell 2013 – 2015
- Hobbies: figure skating, singing a cappella, music composition and arrangement, piano

References

- **Christopher Batten (advisor)**
  Associate Professor of Electrical and Computing Engineering, Cornell University
  cbatten@cornell.edu
- **Alyssa B. Apsel**
  Professor of Electrical and Computer Engineering, Cornell University
  aba25@cornell.edu
- **Michael B. Taylor**
  Associate Professor of Electrical Engineering / Computer Science and Engineering, University of Washington
  prof.taylor@gmail.com
- **Ronald G. Dreslinski**
  Assistant Professor of Electrical Engineering and Computer Science, University of Michigan
  rdreslin@umich.edu
- **Brucek Khailany**
  Lead for the NVIDIA ASIC & VLSI Research Group, NVIDIA Research
  bkhailany@nvidia.com