Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry

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Thesis Defense

Computer Systems Laboratory
School of Electrical and Computer Engineering
Cornell University

Emerging Applications Demand Performance

AR / VR

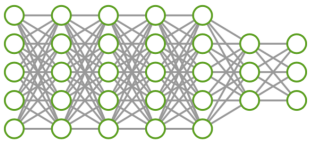
Autonomous Driving

Graph Analytics

Smart Home

Smart Healthcare

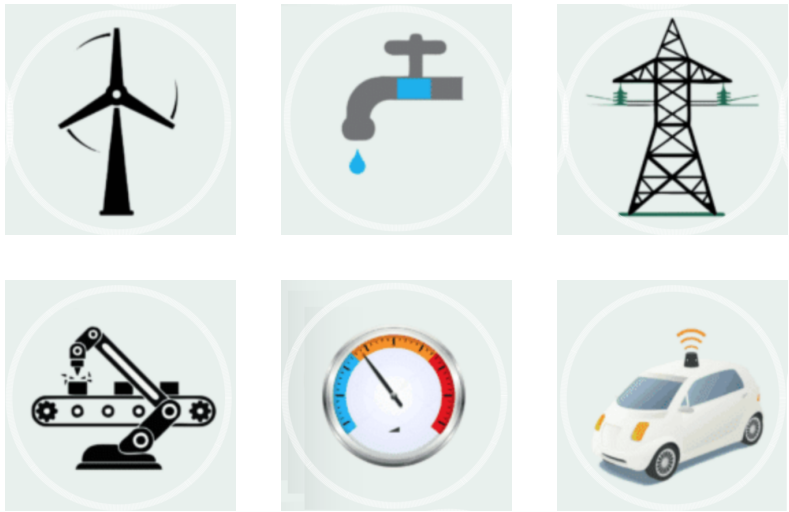
AI



Cybersecurity

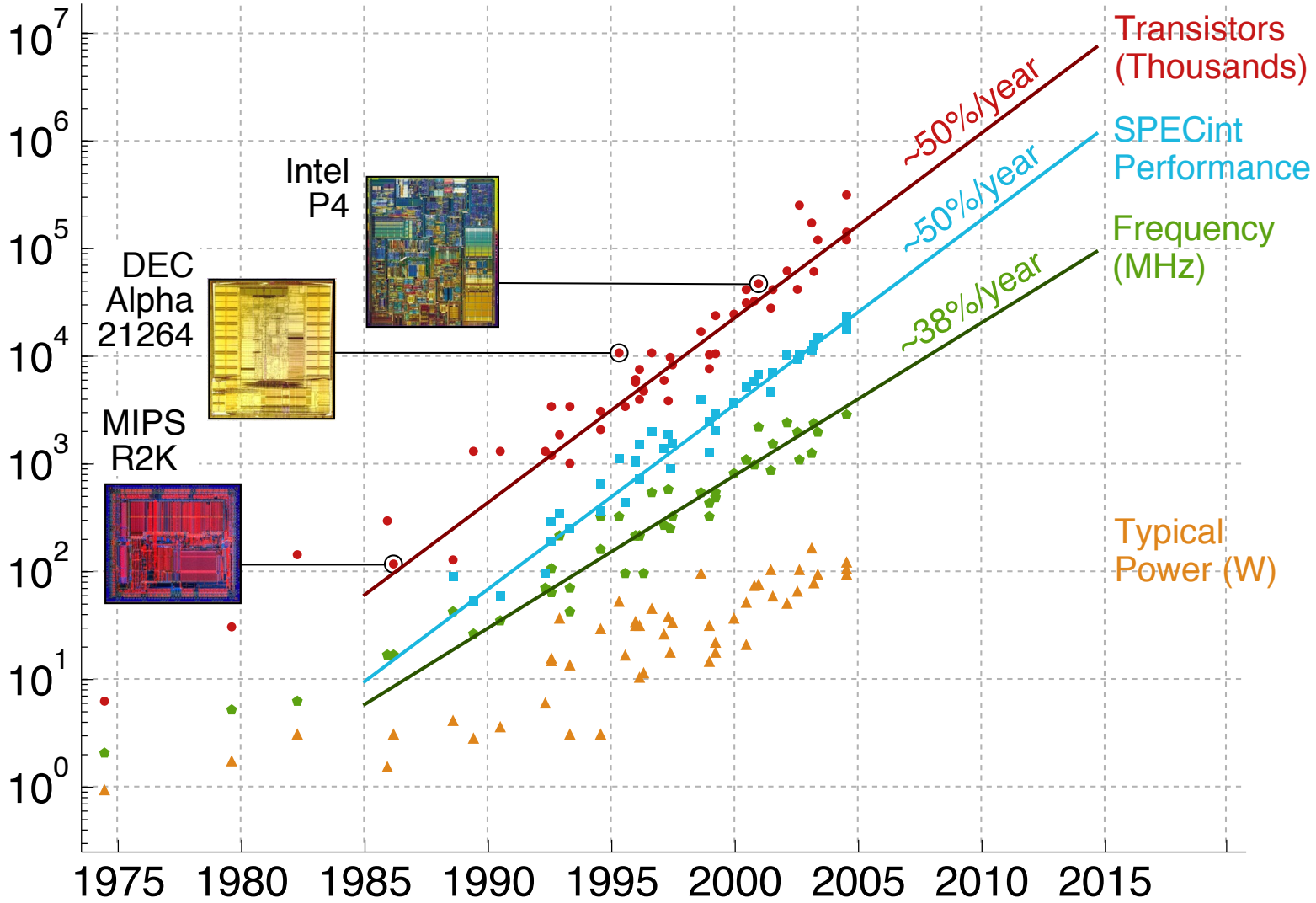
Intelligence on the Edge

Emerging domains have either promised or have already delivered real-world impact



Source: Lanner

The Power Wall



Data collected by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, C. Batten

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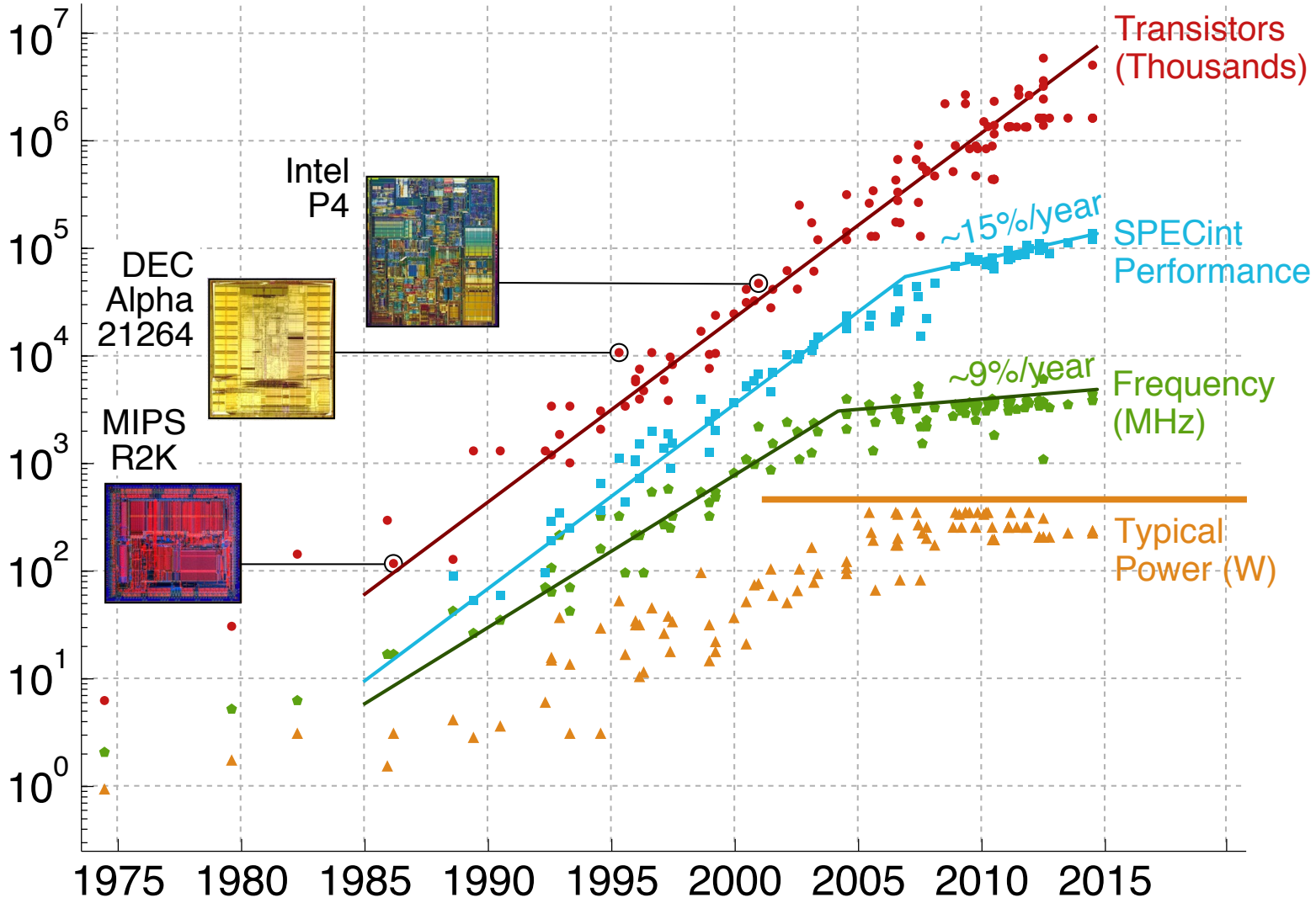

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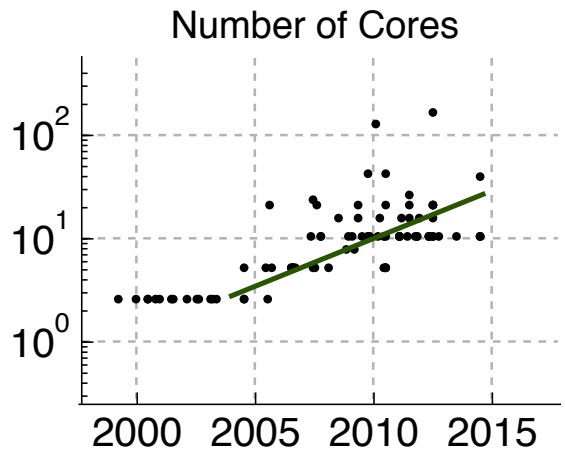
Parallelism and Specialization

Parallelism

Specialization

Parallelism and Specialization

Parallelism



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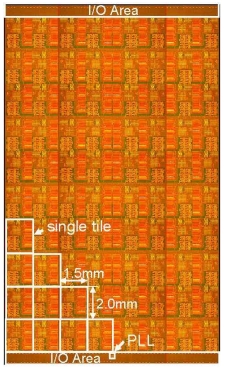
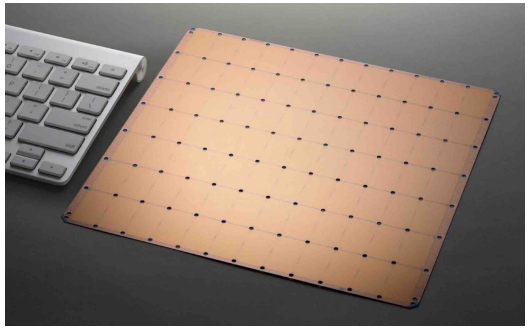


Intel Polaris (2007)
21.7 mm x 12.6 mm
80 cores

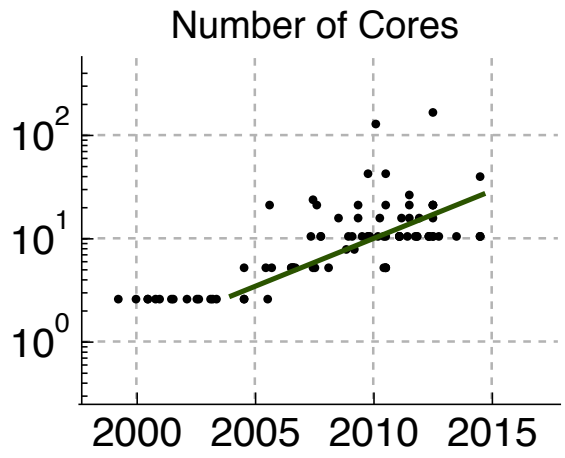


Cerebras Wafer-Scale Engine (2019)
215 mm x 215 mm
400,000 AI-Optimized Cores

Specialization

Parallelism and Specialization

Parallelism



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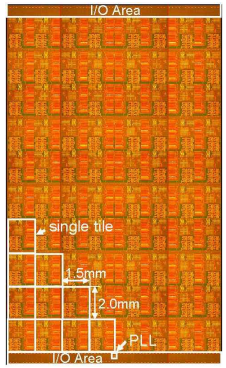

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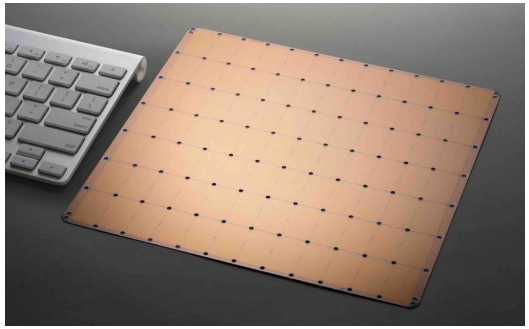


Cerebras Wafer-Scale Engine (2019)
215 mm x 215 mm
400,000 AI-Optimized Cores

Specialization

General Purpose	Lane-Based Accelerators	CGRA-Based Accelerators	Domain-Specific Accelerators	Application-Specific Accelerators
Multicore Manycore	Packed-SIMD Vector Vector-thread	DySER Triggered Instructions	Convolution Engines CNN/DNN Accelerators GPGPU	Crypto / Compression Video encoders Video decoders

Flexible ⟷ Efficient

Parallelism and Specialization

Parallelism

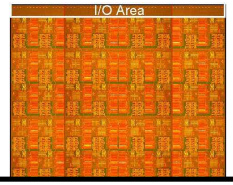
Number of Cores

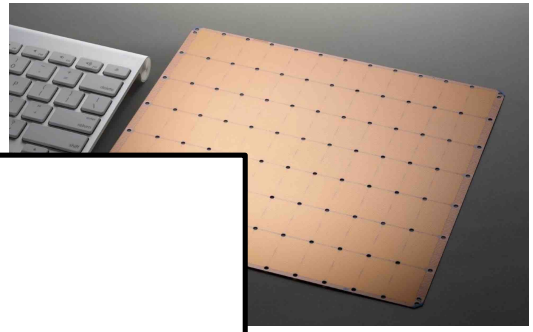
10^2

10^1

10^0

Data colle





Scale Engine (2019)
x 215 mm
Optimized Cores

Key Observation

The combination of parallelism and specialization is steadily increasing *on-chip asymmetry*, which motivates *fine-grain power-control techniques*

Specialization

Gene
Purpo

Multic
Manycore

Vector
Vector-thread

Triggered Instructions

CNN/DNN Accelerators
GPGPU

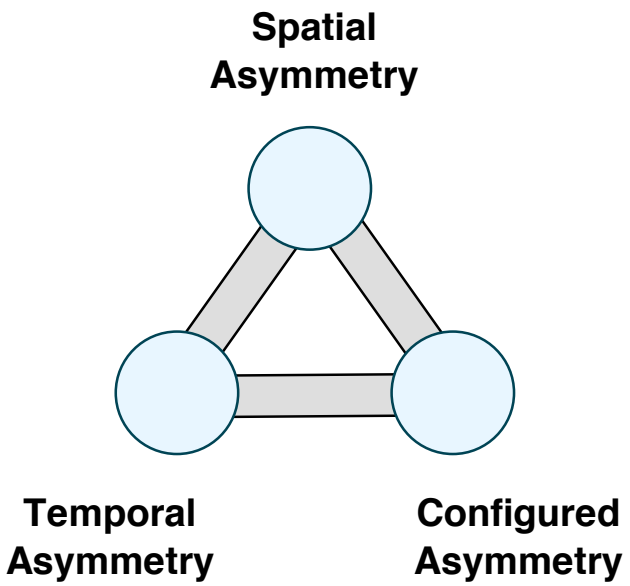
plication-Specific
Accelerators

ypto / Compression
Video encoders
Video decoders

Flexible

Efficient

A Trend of Increasing On-Chip Asymmetry



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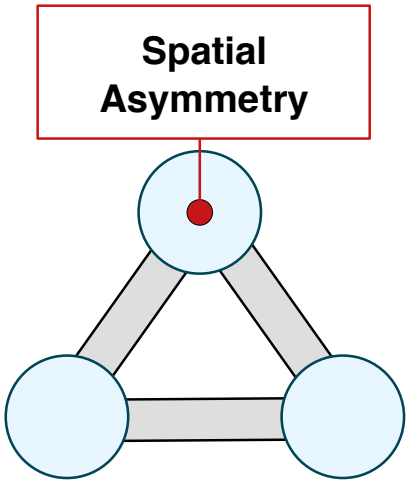
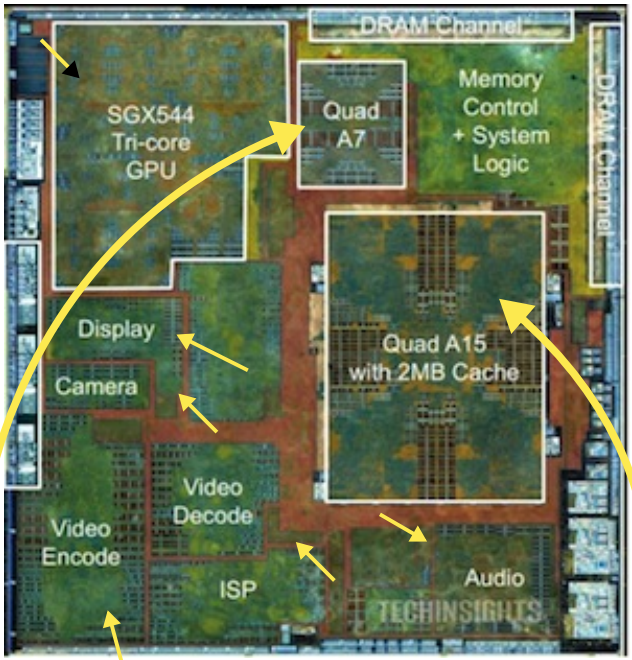


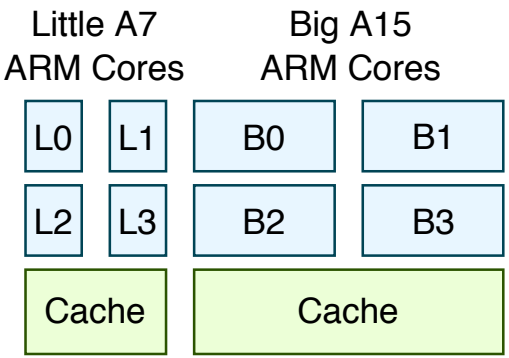
Temporal Asymmetry

Configured Asymmetry

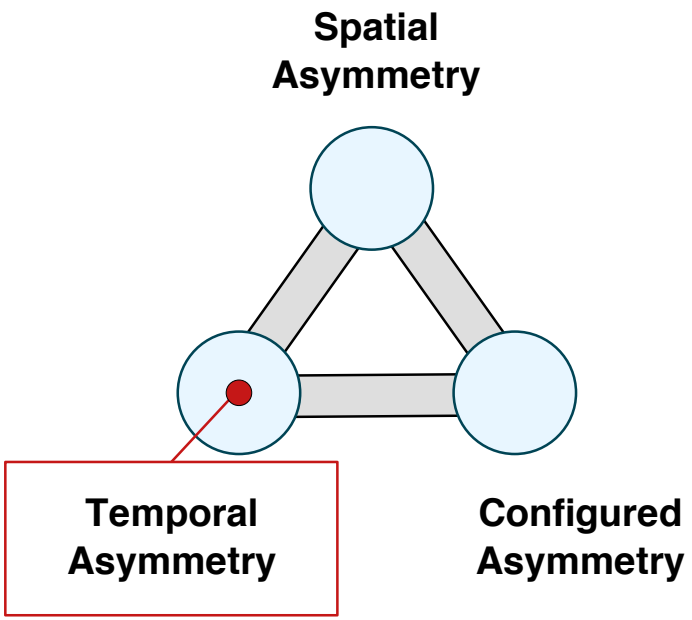
Spatial Asymmetry - Varies across chip

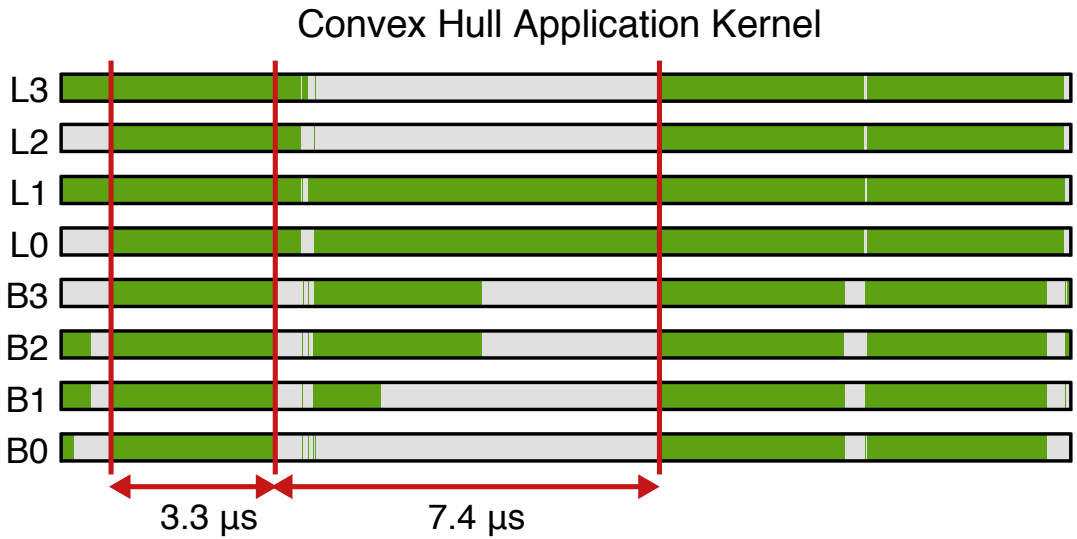


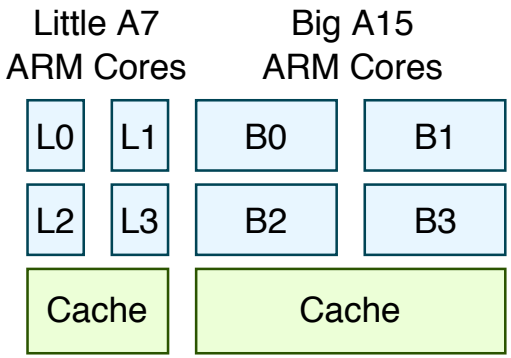
Samsung Exynos Octacore



A Trend of Increasing On-Chip Asymmetry





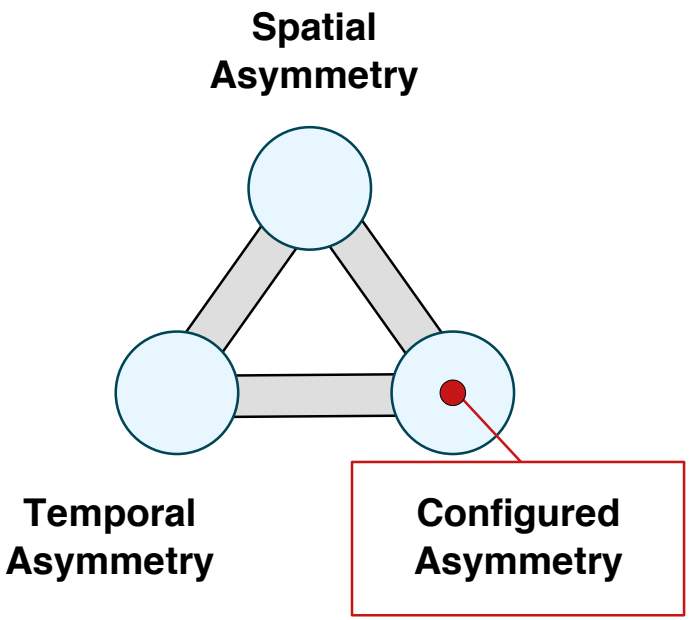


Spatial Asymmetry - Varies across chip

Temporal Asymmetry - Varies at runtime

See also: Kim et al. "System Level Analysis of Fast, Per-Core DVFS" HPCA 2008

A Trend of Increasing On-Chip Asymmetry

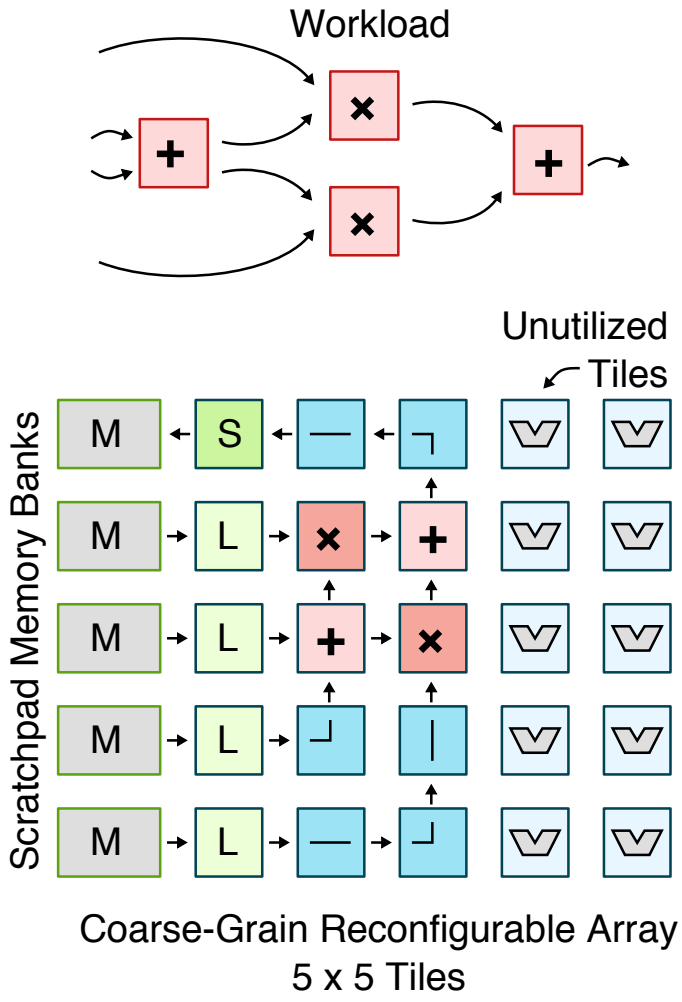


Spatial Asymmetry - Varies across chip

Temporal Asymmetry - Varies at runtime

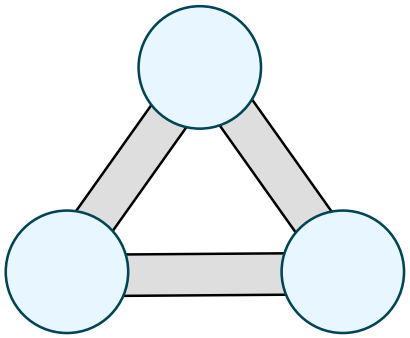
Configured Asymmetry - Set at configure time

Limited Reconfiguration - Similar to purely spatial asymmetry
Rapid Reconfiguration - Increases temporal asymmetry



See also: Mei et al. "ADRES", FPL 2003

A Trend of Increasing On-Chip Asymmetry



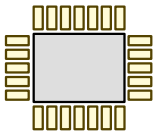
Increasing on-chip asymmetry motivates
fine-grain power-control techniques

Spatial Asymmetry - Varies across chip

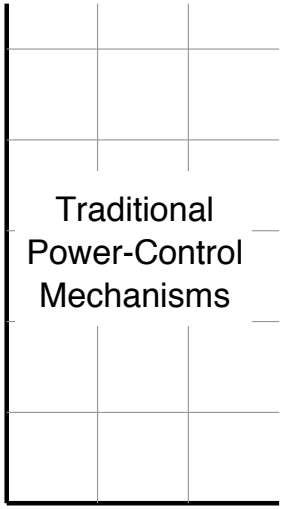
Temporal Asymmetry - Varies at runtime

Configured Asymmetry - Set at configure time

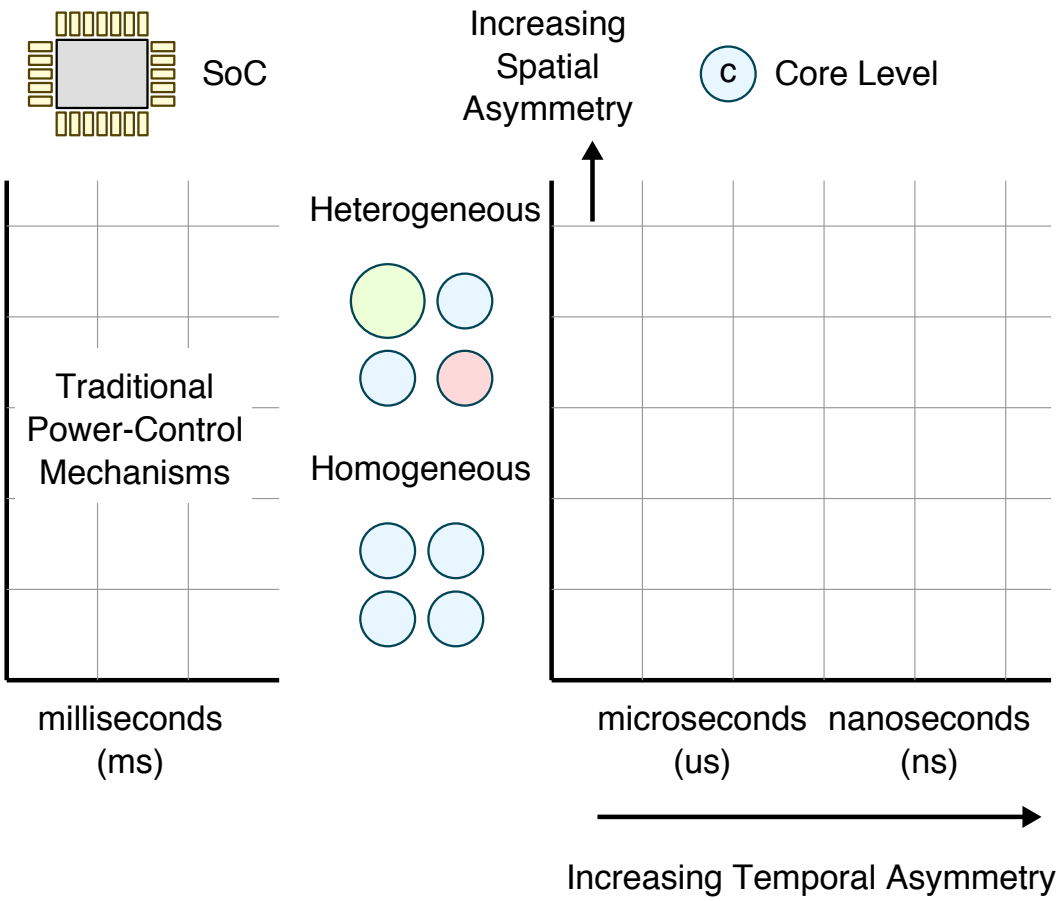
Motivating Fine-Grain Power Control



SoC



Motivating Fine-Grain Power Control



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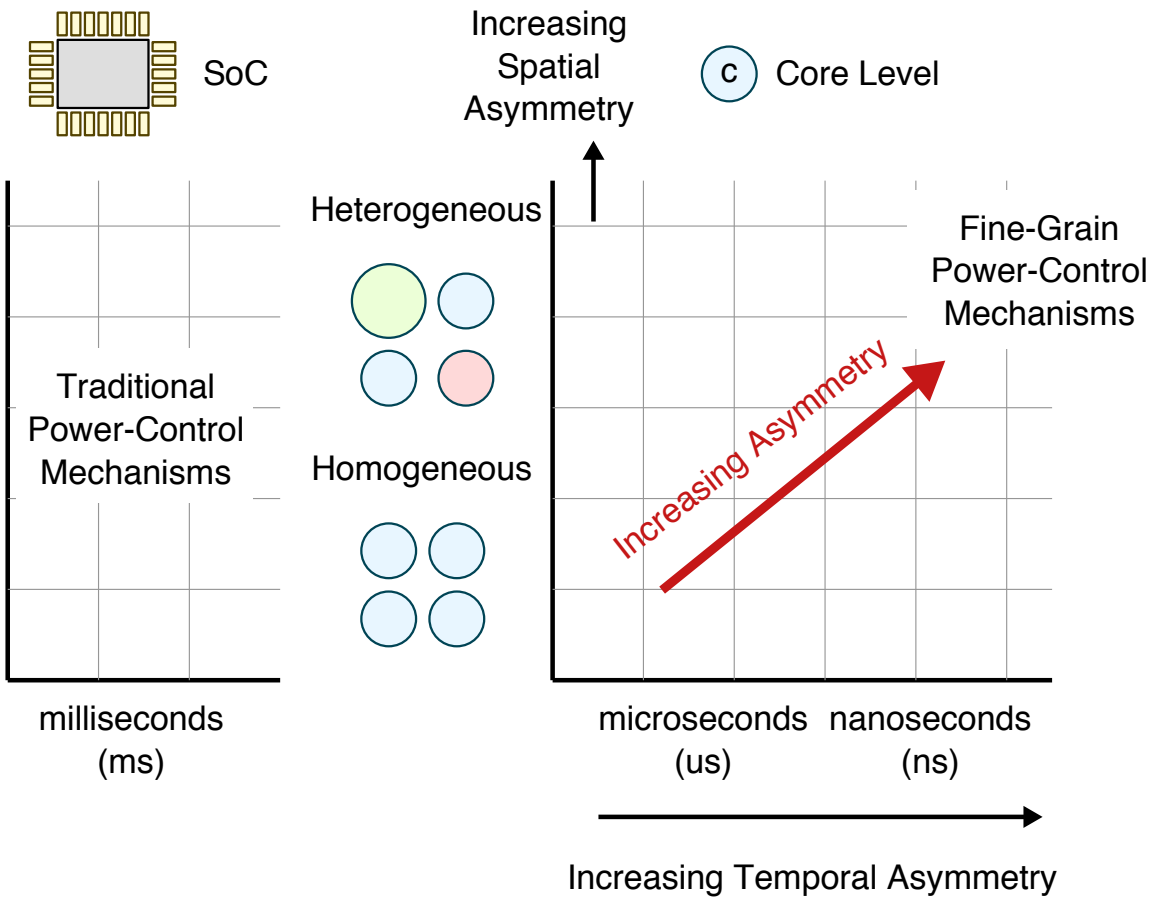

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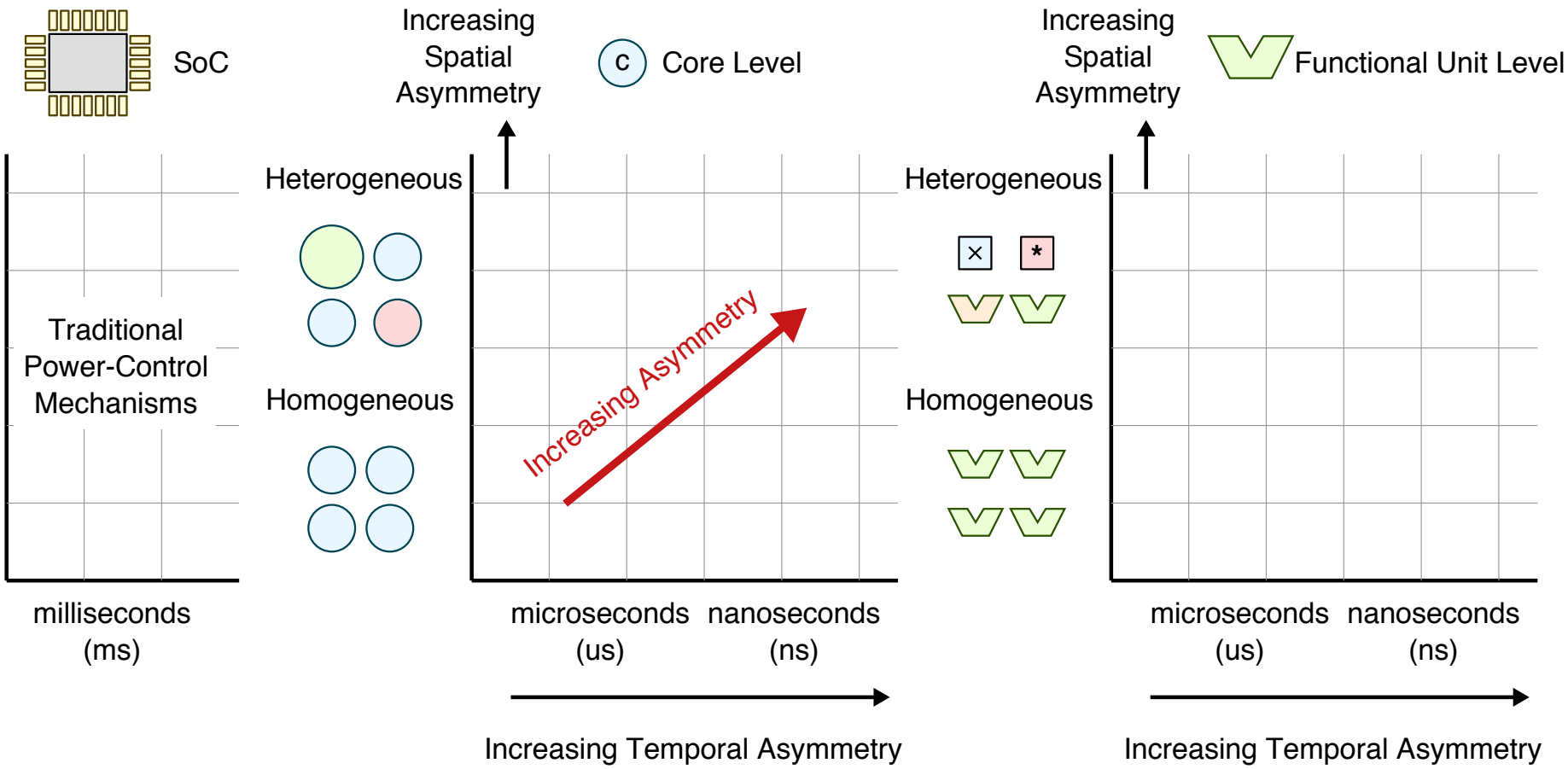

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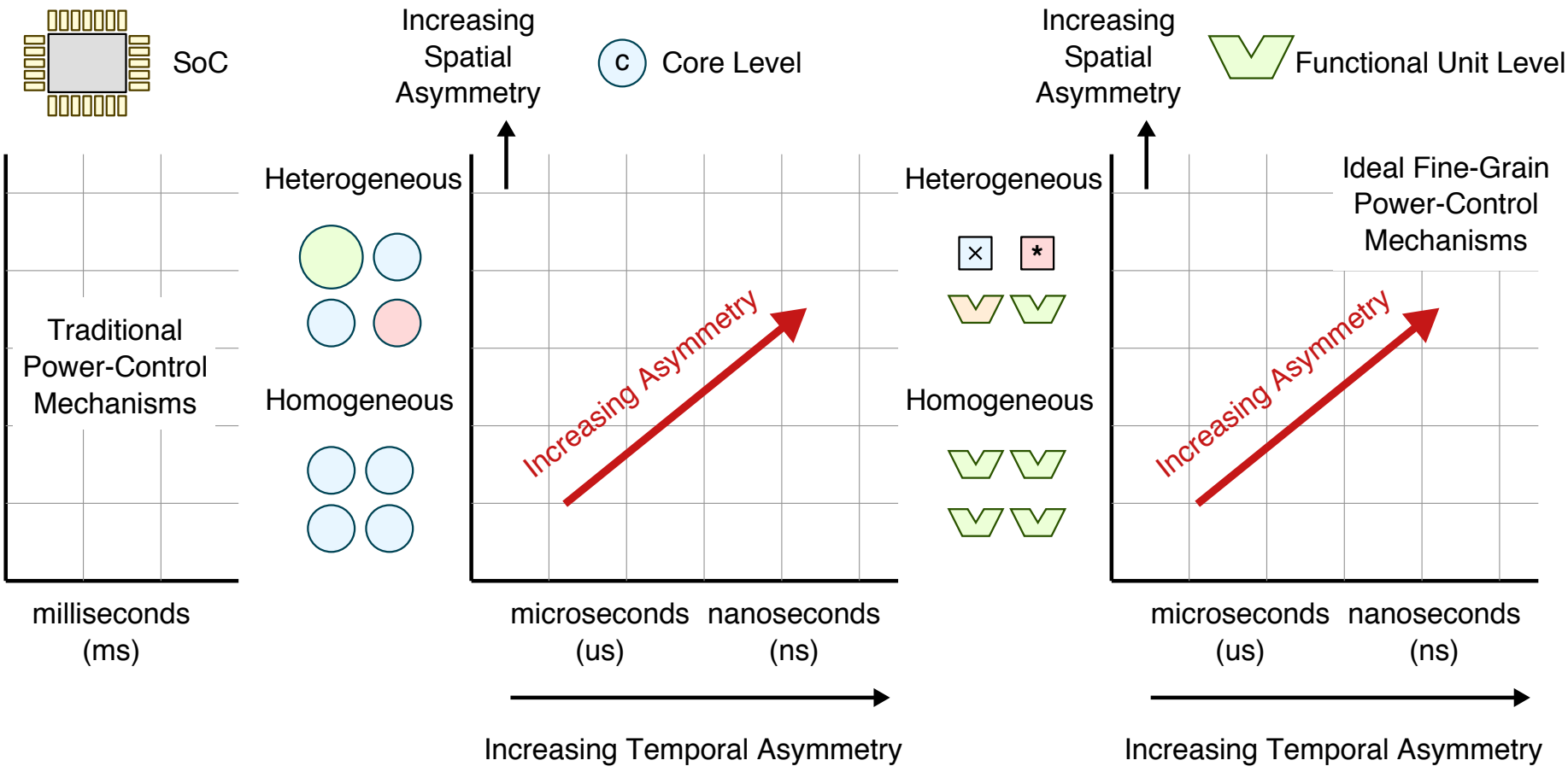
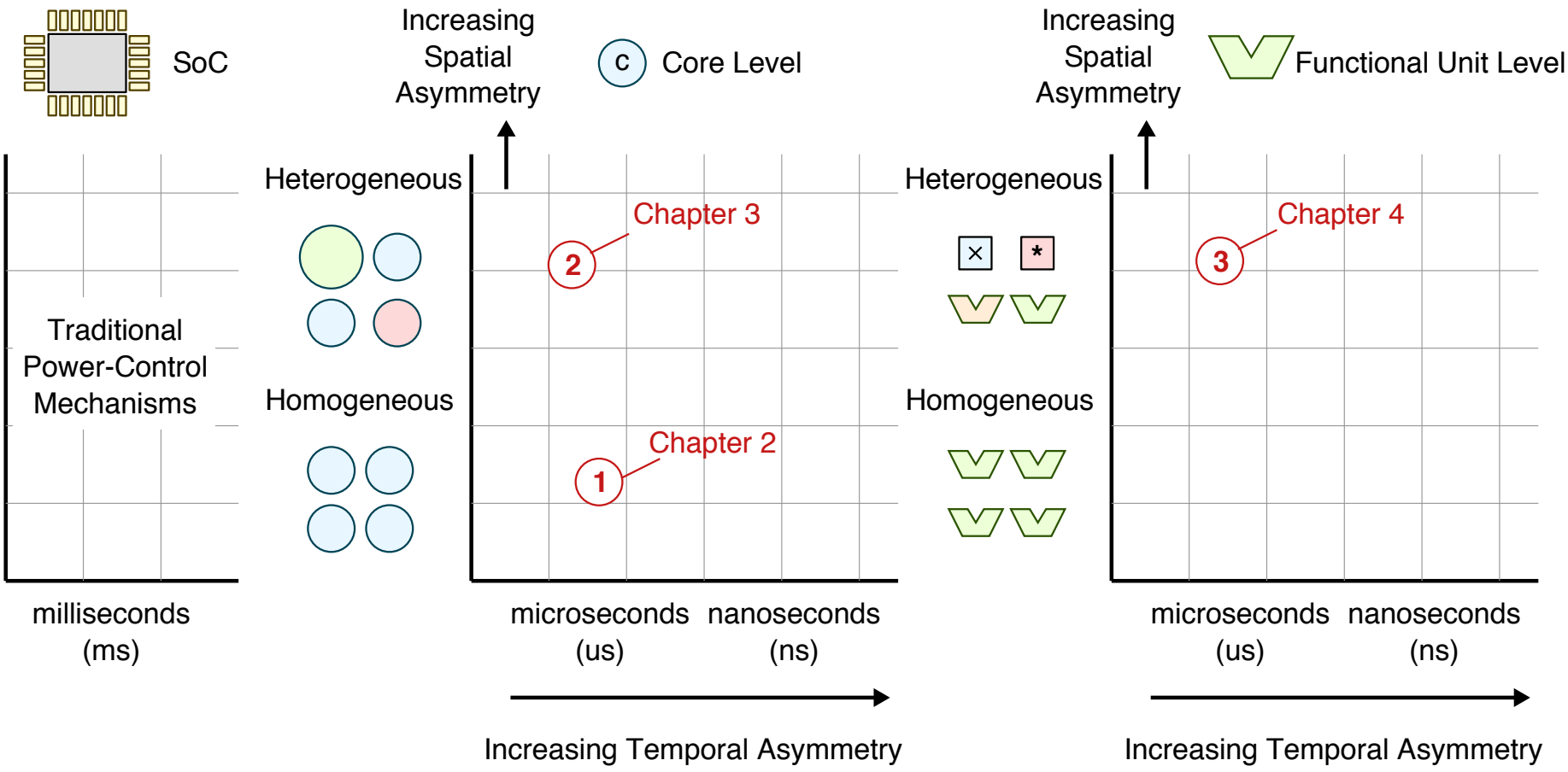


Caveat: Balance flexibility against overheads

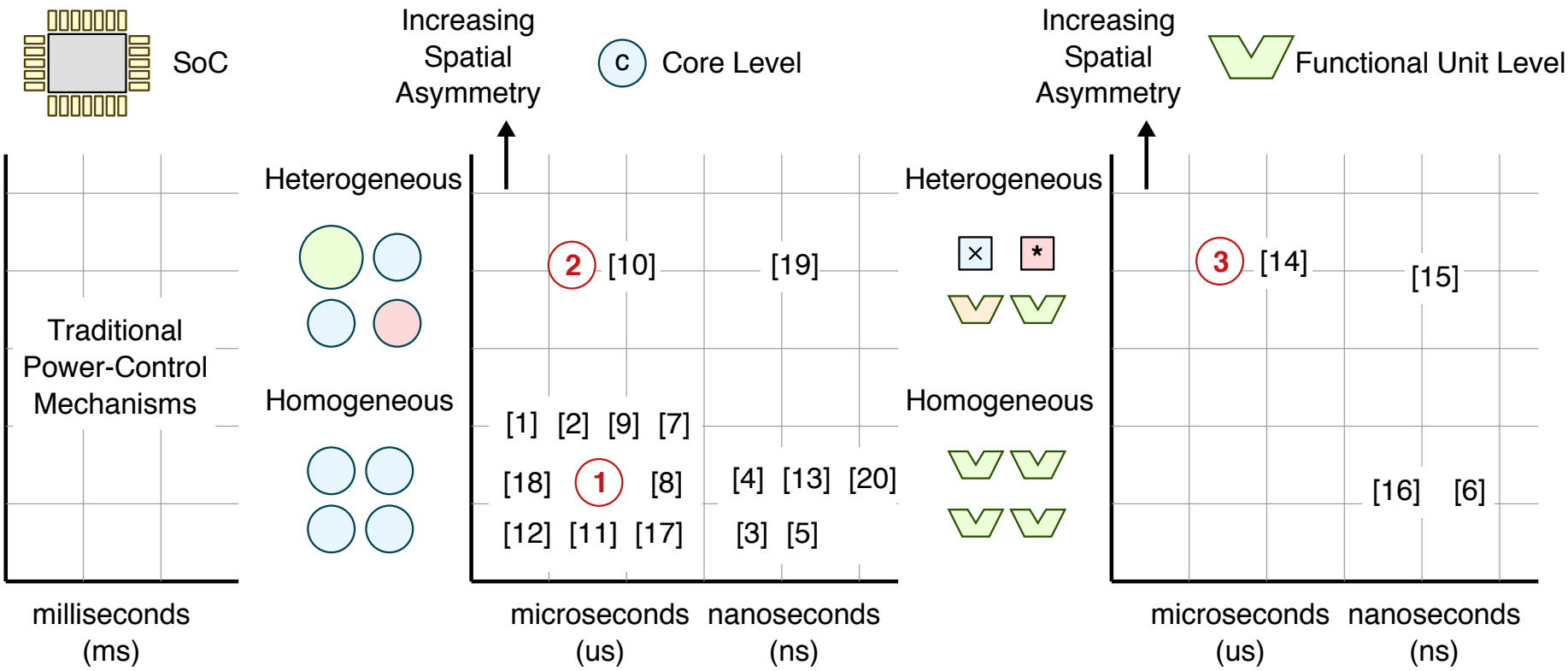
Motivating Fine-Grain Power Control



Thesis Goal

Explore a range of fine-grain power-control techniques across different application domains at both the core- and functional-unit levels

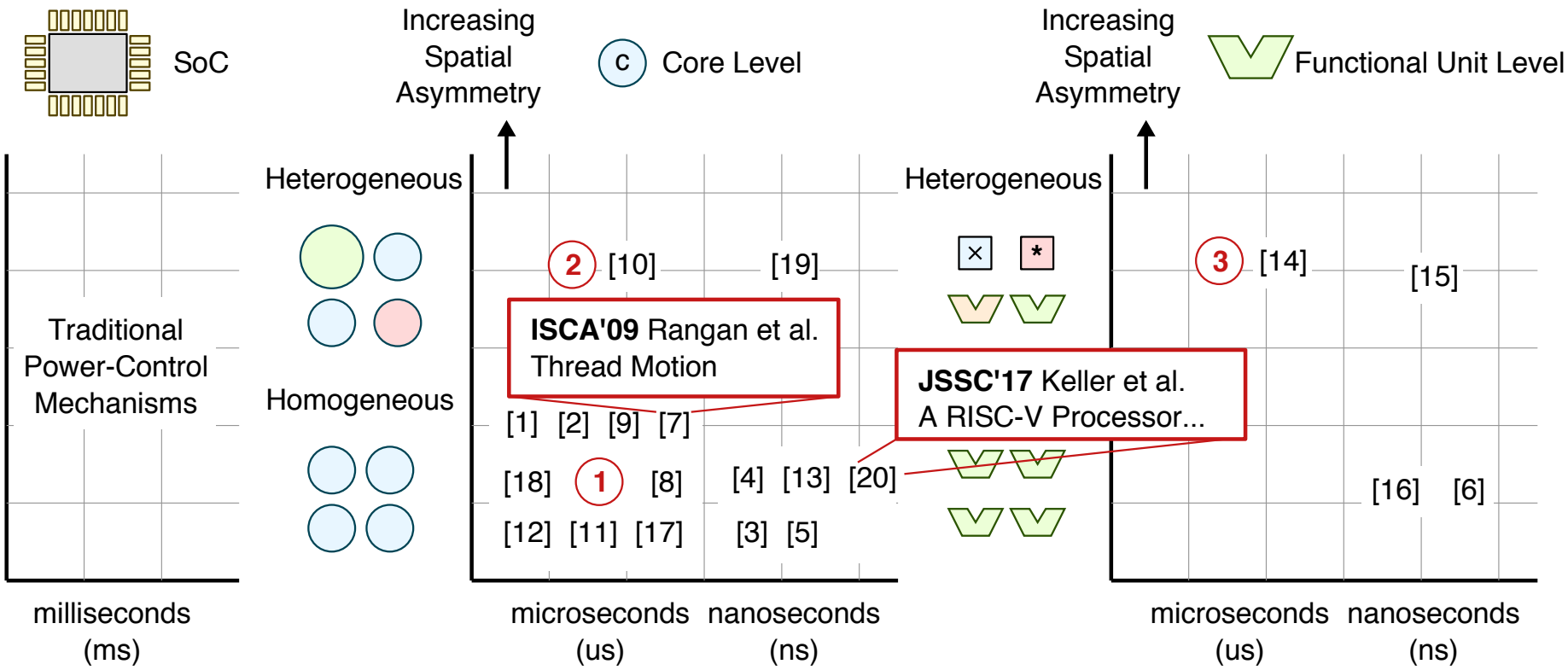
Motivating Fine-Grain Power Control



Selected Works Assuming Fine-Grain Power Control

[1] ISCA'09
[2] HPCA'08
[3] JSSC'09
[4] MICRO'03
[5] PROCIEEE'10
[6] JSSC'06
[7] ISCA'09
[8] ISCA'06
[9] DAC'09
[10] ISCA'05
[11] IEEEMICRO'13
[12] HPCA'14
[13] HPCA'12
[14] MICRO'02
[15] SAMOS'13
[16] ESSCIRC'11
[17] ASPLOS'14
[18] HPCA'15
[19] PACT'14
[20] JSSC'17

Motivating Fine-Grain Power Control



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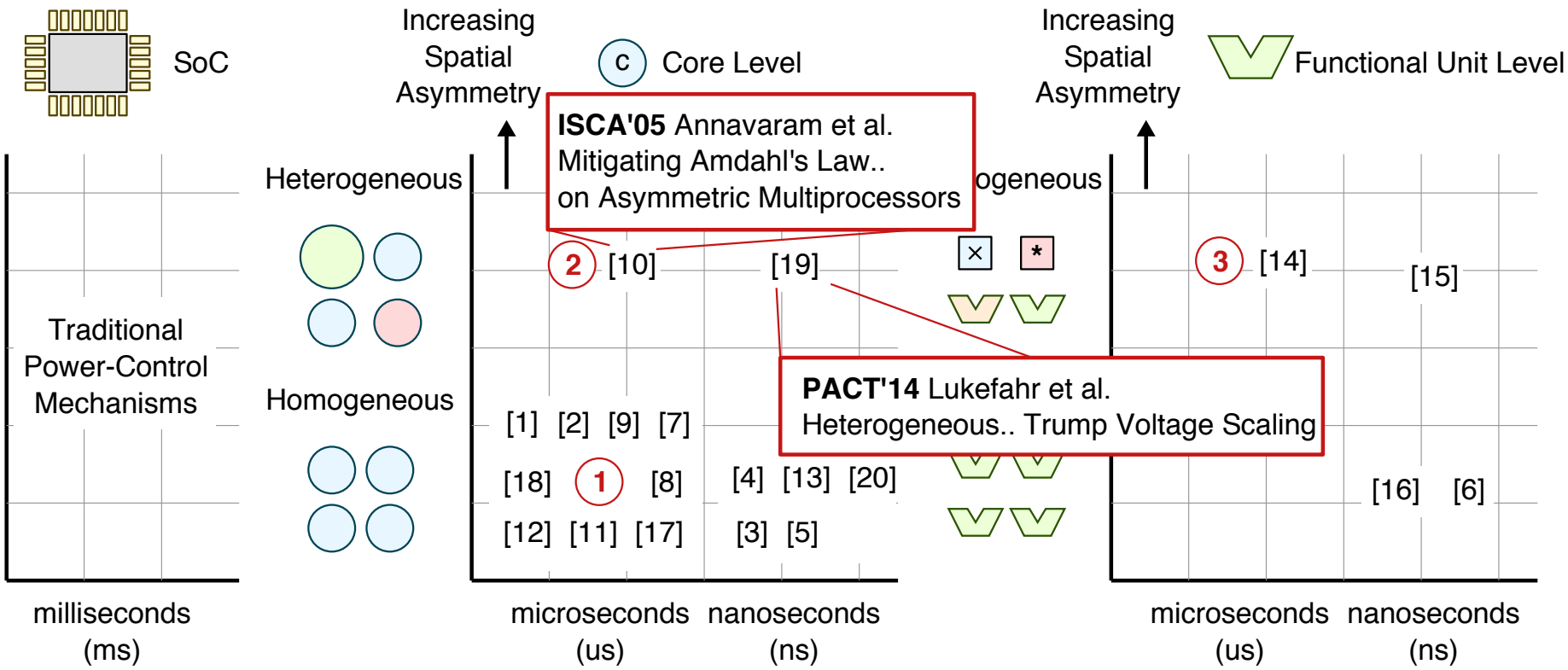

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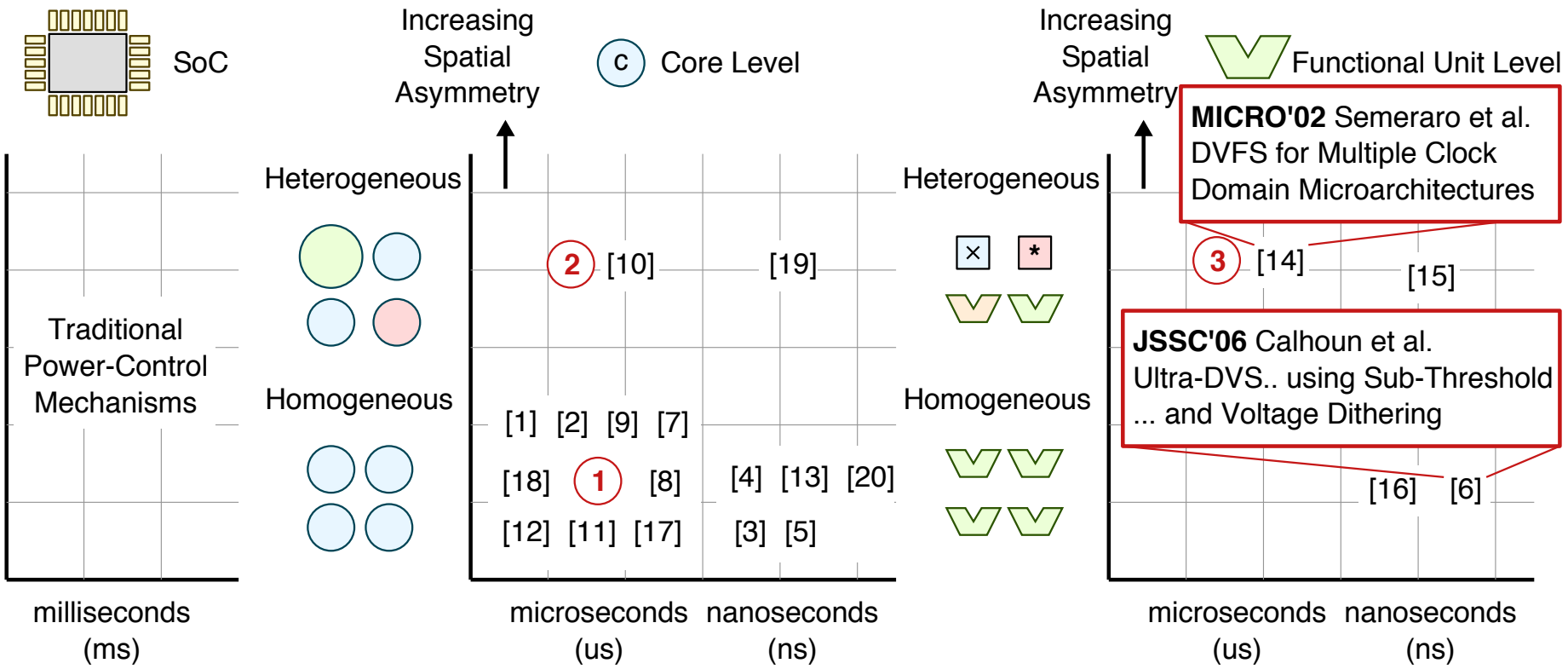
Motivating Fine-Grain Power Control



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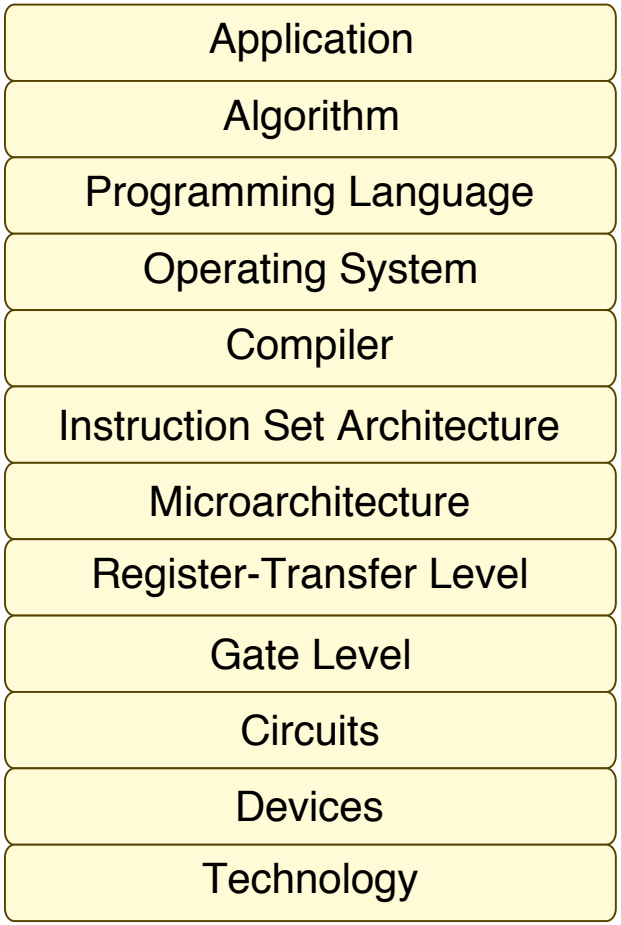
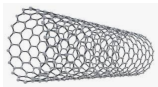
Broken Walls of Abstraction



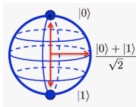
Broken Walls of Abstraction

- Application
- Algorithm
- Programming Language
- Operating System
- Compiler
- Instruction Set Architecture
- Microarchitecture
- Register-Transfer Level
- Gate Level
- Circuits
- Devices
- Technology

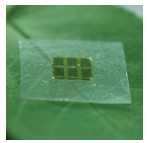
Carbon Nanotubes



Quantum Computing

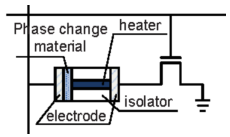


Biodegradable Computing

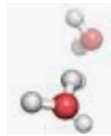


Energy Harvesting

Phase-Change Memory



Molecular Computing



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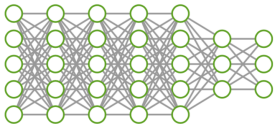
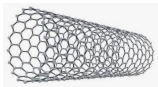


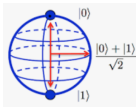
Cybersecurity

Smart Healthcare

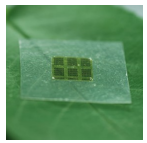
Carbon Nanotubes



Quantum Computing



Biodegradable Computing



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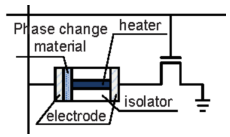
Phase-Change Memory



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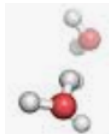

Broken Walls of Abstraction

- Application
- Algorithm
- Programming Language
- Operating System
- Compiler
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- Microarchitecture
- Register-Transfer Level
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- Circuits
- Devices
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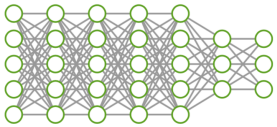
AR / VR

Autonomous Driving

Smart Home

Graph Analytics

AI

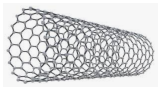


Cybersecurity

Smart Healthcare

Computer Architecture

Carbon Nanotubes



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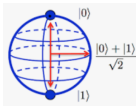

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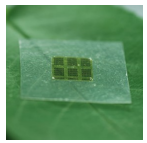

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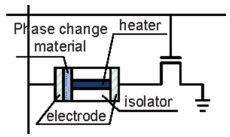
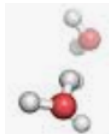


Molecular Computing



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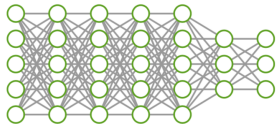

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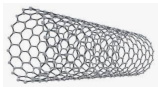

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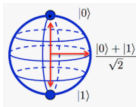

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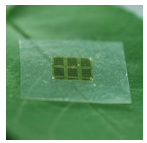

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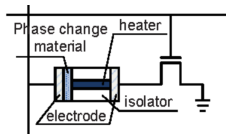

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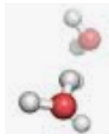
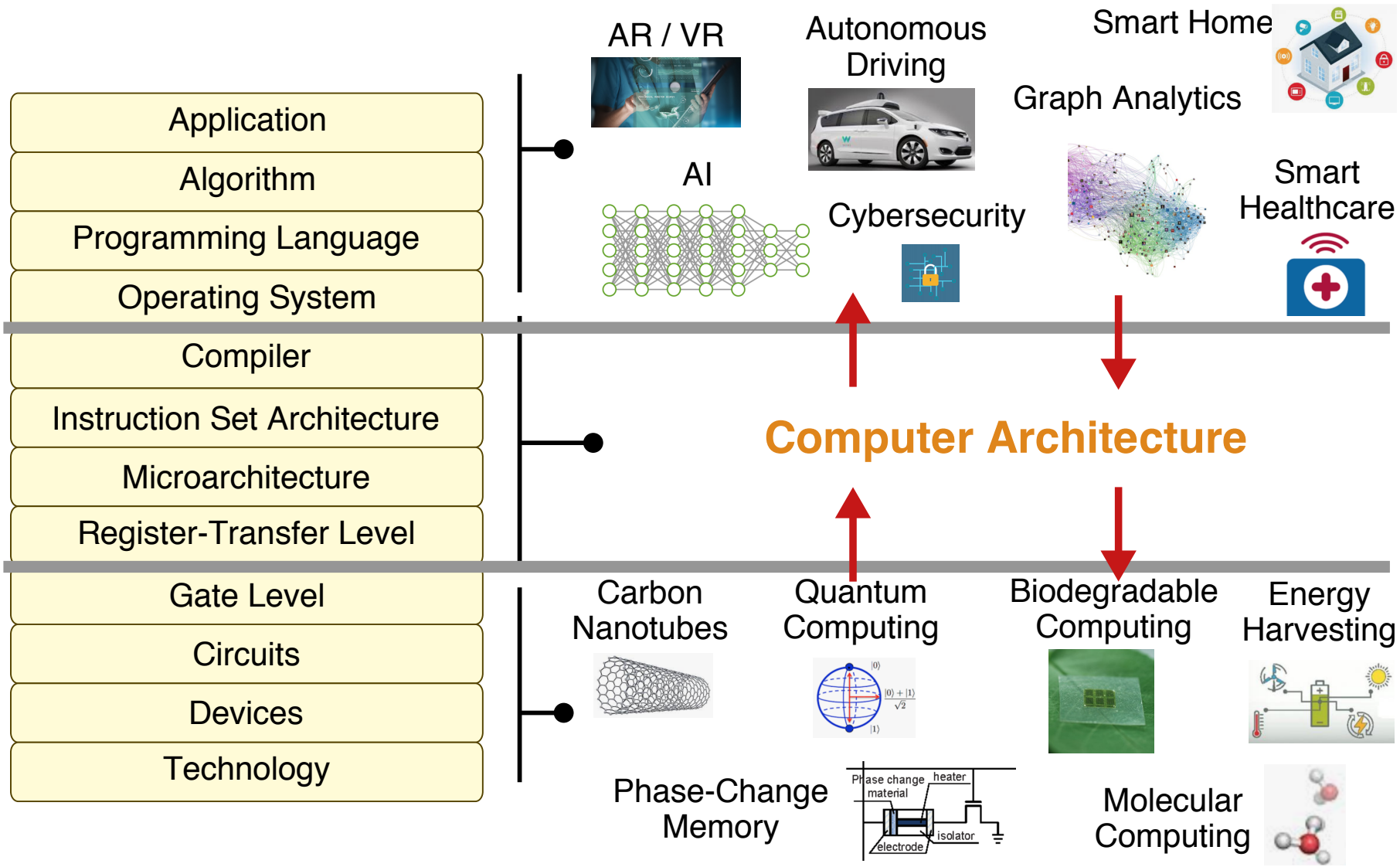
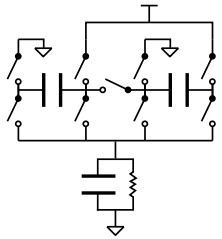


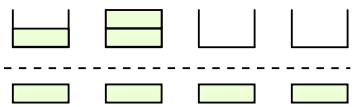
Broken Walls of Abstraction



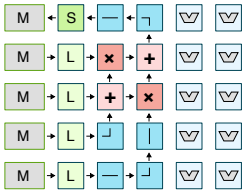
Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry



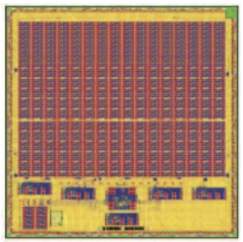
Exploiting Fine-Grain Asymmetry with
On-Chip Voltage Regulation - **MICRO'14**, IEEE TCAS I'18



Exploiting Fine-Grain Asymmetry in
Task-Based Parallel Runtimes - **ISCA'16**, MICRO'17, RISCV'18



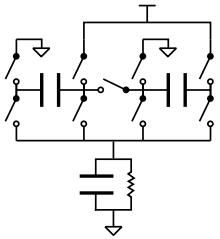
Exploiting Fine-Grain Asymmetry in
Coarse-Grain Reconfigurable Arrays - **Unpublished**



Exploiting Fine-Grain Asymmetry with
Silicon Prototyping - **IEEE MICRO'18**, DAC'18, Hotchips'17

Conclusion

Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry



Exploiting Fine-Grain Asymmetry with

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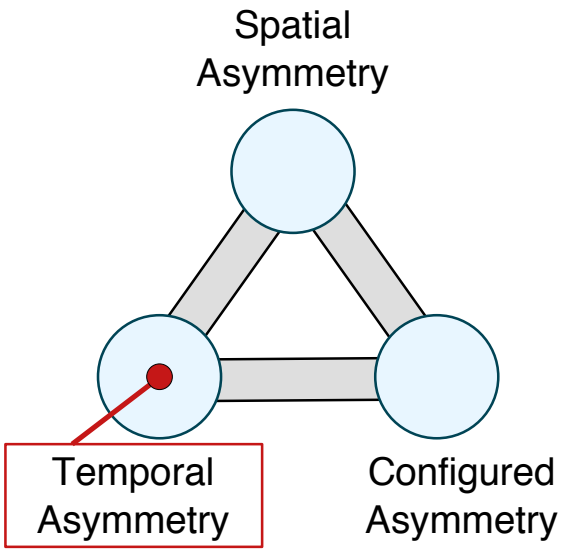

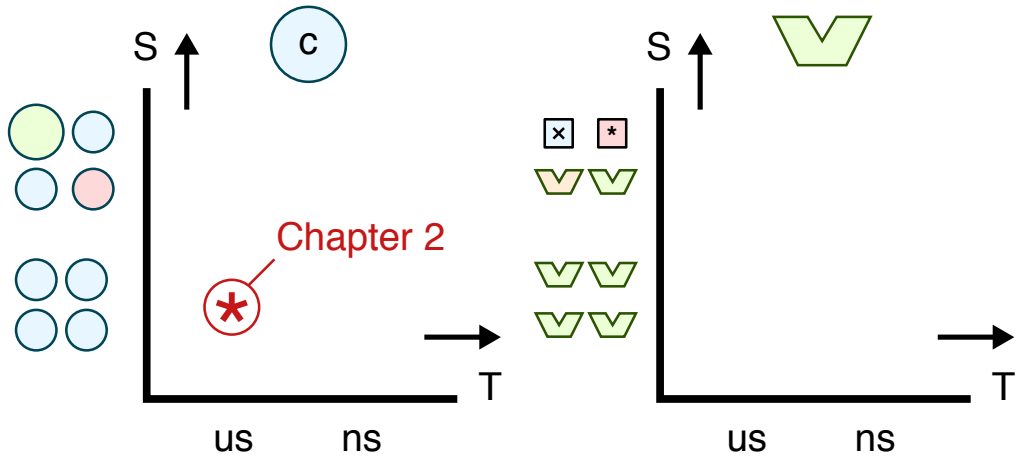

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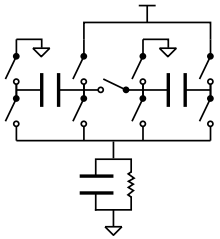

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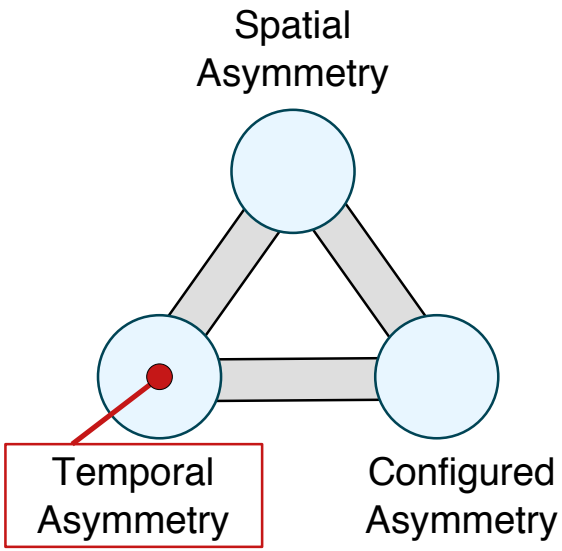
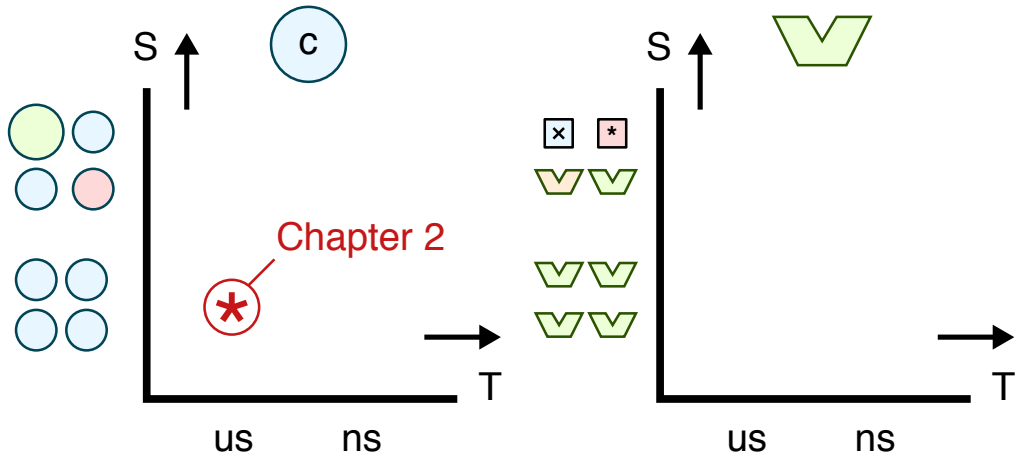
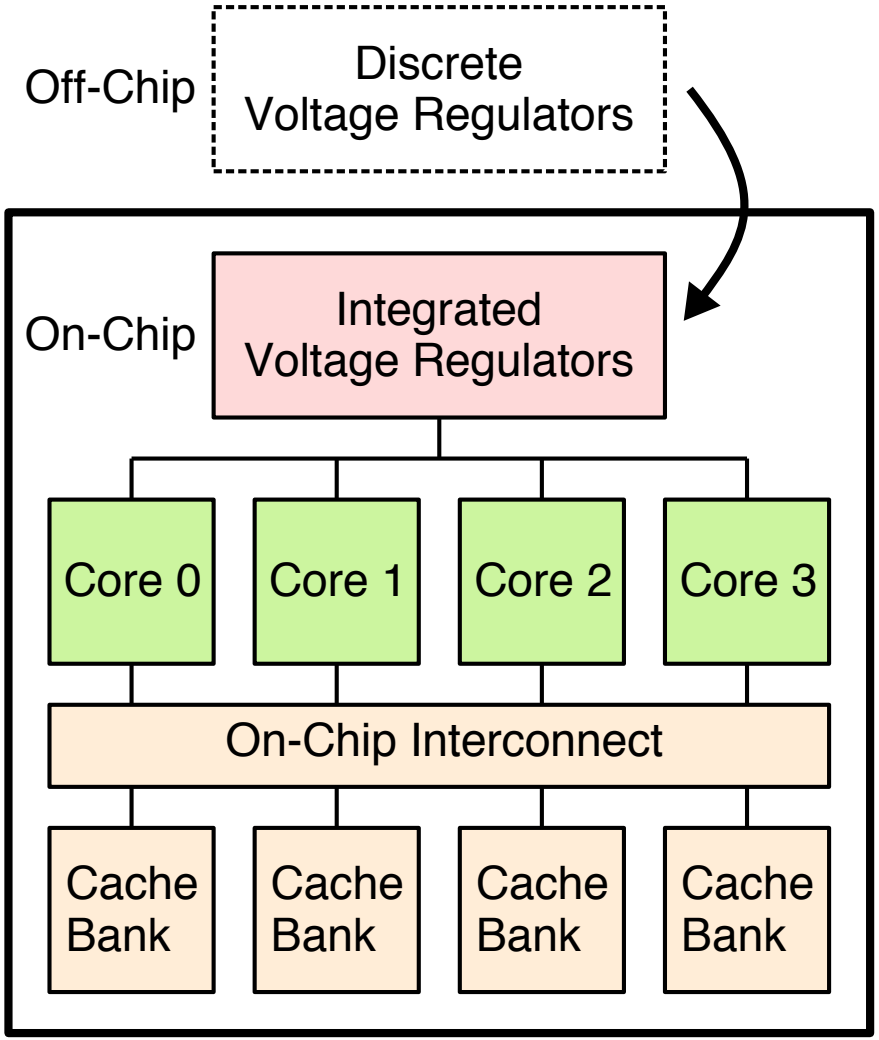




Research Question – Can we use architecture-circuit co-design to enable more efficient fine-grain voltage regulation?

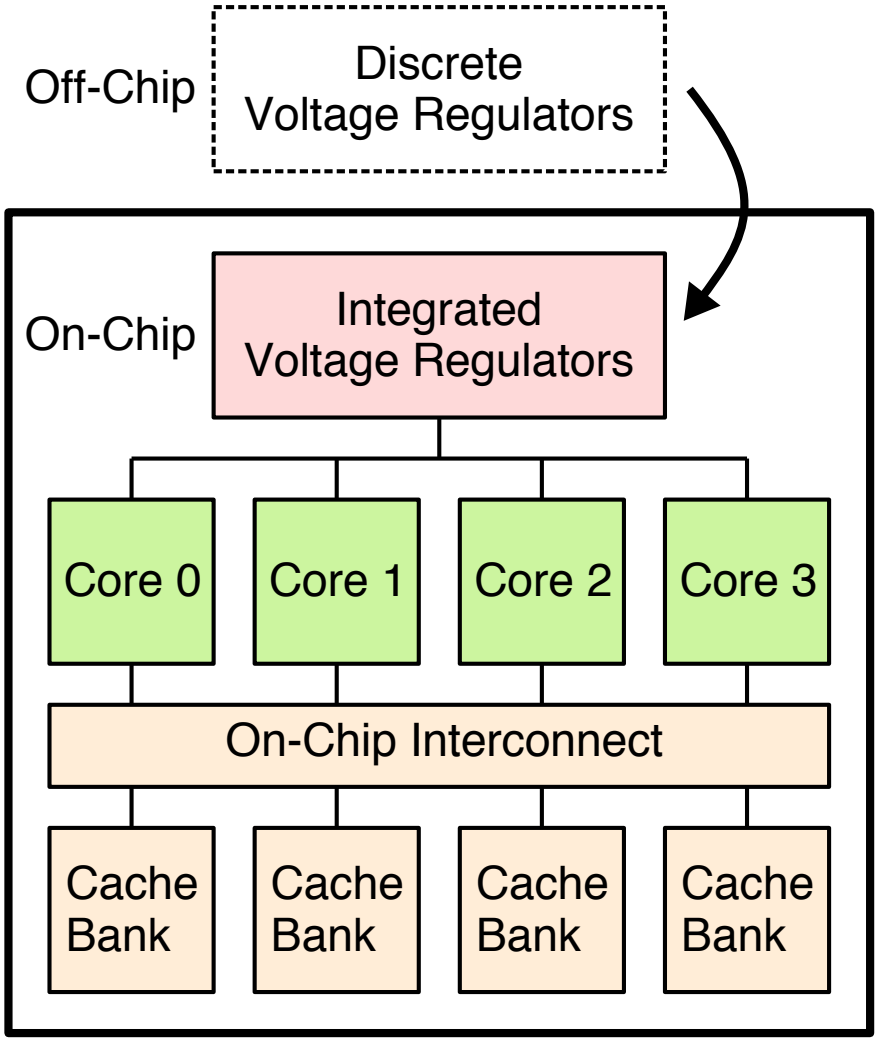
Motivation: Integrated Voltage Regulation (IVR)



Key Benefit of IVR

- Reduced System Cost

Motivation: Integrated Voltage Regulation (IVR)



Key Benefit of IVR

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Challenges of IVR

- Integrated energy-storage elements have low energy densities
- Low switching speeds with high parasitic losses

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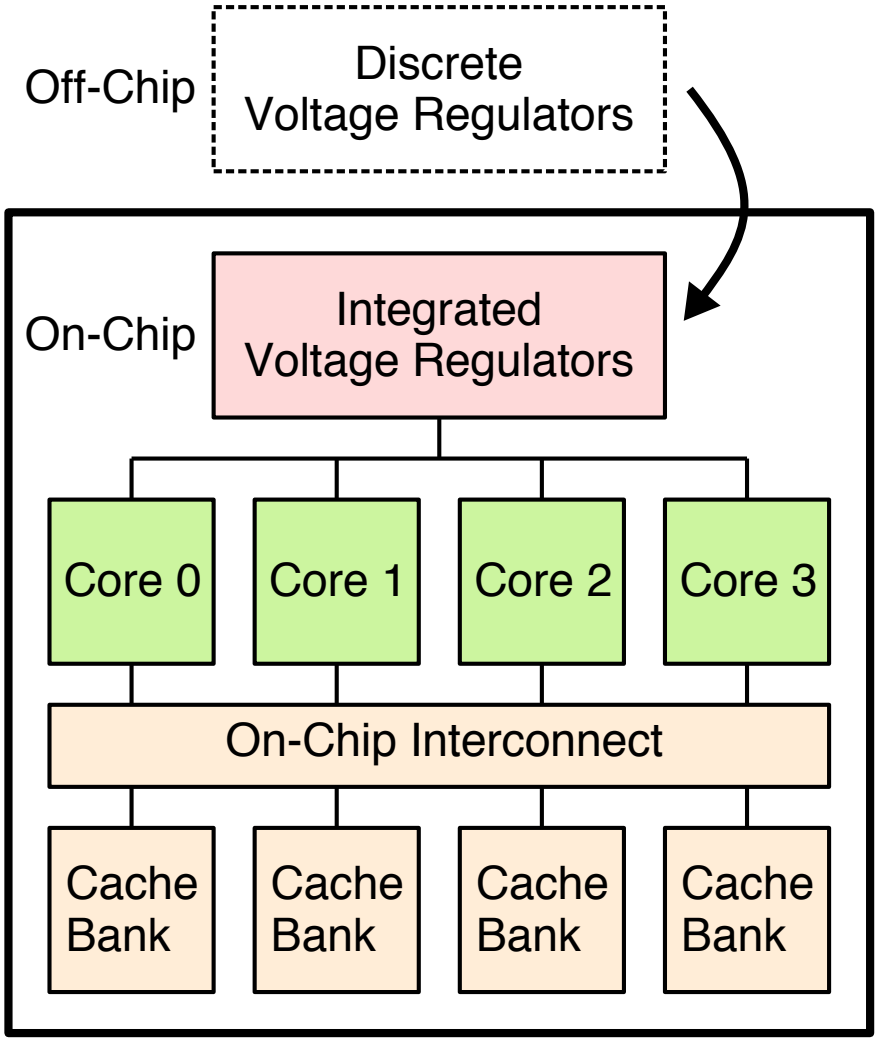

Key Benefit of IVR

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Challenges of IVR

- Integrated energy-storage elements have low energy densities
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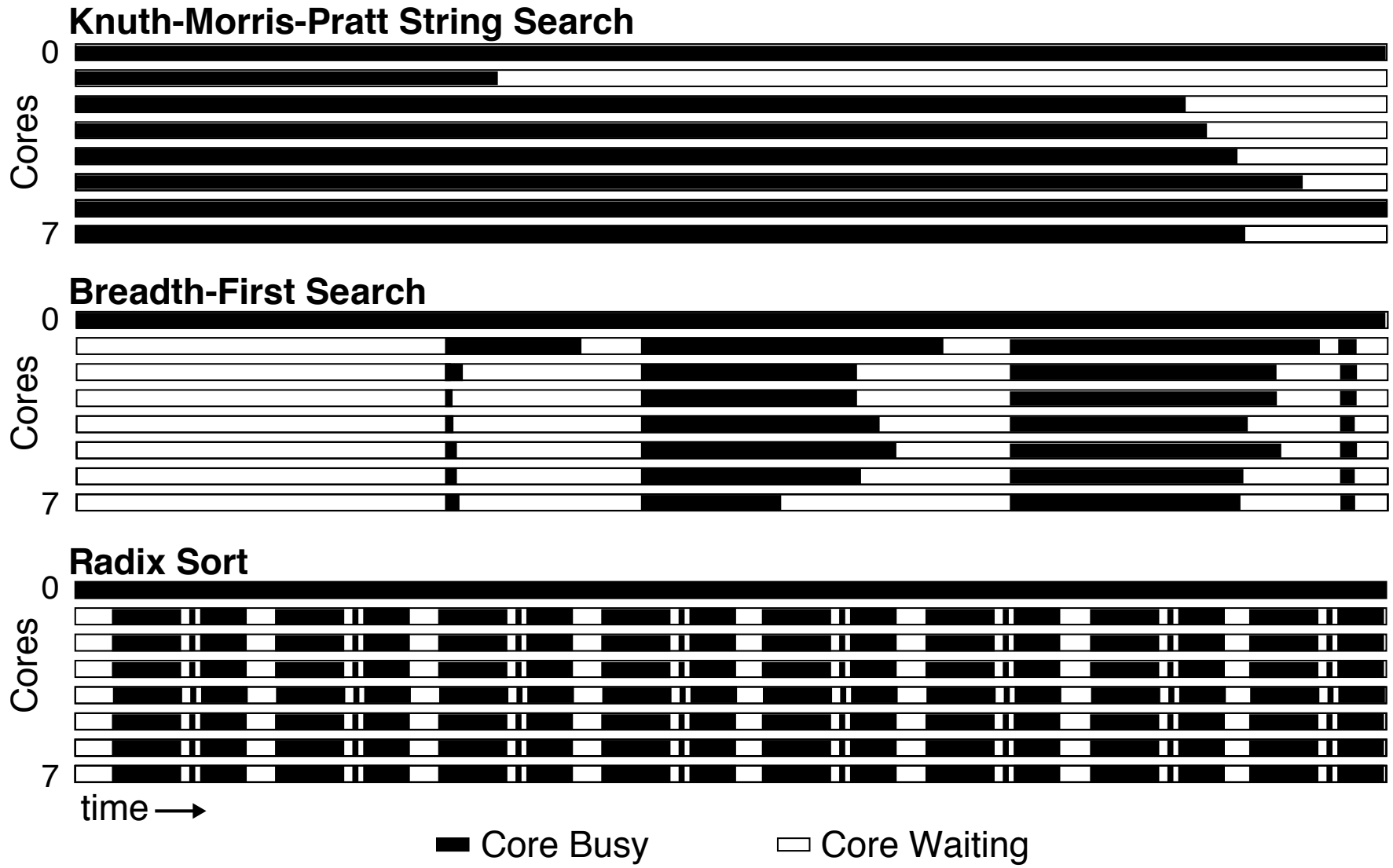
A New Era of IVR

- Energy storage elements have slightly improved energy densities
- Faster switches with low parasitic losses

Fine-Grain Voltage Scaling Opportunities



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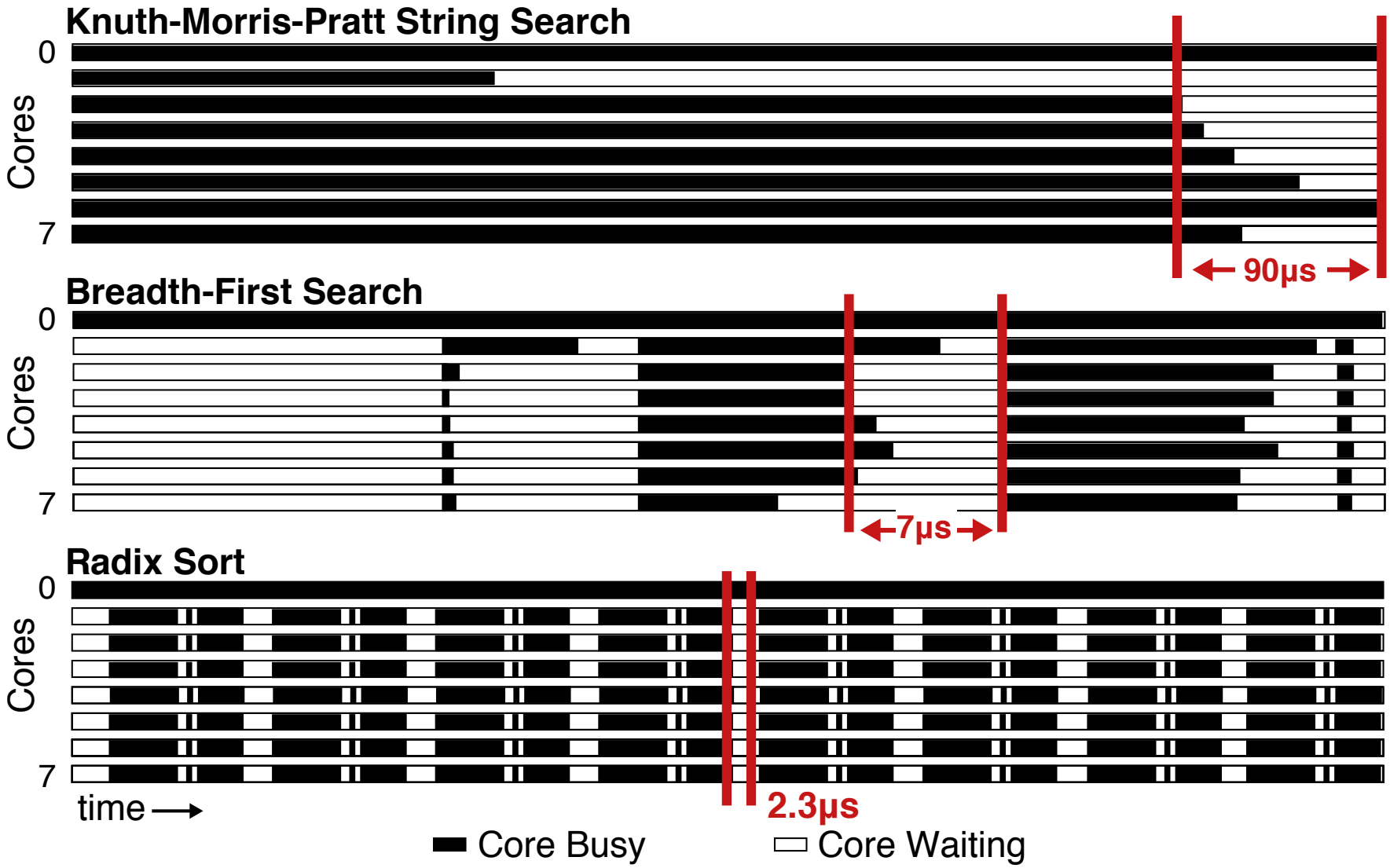
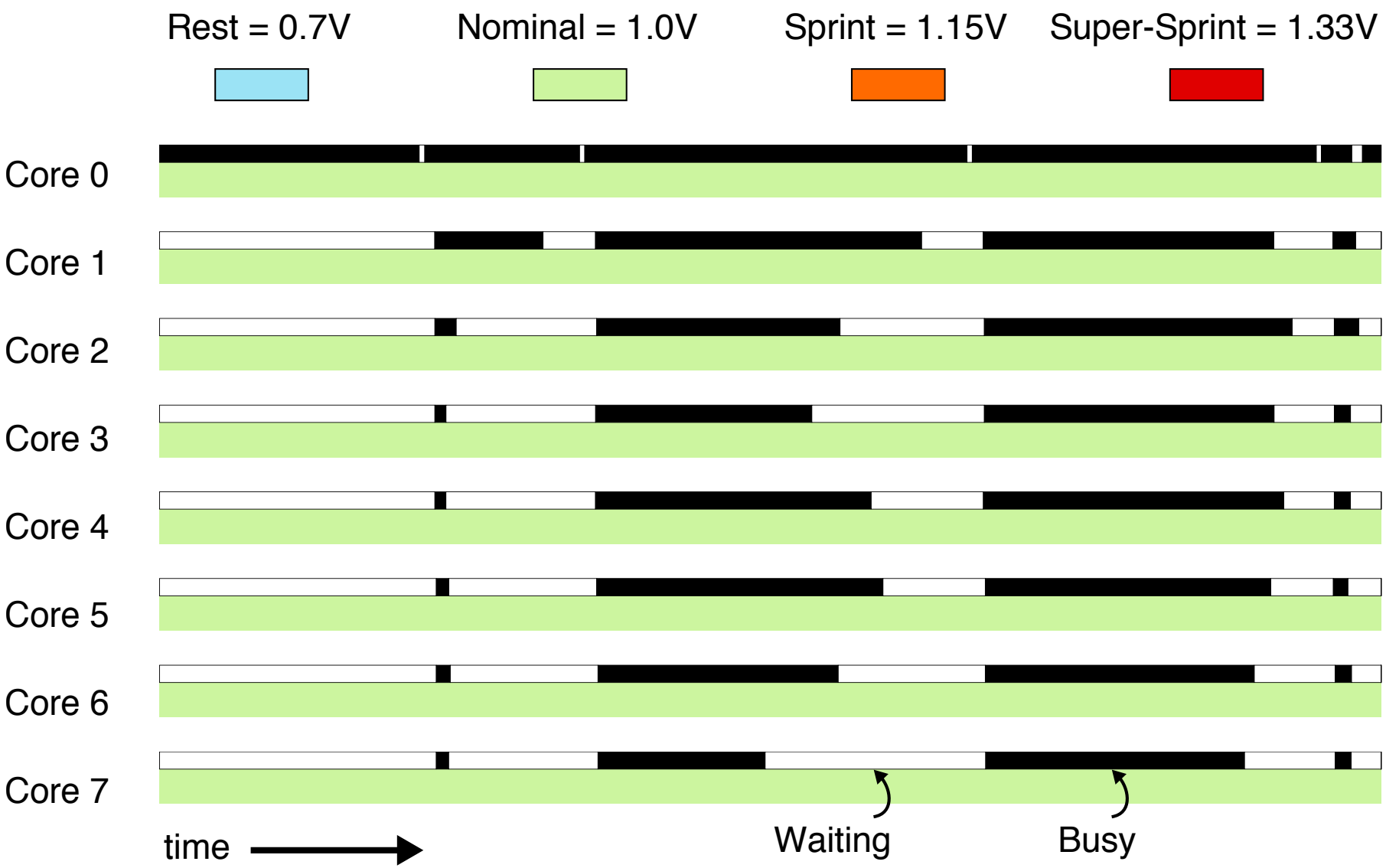


Ideal Fine-Grain Voltage Scaling: Breadth-First Search



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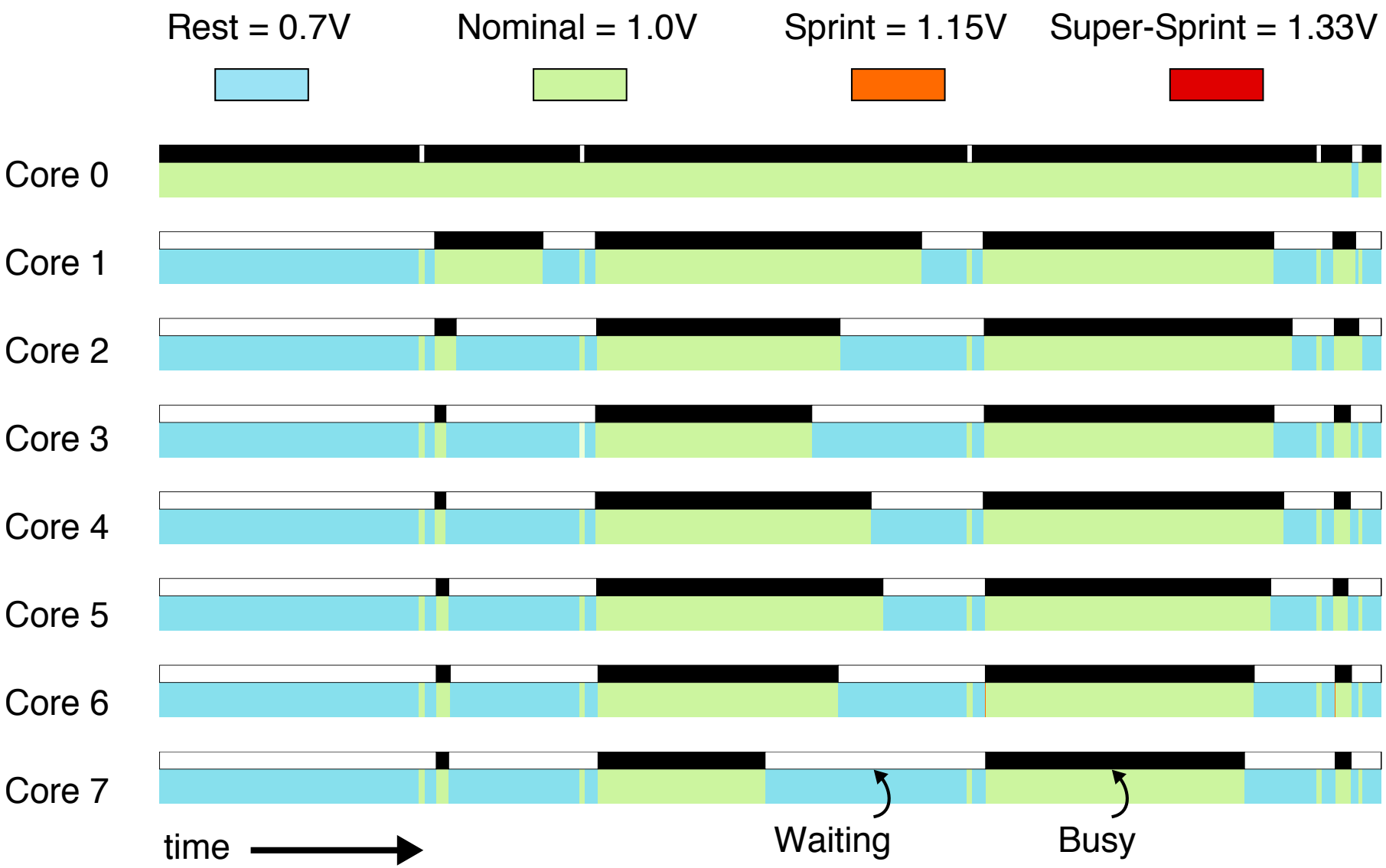

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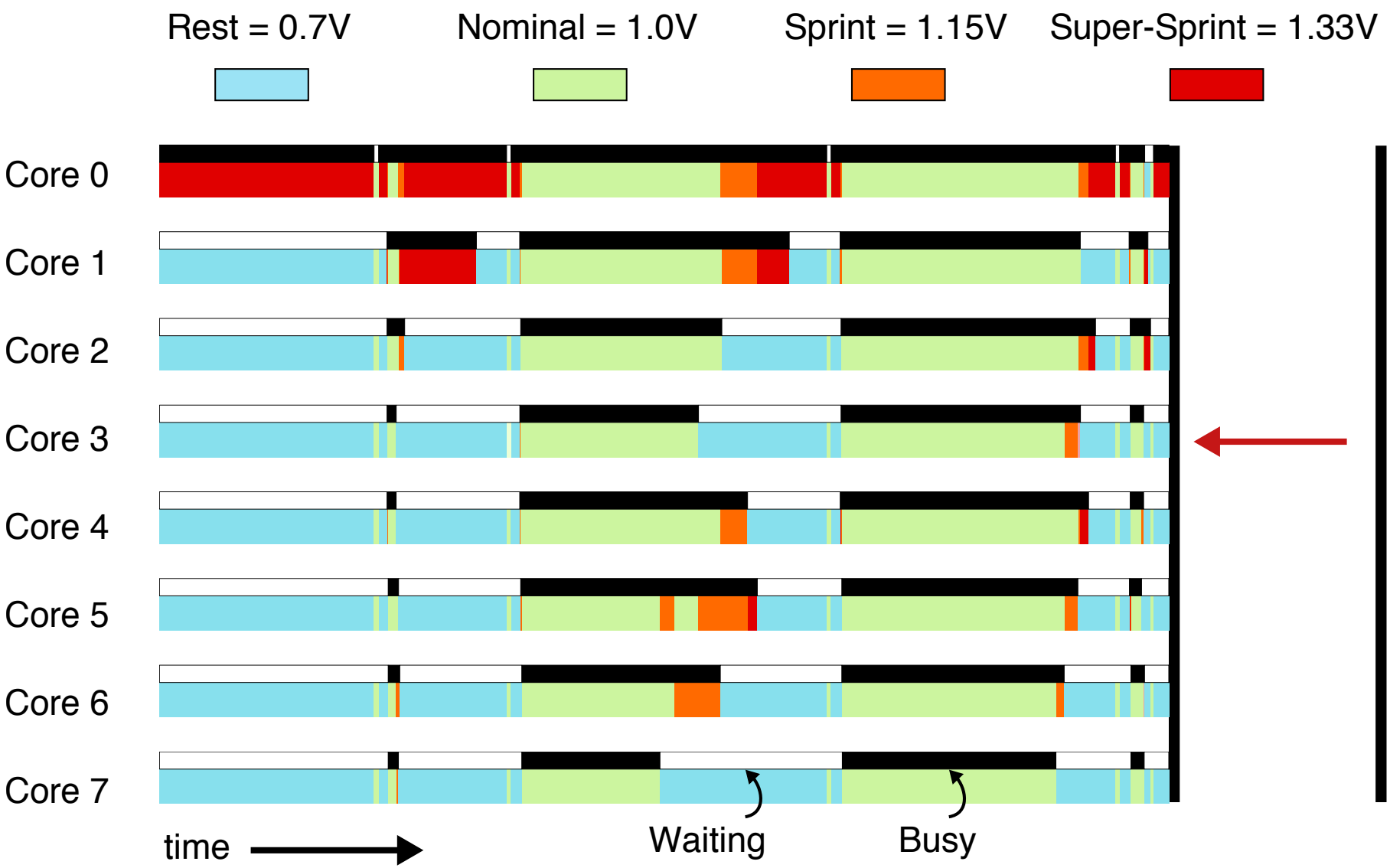

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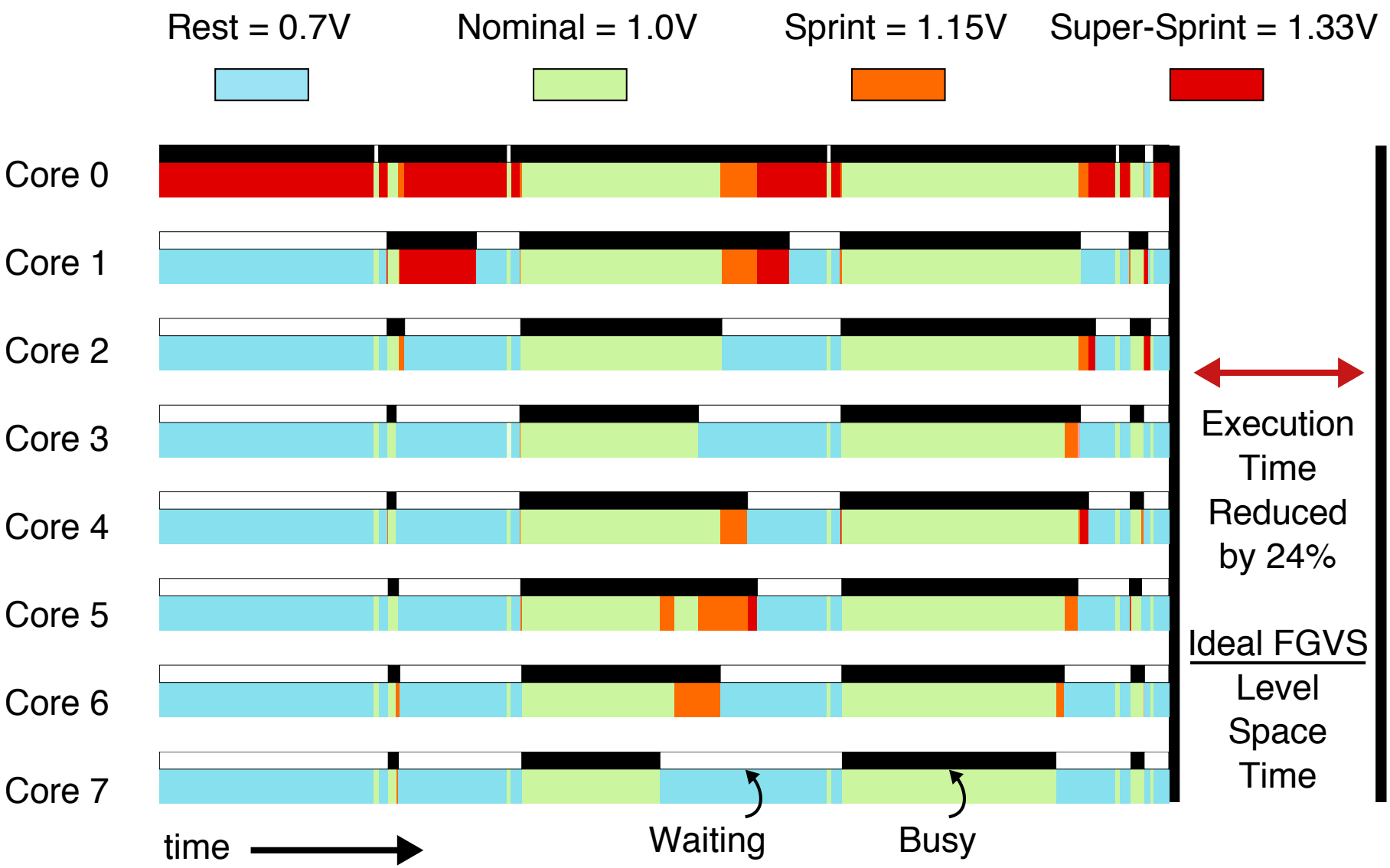
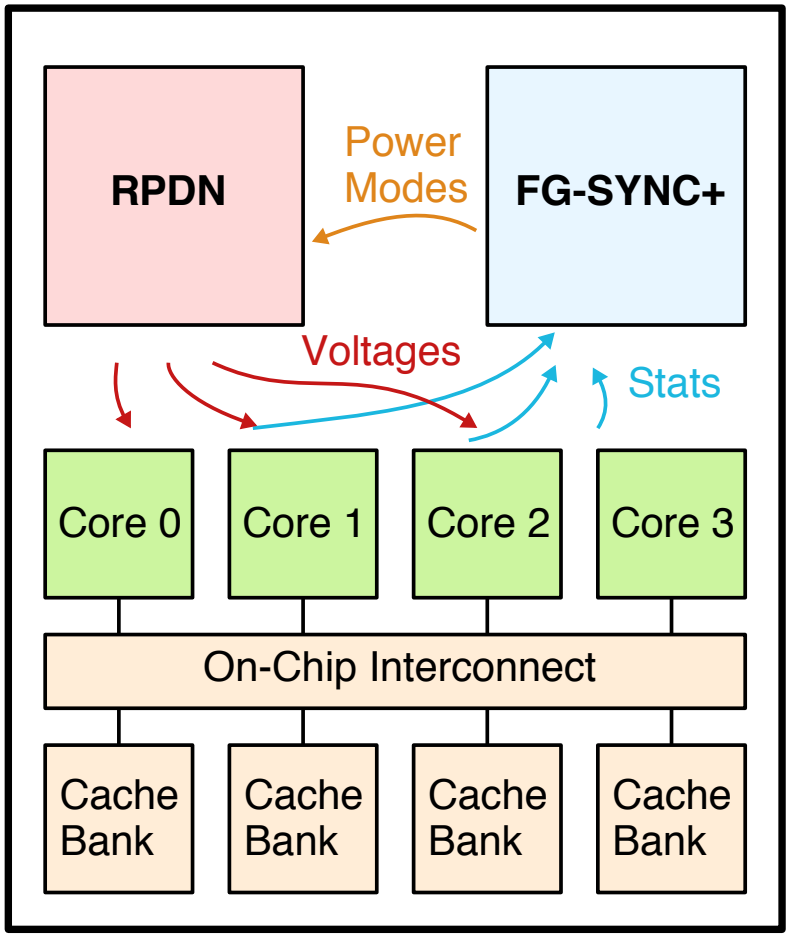


Enabling Realistic Fine-Grain Voltage Scaling



FGVS Architecture: FG-SYNC+

Use lightweight *software hints* and lookup tables derived offline to enable fast multi-level voltage configuration

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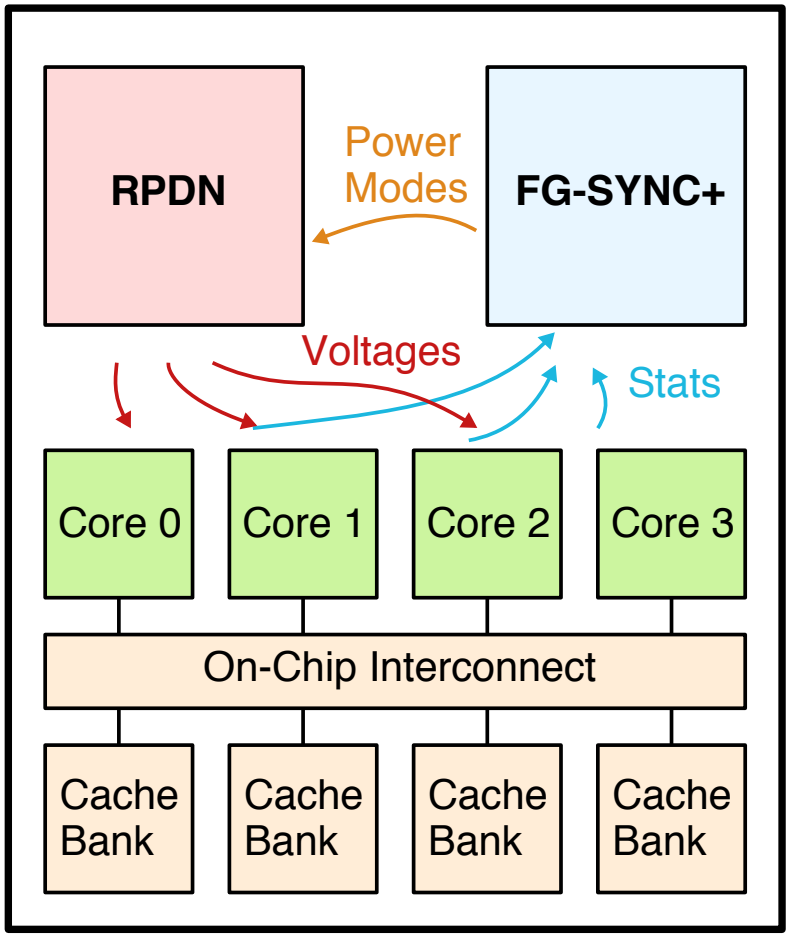


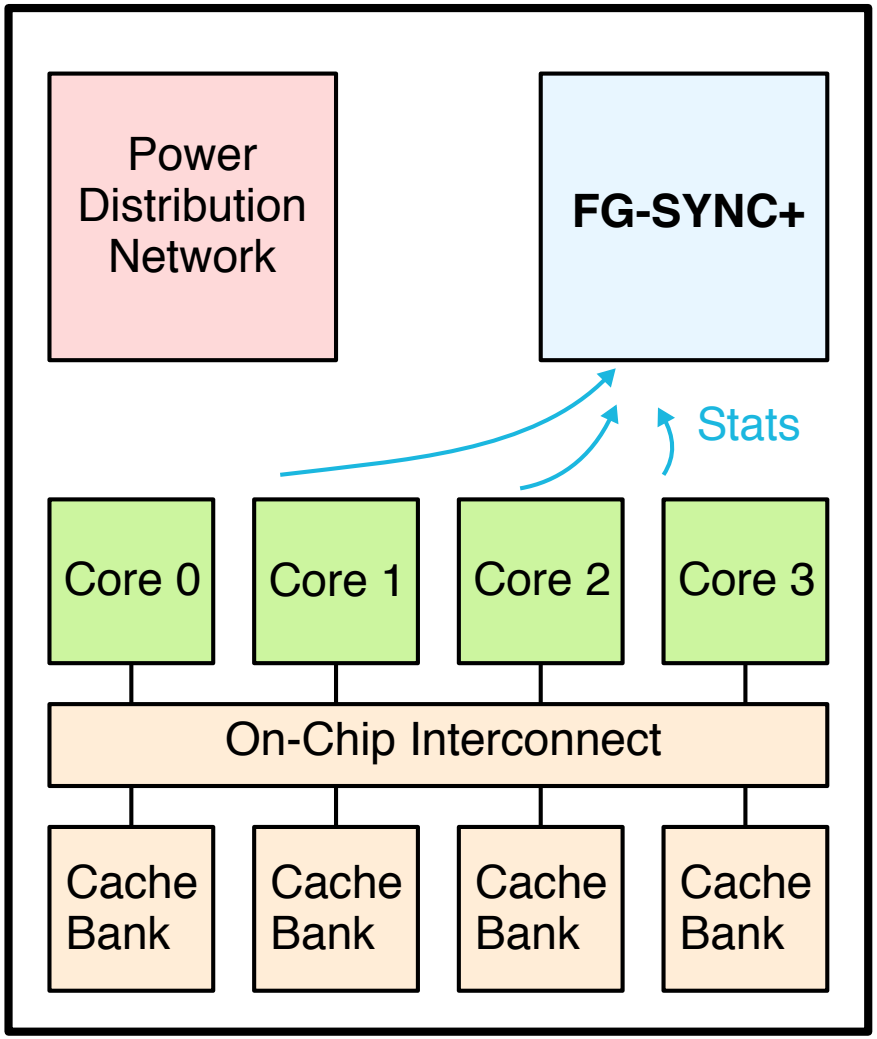
FGVS Architecture: FG-SYNC+

Use lightweight *software hints* and lookup tables derived offline to enable fast multi-level voltage configuration

FGVS Circuits: RPDN

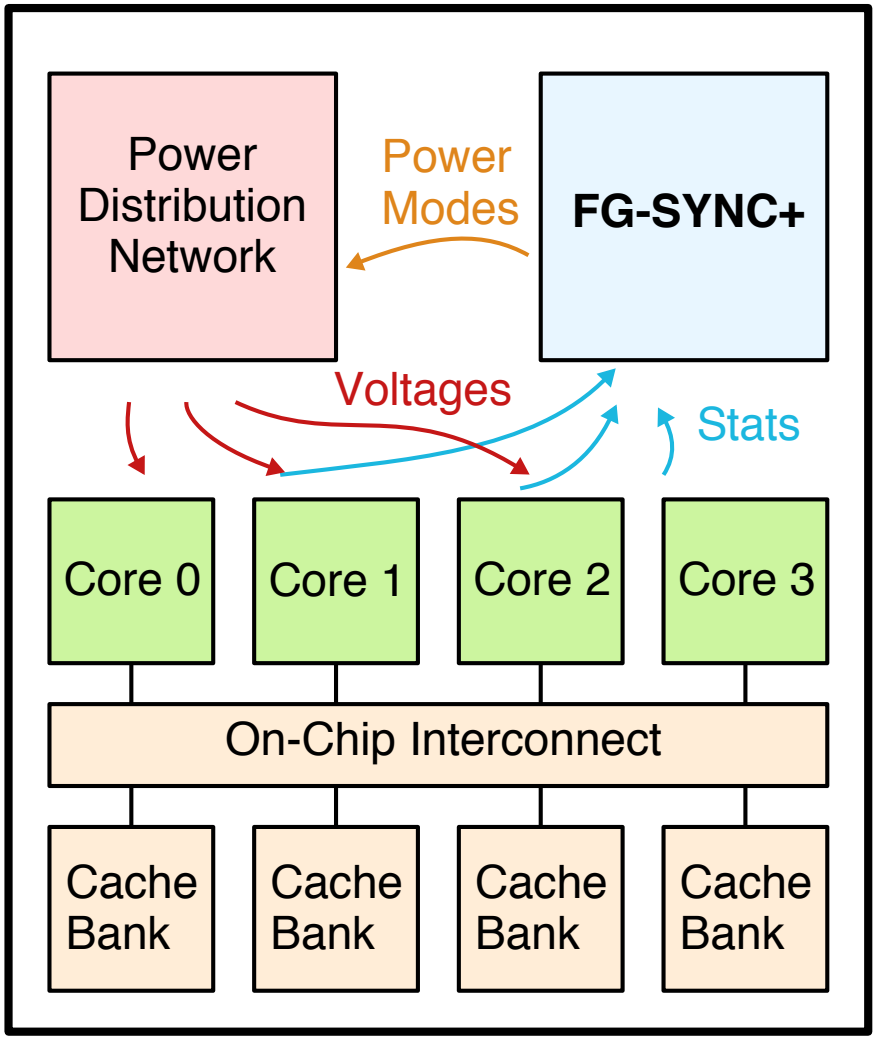
Enable sprinting cores to dynamically borrow energy storage from resting cores

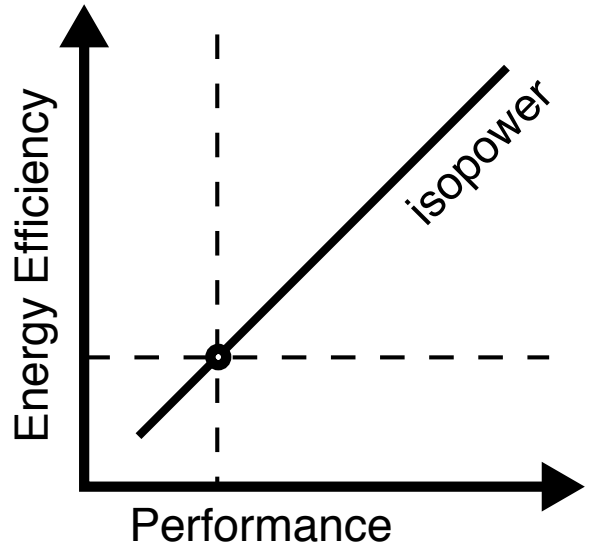
Fine-Grain Synchronization Controller (FG-SYNC+)

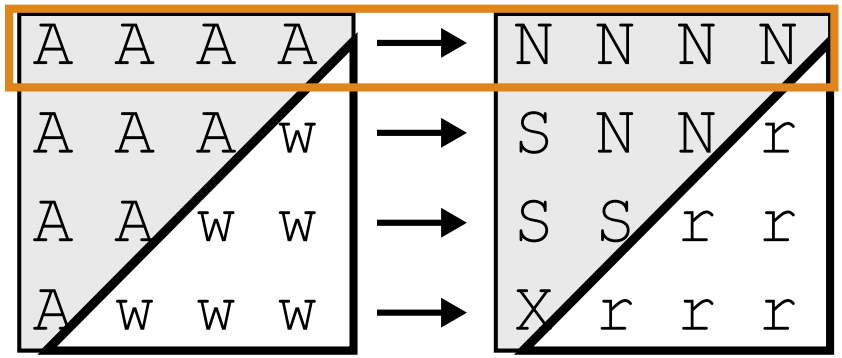



```
parallel_for(int i=0; i<N; n++){
   Before Start: Work Left Hint
   Loop Start: Activity Hint -- busy
   < loop body >
   Loop Ends: Activity Hint -- waiting
}
```

Fine-Grain Synchronization Controller (FG-SYNC+)



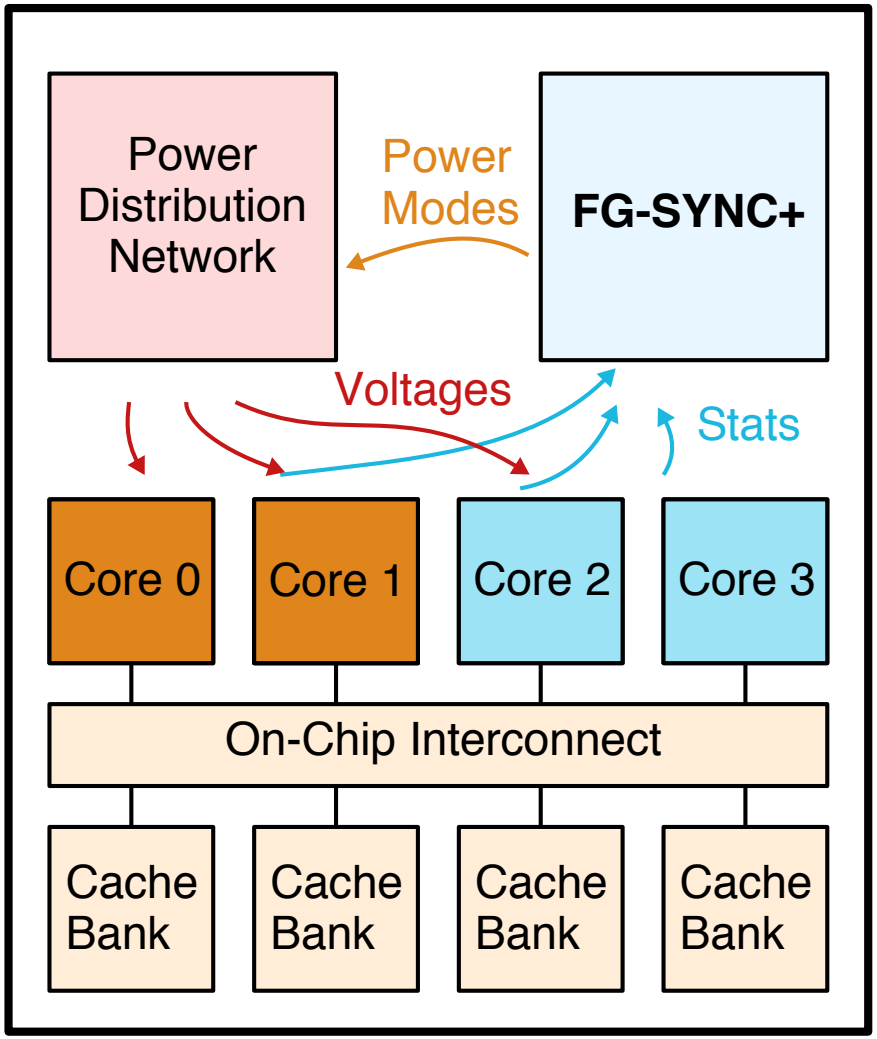


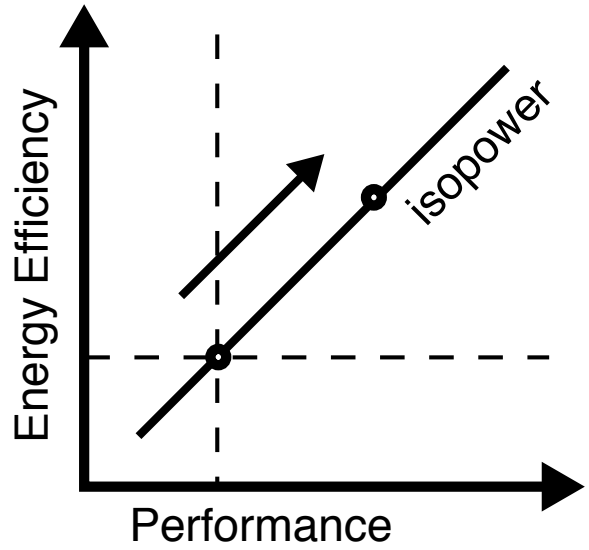


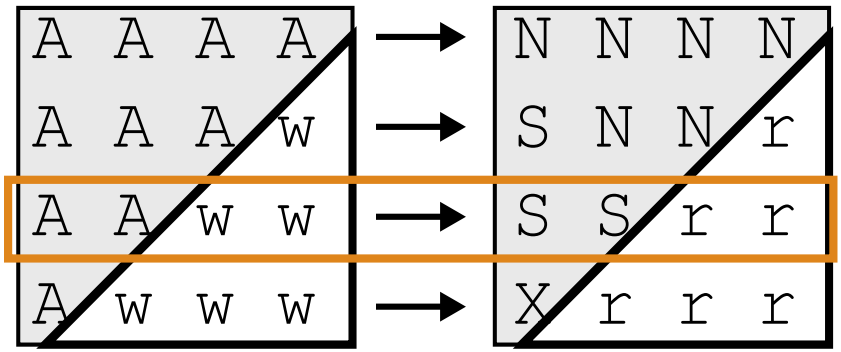
(**A**ctive **W**aiting)

(**N, r** Nominal, rest)
(**S, X** Sprint modes)

Fine-Grain Synchronization Controller (FG-SYNC+)







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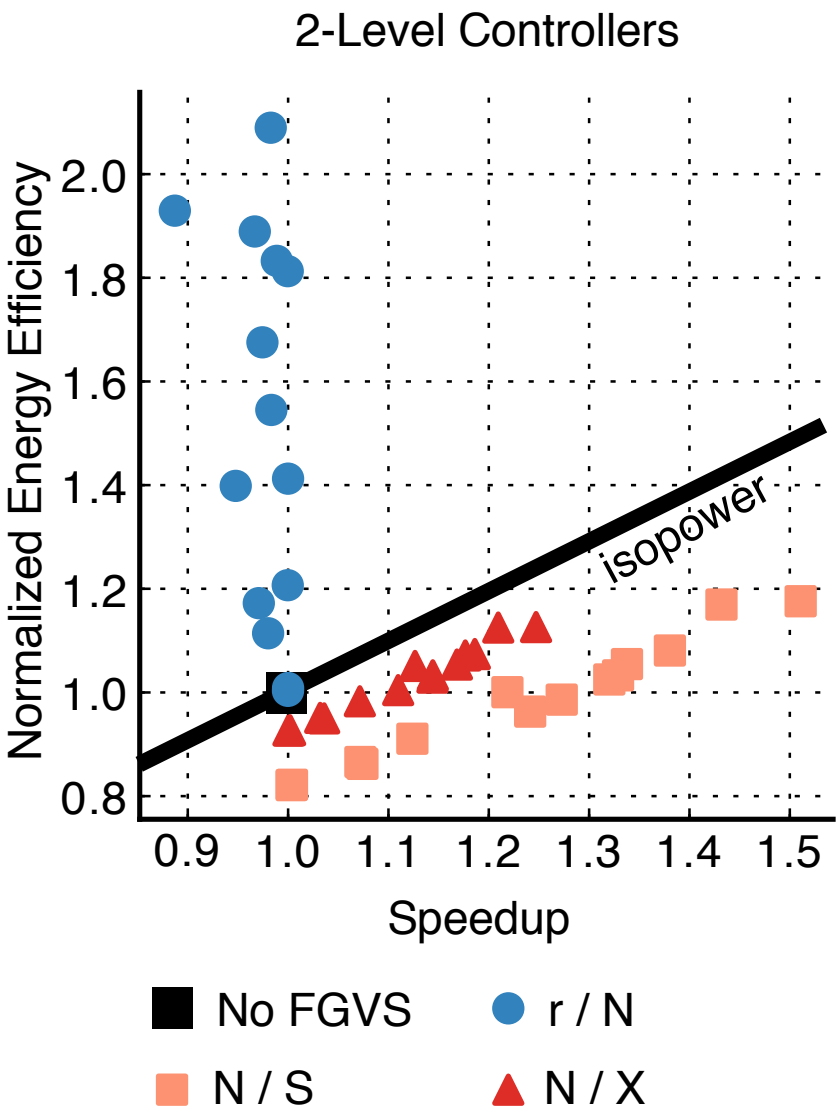
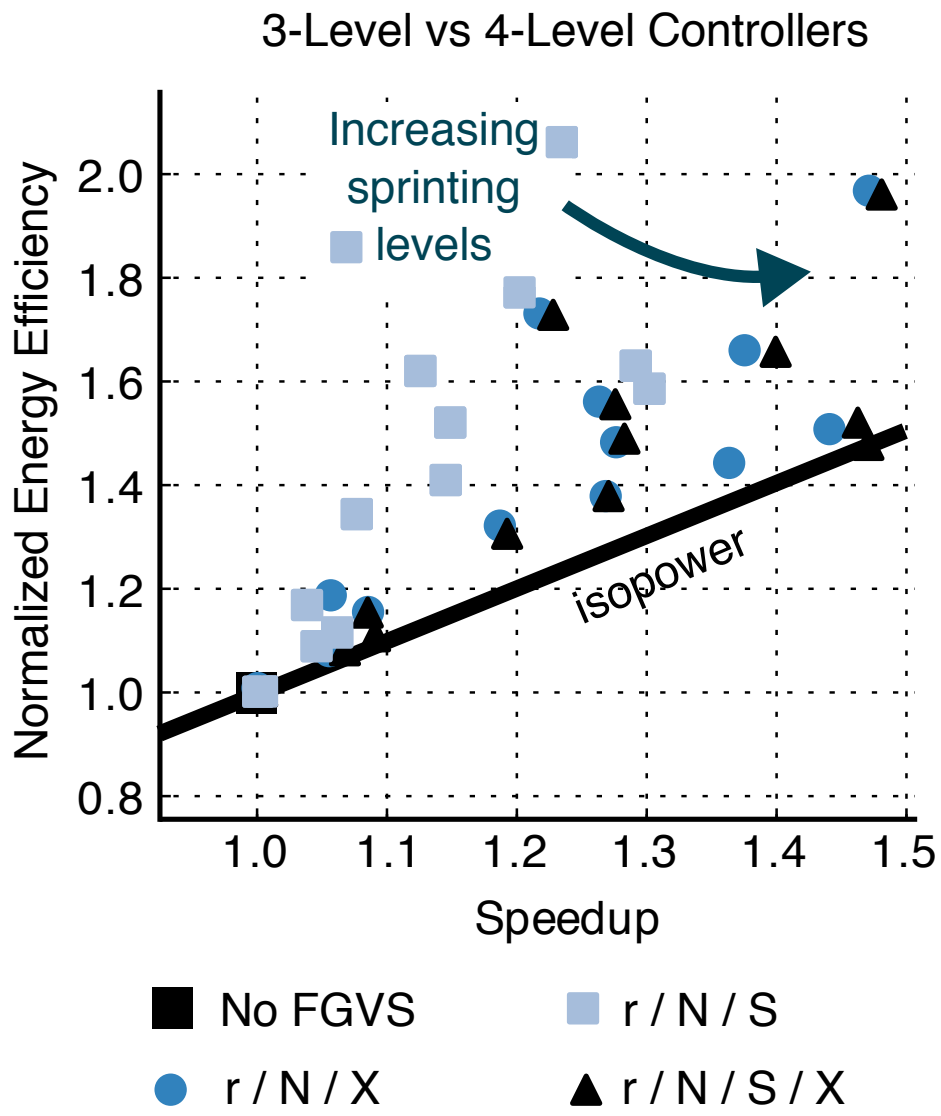
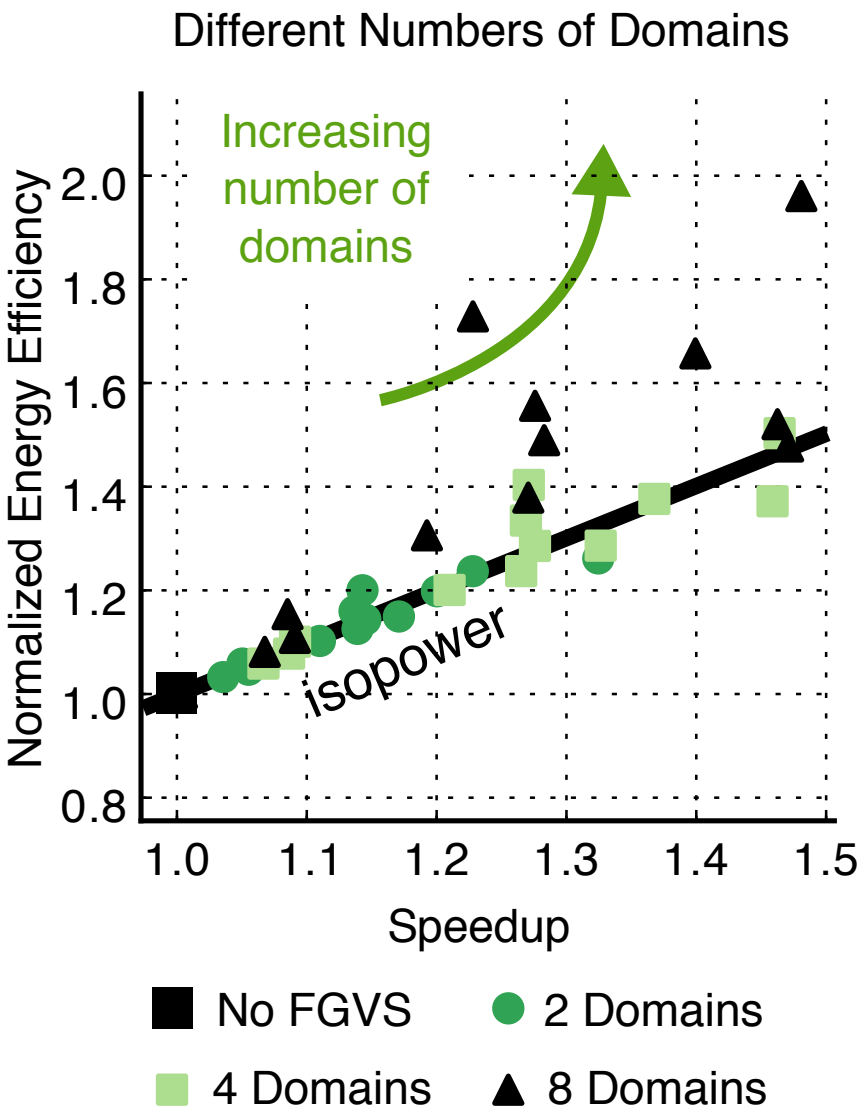
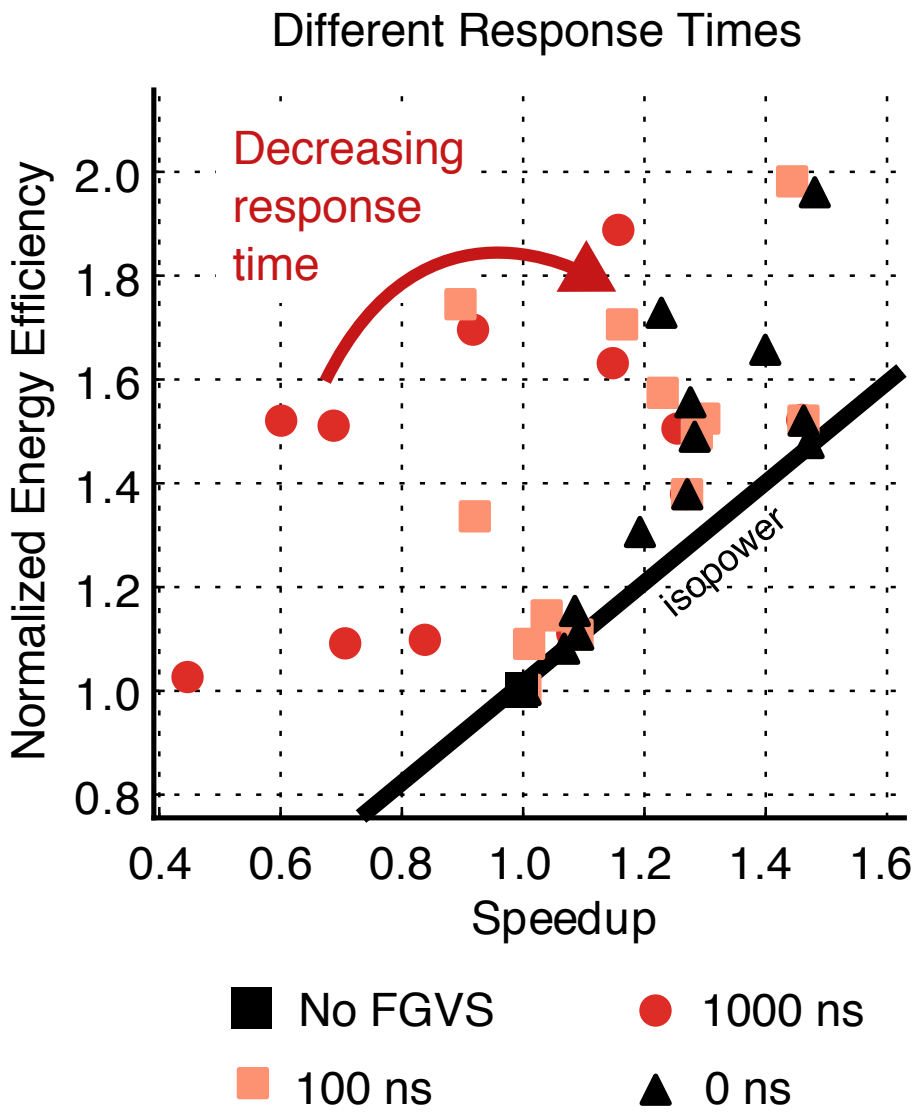
Non-Ideal FGVS: Different Levels



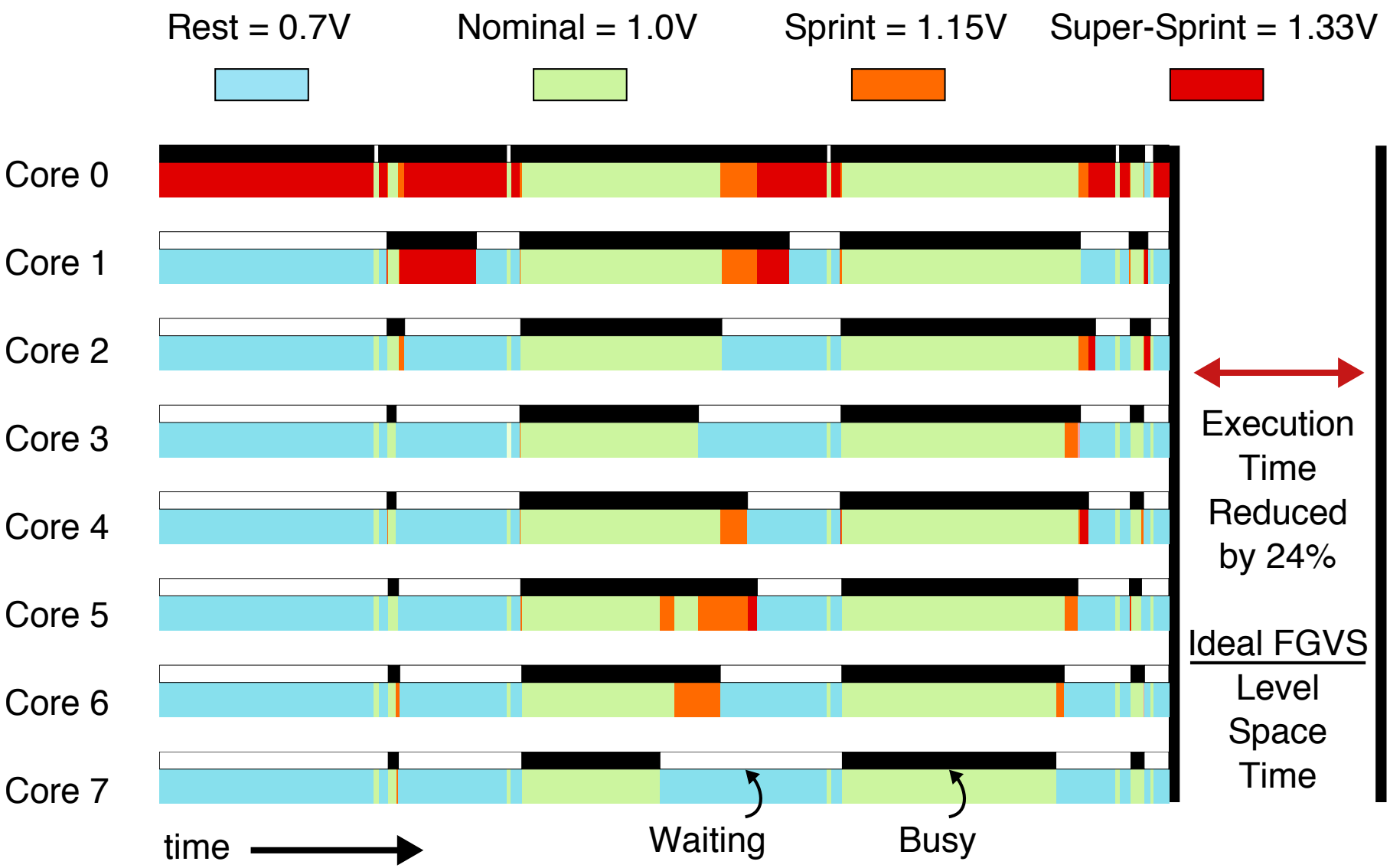


Non-Ideal FGVS: Space and Time

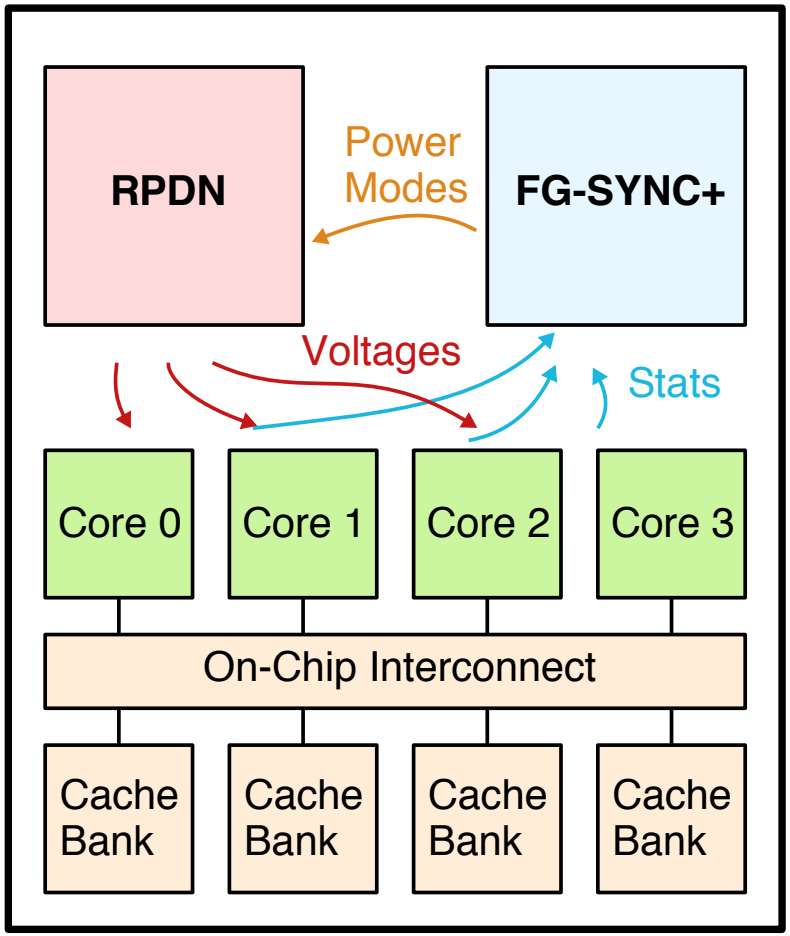




Skipping Details.. FG-SYNC+ Achieved Its Goal



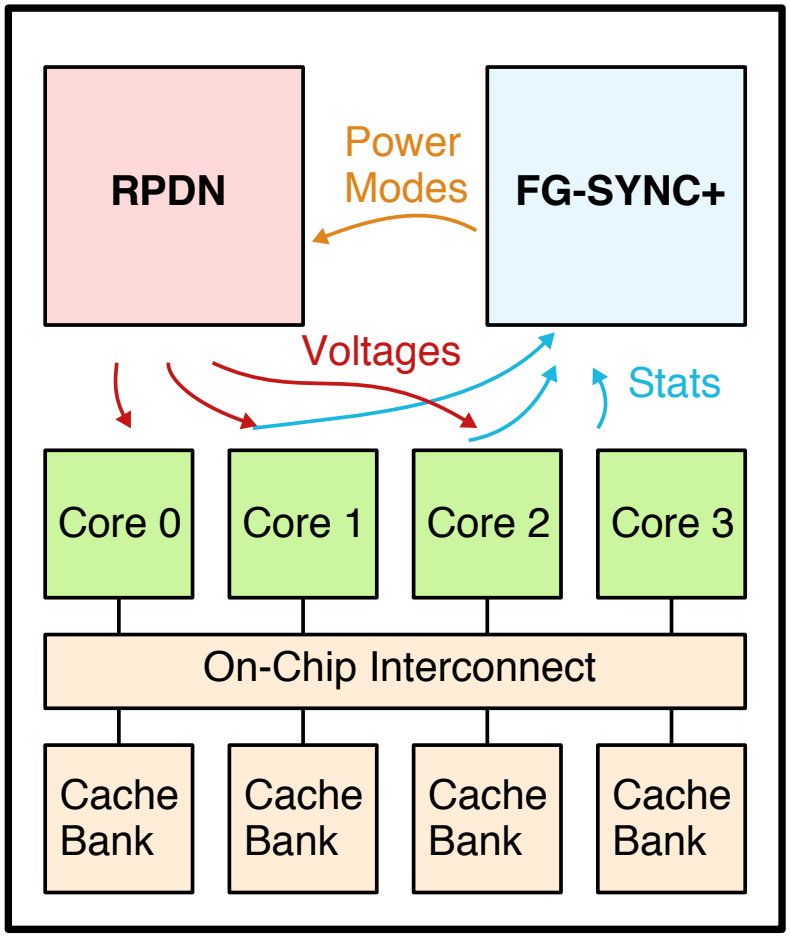
Enabling Realistic Fine-Grain Voltage Scaling



FGVS Architecture: FG-SYNC+

Use lightweight *software hints* and lookup tables derived offline to enable fast multi-level voltage configuration

Enabling Realistic Fine-Grain Voltage Scaling



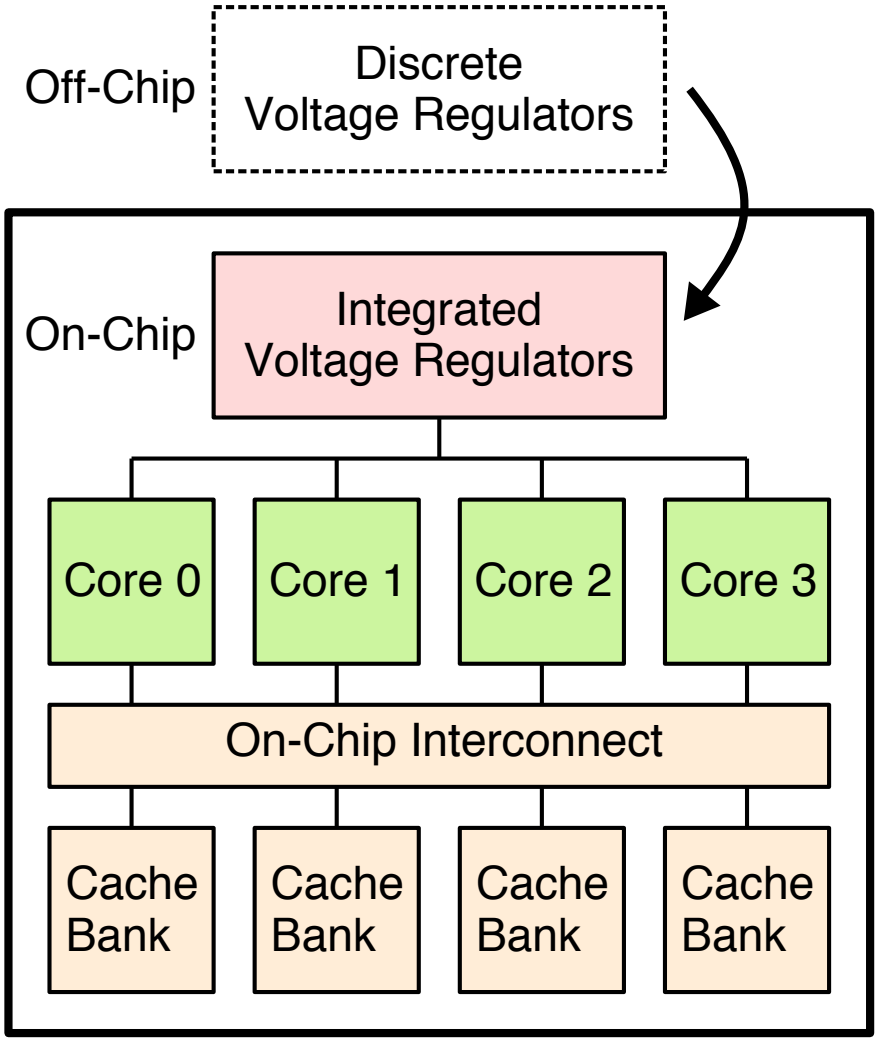
FGVS Architecture: FG-SYNC+

Use lightweight *software hints* and lookup tables derived offline to enable fast multi-level voltage configuration

FGVS Circuits: RPDN

Enable sprinting cores to dynamically borrow energy storage from resting cores

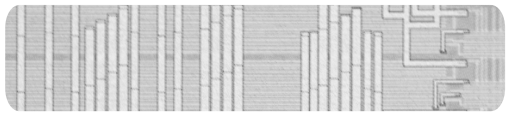
Key Challenge of Integrated Voltage Regulation



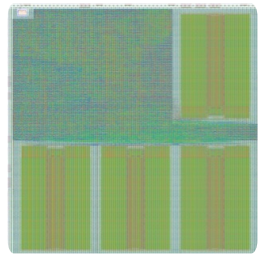
What's the Problem?

- Integrated VRs are BIG

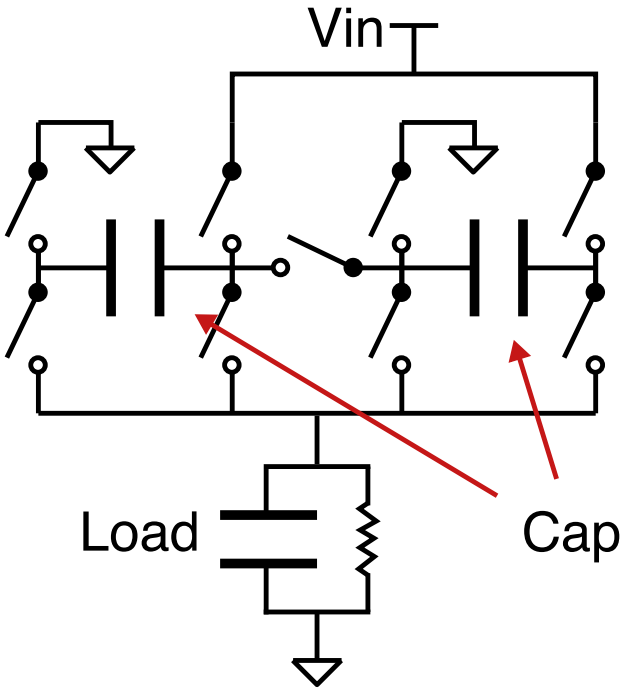
Technology-Normalized
Integrated Voltage Regulator

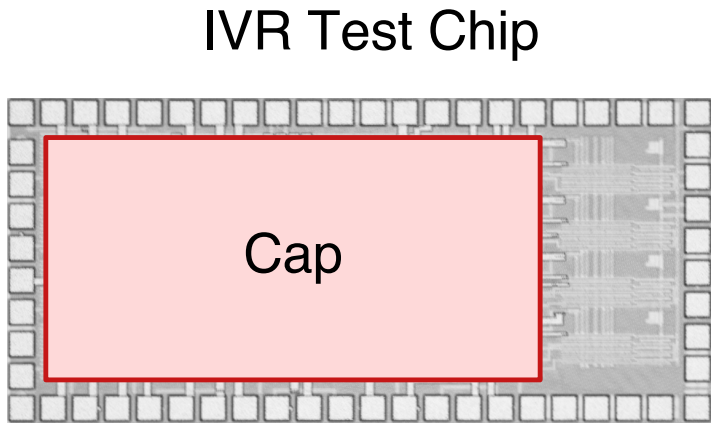


Technology-Normalized
Simple RISC Core

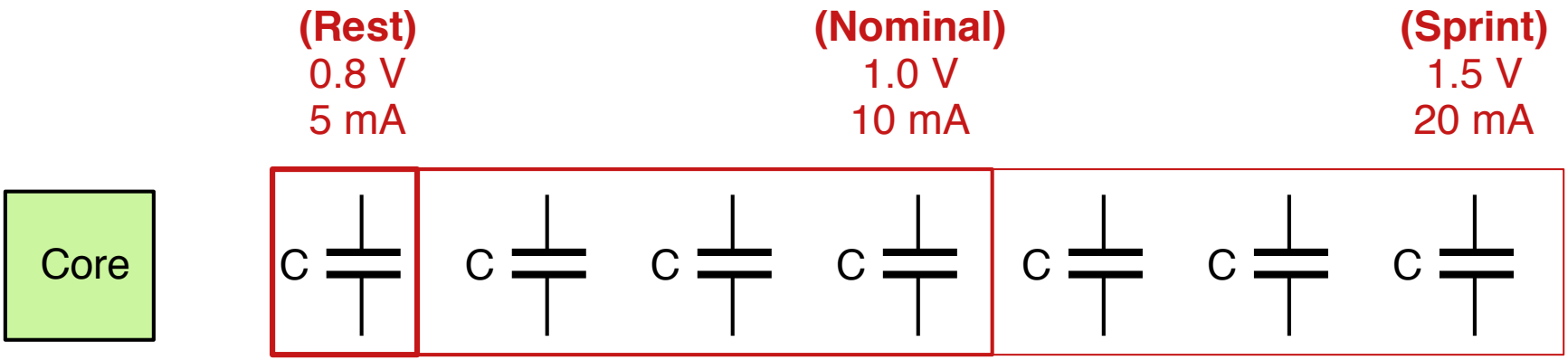


What's taking all that area?

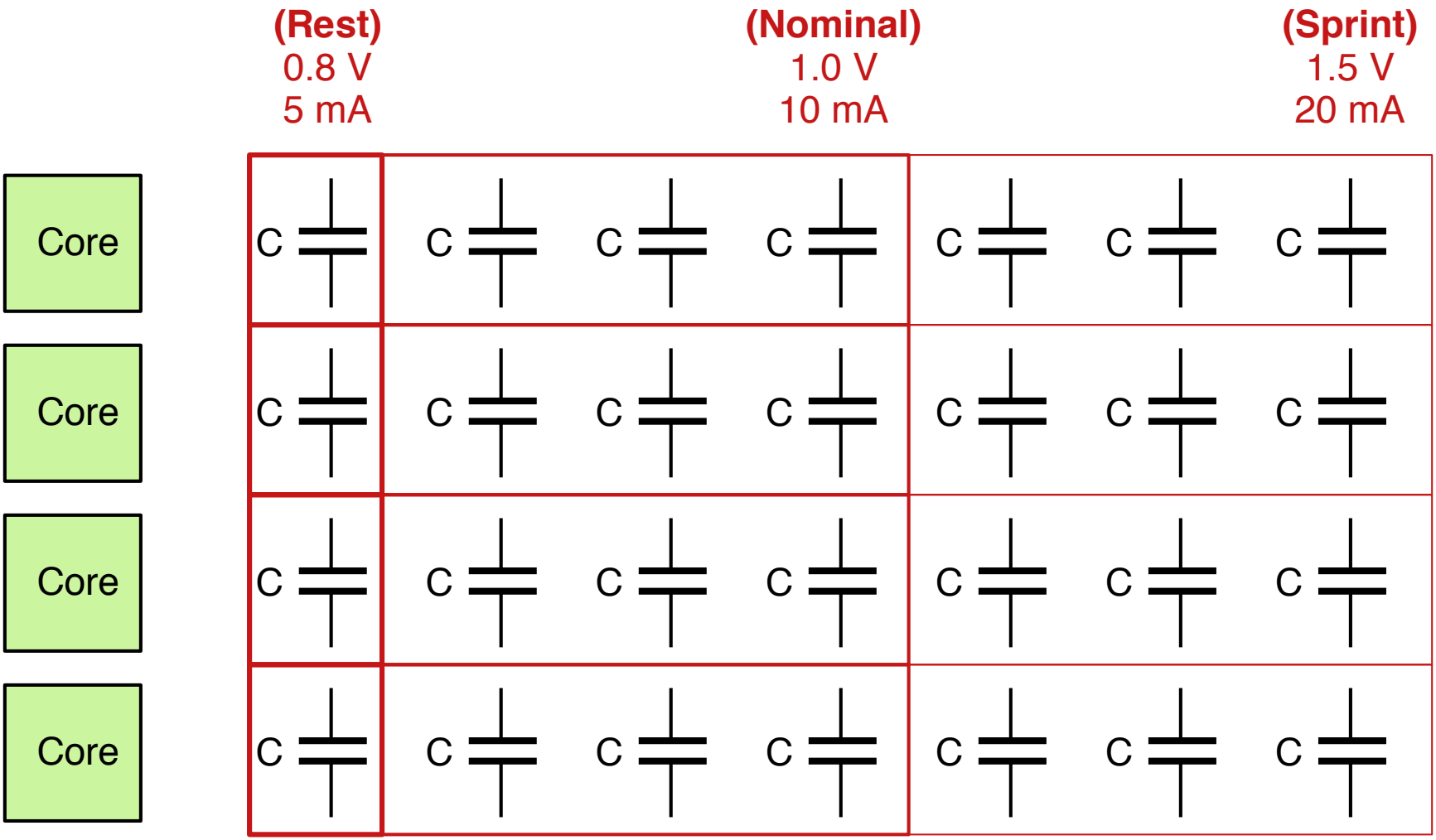




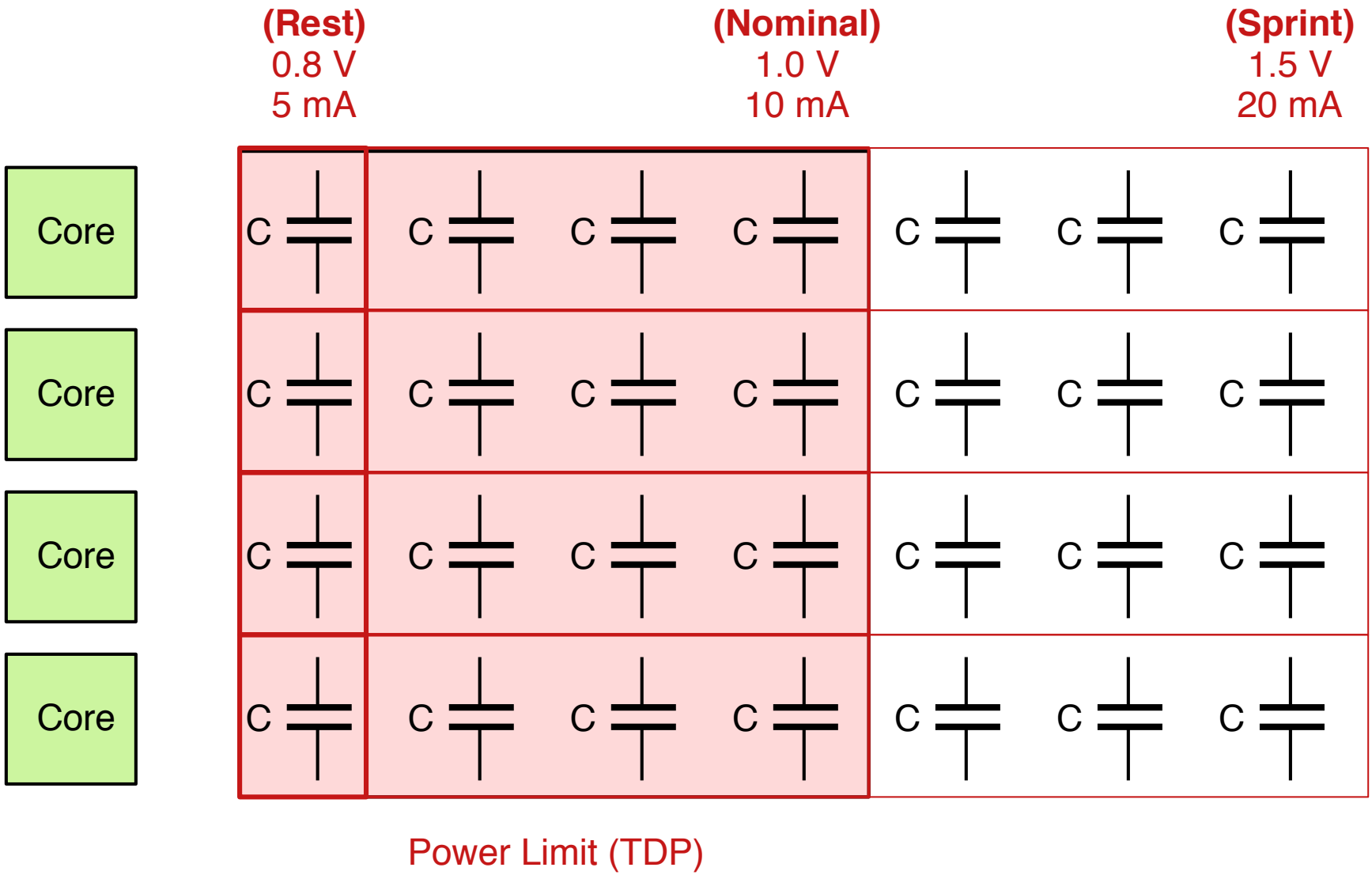
Key Architecture-Level Intuition



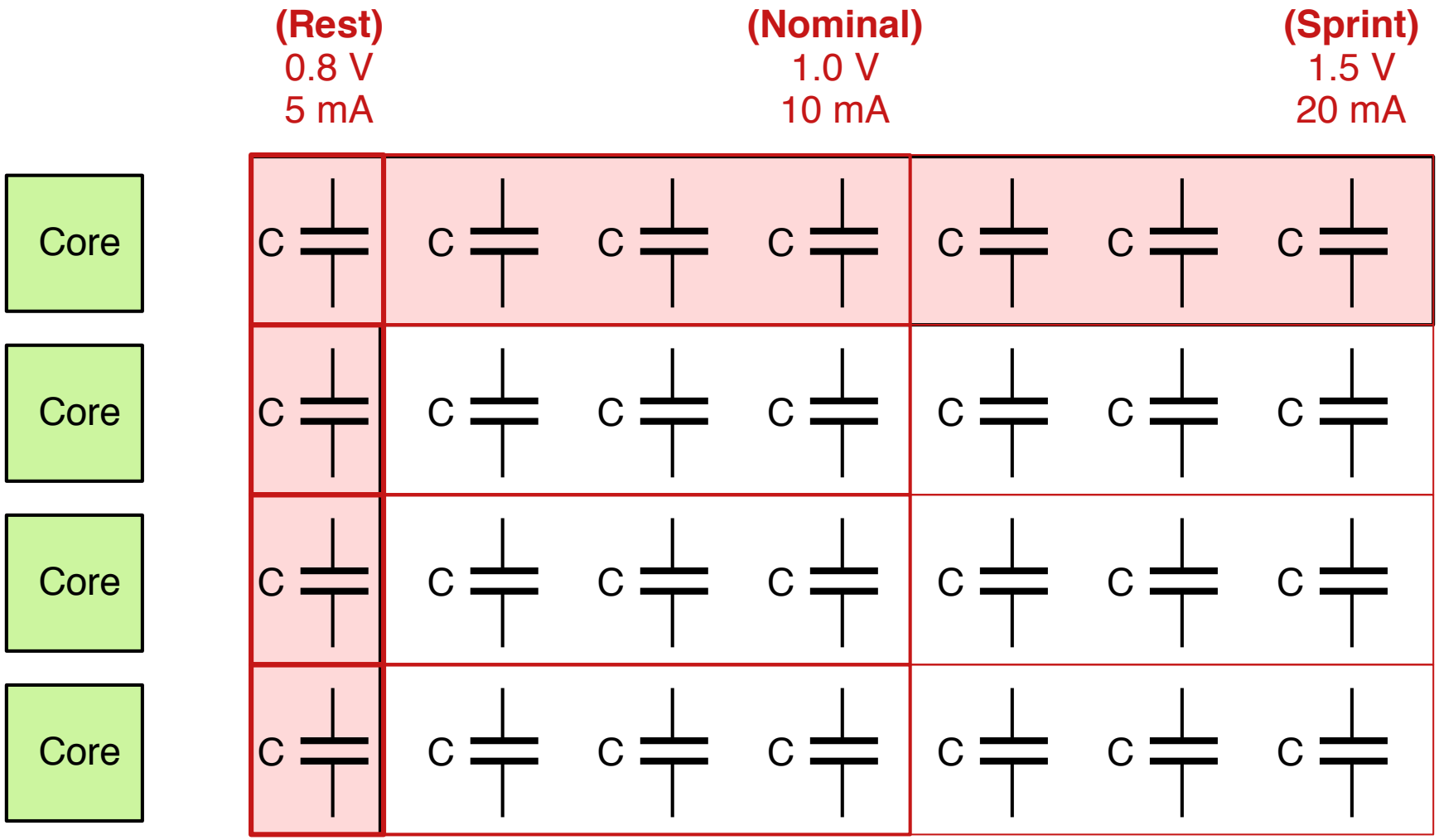
Key Architecture-Level Intuition



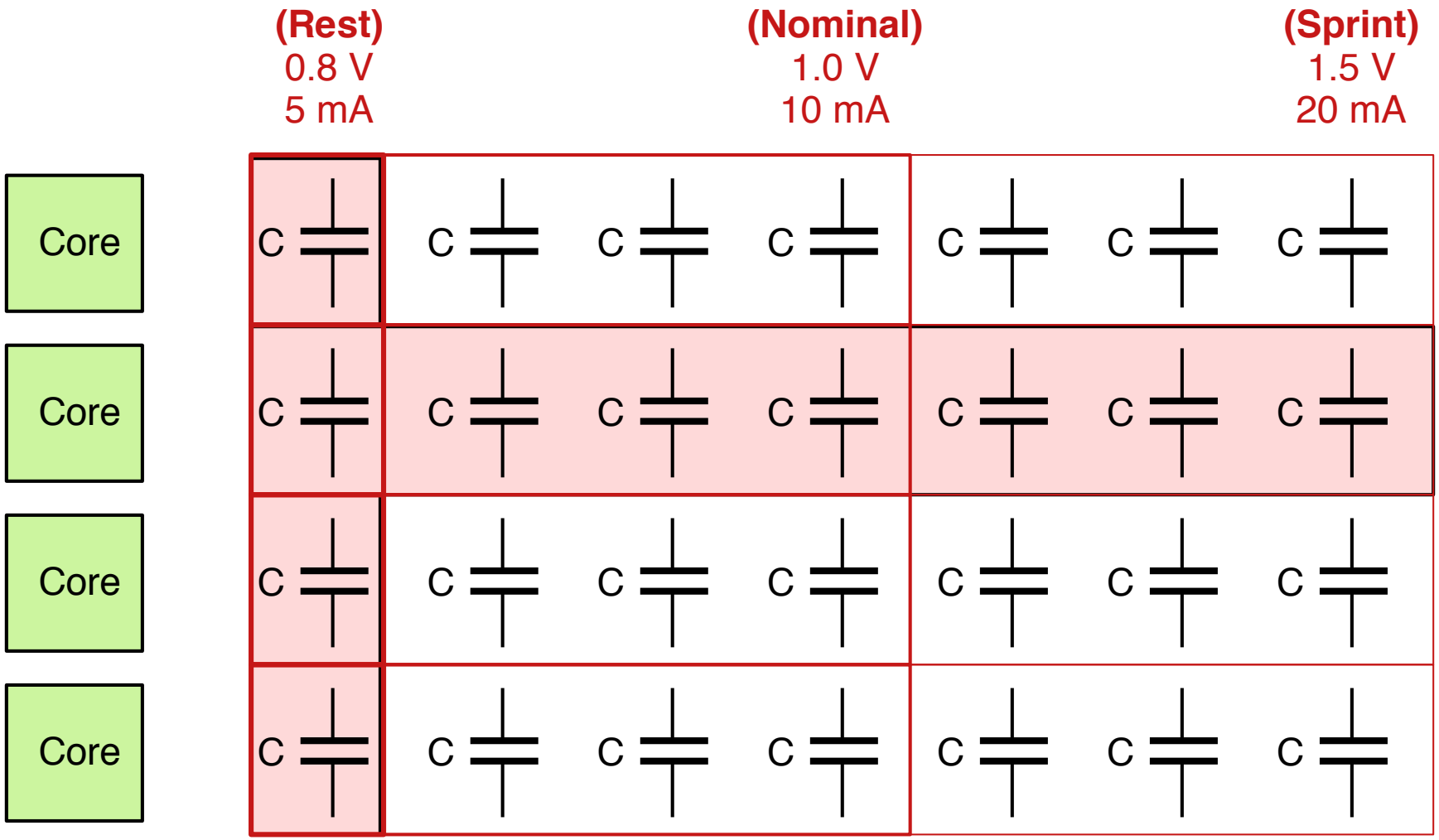
Key Architecture-Level Intuition



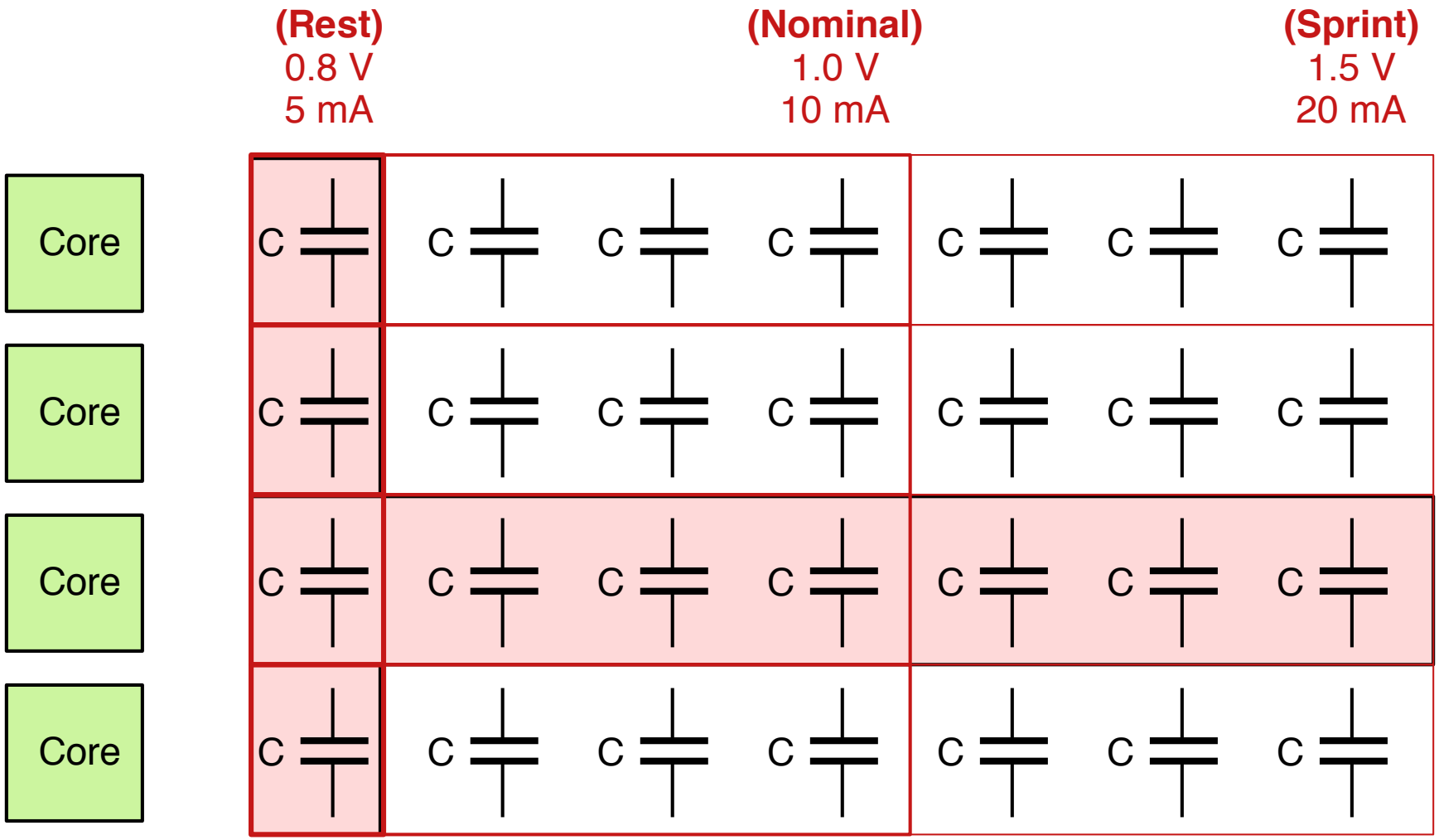
Key Architecture-Level Intuition



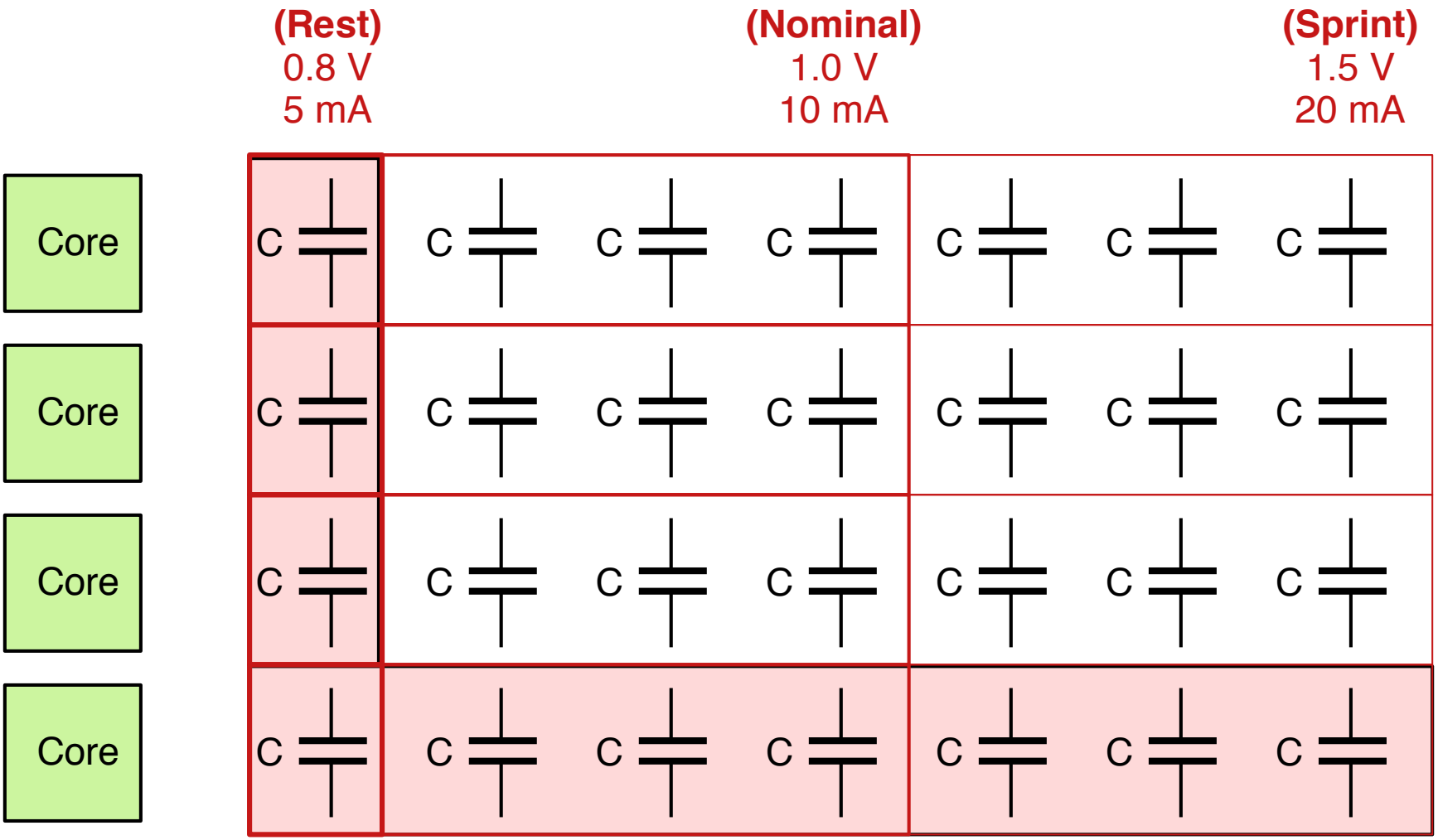
Key Architecture-Level Intuition



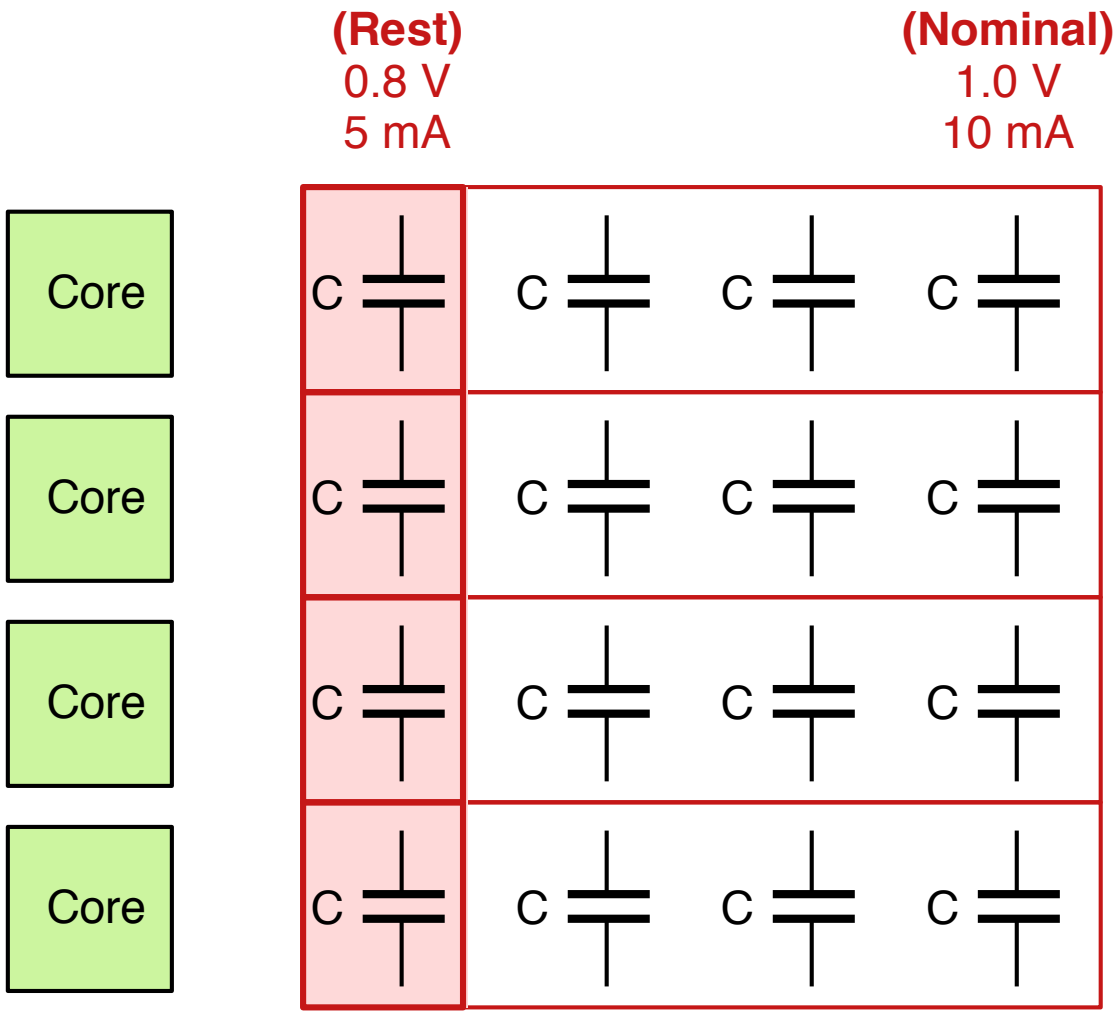
Key Architecture-Level Intuition



Key Architecture-Level Intuition



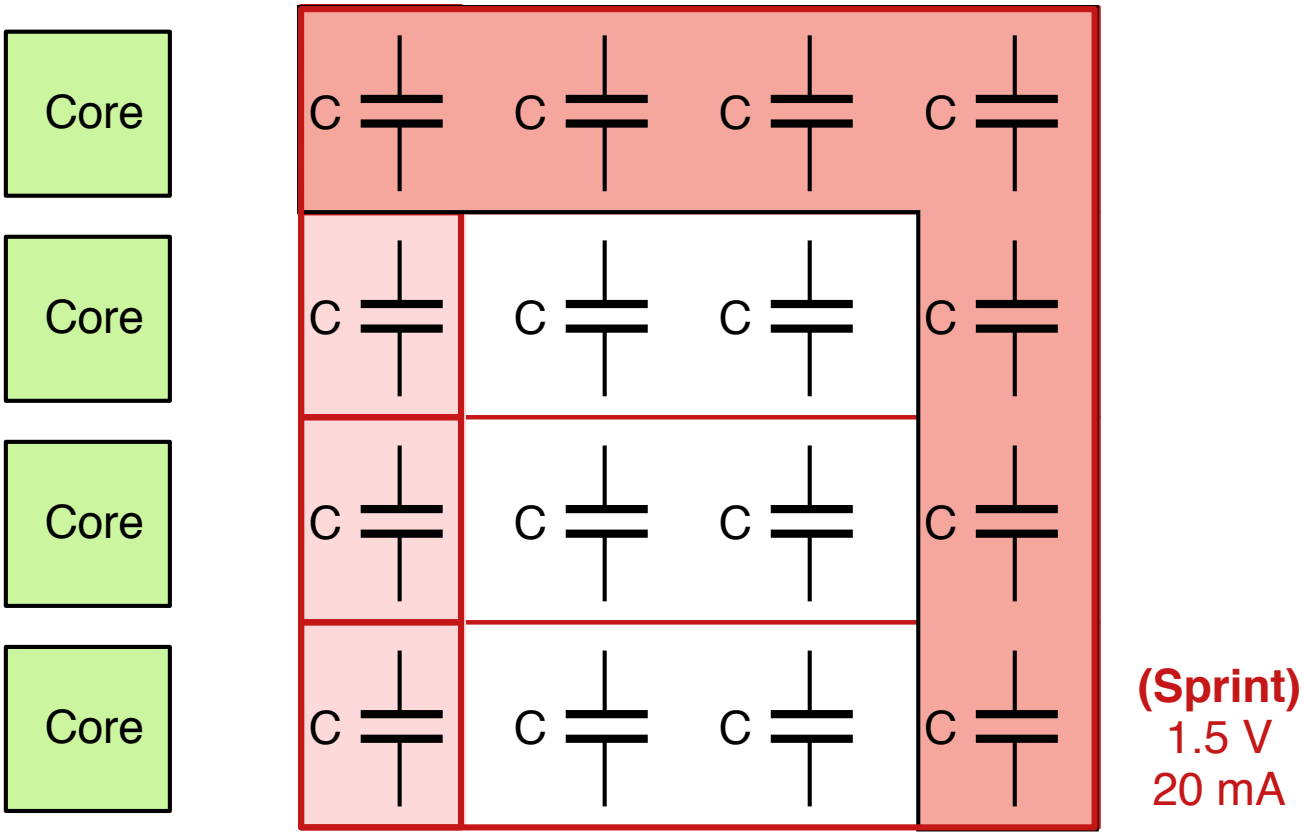
Key Architecture-Level Intuition



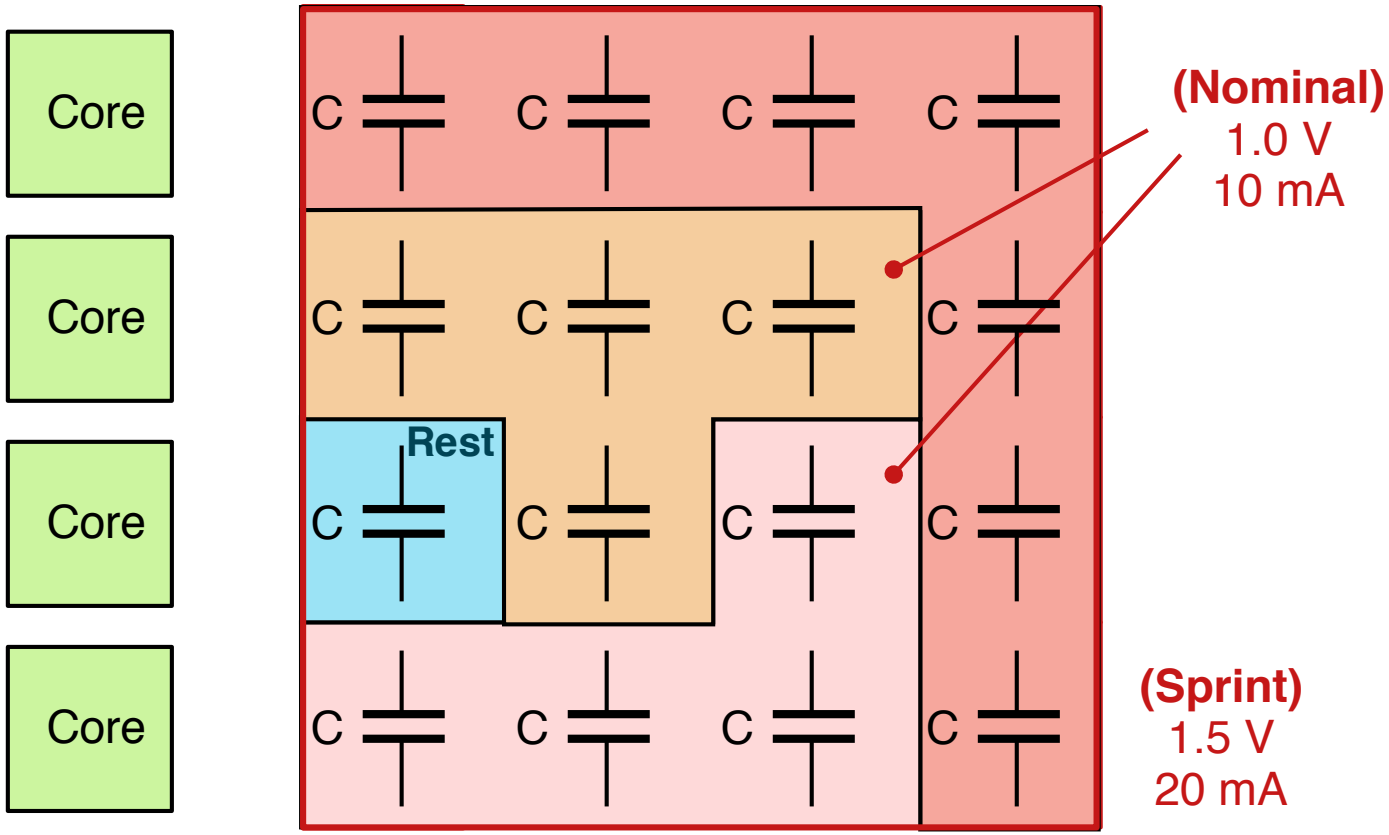
Key Goal

Reduce area without impacting performance and energy efficiency

Key Architecture-Level Intuition

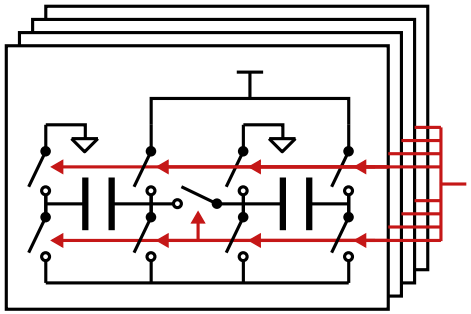


Key Architecture-Level Intuition

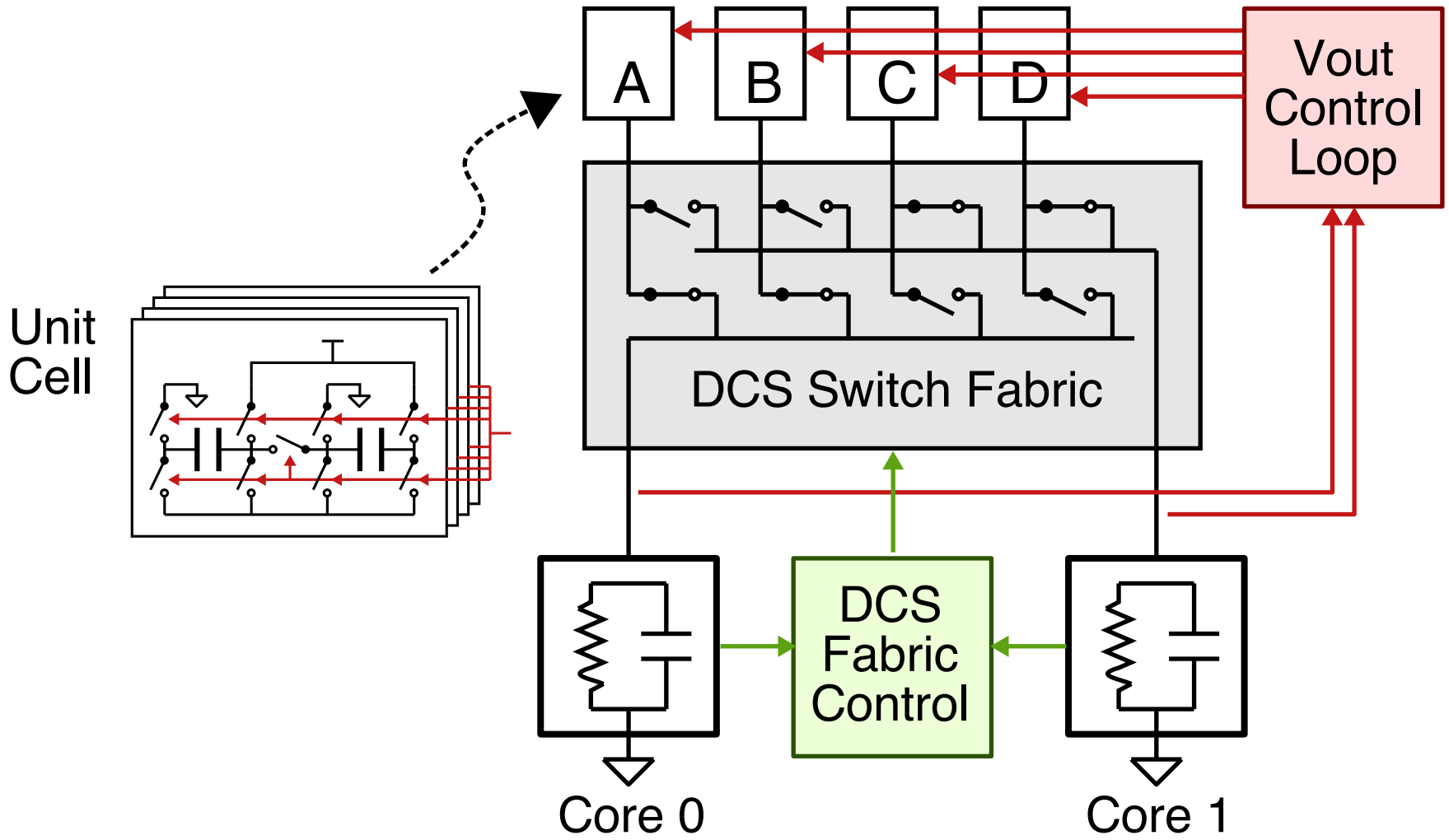


Dynamic Capacitance Sharing

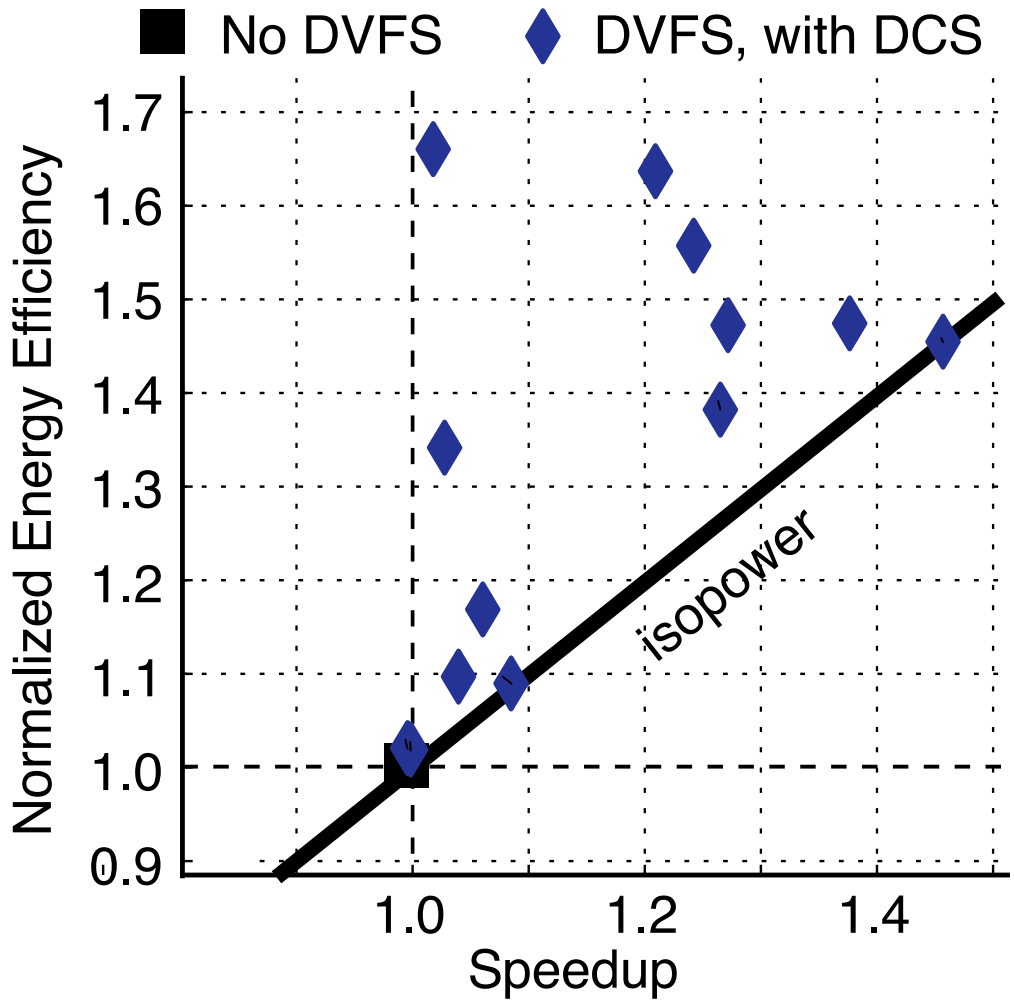
Unit Cell



Dynamic Capacitance Sharing



Evaluation

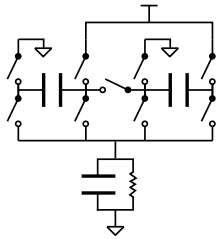


10-50% Speedup and 10-70% Energy Efficiency with Area-Optimized On-Chip VRs (40% area savings)

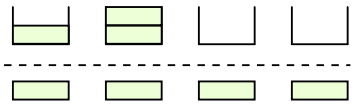
Benchmarks

- bfs
- bilateral
- dither
- kmeans
- mriq
- pbbs-dr
- pbbs-knn
- pbbs-mm
- rsort
- splash2-fft
- splash2-lu
- strsearch
- viterbi

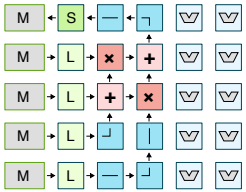
Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry



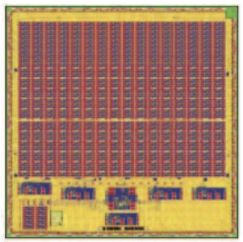
Exploiting Fine-Grain Asymmetry with
On-Chip Voltage Regulation - **MICRO'14**, IEEE TCAS I'18



Exploiting Fine-Grain Asymmetry in
Task-Based Parallel Runtimes - **ISCA'16**, MICRO'17, RISCV'18



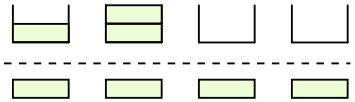
Exploiting Fine-Grain Asymmetry in
Coarse-Grain Reconfigurable Arrays - **Unpublished**



Exploiting Fine-Grain Asymmetry with
Silicon Prototyping - **IEEE MICRO'18**, DAC'18, Hotchips'17

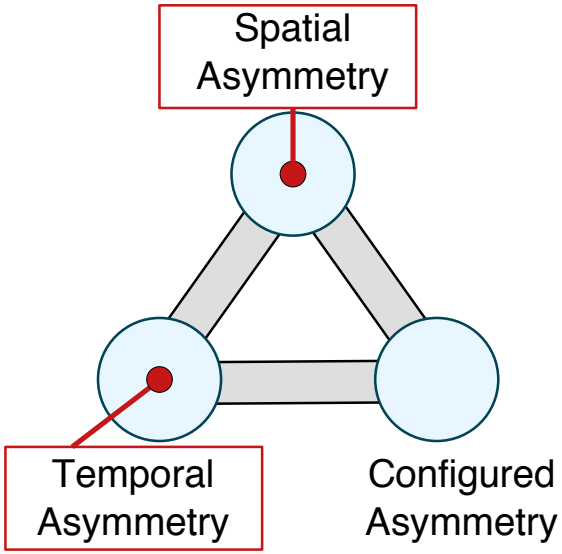
Conclusion

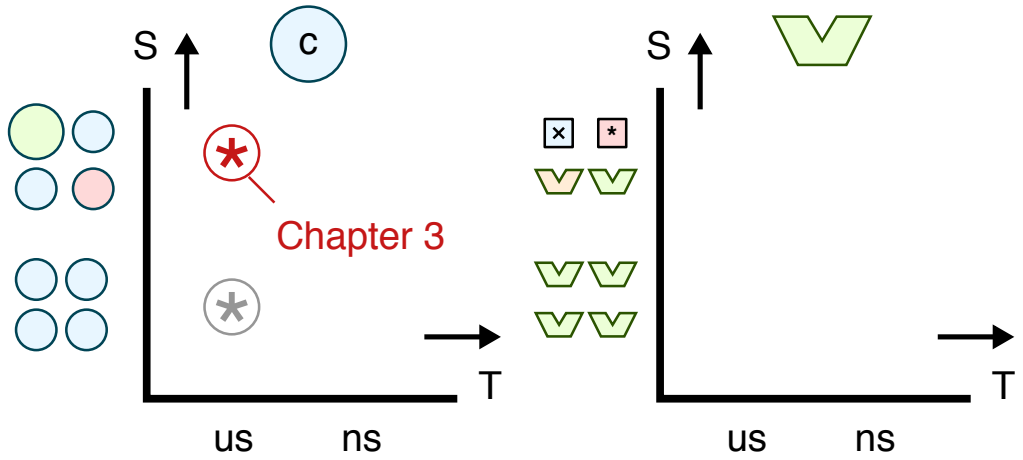
Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry



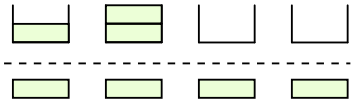
Exploiting Fine-Grain Asymmetry in

Task-Based Parallel Runtimes - ISCA'16, MICRO'17, RISCV'18



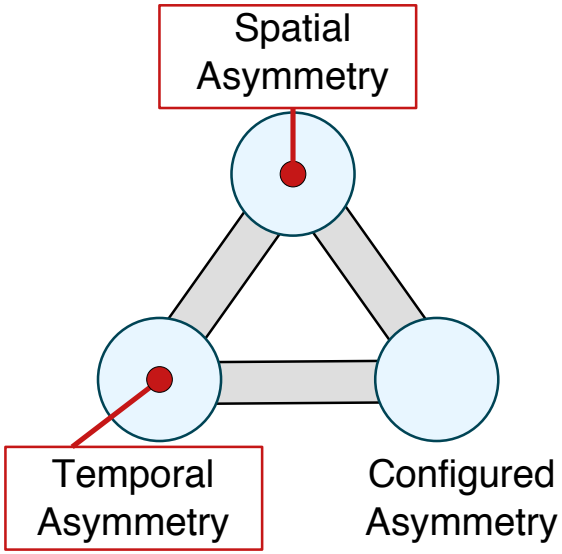


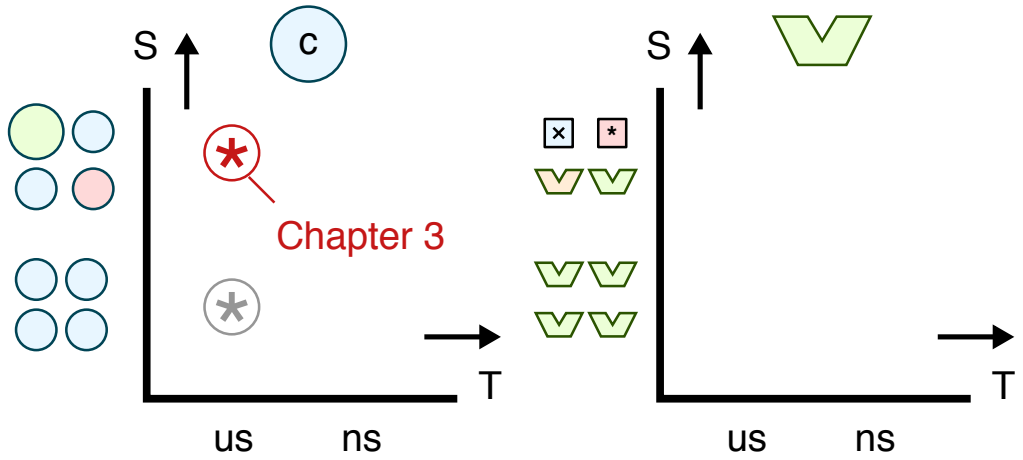
Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry



Exploiting Fine-Grain Asymmetry in

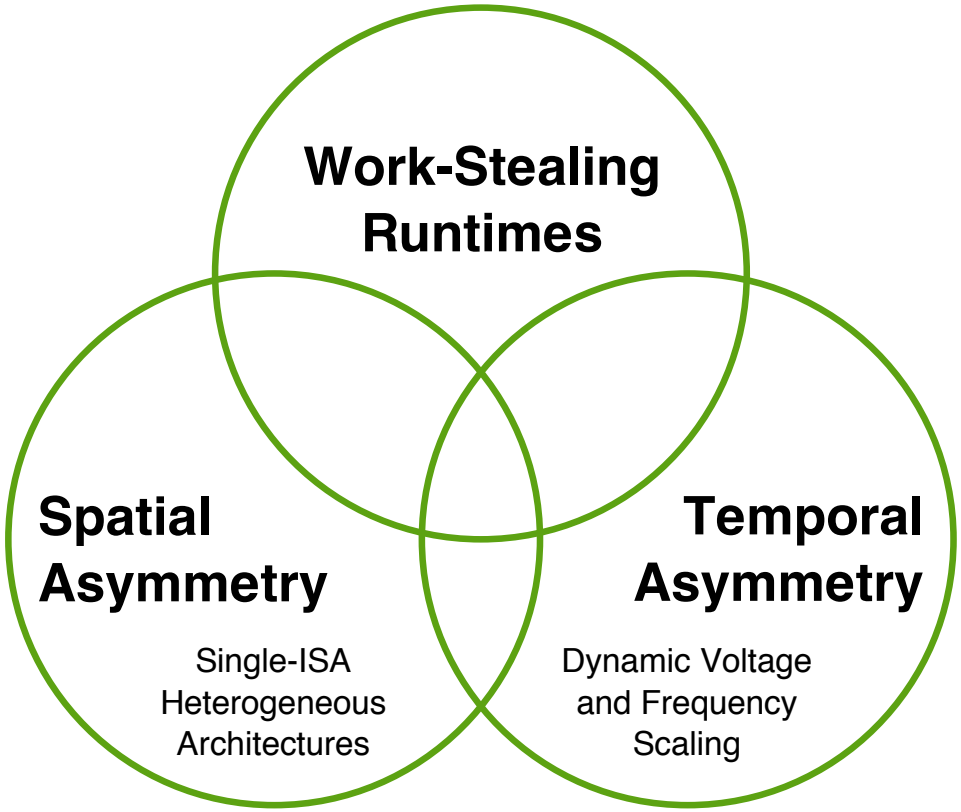
Task-Based Parallel Runtimes - ISCA'16, MICRO'17, RISCV'18





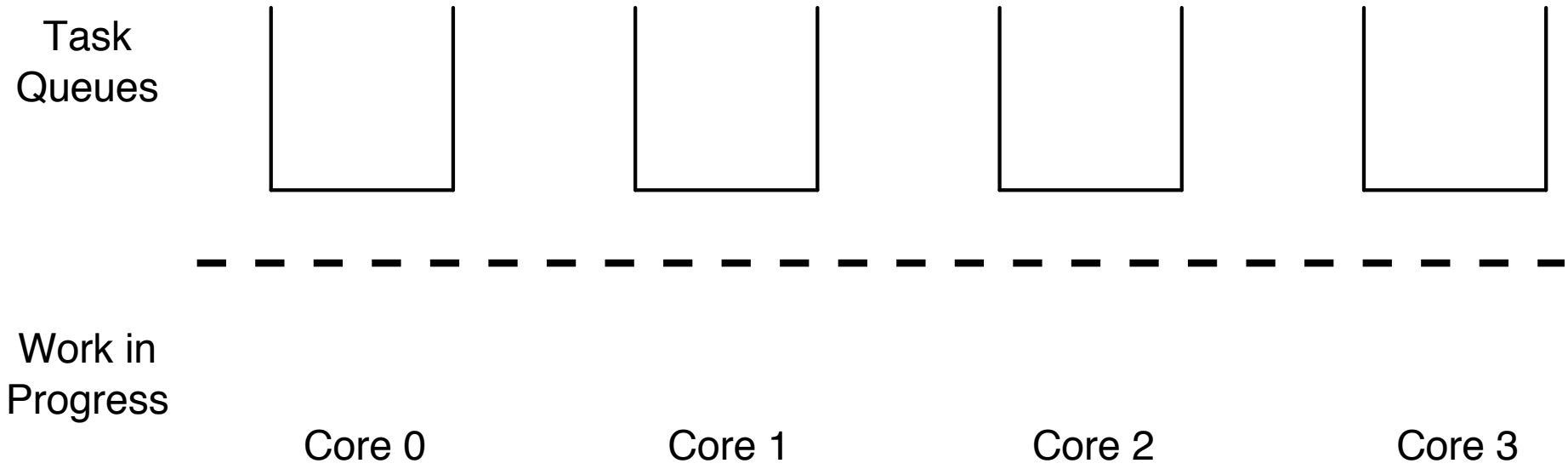
Research Question – Can we leverage fine-grain power control to enable more efficient task-based parallel runtimes executing on heterogeneous systems?

Focusing on Task-Based Parallel Runtimes

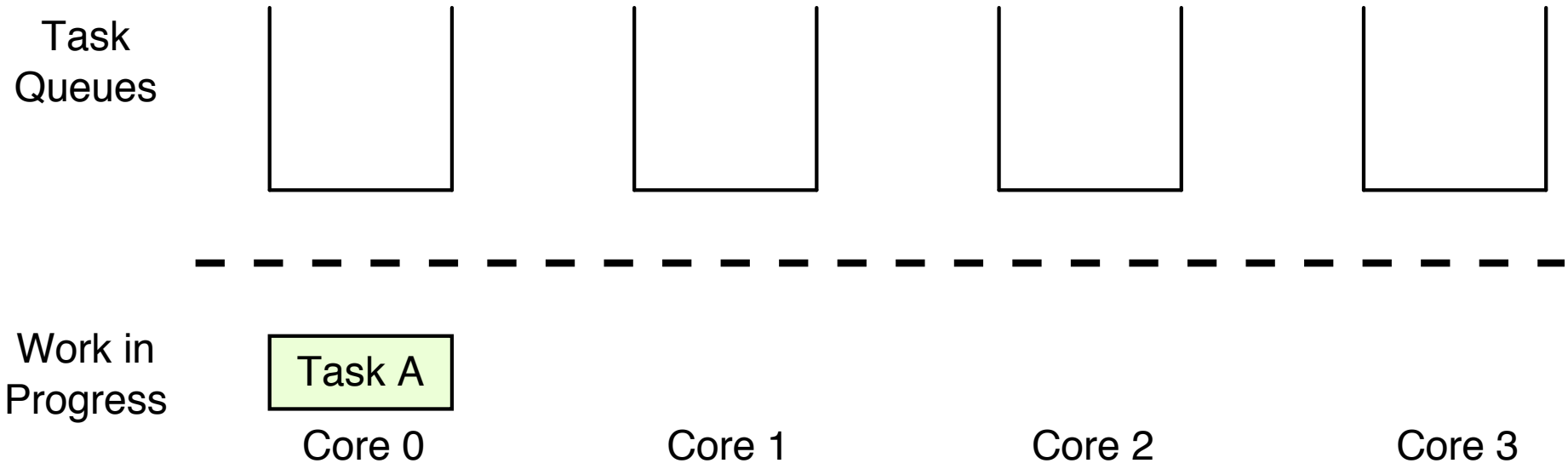


Research Question – Can we leverage fine-grain power control to enable more efficient task-based parallel runtimes executing on heterogeneous systems?

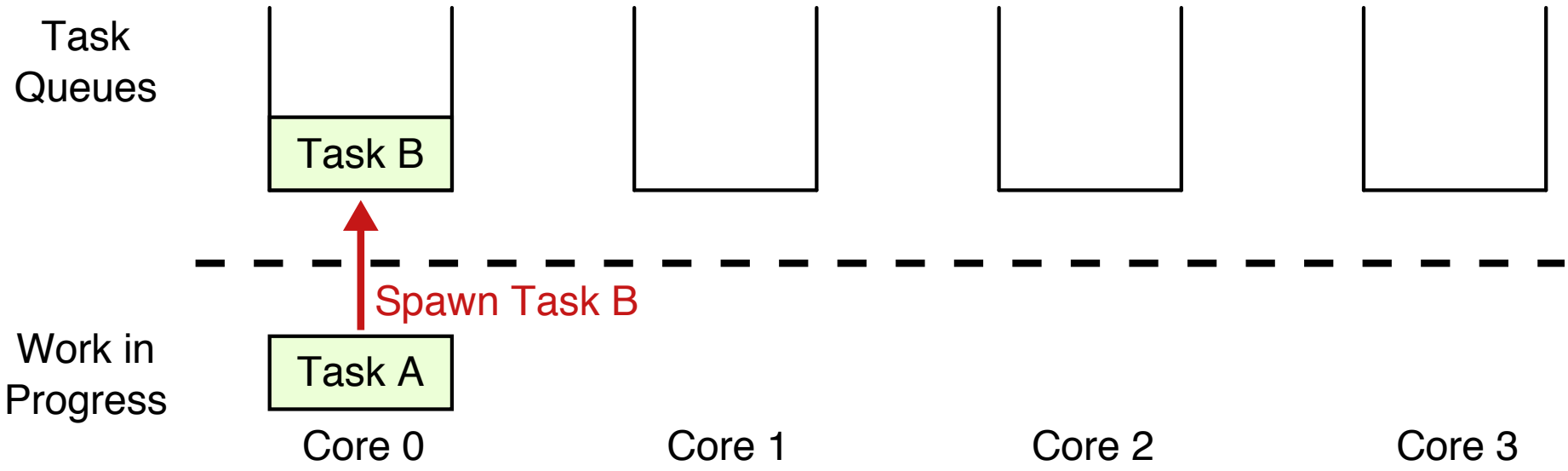
Work-Stealing Runtimes



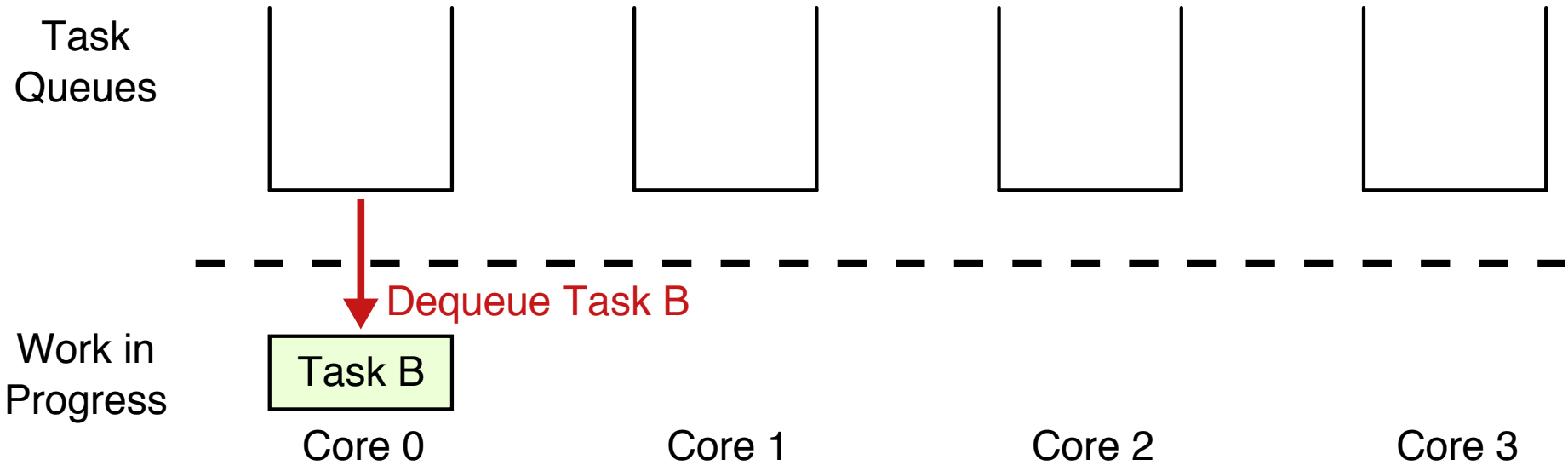
Work-Stealing Runtimes



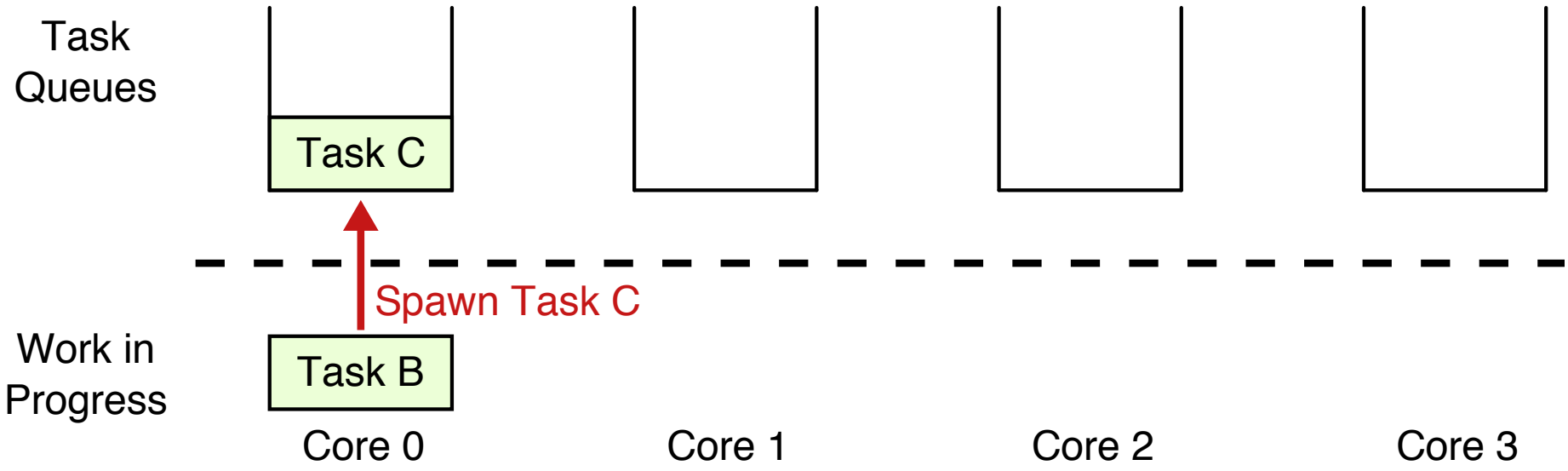
Work-Stealing Runtimes



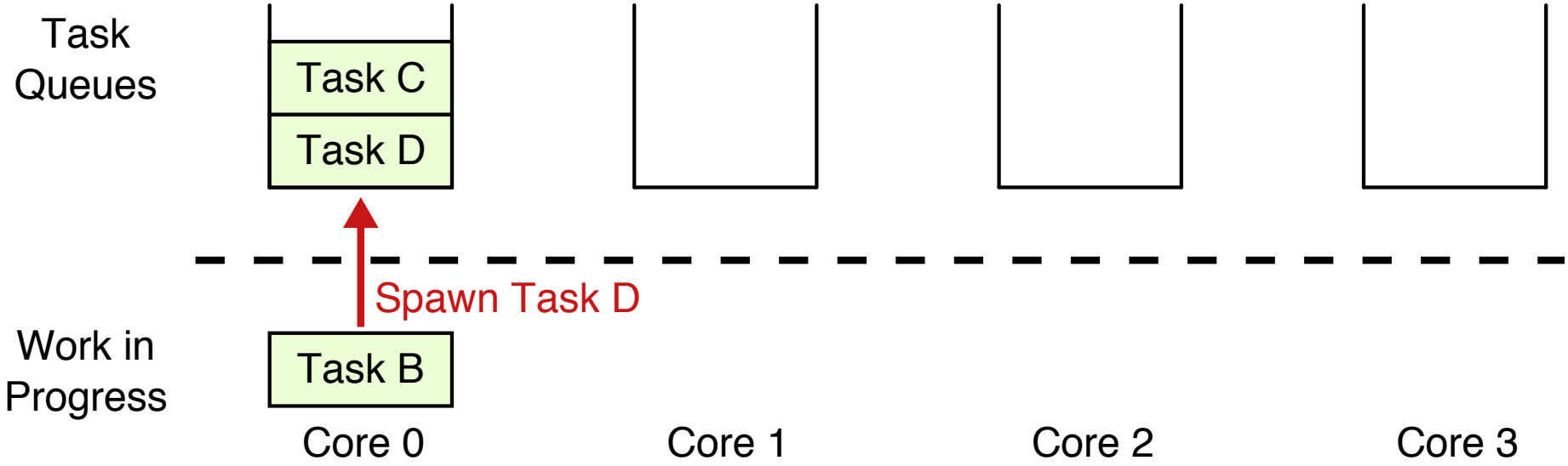
Work-Stealing Runtimes



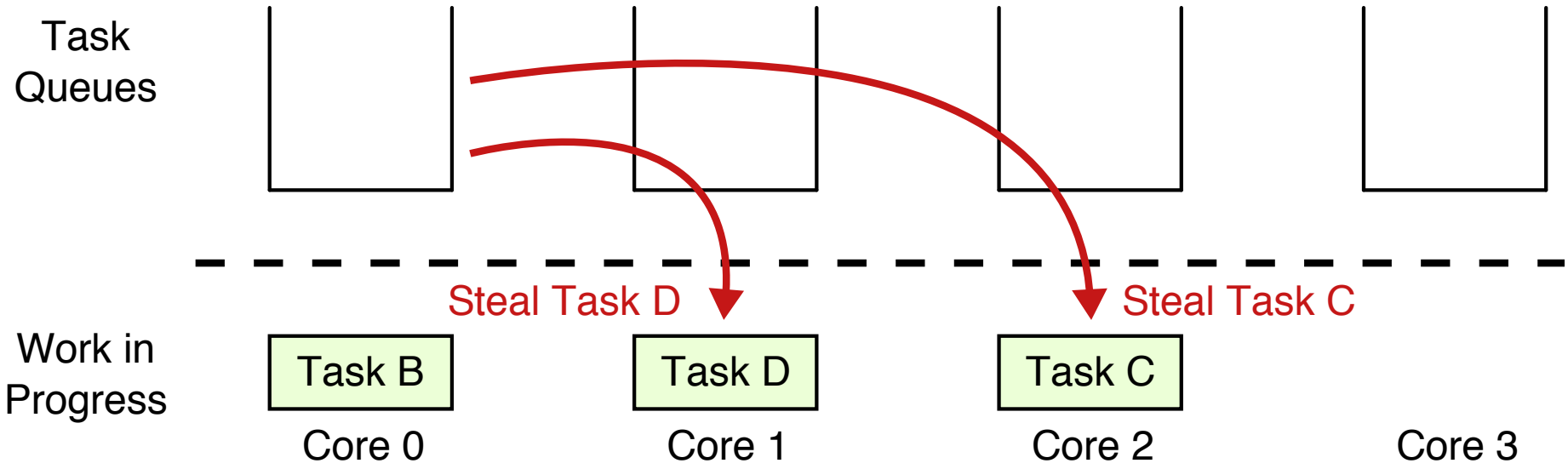
Work-Stealing Runtimes



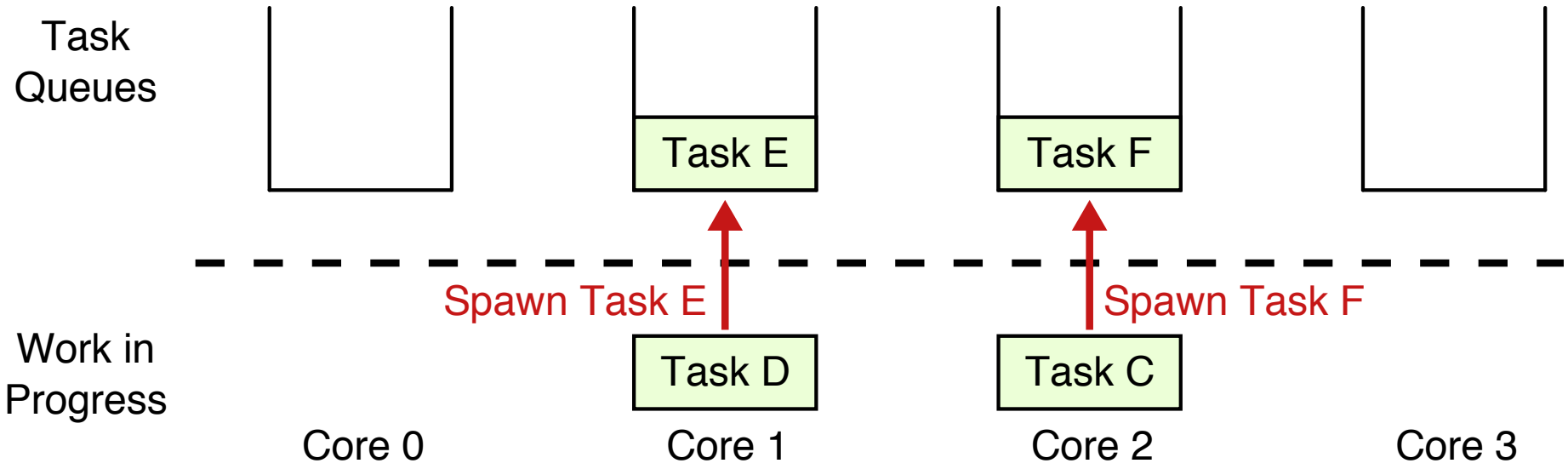
Work-Stealing Runtimes



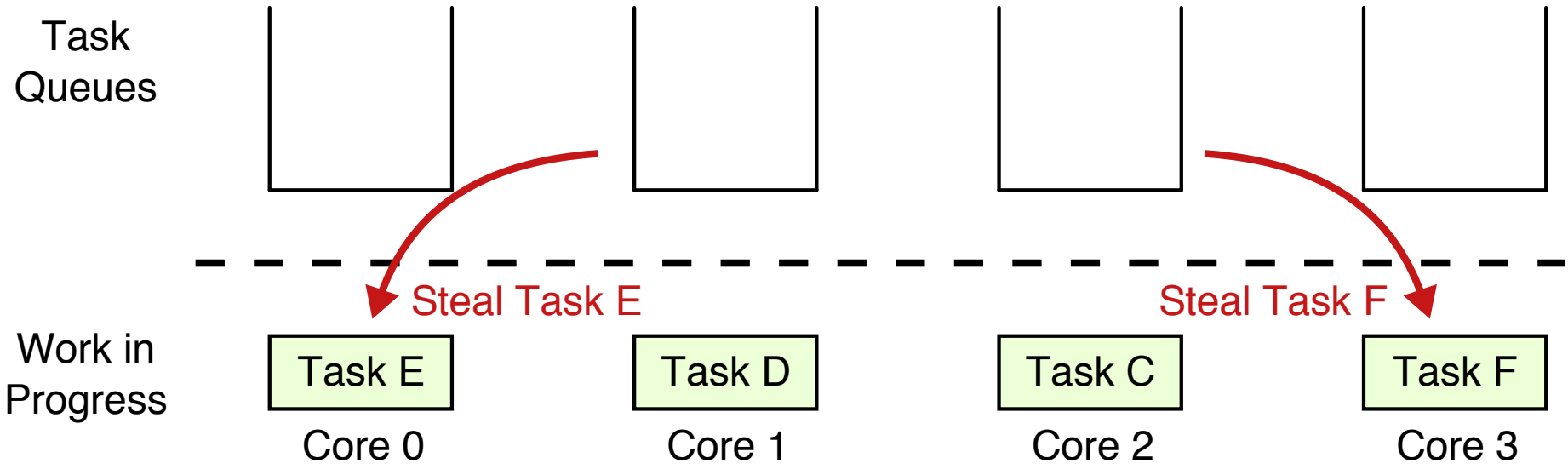
Work-Stealing Runtimes



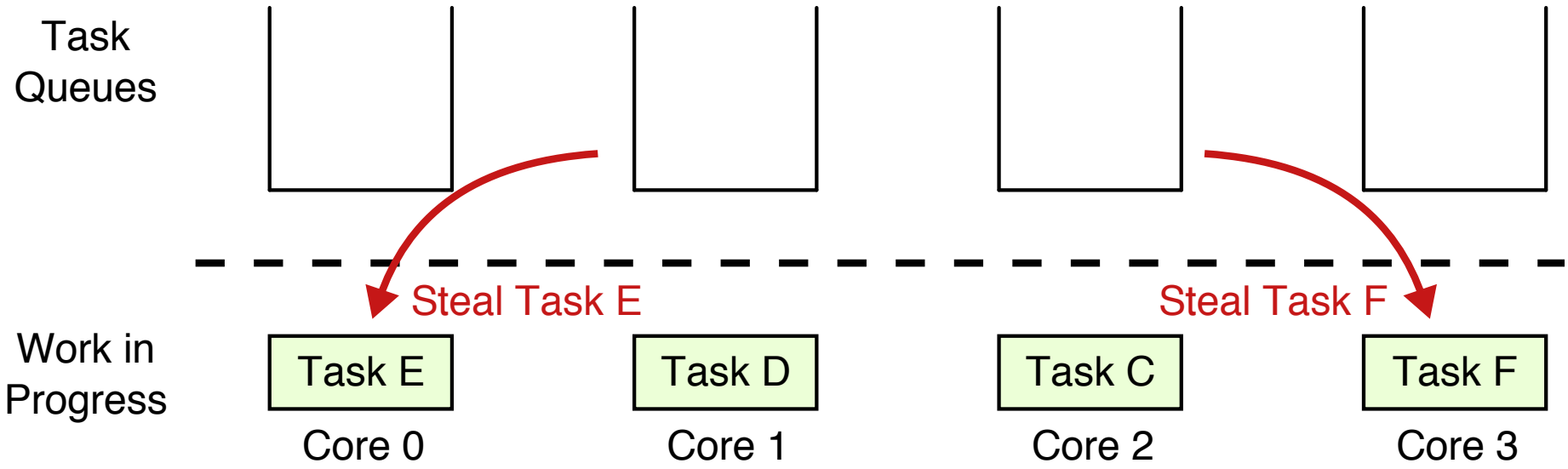
Work-Stealing Runtimes



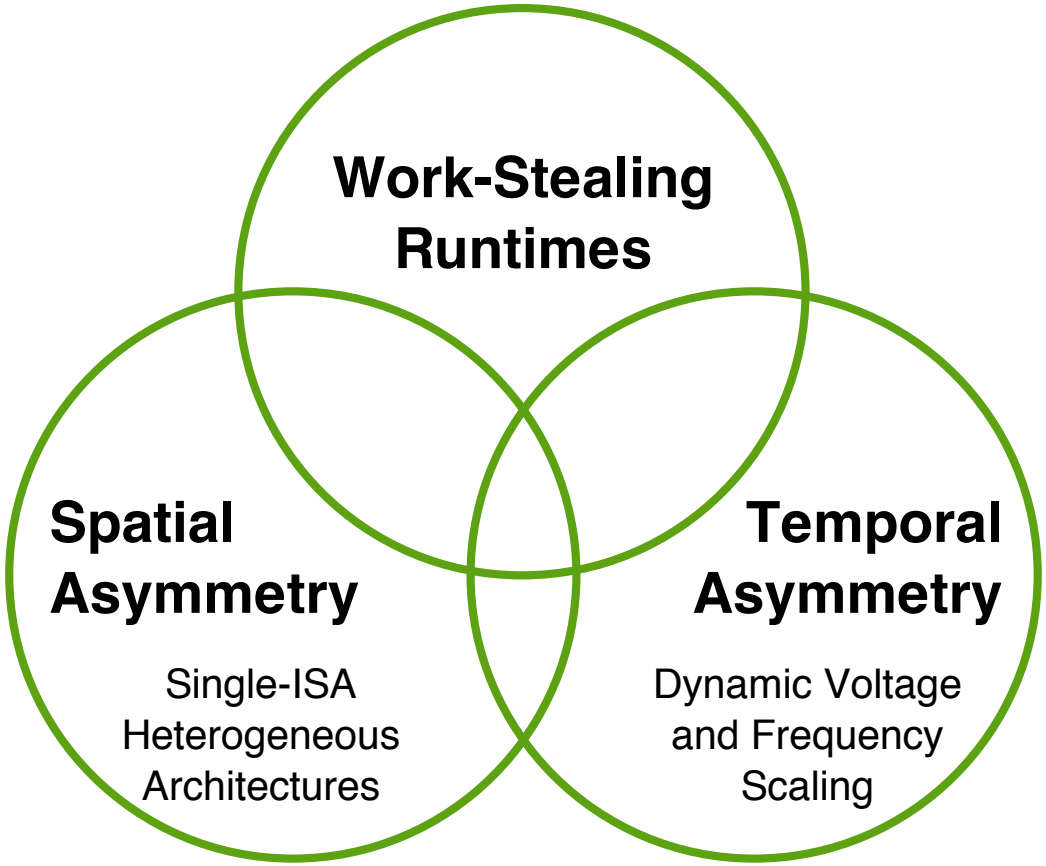
Work-Stealing Runtimes



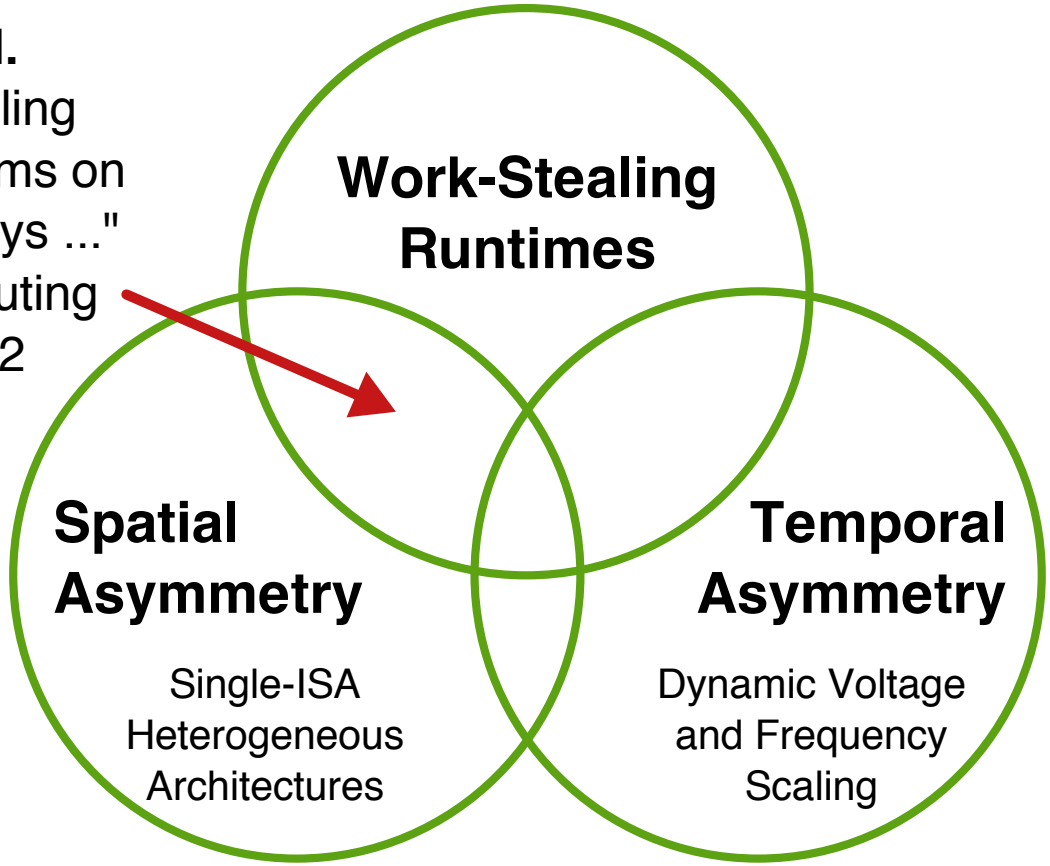
Work-Stealing Runtimes



- Work stealing has good performance, space requirements, and communication overheads in both theory and practice
- Supported in many popular concurrency platforms including: Intel's Cilk Plus, Intel's C++ TBB, Microsoft's .NET Task Parallel Library, Java's Fork/Join Framework, and OpenMP


Work-Stealing Runtimes
Spatial Asymmetry
Single-ISA Heterogeneous Architectures
Temporal Asymmetry
Dynamic Voltage and Frequency Scaling

Bender et al.
"Online Scheduling of Parallel Programs on Heterogeneous Sys ..."
Theory of Computing Systems 2002



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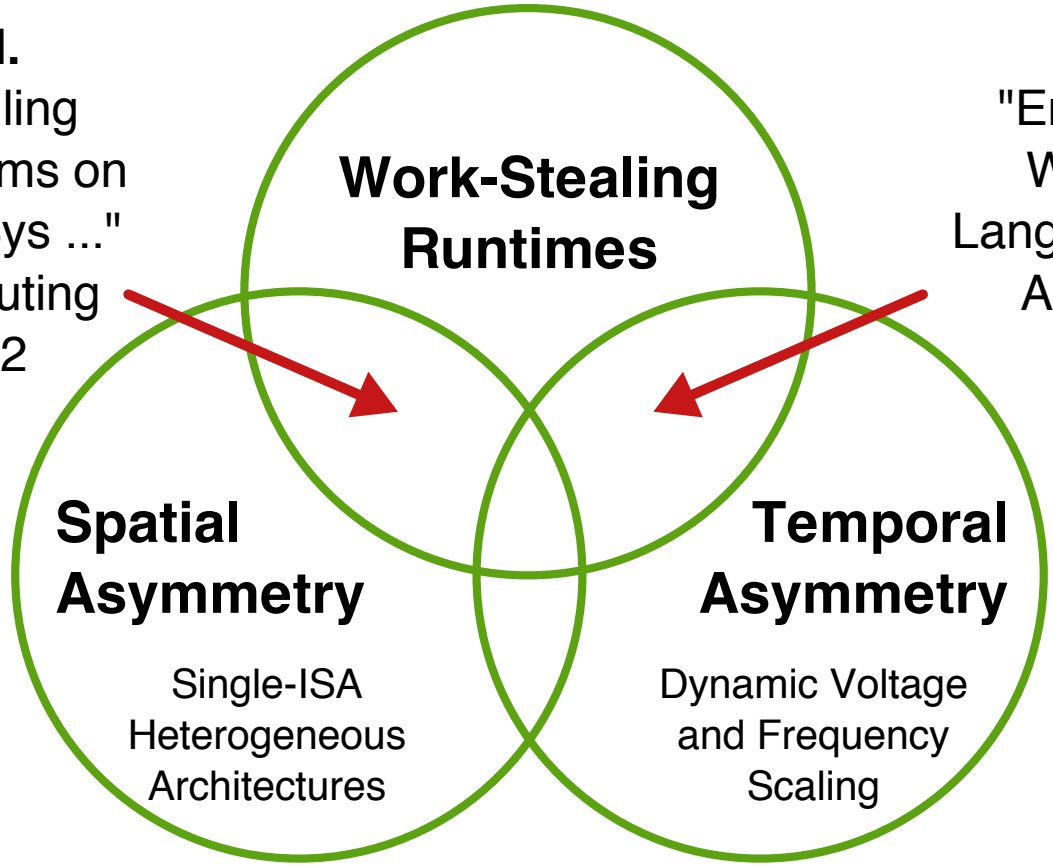
"Energy-Efficient Work-Stealing Language Runtimes"
ASPLOS 2014



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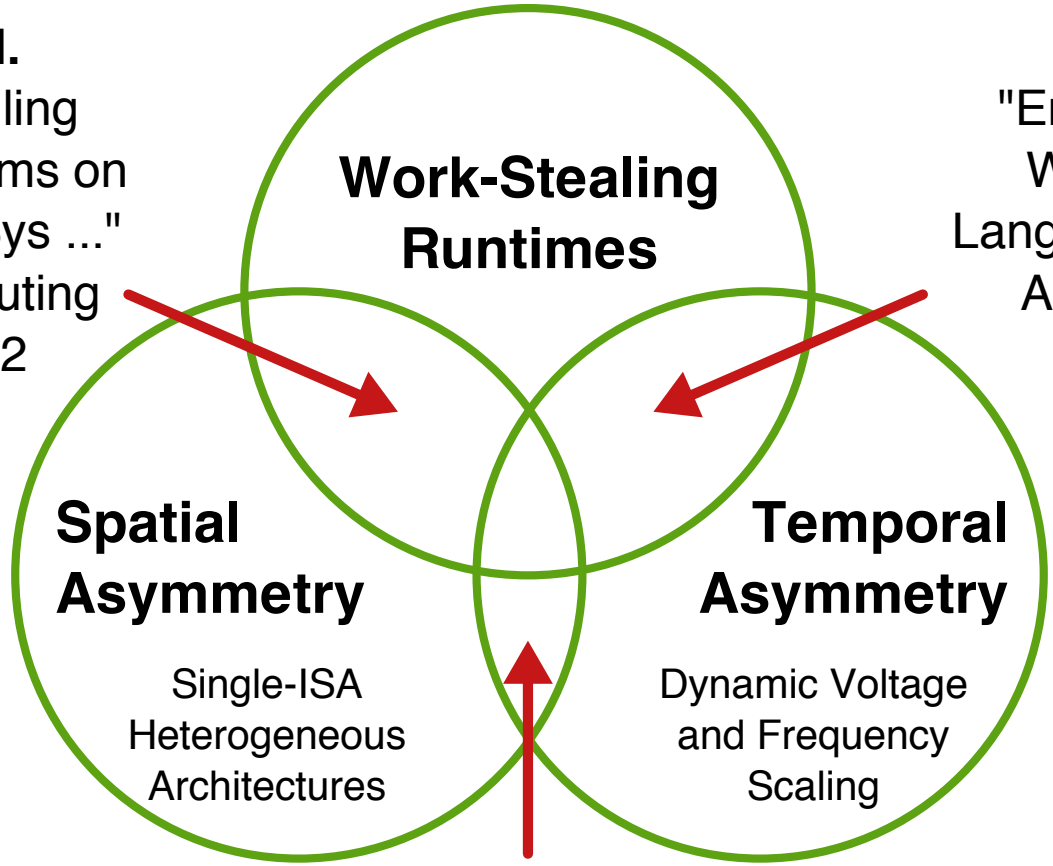

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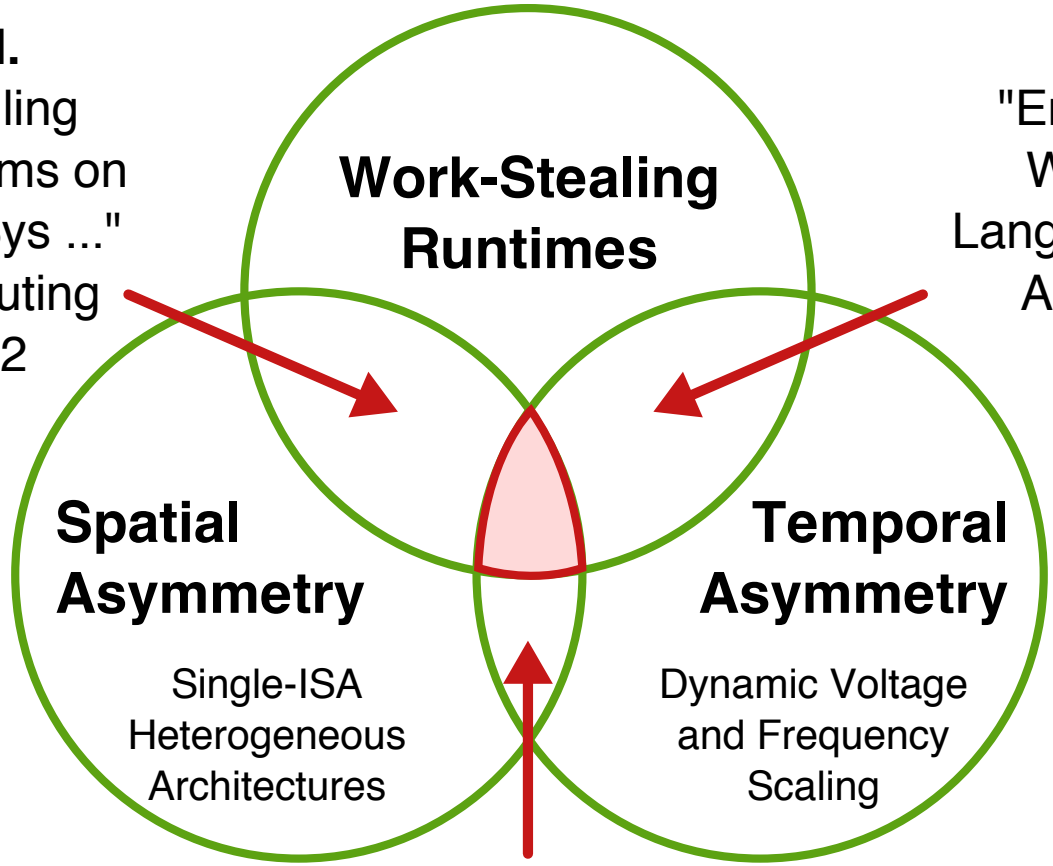

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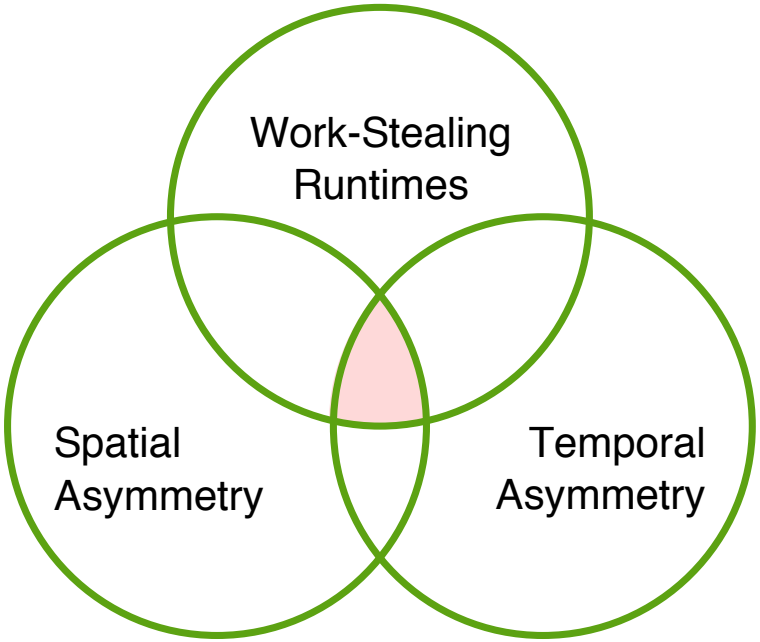
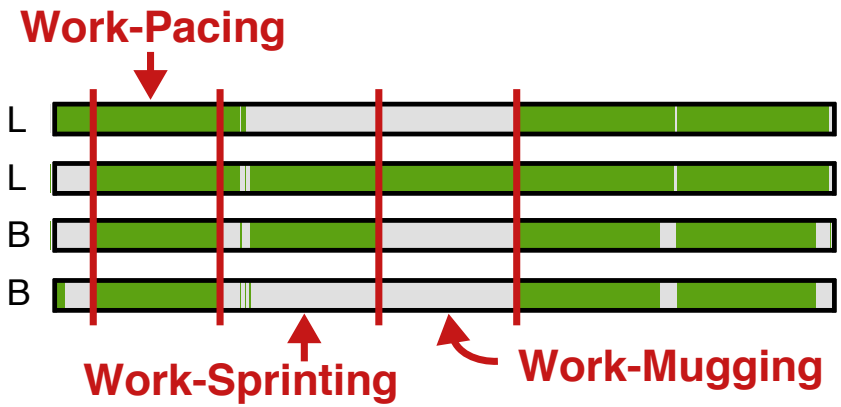
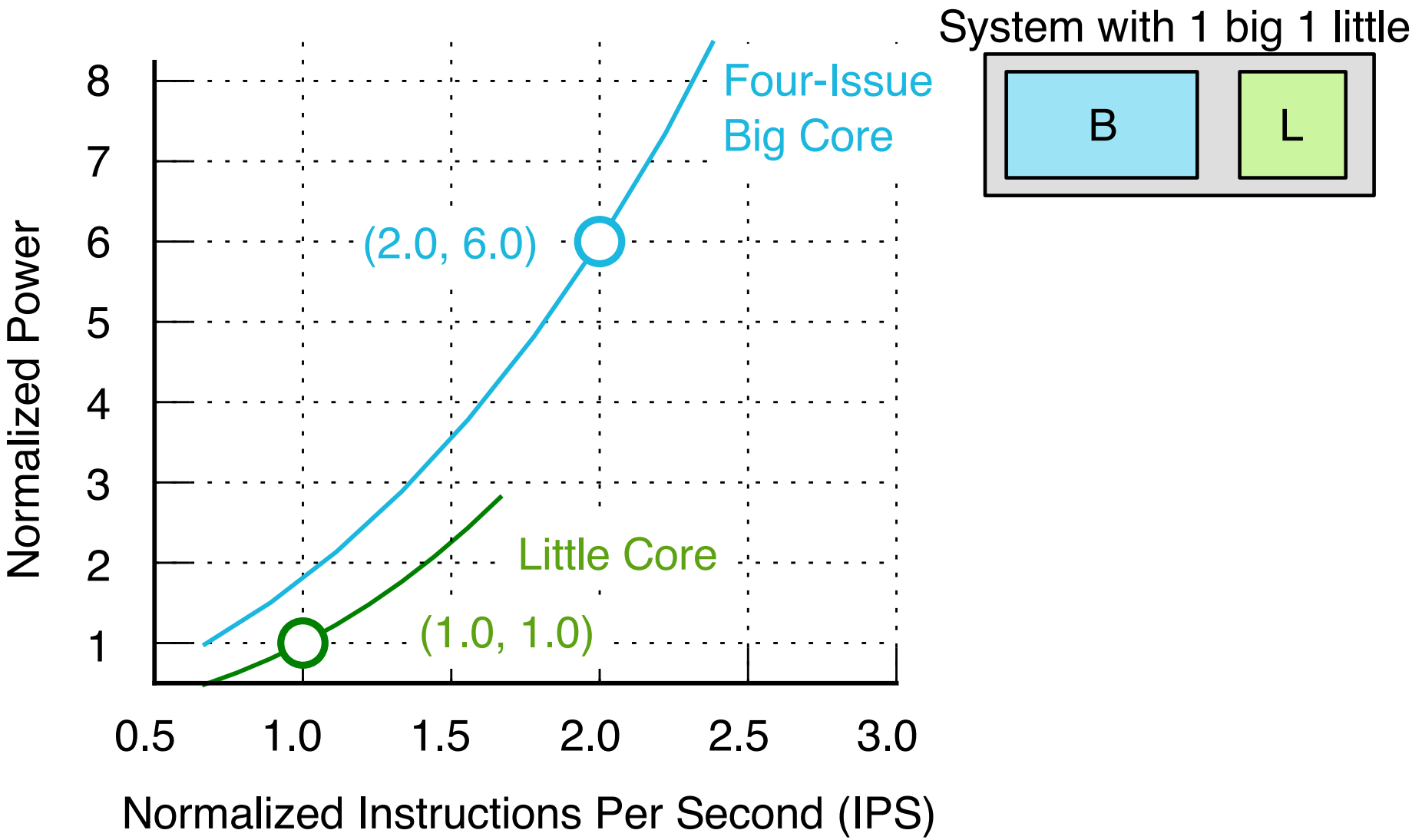




Exploiting Fine-Grain Asymmetry for Task-Based Parallelism

- Intuition
- Work-Pacing
- Results

Building Intuition by Exploring a 1 Big 1 Little System



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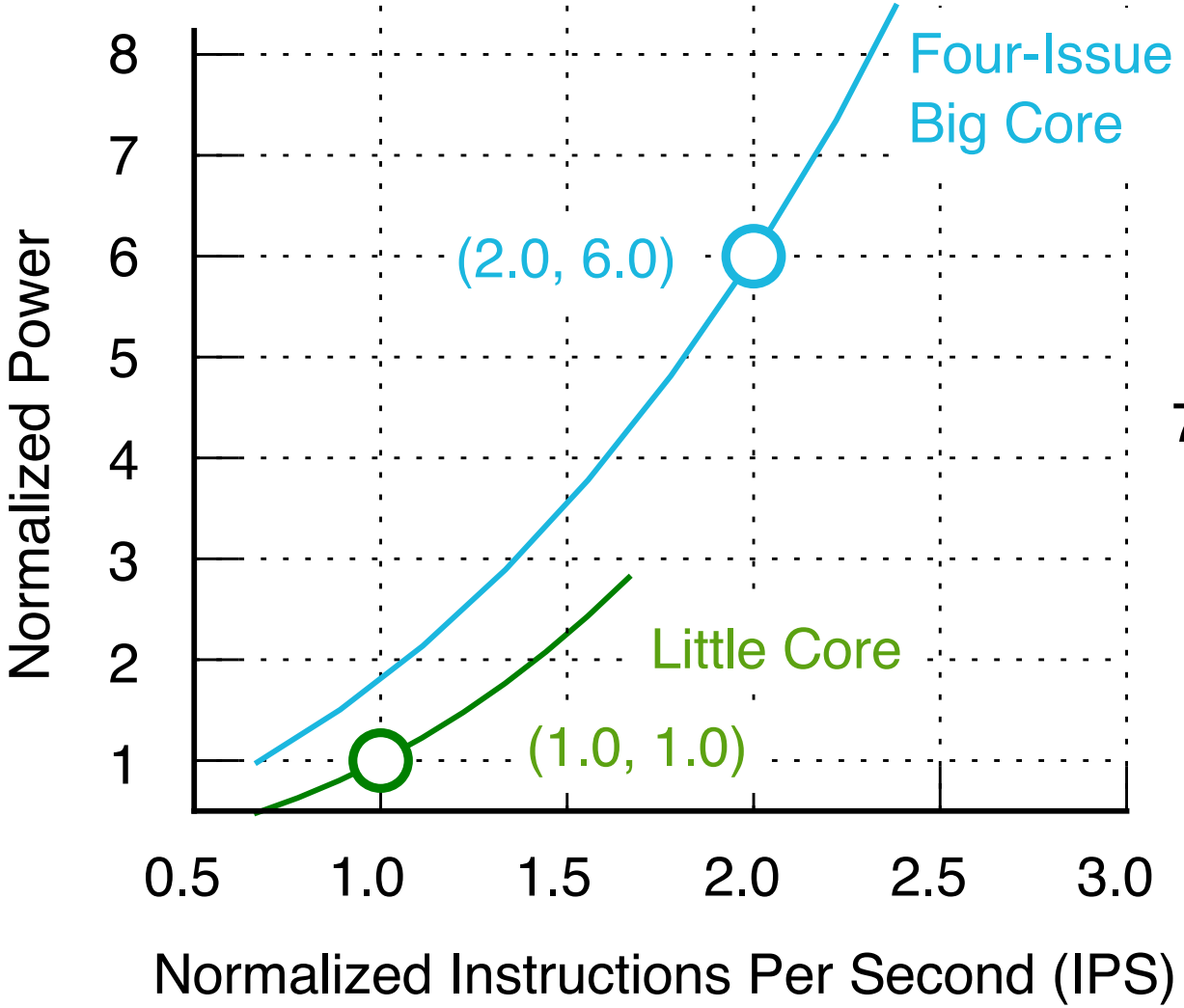

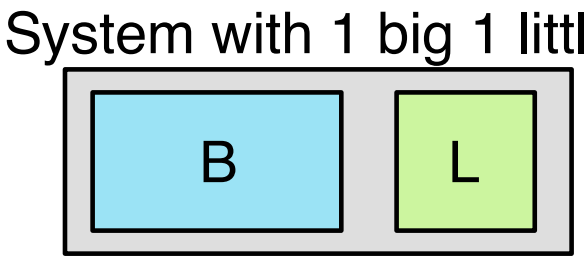

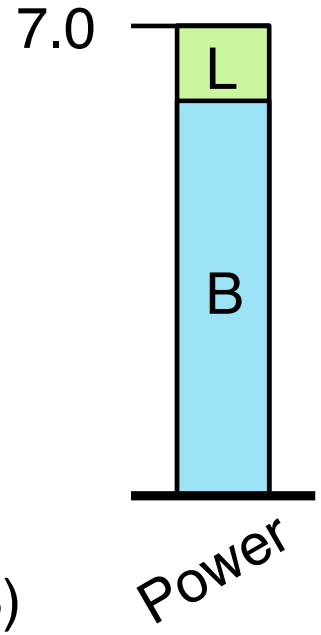

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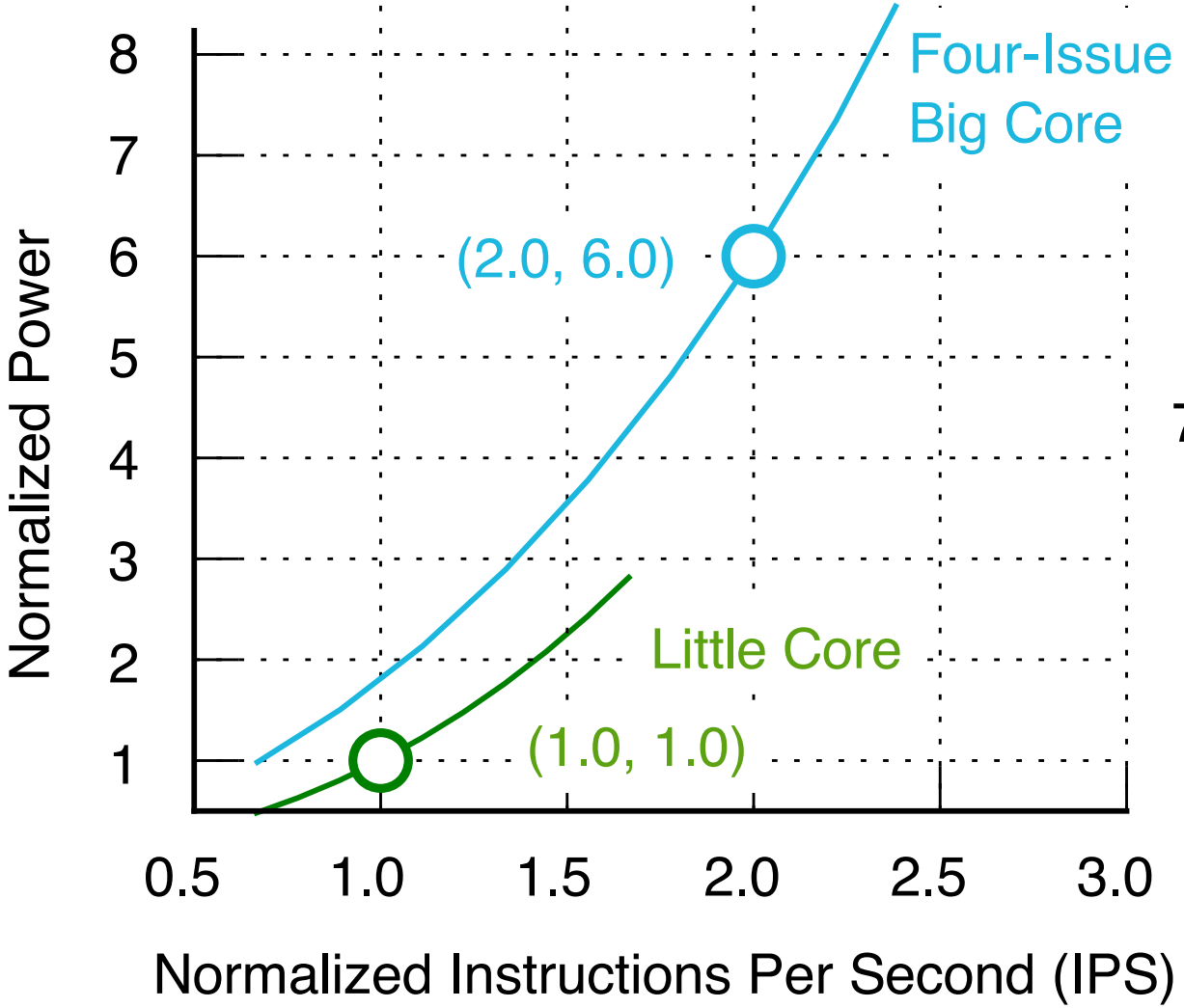

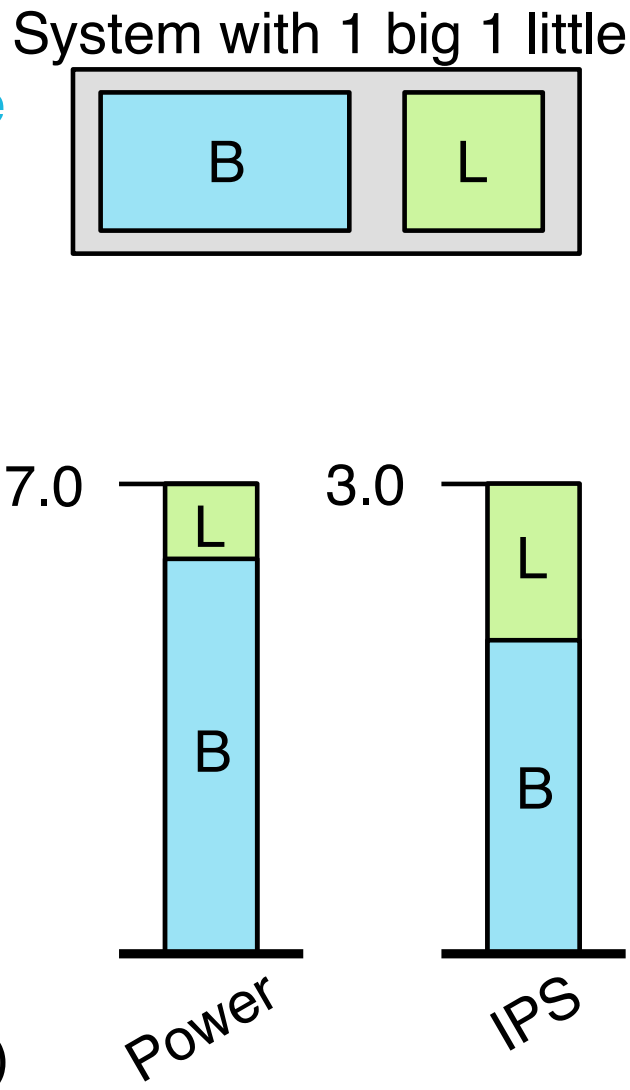

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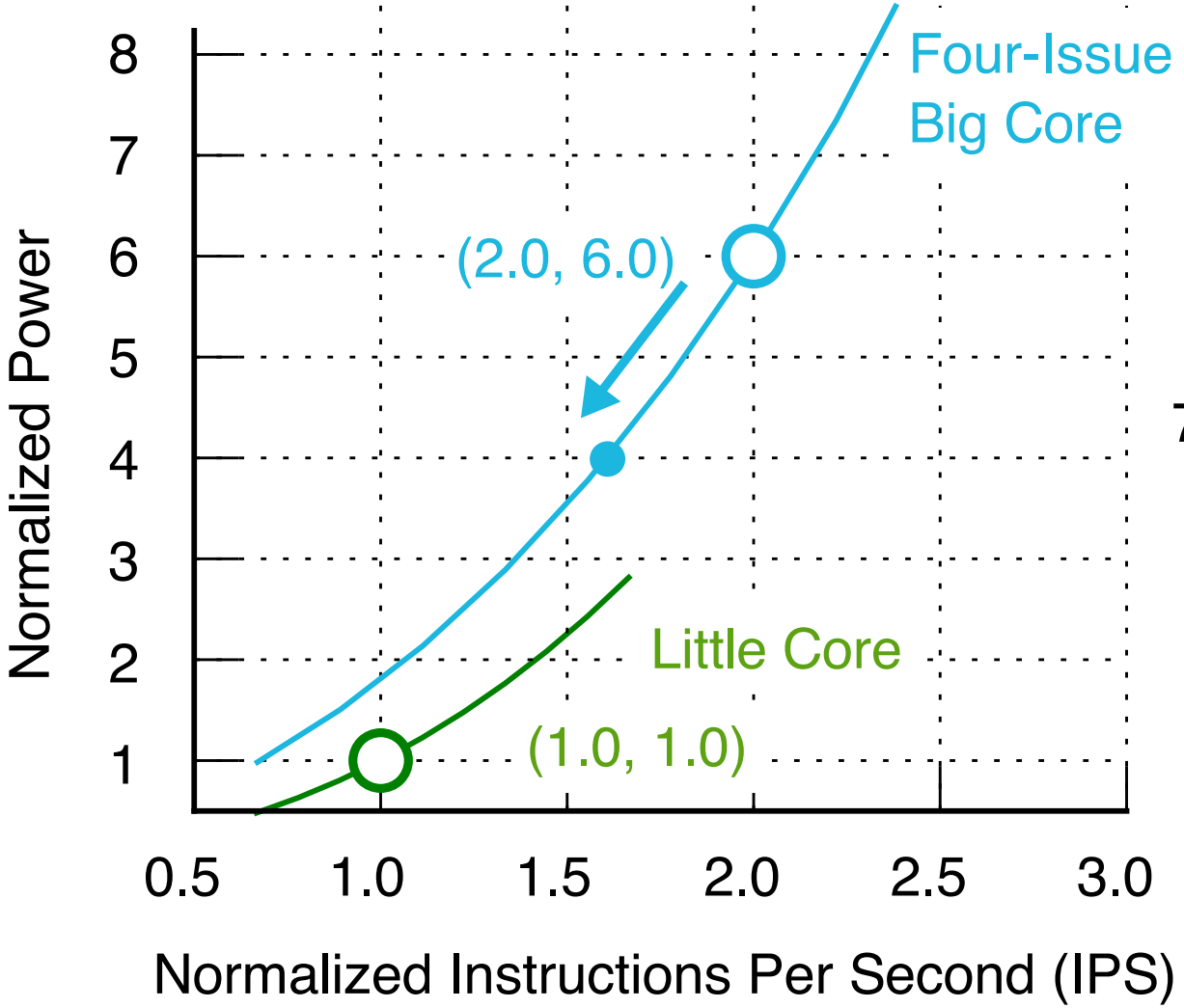

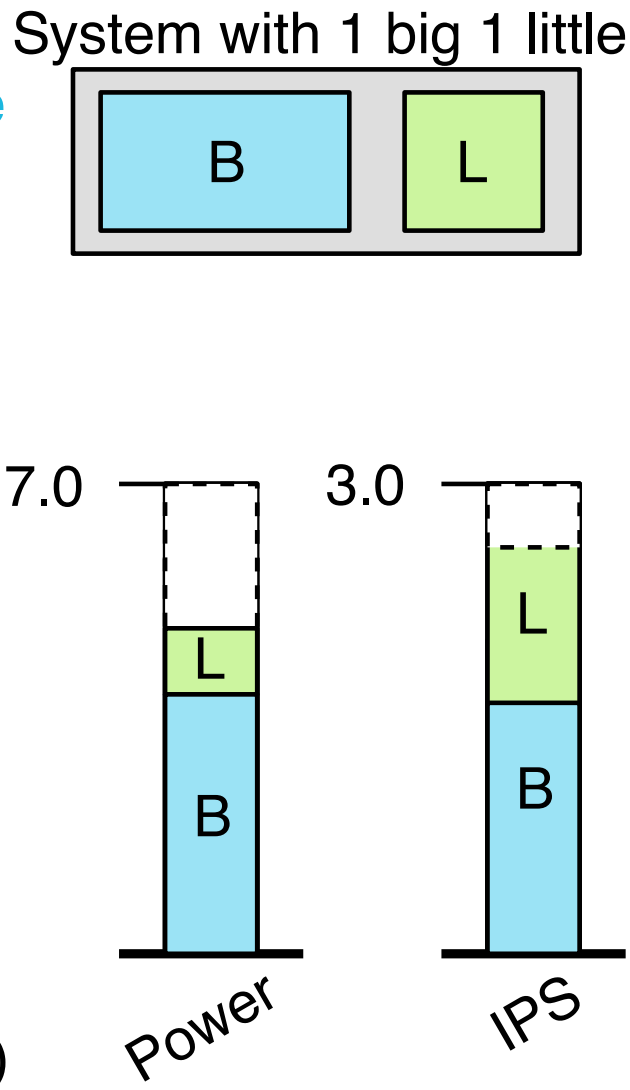

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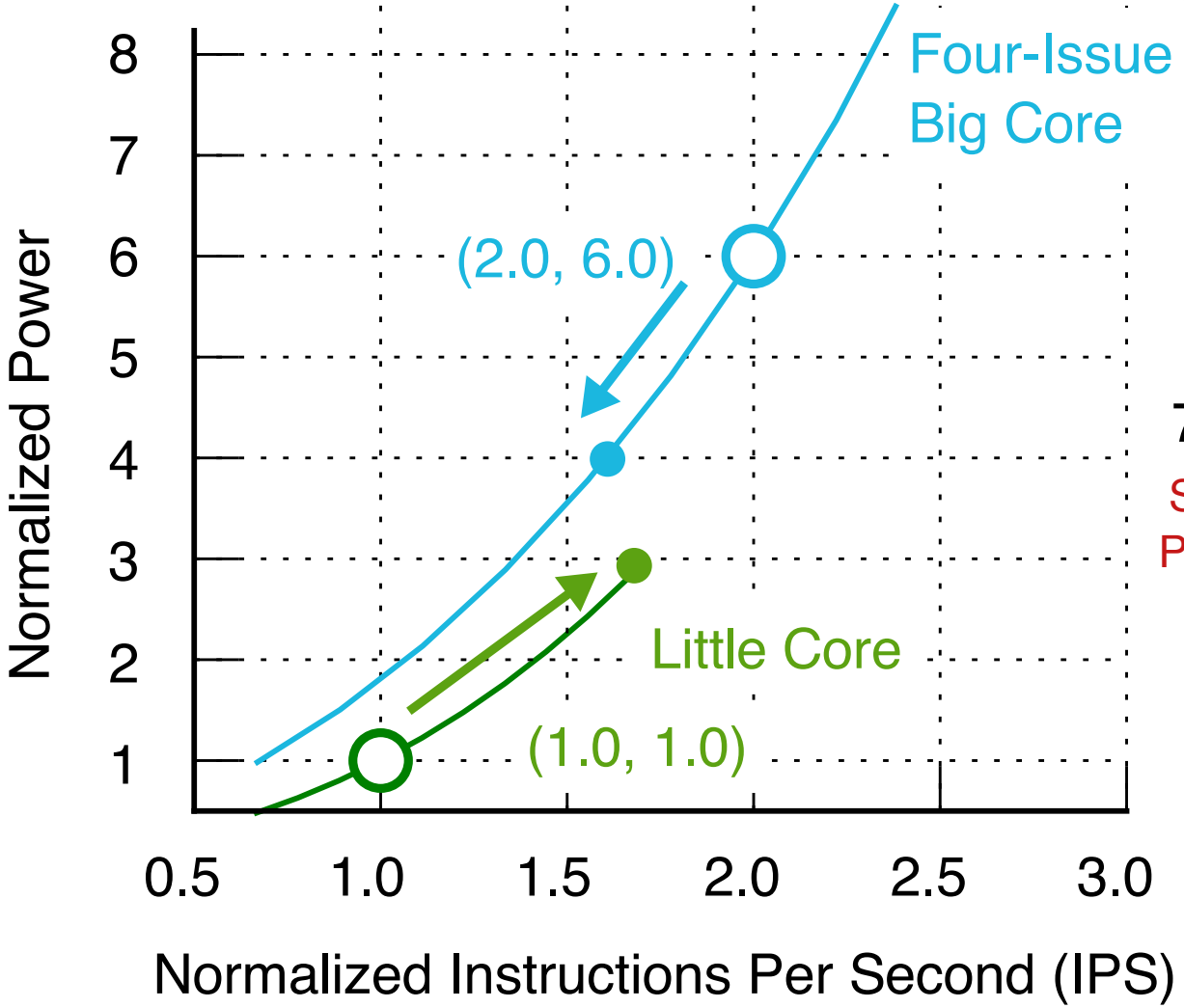

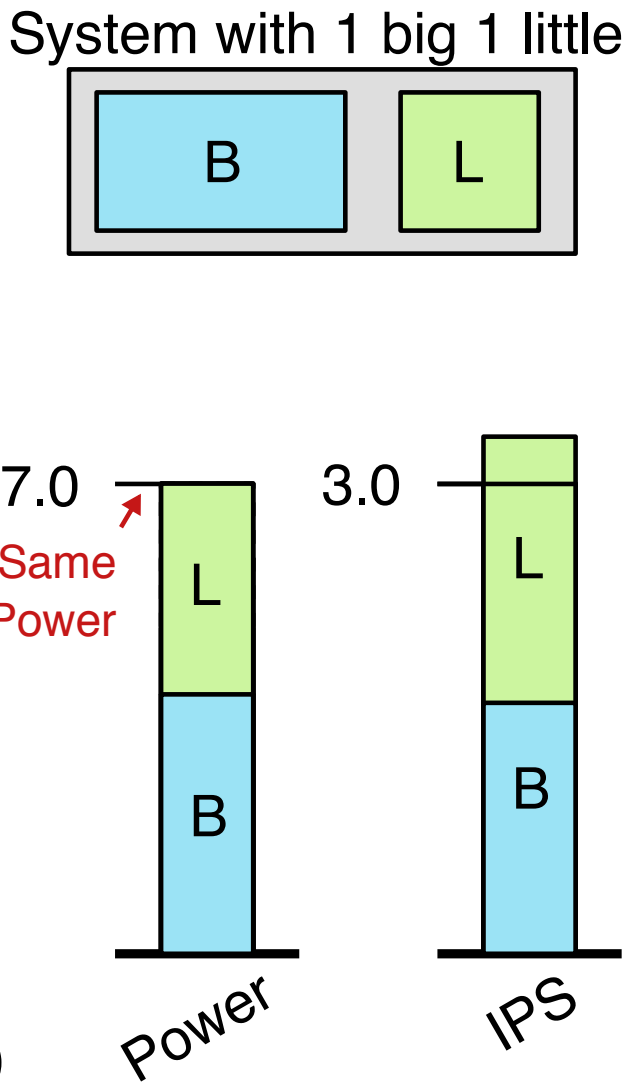

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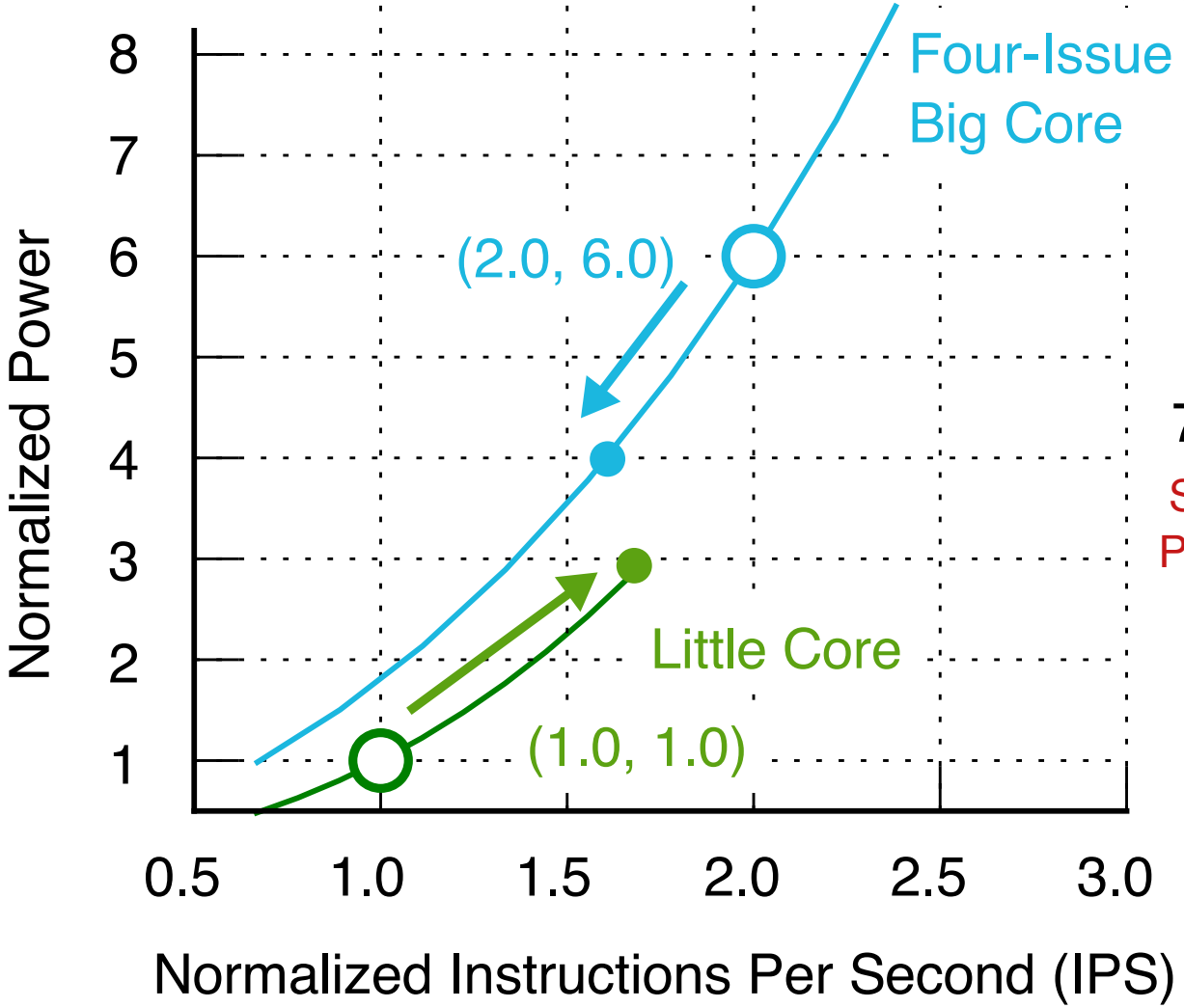

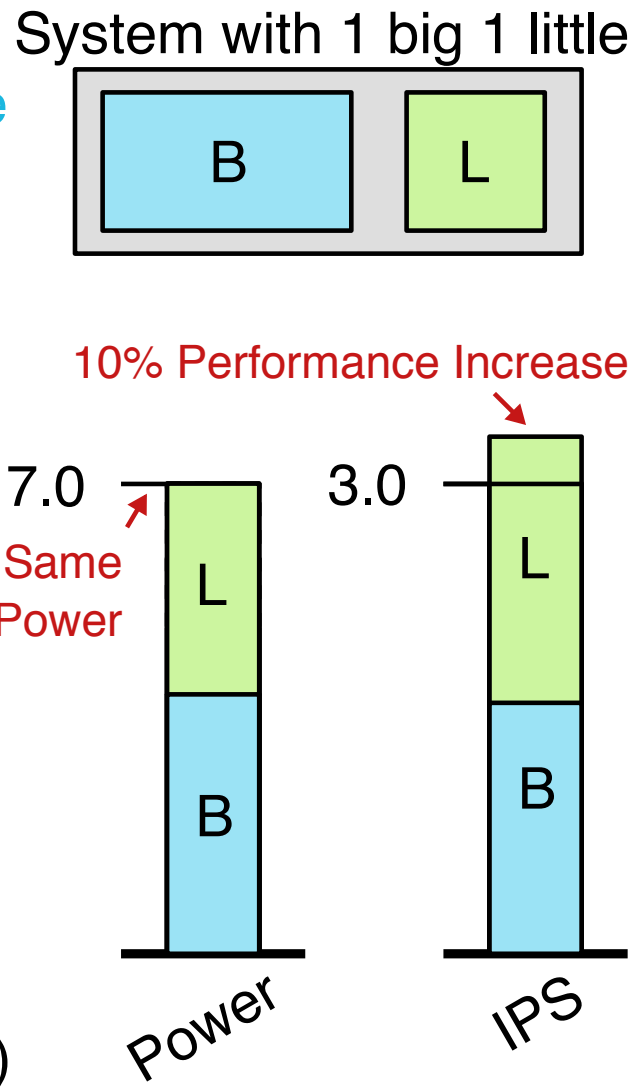

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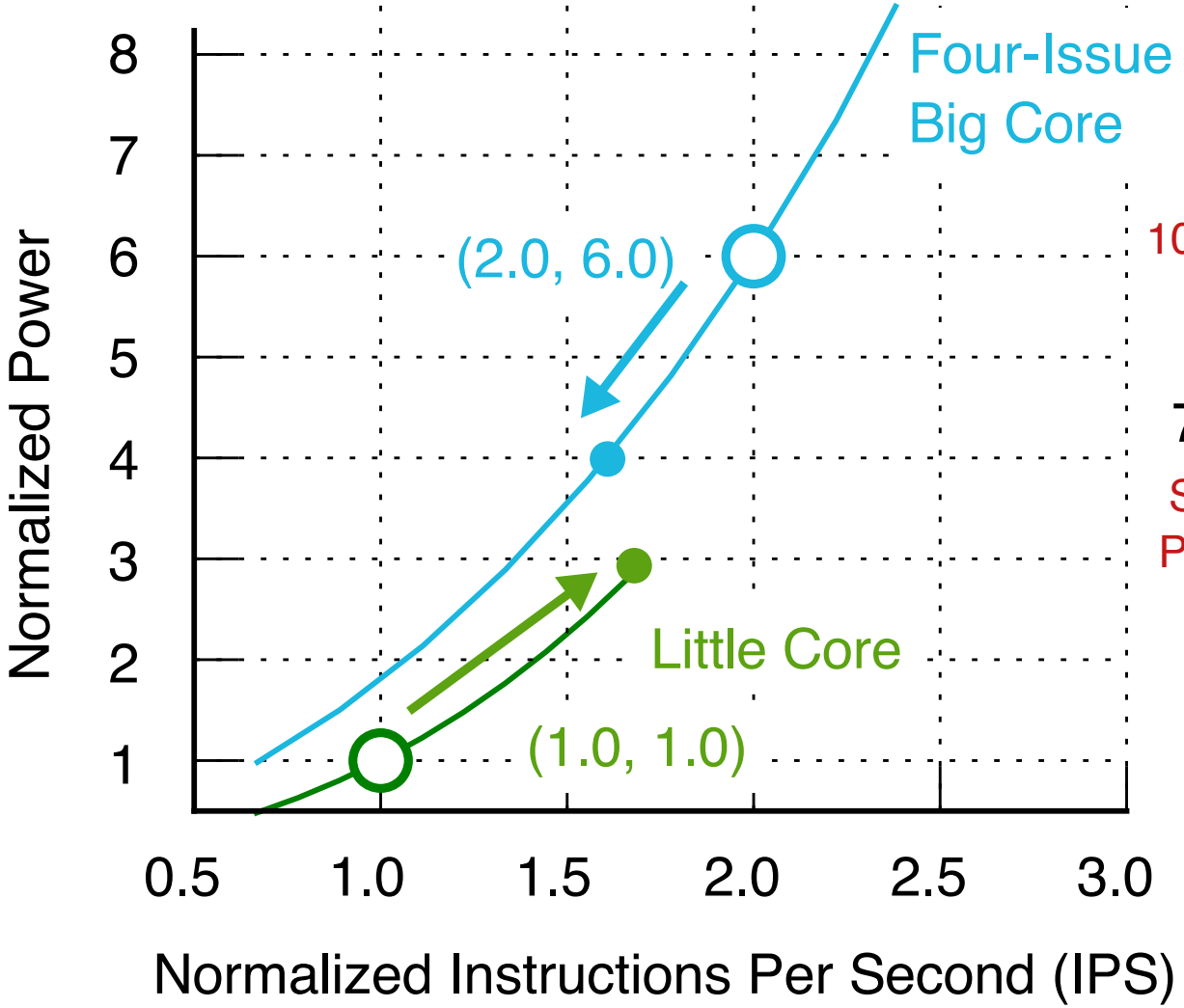
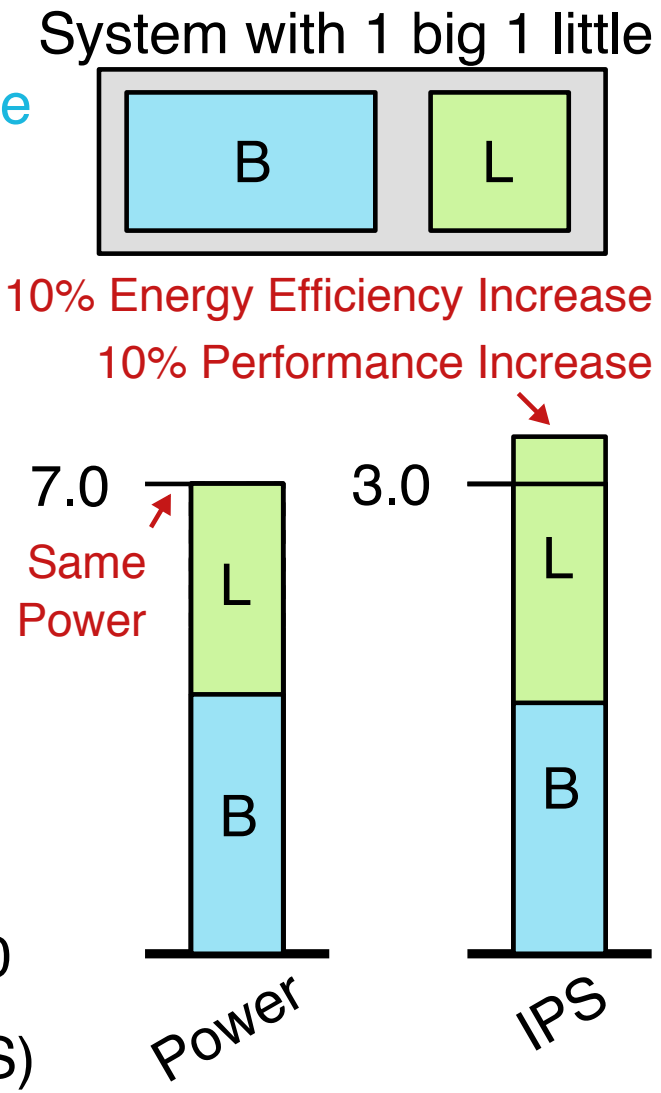
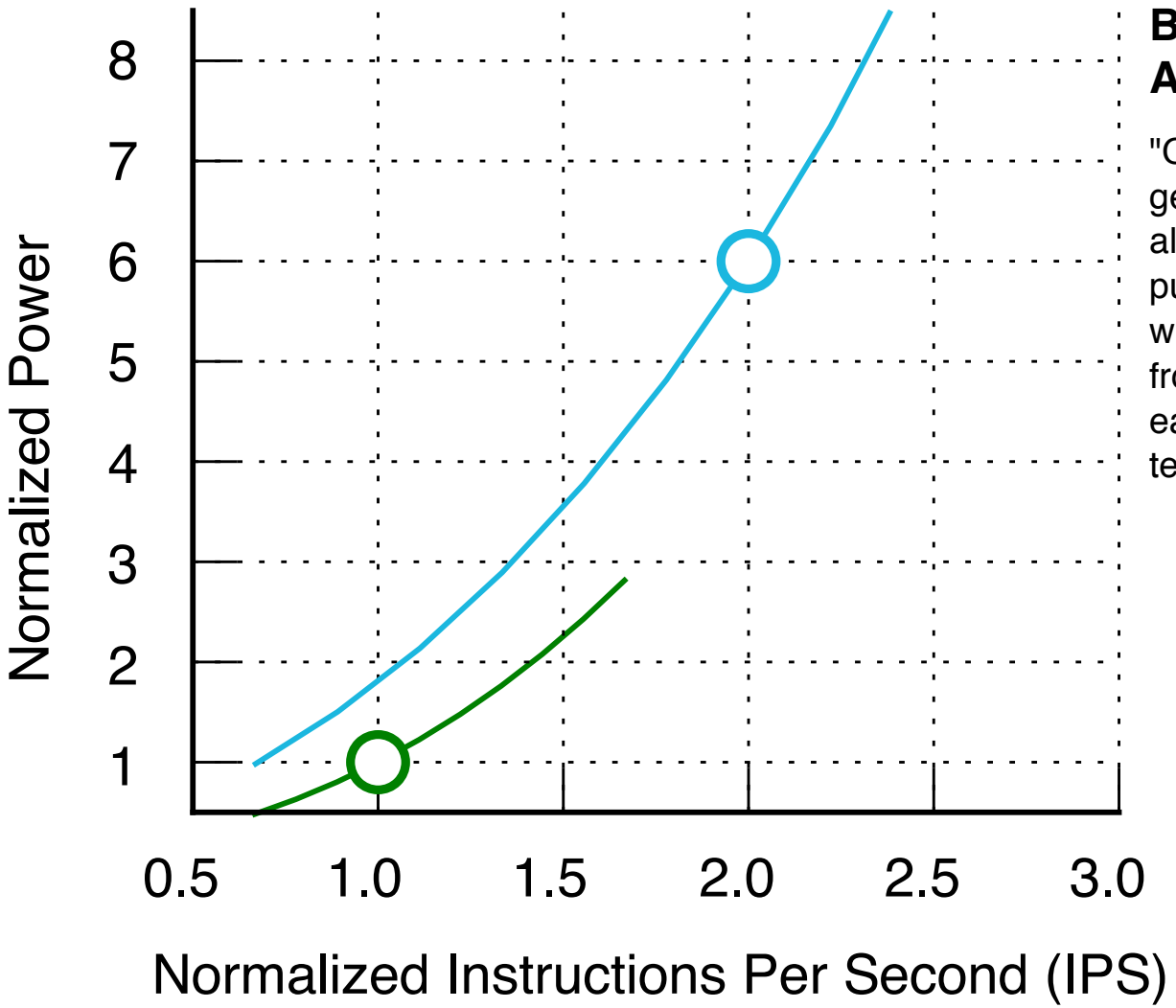




The Law of Equi-Marginal Utility



British Economist
Alfred Marshall (1824 - 1924)

"Other things being equal, a consumer gets **maximum satisfaction** when he allocates his **limited income** to the purchase of different goods in such a way that the **Marginal Utility** derived from the last unit of money spent on each item of expenditure tend **to be equal**."

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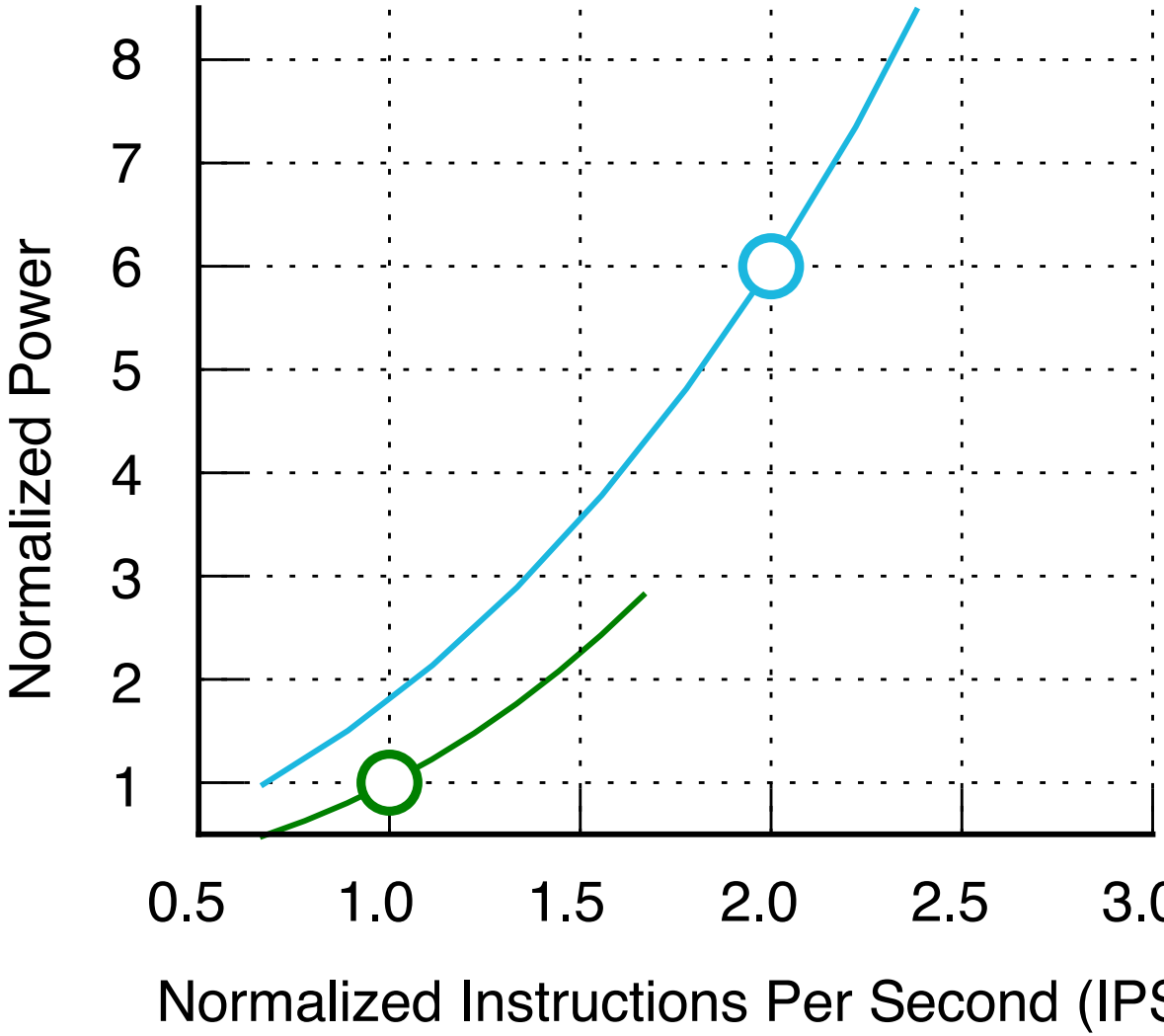

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Balance the ratio of utility (IPS) to cost (power)

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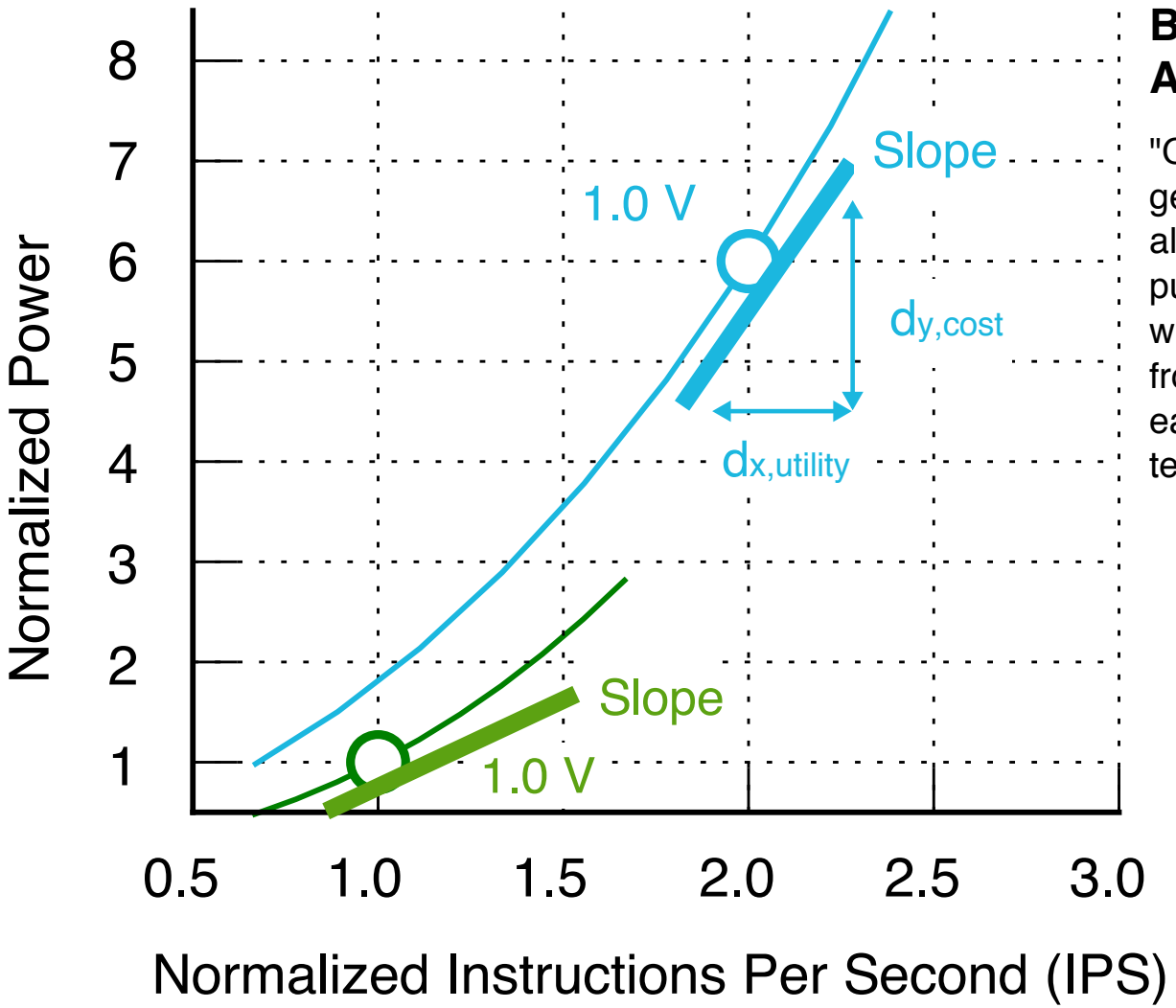

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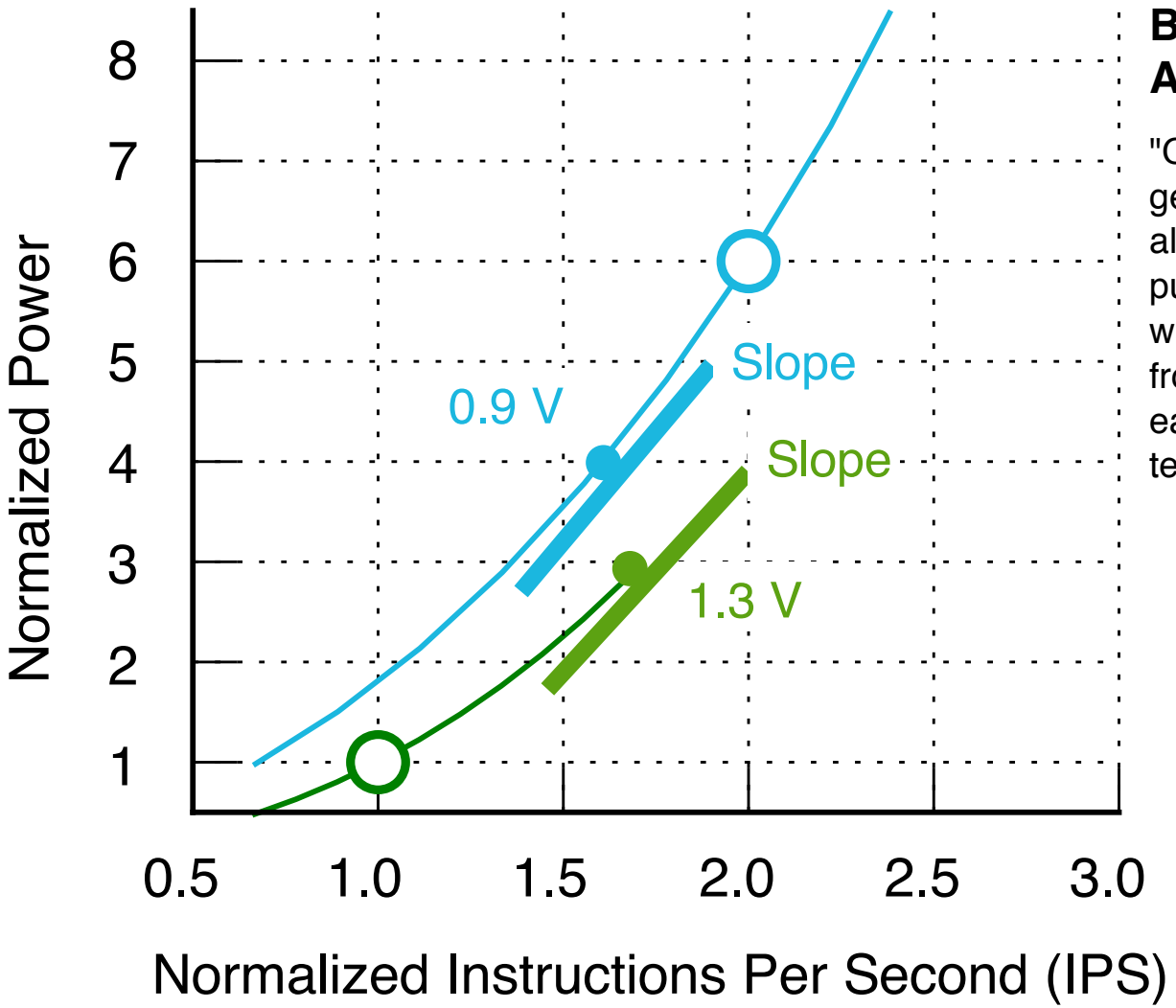

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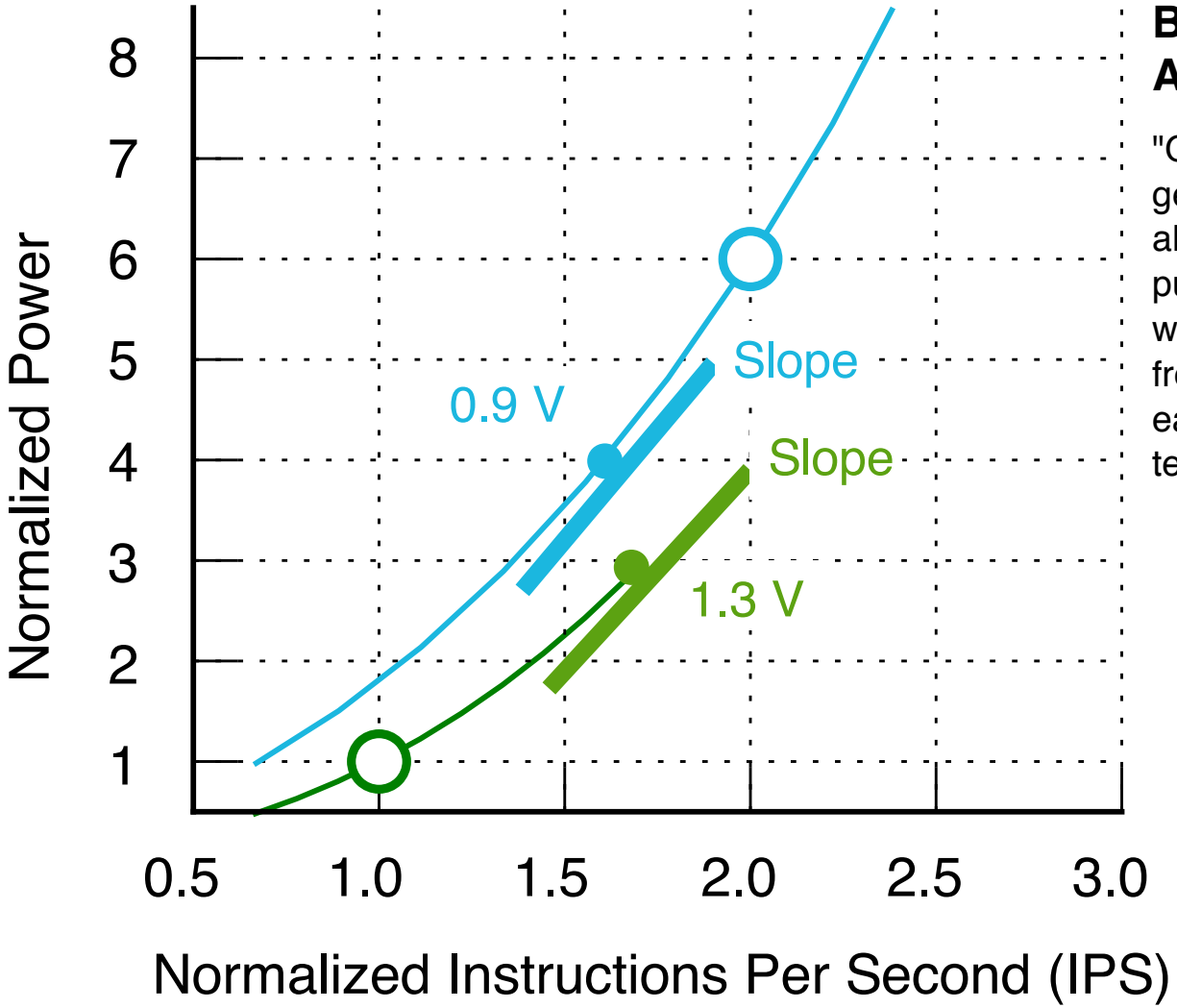

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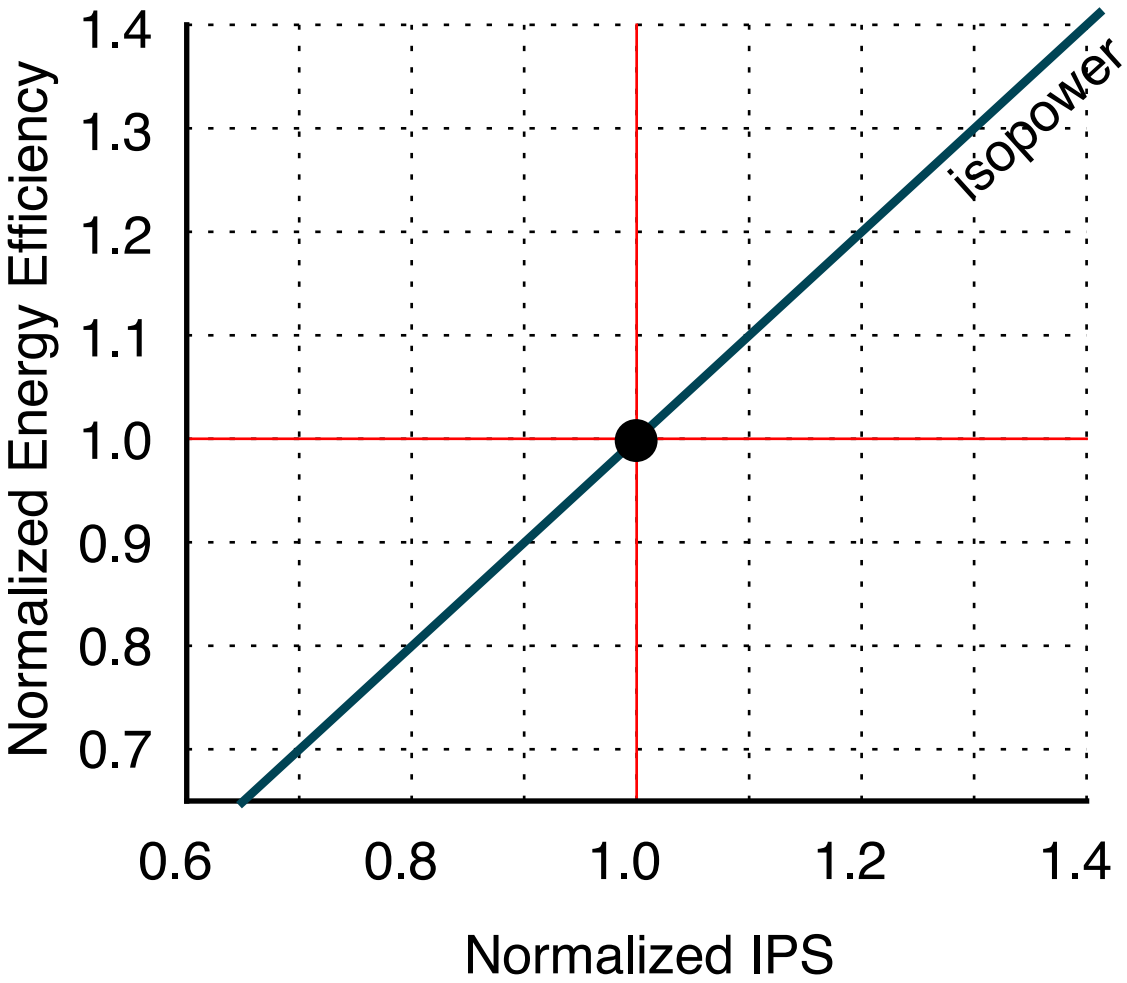
Balance the ratio of utility (IPS) to cost (power)

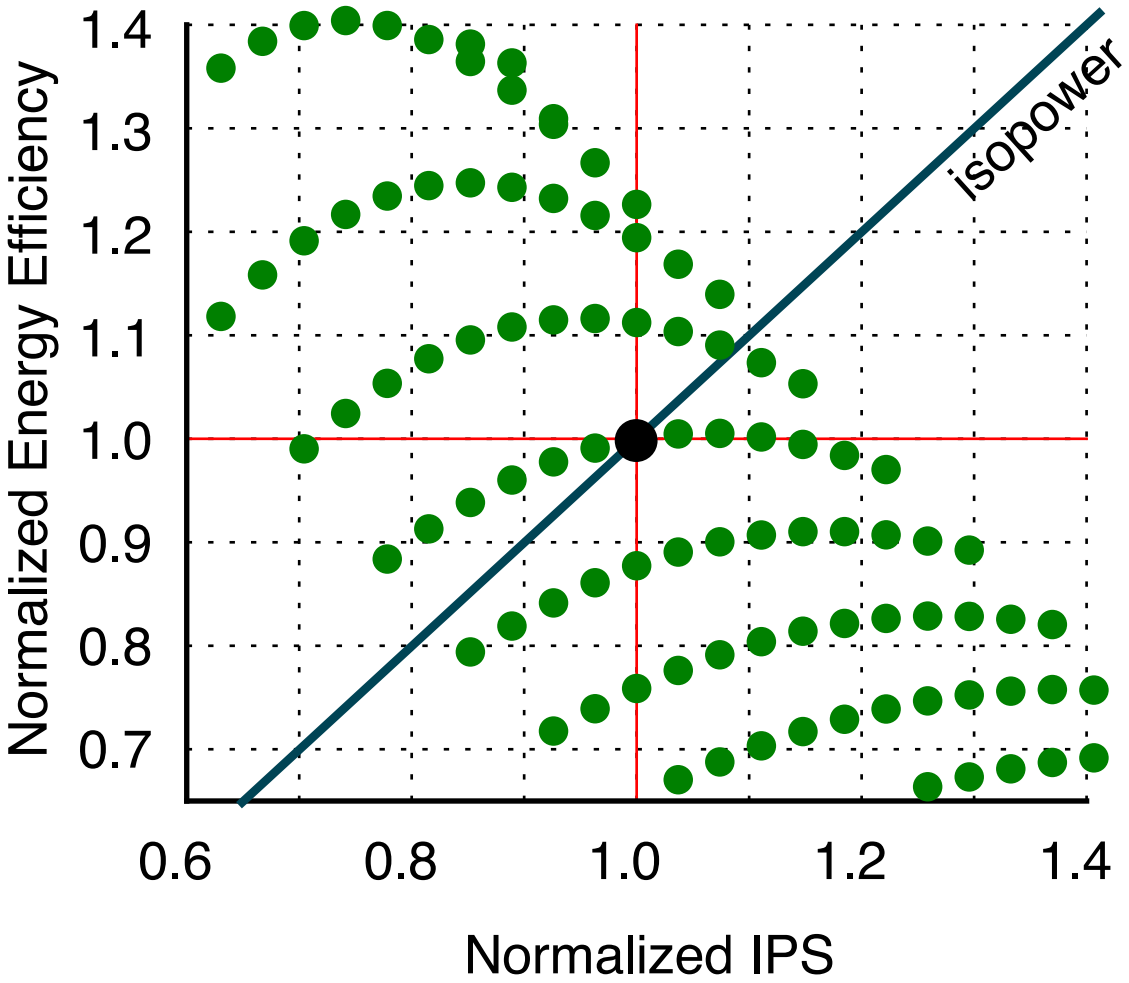
Arbitrage
"Buy Low, Sell High"

Systematic Approach for Balancing Marginal Utility



- 1 Big 1 Little System at Nominal voltage

Systematic Approach for Balancing Marginal Utility

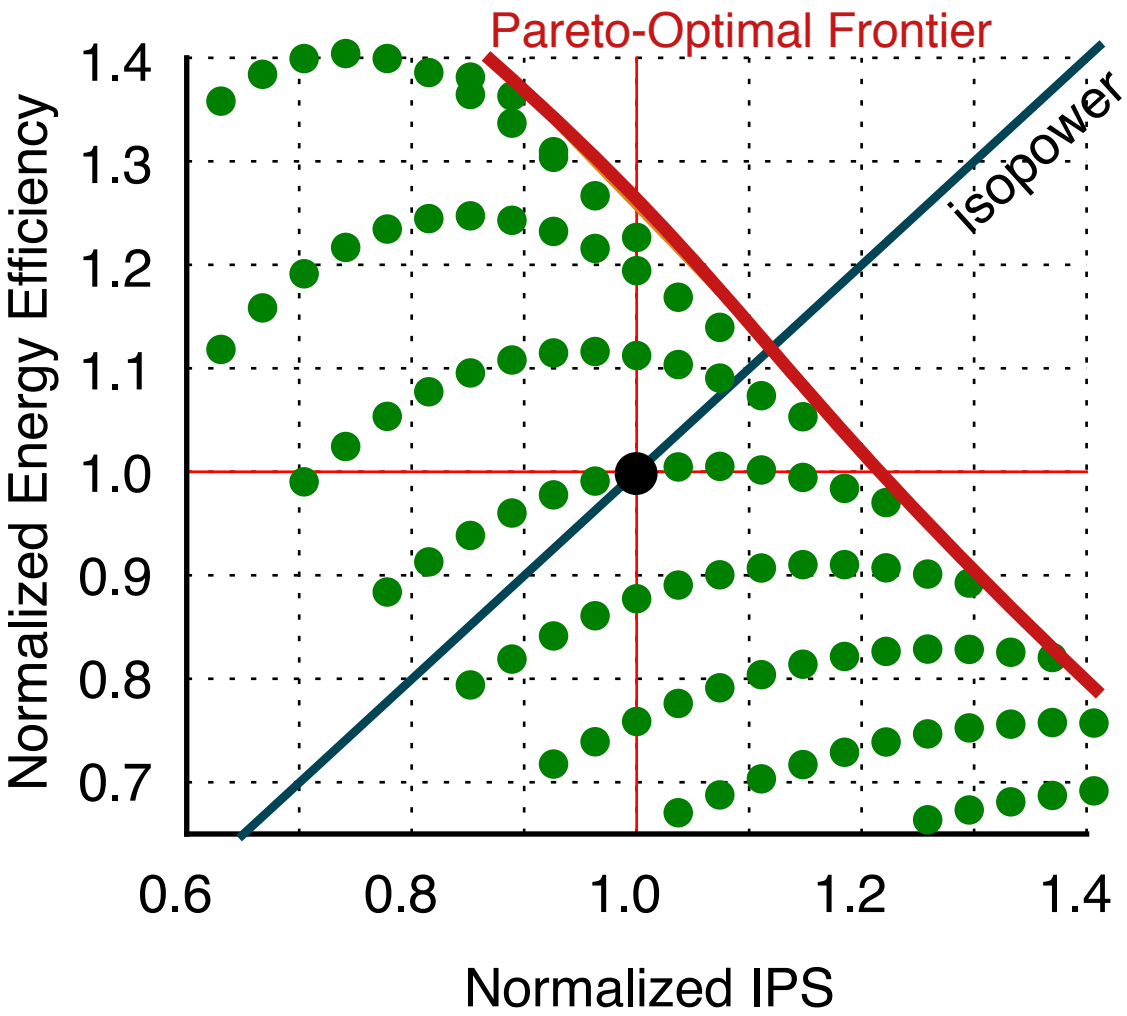


- 1 Big 1 Little System at Nominal voltage
- Individual (V_B, V_L) pair

Assumptions

Perfectly parallel application
Ideal load balancing

Systematic Approach for Balancing Marginal Utility



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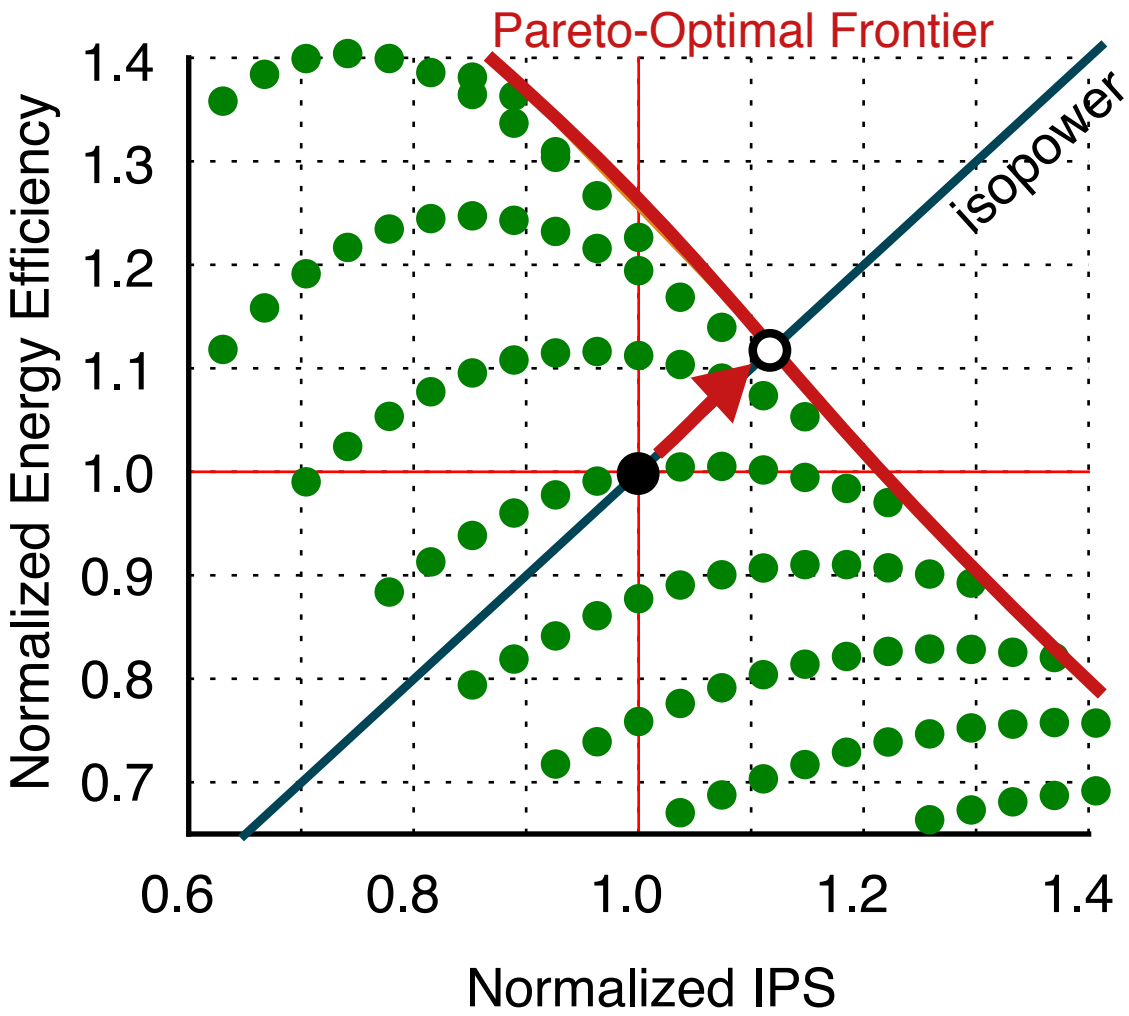


- 1 Big 1 Little System at Nominal voltage
- Individual (V_B, V_L) pair

Assumptions

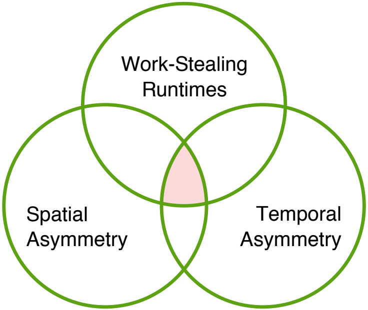
Perfectly parallel application
Ideal load balancing

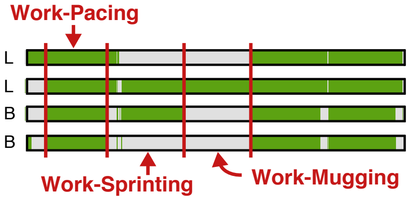
Marginal Utility-Based Optimization Problem

Constraint: *isopower line*

Objective: *maximize performance*

(Solved numerically)



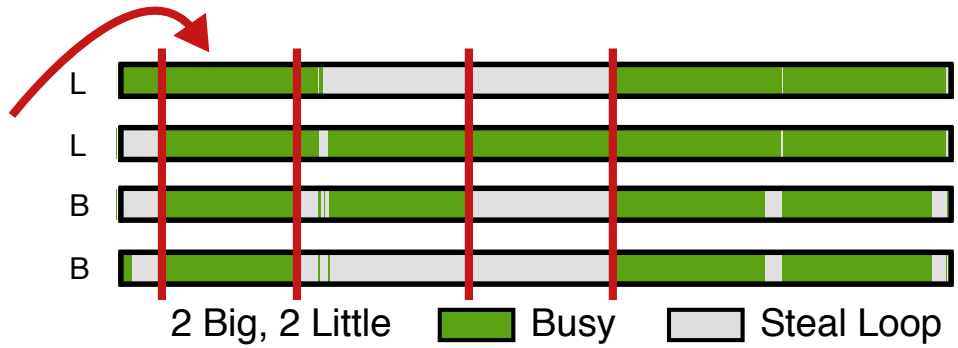


Exploiting Fine-Grain Asymmetry for Task-Based Parallelism

- Intuition
- **Work-Pacing**
- Results

Work-Pacing: Building Intuition

Balance performance/power across cores in the high-parallel (HP) region



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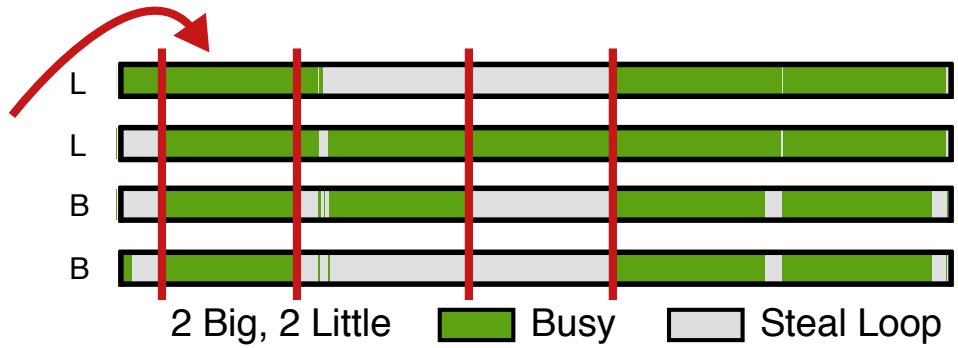
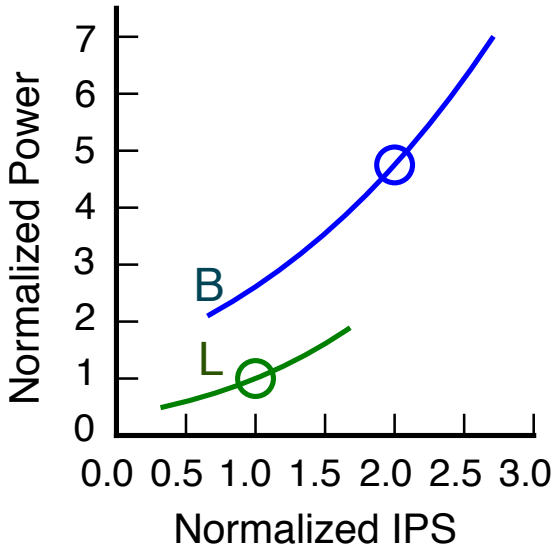
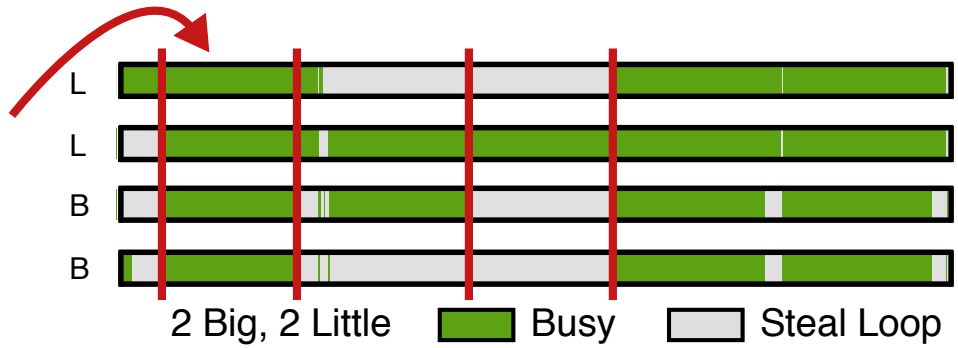


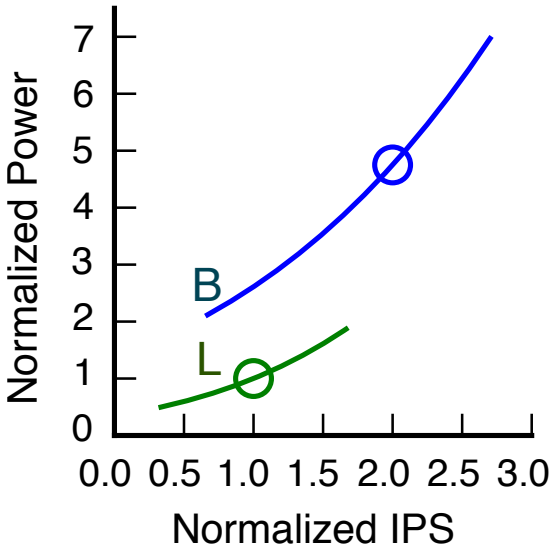


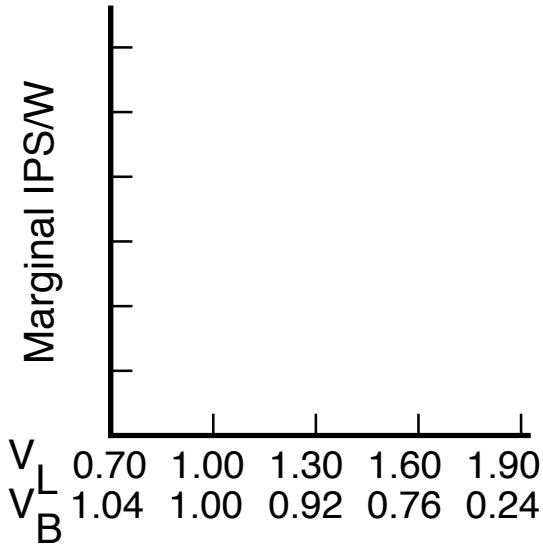
System with both big cores active and both little cores active

Work-Pacing: Building Intuition

Balance performance/power across cores in the high-parallel (HP) region







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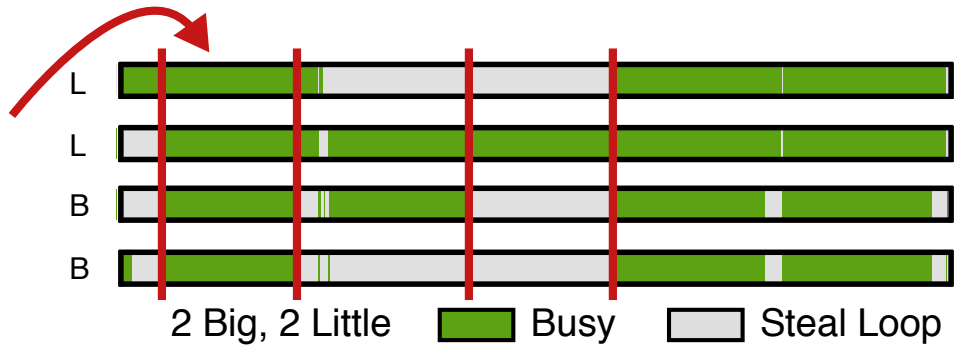
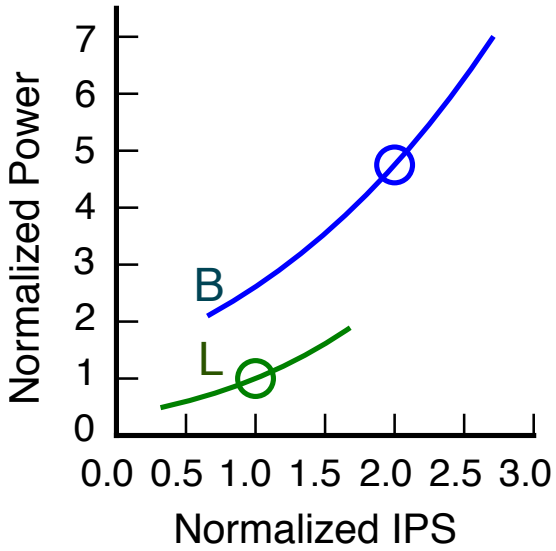
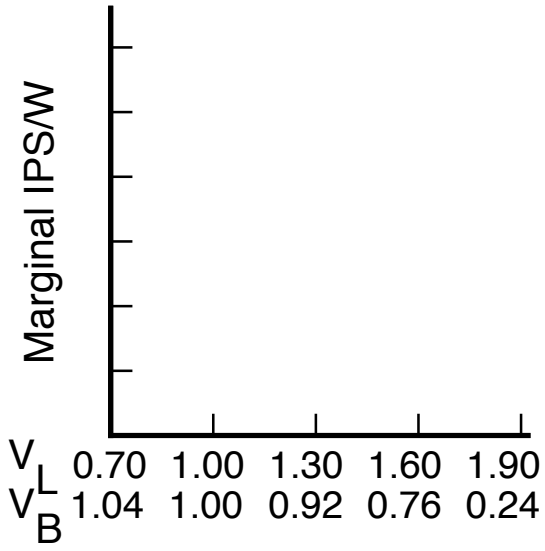
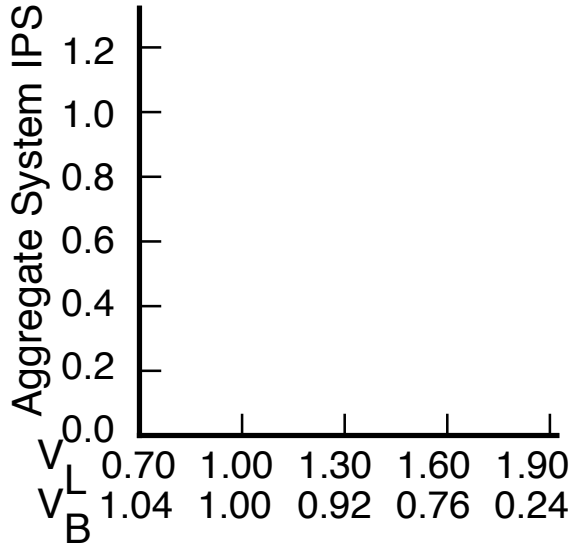




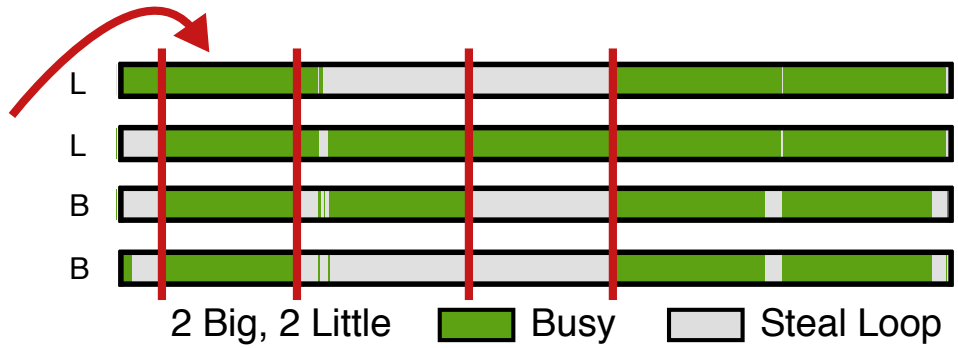


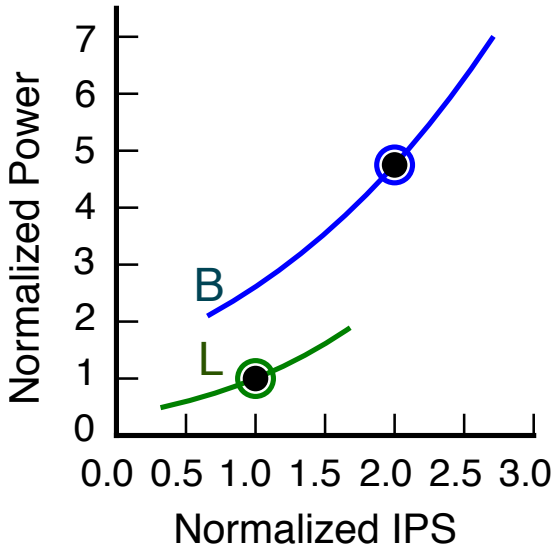


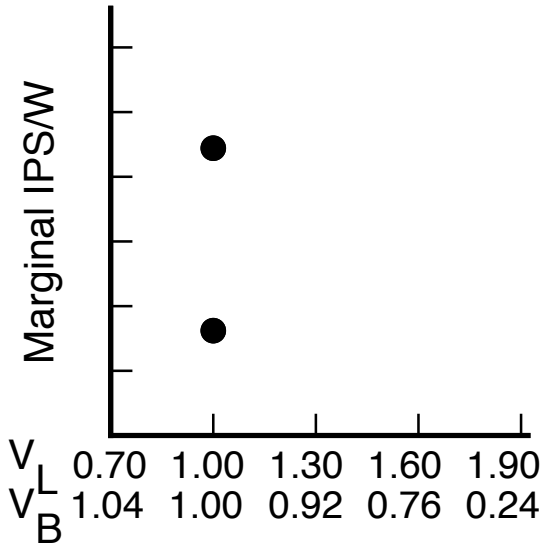
System with both big cores active and both little cores active

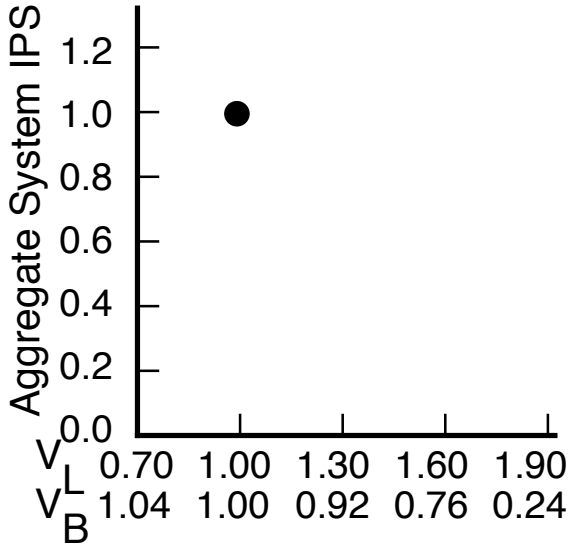
Work-Pacing: Building Intuition

Balance performance/power across cores in the high-parallel (HP) region









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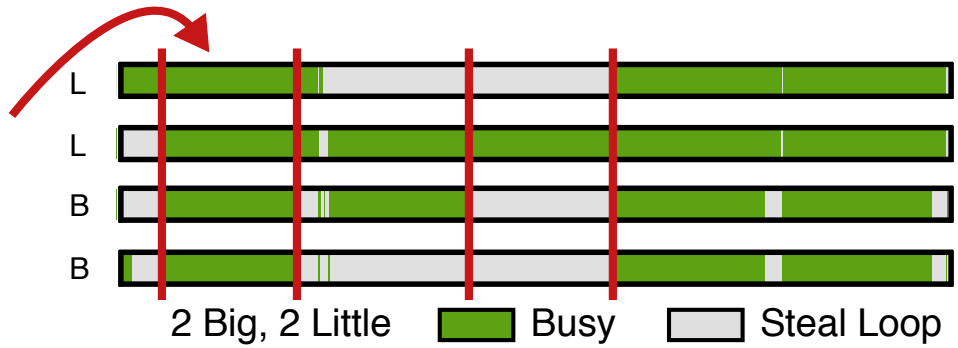
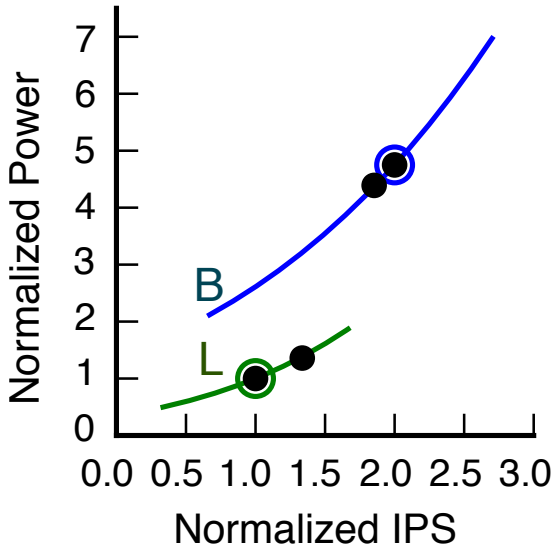
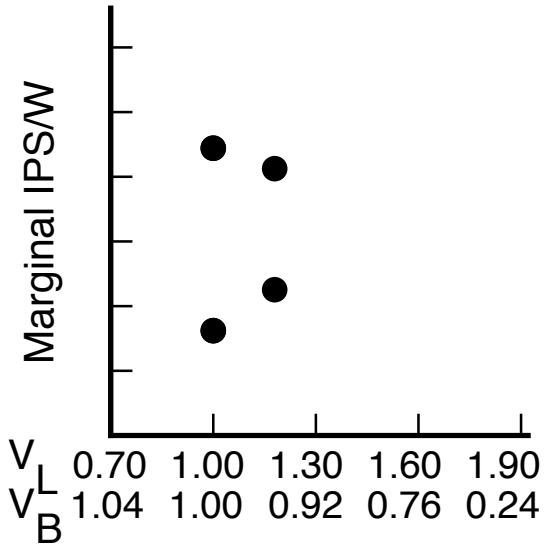
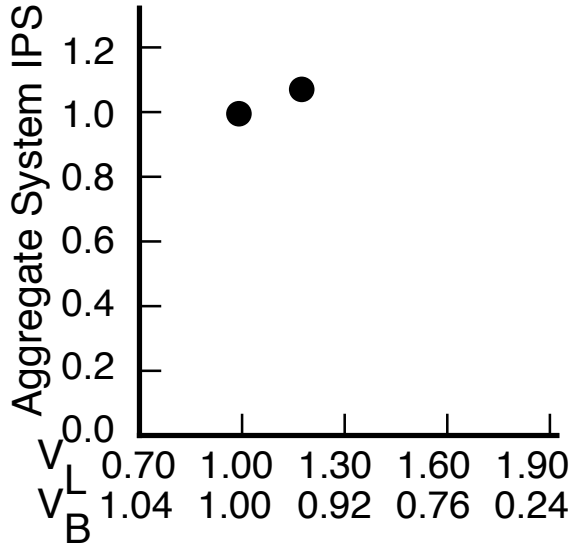




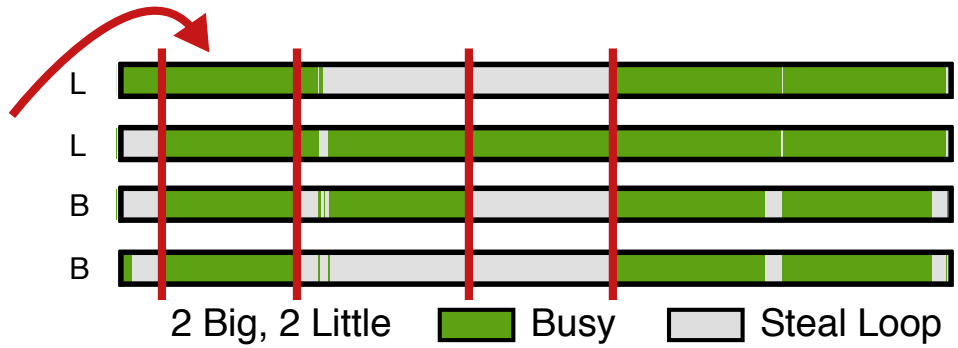


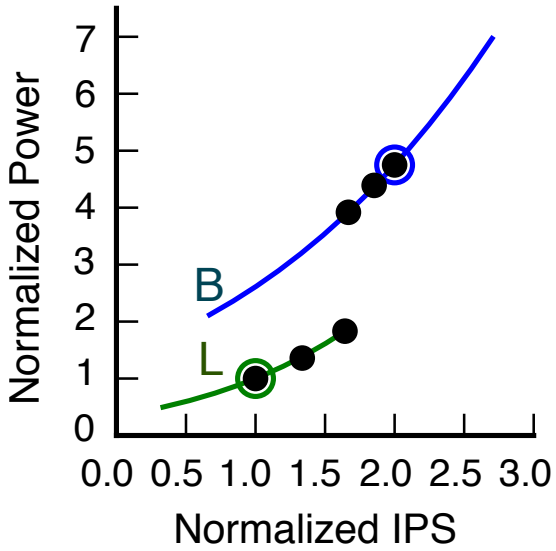


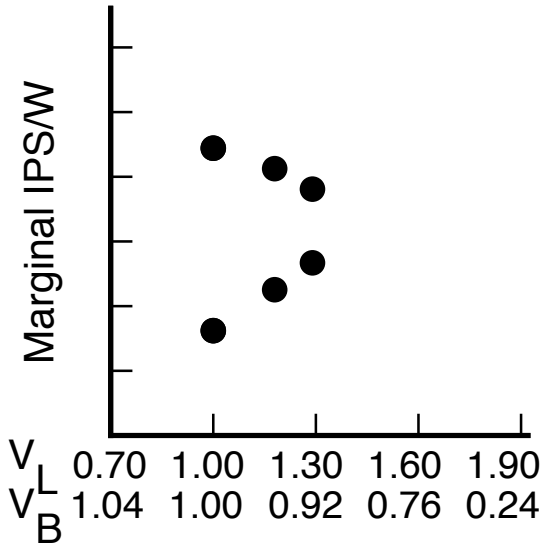
System with both big cores active and both little cores active

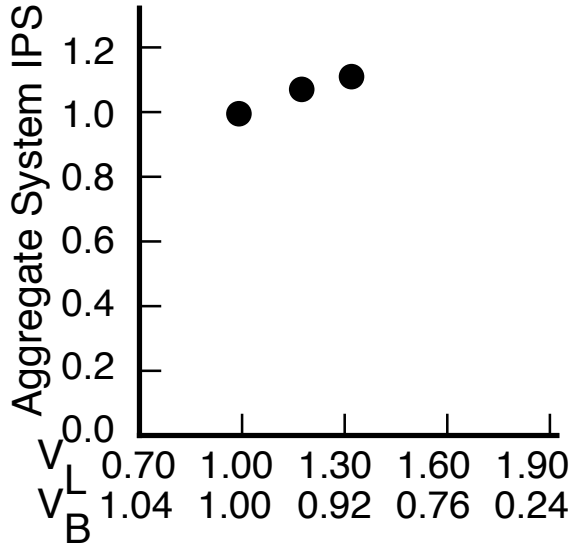
Work-Pacing: Building Intuition

Balance performance/power across cores in the high-parallel (HP) region





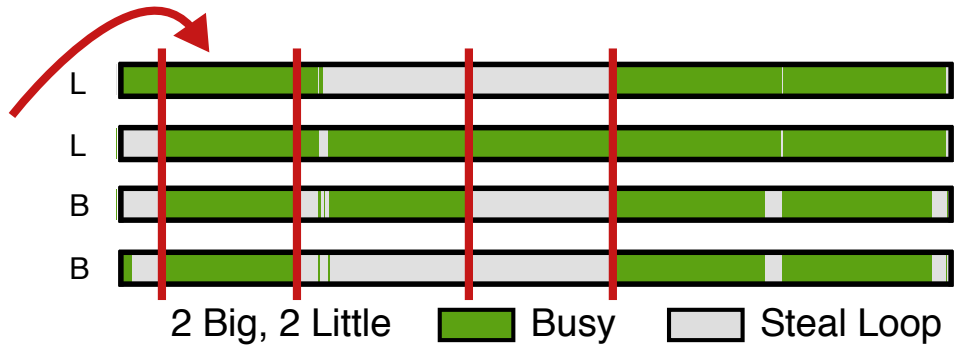


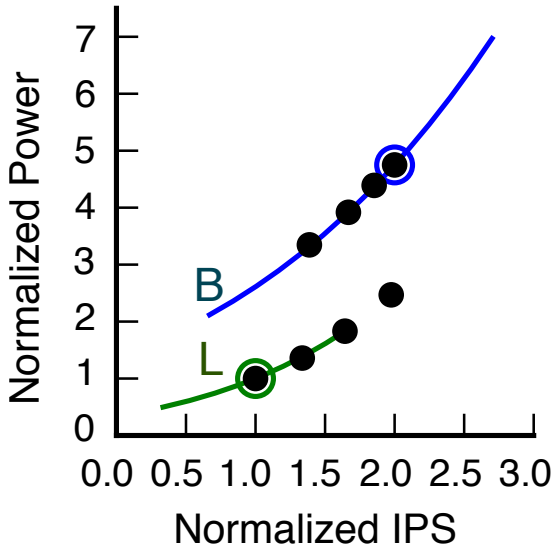


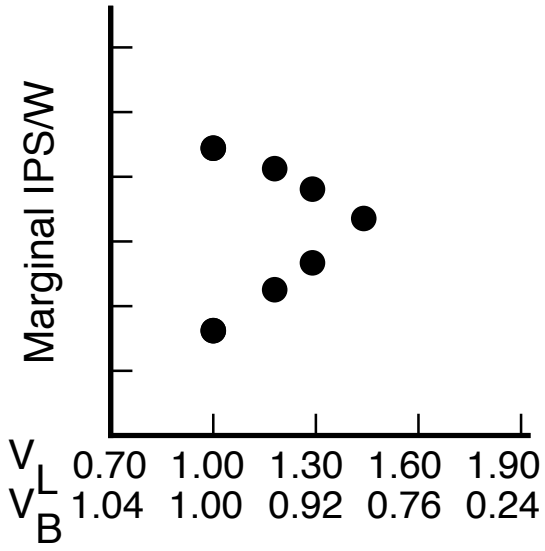
System with both big cores active and both little cores active

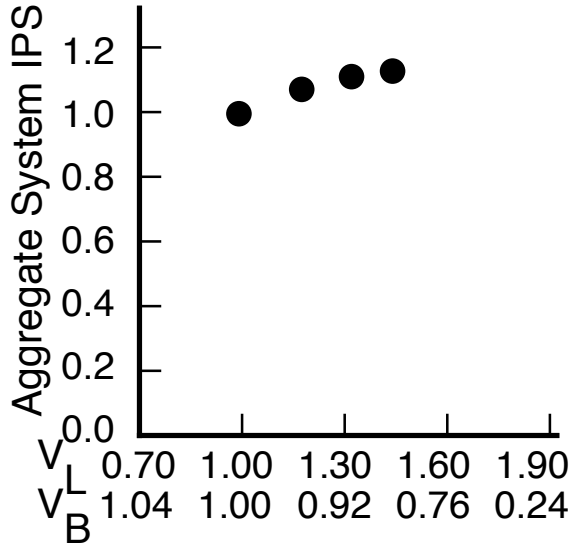
Work-Pacing: Building Intuition

Balance performance/power across cores in the high-parallel (HP) region





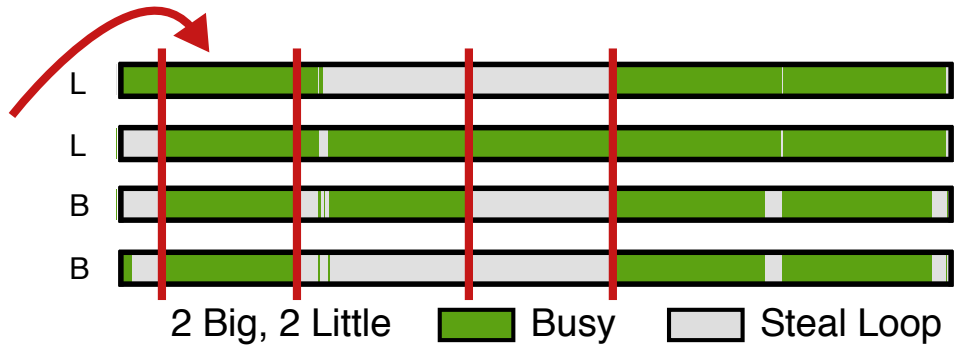


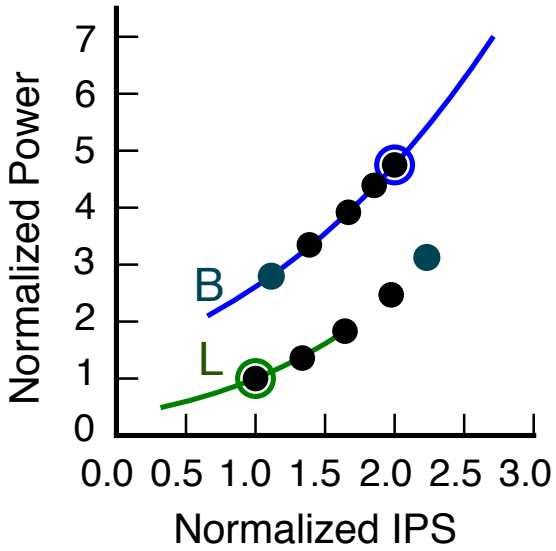


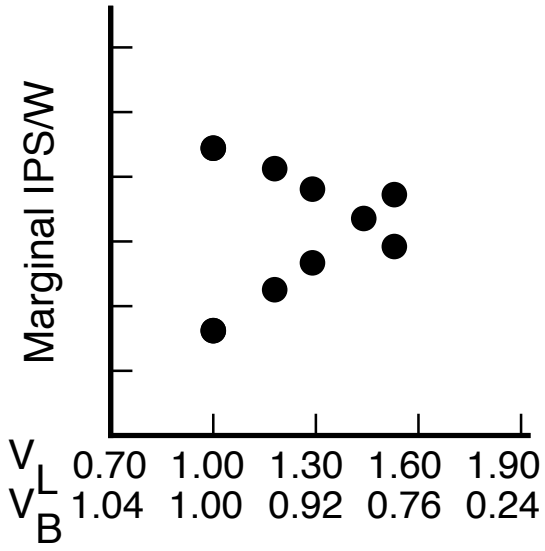
System with both big cores active and both little cores active

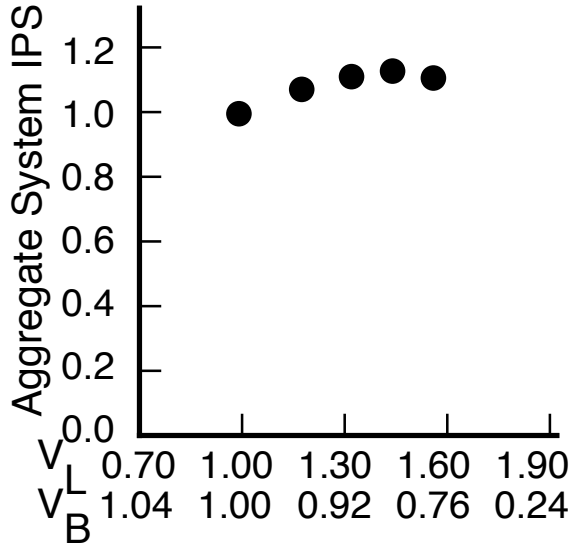
Work-Pacing: Building Intuition

Balance performance/power across cores in the high-parallel (HP) region





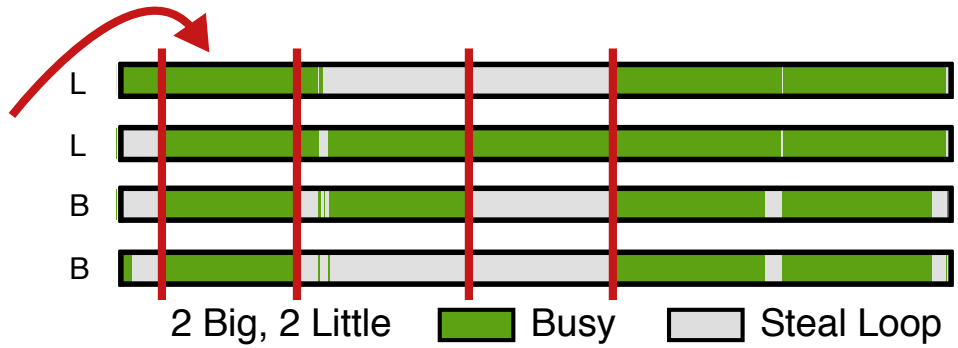


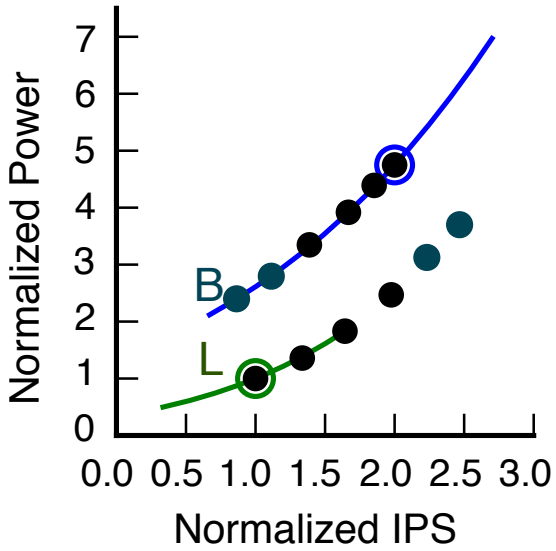


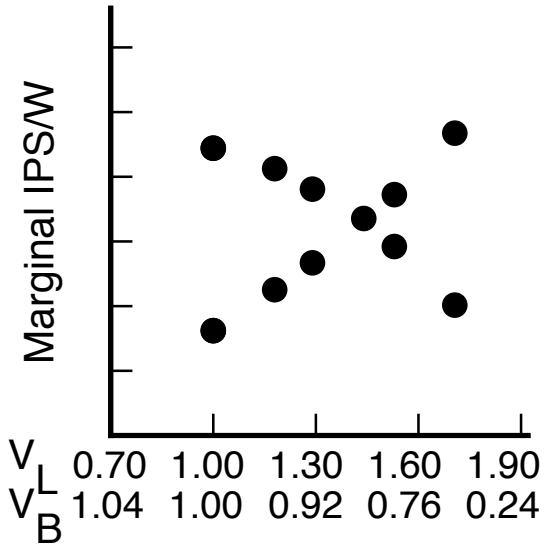
System with both big cores active and both little cores active

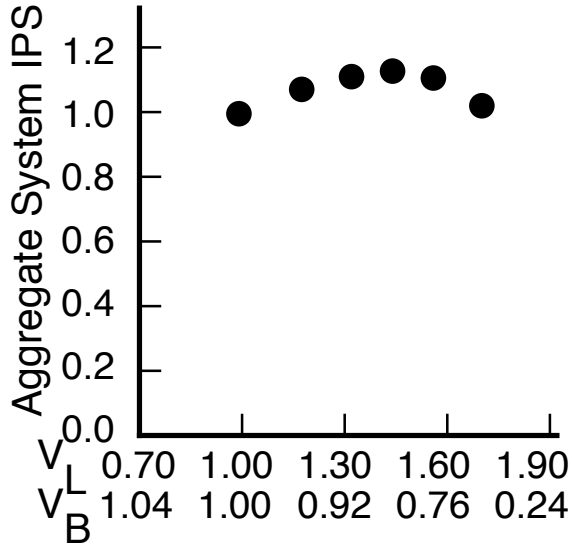
Work-Pacing: Building Intuition

Balance performance/power across cores in the high-parallel (HP) region





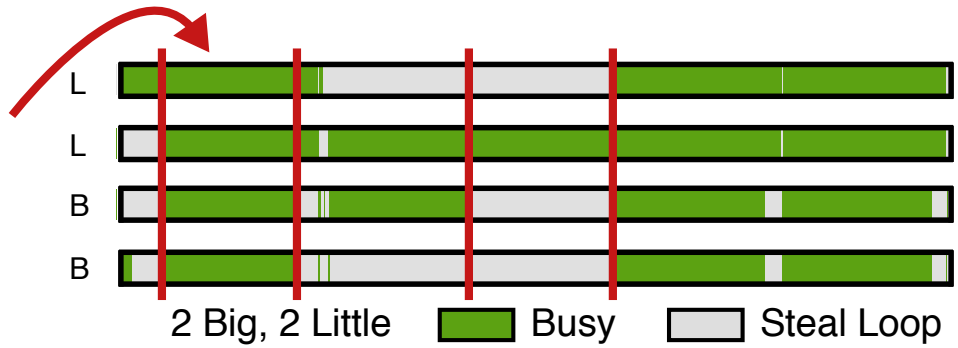


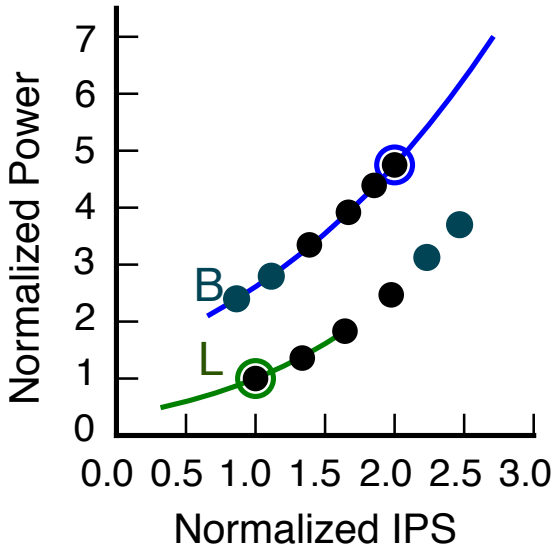


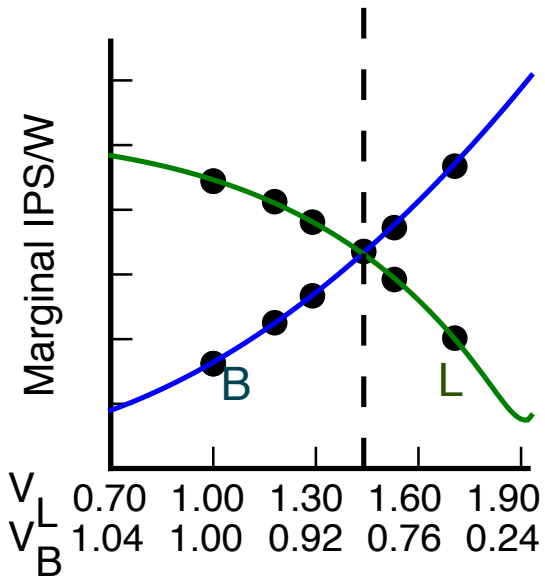
System with both big cores active and both little cores active

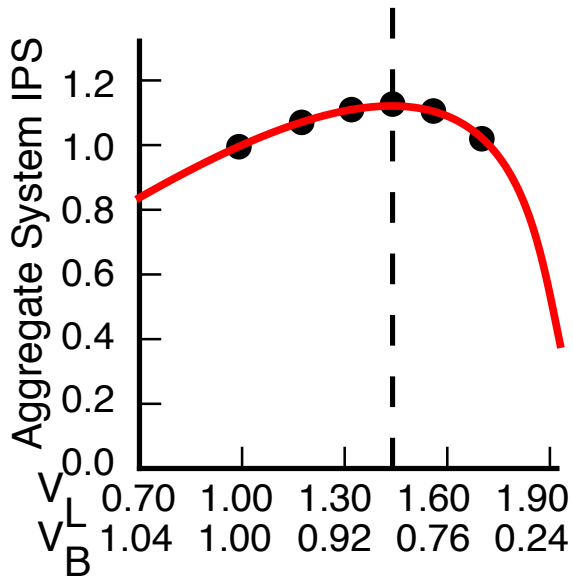
Work-Pacing: Building Intuition

Balance performance/power across cores in the high-parallel (HP) region





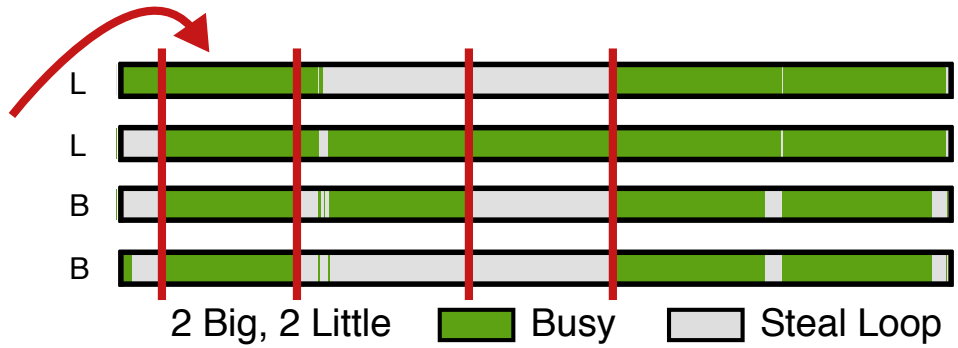


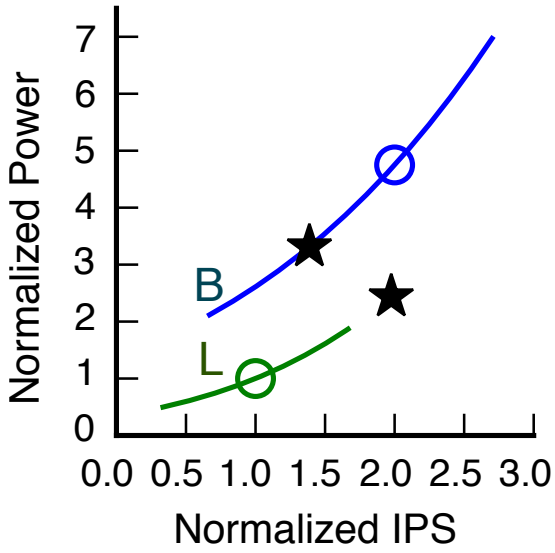


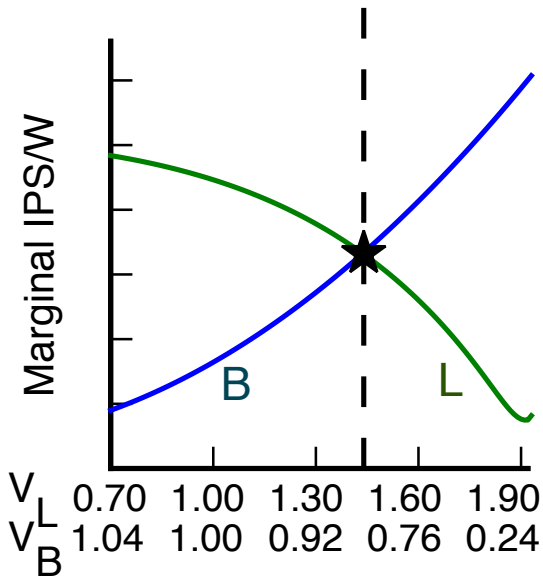
System with both big cores active and both little cores active

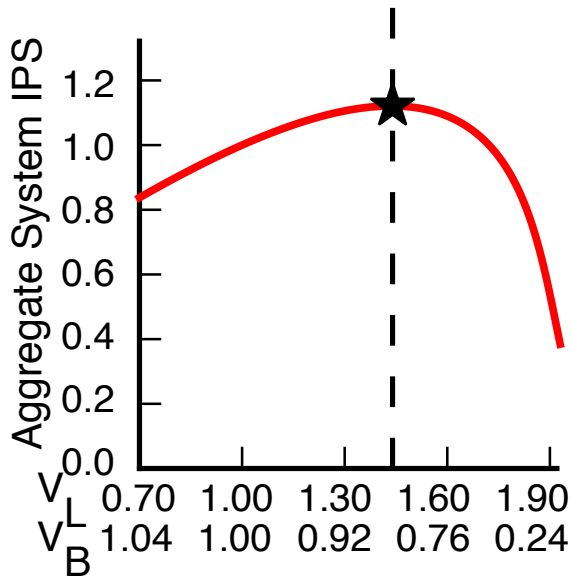
Work-Pacing: Building Intuition

Balance performance/power across cores in the high-parallel (HP) region



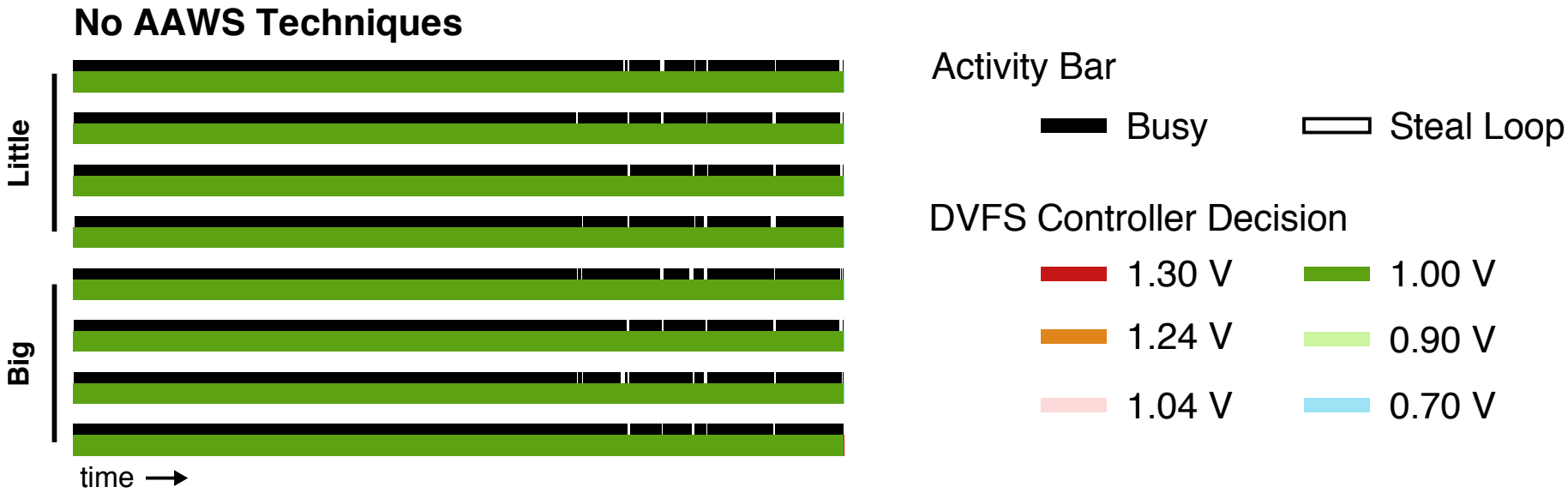




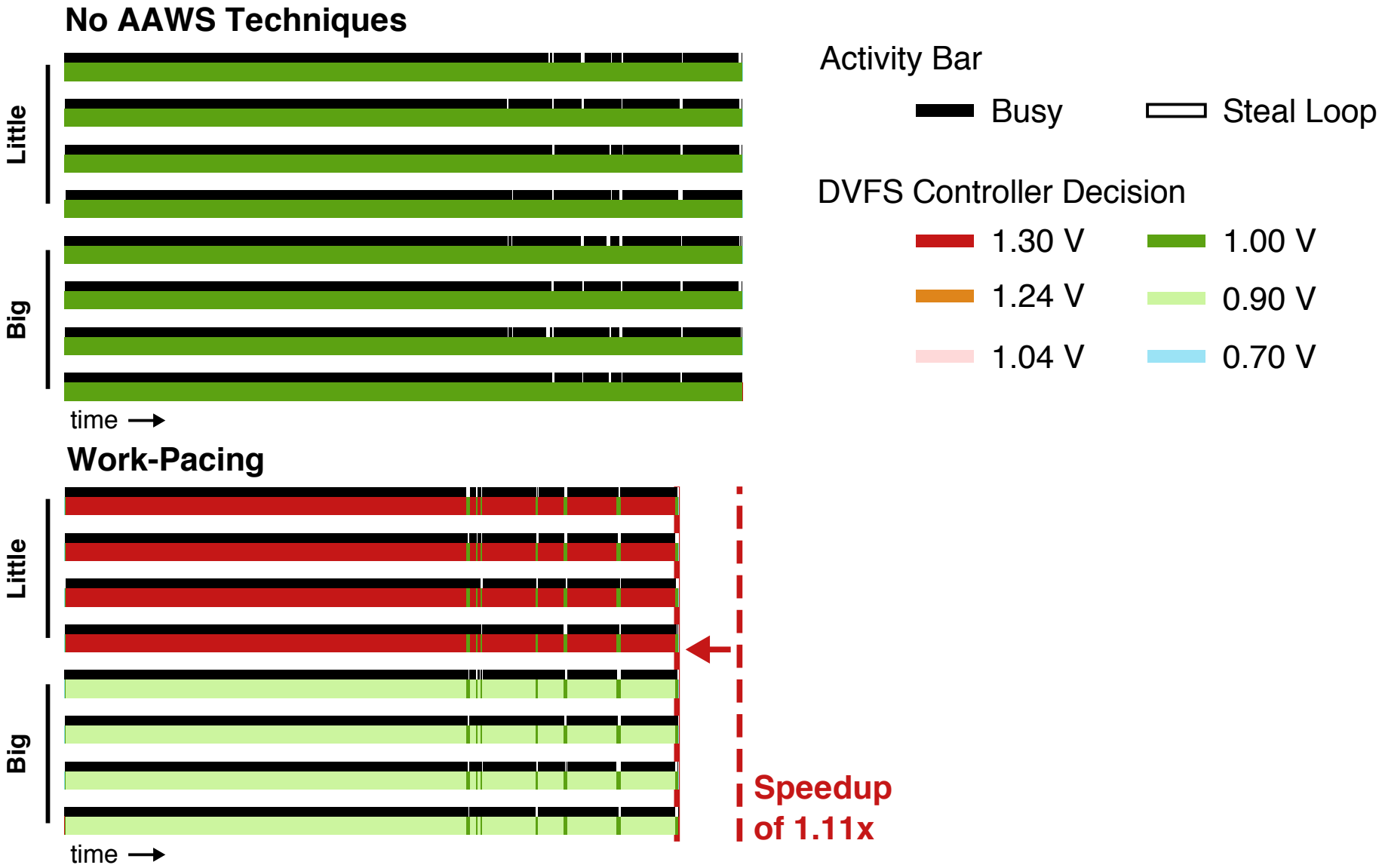


System with both big cores active and both little cores active

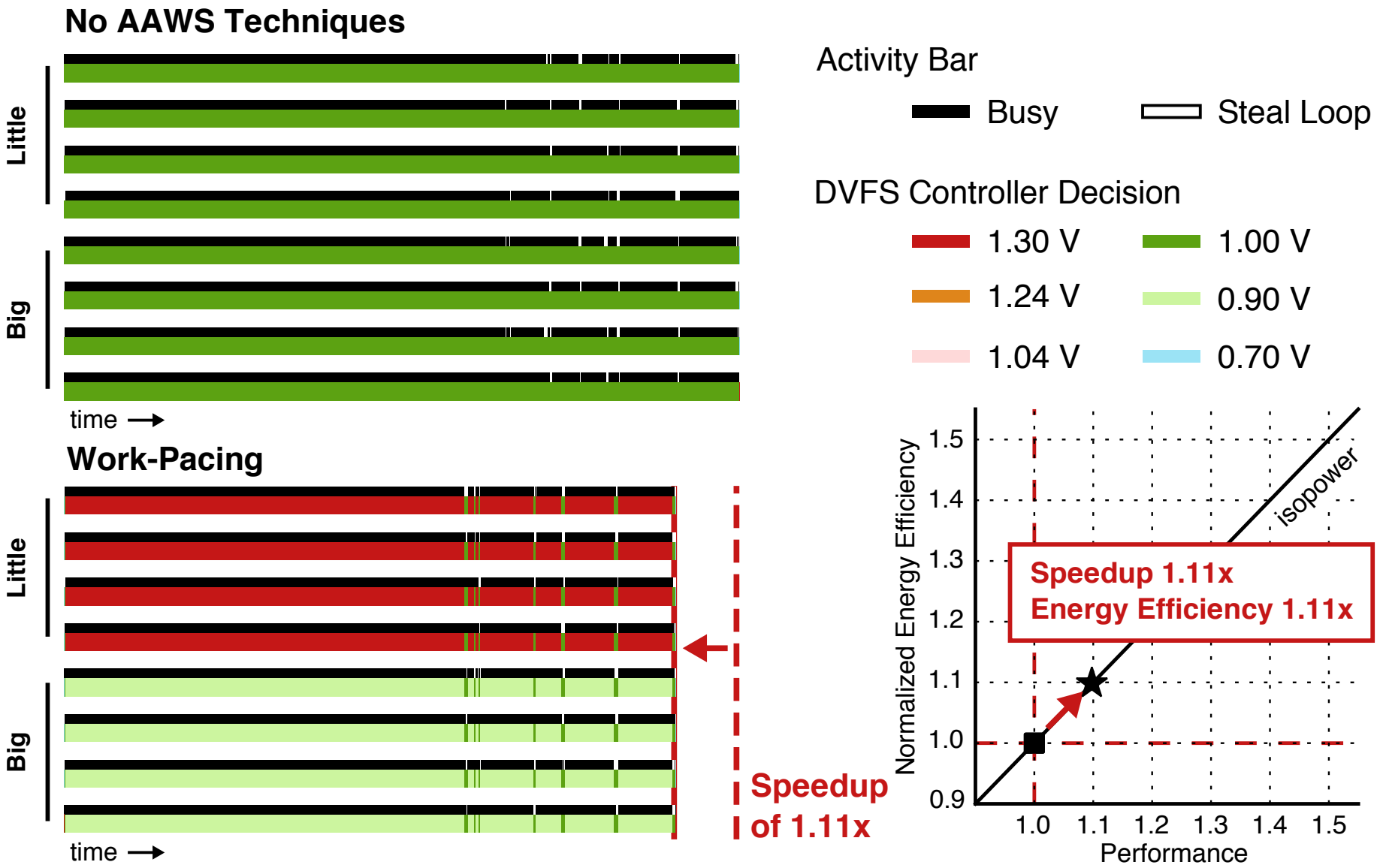
Work-Pacing in *cilk-sort*



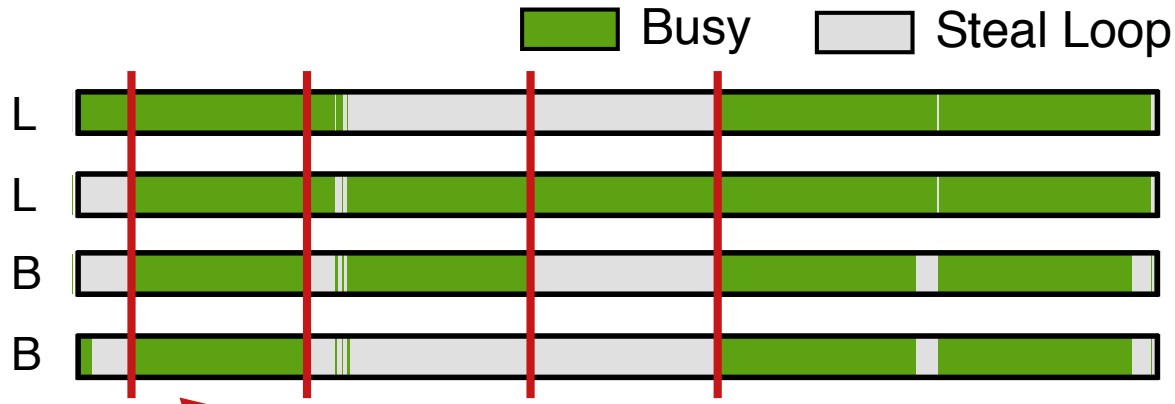
Work-Pacing in *cilk-sort*



Work-Pacing in *cilk-sort*



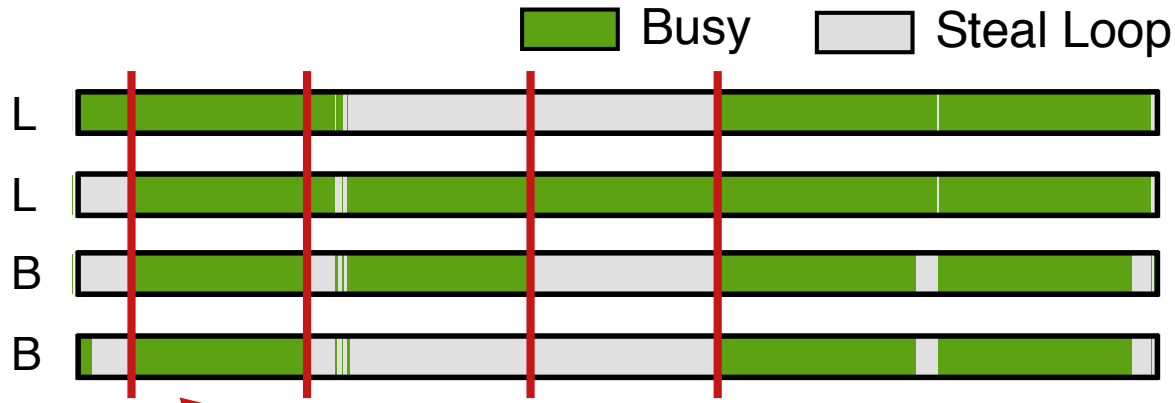
Work-Pacing, Work-Sprinting, and Work-Mugging



Work-Pacing

Balance performance/power across cores in the high-parallel (HP) region

Work-Pacing, Work-Sprinting, and Work-Mugging



Work-Pacing

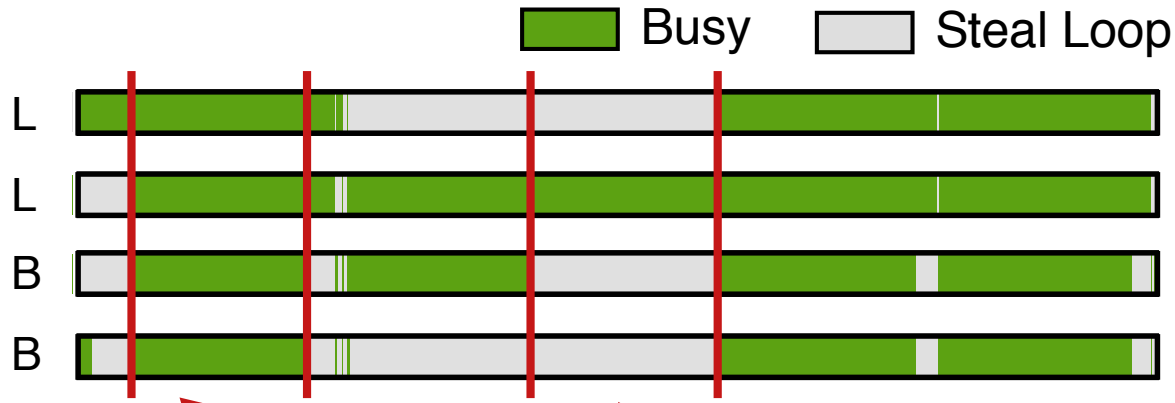
Balance performance/power across cores in the high-parallel (HP) region

Work-Sprinting

Rest cores in the steal loop to the lowest voltage

With additional power slack, balance performance/power across busy cores in the low-parallel (LP) region

Work-Pacing, Work-Sprinting, and Work-Mugging



Work-Pacing

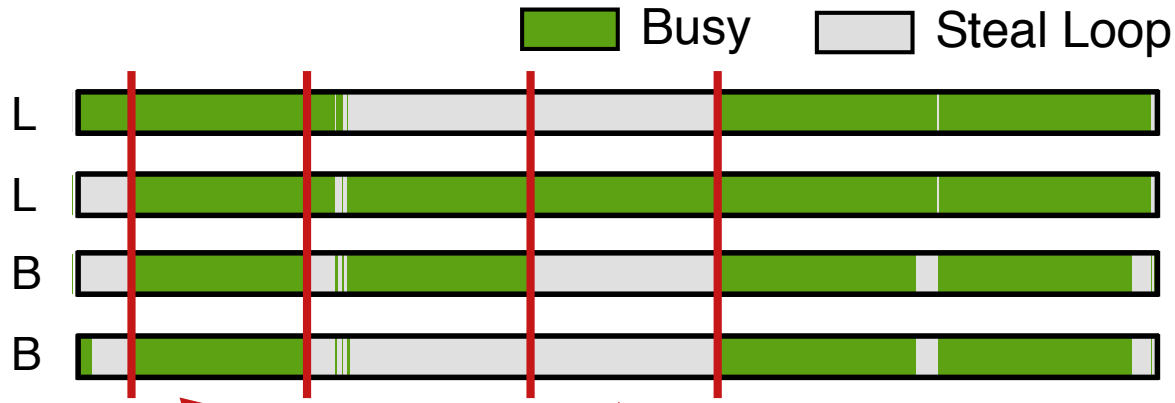
Balance performance/power across cores in the high-parallel (HP) region

Work-Sprinting

Rest cores in the steal loop to the lowest voltage

With additional power slack, balance performance/power across busy cores in the low-parallel (LP) region

Work-Pacing, Work-Sprinting, and Work-Mugging



Work-Pacing

Balance performance/power across cores in the high-parallel (HP) region

Work-Sprinting

Rest cores in the steal loop to the lowest voltage

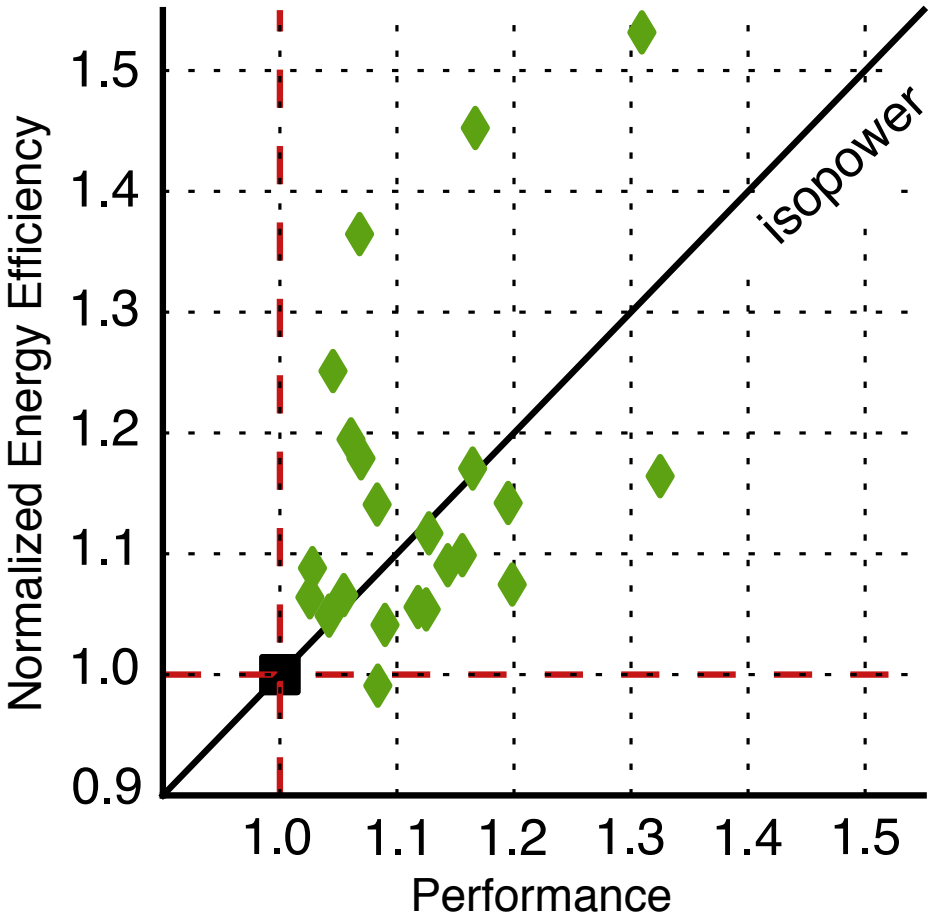
With additional power slack, balance performance/power across busy cores in the low-parallel (LP) region

Work-Mugging

Move work from slow little cores to fast big cores in the low-parallel (LP) region

Inspired by theoretical work - Bender et al. Theory of Computing '02

Evaluation of Complete AAWS Runtime

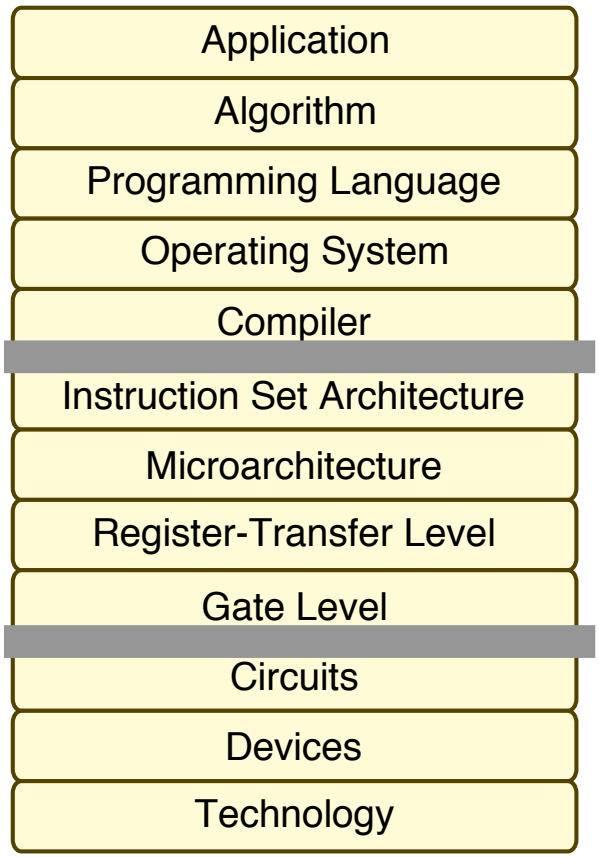


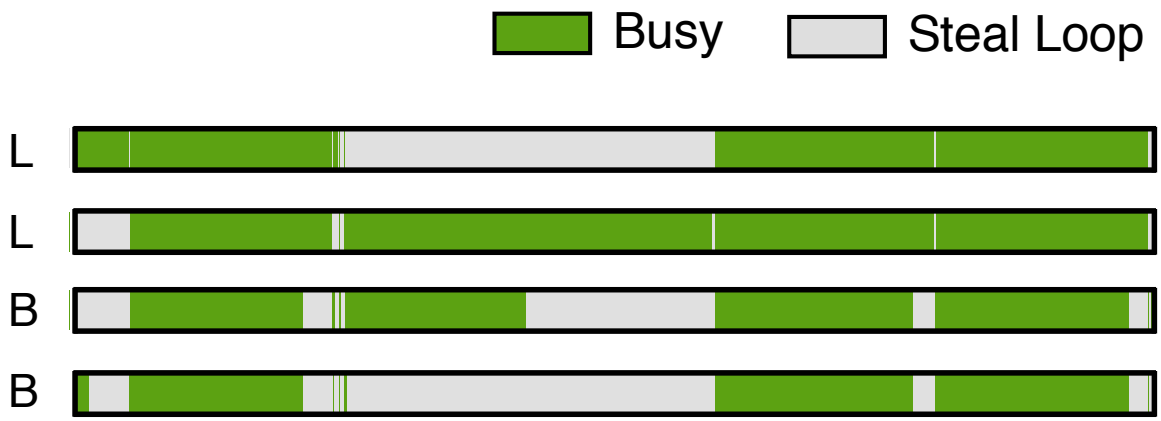
Application Kernels

- pbbs-bfs
- pbbs-quicksort
- pbbs-samplesort
- pbbs-dictionary
- pbbs-convex-hull
- pbbs-radix-sort
- pbbs-knn
- pbbs-max-independent-set
- pbbs-nbody
- pbbs-remove-duplicates
- pbbs-suffix-array
- pbbs-spanning-tree
- cilk-cholesky
- cilk-cilksort
- cilk-heat
- cilk-knapsack
- cilk-matrix-multiply
- parsec-blackscholes
- unbalanced-tree-search

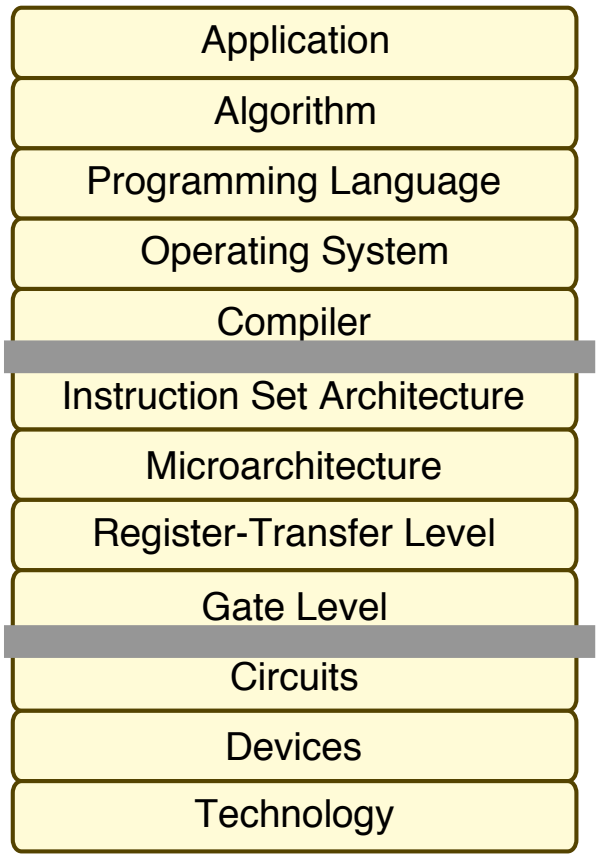
Performance	Median: 1.10 x	Max: 1.32 x
Energy Efficiency	Median: 1.11 x	Max: 1.53 x

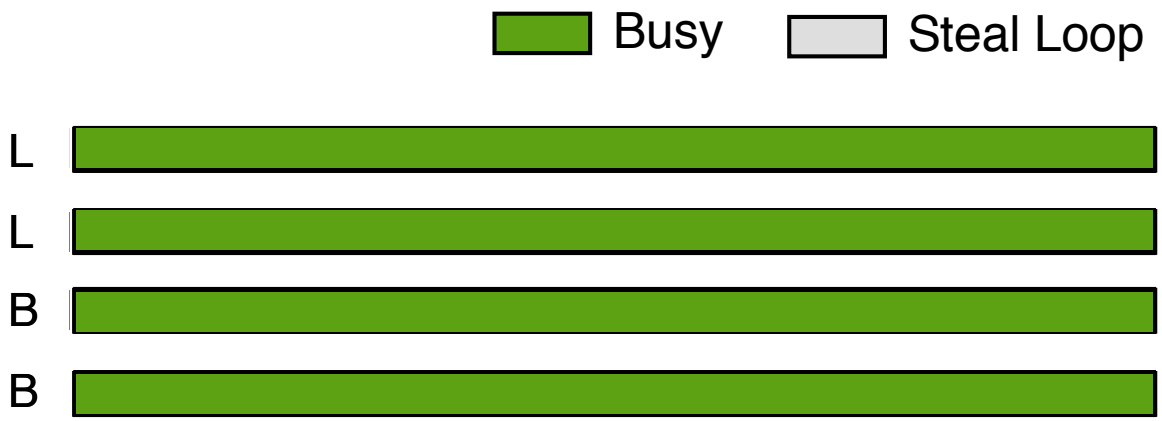
Augmenting the Software/Architecture Interface



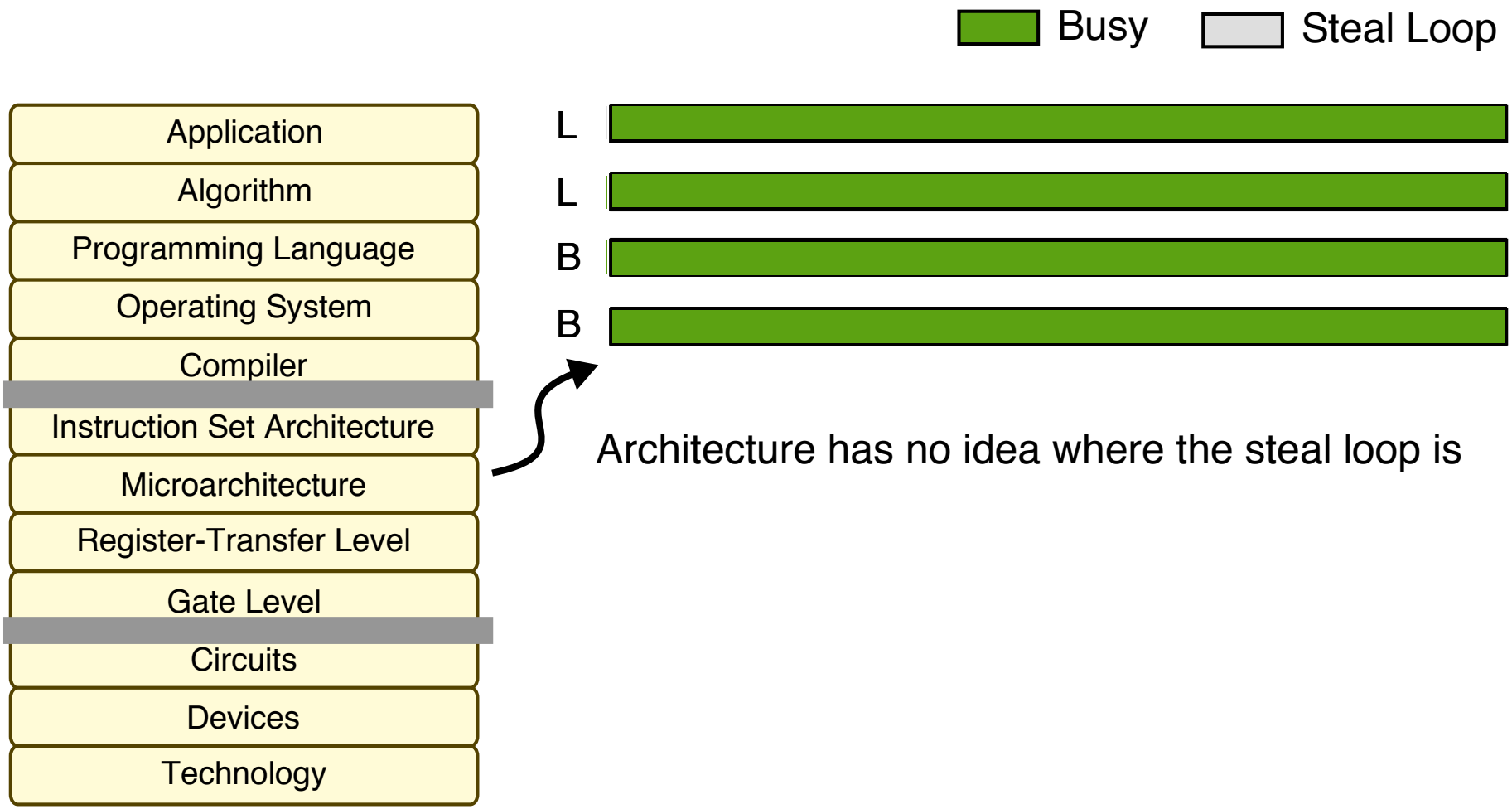


Augmenting the Software/Architecture Interface

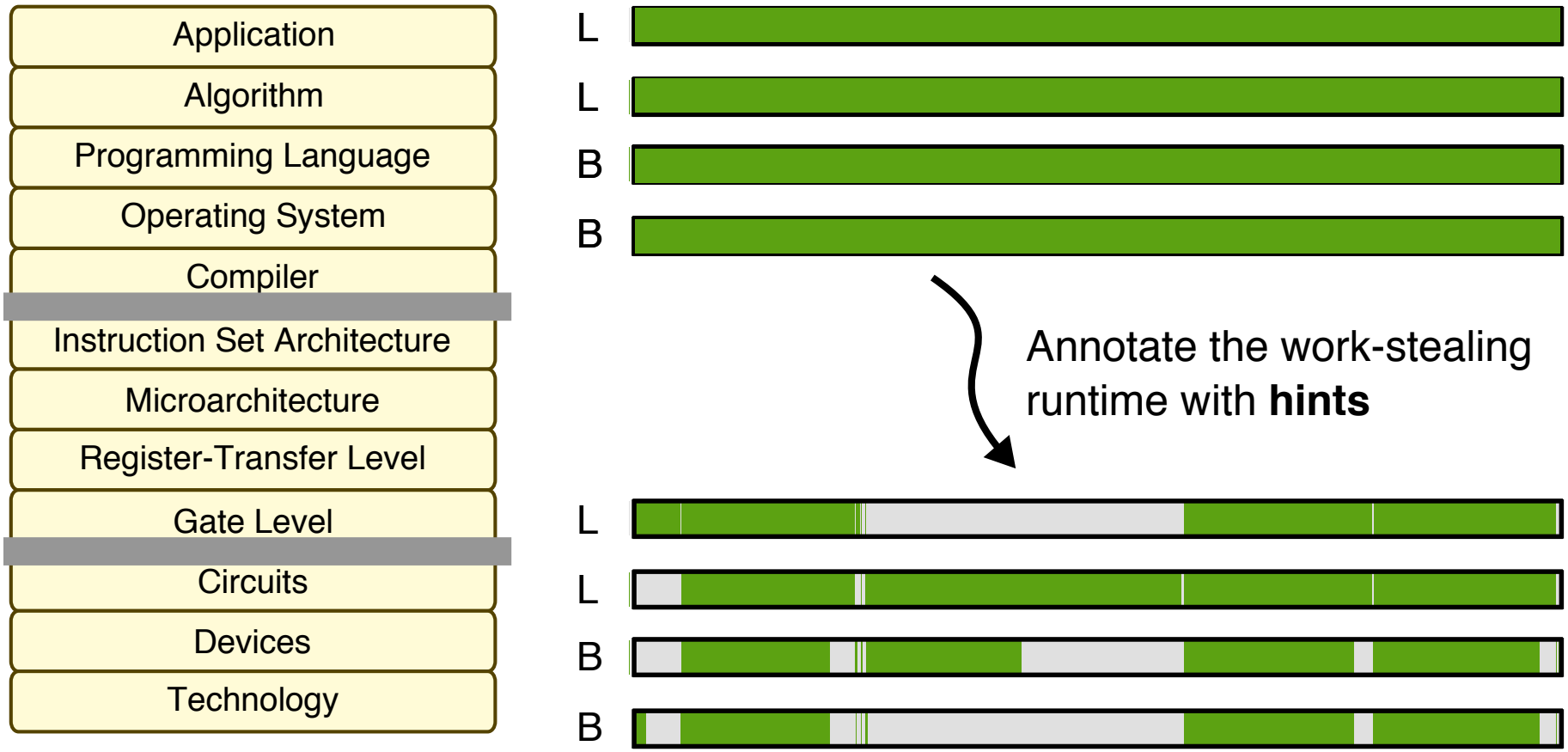




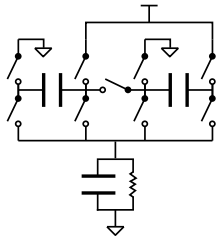
Augmenting the Software/Architecture Interface



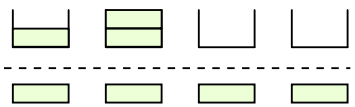
Augmenting the Software/Architecture Interface



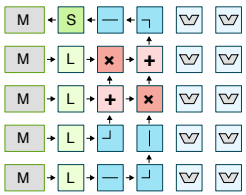
Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry



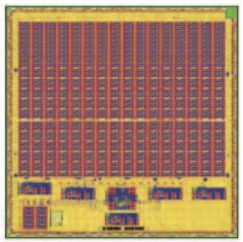
Exploiting Fine-Grain Asymmetry with
On-Chip Voltage Regulation - **MICRO'14**, IEEE TCAS I'18



Exploiting Fine-Grain Asymmetry in
Task-Based Parallel Runtimes - **ISCA'16**, MICRO'17, RISCV'18



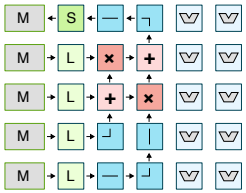
Exploiting Fine-Grain Asymmetry in
Coarse-Grain Reconfigurable Arrays - **Unpublished**



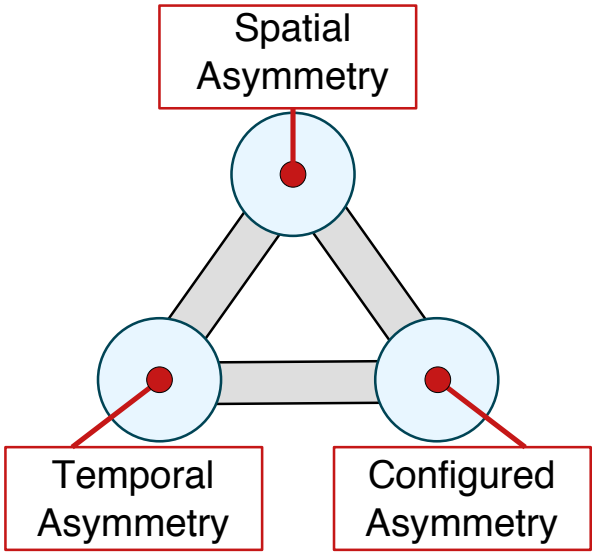
Exploiting Fine-Grain Asymmetry with
Silicon Prototyping - **IEEE MICRO'18**, DAC'18, Hotchips'17

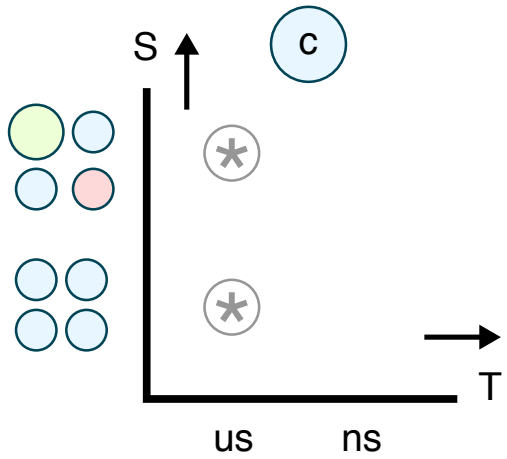
Conclusion

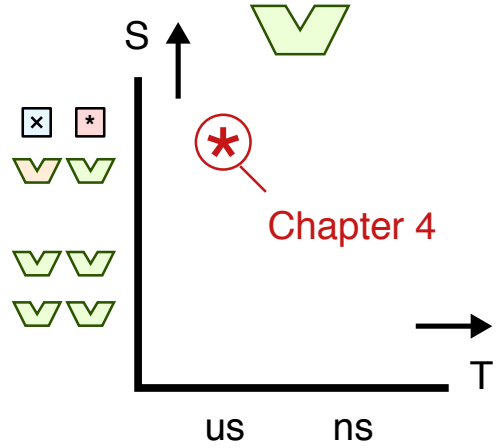
Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry



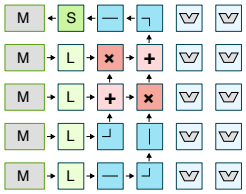
Exploiting Fine-Grain Asymmetry in **Coarse-Grain Reconfigurable Arrays** - Unpublished







Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry



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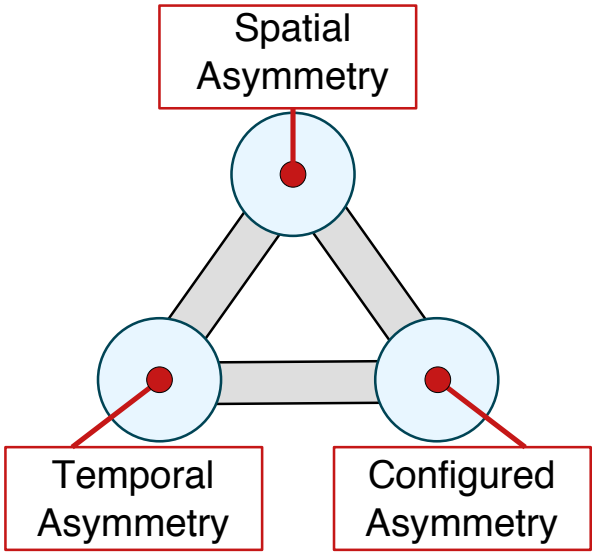
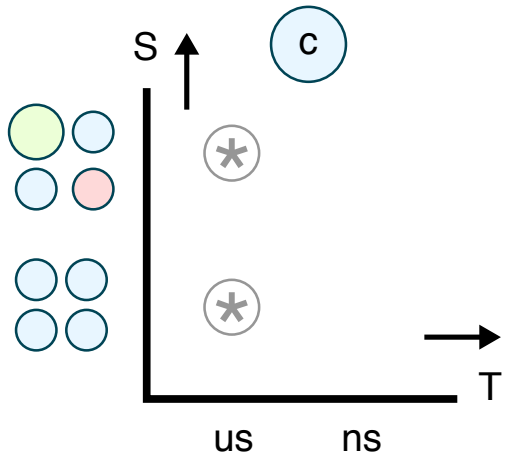
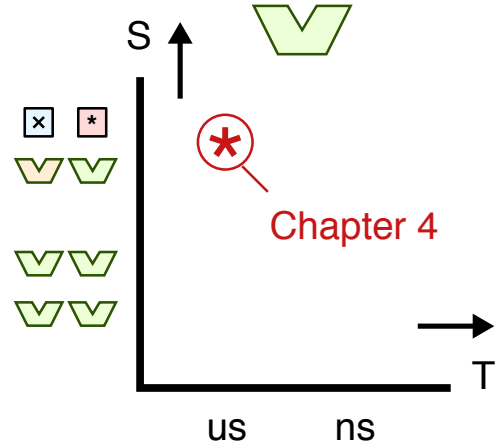
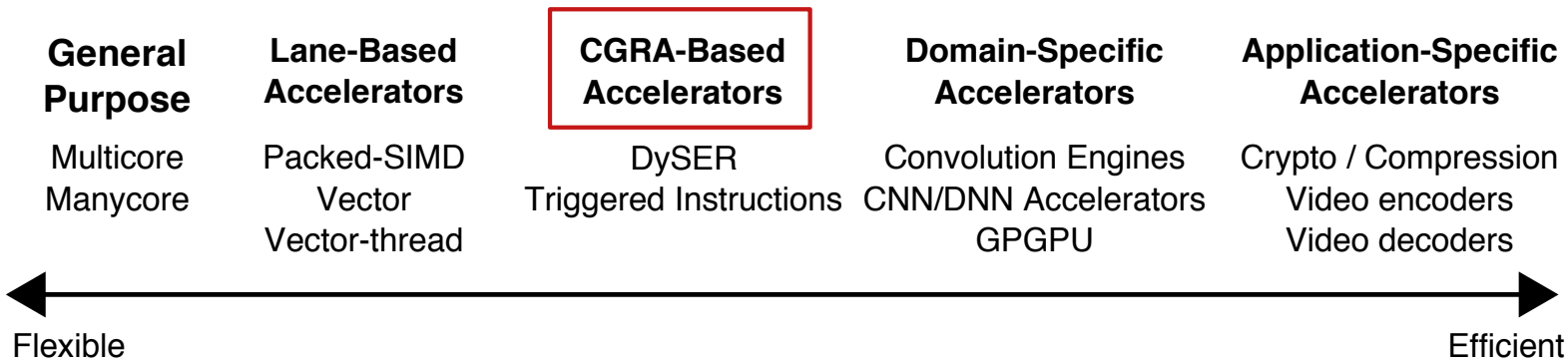






Research Question – Can we leverage fine-grain power-control techniques to optimize CGRAs at configure time?

Coarse-Grain Reconfigurable Arrays (CGRAs)



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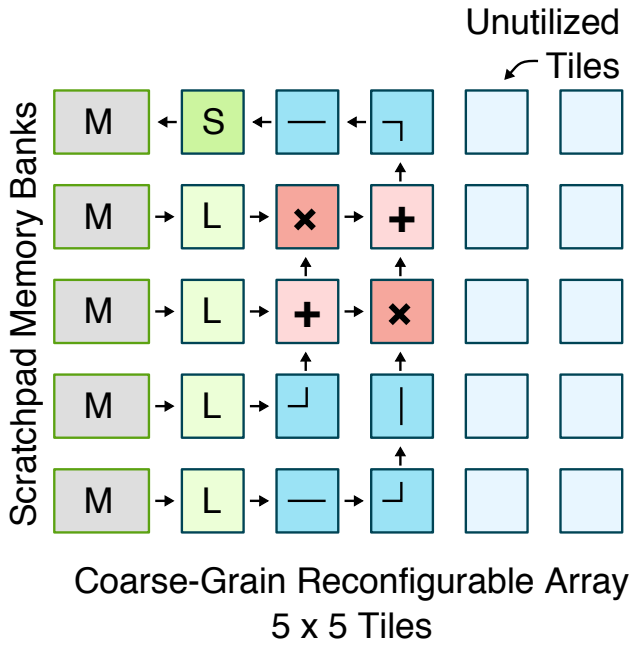

See also: Mei et al. "ADRES", FPL 2003

General Purpose	Lane-Based Accelerators	CGRA-Based Accelerators	Domain-Specific Accelerators	Application-Specific Accelerators
Multicore Manycore	Packed-SIMD Vector Vector-thread	DySER Triggered Instructions	Convolution Engines CNN/DNN Accelerators GPGPU	Crypto / Compression Video encoders Video decoders

Flexible ⟷ Efficient

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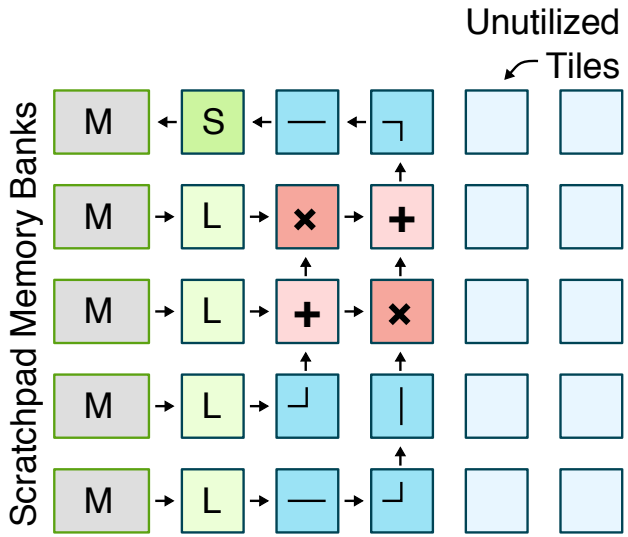

Data movement is more energy-consuming than computation, especially for deep learning

Chen et al. JSSC'16 "Eyeriss..."

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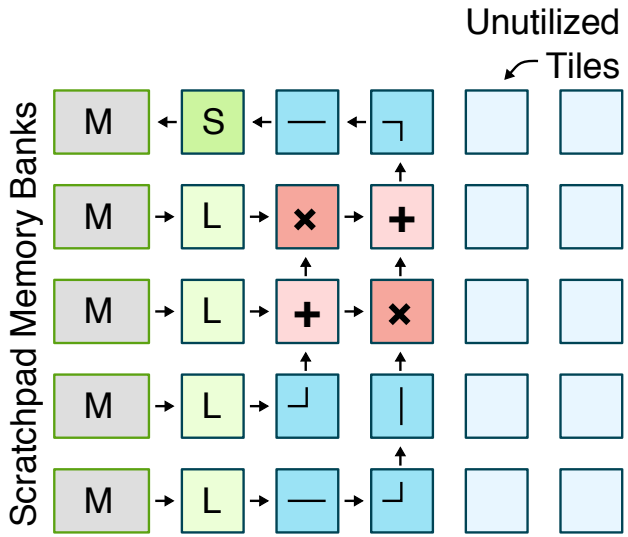

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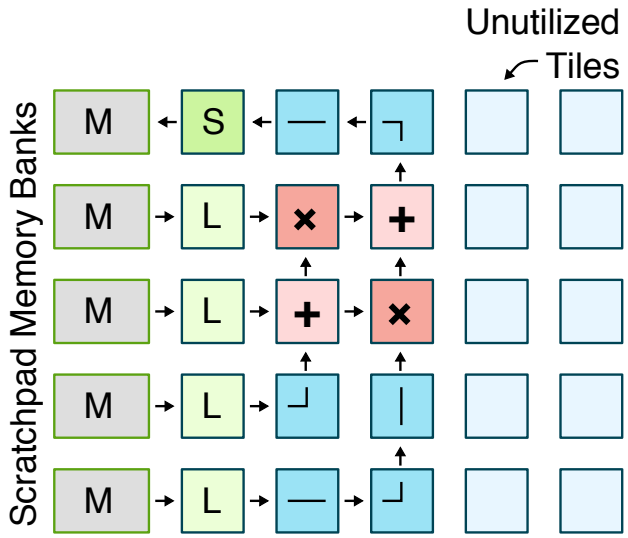

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CGRAs can efficiently map flexible workloads beyond those suitable for deep learning accelerators

Fan et al. TVLSI'18
"Dual-Track CGRA for Object Inference"

See also: Mei et al. "ADRES", FPL 2003

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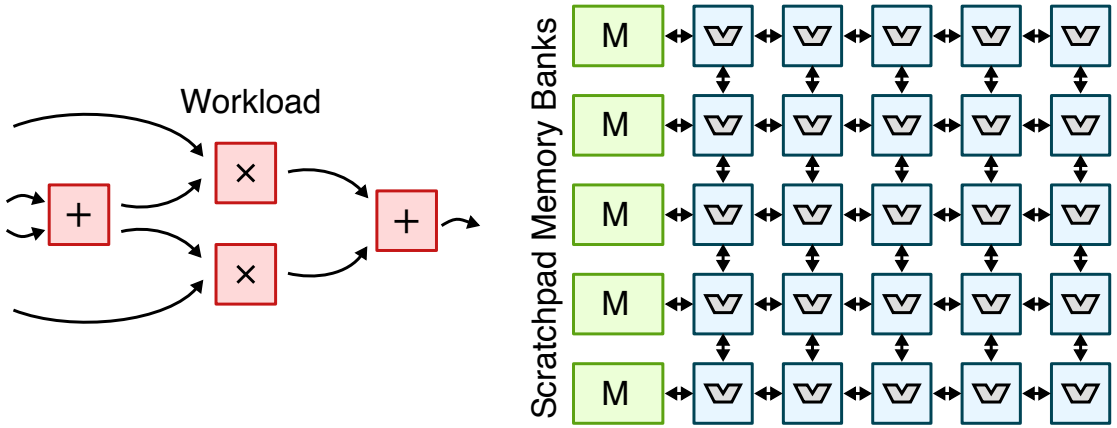
Key Challenges Facing CGRAs

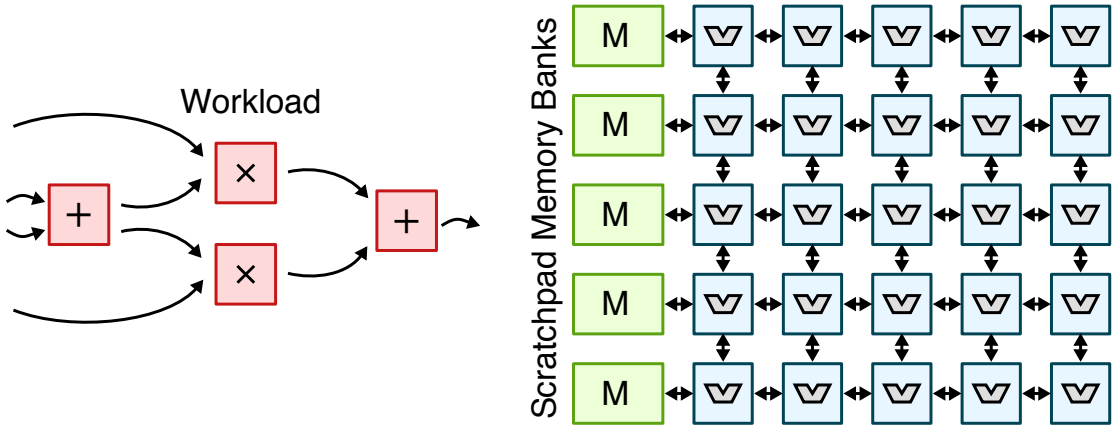


Key Challenge #1 – CGRA compilers must manage *complexity* with

- Resource constraints (routing, functional units, heterogeneity)
- Support for predication
- Dynamic timing behavior unknown at compile time
- Efficient targeting of kernels with high reuse (avoid reconfiguration)
- Over both space and time

See: HPCA'16, HPCA'11, IEEEMICRO'12, LCTES'09, TCAD'18, FPGA'13, FPL'03, FPL'96

Key Challenges Facing CGRAs



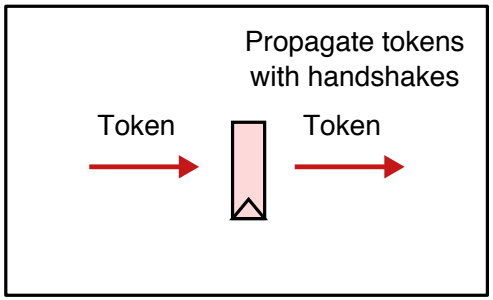
Key Challenge #2 – Complex compilers must optimize *utilization* with

- Abundant physical resources
- Potential heterogeneity across tiles
- Targeting kernels with high utilization (use more of the array)
- Over both space and time

See: HPCA'16, HPCA'11, IEEEMICRO'12, LCTES'09, TCAD'18, FPGA'13, FPL'03, FPL'96

Elastic CGRAs – Huang et al. FPGA 2013

Elastic Buffers



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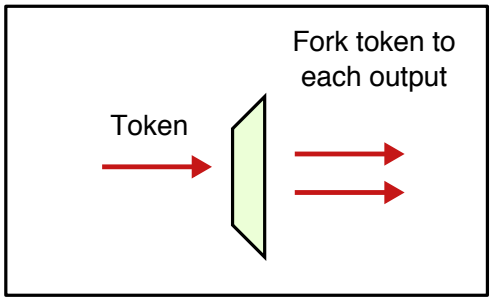

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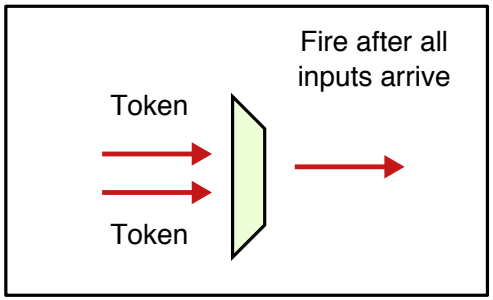
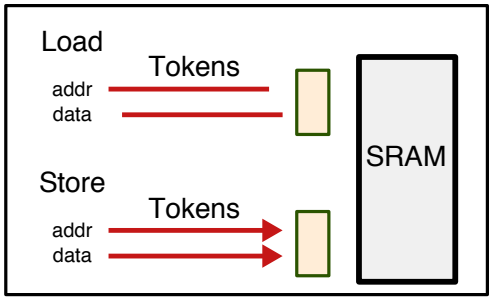
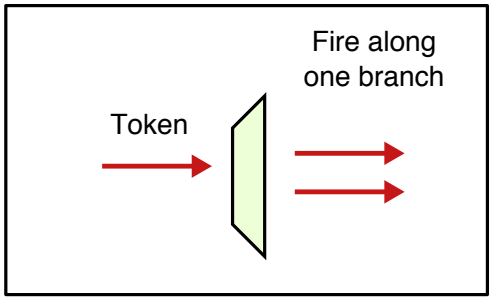


Memory Interfaces



Branch



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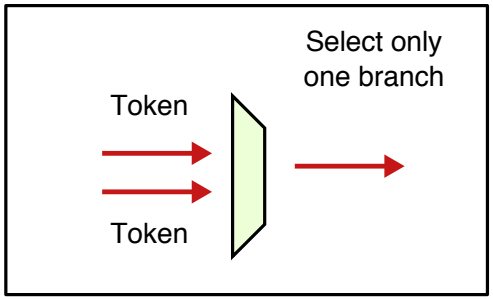

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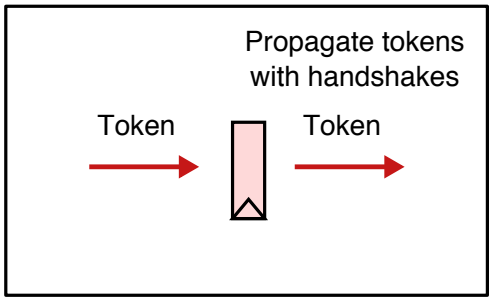

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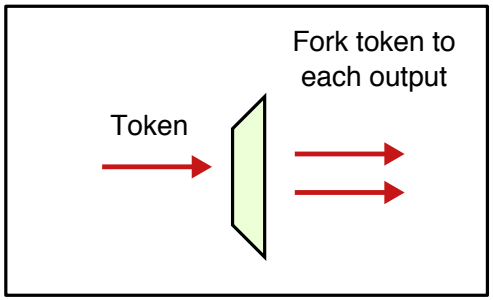

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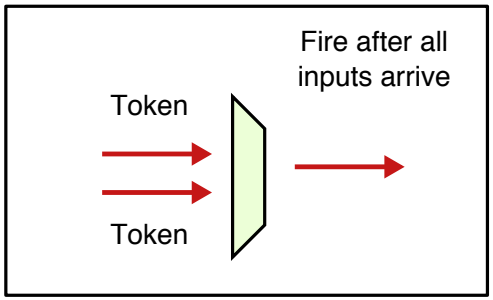

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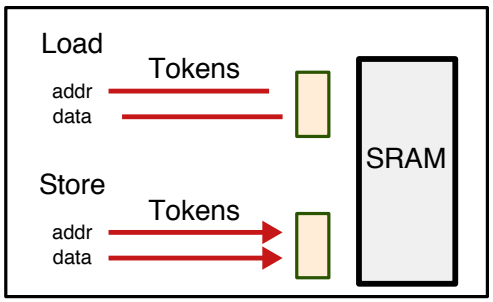

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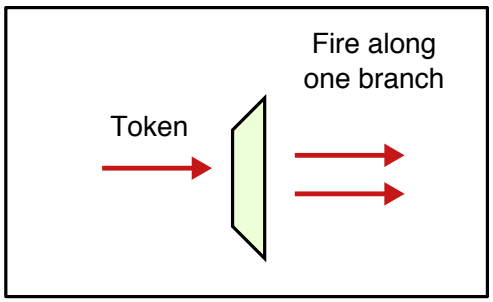

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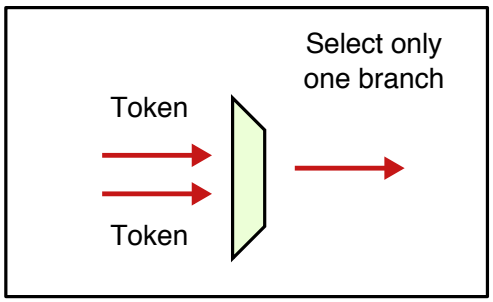

Hardware-managed elastic control flow can drastically simplify compiler complexity

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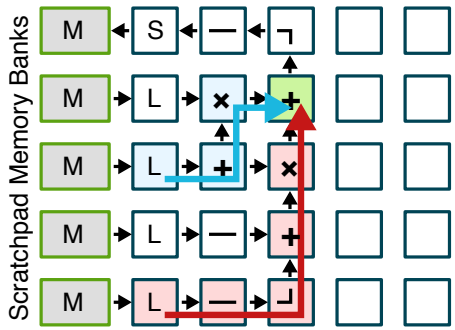

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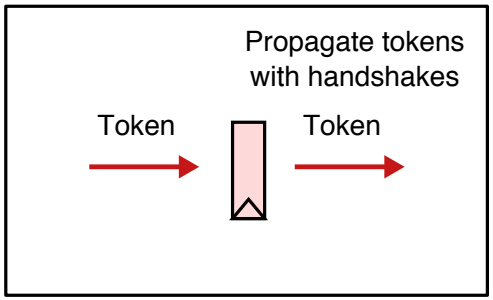

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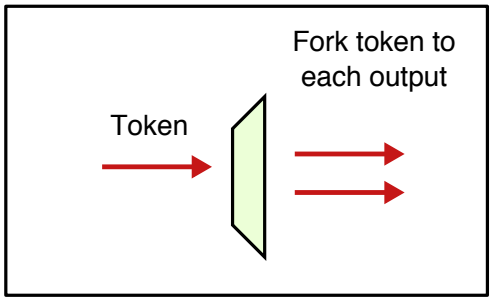

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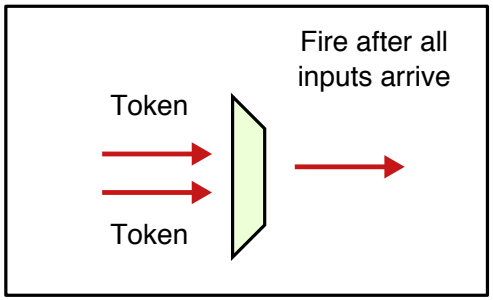

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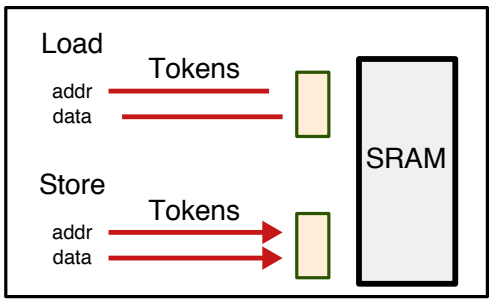

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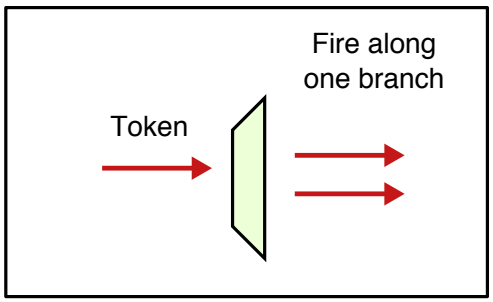

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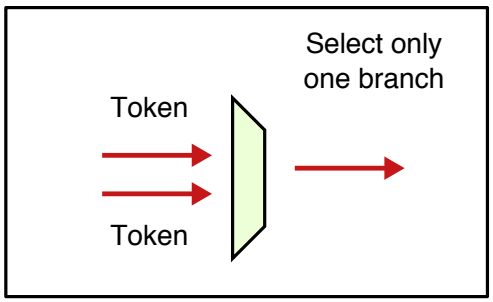

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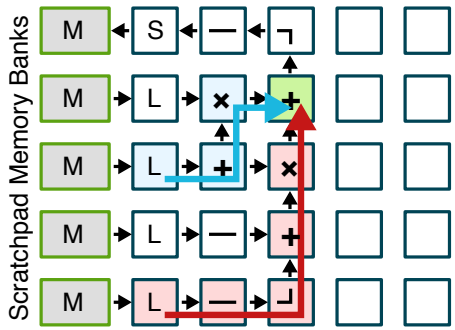
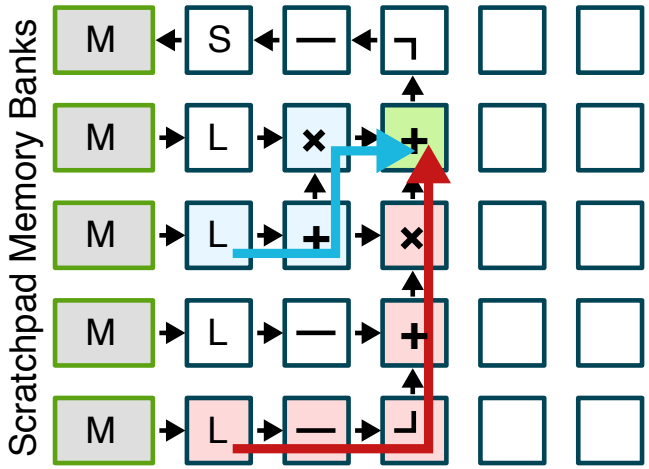
Two other examples of elasticity in CGRAs

Govindaraju et al. [HPCA'11] Fan et al. [TVLSI'18]



Fine-Grain Power Control Challenges

Can we use fine-grain DVFS to optimize execution on an elastic CGRA?



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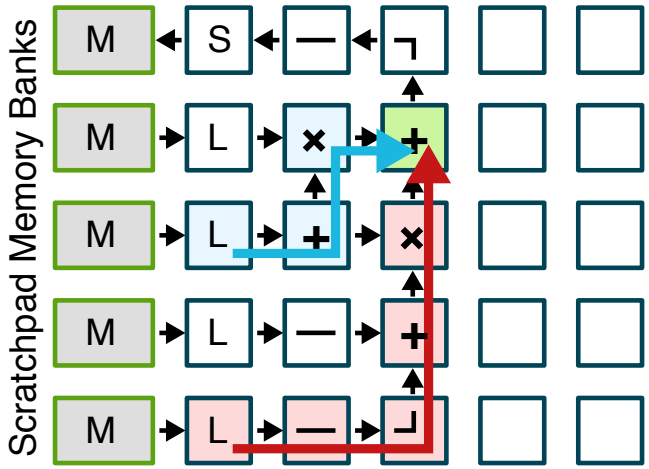

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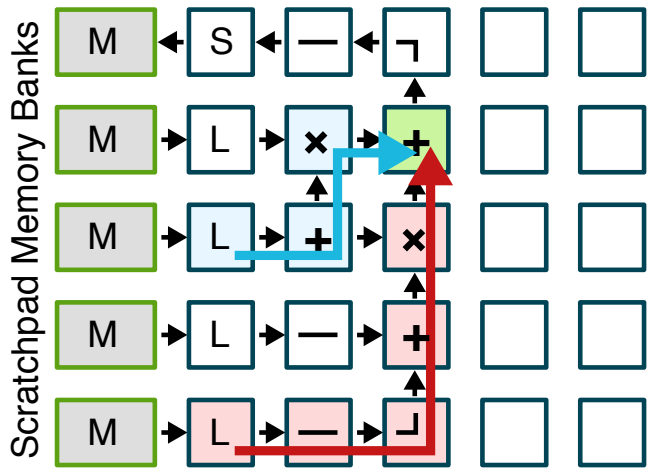

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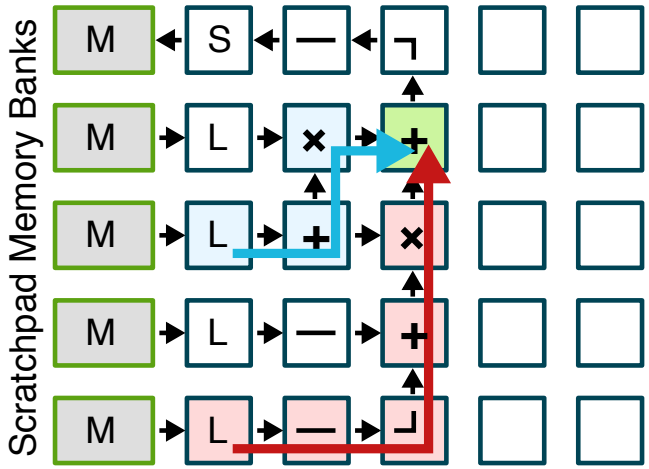

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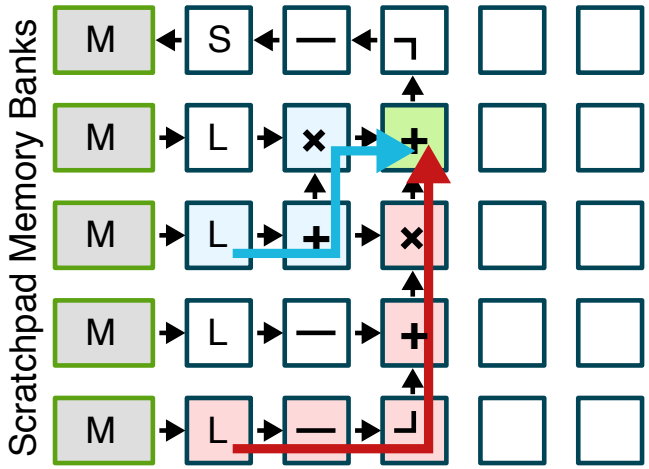

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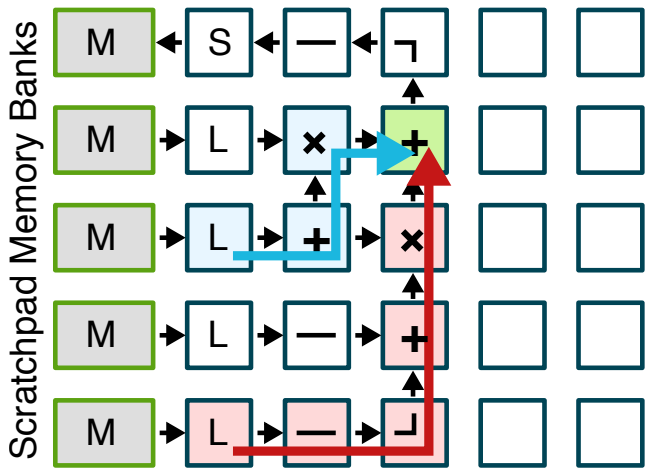

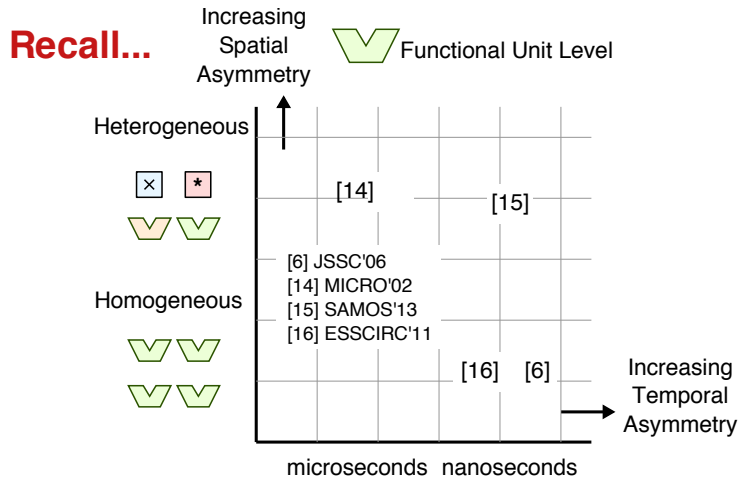

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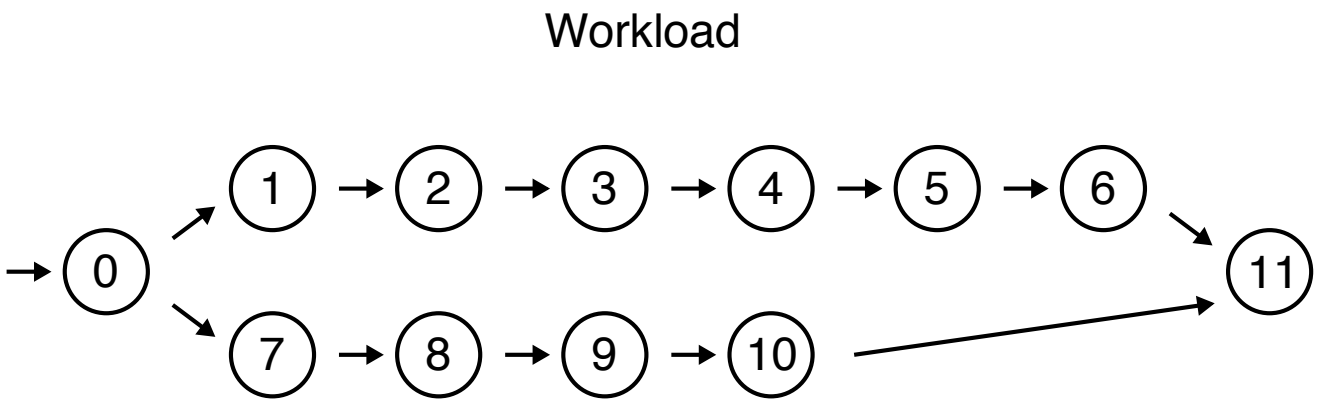
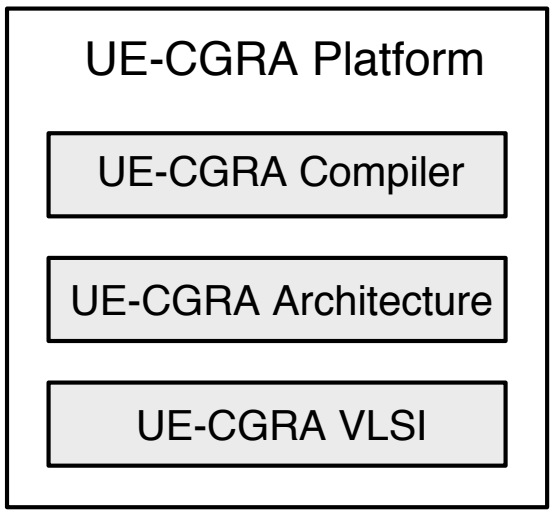
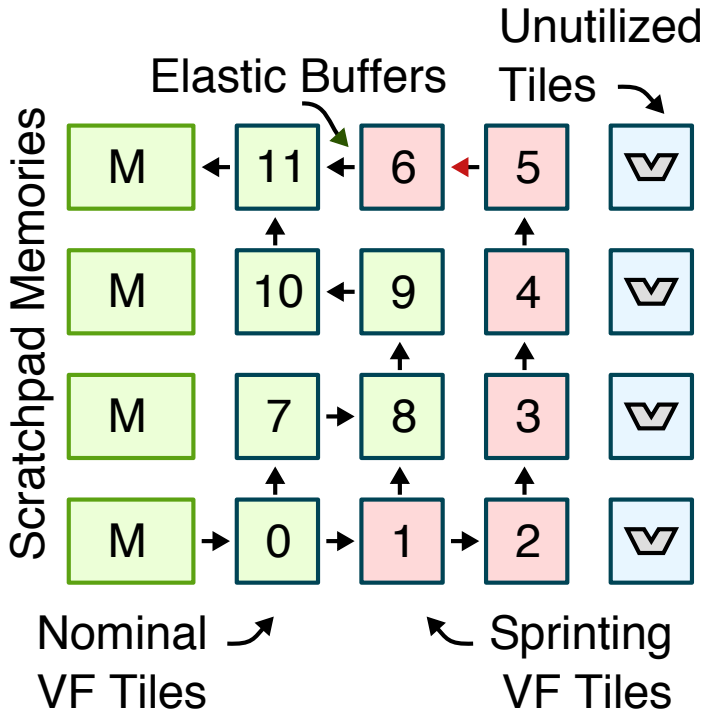
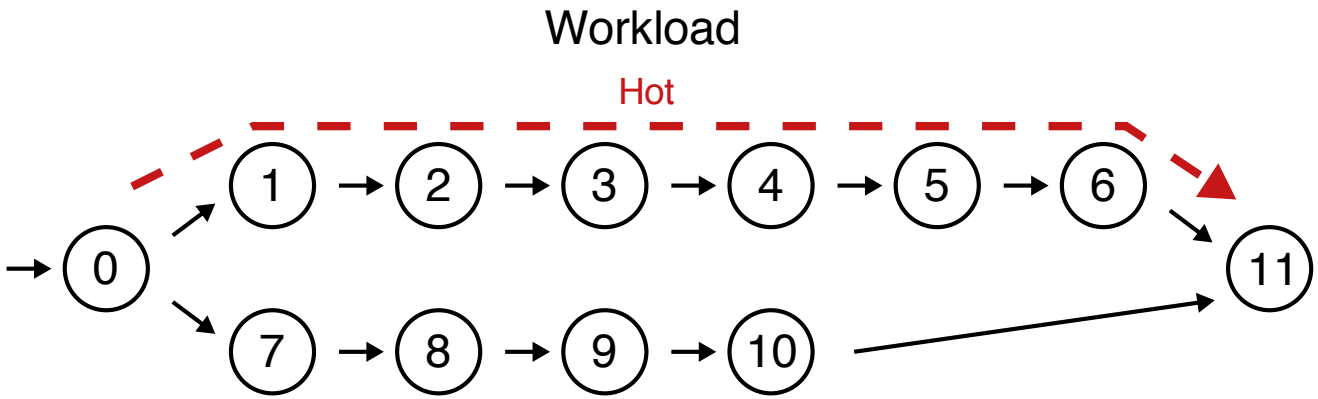
Ultra-Elastic CGRAs (UE-CGRAs)

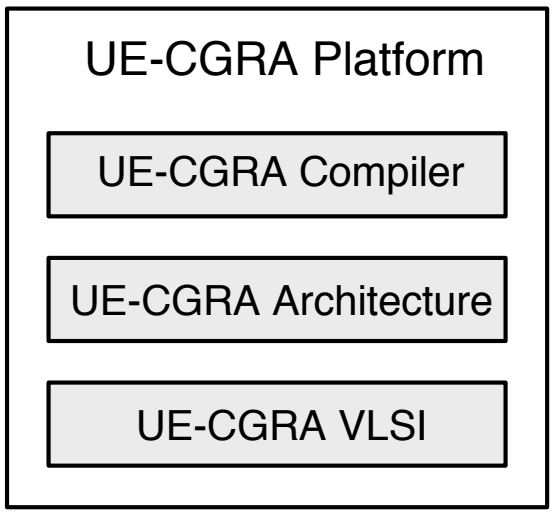


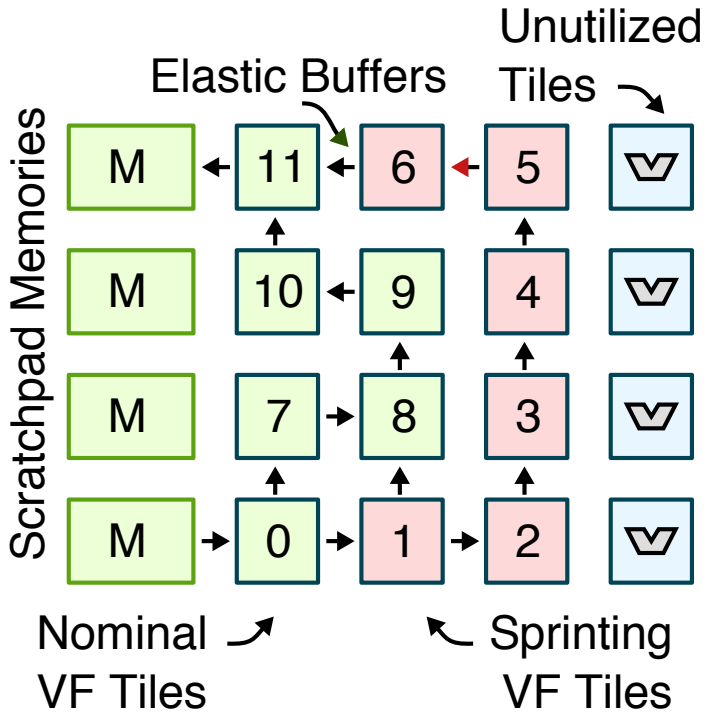


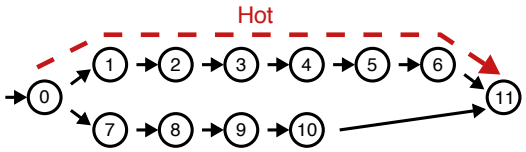


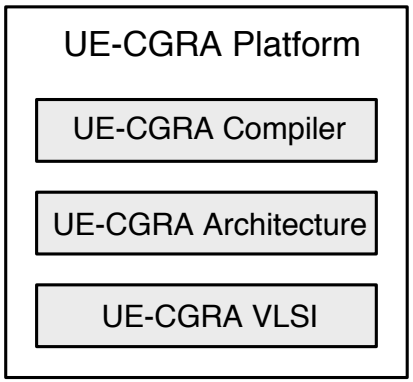
Ultra-Elastic CGRAs (UE-CGRAs)

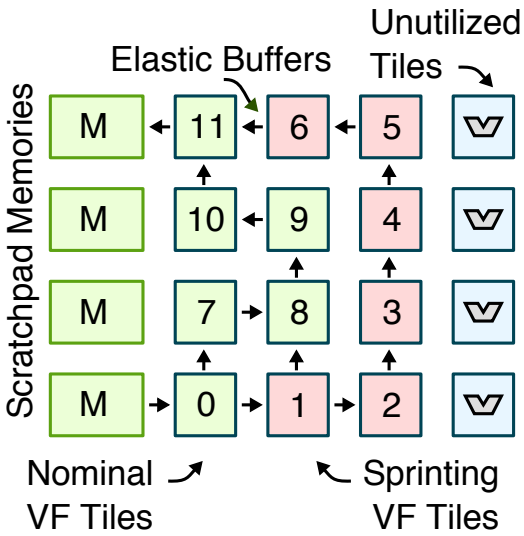








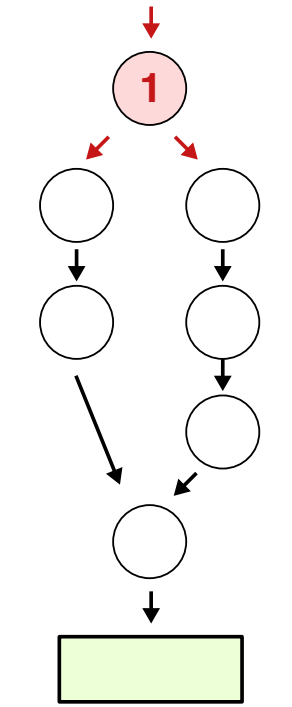




Exploiting Fine-Grain Asymmetry in Ultra-Elastic CGRAs

- Analytical Modeling
- UE-CGRA Compiler and Architecture
- UE-CGRA VLSI
- Methodology
- Evaluation

Elastic CGRA Analytical Performance Model

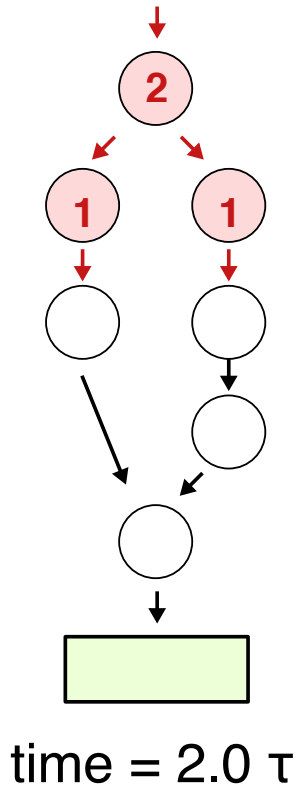


time = 1.0 τ

Discrete-event performance simulator

- Tokens flow and exit the dataflow graph

Elastic CGRA Analytical Performance Model



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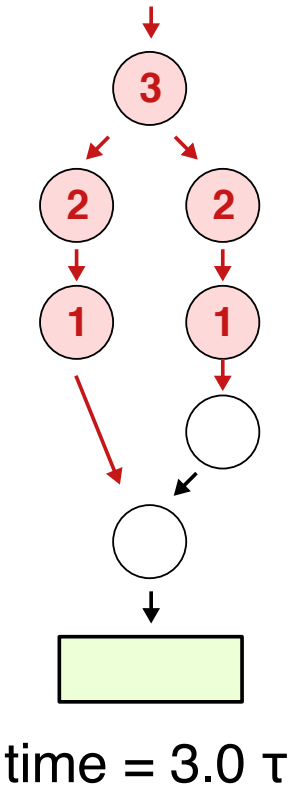
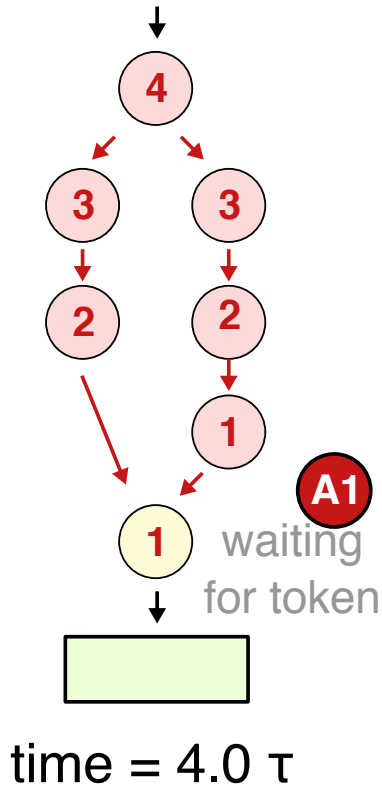


time = 3.0 τ

Discrete-event performance simulator

- Tokens flow and exit the dataflow graph

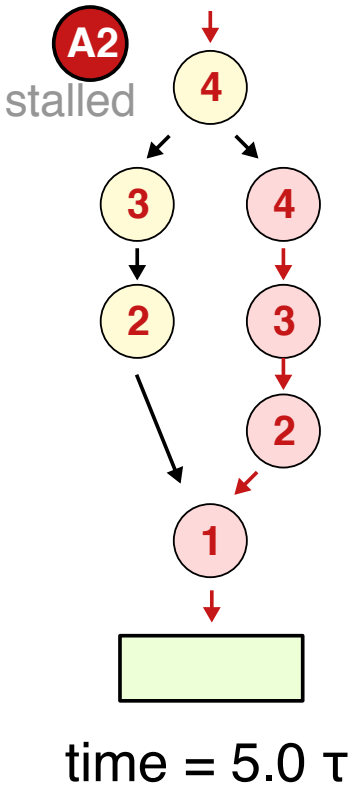
Elastic CGRA Analytical Performance Model



Discrete-event performance simulator

- Tokens flow and exit the dataflow graph
- Nodes fire when all input tokens arrive

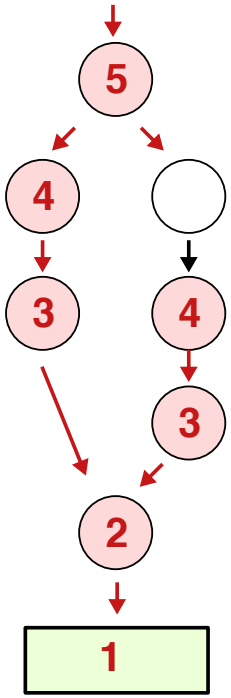
Elastic CGRA Analytical Performance Model



Discrete-event performance simulator

- Tokens flow and exit the dataflow graph
- Nodes fire when all input tokens arrive
- Nodes apply backpressure

Elastic CGRA Analytical Performance Model



time = 6.0 τ

Discrete-event performance simulator

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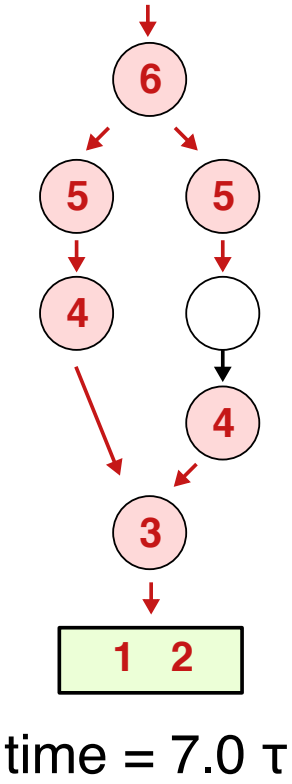
Elastic CGRA Analytical Performance Model



time = 7.0 τ

Discrete-event performance simulator

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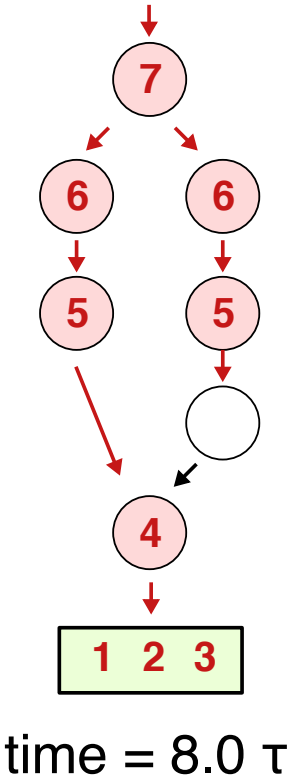
Elastic CGRA Analytical Performance Model



time = 8.0 τ

Discrete-event performance simulator

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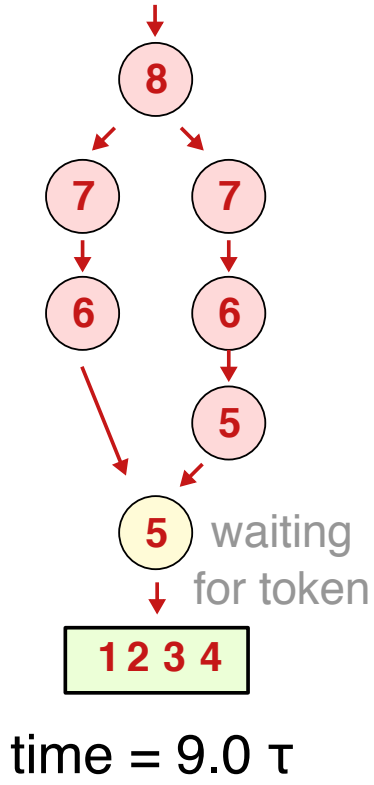

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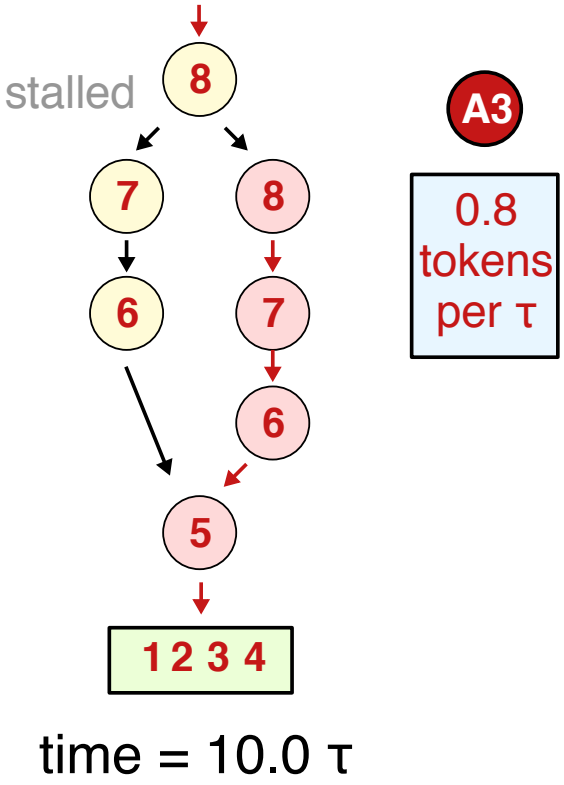

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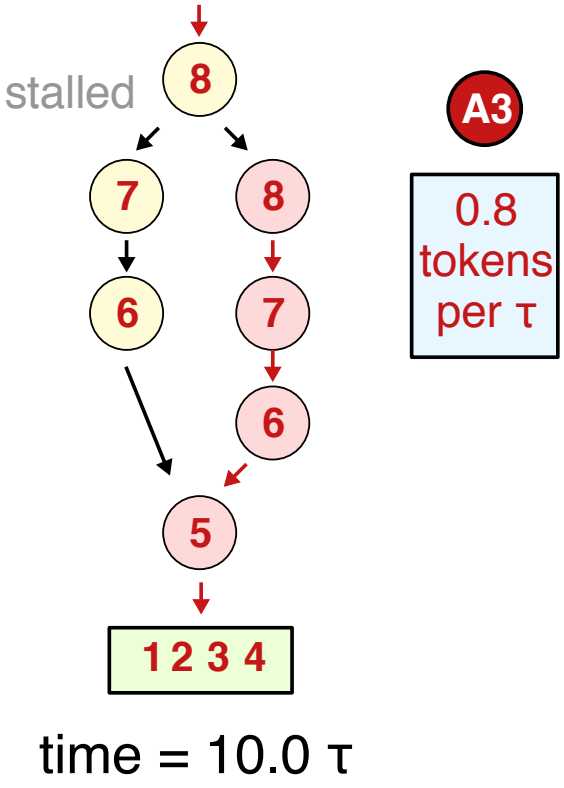

Discrete-event performance simulator

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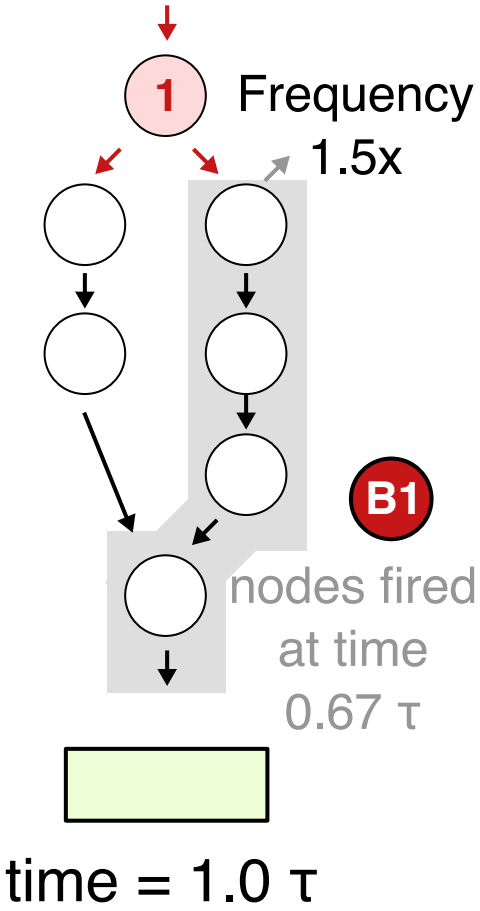
- Nodes apply backpressure

Mapping to a real elastic CGRA

- All nodes map to a single unique tile
- Any tile can communicate with any other
- All tiles run at the same VF mode

Ultra-Elastic CGRA Analytical Performance Model



Discrete-event performance simulator

- Nodes produce tokens at different rates
- Slow nodes produce at 1.0τ intervals

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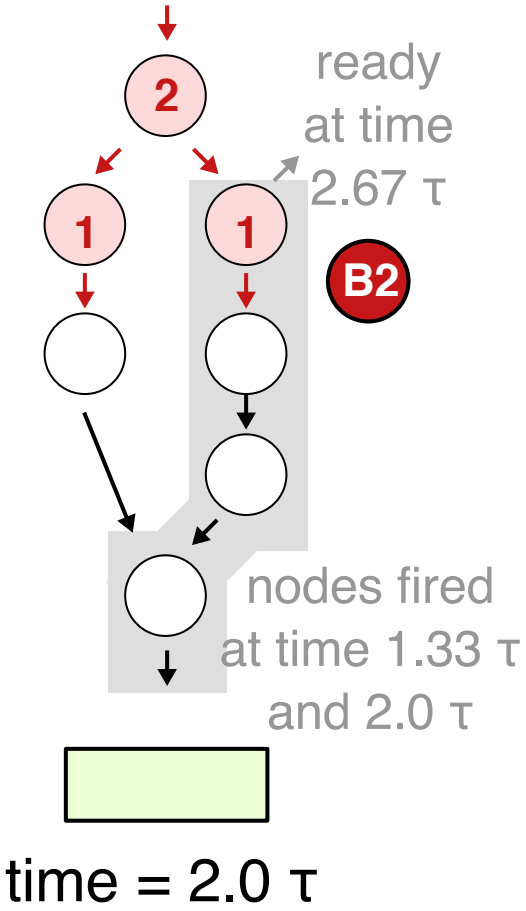

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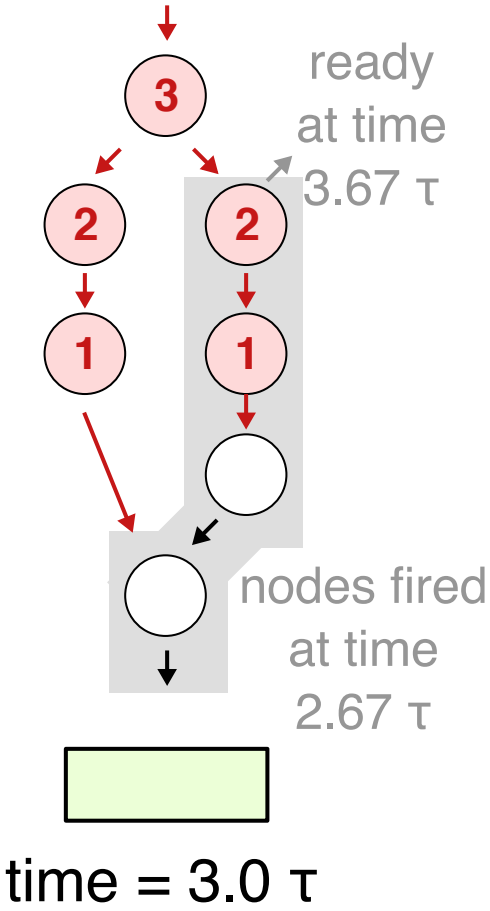

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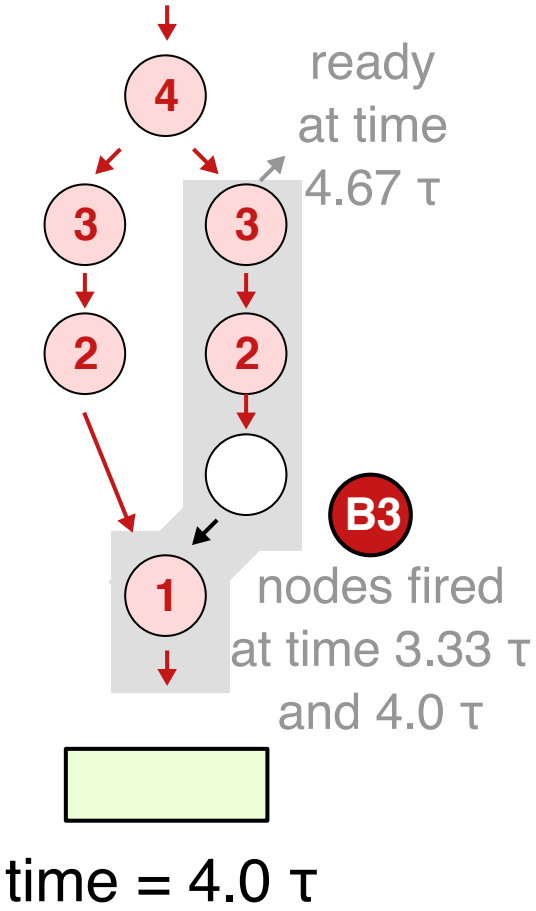

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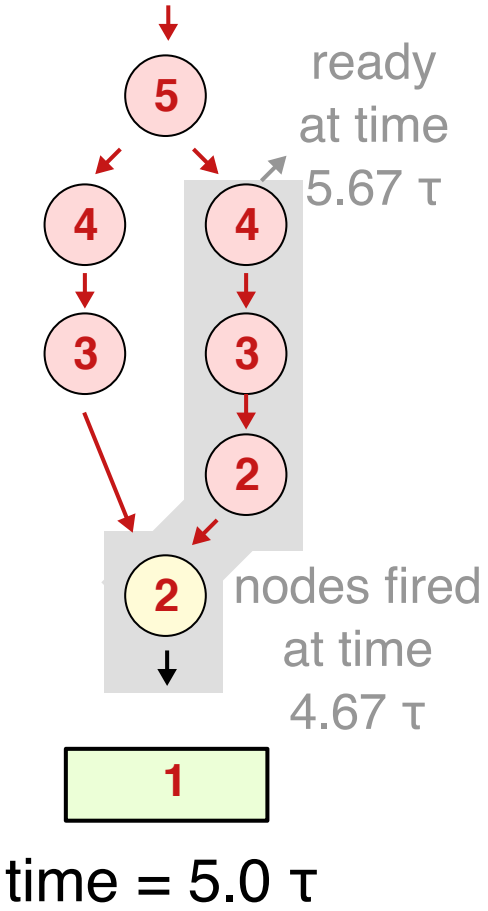

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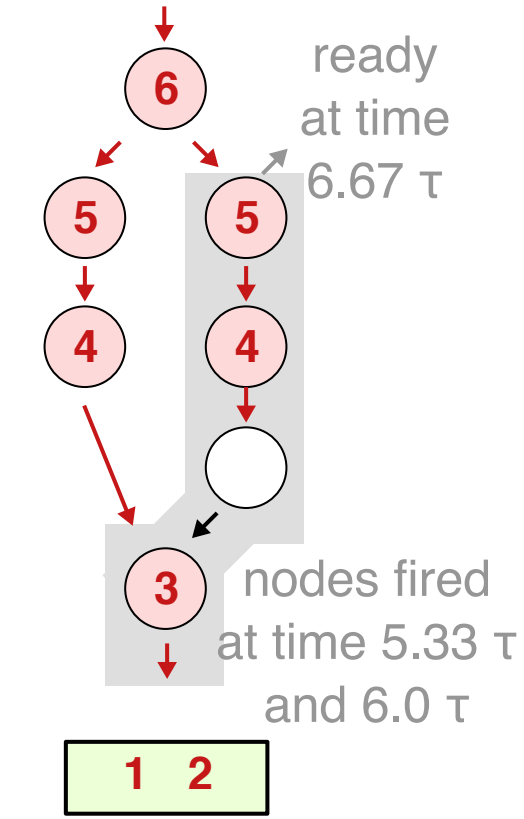

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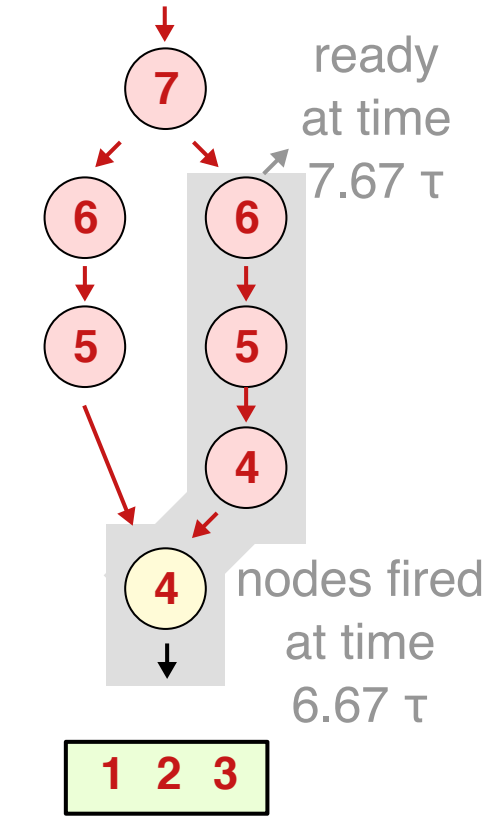

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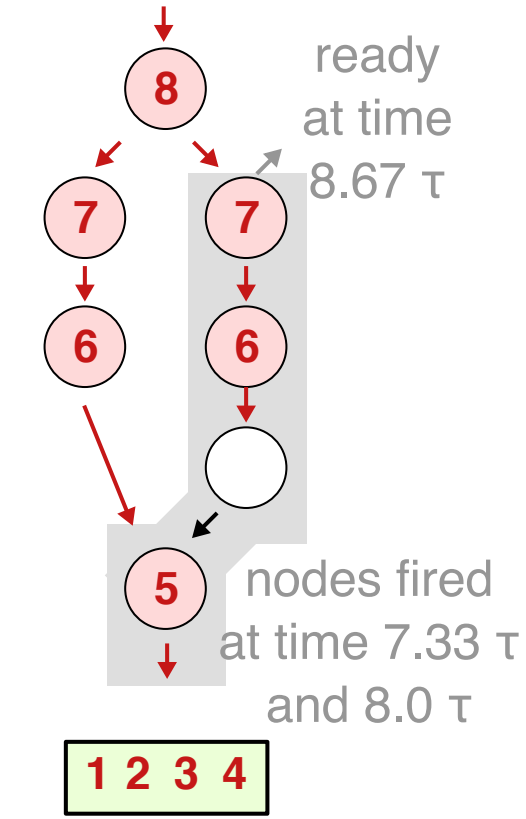

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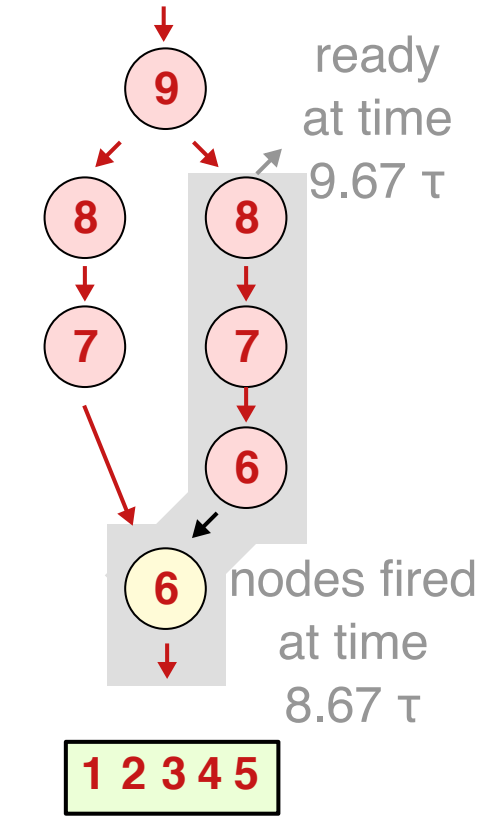

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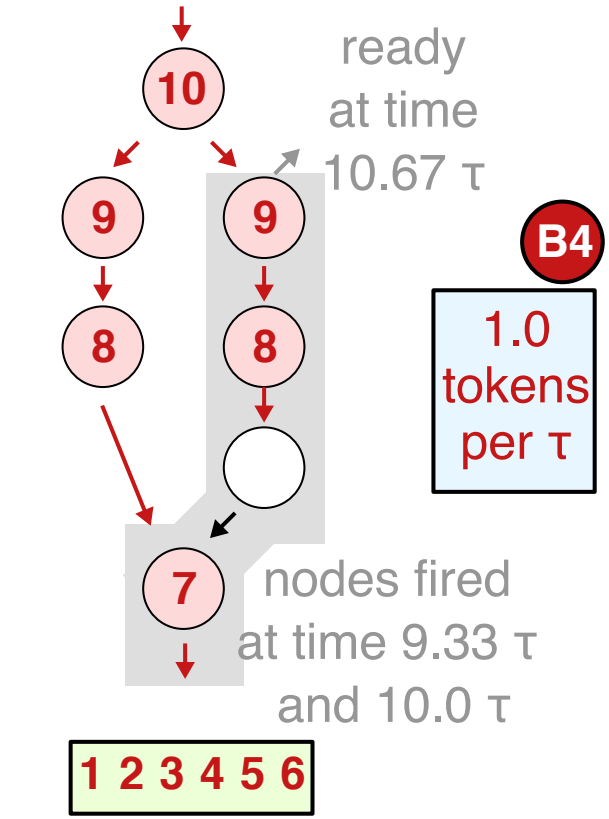

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Analytical Energy Modeling

- First-order power equations

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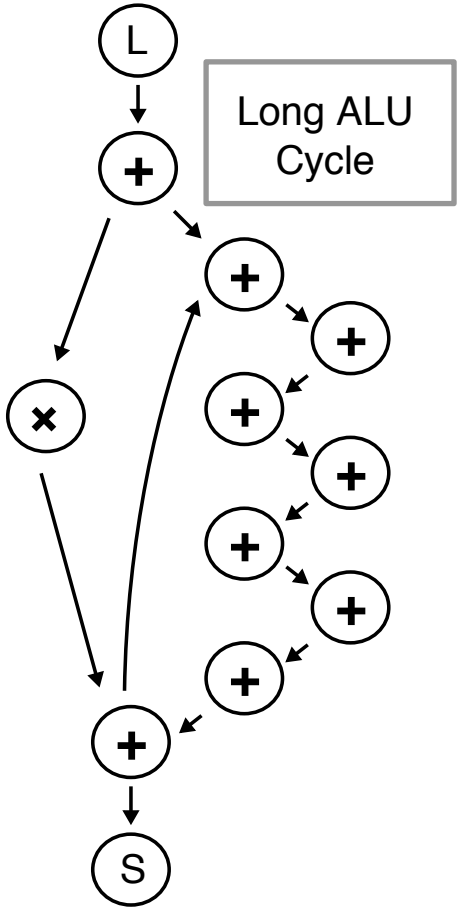
- Voltage and frequency levels
  - Rest voltage – 0.61 V at 3 $\times$ slower frequency
  - Nominal voltage – 0.90 V at 1 $\times$ frequency
  - Sprint voltage – 1.23 V at 1.5 $\times$ frequency

UE-CGRA Analytical Case Study #1

Dataflow Graph



UE-CGRA Analytical Case Study #1

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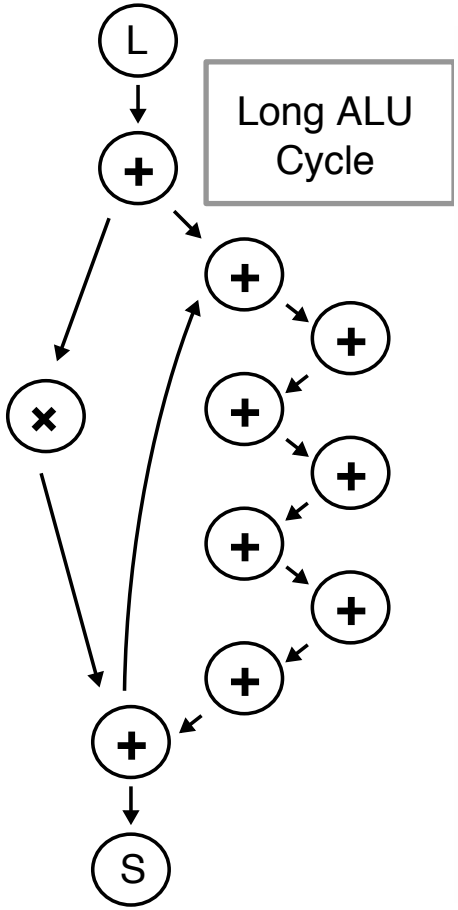
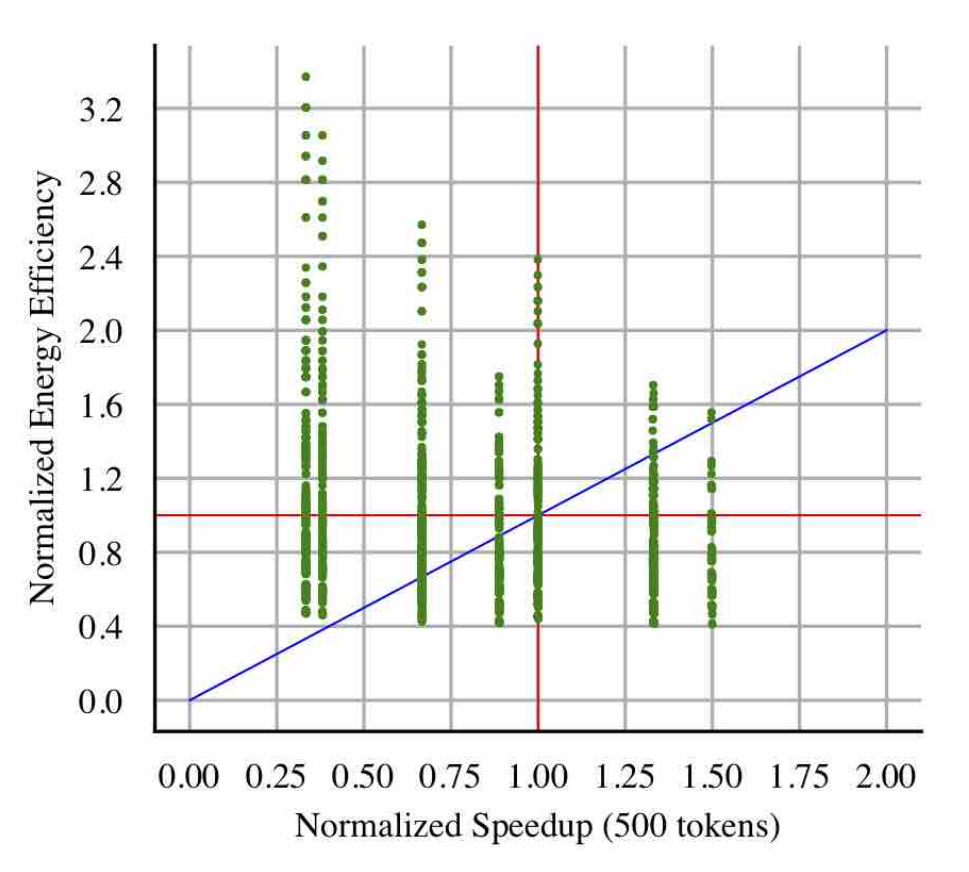


Analytical Sweep



UE-CGRA Analytical Case Study #1

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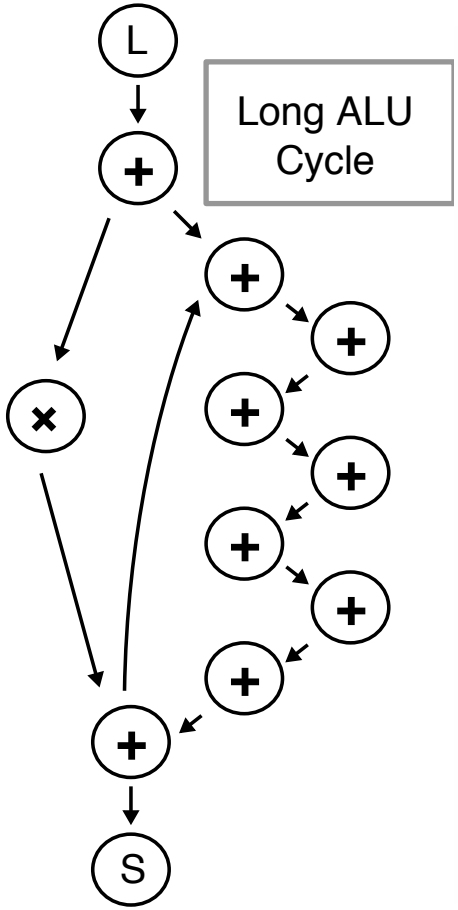

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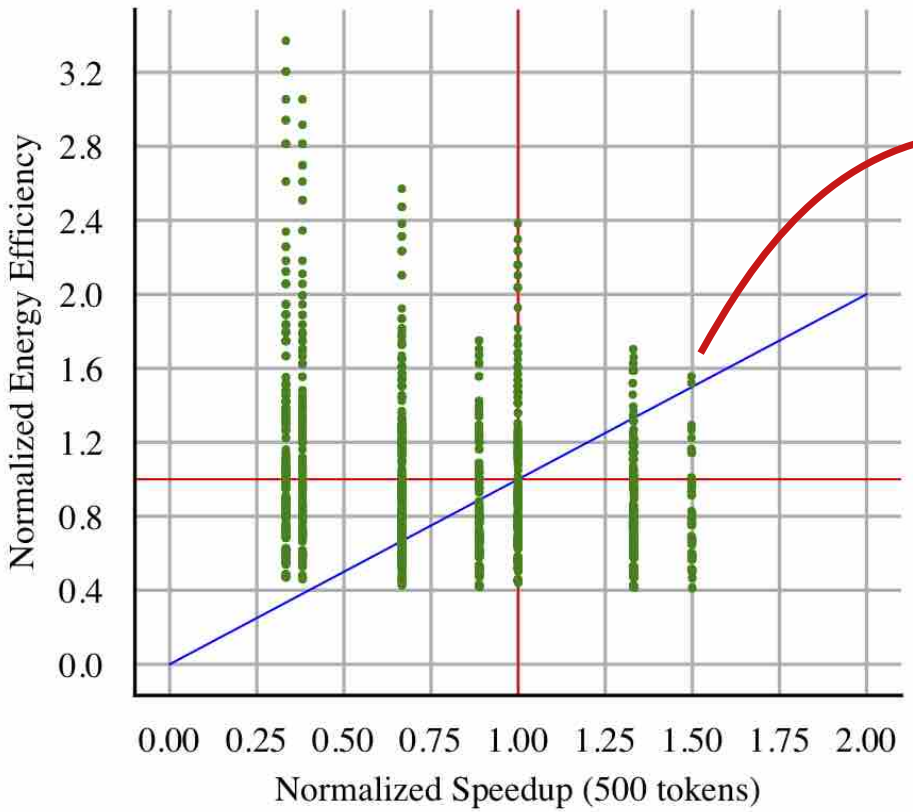
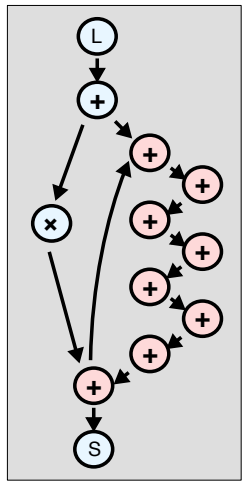


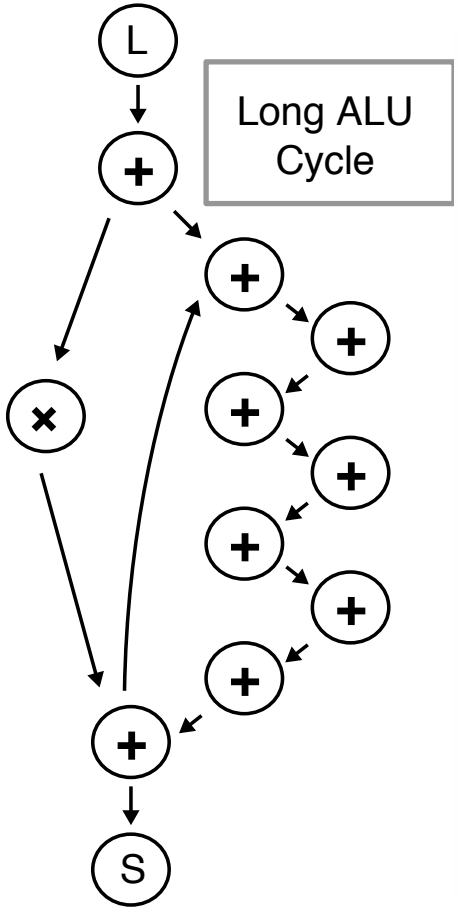
1.5x speedup
1.6x energy eff.



Sprint 1.23V
Nominal 1.0V
Rest 0.61V

UE-CGRA Analytical Case Study #1

Dataflow Graph



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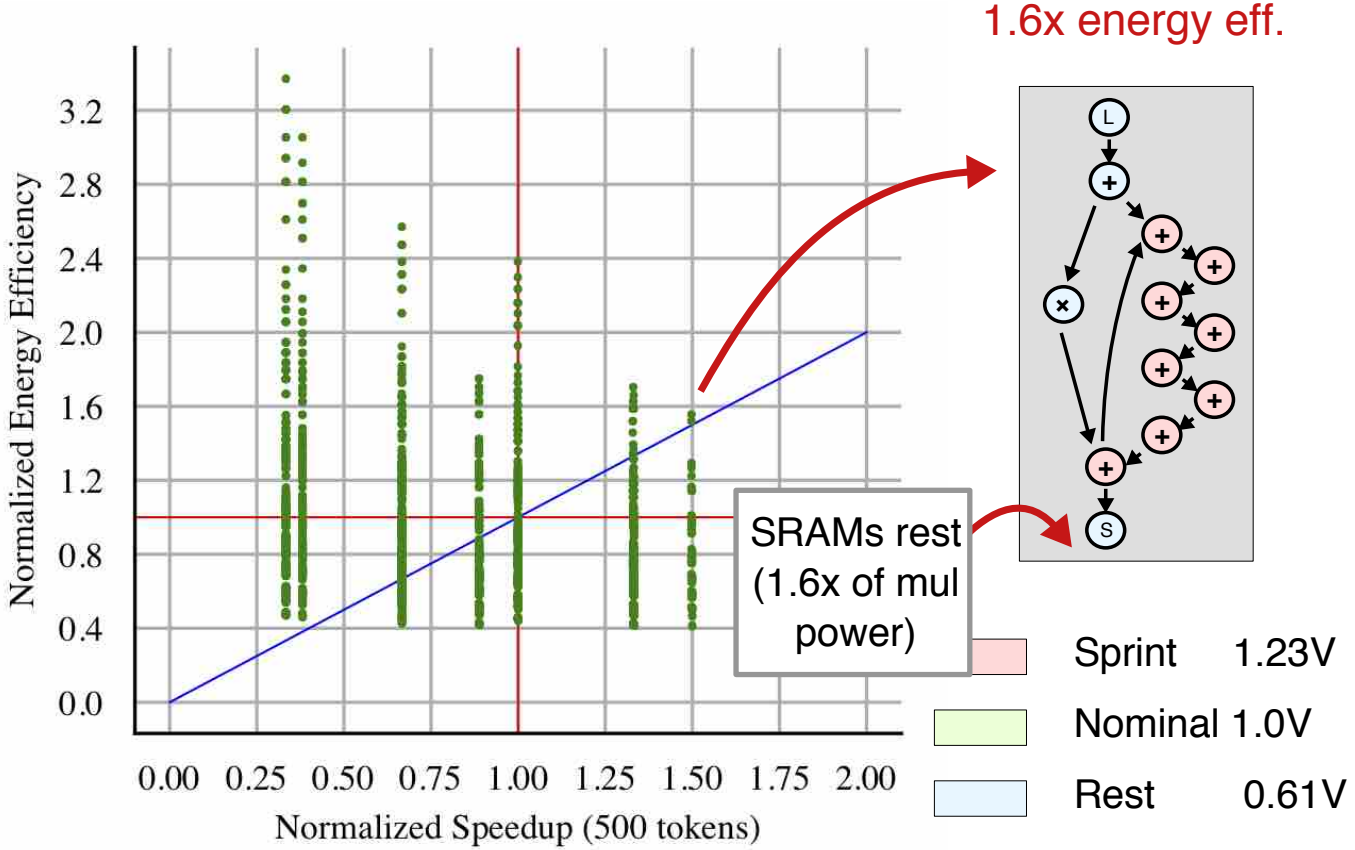

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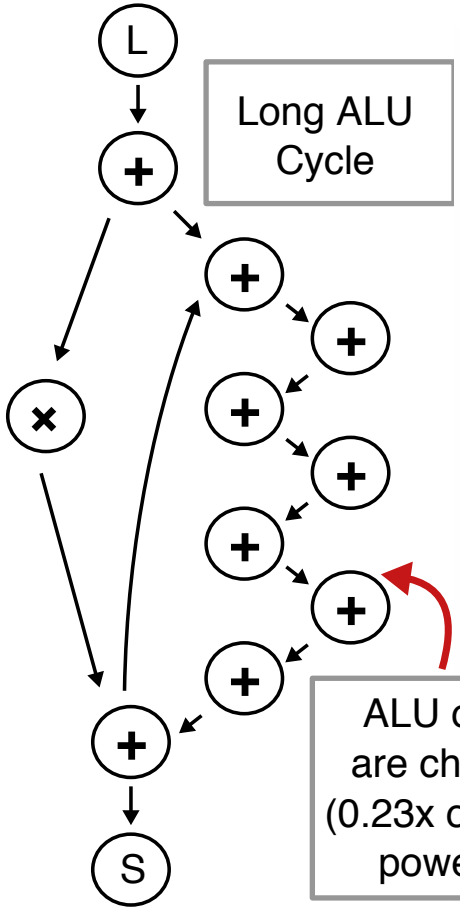

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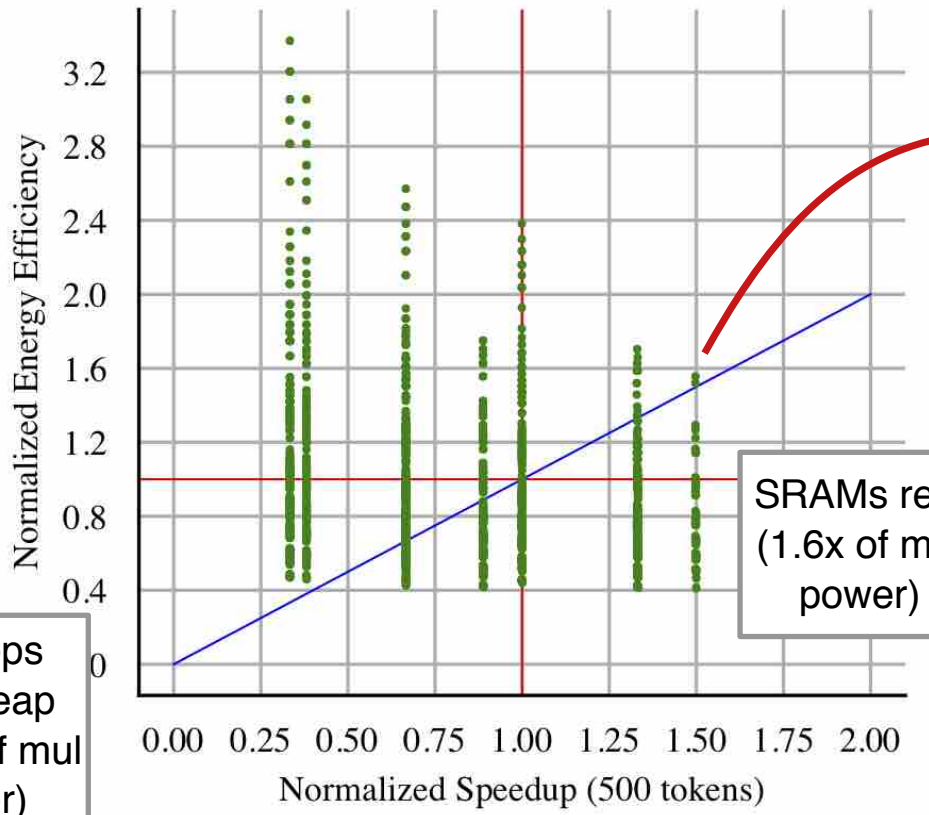

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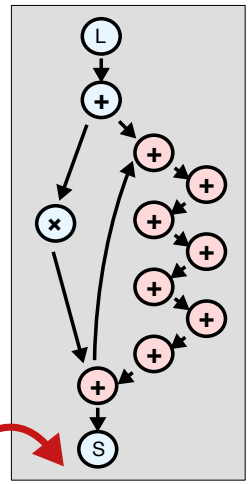
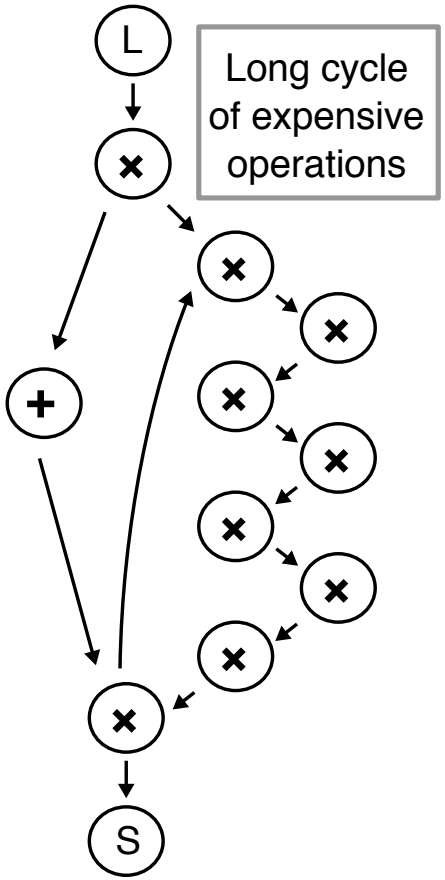


SRAMs rest (1.6x of mul power)

Sprint 1.23V
Nominal 1.0V
Rest 0.61V

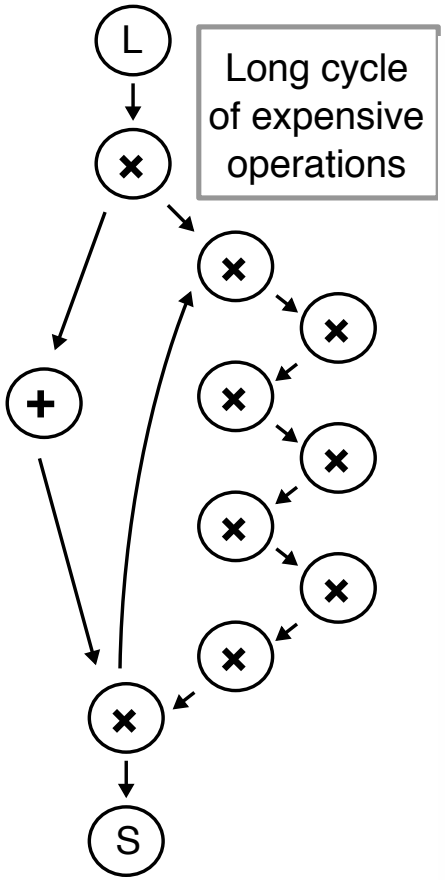
UE-CGRA Analytical Case Study #2

Dataflow Graph

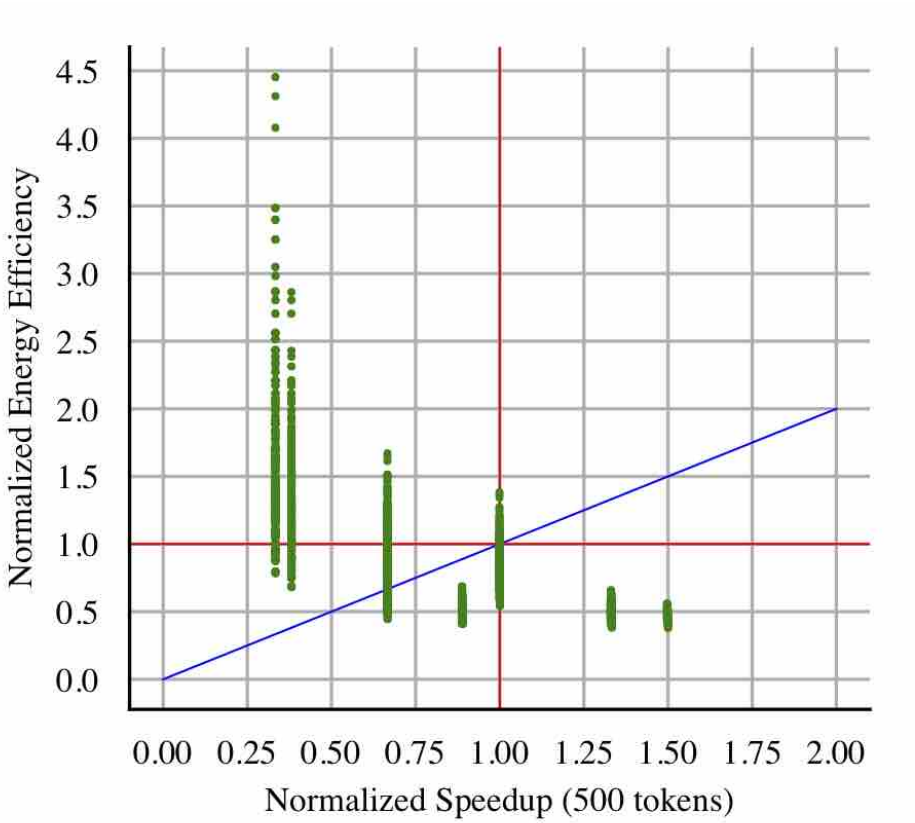


UE-CGRA Analytical Case Study #2

Dataflow Graph



Analytical Sweep



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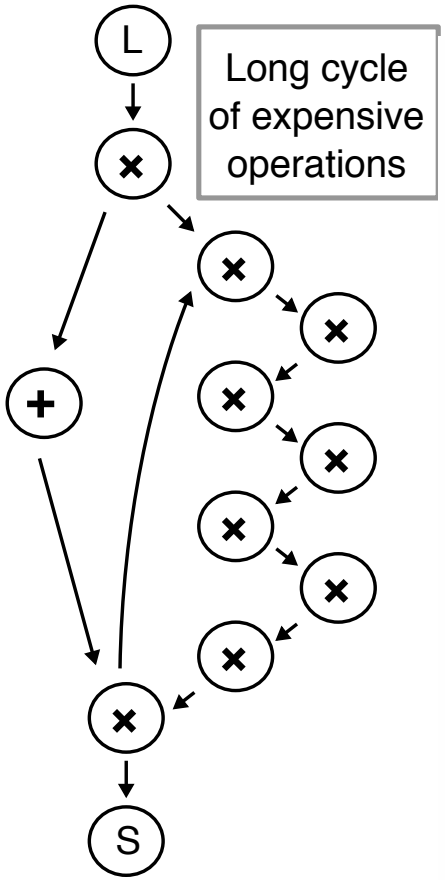

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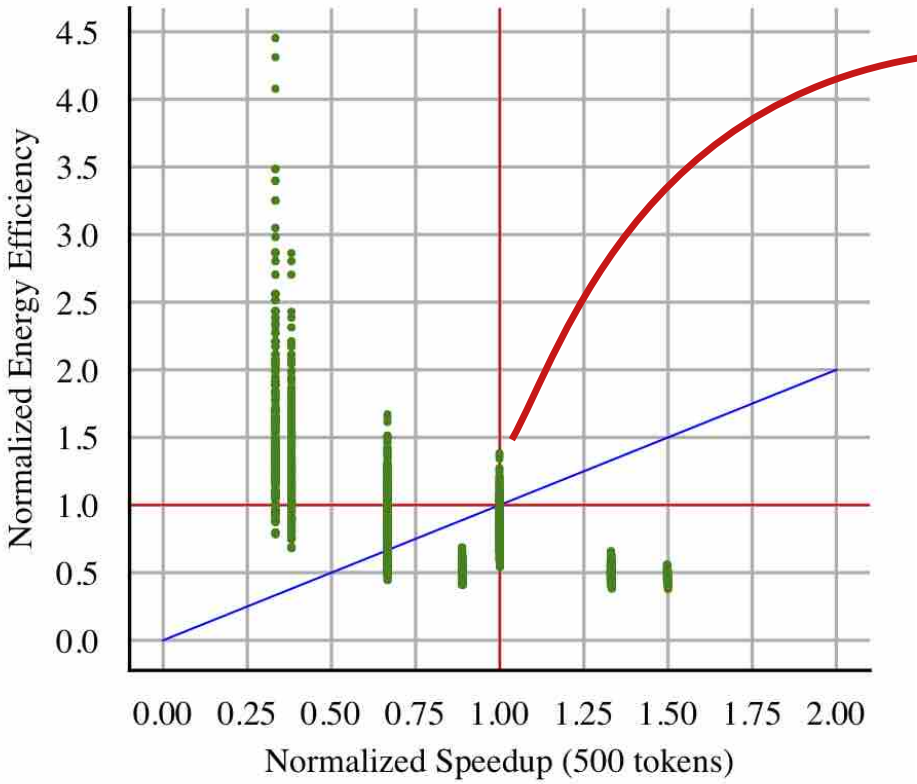

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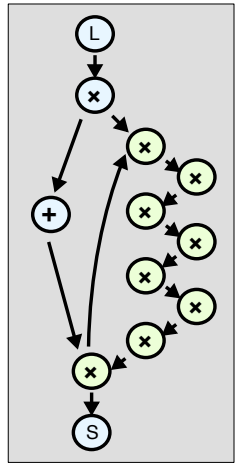

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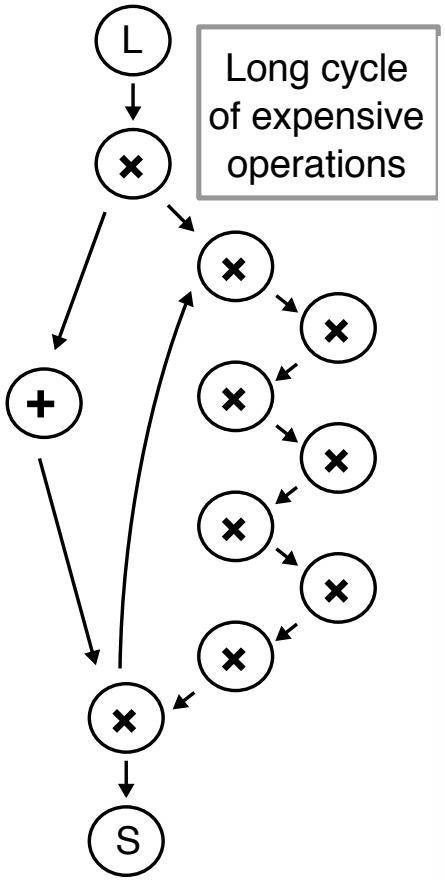

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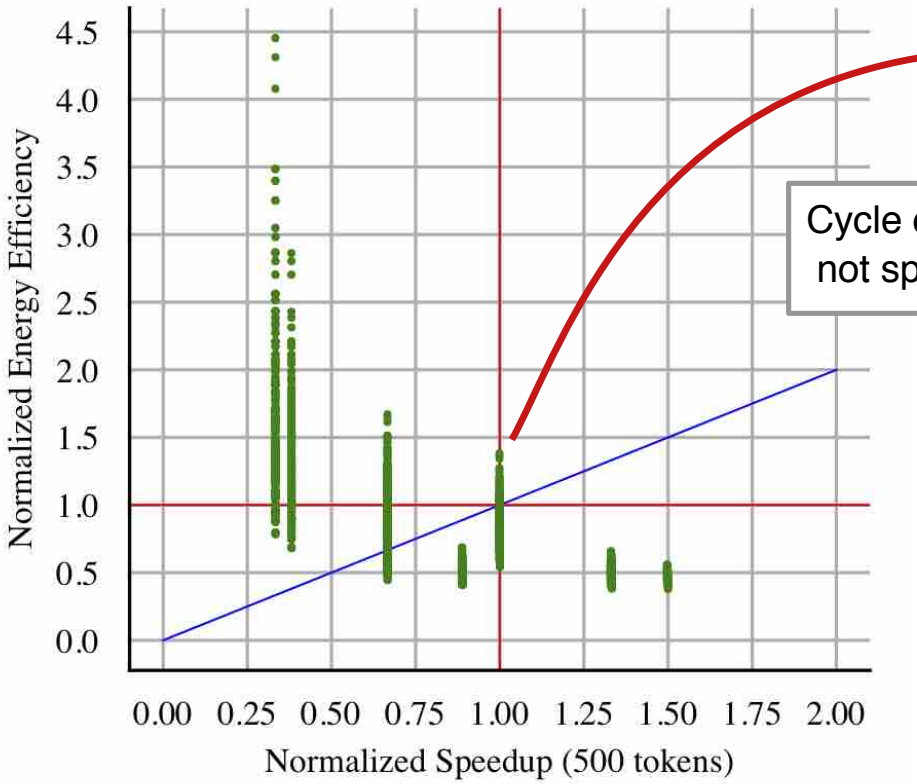

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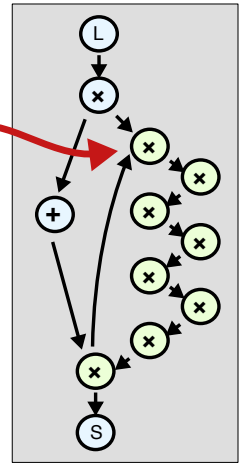

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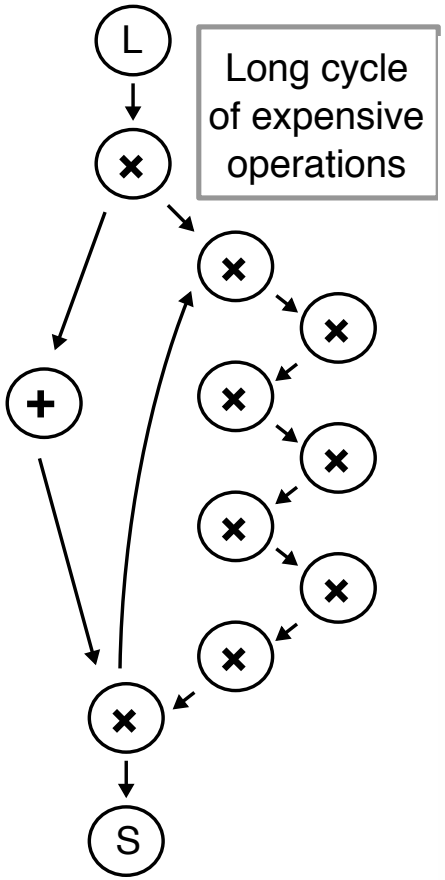
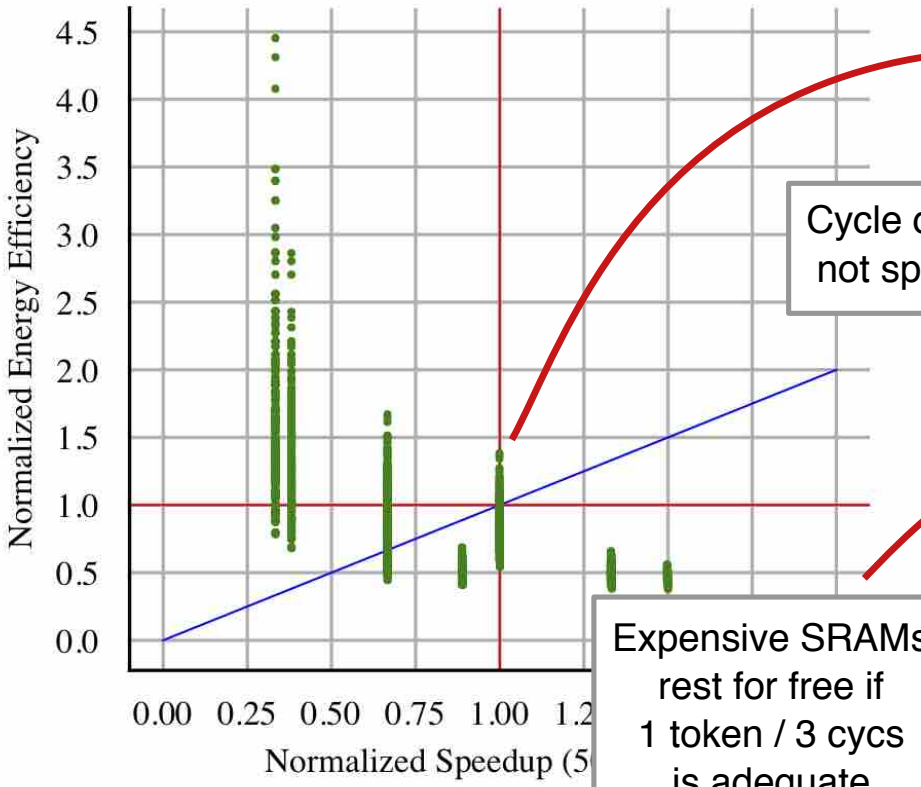


Long cycle of expensive operations

Analytical Sweep



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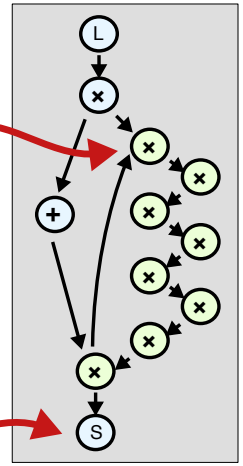

Expensive SRAMs rest for free if 1 token / 3 cycs is adequate

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UE-CGRA Analytical Summary

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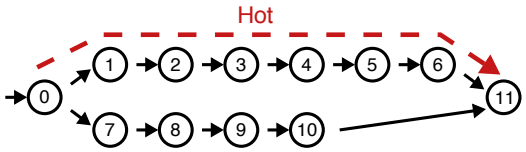
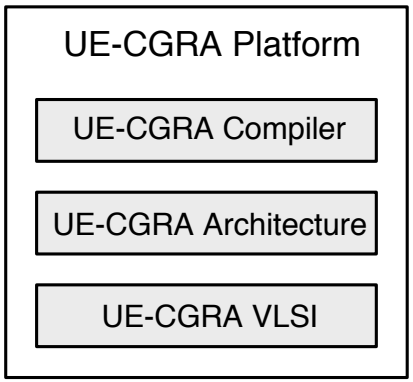
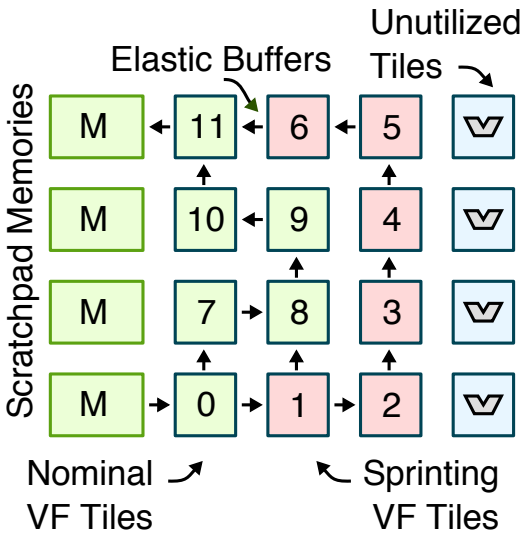
- Long dependent chains of *cheap* operators (whether from cycles or from series-parallel joins) are excellent candidates for performance improvement with minimal impact to energy







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- UE-CGRA Compiler and Architecture
- UE-CGRA VLSI
- Methodology
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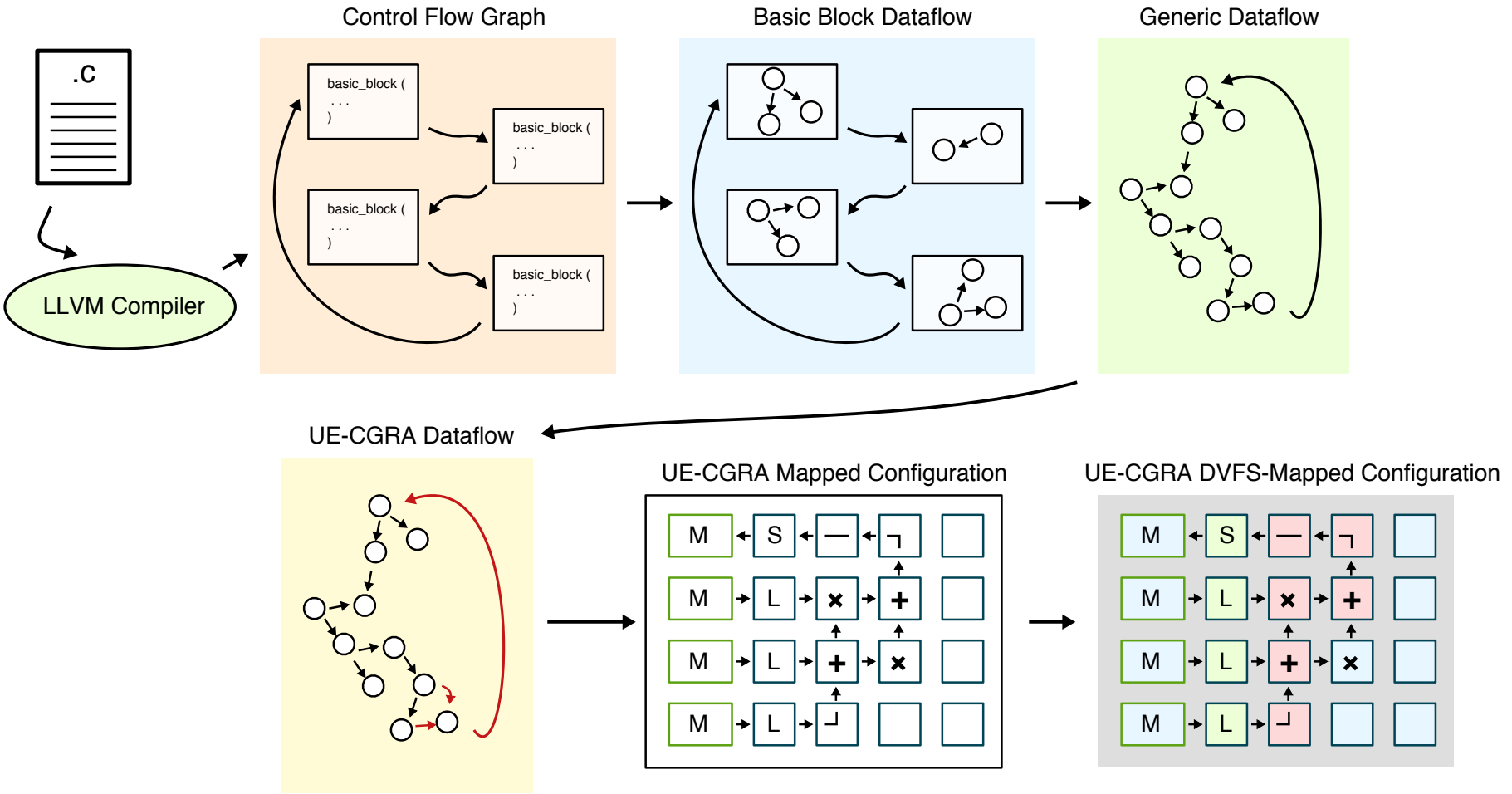

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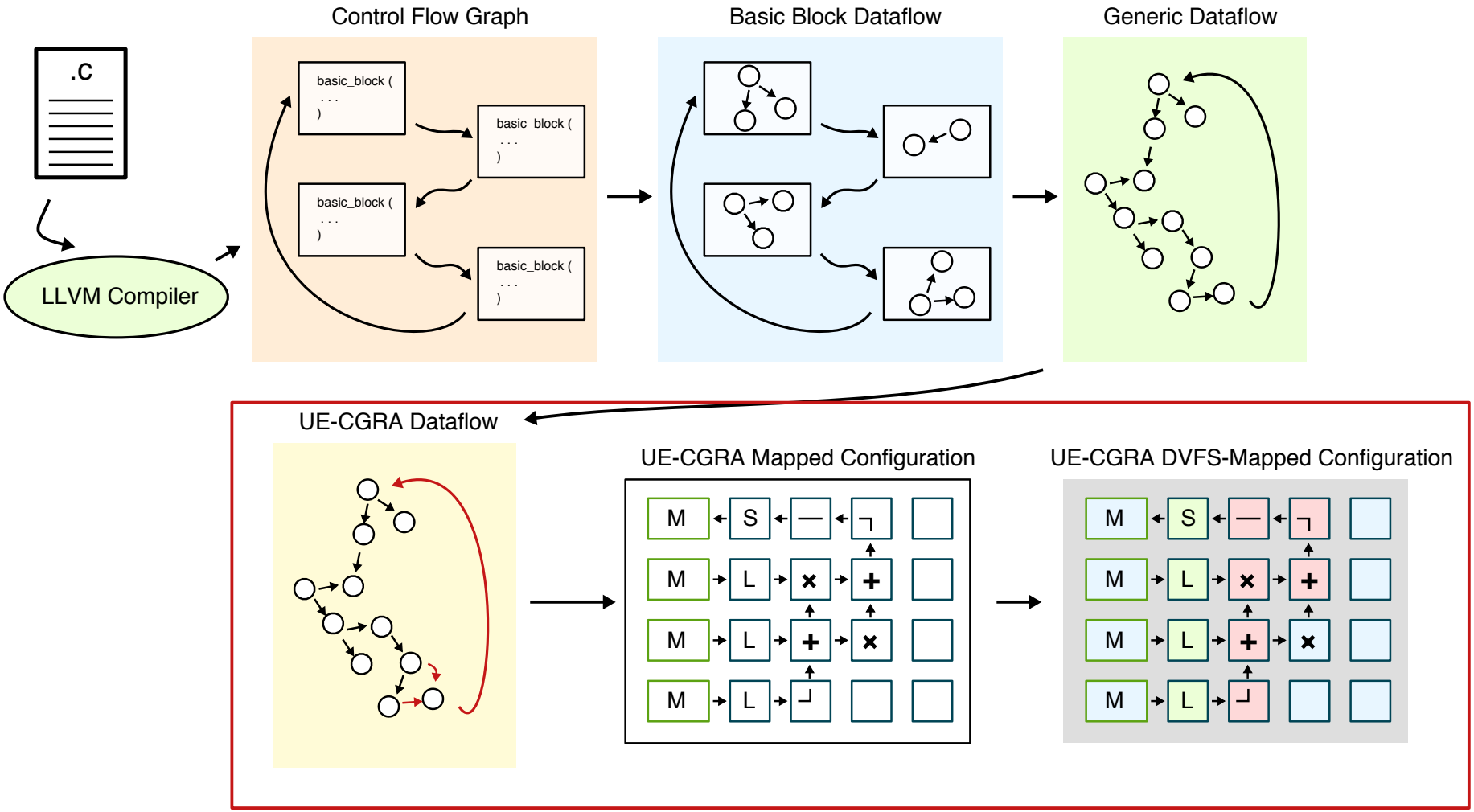

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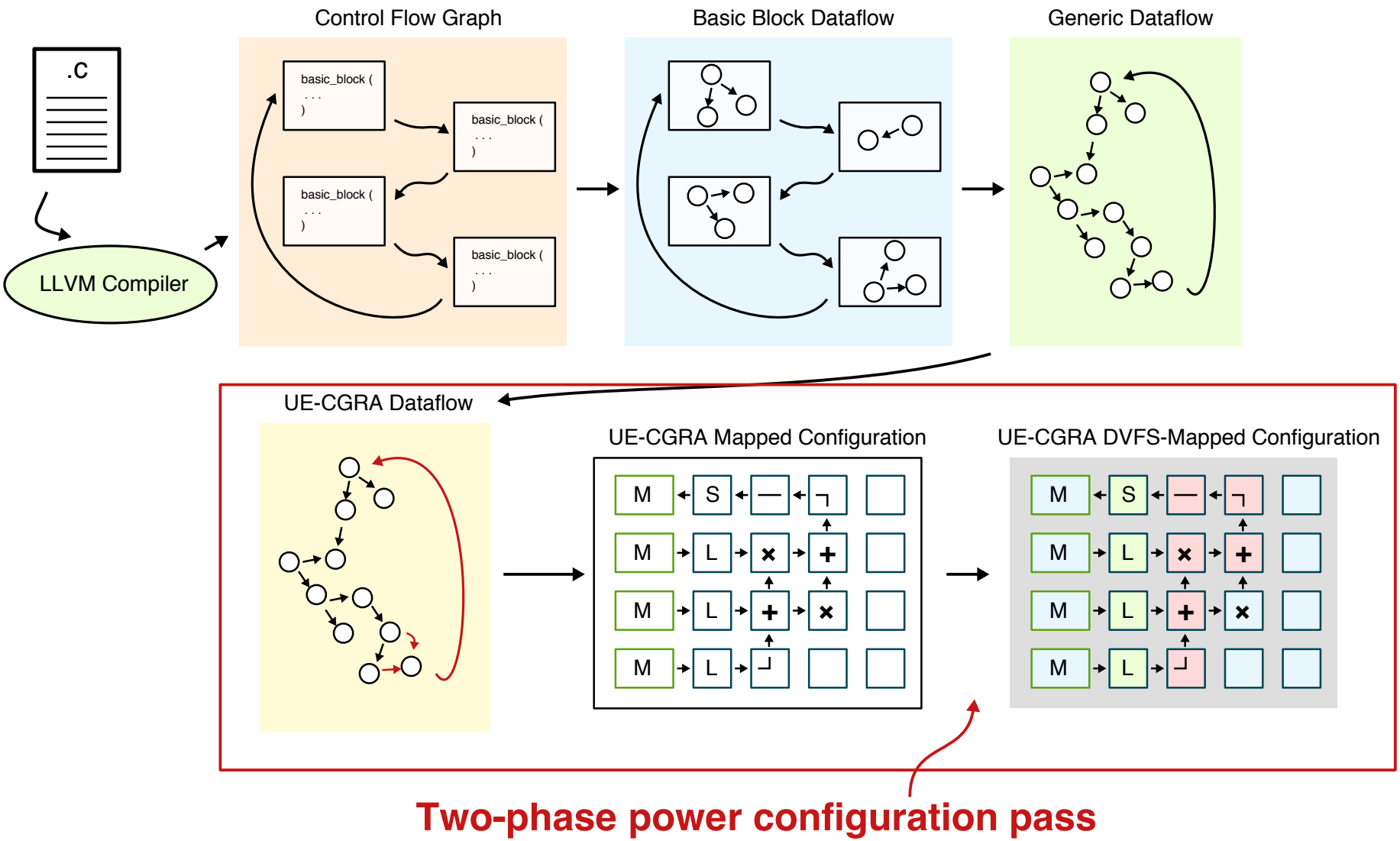
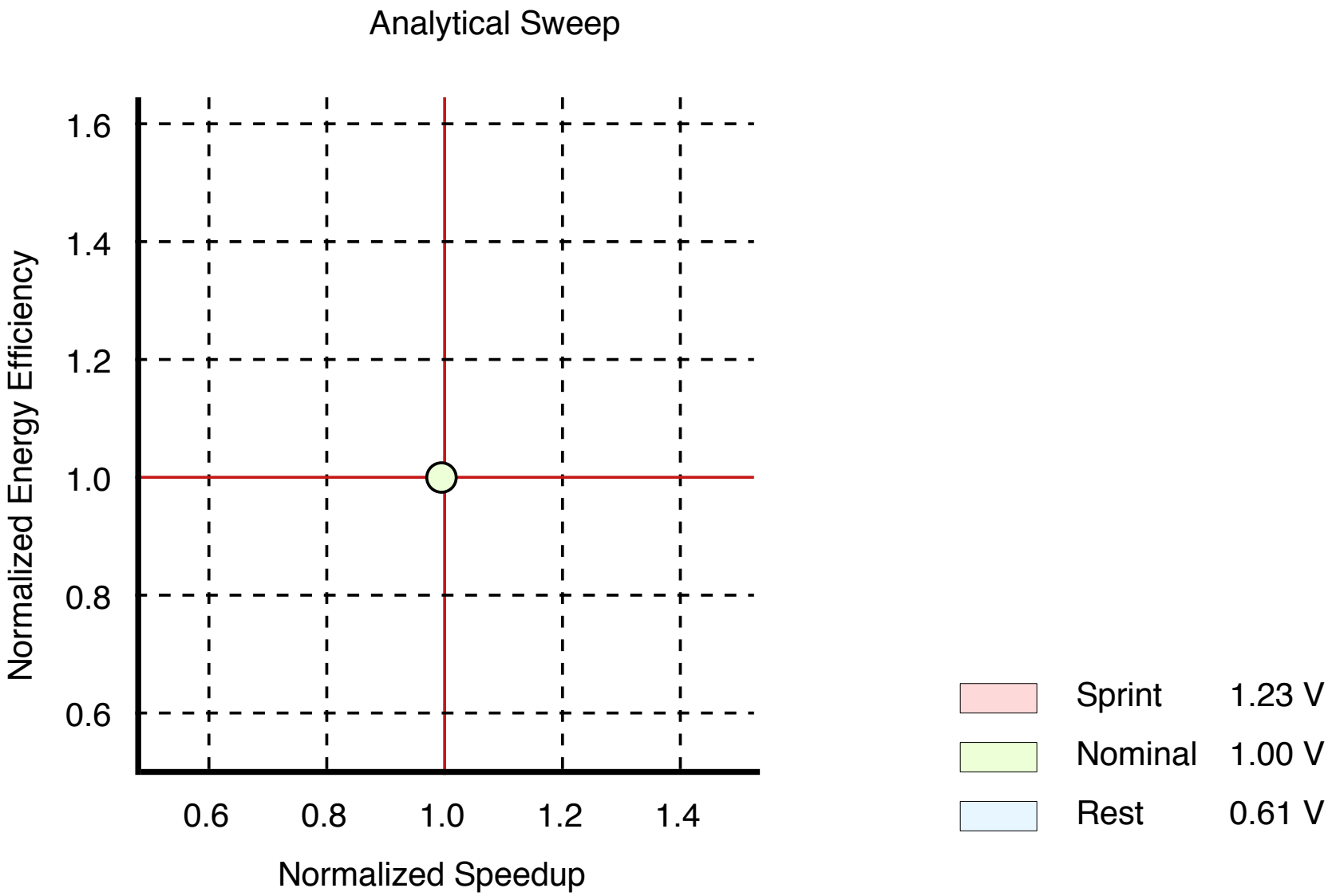


Two-Phase Power Configuration Pass



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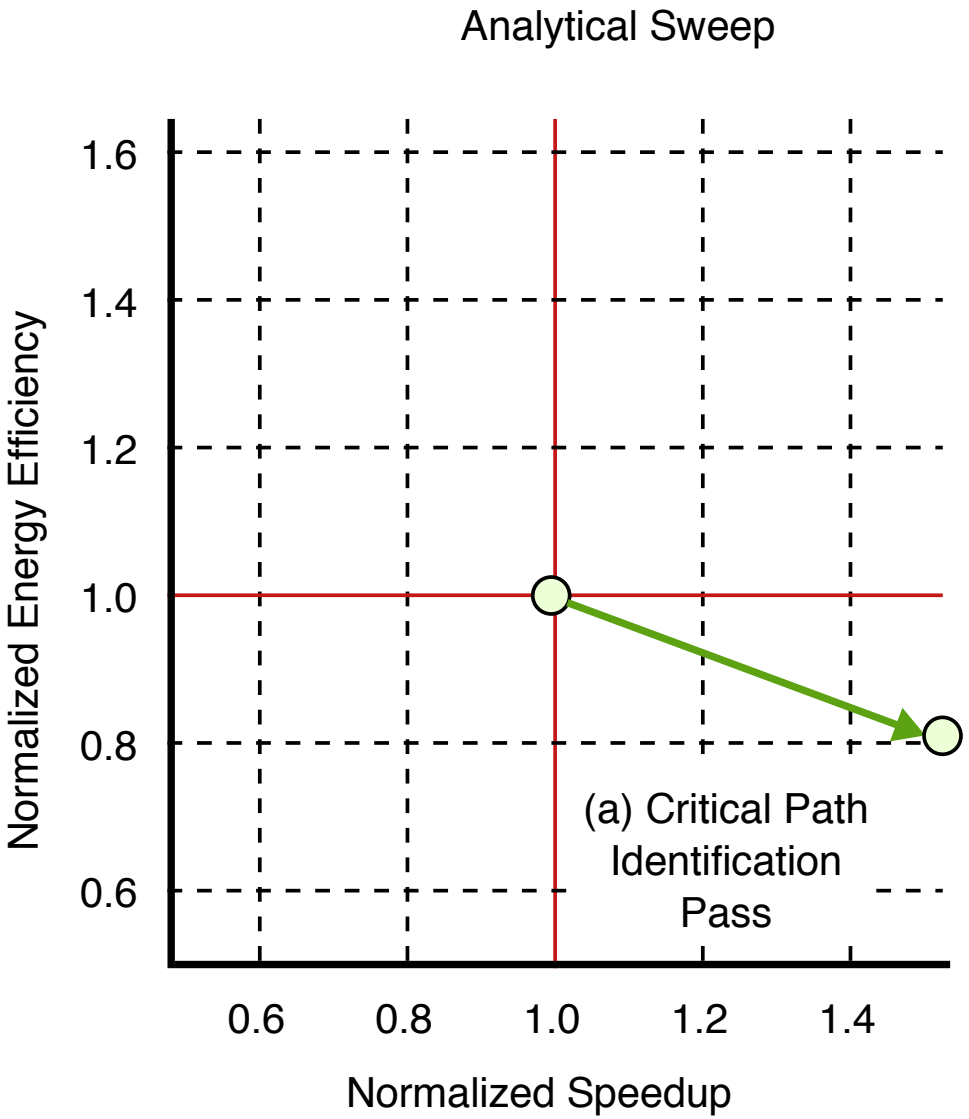

After (a)

1.5x speedup
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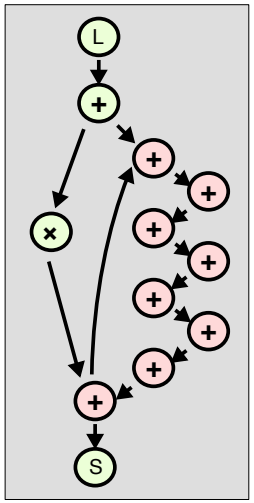

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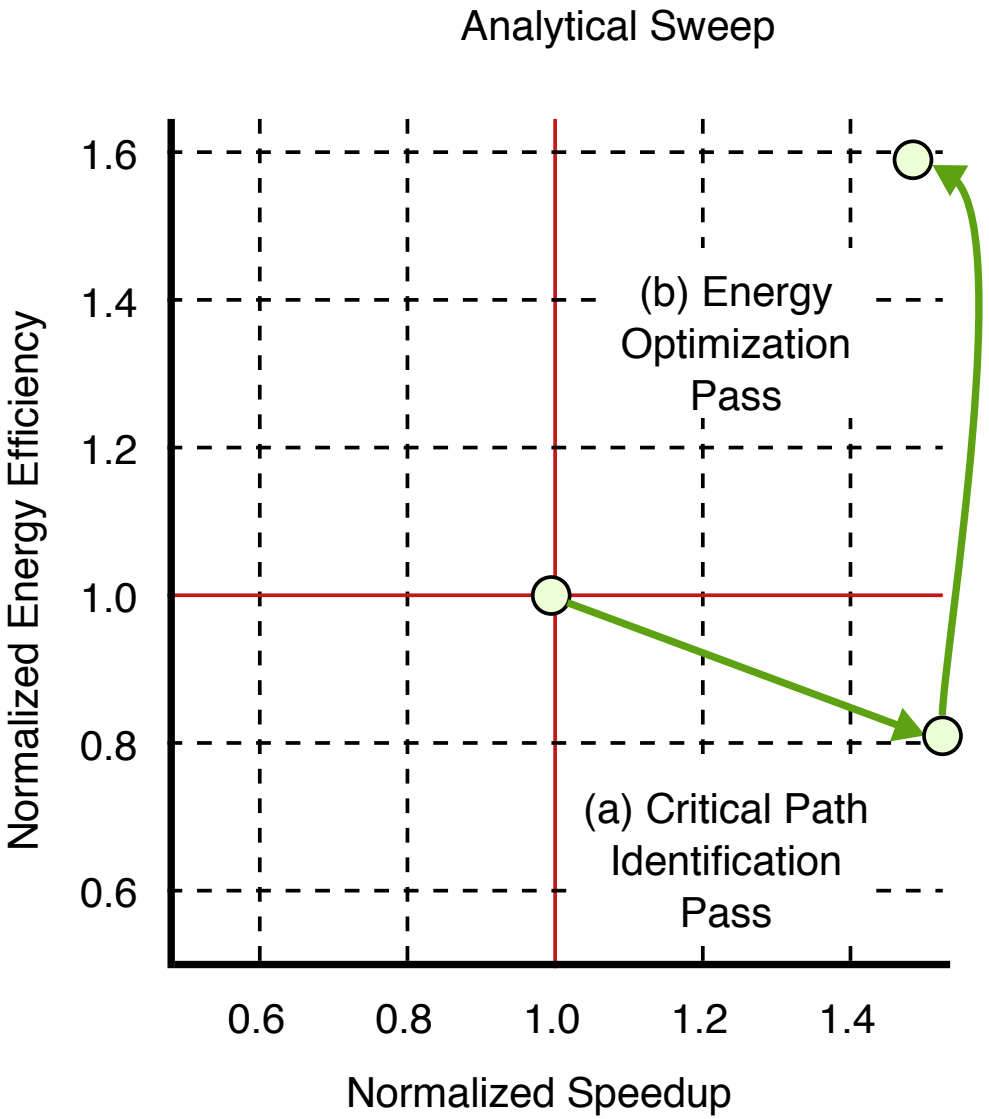

After (a)

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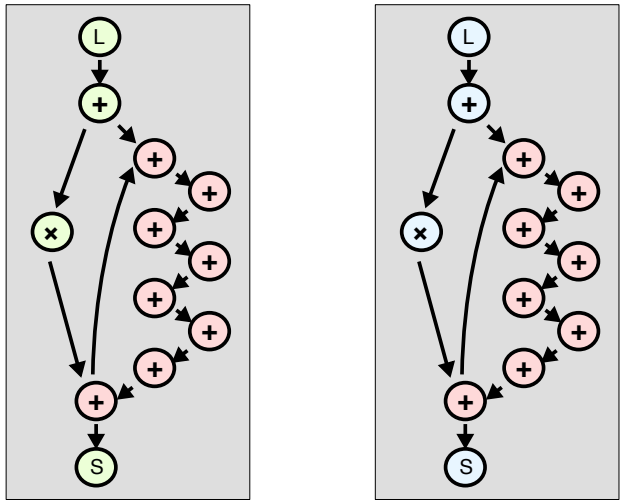

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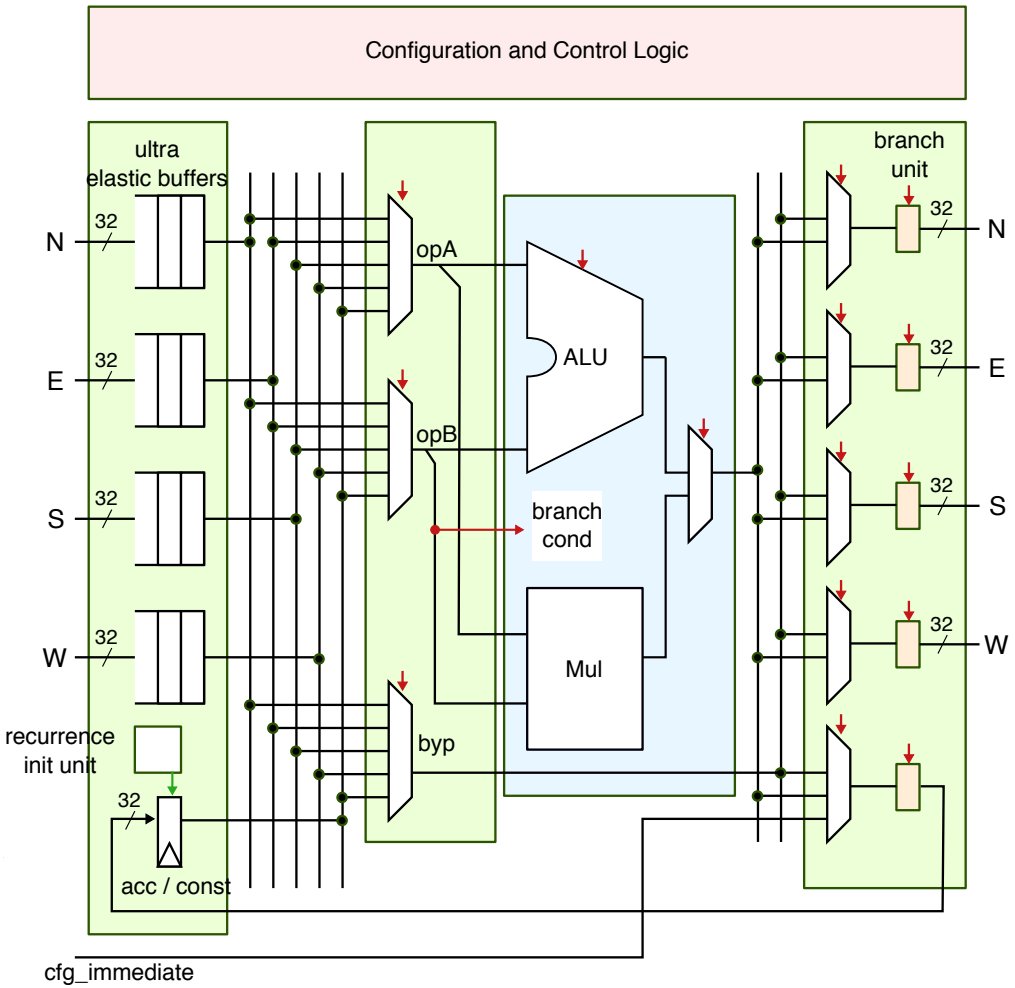
UE-CGRA Tile



- Input queues
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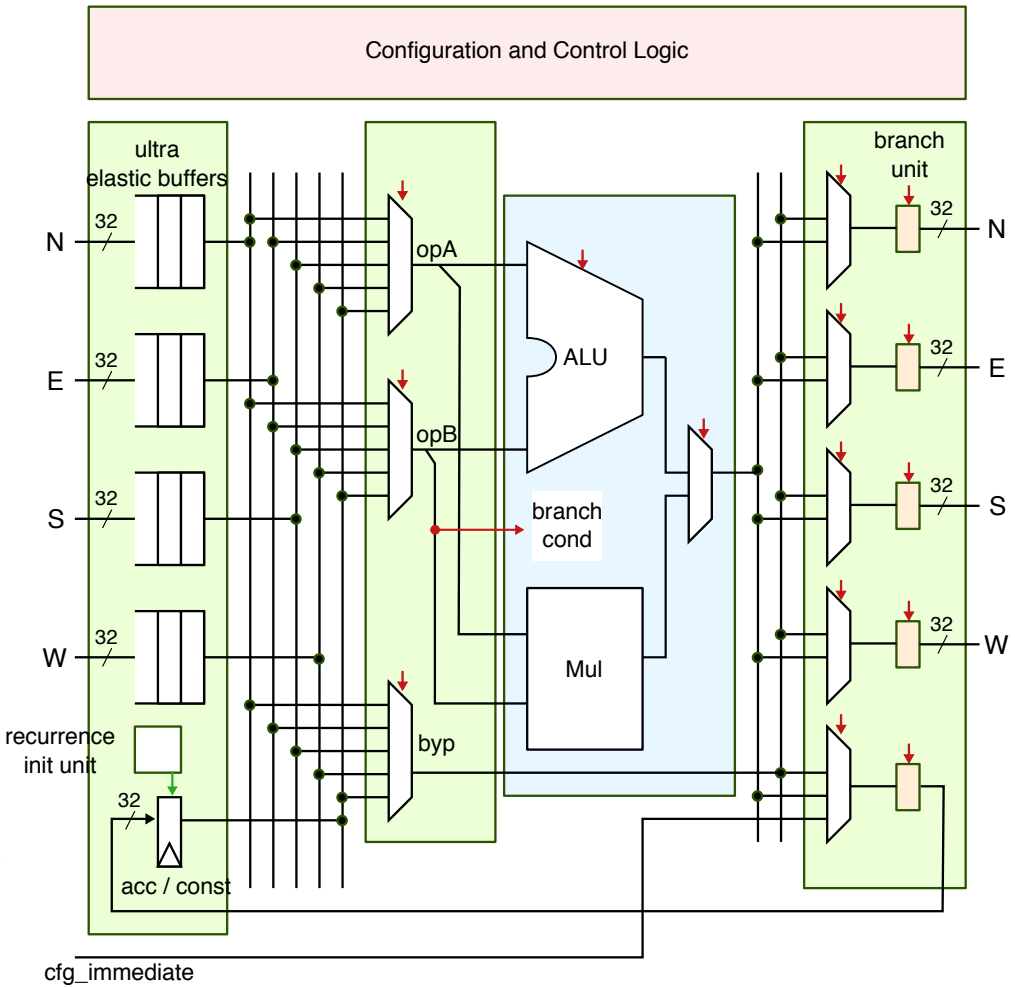

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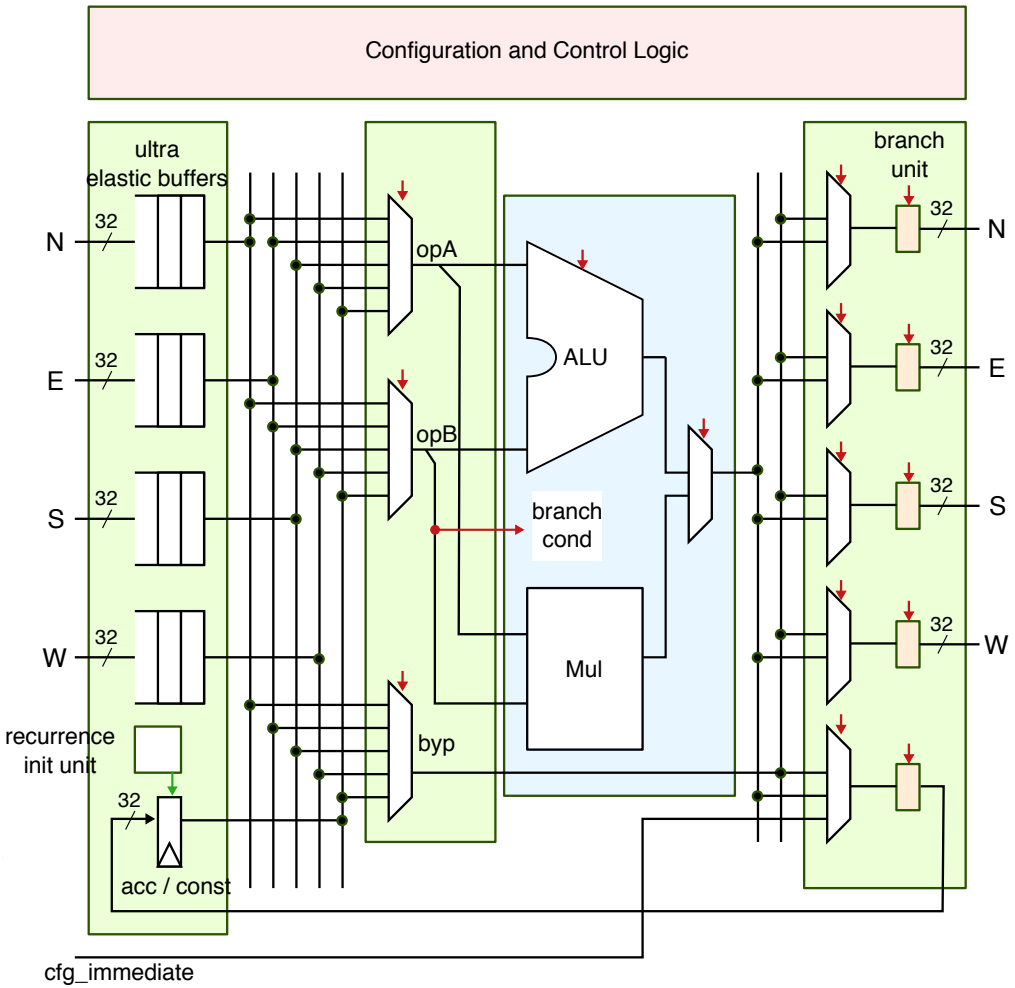

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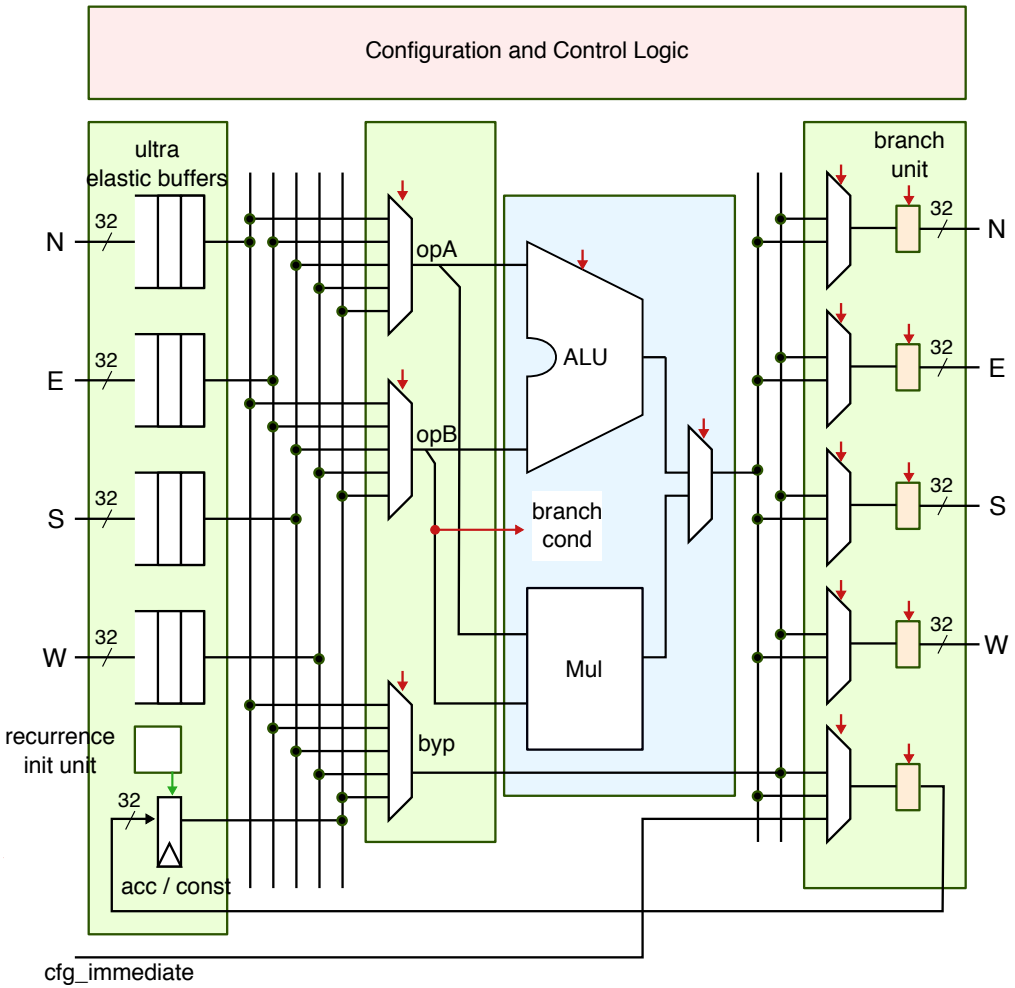

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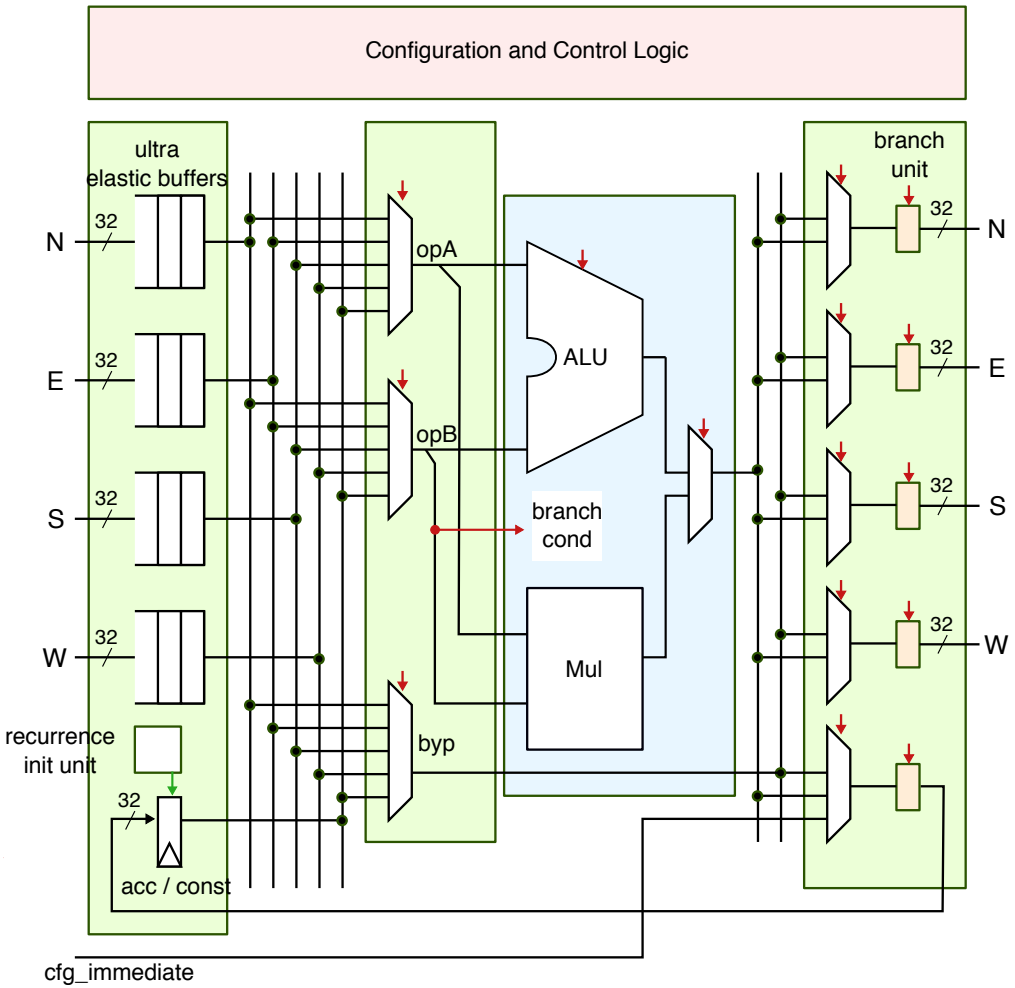

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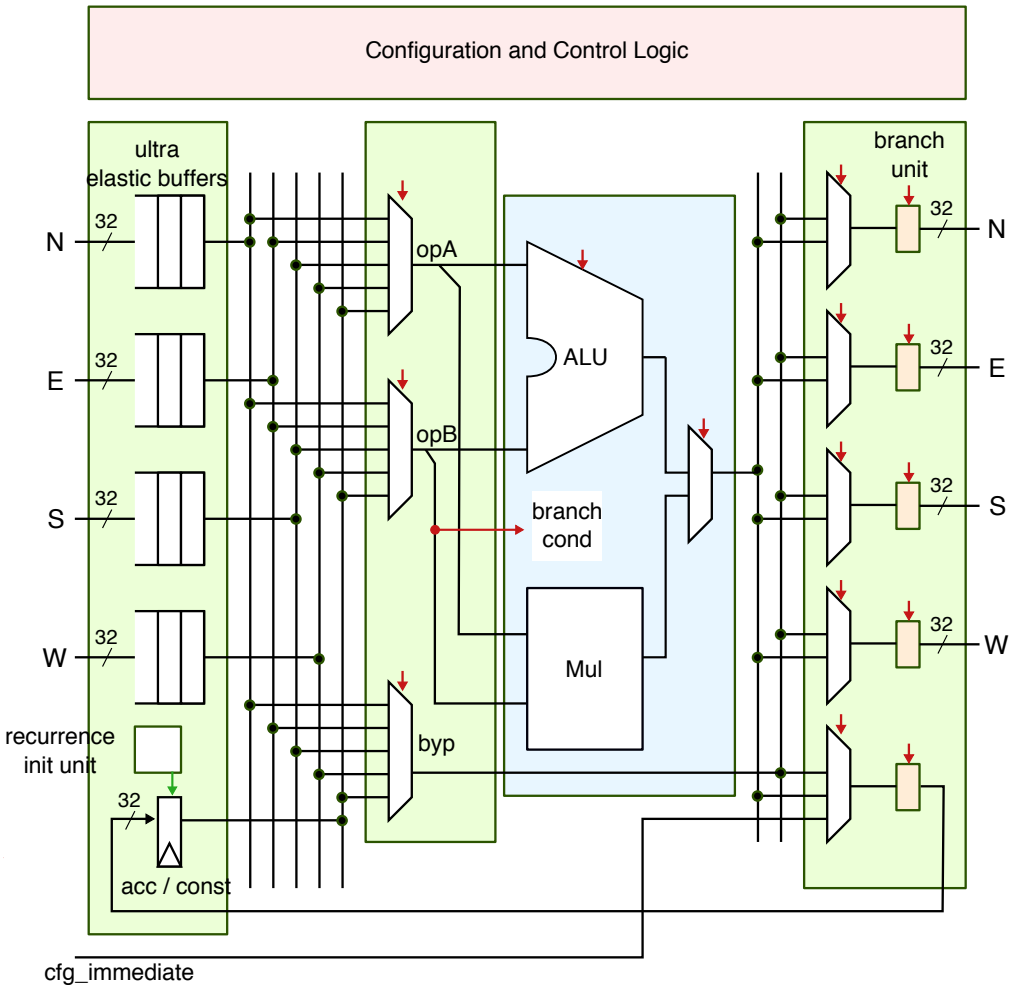

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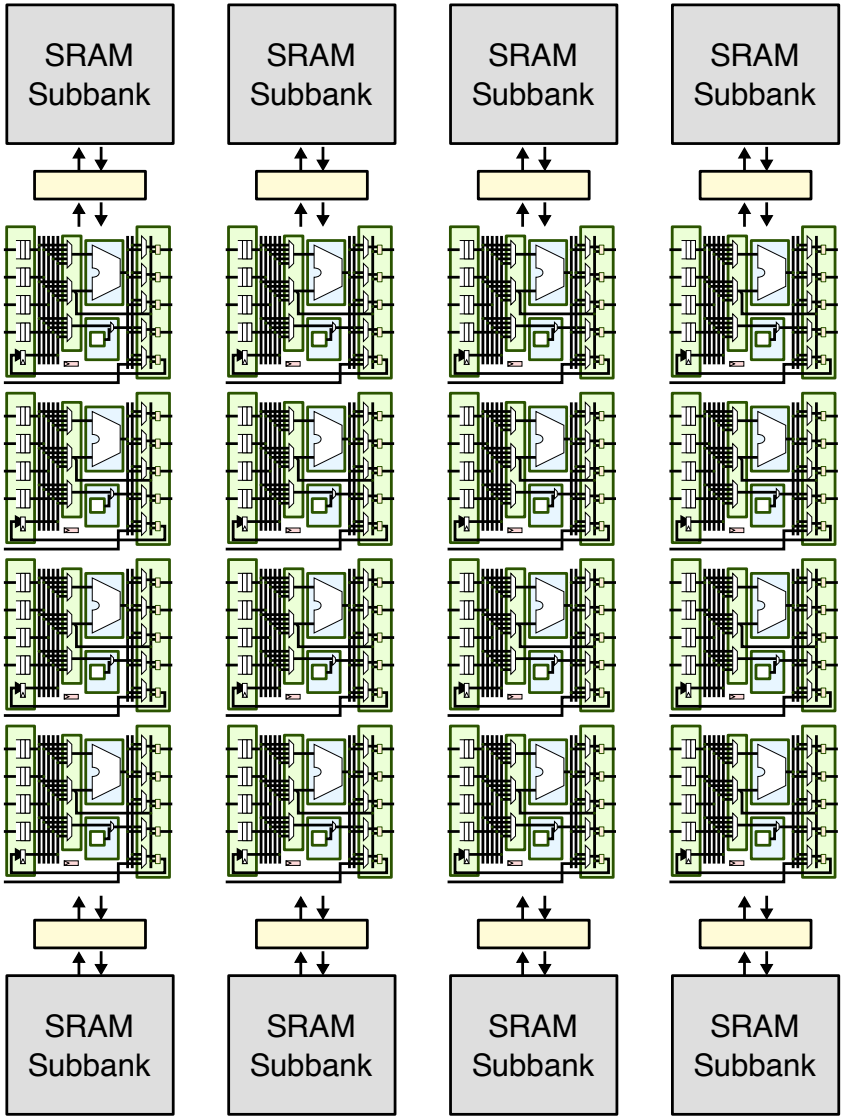
- Branching support
  - Control flow is data flow

UE-CGRA Architecture

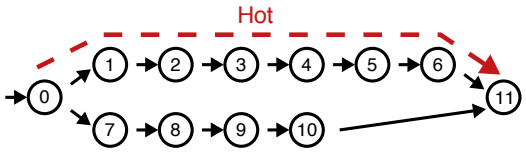


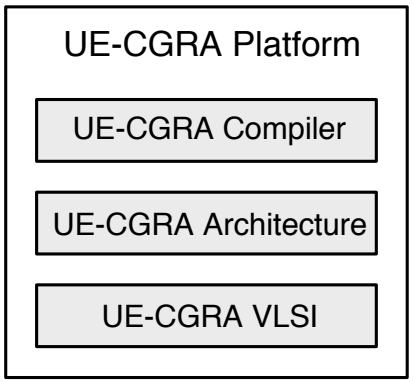
UE-CGRA composed of

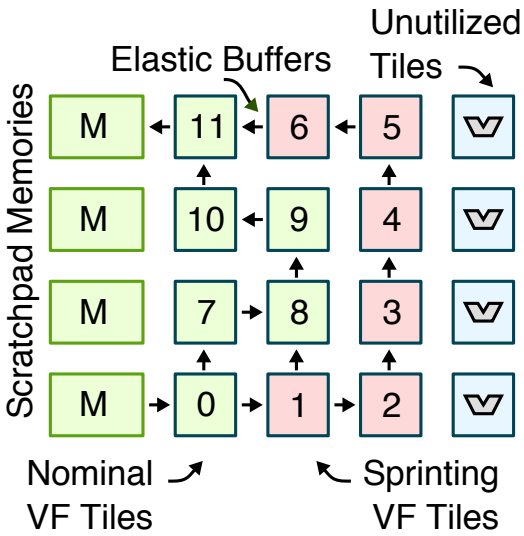
- Tiles with elastic interfaces
- SRAM subbanks
- Elastic memory adapters (similar to Huang et al. FPGA 2013)

Systolic configuration phase reuses the data network

UE-CGRA VLSI circuitry is not shown here







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  - NREs rise exponentially
  - Asynchronous clock-domain crossings are hard to verify

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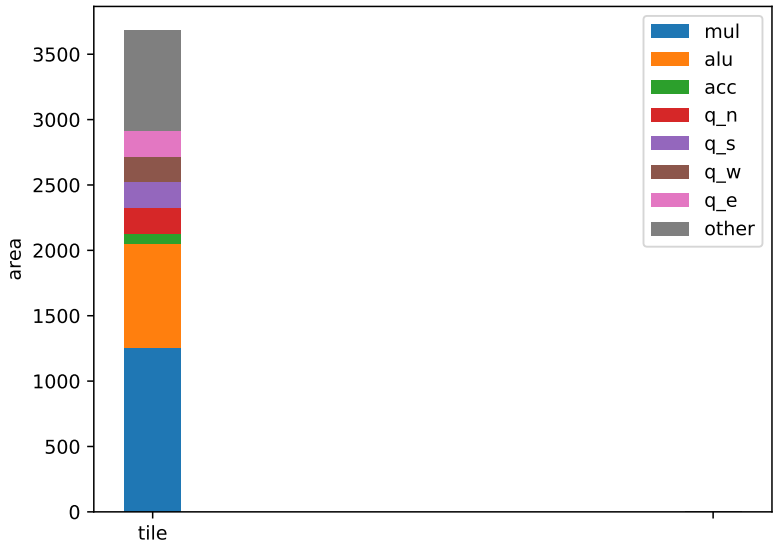
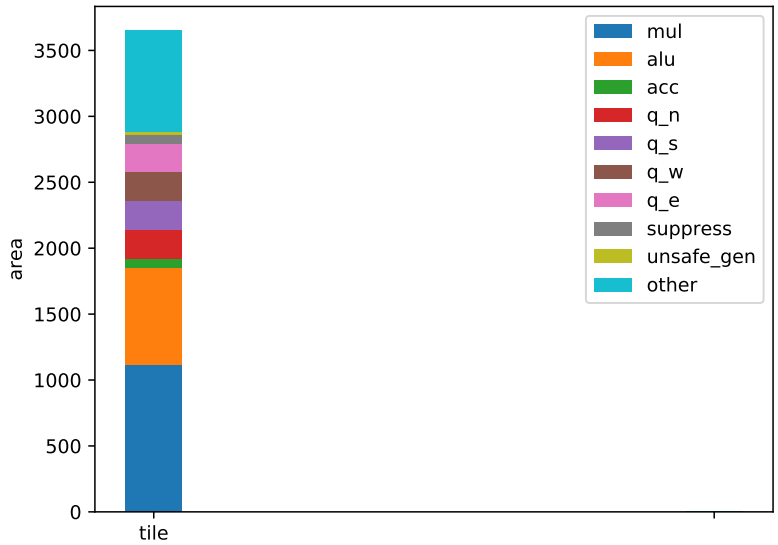
  - No level shifters are used
- Compiler optimizations
  - Functionality and leakage-aware mapping (0.61V never talks to 1.23V)
  - Energy-aware optimization pass to rest expensive operators

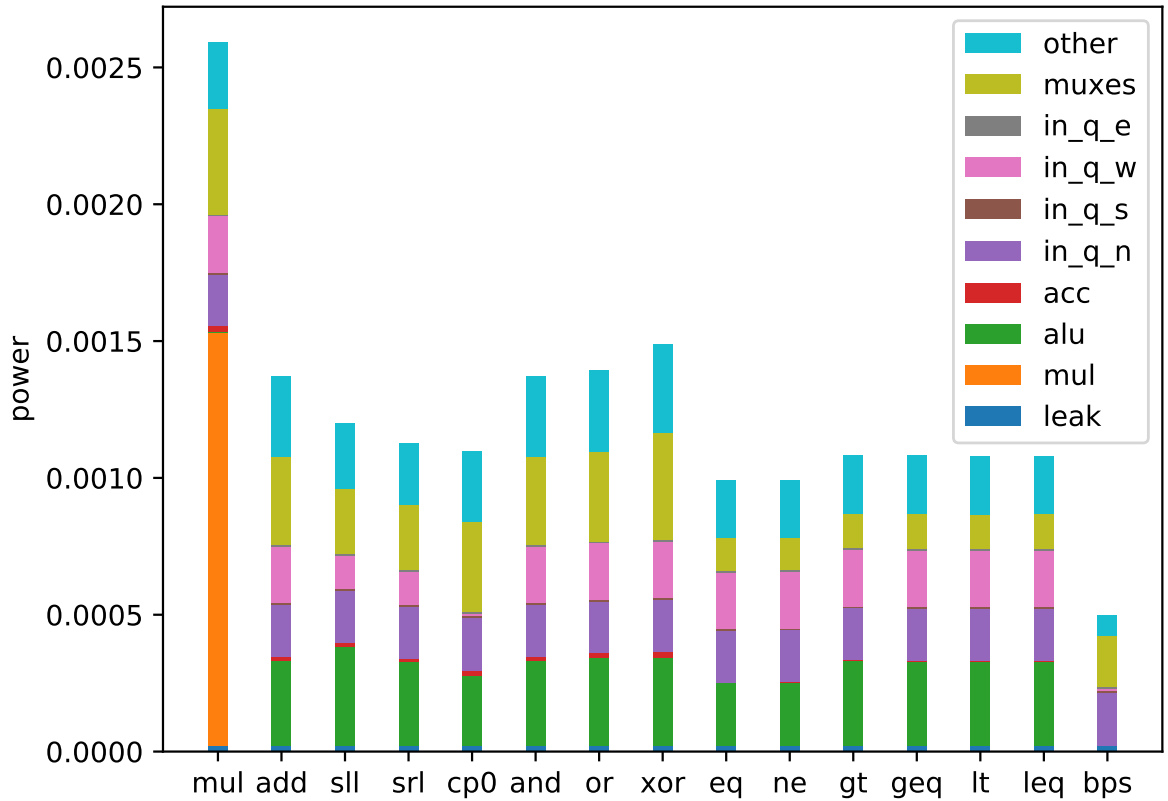
UE-CGRA Methodology – Area





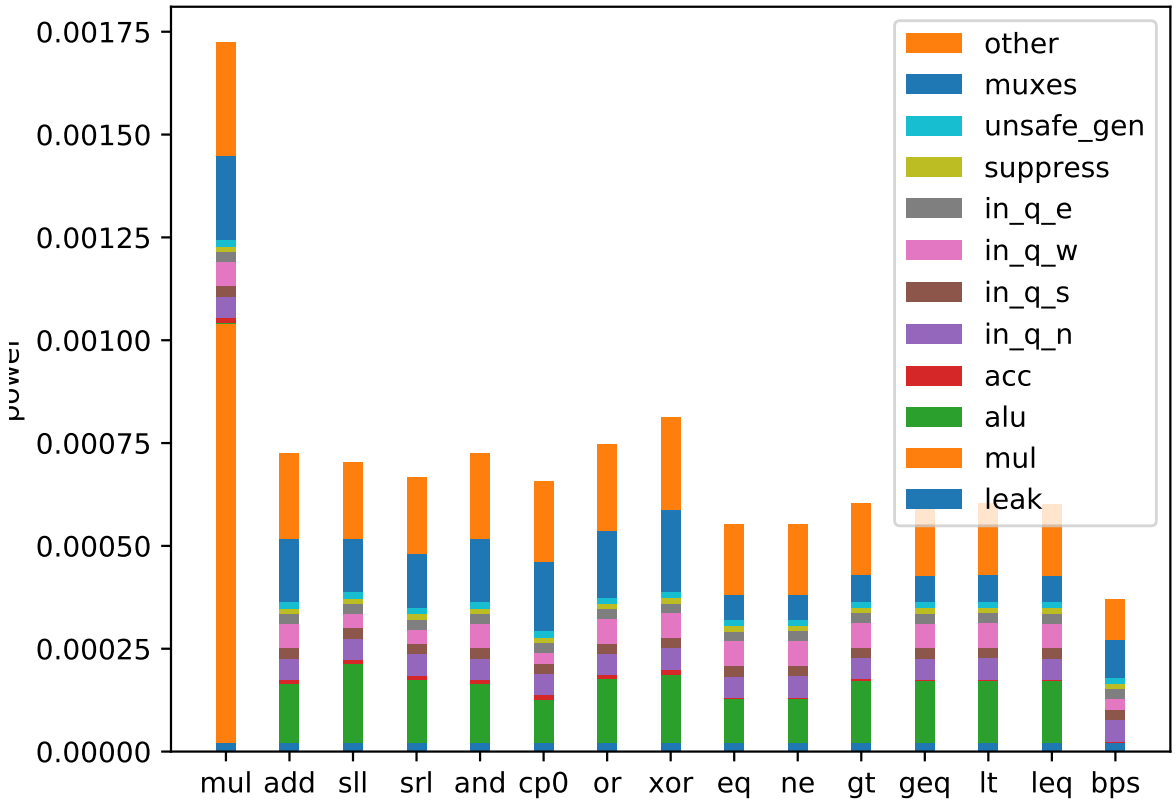
Preliminary area overhead estimates for ultra-elastic circuitry is small, but does not account for multi-rail supply voltage islands (power headers, margining between domains, more congested metal routing)

UE-CGRA Methodology – Elastic Tile Power



Preliminary power estimates show only small differences in tile-level power breakdowns with ultra-elastic circuitry, but does not account for clock tree power, leakage at crossings, power header overheads.

UE-CGRA Methodology – Ultra-Elastic Tile Power



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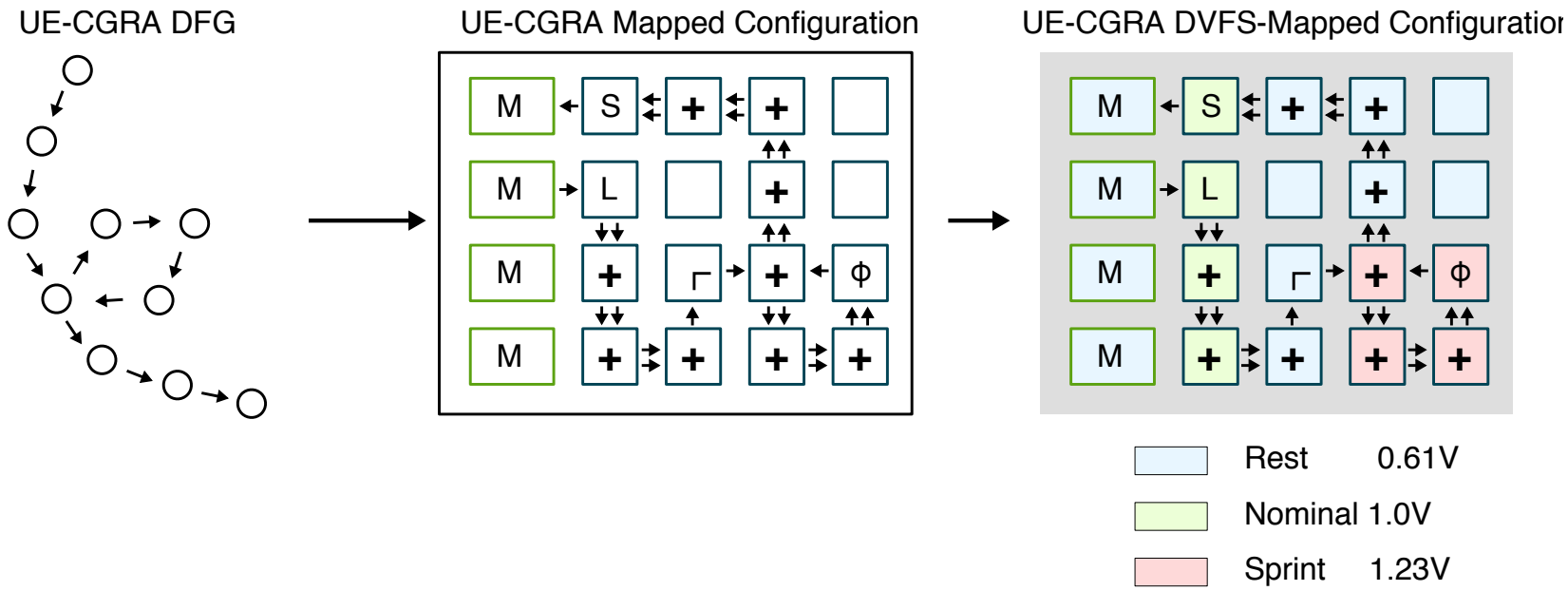
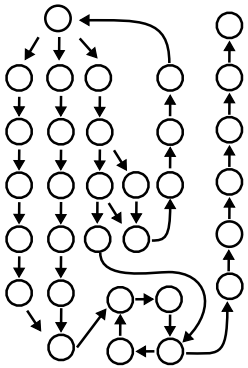
UE-CGRA Results



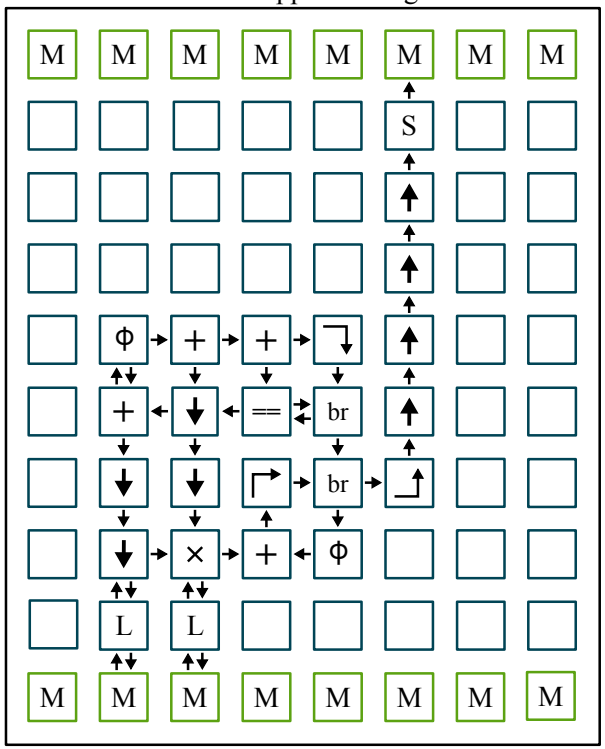
An example series-cyclic microbenchmark dataflow graph

UE-CGRA Results

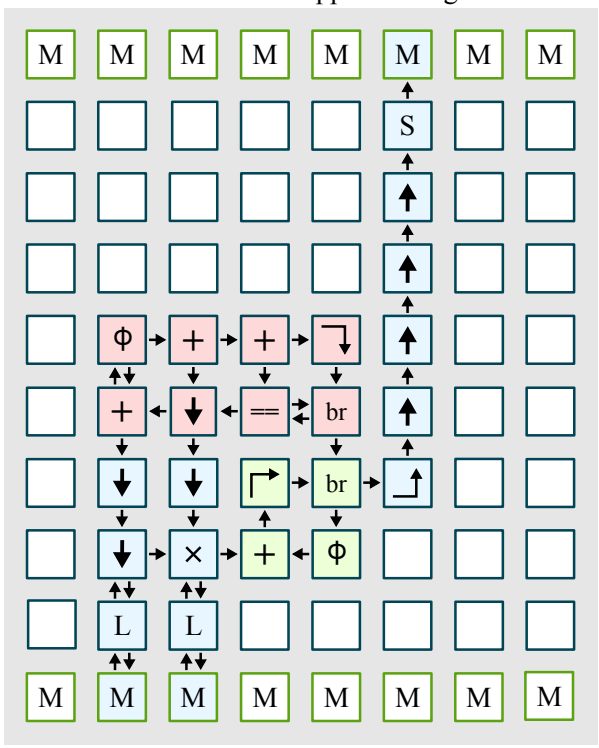
UE-CGRA DFG



UE-CGRA Mapped Configuration



UE-CGRA DVFS-Mapped Configuration



Rest 0.61V

Nominal 0.90V

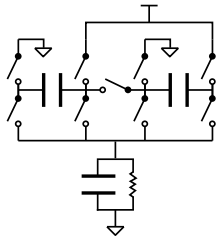
Sprint 1.23V

UE-CGRA Results

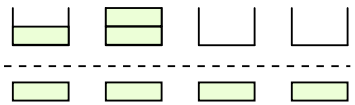
Benchmark	Iterations per Second	Energy
Series-Cyclic (base)	124018K	29.91 pJ per token
Series-Cyclic (fast)	184729K	30.56 pJ per token
Improvement	1.49 ×	0.98 ×
Series-Parallel (base)	242522K	87.21 pJ per token
Series-Parallel (fast)	275988K	93.42 pJ per token
Improvement	1.14 ×	0.93 ×
FIR (base)	62176K	43.58 pJ per token
FIR (fast)	92735K	45.81 pJ per token
Speedup	1.49 ×	0.95 ×

Preliminary results for both performance and energy efficiency for an 8×8 array

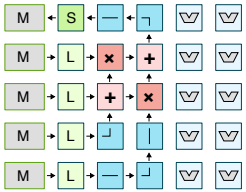
Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry



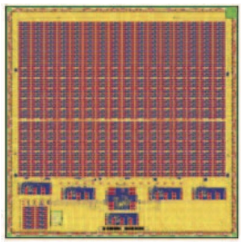
Exploiting Fine-Grain Asymmetry with
On-Chip Voltage Regulation - **MICRO'14**, IEEE TCAS I'18



Exploiting Fine-Grain Asymmetry in
Task-Based Parallel Runtimes - **ISCA'16**, MICRO'17, RISCV'18



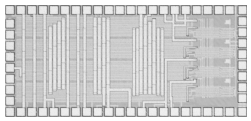
Exploiting Fine-Grain Asymmetry in
Coarse-Grain Reconfigurable Arrays - **Unpublished**



Exploiting Fine-Grain Asymmetry with
Silicon Prototyping - **IEEE MICRO'18**, DAC'18, Hotchips'17

Conclusion

Silicon Prototyping

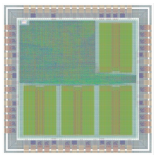


DCS (2014)

TSMC 65nm
1mm x 2.2mm
[TCAS'18, MICRO'14]

Research Purpose

Directly implement and characterize the voltage regulator designs supporting dynamic capacitance sharing

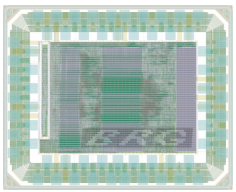


BRGTC1 (2016)

IBM 130nm
2mm x 2mm
[Poster at HOTCHIPS'16]

Research Purpose

Silicon-validate PyMTL-generated RTL

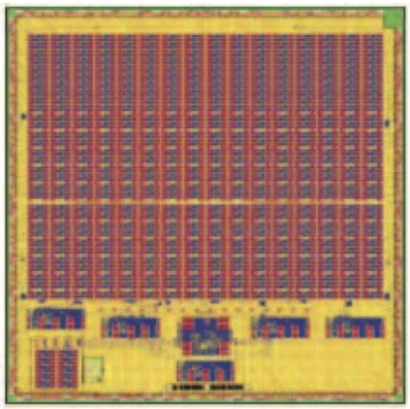


BRGTC2 (2018)

TSMC 28nm
1mm x 1.25mm
[WOSET'18, RISCV'18]

Research Purpose

Explore preliminary new ideas on hardware optimization for task-based parallel runtimes and also silicon-validate PyMTL in a more advanced node



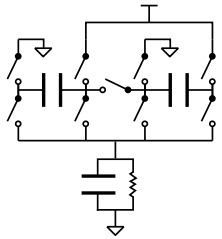
Celerity (2017)

TSMC 16nm FinFET
5mm x 5mm
[IEEE-MICRO'18
CARRV'17
HOTCHIPS'17]

Research Purpose

Explore a range of productive hardware design and verification tools -- synthesizable analog IP (PLL, digital LDO), high-level synthesis (complex HLS-generated BNN accelerator), Python-based HDLs, area-efficient and high-bandwidth manycore networks (496-core RISC-V tiled manycore), and open-source generators.

Software, Architecture, and VLSI Co-Design for Exploiting Fine-Grain Asymmetry



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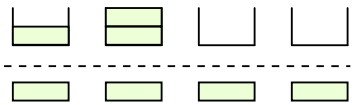
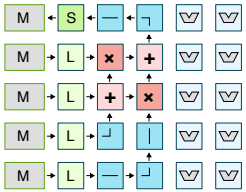


Exploiting Fine-Grain Asymmetry in
Task-Based Parallel Runtimes - **ISCA'16**, MICRO'17, RISCV'18



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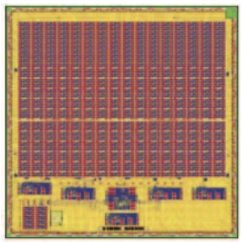

Exploiting Fine-Grain Asymmetry with
Silicon Prototyping - **IEEE MICRO'18**, DAC'18, Hotchips'17

Conclusion

Acknowledgements and Funding

Acknowledgements and Funding

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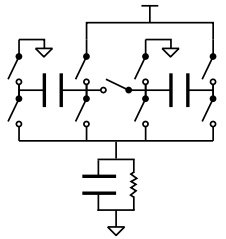
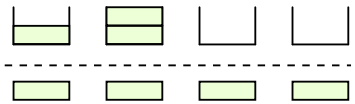
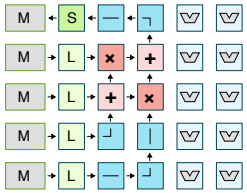
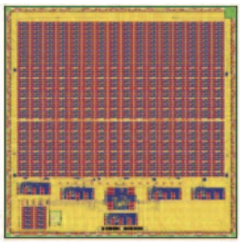
- **BRGTC1/2**: Shunning Jiang, Khalid Al-Hawaj, Ivan Bukreyev, Berkin Ilbeyi, Tuan Ta, Lin Cheng, Julian Puscar, Ian Galton, Moyang Wang, Bharath Sudheendra, Nagaraj Murali, Suren Jayasuriya, Shreesha Srinath, Taylor Pritchard, Robin Ying, Christopher Batten

Takeaway Points









Parallelism and specialization are increasing on-chip **fine-grain asymmetry**, which must be managed by similarly **fine-grain power-control techniques**

Controlling these techniques through **cross-stack co-design** can enable:

- Smaller area for *integrated voltage regulation*
- Asymmetry-aware *task-based parallel runtimes*
- More efficient *elastic CGRAs*

Thank you!