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Project 06 – Memory and Write back

Procedure

This lab was the last to finish up the stages of the DLX processor. This required that we implement the data memory as well as the ability to write back to the registers. We had already written the data .mif files so setting up the data RAM was as simple as implementing the Quartus IP RAM and connecting it to the project. Then implementing the memory and write back stages was significantly easier than previous stages.

Once all of the stages were connected in the top level, the processor was ready to go and we just needed to write the testbench. The testbench was rather trivial this time around, because the processor is now capable of running the instructions in memory on its own, so we essentially just supplied the clock.

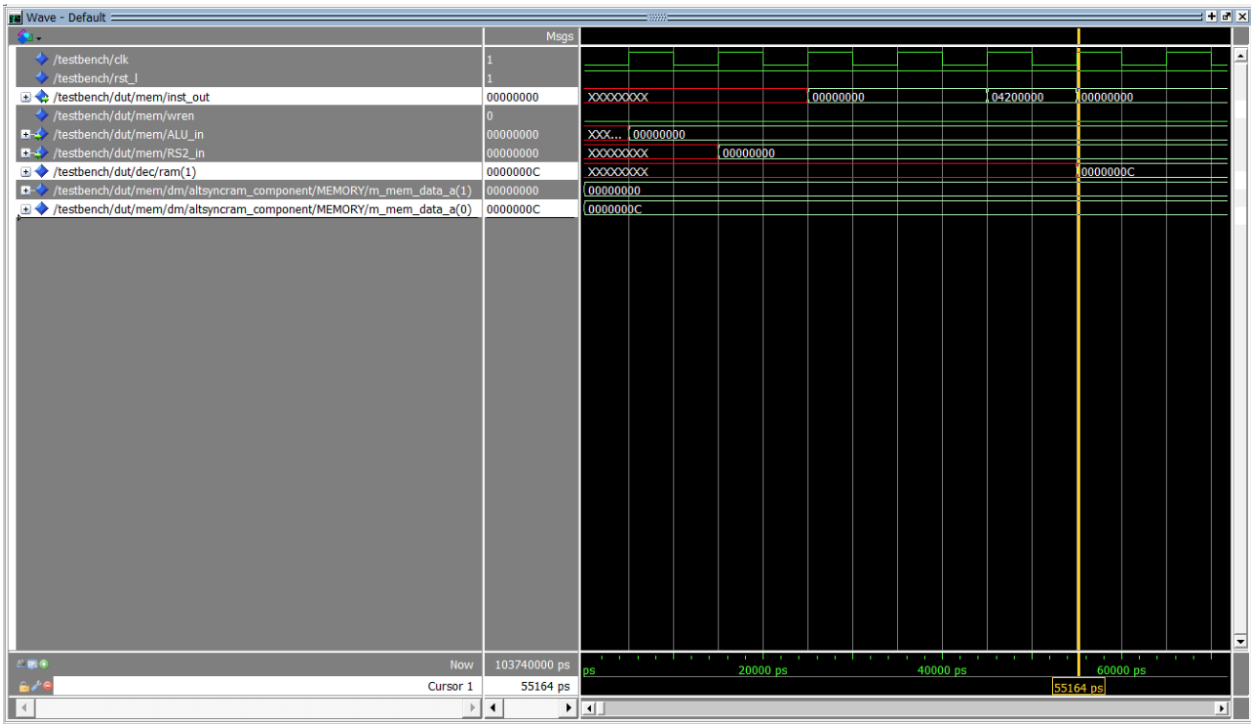

Figure 1: The last two rows are the data_memory, the third to last is the ram address where the initial number and then the result are stored.

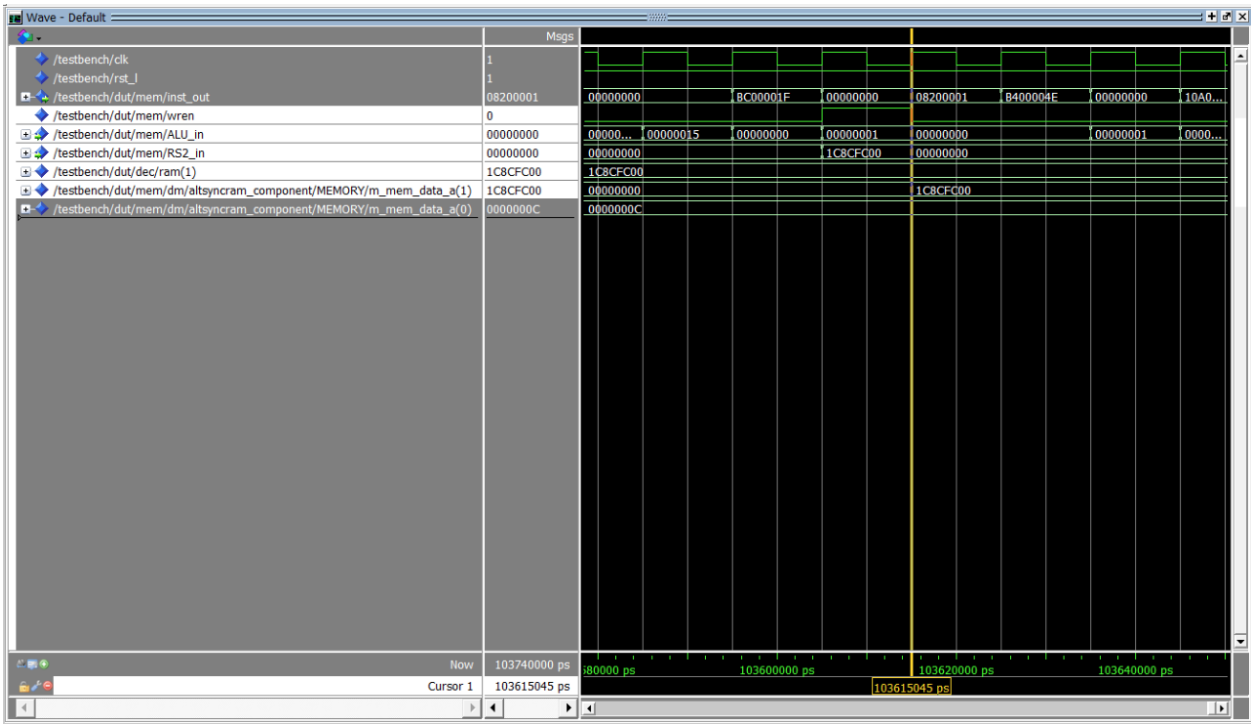

Figure 2: Showing 0x1C8CFC00 as the result, or base 10: 479,001,600

Results

We were successful in creating the final stages, and were able to show the 12! Computation.

Conclusions

This project was a success, and we completed the memory and write back stages as well as the testbench to go with it.