Calvin Passmore

ECE 6470

# Homework 4

# Problem 1

You are synthesizing a chip composed of random logic with an average activity factor of 0.1. You are using a standard cell process with an average switching capacitance of 450 pF/mm2. Estimate the dynamic power consumption of your chip if it has an area of 70 mm2 and runs at 450 MHz at VDD=0.9V.

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$P_{dynamic} = P_{switching} + P_{shortcircuit}$

$P_{shortcircuit} \approx 0$

$P_{switching} = \alpha C V_{DD}^2 f$

In [ ]:
```
# P switching
alpha = 0.1
C_A = 450e-12 # pf/mm2
A = 70 # mm2
C = C_A * A # pf
f = 450e6
Vdd = 0.9

alpha * C * Vdd**2 * f
```

Out[ ]:
```
1.1481750000000002
```

$P_{dynamic} = 1.148$

# Problem 2

Determine the activity factor for the signal shown in Figure 5.34. The clock rate is 1 GHz

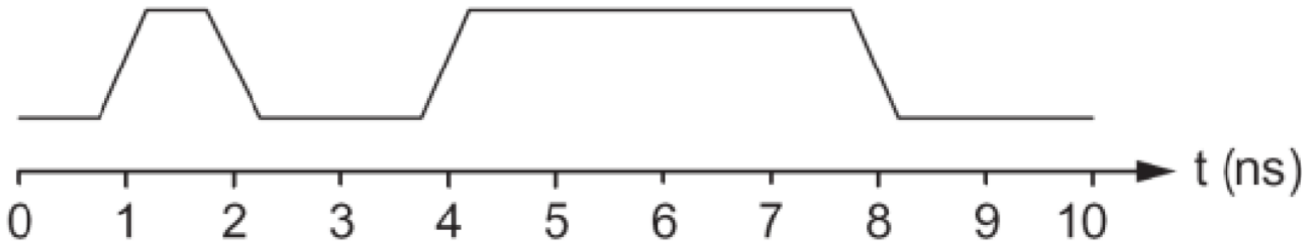


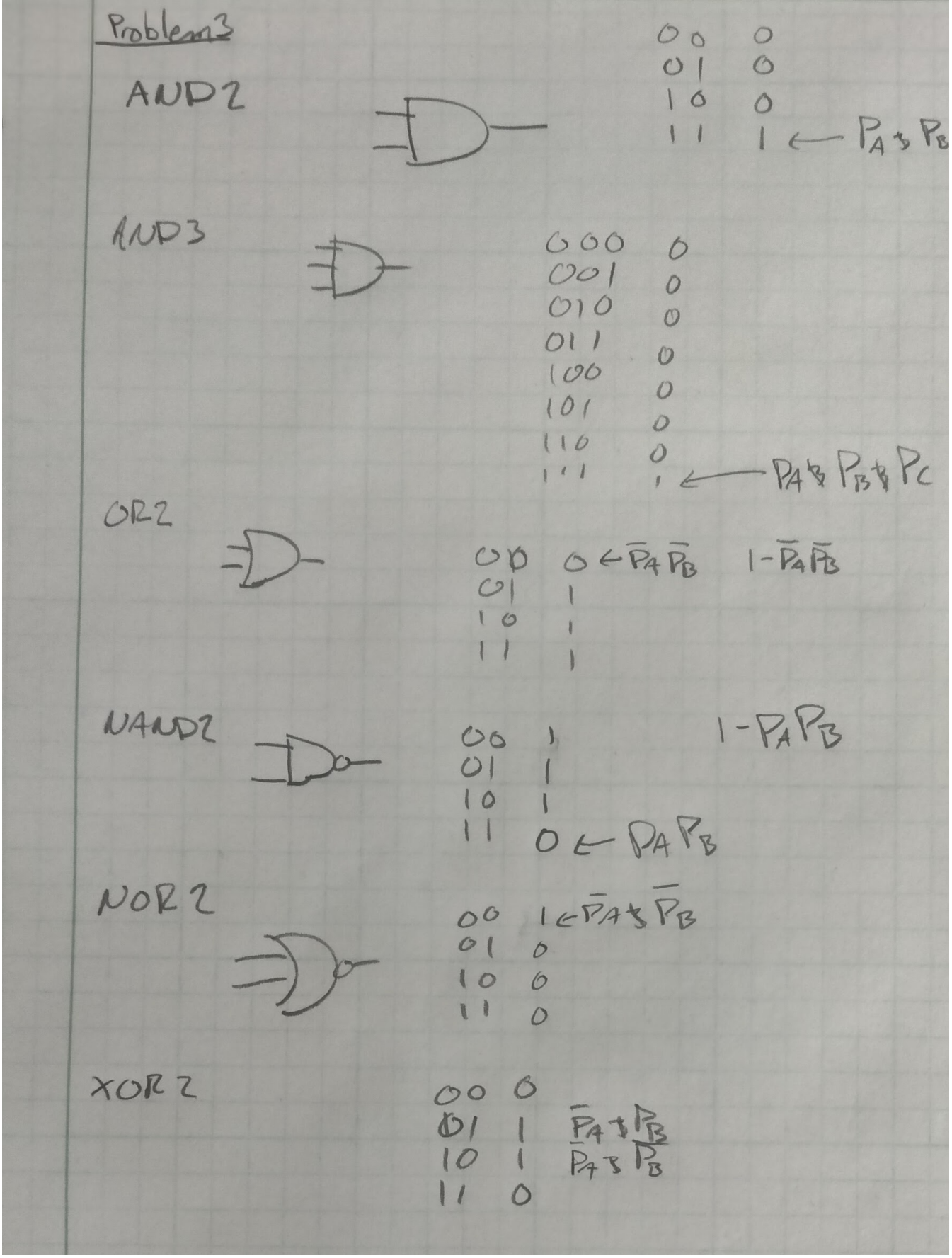

**FIGURE 5.34** Signal for Exercise 5.4

The activity factor is 1/2 because out of 10 clock cycles, 5 of them are high, and 5 are low.

# Problem 3

Derive the switching probabilities in Table 5.1.

| Gate | $P_Y$ |
|---|---|
| AND2 | $P_A P_B$ |
| AND3 | $P_A P_B P_C$ |
| OR2 | $1 - \overline{P}_A \overline{P}_B$ |
| NAND2 | $1 - P_A P_B$ |
| NOR2 | $\overline{P}_A \, \overline{P}_B$ |
| XOR2 | $P_A \overline{P}_B + \overline{P}_A P_B$ |




## Problem 4

Construct a table similar to Table 5.2 for a 2-input NOR gate. (Assuming Vs is between A and B PMOS)

Ign = 6.3nA Igp = 0

Ioffn = 5.6nA Ioffp = 9.3nA

| Input State | $I_{sub}$ | $I_{gate}$ | $I_{total}$ | Vx |
|---|---|---|---|---|
| 00 | 11.2 | 0 | 11.2 | Stack Effect |
| 01 | 9.3 | 6.3 | 15.6 | Vt |
| 10 | 9.3 | 6.3 | 15.6 | 1 |
| 11 | ≈1 | 12.6 | 13.6 | 1 |