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ECE 6470

Homework 3

Problem 1

(10.3) For each of the following sequencing styles, determine the minimum logic contamination delay in each clock cycle (or half-cycle, for two-phase latches). Assume there is zero clock skew.

a. Flip-flops

b. Two-phase transparent latches with 50% duty cycle clocks

c. Two-phase transparent latches with 60 ps of nonoverlap between phases

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a. tcd ≥ thold - tccq = 30ps-50ps = -20ps

b. tcd ≥ thold - tccq - tnonoverlap = 30ps - 50ps - 0 = -20ps

c. tcd ≥ thold - tccq - tnonoverlap = 30ps - 50ps - 60 = -80ps

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Problem 2

(10.4) Repeat Exercise 1 if the clock skew between any two elements can be up to 50 ps.

Contamination delay is the 'best case' delay to the start of a signal change, since the clock scew can be **up to** 50 ps, it could be 0ps. In this case the answers would be the same as Problem 1. However, this isn't an interesting or different problem, so I'm assuming the clock skew **is** 50ps and switching happens on exactly Vdd/2 or 25ps.

a. tcd ≥ thold - tccq + tskew = 30ps - 50ps + 50ps = 30ps

b. tcd ≥ thold - tccq - tnonoverlap + tskew = 30 - 50 - 0 + 50 = 30ps

c. tcd ≥ thold - tccq - tnonoverlap + tskew = 30 - 50 - 60 + 50 = -30ps

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Problem 3

(10.5) Suppose one cycle of logic is particularly critical and the next cycle is nearly empty. Determine the maximum amount of time the first cycle can borrow into the second for each of the following sequencing styles. Assume there is zero clock skew and that the cycle time is 500 ps.

a. Flip-flops

b. Two-phase transparent latches with 50% duty cycle clocks

c. Two-phase transparent latches with 60 ps of nonoverlap between phases

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a. tborrow ≤ Tc/2 - (tsetup + tnonoverlap) = 500/2 - 65 - 0 = 185ps

b. tborrow ≤ Tc/2 - (tsetup + tnonoverlap) = 500/2 - 25 - 0 = 225ps

c. tborrow ≤ Tc/2 - (tsetup + tnonoverlap) = 500/2 - 25 - 60 = 165ps

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Problem 4

(10.6) Repeat Exercise 3 if the clock skew between any two elements can be up to 50 ps.

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a. tborrow ≤ Tc/2 - (tsetup + tnonoverlap) + tskew = 500/2 - 65 - 0 + 50 = 235ps

b. tborrow ≤ Tc/2 - (tsetup + tnonoverlap) + tskew = 500/2 - 25 - 0 + 50 = 275ps

c. tborrow ≤ Tc/2 - (tsetup + tnonoverlap) + tskew = 500/2 - 25 - 60 + 50 = 215 ps

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Problem 5

(10.8) Consider a flip-flop built from a pair of transparent latches using nonoverlapping clocks. Express the setup time, hold time, and clock-to-Q delay of the flip-flop in terms of the latch timing parameters and tnonoverlap , relative to the rising edge of φ1.

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tff_setup = tl_setup + tl_dq

tff_hold = tl_hold

tff_cq = tl_cq

Problem 6

(10.9) For the path in Figure 10.54, determine which latches borrow time and if any setup time violations occur. Repeat for cycle times of 1200, 1000, and 800 ps. Assume there is zero clock skew and that the latch delays are accounted for in the propagation delay.

a. Δ1 = 550 ps; Δ2 = 580 ps; Δ3 = 450 ps; Δ4 = 200 ps

b. Δ1 = 300 ps; Δ2 = 600 ps; Δ3 = 400 ps; Δ4 = 550 ps

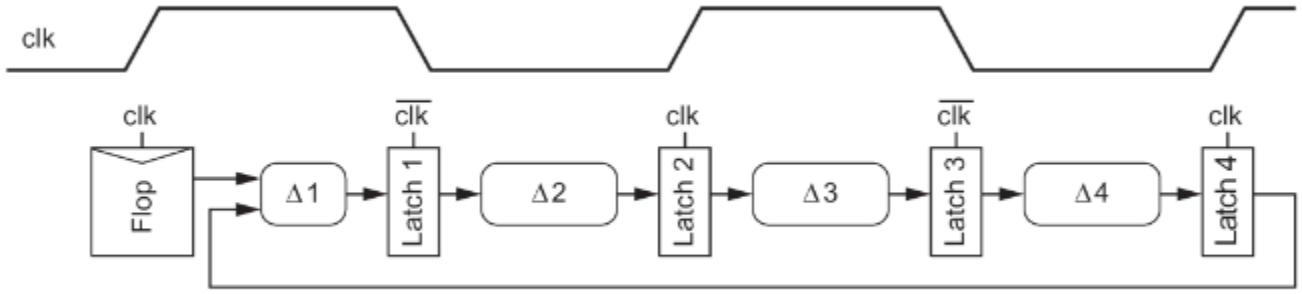

FIGURE 10.54 Example path

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a.

	1200	1000	800
Borrow time	None	1 would borrow from 2 which would them borrow from 3 which would borrow from 4	They would all have to borrow from eachother
Setup Violations	None	No setup violations would be present	1-3 have setup time violations, 4 doesn't on it's own, but when 3 tries to borrow it's time it will result in a violation

b.

	1200	1000	800
Borrow time	None	2 would borrow 100 from 3, and 4 would borrow from 1	2 would borrow from 3 which would borrow from 4 which would borrow from 1
Setup Violations	None	None	2-4 have setup time violations