Problem 5

(10.8) Consider a flip-flop built from a pair of transparent latches using nonoverlapping clocks. Express the setup time, hold time, and clock-to-Q delay of the flip-flop in terms of the latch timing parameters and tnonoverlap , relative to the rising edge of φ1.

---

tff_setup = tl_setup + tl_dq

tff_hold = tl_hold

tff_cq = tl_cq

Problem 6

(10.9) For the path in Figure 10.54, determine which latches borrow time and if any setup time violations occur. Repeat for cycle times of 1200, 1000, and 800 ps. Assume there is zero clock skew and that the latch delays are accounted for in the propagation delay.

a. Δ1 = 550 ps; Δ2 = 580 ps; Δ3 = 450 ps; Δ4 = 200 ps

b. Δ1 = 300 ps; Δ2 = 600 ps; Δ3 = 400 ps; Δ4 = 550 ps

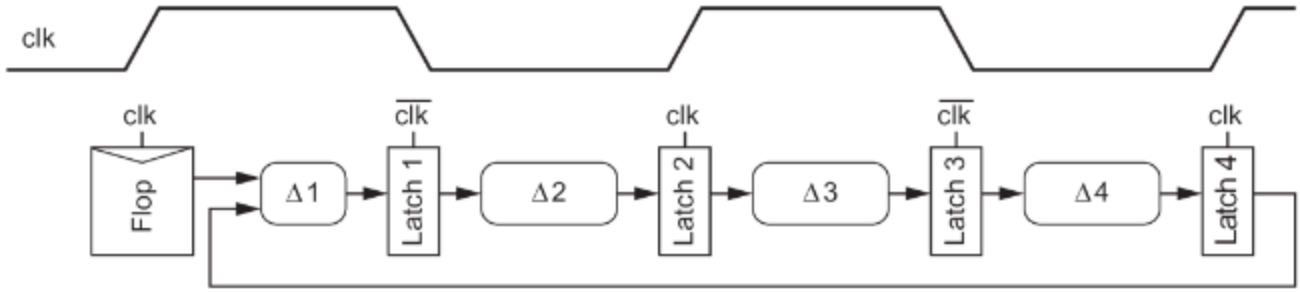

FIGURE 10.54 Example path

---

a.

	1200	1000	800
Borrow time	None	1 would borrow from 2 which would them borrow from 3 which would borrow from 4	They would all have to borrow from eachother
Setup Violations	None	No setup violations would be present	1-3 have setup time violations, 4 doesn't on it's own, but when 3 tries to borrow it's time it will result in a violation

b.

	1200	1000	800
Borrow time	None	2 would borrow 100 from 3, and 4 would borrow from 1	2 would borrow from 3 which would borrow from 4 which would borrow from 1

	1200	1000	800
Setup Violations	None	None	2-4 have setup time violations