Optical sensor communication to FPGA and HPS

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1 Concept description

To measure the movement of a slot car an optical mouse sensor will be used (ADNS-3080). The communication between sensor and FPGA is a state machine, which is reading product ID (address: 0x00) - valid value is 0x17.
After receiving valid product ID the burst register (address: 0x50) will be read. If the first byte (motion register) has the value 0x80 a new motion is detected and the X/Y data will be sent to firmware using Avalon bus to HPS.

2 ADNS 3080

The optical sensor can communicate via MISO and MOSI wire, controlled by SCLK (system clock), NCS (negated chip select), RST (reset for sensor) and NPD (negated power down).
For further information of receiving data please read the datasheet of ADNS 3080 (adns_3080.pdf).

3 FPGA Cyclone V and SoC

3.1 Read burst register of optical sensor

To read the burst register the FPGA component is the master for slave sensor. The FPGA is controlling all inputs to ADNS 3080 refering to the communication protocol in ADNS 3080 datasheet. After reseting sensor the product ID will be received. After that the burst register will be read and each difference in X or Y will be sent to HPS.

3.2 Avalon to sensor communication

The Avalon bus is used to send the data from sensor component to HPS. This bus is created in QSYS with a distributed memory. The firmware is able to read the data from these memory addresses now (defined in hps_0.h).