BTN8960 /62 /80 /82

NovalithIC™

High Current PN Half Bridge

Application Note

Rev. 0.4, 2015-07-02

Automotive Power

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1 Abstract

Note: The following information is only given to help with the implementation of the device and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This Application Note is intended to provide information and hints for a high current design, using PWM control with the NovalithIC™ half-bridge family BTN8960 /62 /80 /82 for the automotive environment.

This contains one P-channel high side MOSFET and with an integrated driver IC in one package. The NovalithIC™ is the interface between the microcontroler and the motor, equipped with diagnostic and protection functions.

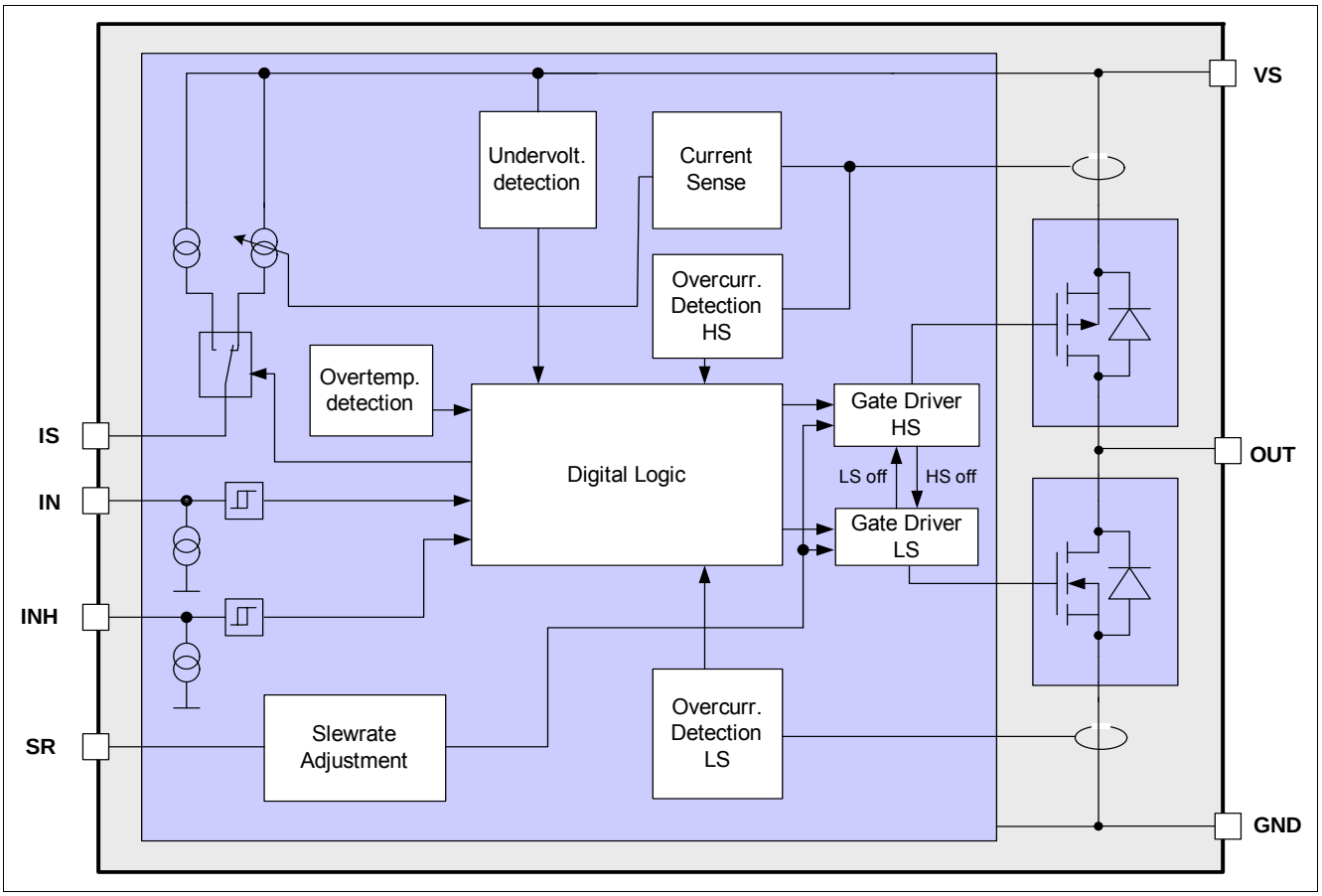

Figure 1 Block Diagram BTN8960 /62 /80 /82

2 Motor Configurations

Electrical motors are built with various architectures. Mechanically commutated motors with brushes, so called DC motors or electrically commutated motors, so called BLDC motors (Brush Less DC motors). The NovalithIC™ family can support all of them due to, the flexibility of the half-bridge concept.

Using NovalithIC™ controlling a DC-motor has the following advantages:

- Extremely low parasitic inductances between high side and low side MOSFET.
- Optimized switching performance of the MOSFET's to reduce power losses and EMC emission.
- Driving the motor with PWM for torque and speed control.
- Integrated freewheeling transistor.
- Integrated current measurement.
- Integrated diagnosis and protection.
- Microcontroller -compatible input pins.
- Small and PCB-area saving package.

2.1 Half-bridge configuration for mono-directional motor control

Figure 2 shows the design of a mono-directional motor control with NovalithIC™. In most cases, the motor is connected between "OUT" and "GND". This is because the chassis of a car is "GND", and therefore a short to "GND" is much more probable than a short to "V_S". For this reason it is statistically safer with a motor connected to "GND", because if a short accures in this case, the motor is not running.

Generally, it is also possible to use the NovalithIC™ to drive the motor between "OUT" and "V_S". The inverted "IN" signal must be respected.

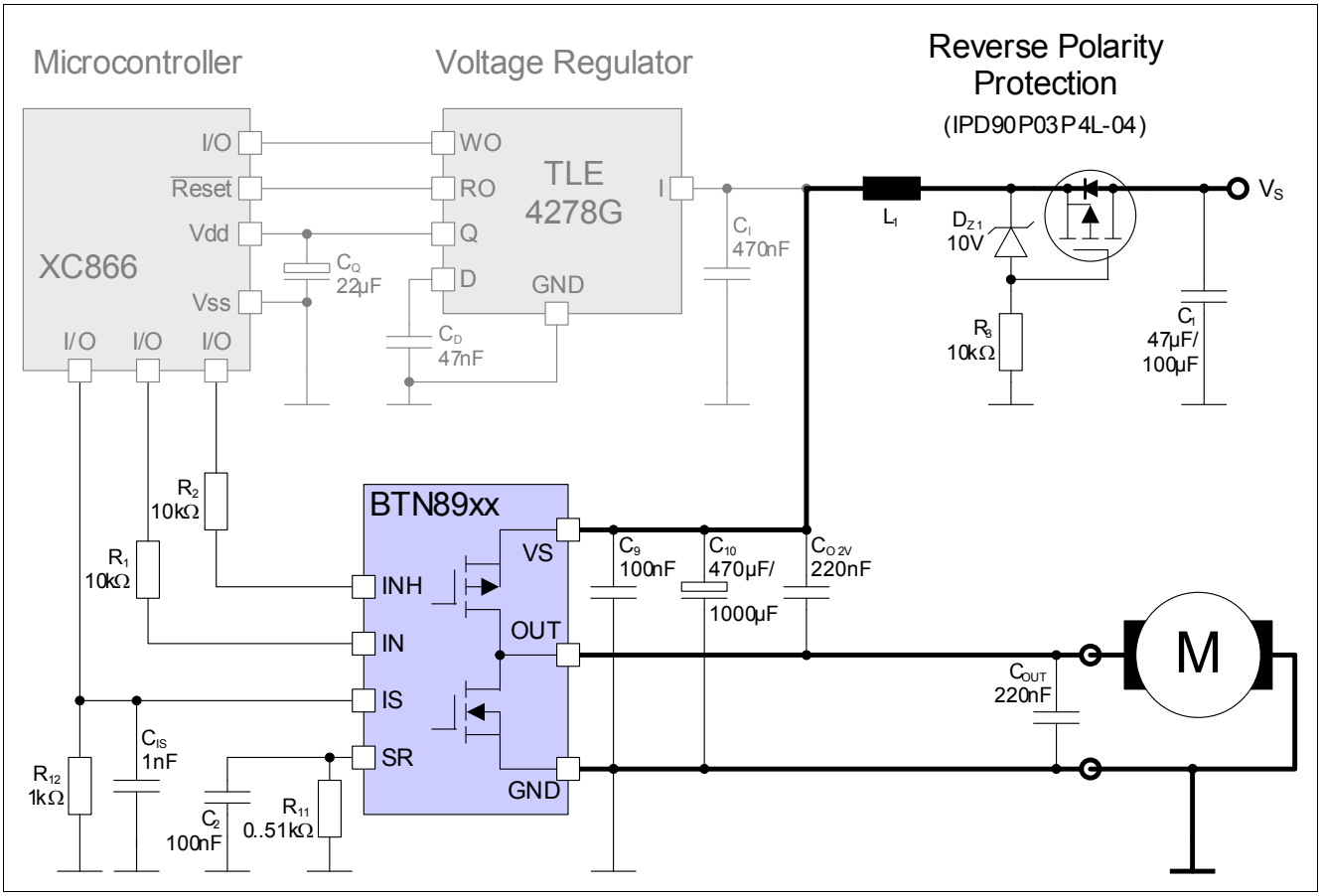

Figure 2 Application circuit for a monodirectional motor with BTN8960 /62 /80 /82

2.2 H-Bridge configuration for bidirectional motor control

With the NovalithIC™ family it is easy to build an H-bridge for bidirectional DC motor control by simply combining two devices in H-bridge configuration, as it is shown in **Figure 3**.

Motor Configurations

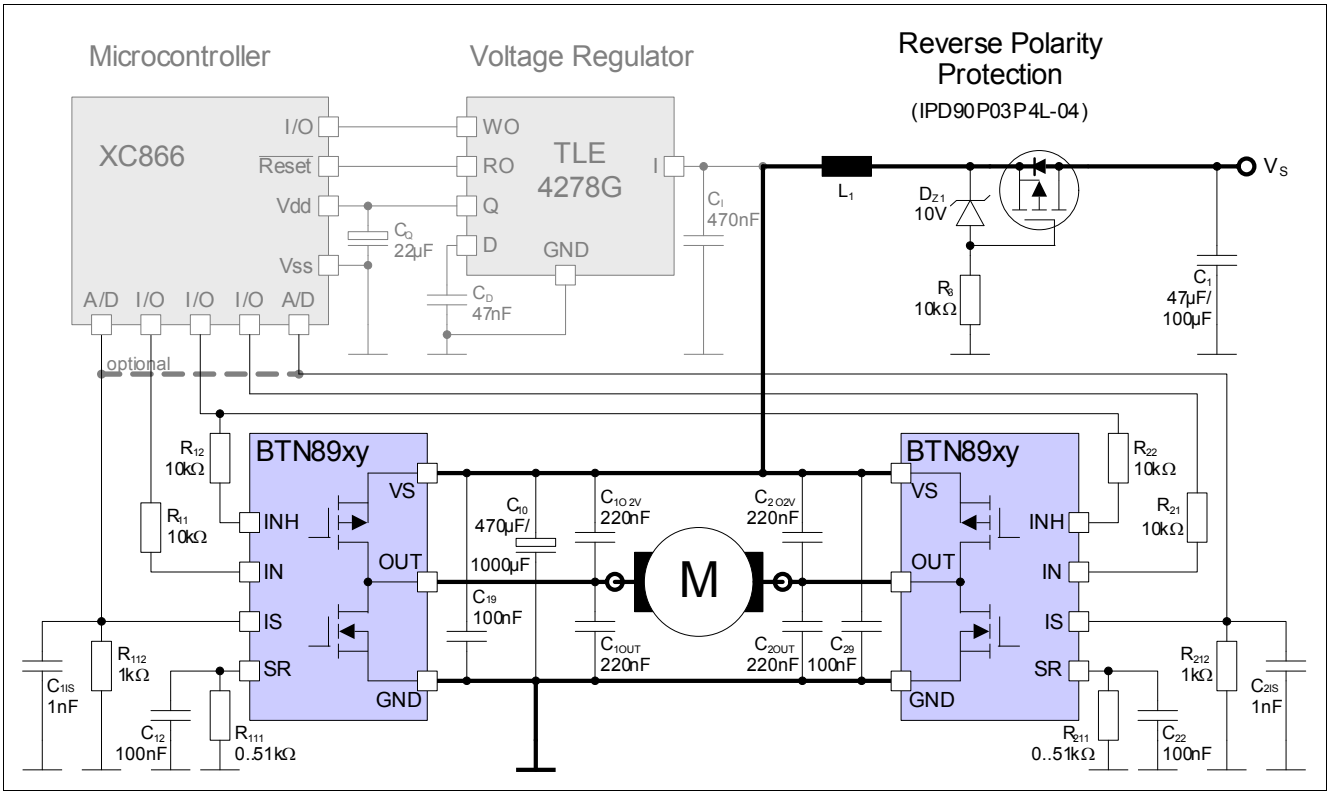

Figure 3 Application circuit for a bidirectional motor with BTN8960 /62 /80 /82 H-bridge

3 Parasitic Inductance

In high-current applications, which the NovalithIC™ family is designed for, special care must be taken for parasitic inductors. The same is valid in case of very high frequencies, which are interesting with regard to EMC considerations.

Each kind of wire in the application is an inductor, e.g. PCB wires, bond wires, etc. The wire inductance can be estimated with

- 1mm PCB wire length approximately 1.2 nH
- 1 PCB via approximately 1 nH

The voltage drop of a wire can be calculated in the following way:

$$U_L = L \cdot \frac{dI}{dt} \tag{3.1}$$

As can be seen from this equation, care must be taken with the parasitic wire inductors with increasing current and decreasing switching time. The NovalithIC™ is designed to switch high currents very quickly. This means in applications with NovalithIC™, the parasitic inductors are relevant and special care must be taken.

3.1 Measuring signals at NovalithIC™

The parasitic inductance also has an influence on the measurement results. To measure the true signals at the NovalithIC™ it is mandatory to position the measurement probes directly at the device, as it is shown in **Figure 4**. The probe is connected directly to the V_s-pin of the NovalithIC™ and the reference signal directly to the GND-pin of the device.

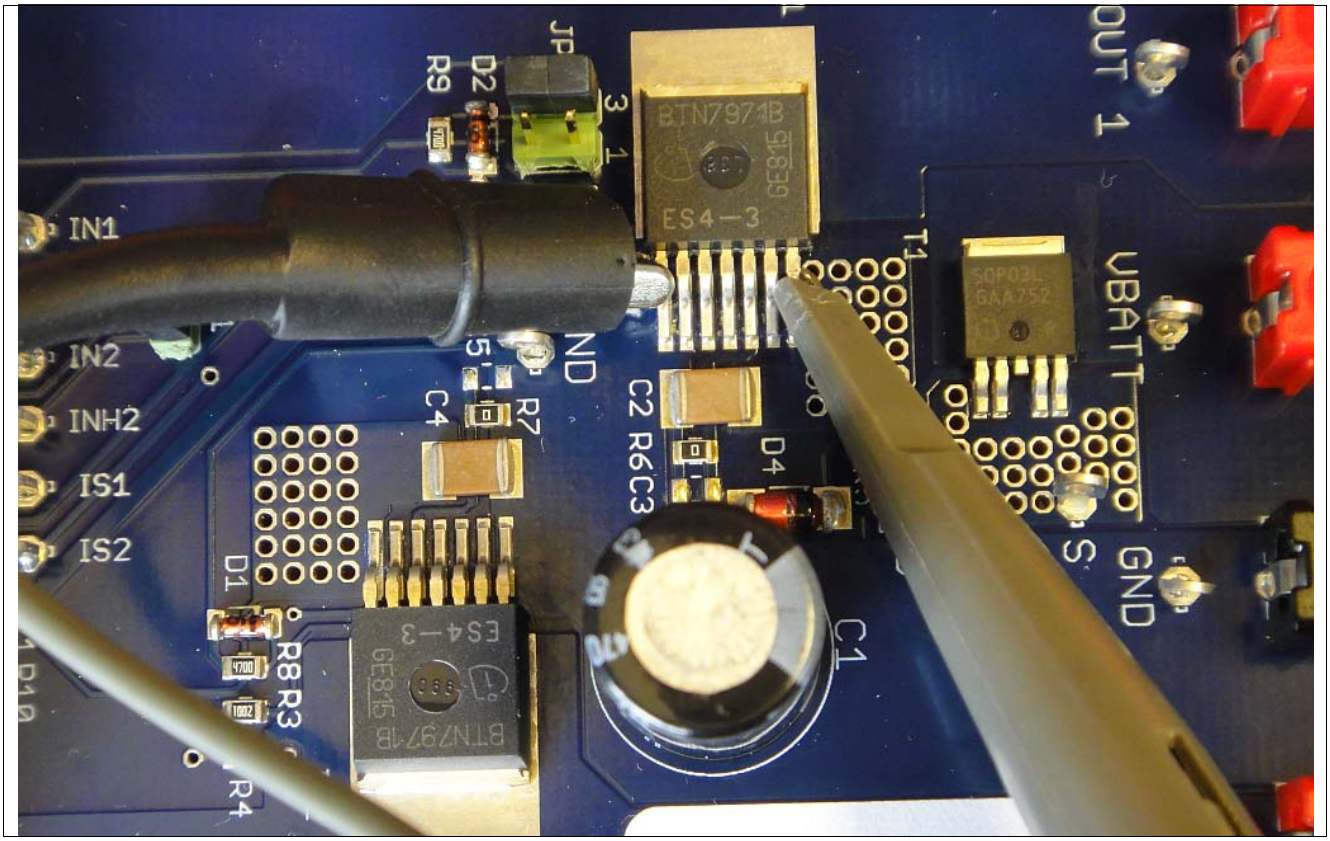

Figure 4 Measuring V_s with Probe and Reference Directly Connected to NovalithIC™

Doing so enables to monitoring of the NovalithIC™ supply voltage when high currents are switched. For example when a short-circuit current is switched, this is the only possibility for measurement if the DC-link capacitor is sufficient to keep the supply voltage above the undervoltage detection threshold (also see **Chapter 4.2**).

4 Design guideline

For a safe and sufficient motor control design, discrete components are needed. Some of them must be dedicated to the motor application and some to the NovalithIC™.

4.1 Schematic and layout design rules

Figure 5 and **Figure 6** show an example of a schematic plus a corresponding layout for a half-bridge motor control with NovalithIC™.

The best performance in terms of parasitic inductance and EMC can be reached with a GND plane, which we strongly recommend be used.

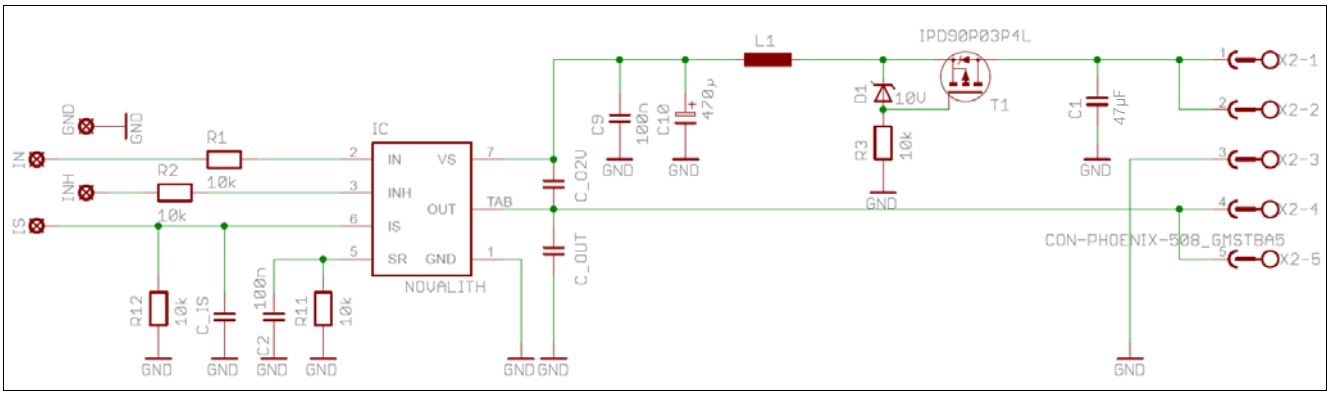

Figure 5 Example of a half-bridge schematic with NovalithIC™

Important design and layout rules:

The basis for the following items is the parasitic inductance of electrical wires, as described in **Chapter 3**.

- C10, so called DC-link capacitor: This electrolytic capacitor is required to keep the voltage ripple at the V_S-pin of the NovalithIC™ low during switching operation (the measurement procedure for the supply voltage is described in **Chapter 3.1**). It is strongly recommended that the voltage ripple at the NovalithIC™ V_s-pin to GND-pin be kept below 1 V peak to peak. The value of C10 must be aligned accordingly. See **Equation (4.9)**.
  Most electrolytic capacitors are less effective at cold temperatures. It must be assured that C10 is also effective under the worst case conditions of the application.
  The layout is very important. As shown in **Figure 6**, the capacitor C10 must be positioned with very short wiring at the NovalithIC™. This must be done to keep the parasitic inductors of the PCB-wires as small as possible.
- C9: This ceramic capacitor supports C10 to keep the supply voltage ripple low and covers the fast transients between the V_s-pin and the GND-pin. The value of this ceramic capacitor must be chosen so that fast V_s-ripple at the NovalithIC™ does not exceed 1 V peak to peak.
  The layout wiring for C9 must be shorter than for C10 to the NovalithIC™ to keep the parasitic PCB-wire inductance as small as possible. In addition the parasitic inductance could be kept low by placing at least two vias for the connection to the GND-layer.
- C_O2V: This ceramic capacitor is important for EMI in order to avoid entering electro magnetic disturbances into the NovalithIC™ as much as possible. Good results have been achieved with a value of 220 nF.
  In terms of layout, it is important to place this capacitor between “OUT” and “V_s” without significant additional wiring from C_O2V to the V_s- and OUT-line.

Design guideline

- C_OUT: This ceramic capacitor helps improve the EMI and the ESD performance of the application. Good results have been achieved with a value of 220 nF.
  To keep the RF and ESD out of the board, the capacitor is most effective when positioned directly on the board connector. In addition, the parasitic inductance could be kept low by placing at least two vias for the connection to the GND-layer.
- C1: This ceramic capacitor helps to improve the EMI and the ESD performance. In combination with L1 and C10 plus C9 a Pi-filter improves the electro magnetic emission on the V_S-line.
  Layout rules are the same as for C_OUT.

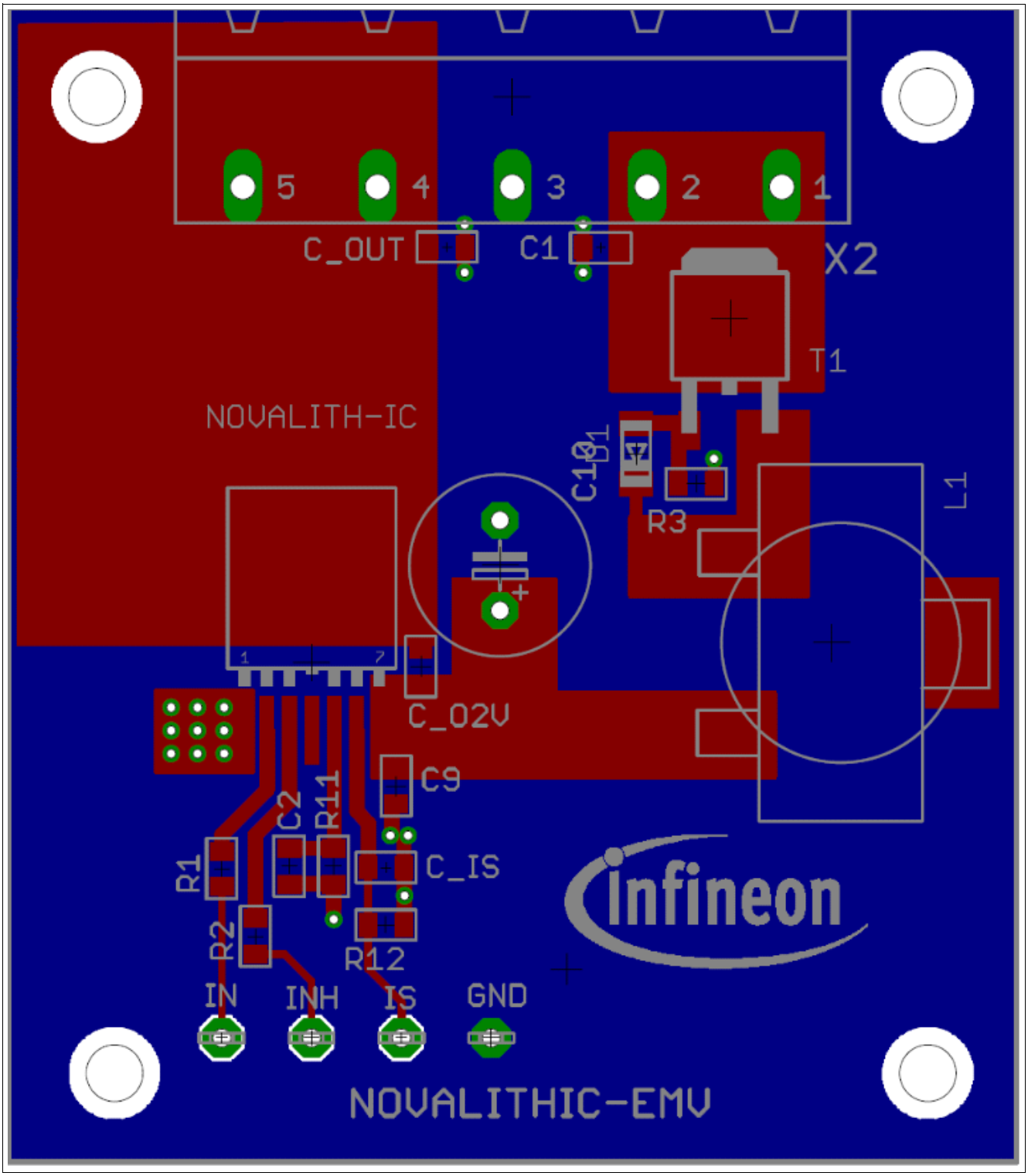

Figure 6 Example of an half-bridge layout with NovalithIC™ (not true to scale)

Other components:

- T1, D1 and R3: Reverse polarity protection. See **Chapter 4.4**.
- R11: Slew rate resistor according to data sheet.
- C2: Stabilization for slew rate resistor (R11).

- R12: Resistor to generate a current sensing voltage from the IS current.
- C_IS: Ceramic capacitor for EMI improvement. GND connection with at least two GND-vias. A good value is 1 nF.
  In case the current should be measured during the PWM-phase, this capacitor must be adapted to the ON-time inside the PWM-phase.
- R1 and R2: Device protection in case of µC pins shorted to V_s.

4.2 DC-link capacitor

For the stability of the DC-link voltage a sufficient capacitor is mandatory (in **Figure 2**, **Figure 3** and **Figure 5** it is C10). This is one of the most important component in a motor design with semiconductor switches.

The DC-link capacitor could be insufficient, because:

- The capacitor value is too small.
- The ESR of the capacitor is too high.
- When cold the capacitor value is too small.
- The distance between the DC-link capacitor and the NovalithIC™ is too large.
- The wiring between the DC-link capacitor and the NovalithIC™ is too long (see **Chapter 3**).

The value must be chosen carefully, taking the under-voltage toggling into account, which is described in **Chapter 4.2.2**.

4.2.1 Calculation of the DC-link capacitor and Pi-filter

As already mentioned in the design- and layout-rules of **Figure 5** the voltage ripple at the NovalithIC™ V_s-pin must not exceed 1 V peak to peak. The necessary DC-link capacitor can be estimated in the following way:

Motor control with PWM means for the DC-link voltage to provide energy pulses during the “ON-phase” of the PWM cycle. The DC-link pulses are shown in **Figure 7**.

This energy must be provided by the DC-link capacitor. This can generally be described with

(4.1)

$$E = \frac{1}{2} \cdot C \cdot V^2 = P \cdot T$$

(4.2)

$$C = C_{DC-link}$$

The voltage at the DC-link capacitor consists of the DC-part and the delta voltage from the supply ripple:

(4.3)

$$V = V_{S,DC} + \Delta V_S$$

The total power in this system consists of the DC-power plus the power of the energy pulse (E_{pulse}), which provides the energy to the motor during the ON-phase of the half bridge.

(4.4)

$$P = P_{DC} + \Delta P$$

The maximum pulse length is determined by the PWM frequency, theoretically at a duty cycle of 100%:

(4.5)

$$T = T_{pulse} = T_{PWM} = \frac{1}{f_{PWM}}$$

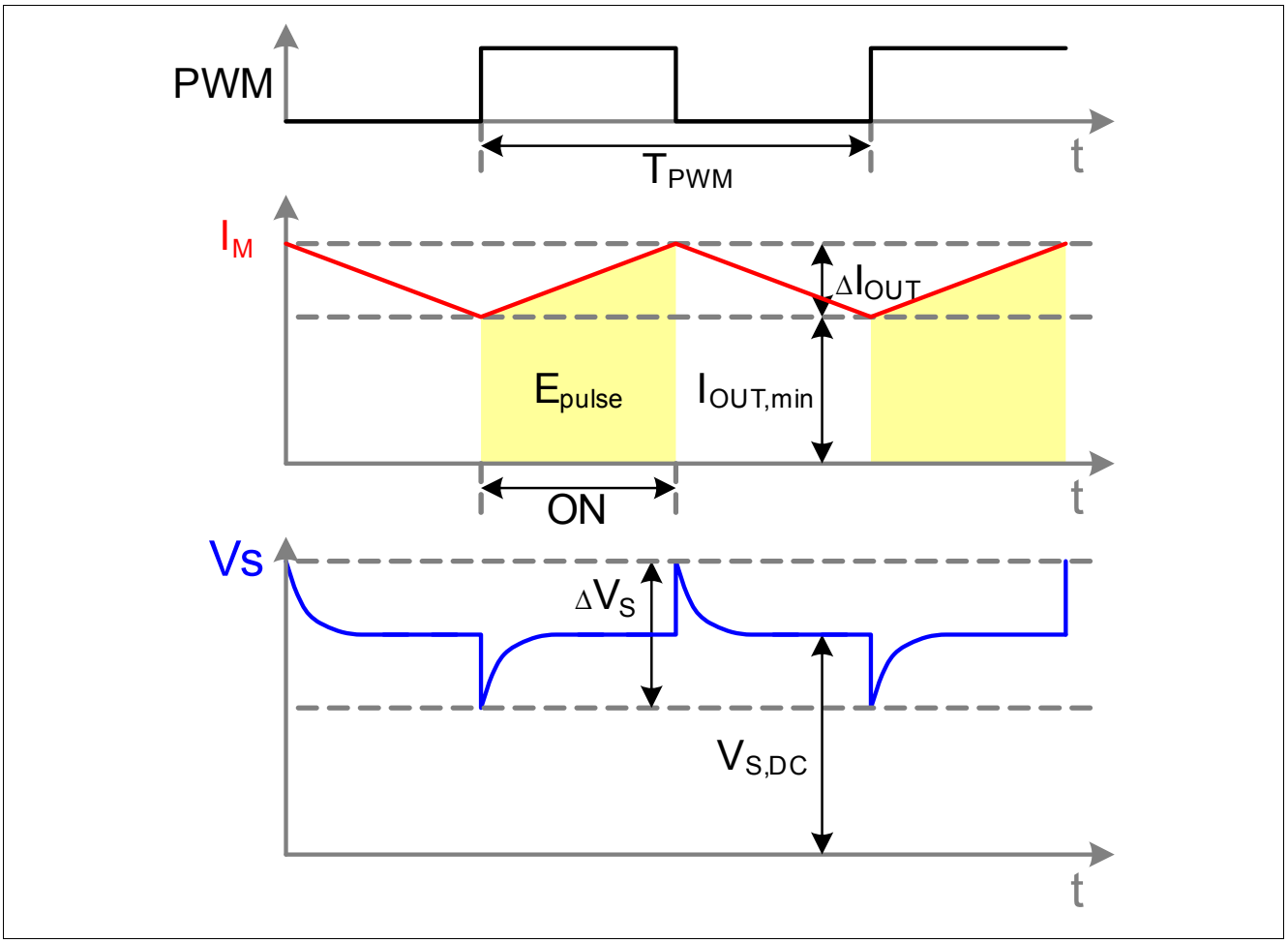

Figure 7 PWM control (PWM = IN-pin-signal, I_M = motor current and V_S = V_S-pin-voltage @ NovalithIC)

Insertion of **Equation (4.2)** to **Equation (4.5)** into **Equation (4.1)**

(4.6)

$$E = \frac{1}{2} \cdot C_{DC-link} \cdot (V_{S,DC} + \Delta V_S)^2 = (P_{DC} + \Delta P) \cdot T_{PWM}$$

(4.7)

$$\frac{1}{2} \cdot C_{DC-link} \cdot (V_{S,DC}^2 + 2 \cdot V_{S,DC} \cdot \Delta V_S + \Delta V_S^2) = P_{DC} \cdot T_{PWM} + \Delta P \cdot T_{PWM}$$

(4.8)

$$\cancel{\frac{1}{2} \cdot C_{DC-link} \cdot V_{S,DC}^2} + C_{DC-link} \cdot V_{S,DC} \cdot \Delta V_S + \underbrace{\frac{1}{2} \cdot C_{DC-link} \cdot \Delta V_S^2}_{negligible} = \cancel{P_{DC} \cdot T_{PWM}} + \Delta P \cdot T_{PWM}$$

Finally the equation to calculate the DC-link capacitor is:

(4.9)

$$\boldsymbol{C_{DC-link} \geq \frac{\Delta P \cdot T_{PWM}}{V_{S,DC} \cdot \Delta V_S}}$$

Based on **Equation (4.1)** and refering to the energy of on single pulse, as marked with E_{pulse} (≈ ΔP • T_{PWM}) in **Figure 7**:

(4.10)

$$\Delta P = V_S \cdot I_{nom} \approx V_S \cdot (I_{OUT,\min} + \frac{1}{2} \Delta I_{OUT})$$

The DC-link capacitor is primarily the energy buffer for the switching process of the PWM motor control. Secondly it is part of the Pi-filter. This means first the DC-link capacitor must be calculated according to **Equation (4.9)**. Based on this, it is recommended that the second capacitor of the Pi-filter C1 be estimated with:

(4.11)

$$\boldsymbol{C_1 = \frac{1}{10} \cdot C_{DC-link} = \frac{1}{10} \cdot C_{10}}$$

Generally the border frequency of the L_1-C_1-filter is determined with

(4.12)

$$f_g = \frac{1}{2 \cdot \Pi \cdot \sqrt{L_1 \cdot C_1}}$$

We recommend setting the border frequency f_g to half the value of the PWM -frequency f_{PWM}.

(4.13)

$$f_g = \frac{1}{2} \cdot f_{PWM} = \frac{1}{2 \cdot \Pi \cdot \sqrt{L_1 \cdot C_1}}$$

(4.14)

$$L_1 = \frac{1}{\Pi^2 \cdot f_{PWM}^2 \cdot C_1}$$

Summary:

First calculate the DC-link capacitor with **Equation (4.9)**.

Second calculate the other capacitor of the Pi-filter with **Equation (4.11)**.

Then calculate the inductor of the Pi-filter with **Equation (4.14)**.

And last but not least, do not forget the important layout rules and how to measure the supply voltage correctly.

4.2.2 Under-voltage toggling

The power supply cable of most modules in a car are several meters long. The longer the supply cable is, the higher its parasitic inductance. In addition, most modules have a Pi-filter at the supply line with a inductor for EMC reasons. The sum of the supply line inductances have a significant influence on the V_s-voltage. When switching the motor ON during a normal motor start or PWM control, with a insufficient DC-link capacitor the supply voltage drops below the under-voltage threshold and the NovalithIC™ is switched to tristate. The supply voltage recovers above the under-voltage threshold and the NovalithIC™ switches on again, again dropping below the under-voltage threshold ...

This effect can result in frequencies higher than 100 kHz, as is shown in **Figure 8**. The device will be damaged by the power dissipation of the switching losses, which is faster than the reaction time of the over temperature shut down, because of the high switching frequency.

The under-voltage toggling will be worse if the OUT is shorted to GND.

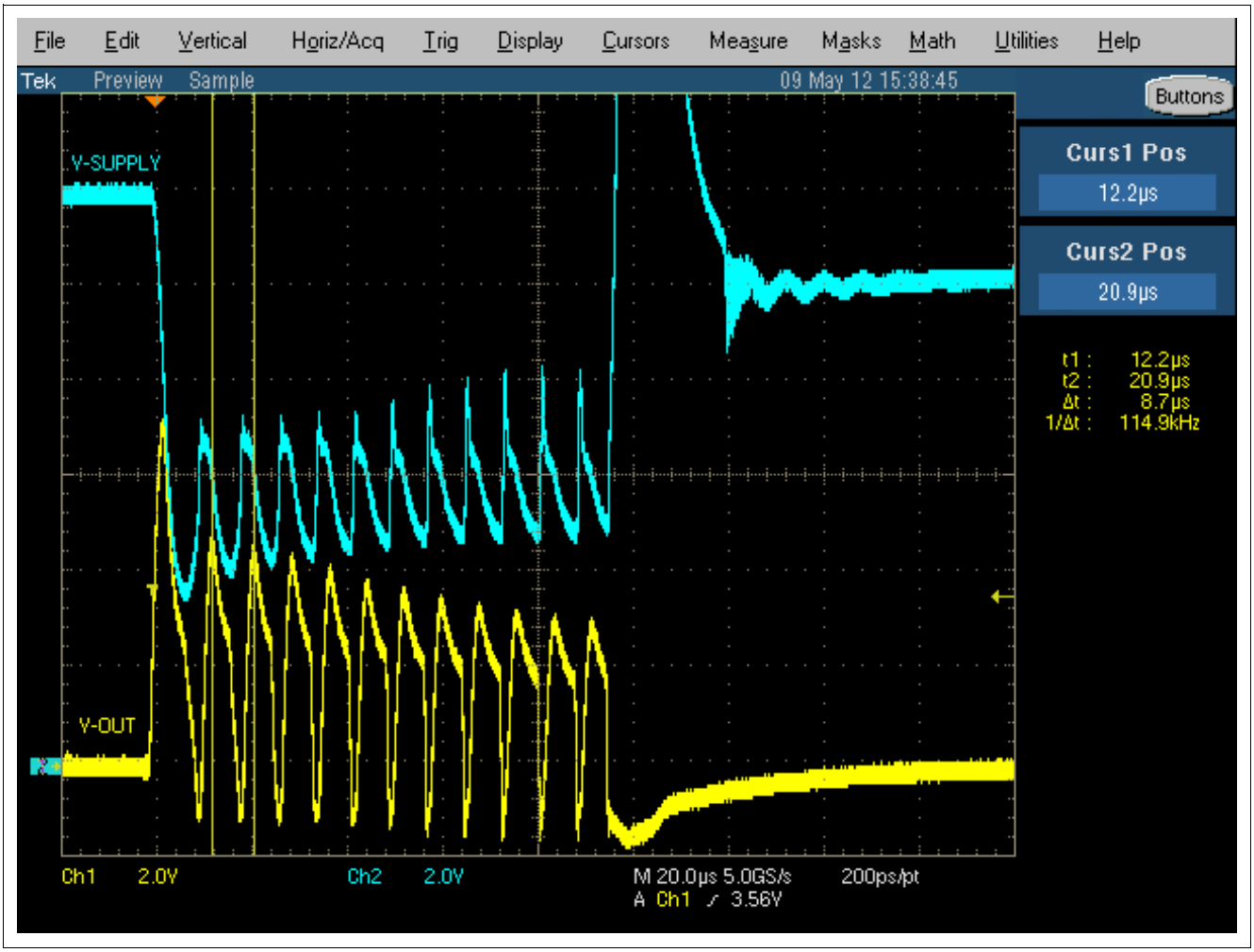

Figure 8 Under-voltage toggling started by short to GND and enabled by an insufficient DC-link capacitor

With a sufficient DC-link capacitor the supply voltage drop is limited so as not to reach the under-voltage threshold, as is shown in **Figure 9**.

Both measurements in **Figure 8** and **Figure 9** are conducted with the Infineon “NovalithIC Demo Board V2.1” with BTN7933. The “ON-time” is limed to 100 µs by the IN-signal, as shown in **Figure 9**. Only the DC-link capacitor is switched between the two measurements.

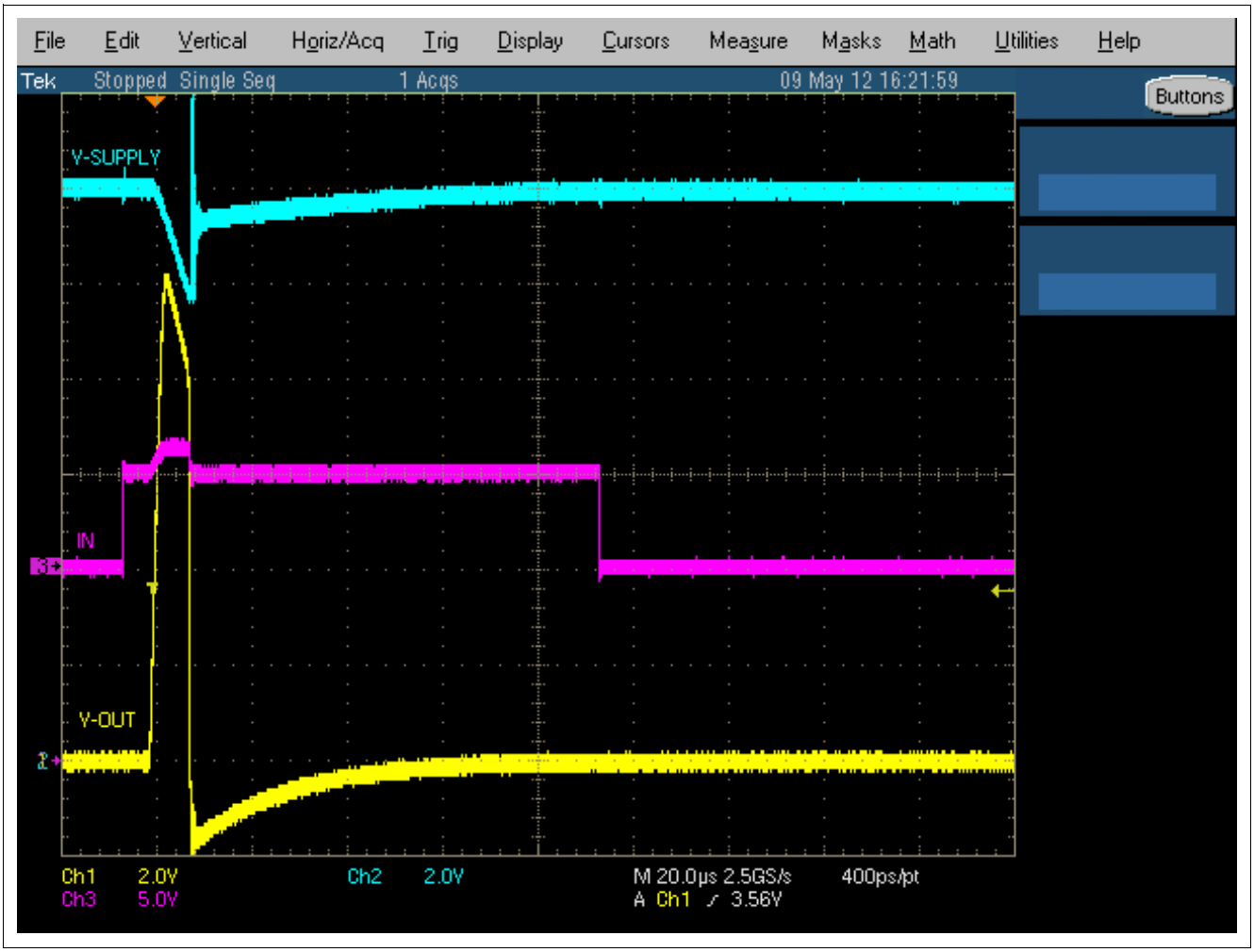

Figure 9 The sufficient DC-link capacitor avoided under-voltage -toggling in case of a short to GND

4.3 Driving inductive loads over long wires

Inductive loads have a lowpass filter characteristic, like a motor. Because of this, the wire from the NovalithIC™ OUT to the motor injects electro magnetic disturbances into the OUT-pin. This antenna effect increases as the length of the motor wire increases.

The definition of a long motor wire strongly depends on the application and the environment. To provide a general idea, wire lengths of approximately 20 cm and more are considered as "long wire". The motor wire should therefore be as short as possible.

4.3.1 PWM operation

In case of a long motor wire and PWM operation the electro magnetic emission (EME) increases with the wire length and with the switching speed (inversion of $t_{r(HS)}$, $t_{r(LS)}$, $t_{f(HS)}$ and $t_{f(LS)}$). In this case it is advantageous to reduce the switching speed with the slew rate resistor at the SR-pin (see **Figure 5**, R_{11}). Reducing the switching speed has probably a impact on the PWM-frequency, which may needs to be adapted. In any case the power dissipation and the cooling concept needs to be reviewed. The slew rate resistor at the SR-pin should not exceed the max. slew rate resistor value of the data sheet $R_{SR} \leq 51$ kΩ.

4.3.2 Current sense

A long motor wire can pick up electro magnetic disturbances which could influence the current sense signal at the IS-pin. If a high accuracy of the current measurement is needed, it is recommended to use the IS-pin as status flag diagnosis and perform the current measurement with an external shunt plus current sense amplifier. An schematic example is shown in **Figure 10**.

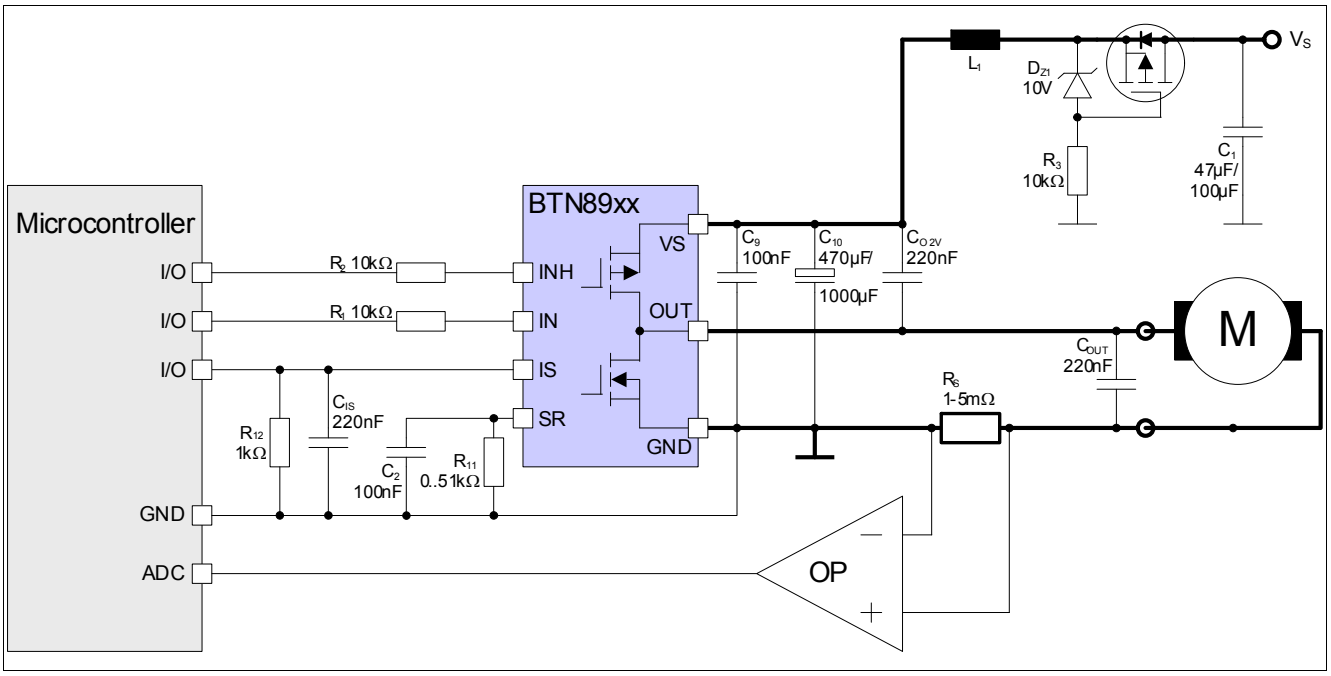

Figure 10 BTN89xx with external current measurement

4.4 Reverse polarity protection

The semiconductor technology of NovalithIC™ used has a parasitic PN -diode from “GND” to the supply voltage pin “V_s”. If the supply voltage is inverted, a huge current will flow through this parasitic PN -diode and will damage the device. With reverse polarity protection, the reverse current is not possible and the semiconductor components of the design are protected.

In the schematic in **Figure 5**, reverse polarity protection is provided with a P-channel MOSFET (IPD90P03P4L-04), a zener-diode (D_1) and a resistor (R_3).

Normal operation V_s > GND:

- P-MOSFET OFF: The application is supplied by the body-diode of the reverse polarity protection transistor (IPD90P03P4L-04), e.g. in case of a power-up. The status “P-MOSFET ON” will quickly be reached.
- P-MOSFET ON: After the power-up in which the body diode was used as a supply path, the zener diode plus the resistor will generate a gate-source voltage in the range of 10 V and the P-MOSFET is in ON-state. Only the $R_{DS,on}$ is in the power supply path.

Reverse polarity condition V_s < GND:

- The gate source voltage of the reverse polarity protection transistor is continuously “LOW” and the transistor is switched OFF. No current can flow in this state. The application will not be damaged.

4.5 Cooling

The NovalithIC™ half-bridge, driving high current generates power dissipation. These are R_{ON} losses and switching losses in case of PWM control, which heat up the device. For details, please see **Chapter 7**. The package PG-TO263-7-1 provides a low thermal resistance which can be combined with a heat sink on the PCB to avoid exceeding the absolute maximum temperature values of the data sheet.

In **Figure 6** a cooling area (brown top layer, where the NovalithIC™-OUT is connected) has already been drawn. Depending on the power dissipation, other thermal sources on the PCB and the ambient temperature, the cooling needs to be carefully adapted to each application.

In addition the reverse polarity protection transistor T1 (**Figure 5** and **Figure 6**) generates $R_{DS,on}$ power losses and the cooling concept for this transistor must ensure that the device does not exceed the absolute maximum junction temperature.

5 Current Sense Improvement

The NovalithIC™ half-bridge-family has a current sense function with an IS-pin which provides the output current divided by a factor, so called dk_{ILIS}. The precision of the current measurement could be significantly improved by eliminating the IS-offset, dk_{ILIS}-production spread and respecting the temperature dependency of the dk_{ILIS}.

The table below provides an overview of possible combinations of procedures to reduce current measurement errors.

Table 1 Current sense procedure and benefits

Procedures			Load current tolerance
Offset compensation			±28%
Offset compensation	Device dkILIS measurement		±10%
Offset compensation	Device dkILIS measurement	Temperature estimation	±6%
Offset compensation	Device dkILIS measurement	Temperature compensation	±3%

5.1 Characteristic of the dk_{ILIS}

The dk_{ILIS} has characteristic dependencies. The most important ones with respect to the supply voltage V_s and with respect to the temperature, are described in this chapter.

5.1.1 Supply voltage dependency of dk_{ILIS}

The dependency of the dk_{ILIS} of the supply voltage V_s is negligible, as **Figure 11** shows. This means the supply voltage can be ignored when calculating the load current.

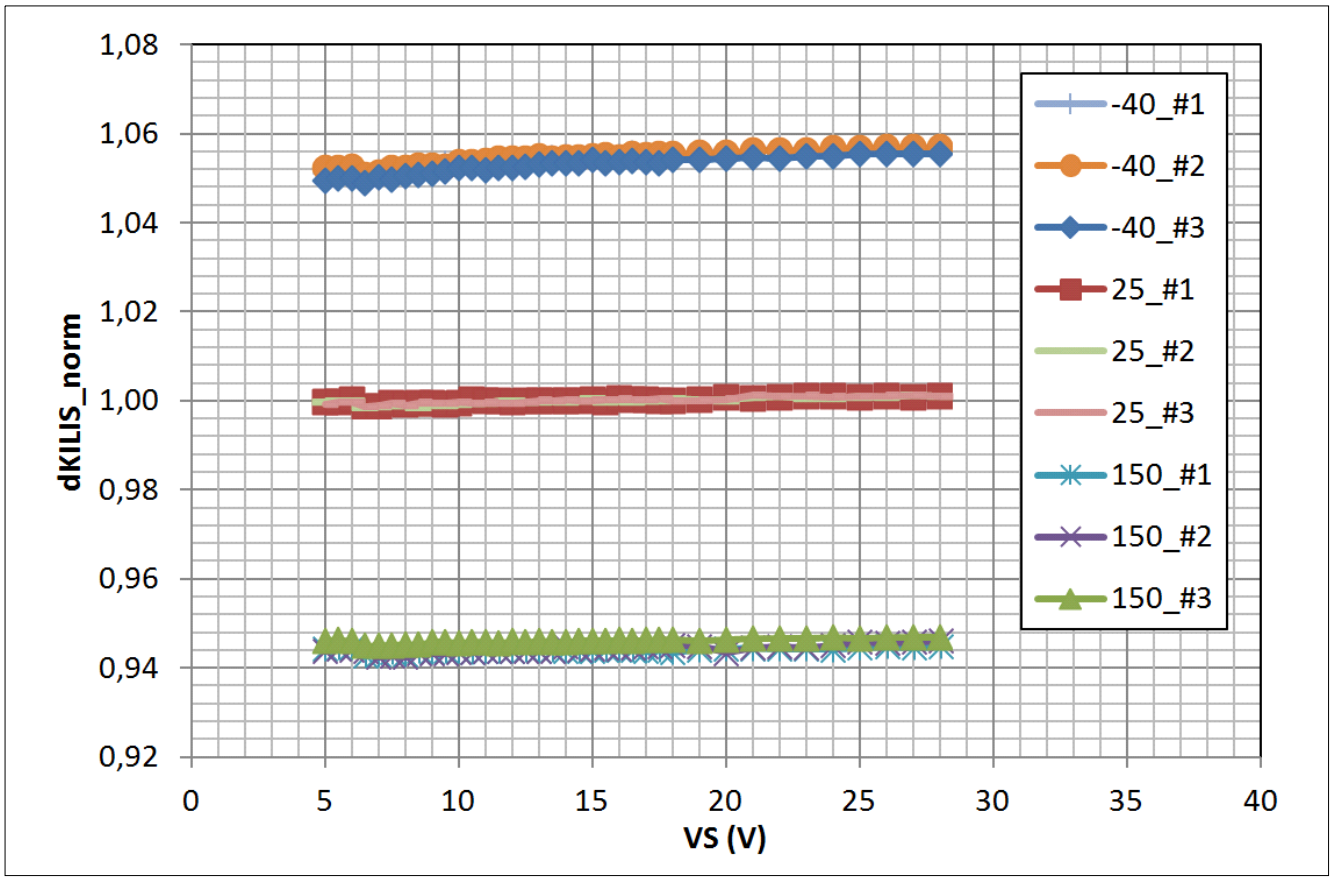

Figure 11 dk_{ILIS} vs. the supply voltage V_s

5.1.2 TC 1000 life time tests

Life time tests of 1000 hours with a dedicated device stress set up and with many devices from different production lots showed the dk_{ILIS} is decreasing over life time up to -3%.

5.1.3 Temperature drift of the dk_{ILIS}

Figure 12 and **Figure 13** show the characteristics of the dk_{ILIS} vs. temperature and production spread with a scaling at 25°C, including a series of lab measurement points for one device.

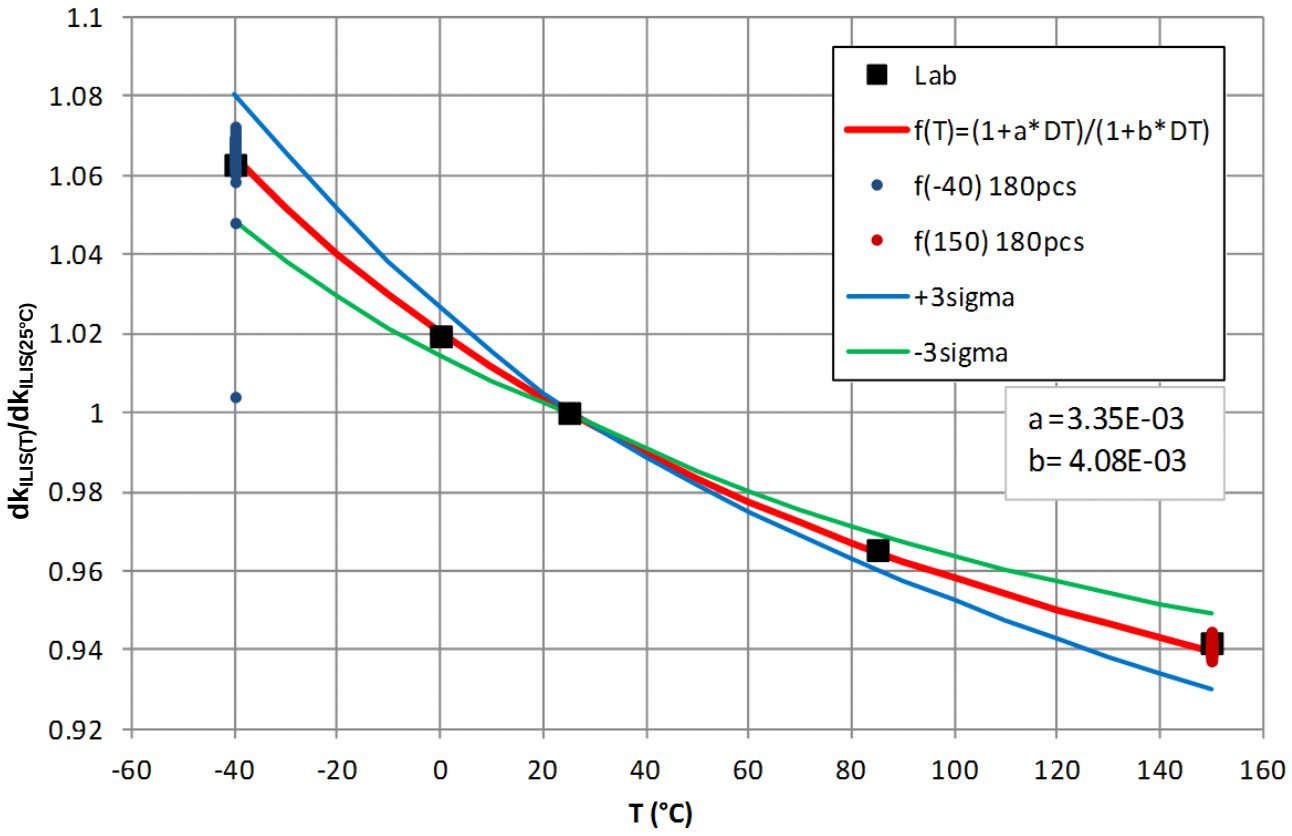

Figure 12 BTN8960 /62 dk_{ILIS} vs. temperature

The function f(T) is dependent on the temperature coefficient of the shunt resistance in the control chip (a), the temperature coefficient of the shunt (b) and DT = T - 25 °C.

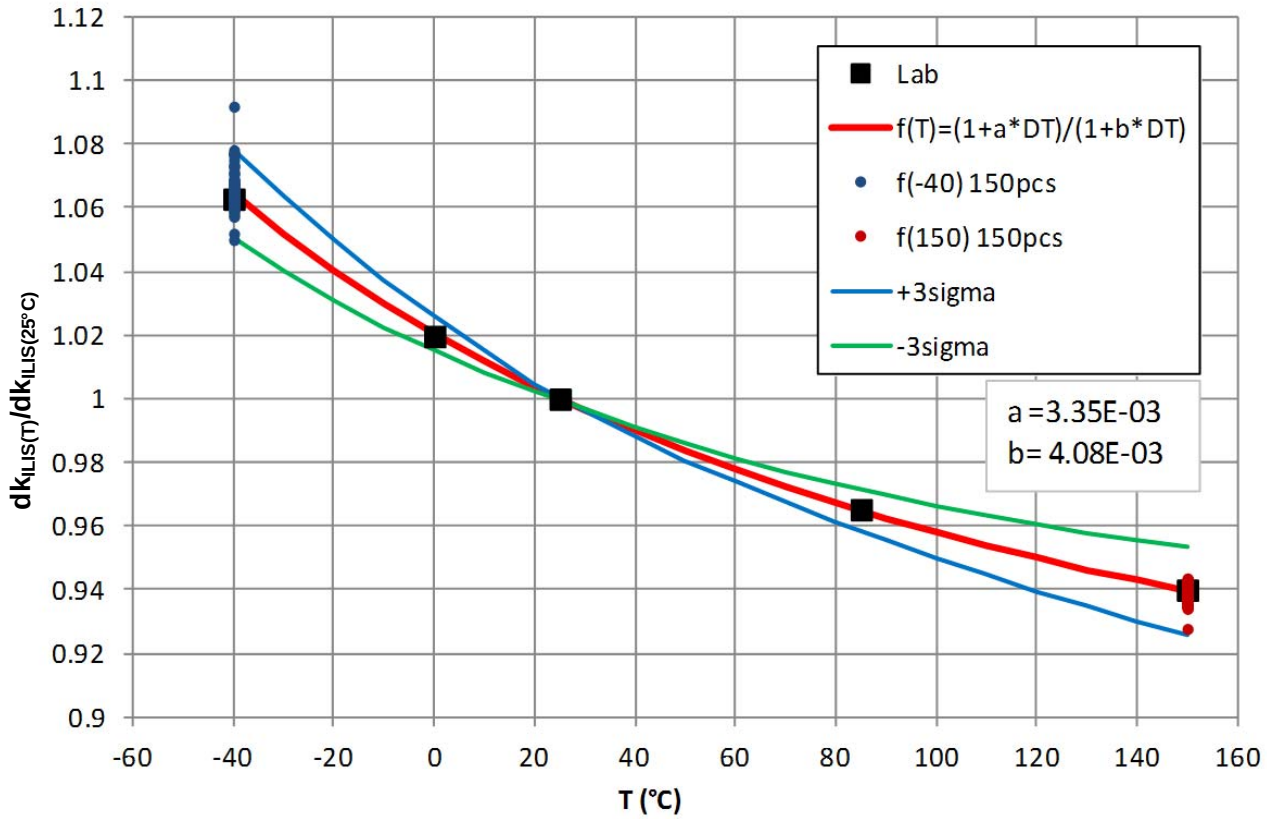

Figure 13 BTN8980 /82 dk_{ILIS} vs. temperature

The function f(T) is dependent on the temperature coefficient of the shunt resistance in the control chip (a), the temperature coefficient of the shunt (b) and DT = T - 25 °C.

5.2 Offset compensation

The BTN89xy series is featured with an artificial offset current at the IS-pin. This is shown in **Figure 14**.

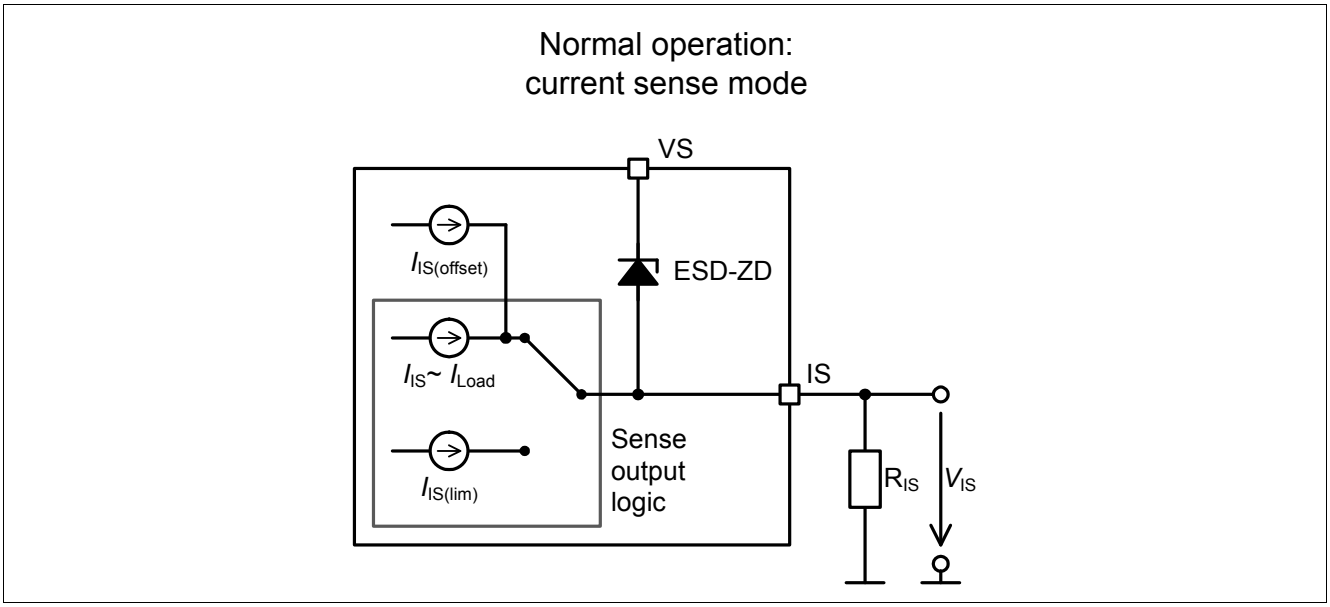

Figure 14 IS-Pin Internal Structure

With this structure, it is possible to always have a measurable offset at IS without a load current. This makes it easy to measure the offset with the microcontroller, store the offset value and process this in the current measurement procedure.

The offset must be compensated to allow a precise current measurement with the IS-pin.

The offset should be compensated before activating the load. When an application such as a fuel pump runs constantly with PWM, you can perform the offset compensation when INH=high and IN=low. In the PWM-phase, the best measurement results are achieved just before the rising edge of the IN-signal.

With this procedure, the specified dk_{ILIS} of ±28% could be reached, even for small load currents. This includes production spread, temperature dependency and aging. Most errors are caused by production spread, which could be compensated by measuring of the dk_{ILIS} of each device (device-specific dk_{ILIS}). Details of this approach are described in the relevant chapter.

5.3 Device specific dk_{ILIS}

With a measurement of the offset current and one IS-value at a certain load current at 25 °C (e.g. 20 A), it is possible to determine the individual $dk_{ILIS\text{-}device}$ and store it permanently to the microcontroller of the application. With this value, the graphs in **Figure 12** and in **Figure 13** are valid. The extreme values are indicated by the blue line (+3sigma):

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS\text{-}min\text{-}H}$ = 0.93 (blue @ 150 °C)

Taking into account the aging of the device (see **Chapter 5.1.2**) the minimum value of **Figure 12** and **Figure 13** (blue line) must be reduced by 3% (multiplying 0.97). This means the extreme values are as follows:

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS\text{-}min\text{-}H\text{-}old} = dk_{ILIS\text{-}min\text{-}H} * 0.97 = 0.9$

This could be assumed as an error of ±10% including temperature drift and aging.

In this case, the typical value should be assumed as follows:

- $dk_{ILIS\text{-}typ}$ = 0.99

The device calibration could be implemented in the module test sequence.

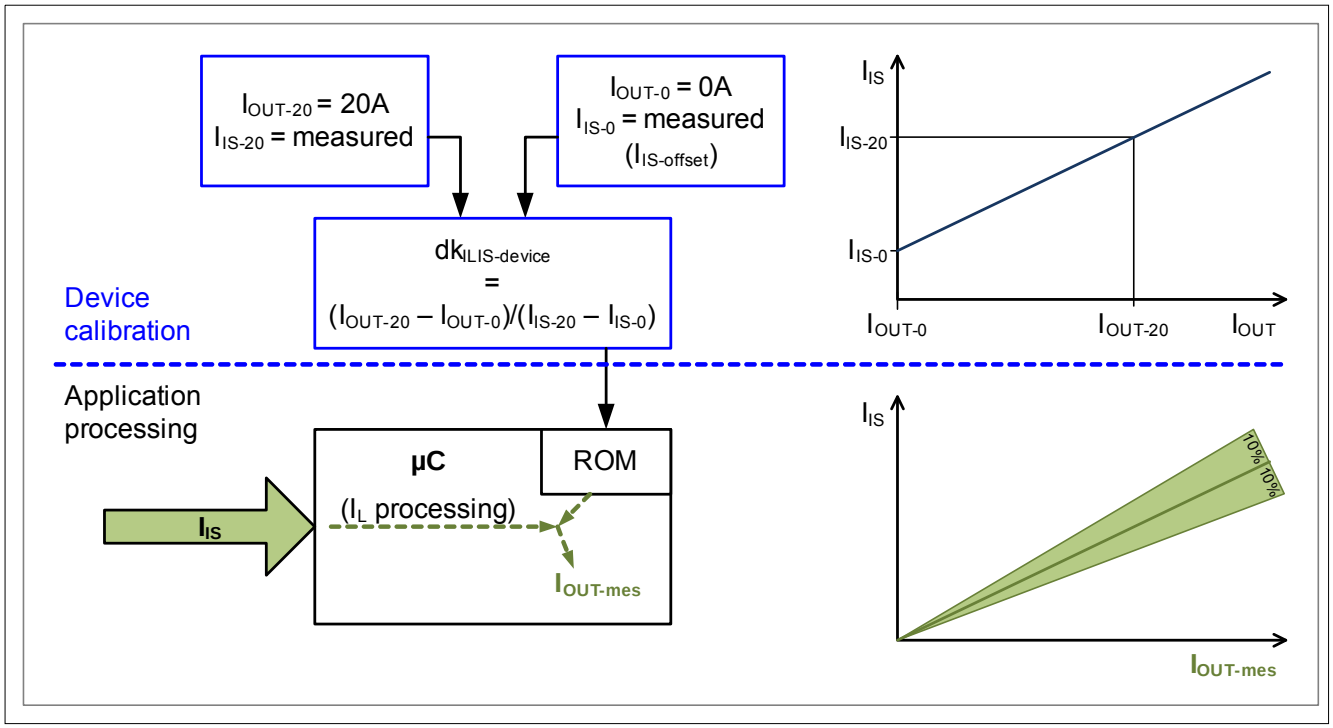

Figure 15 Generating the device fine $dk_{ILIS-device}$

5.4 Device fine dk_{ILIS} and temperature compensation

On the other hand, the dk_{ILIS} is dependent on the temperature, which is shown in **Figure 12** and **Figure 13**. These figures show a characteristic temperature drift with a low content of production spread. This makes it possible to measure the temperature on the PCB and reduce the temperature dependency by means of a calculation in the microcontroller. This procedure is illustrated in **Figure 16**.

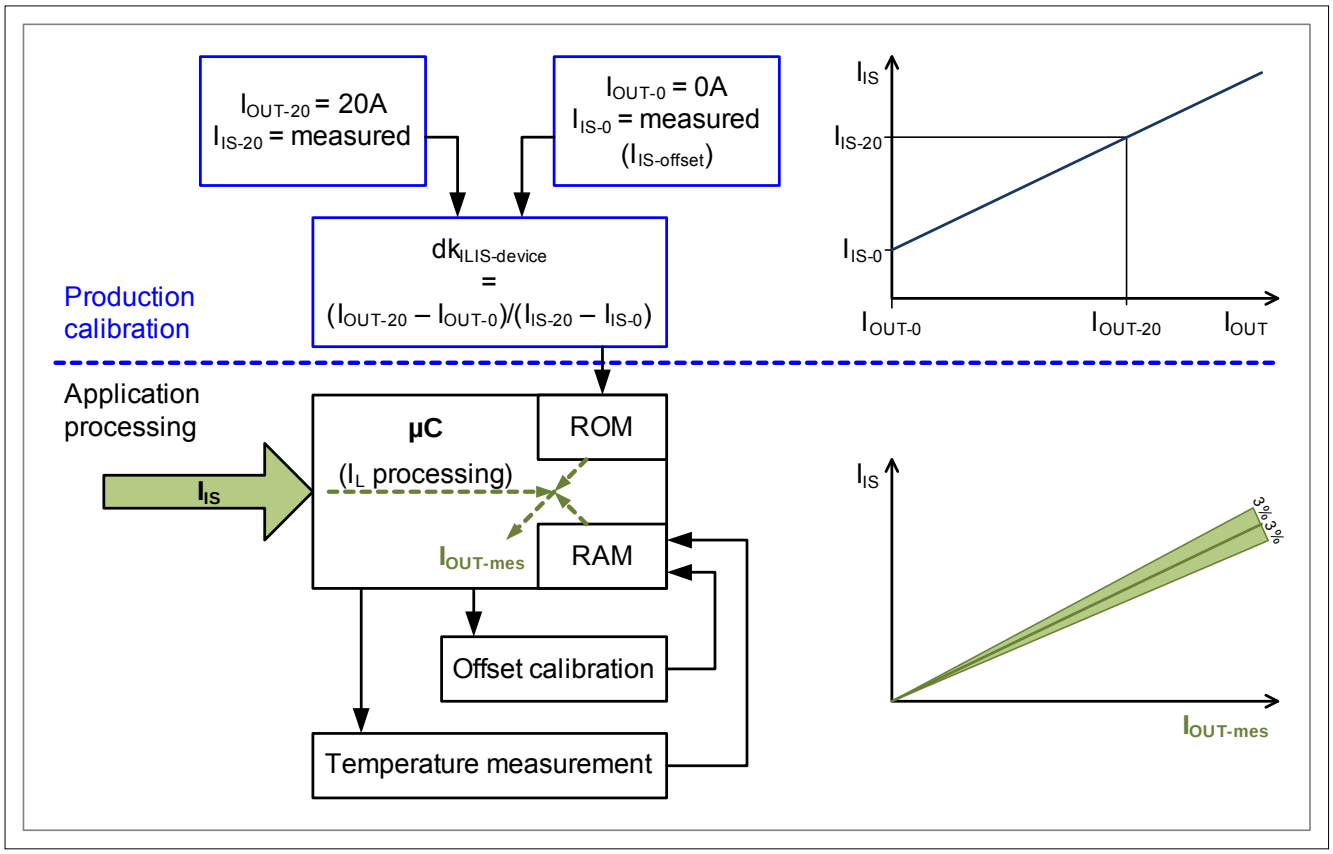

Figure 16 Load current "I_{OUT}" calculation with temperature compensation

Taking the extreme values from **Figure 13**:

- $dk_{ILIS-max-C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS-min-C}$ = 1.05 (green @ -40 °C)
- $dk_{ILIS-max-H}$ = 0.955 (green @ 150 °C)
- $dk_{ILIS-min-H}$ = 0.925 (blue @ 150 °C)

Multiplying the min. values with a factor of 0.97 (-3% aging) produces the following values:

- $dk_{ILIS-max-C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS-min-C-old}$ = 1.0185 (green @ -40 °C)
- $dk_{ILIS-max-H}$ = 0.955 (green @ 150 °C)
- $dk_{ILIS-min-H-old}$ = 0.9 (blue @ 150 °C)

Calculating the typical value for:

- $dk_{ILIS-typ-C}$ = 1.05
- $dk_{ILIS-typ-H}$ = 0.928

These values could be compensated with a temperature measurement and the characteristic from **Figure 12** and **Figure 13** to provide the value of $dk_{ILIS-typ}$ = 1.

With this compensation, the new min. and max. values are:

- $dk_{ILIS-max-C-T}$ = 1.03 (blue @ -40 °C)
- $dk_{ILIS-min-C-old-T}$ = 0.9685 (green @ -40 °C)

- $dk_{ILIS\text{-}max\text{-}H\text{-}T}$ = 1.027 (green @ 150 °C)
- $dk_{ILIS\text{-}min\text{-}H\text{-}old\text{-}T}$ = 0.972 (blue @ 150 °C)

After temperature compensation, the min. and max. values are $dk_{ILIS\text{-}min\text{-}H\text{-}old\text{-}T}$ and $dk_{ILIS\text{-}max\text{-}C\text{-}T}$.

Ultimately, a current measurement with a precision of ±3% could be achieved!

If higher tolerances are acceptable, the temperature measurement can be less precise.

5.4.1 An example of the I_{IS} failure with a rough temperature estimation

Assuming the dk_{ILIS} was calibrated during production at 25 °C, the I_{IS} measurement failure could be reduced to ±6%, only by estimating if the temperature is above or below 25 °C. This estimation could be done e.g. by using the temperature characteristic of the $I_{IS\text{-}offset}$, which is included in the data sheet.

Temperature below 25° C:

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS\text{-}min\text{-}25°C}$ = 1

Reducing the min. values with the -3% aging (multiplying with 0.97) the following values will be calculated:

- $dk_{ILIS\text{-}max\text{-}C}$ = 1.08 (blue @ -40 °C)
- $dk_{ILIS\text{-}min\text{-}25°C\text{-}old}$ = 0.97

For temperatures above 25 °C the calculation method is essentially the same.

Ultimately, a current measurement with a precision of ±6% could be achieved without any external temperature measurement!

5.5 IS-pin current sensing and fault detection

The BTN8960 /62 /80 /82 provides several additional sense and diagnosis functionalities, which will be explained here.

5.5.1 Current sense behavior

In comparison to its predecessor BTN79xy, the BTN89xy family's current sense output functionality has an advanced feature. For illustration purposes, both the BTN7960 and the BTN8960 were deployed in the same high side switching scenario, where an inductive load to ground was toggled with a duty cycle of 50%. Both measurements were conducted with the Infineon “NovalithIC™ Demo Board V2.2”. The resulting measurements are shown in **Figure 19** for the BTN7960 and in **Figure 18** for the BTN8960. As described in **Figure 14**, both types have a similar behavior in the case of an error. Instead, their current sense functionality differs in normal operating mode. While the BTN79xy blanks the IS output to 0A when the high side MOSFET is switched off, the BTN89xy provides the offset current $I_{IS(offset)}$ instead.

For monitoring purposes, the behavior of both the BTN79xy and the BTN89xy can be used for continuous current monitoring, even in freewheeling mode: In bi-directional motor applications with two BTN98xy, the freewheeling current can be monitored at the high side MOSFET in forward direction. As shown in **Figure 17**, the freewheeling current $I_{FW,HS}$ can be observed with both high side MOSFETs being closed. In the scenario shown, the IS output of the left BTN89xy provides the current dependent signal, while the $I_{FW,HS}$ flows through the right BTN89xy in reverse direction.

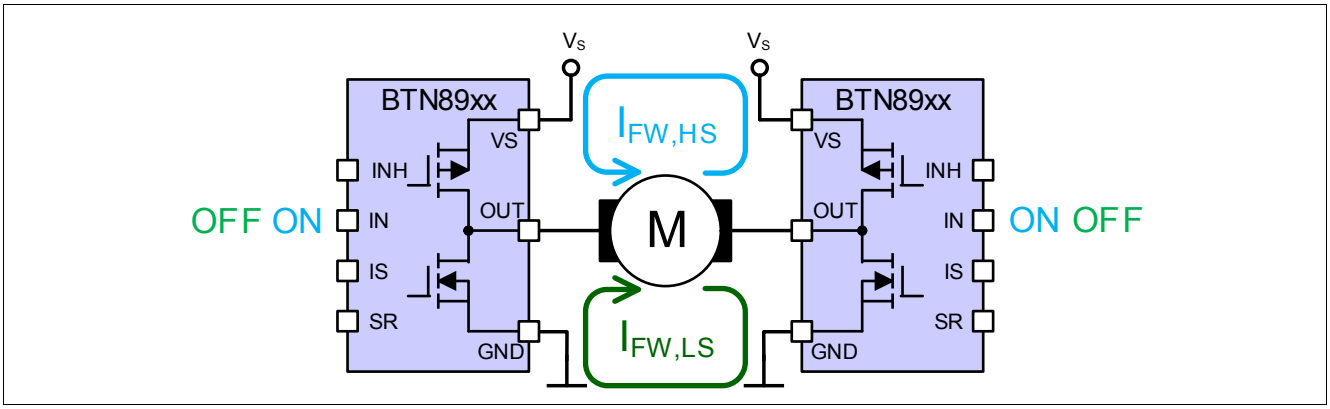

Figure 17 Two freewheeling path options for bi-directional motor applications, implemented with two BTN8960 /62 /80 /82.

5.5.1.1 BTN89yz - advanced current sense and fault diagnosis

In comparison to the BTN79xy, the BTN89xy does not mute the IS current sense output signal, which is always present. This results in the following behavior and additional diagnostic possibilities:

- Offset compensation of $I_{IS(offset)}$:
  If no current is flowing through the high side MOSFET, the current sense offset $I_{IS(offset)}$ can be monitored at the IS-pin. This can be ensured while the high side switch is being switched off via the IN-pin and the freewheeling path doesn't go through the high side MOSFET. If measured, this value can be used for an online offset calibration of $I_{IS(offset)}$, according to **Chapter 5.2**. In **Figure 18** this scenario is marked with (2). In the case of a fault condition, the IS-pin will provide a constant current of $I_{IS(lim)}$, which can be clearly distinguished from the lower offset current $I_{IS(offset)}$.
- Online calibration of $I_{IS(offset)}$ and continuous current monitoring:
  If two BTN89xy devices are deployed in H-bridge configuration, the user can choose between either monitoring the freewheeling current or the online calibration of $I_{IS(offset)}$ by adapting the freewheeling path accordingly. An offset calibration of $I_{IS(offset)}$ for both the left and right BTN89xy can be carried out by choosing a freewheeling path through both low side MOSFETs, with the freewheeling current $I_{FW,LS}$ displayed in **Figure 17**. As previously described, the current can be monitored continuously with a freewheeling current $I_{FW,HS}$ flowing through the two high side MOSFETs.

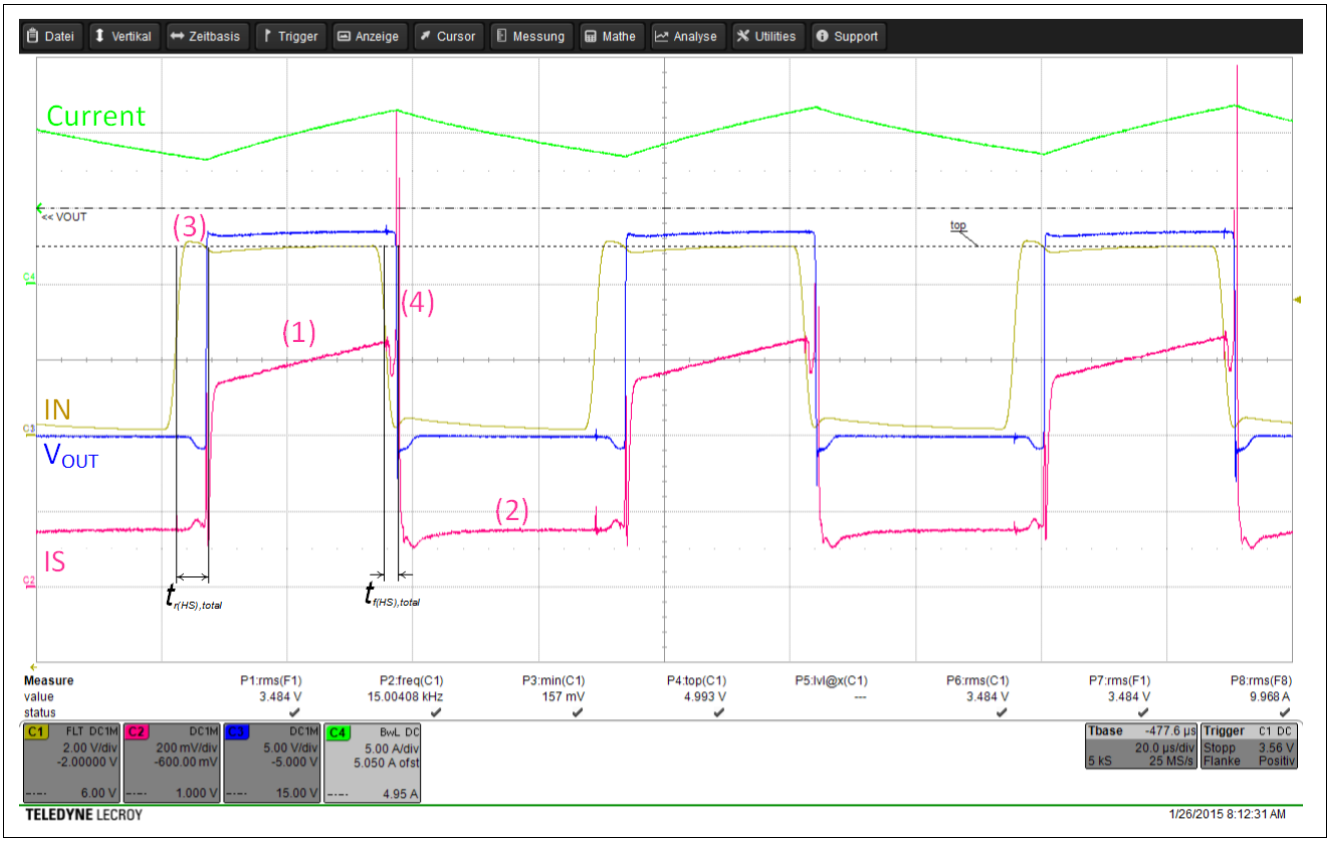

Figure 18 Measurement of a BTN8960, switching an inductive load to GND. (1): current sense signal, (2): current sense offset current $I_{IS(offset)}$

5.5.1.2 BTN79xy current sense limitations

The current is sensed to the IS output pin, if the high side (HS) MOSFET is activated and the INH and IN-pins are high (marked with (1) in **Figure 19**). This results in a current dependent IS output signal. For all other cases, the switching on (3) / off (4) phases of the high side MOSFET and for low IN inputs (2), the IS output signal is 0 A, as shown in **Figure 19**. In the case of a fault condition, the IS-pin will provide a constant current of $I_{IS(lim)}$ that can be uniquely identified for a low IN-pin.

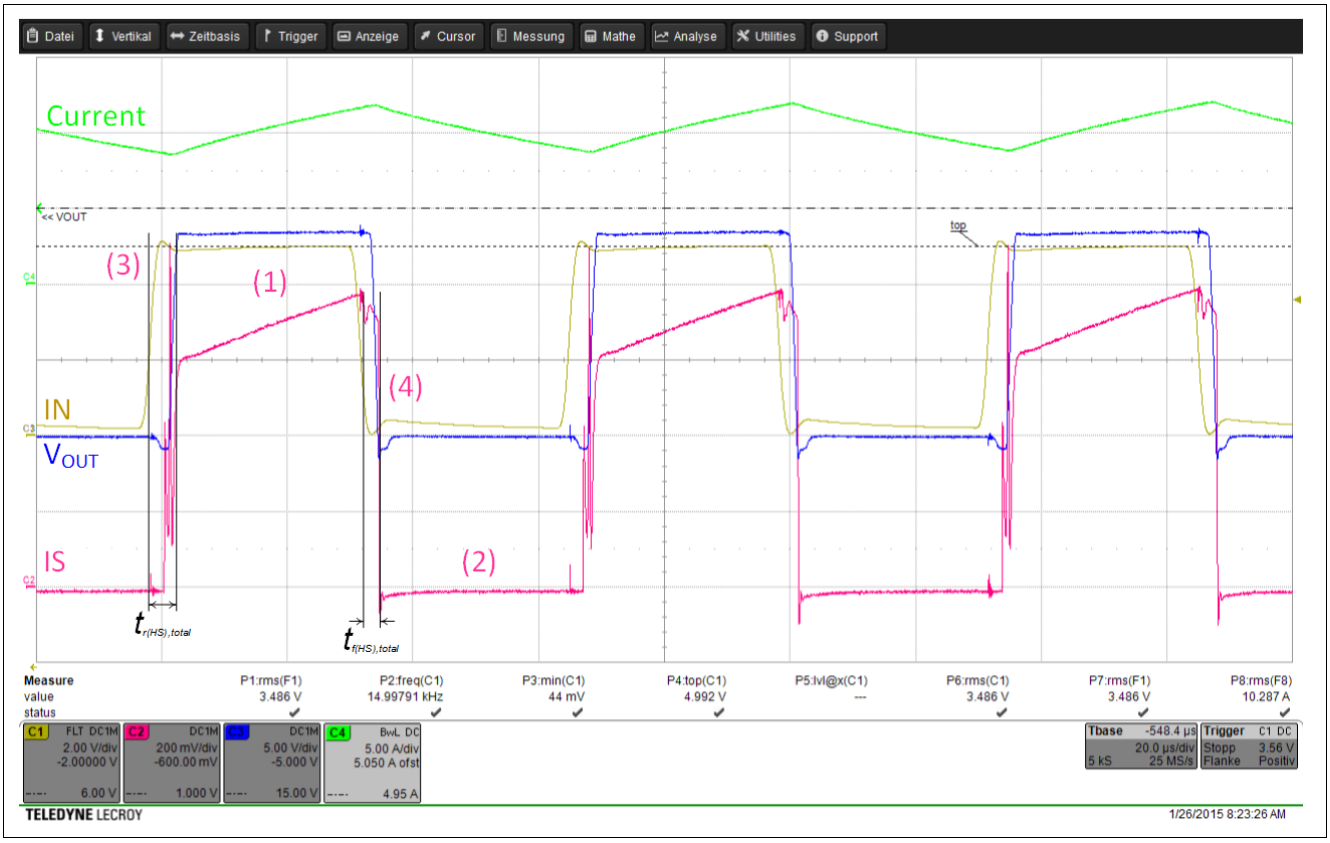

Figure 19 Measurement of a BTN7960, switching an inductive load to GND. (1): current sense signal, (2): current sense functionality switched off

5.5.2 Fault detection

The current sense accuracy depends on the spread of the two parameters dk_{ILIS} and $I_{IS(offset)}$. The resulting maximal, typical and minimal behavior is displayed in **Figure 20** for the BTN8960/62 and in **Figure 21** for the BTN8980/82. Here, the limits for the sense current in fault condition $I_{IS(lim)}$ are also shown.

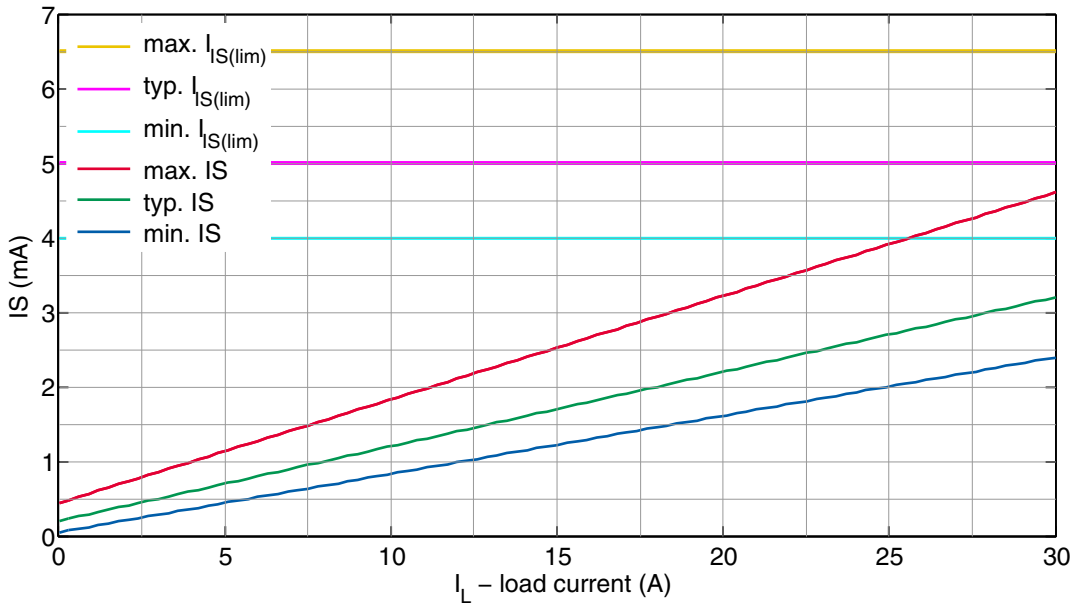

Figure 20 Behavior of the BTN8960/62's IS output pin for current sense and fault condition according to parameter tolerances

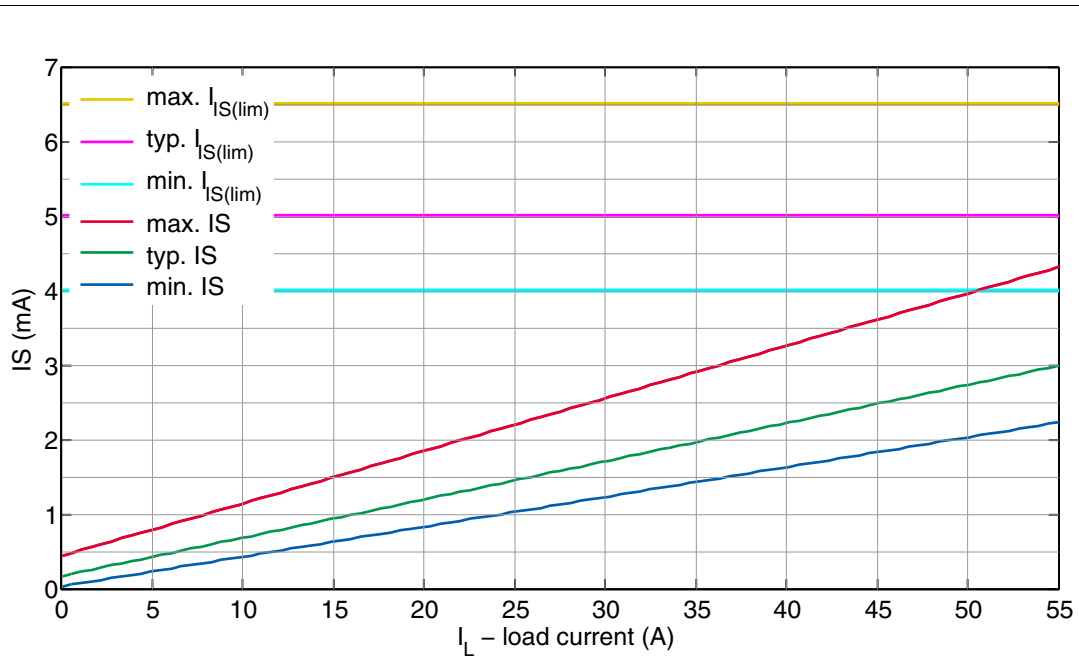

Figure 21 Behavior of the BTN8980/82's IS output pin for current sense and fault condition according to parameter tolerances

The possibility to distinguish whether a current sense signal or the constant sense current $I_{IS(lim)}$, indicating a fault condition, can be measured at the IS-pin is also an important issue. Therefore the fault distance between the two states is further considered. The combined (possible) output options for both states can be seen in **Figure 20** for the BTN8960/62 and in **Figure 21** for the BTN8980/82. For a worst case combination of the three

parameters $I_{IS(lim)}$, dk_{ILIS} and $I_{IS(offset)}$, provided in the data sheet for the given tolerances, there is a current range, where it is not possible to distinguish the right operation mode, whether there is a fault or not.

The corresponding break-even point for the BTN8960/62 can be calculated for the load current I_L accordingly:

(5.1)

$$I_L = dk_{ILIS} \cdot (I_{IS} - I_{IS(offset)}) = dk_{ILIS} \cdot (I_{IS(lim)} - I_{IS(offset)})$$

(5.2)

$$I_L = 7,2 \cdot 10^3 \cdot (4\text{mA} - 440\mu\text{A}) \approx 25,6\text{A}$$

For such a system, it wouldn't be possible to distinguish easily between the fault condition current $I_{IS(lim)}$ and a current sense signal, for I_L > 25 A if the BTN8960/62 is used, and I_L > 50 A for the BTN8980/82. For a more precise consideration, also the temperature dependency of $I_{IS(lim)}$, dk_{ILIS} and $I_{IS(offset)}$ has to be considered. For the given critical area for load currents I_L > 25 A, especially the parameters dk_{ILIS} and $I_{IS(lim)}$ have the greatest influence. The temperature dependency of dk_{ILIS} is described in **Chapter 5.1.3**, and of $I_{IS(lim)}$ in **Chapter 5.5.2.1**:

- For a rising temperature, the fault condition current $I_{IS(lim)}$ increases, and vice versa.
- For a rising temperature the dk_{ILIS} decreases and vice versa.

This relationship is also illustrated by **Figure 22**.

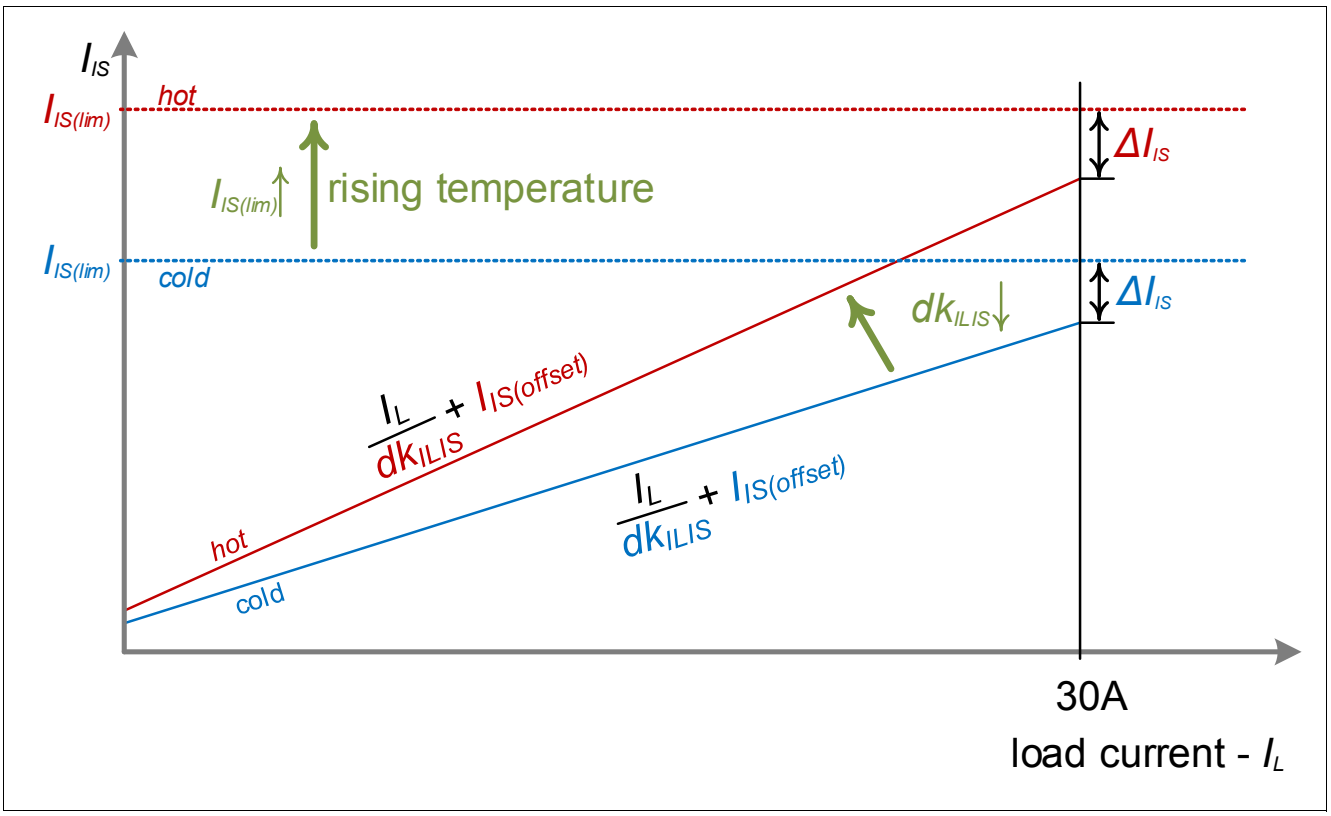

Figure 22 Illustration of the temperature dependencies of the fault distance and relevant parameters

Additionally the difference between the fault condition current $I_{IS(lim)}$ and the sensed current $I_{IS}(I_L)$ can be calculated as follows:

(5.3)

$$\Delta I_{IS} = I_{IS(lim)} - I_{IS(I_L)} = I_{IS(lim)} - \left(\frac{I_L}{dk_{ILIS}} + I_{IS(offset)} \right)$$

Equation (5.3) shows, that for a rising temperature, both $I_{IS(lim)}$ and $I_{IS}(I_L)$ (due to I_L / dk_{ILIS}) increase.

Combining the spread of dk_{ILIS} and $I_{IS(lim)}$ over temperature, this behavior results in a ΔI_{IS}that, at the min. current limitation detection level $I_{CLx0,min}$, is typically above 0,5 mA for the BTN8960/62, as shown in **Figure 23** and **Figure 24** and above 0,75 mA for the BTN8980/82, shown in **Figure 25** and **Figure 26**. To summarize, we can say that it is possible to distinguish between a current sense signal $I_{IS}(I_L)$ and a fault condition current $I_{IS(lim)}$ for any temperature.

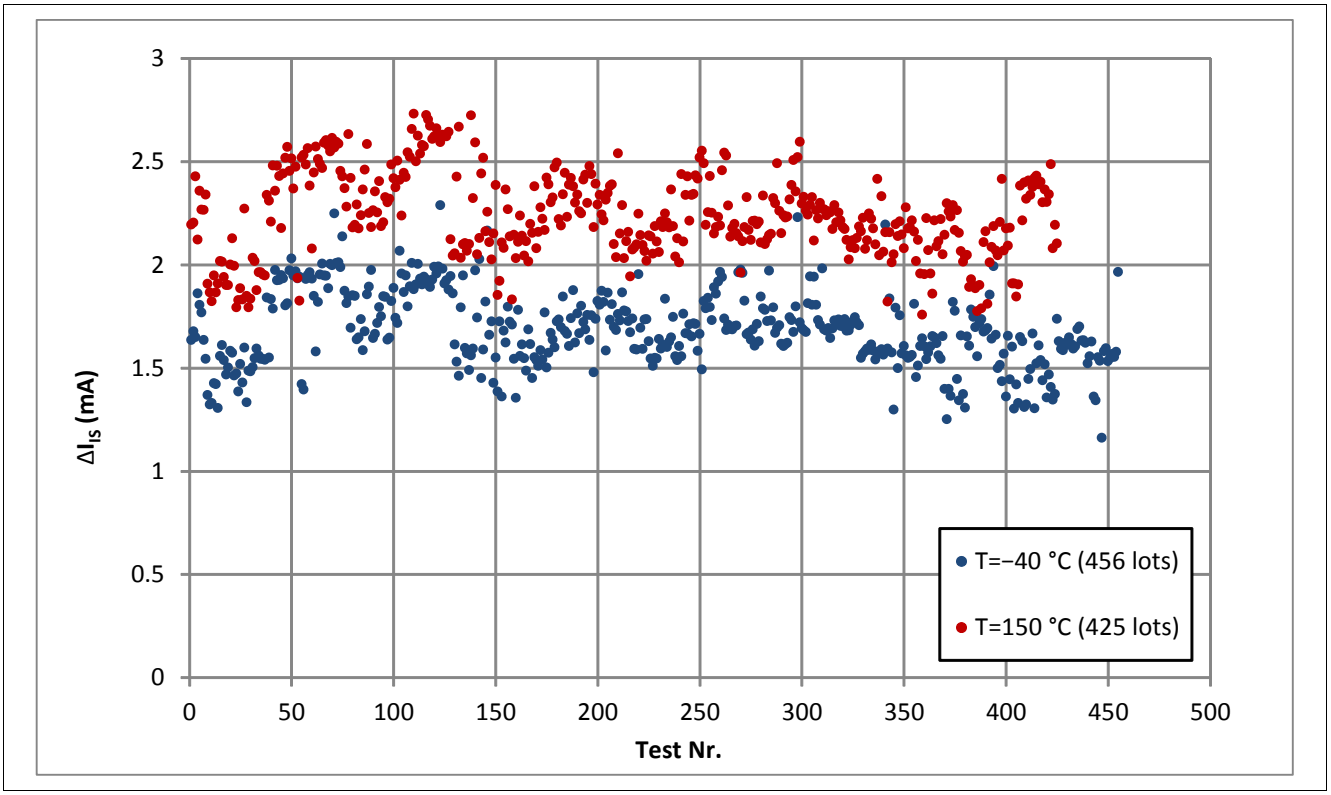

Figure 23 Temperature dependent ΔI_{IS} for BTN8960/62, according to Equation (5.3), for the median value of each lot and temperature at the min. current limitation detection level $I_L = I_{CLx0,min}$ = 30 A.

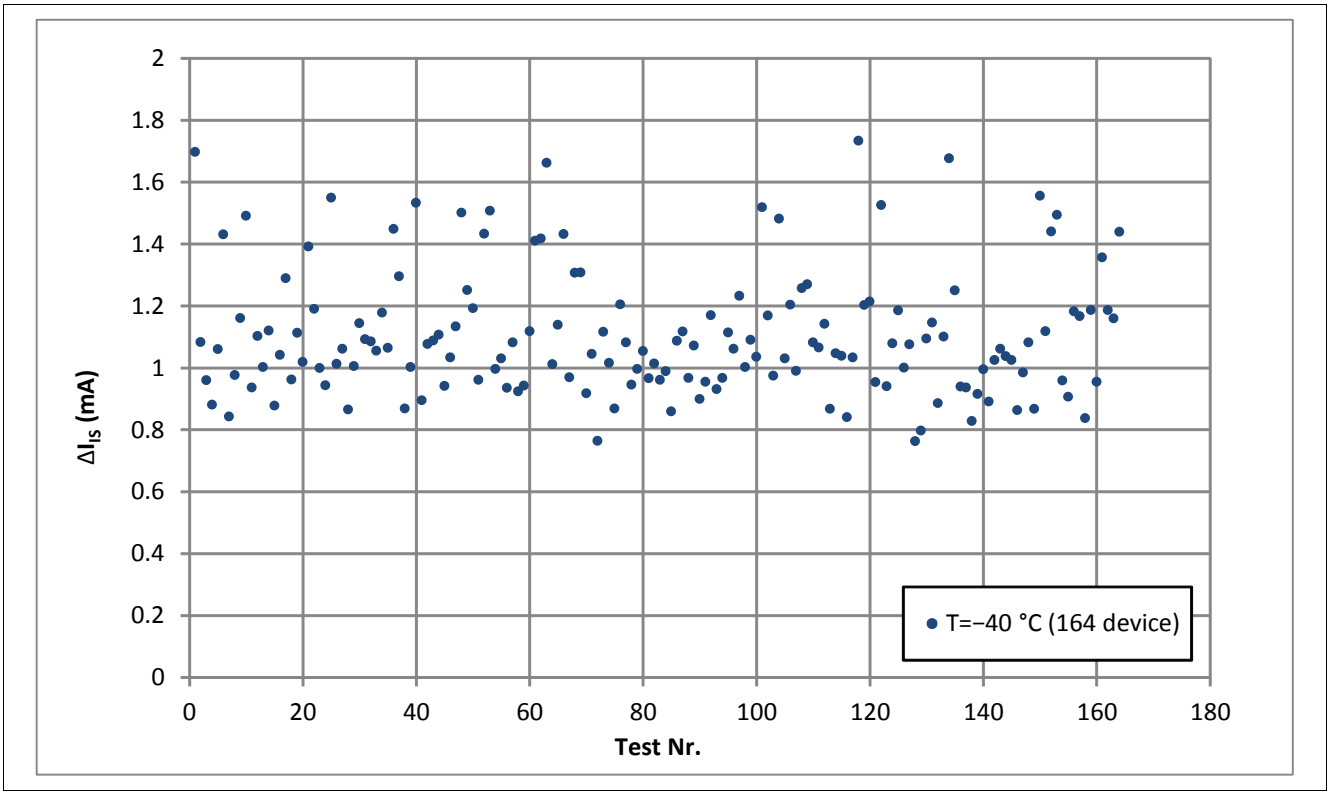

Figure 24 Temperature dependent ΔI_{IS} for BTN8960/62, according to Equation (5.3), calculated individually for each device of lot 447 for −40°C in Figure 23, with $I_L = I_{CLx0,min}$ = 30 A.

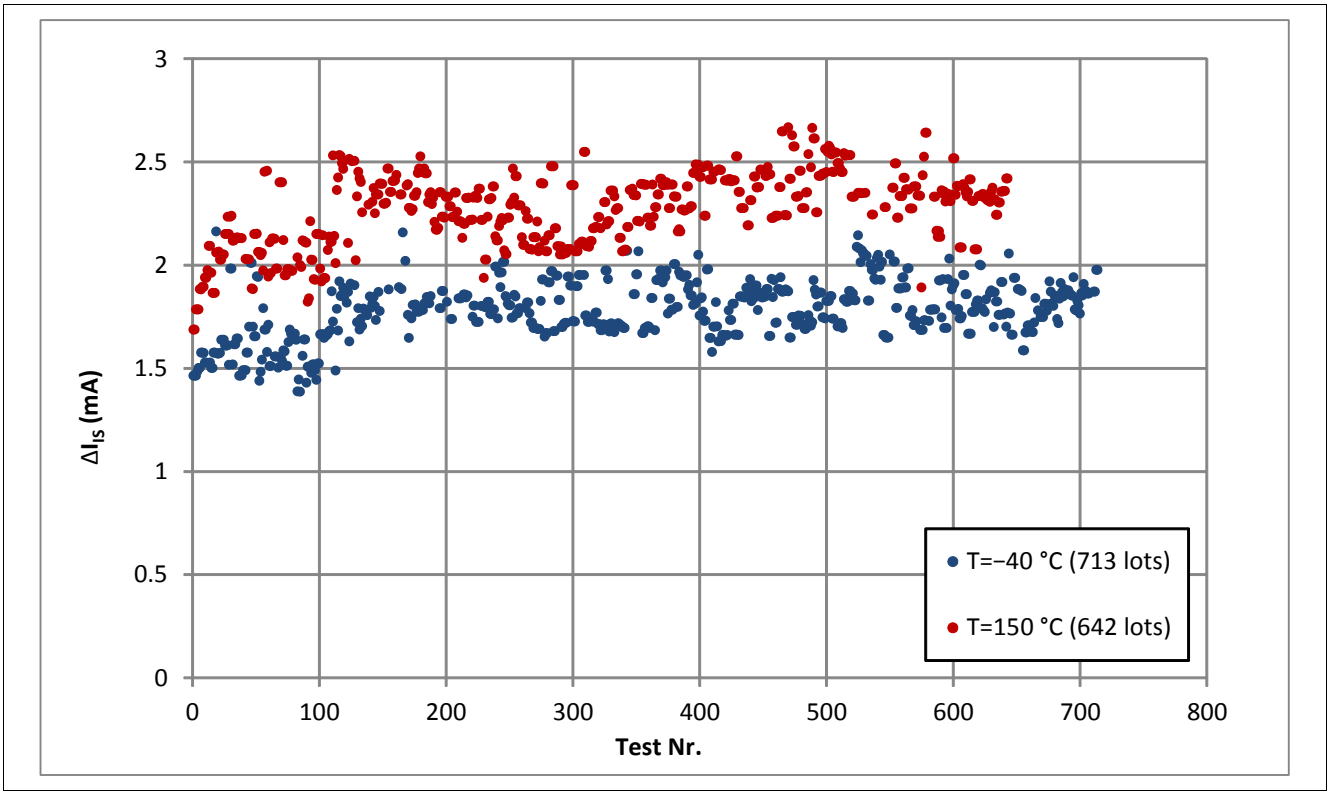

Figure 25 Temperature dependent ΔI_{IS} for BTN8980/82, according to Equation (5.3), for the median value of each lot and temp. at the min. current limitation detection level $I_L = I_{CLx0,min}$ = 55 A.

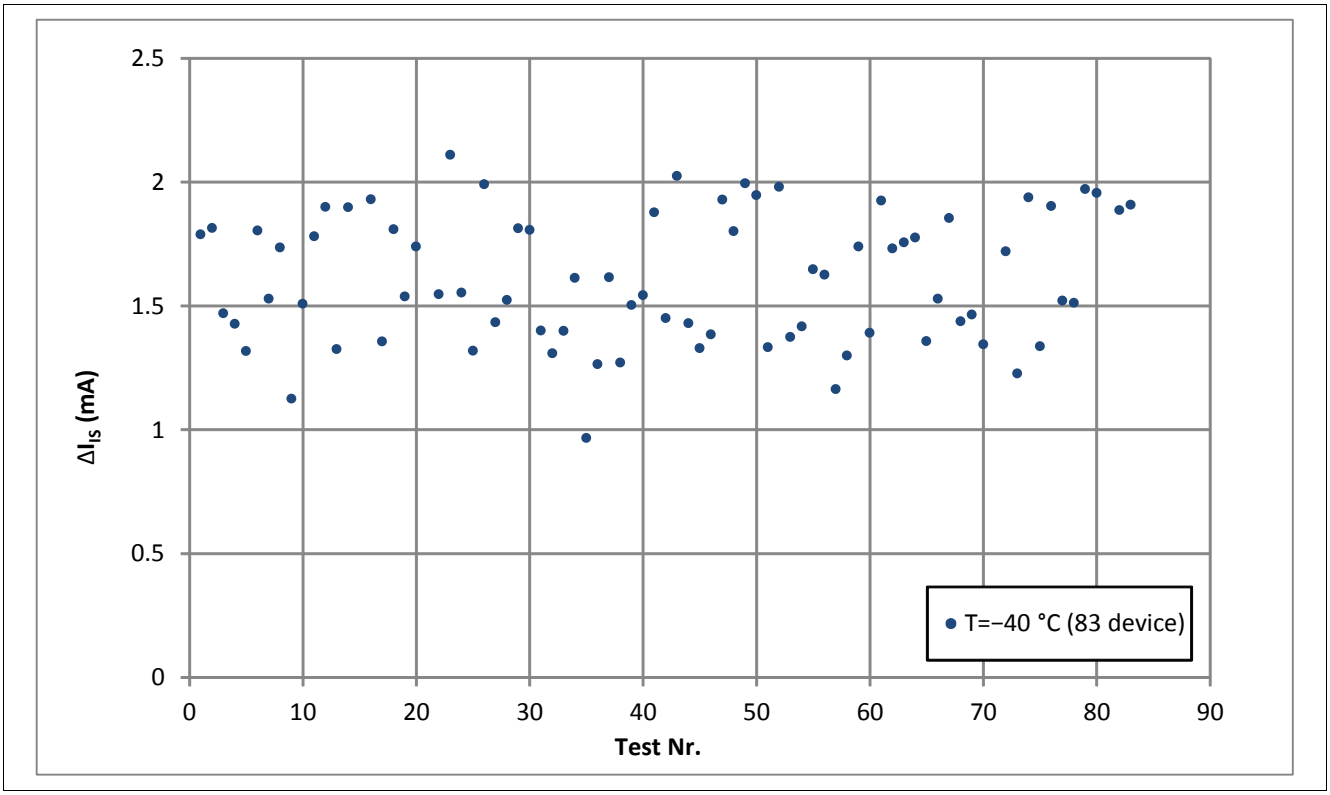

Figure 26 Temperature dependent ΔI_{IS} for BTN8982, according to Equation (5.3) calculated individually for each tested device of lot 85 for −40°C in Figure 25, with $I_L = I_{CLx0,min}$ = 55 A.

5.5.2.1 Temperature drift of the IS-pin's current in fault condition $I_{IS(lim)}$

The characteristics of the $I_{IS(lim)}$ vs. temperature and production spread is shown in **Figure 27** for the BTN8960/62 and in **Figure 28** for the BTN8980/82, including a series of lab measurement points for one device.

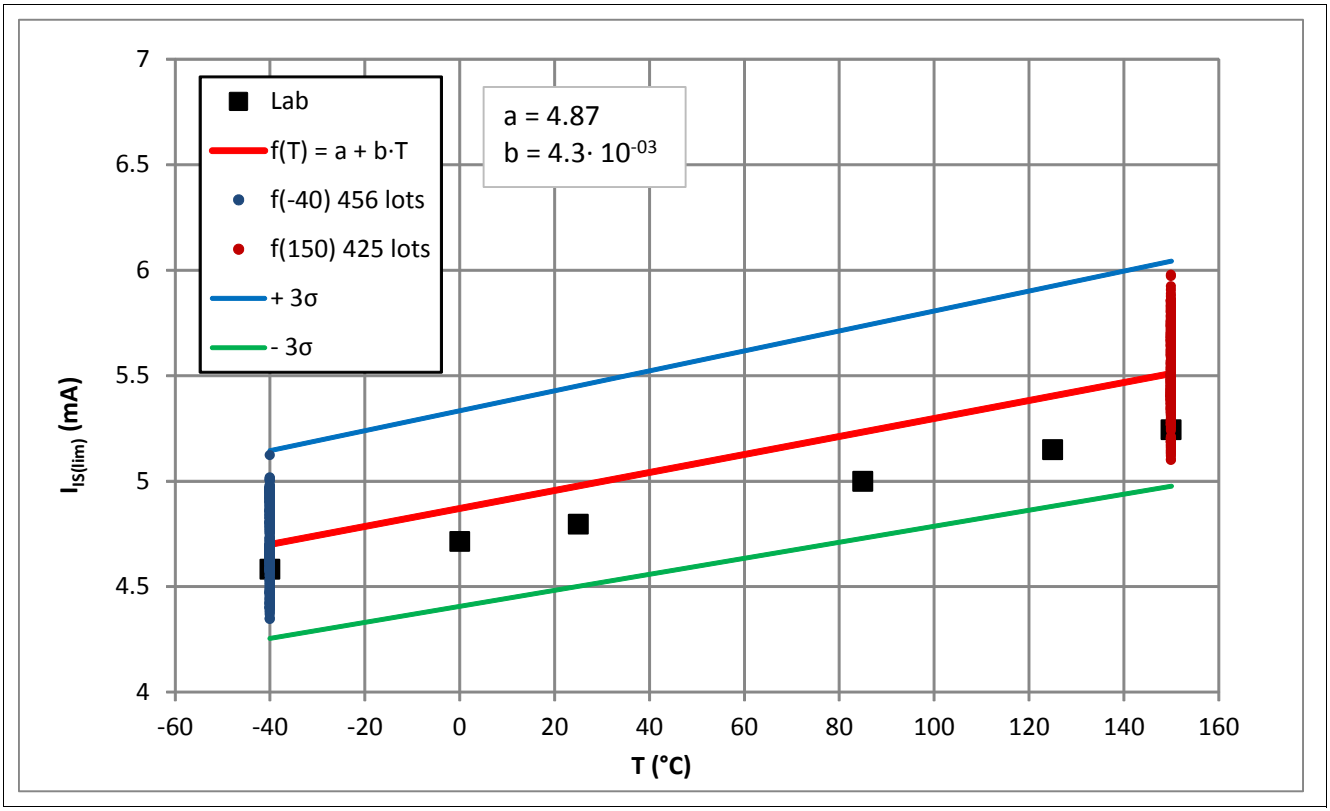

Figure 27 BTN8960/62 $I_{IS(lim)}$ vs. temperature

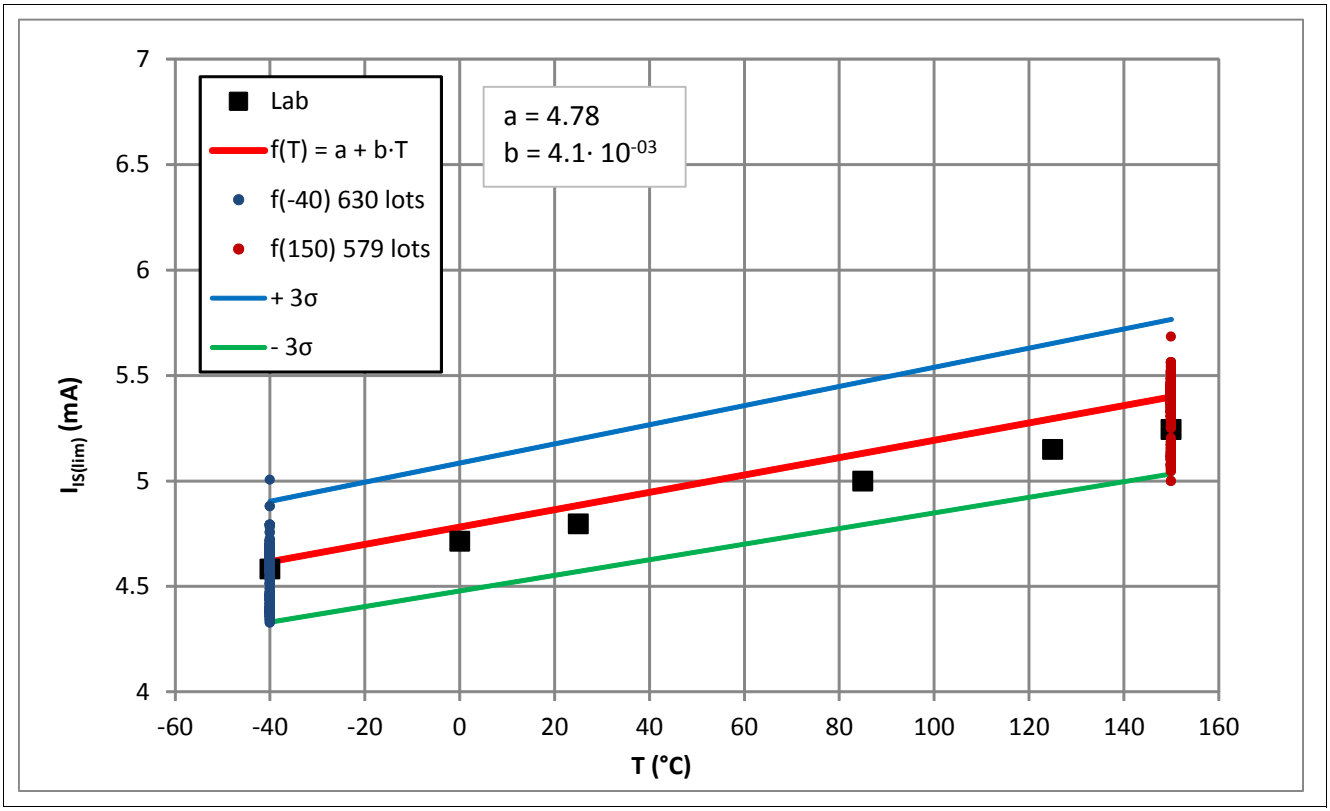

Figure 28 BTN8980/82 $I_{IS(lim)}$ vs. temperature

5.5.2.2 Failure detection flow chart

The consideration of ΔI_{IS} above provides a procedure for detecting fault conditions ($I_{IS(lim)}$), which is also summarized in **Figure 29**:

- Calibration of $I_{IS(lim)}(T_0)$ for a specific temperature T_0: Calculation of offset a with the given / typical slope b. Ideally measurement of $I_{IS(lim)}(T_1)$ for a second temperature T_1, to perform a two point calibration and calculate both offset a and slope b for each individual device.
- Calculation of temperature dependent $I_{IS(lim)}(T)$ = f(T) while the device is operating according to **Chapter 5.5.2.1**.
- If a current limit of $I_{IS} = I_{IS(lim)}(T)$ - 0,5 mA (BTN8960/62, respectively 0,75 mA for the BTN8980/82) is exceeded, a fault condition is detected.

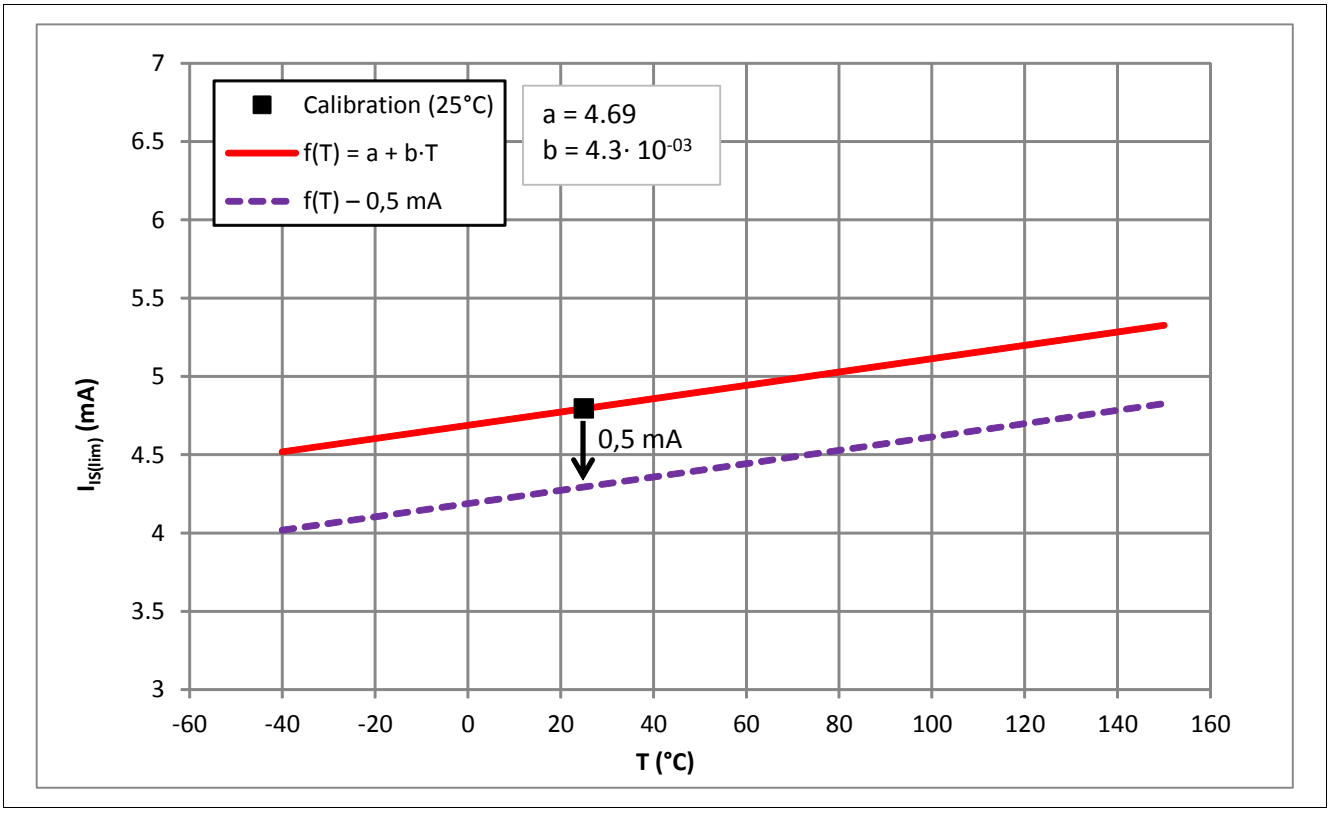

Figure 29 One point calibration of $I_{IS(lim)}$ and the resulting fault detection level over temperature for the BTN8960/62

Additional measures are available for ascertaining fault conditions. **Figure 30** describes a possible procedure. Carrying out a plausibility check after detecting a potential fault allows you to determine if a specific load current value in the current range of $I_{IS(lim)}$ is possible at a specific operating point.
If this is the case, check whether that value stays in a certain range by performing a series of measurements. Depending on the application, the scattering of the current sense signal of an electric motor should be much higher than that of the constant fault current. An additional way of validating a fault condition is by measuring the IS output pin for a low IN input pin. As illustrated in **Figure 17**, the fault condition can be monitored by choosing the low side freewheeling path, ensuring that no current is flowing through the high side MOSFETs. The fault condition current $I_{IS(lim)}$ can be clearly distinguished from the lower offset current $I_{IS(offset)}$. For applications running with a PWM duty cycle of 100 %, the duty cycle must be reduced for certain cycles in order to validate a fault condition. This fault detection procedure is summarized in **Figure 30**.

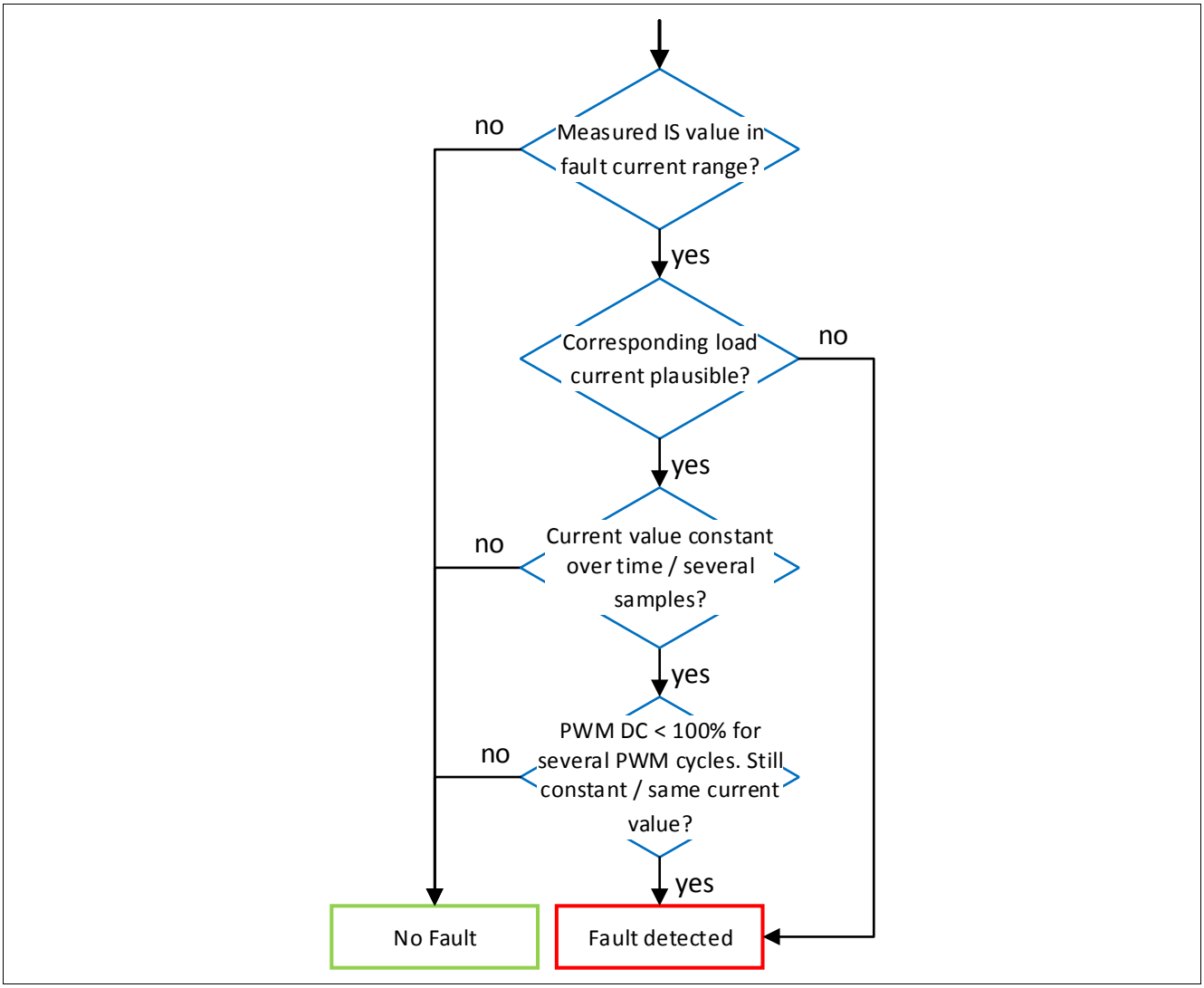

Figure 30 Possible fault condition validation process flow

6 Switching Timing

For the ADC measurement of the IS-pin, the timing behavior of the BTNx9yz needs to be considered. As the current sense output is proportional to the current through the high side switch, only the high side switch behavior is considered here exemplary. The behavior of the low side switch can be considered in an equal fashion. An overview of the rising and falling switching procedure is shown in **Figure 31**.

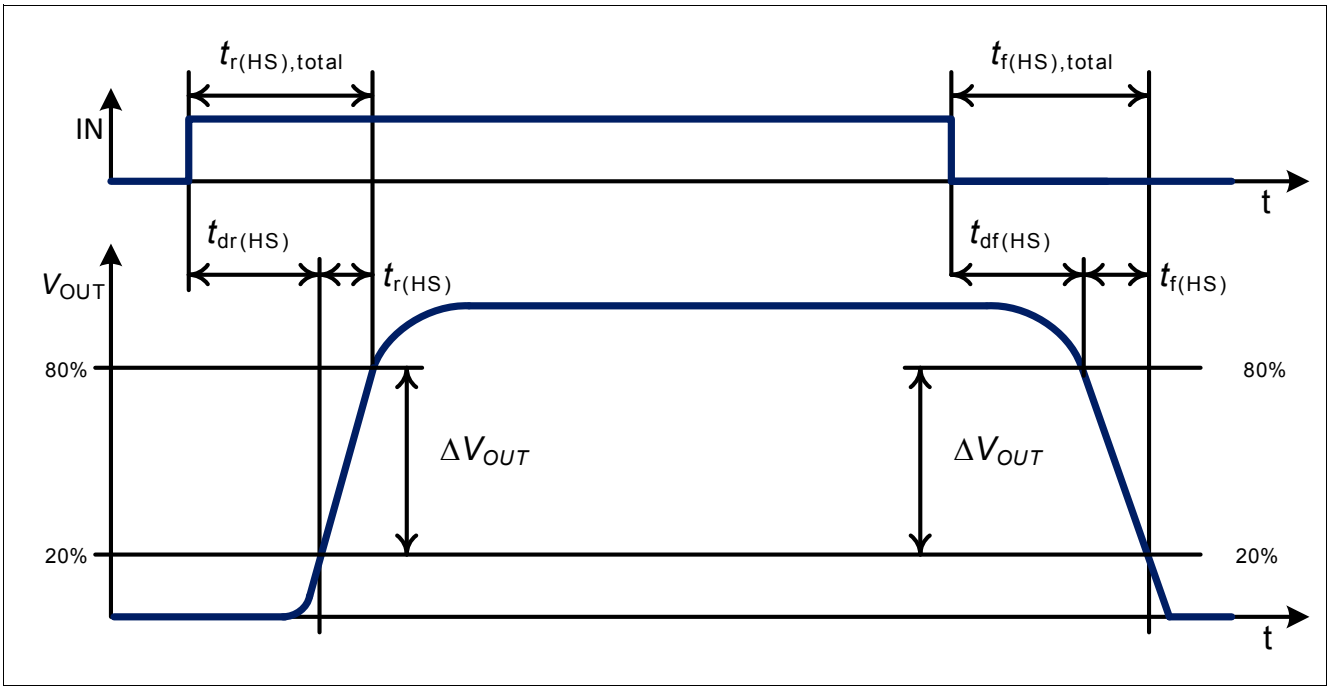

Figure 31 Timing behavior overview of a BTNx9yz high side switch

6.1 Timing behavior for rising edge on high side switch

As shown in the data sheet, the time between the IN-pin rising from a 0 to 1 corresponding voltage level and the BTN8960 /62 /80 /82 output voltage rising from (around) 0 V to 80 % of the final output voltage (typically: $V_{OUT} \approx V_S$) can be summed up to the following delay, as shown in **Figure 31**:

$$t_{r(HS),total} = t_{dr(HS)} + t_{r(HS)} \quad (6.1)$$

Depending on the chosen resistor value for R_{SR}, both the switch ON delay time $t_{dr(HS)}$ and the rise-time $t_{r(HS)}$ get affected. The dependencies are shown in **Figure 32** (BTN8962TA) / **Figure 35** (BTN8982TA) for the switch ON delay time $t_{dr(HS)}$ and in **Figure 33** (BTN8962TA) / **Figure 36** (BTN8982TA) for the rise-time $t_{r(HS)}$. The resulting dependency of the resistor R_{SR} on the total delay time $t_{r(HS),total}$ is displayed in **Figure 34** (BTN8962TA) / **Figure 37** (BTN8982TA).

6.1.1 BTN8962TA

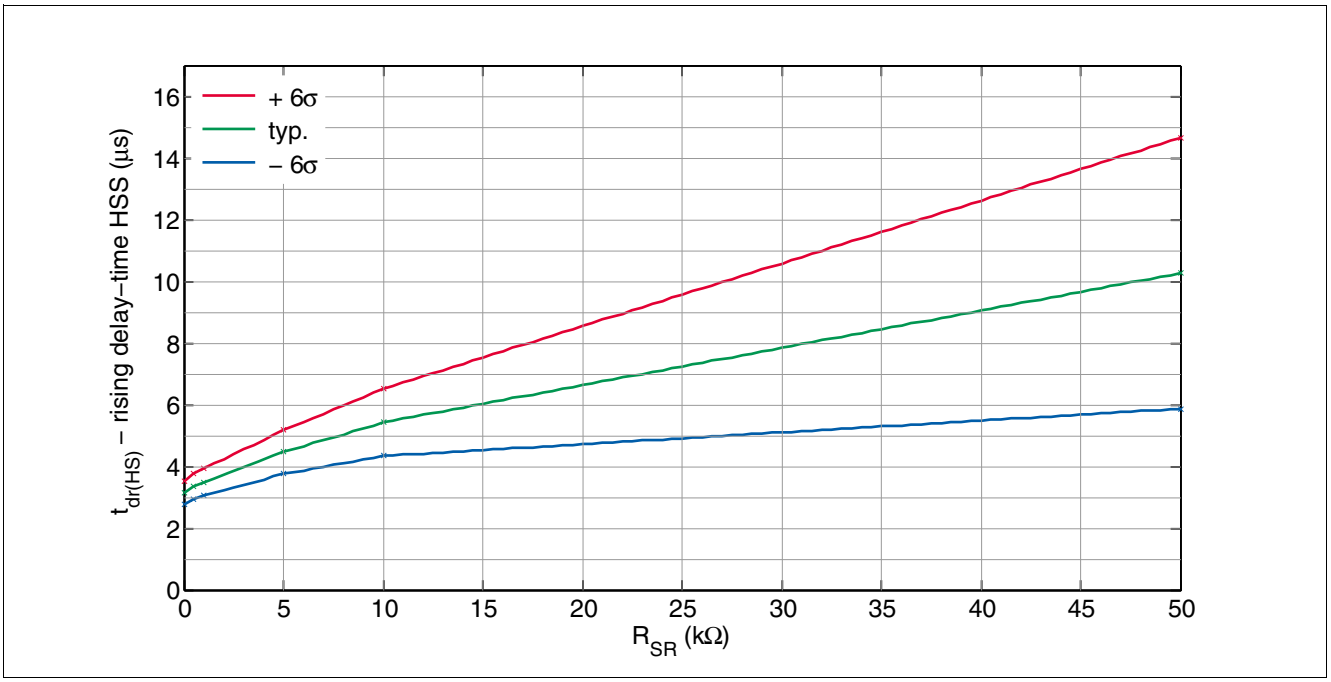

Figure 32 Dependency of the slew rate resistor R_{SR} on the rising delay time of the high side switch $t_{dr(HS)}$: BTN8962TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

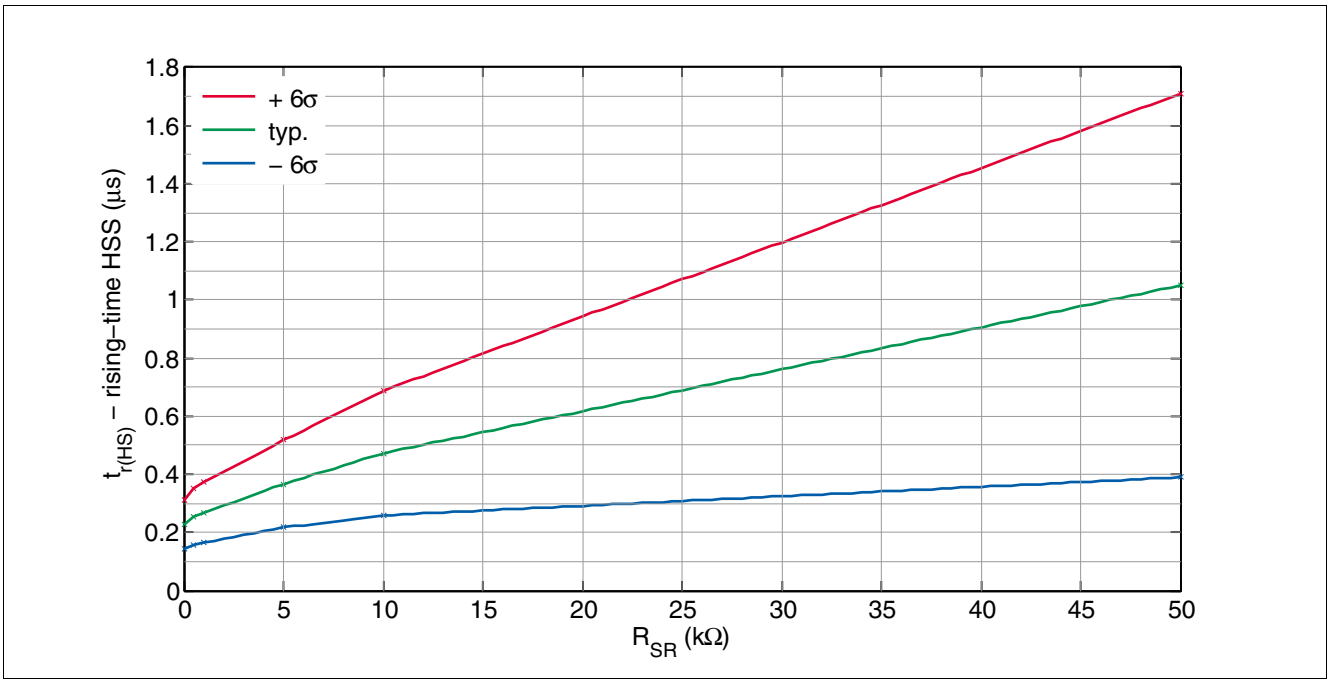

Figure 33 Dependency of the slew rate resistor R_{SR} on the rising time of the high side switch $t_{r(HS)}$: BTN8962TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

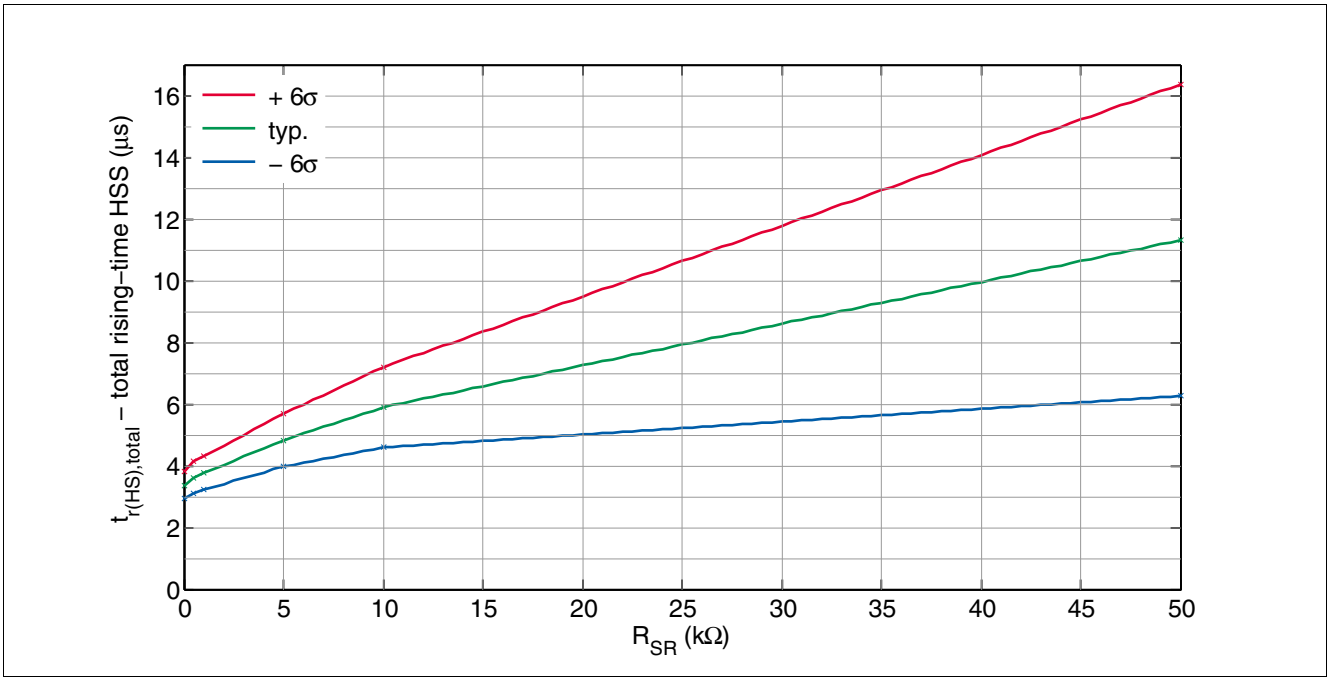

Figure 34 Dependency of the slew rate resistor R_{SR} on the total rising time of the high side switch with $t_{r(HS),total} = t_{r(HS)} + t_{dr(HS)}$: BTN8962TA ($V_S$ = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

6.1.2 BTN8982TA

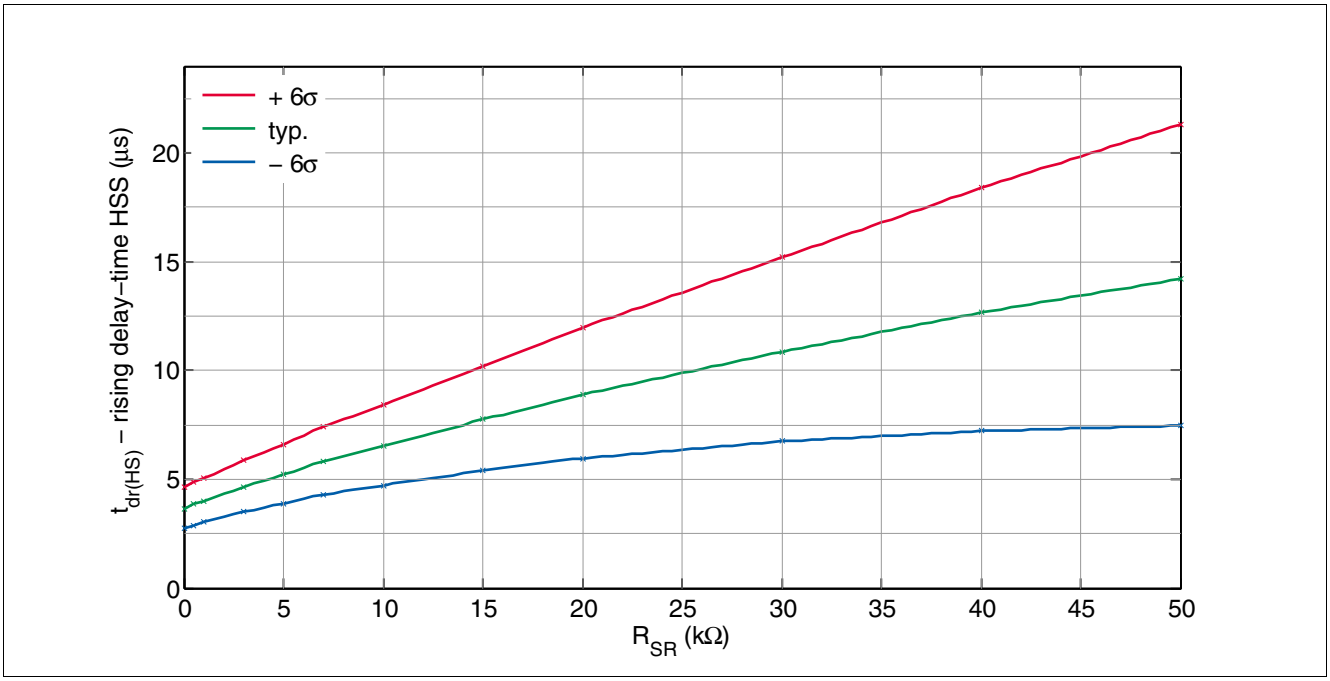

Figure 35 Dependency of the slew rate resistor R_{SR} on the rising delay time of the high side switch $t_{dr(HS)}$: BTN8982TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

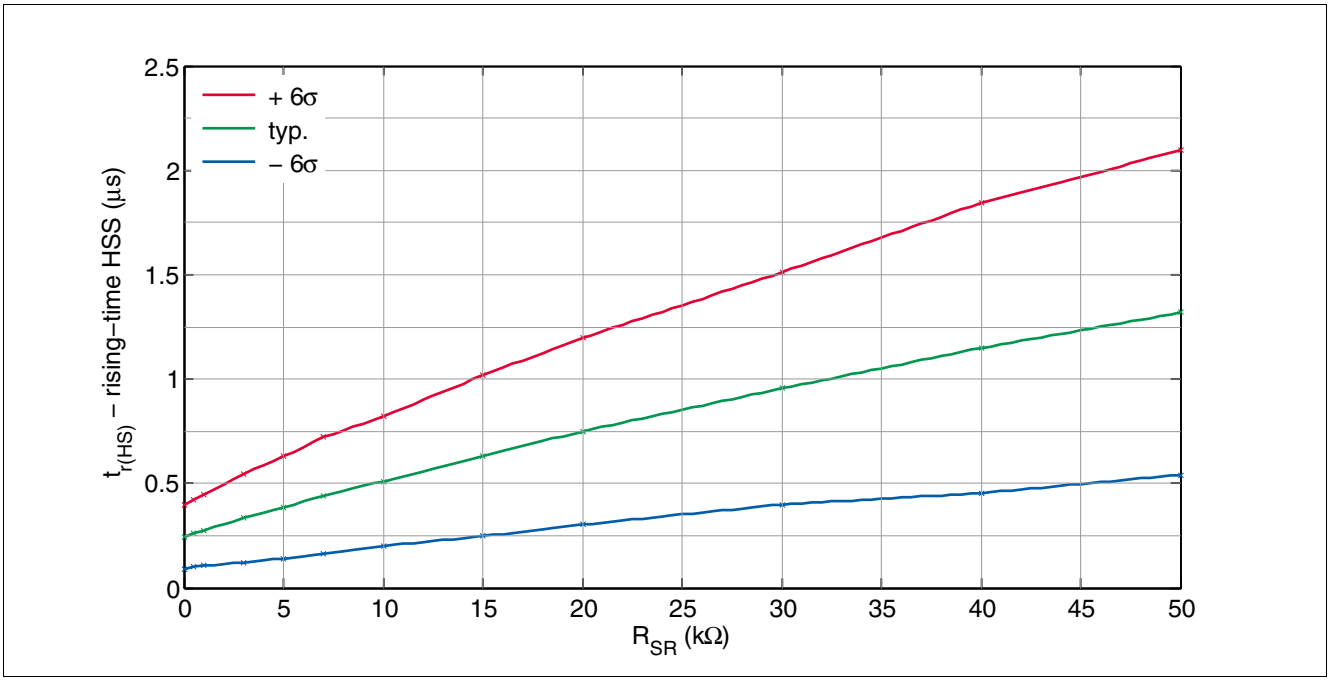

Figure 36 Dependency of the slew rate resistor R_{SR} on the rising time of the high side switch $t_{r(HS)}$: BTN8982TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

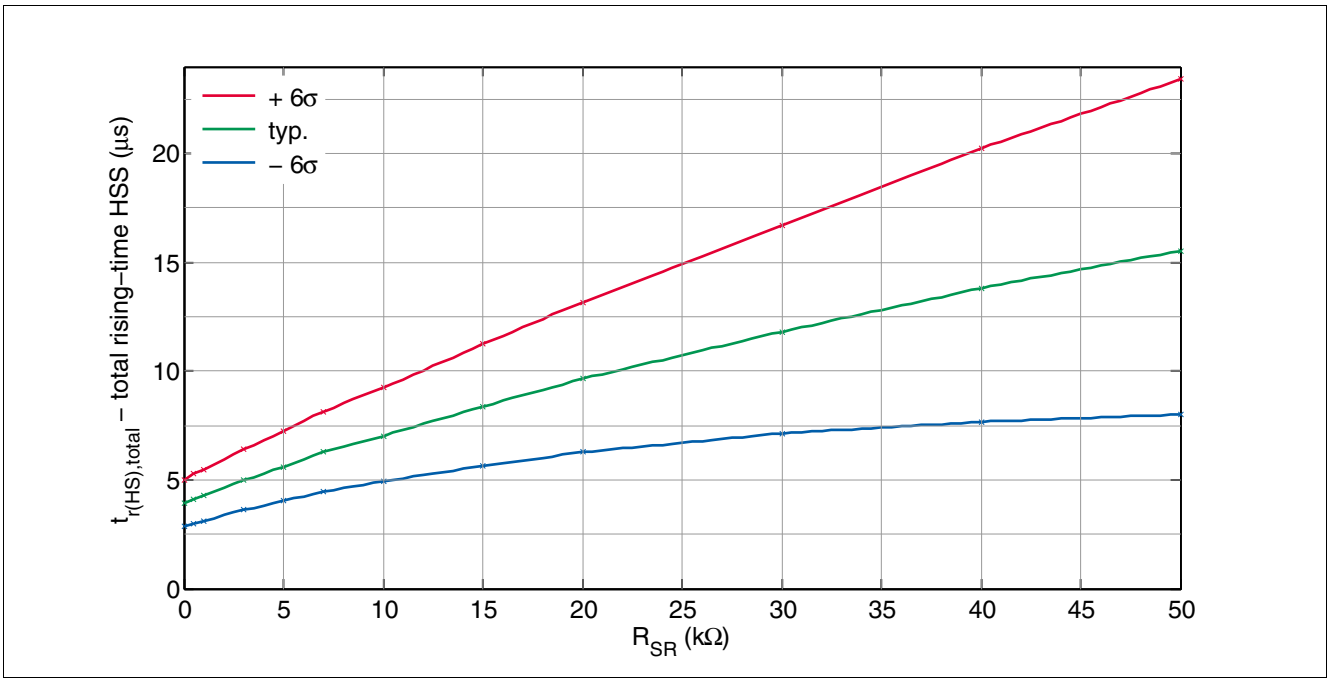

Figure 37 Dependency of the slew rate resistor R_{SR} on the total rising time of the high side switch with $t_{r(HS),total}$ = $t_{r(HS)}$ + $t_{dr(HS)}$: BTN8982TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

6.2 Timing behavior for falling edge on high side switch

For a falling edge on the IN input pin, the delay time between the falling edge of the IN input pin and the lower deviation of 20 % of the $V_{OUT} \approx V_S$ voltage level of the output pin OUT is considered:

$$t_{f(HS),total} = t_{df(HS)} + t_{f(HS)} \quad (6.2)$$

The dependencies of the resistor R_{SR} on the delays are shown in **Figure 38** (BTN8962TA) / **Figure 41** (BTN8982TA) for $t_{df(HS)}$, **Figure 39** (BTN8962TA) / **Figure 42** (BTN8982TA) for $t_{f(HS)}$ and resulting in the total delay time $t_{f(HS),total}$ in **Figure 40** (BTN8962TA) / **Figure 43** (BTN8982TA).

6.2.1 BTN8962TA

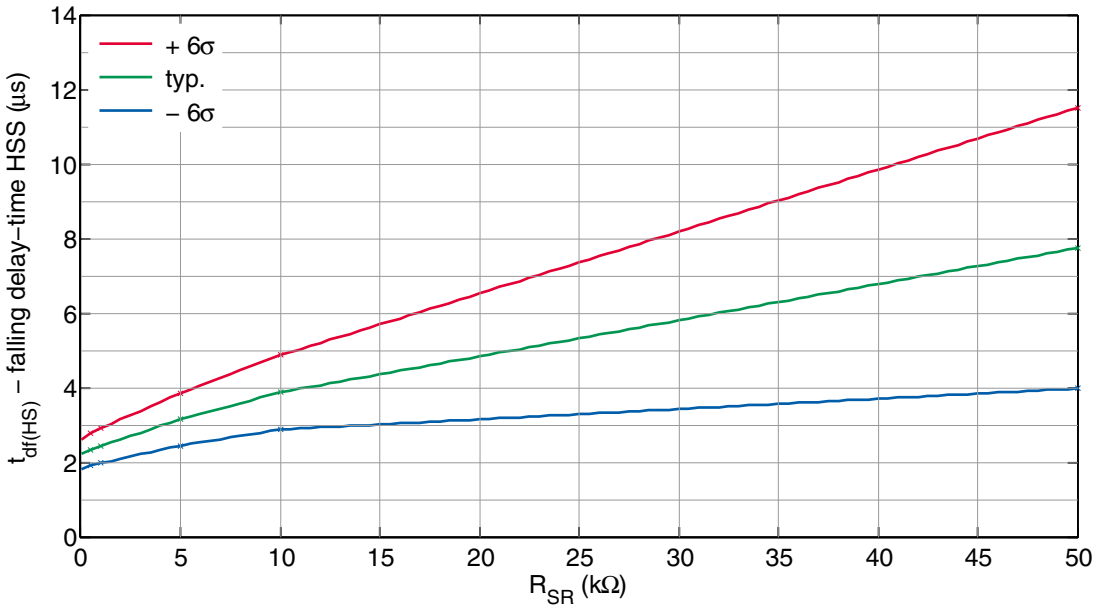

Figure 38 Dependency of the slew rate resistor R_{SR} on the falling delay time of the high side switch $t_{df(HS)}$: BTN8962TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

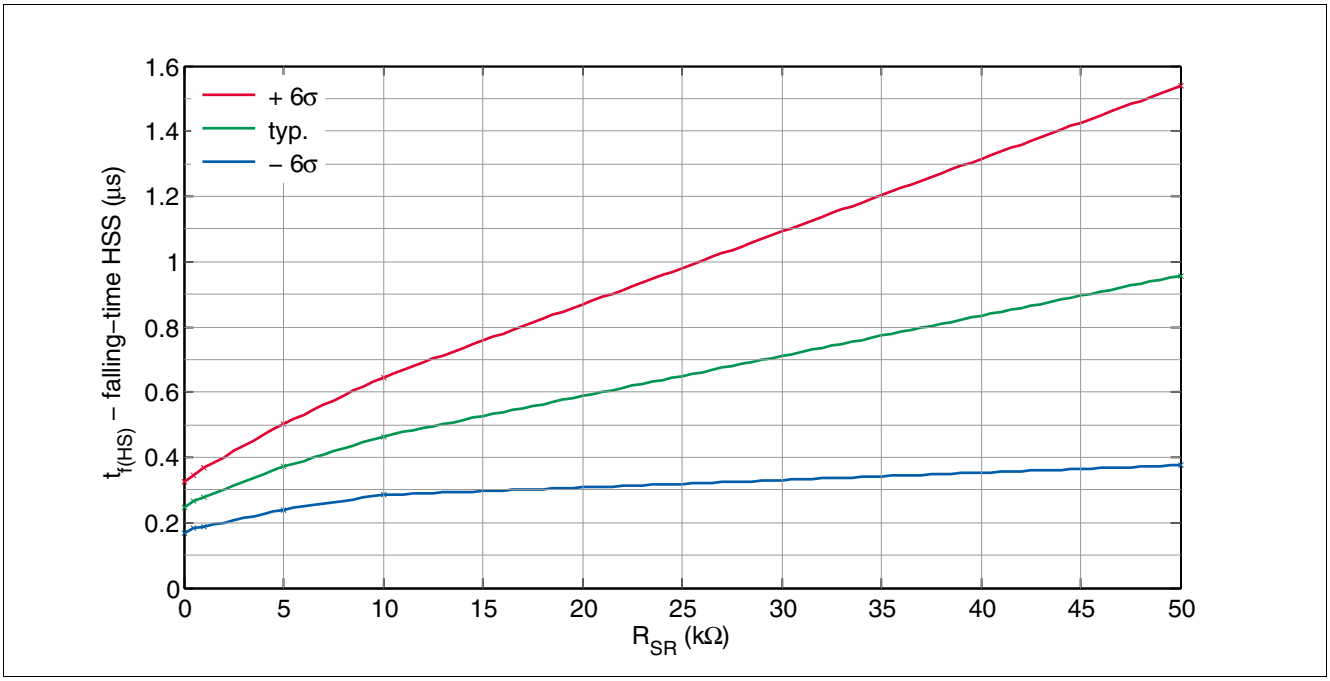

Figure 39 Dependency of the slew rate resistor R_{SR} on the falling time of the high side switch $t_{f(HS)}$: BTN8962TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

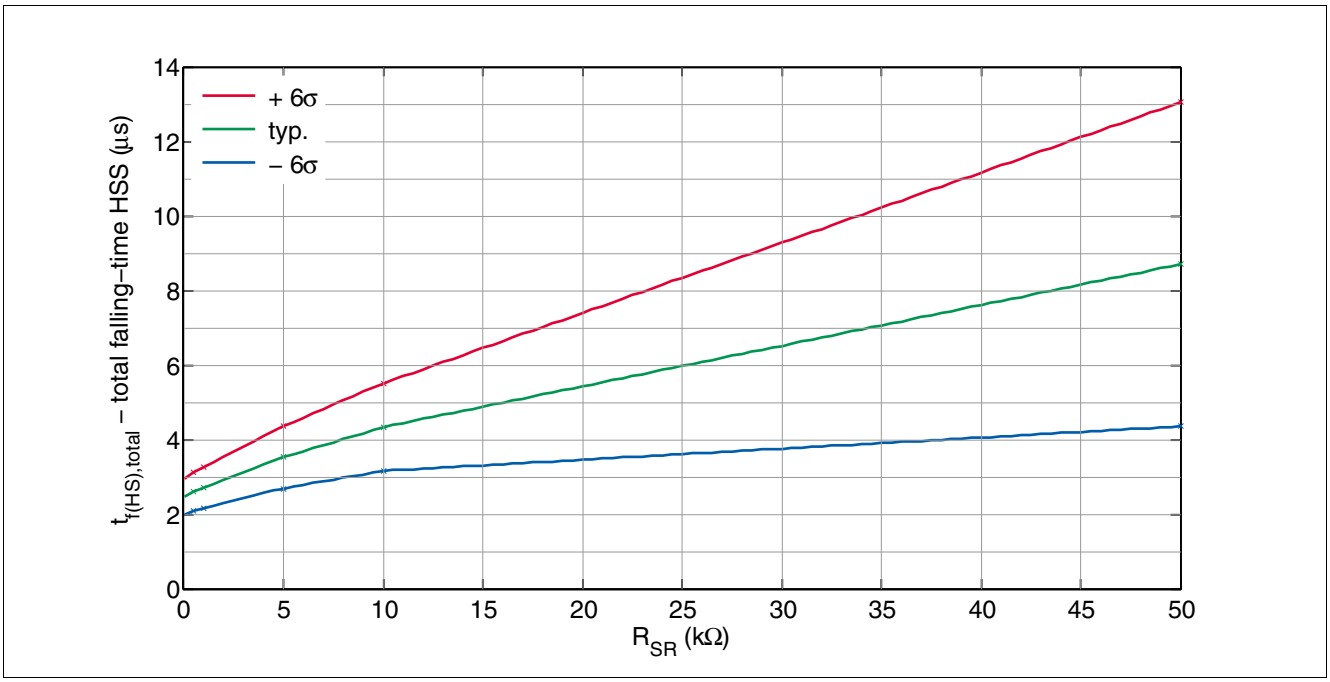

Figure 40 Dependency of the slew rate resistor R_{SR} on the total falling time of the high side switch with $t_{f(HS),total} = t_{f(HS)} + t_{df(HS)}$: BTN8962TA ($V_S$ = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

6.2.2 BTN8982TA

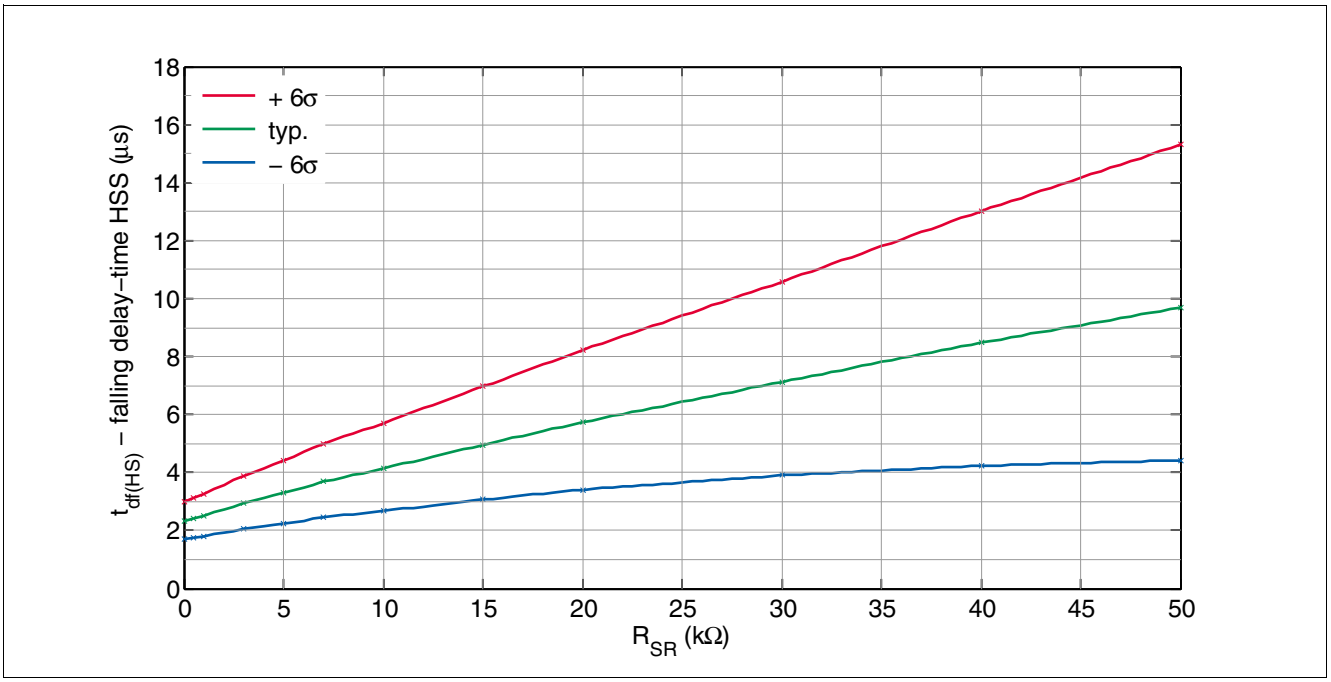

Figure 41 Dependency of the slew rate resistor R_{SR} on the falling delay time of the high side switch $t_{df(HS)}$: BTN8982TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

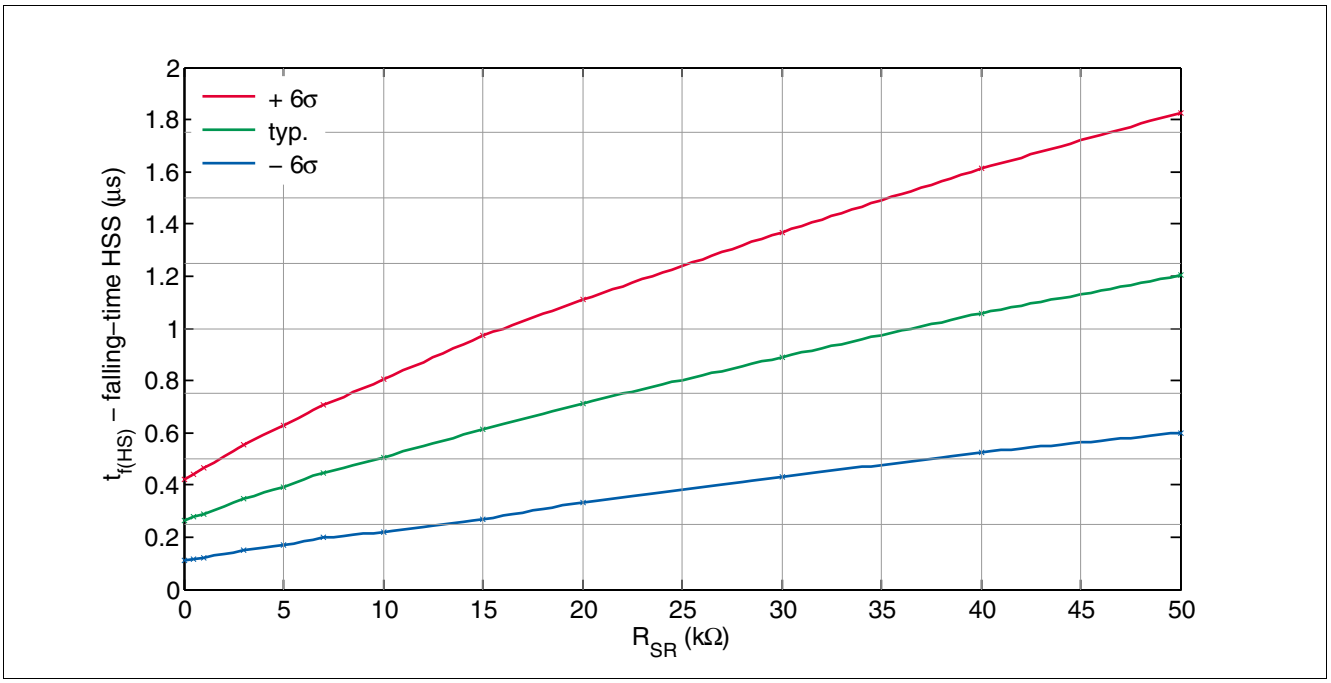

Figure 42 Dependency of the slew rate resistor R_{SR} on the falling time of the high side switch $t_{f(HS)}$: BTN8982TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

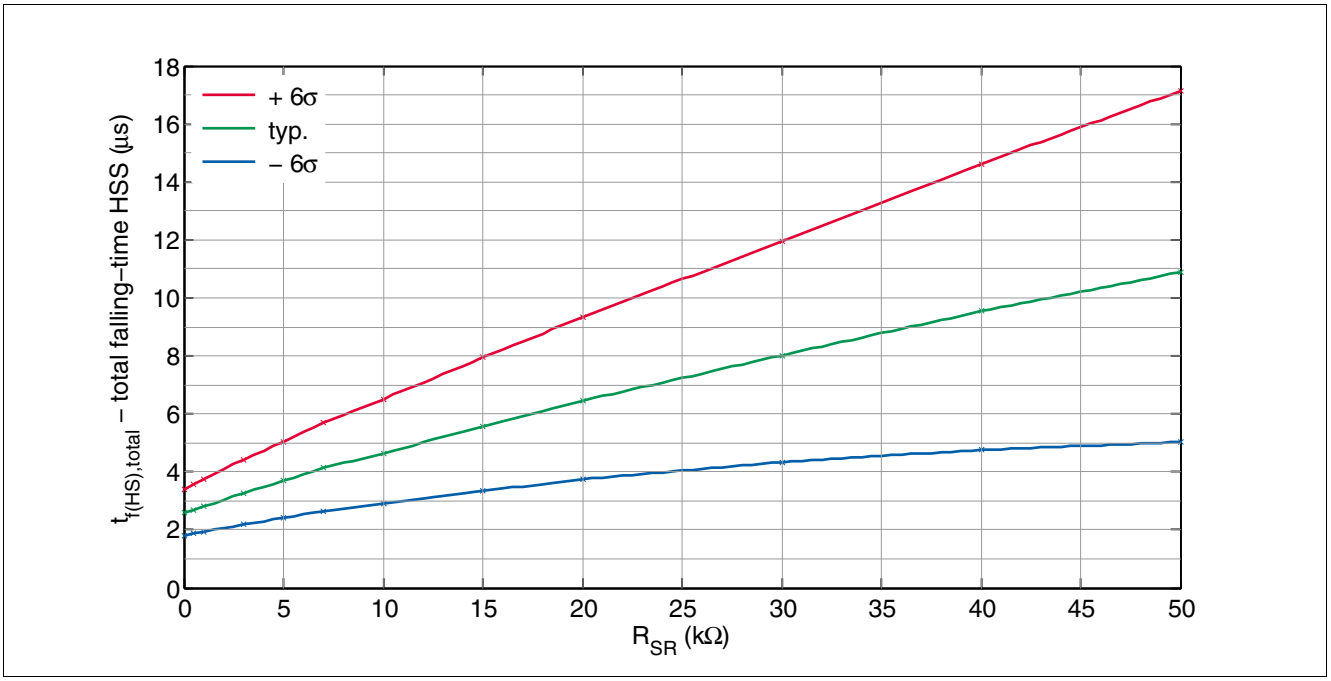

Figure 43 Dependency of the slew rate resistor R_{SR} on the total falling time of the high side switch with $t_{f(HS),total} = t_{f(HS)} + t_{df(HS)}$: BTN8982TA ($V_S$ = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

6.3 Timing behavior for rising edge on low side switch

Both the switch ON delay time $t_{dr(LS)}$ and the rise-time $t_{r(LS)}$ depend on the resistance of R_{SR}. The dependencies are shown in **Figure 44** (BTN8962TA) / **Figure 46** (BTN8982TA) for the switch ON delay time $t_{dr(LS)}$ and in **Figure 45** (BTN8962TA) / **Figure 47** (BTN8982TA) for the rise-time $t_{r(LS)}$, according to the definition from the data sheet, which is also shown in **Figure 31**.

6.3.1 BTN8962TA

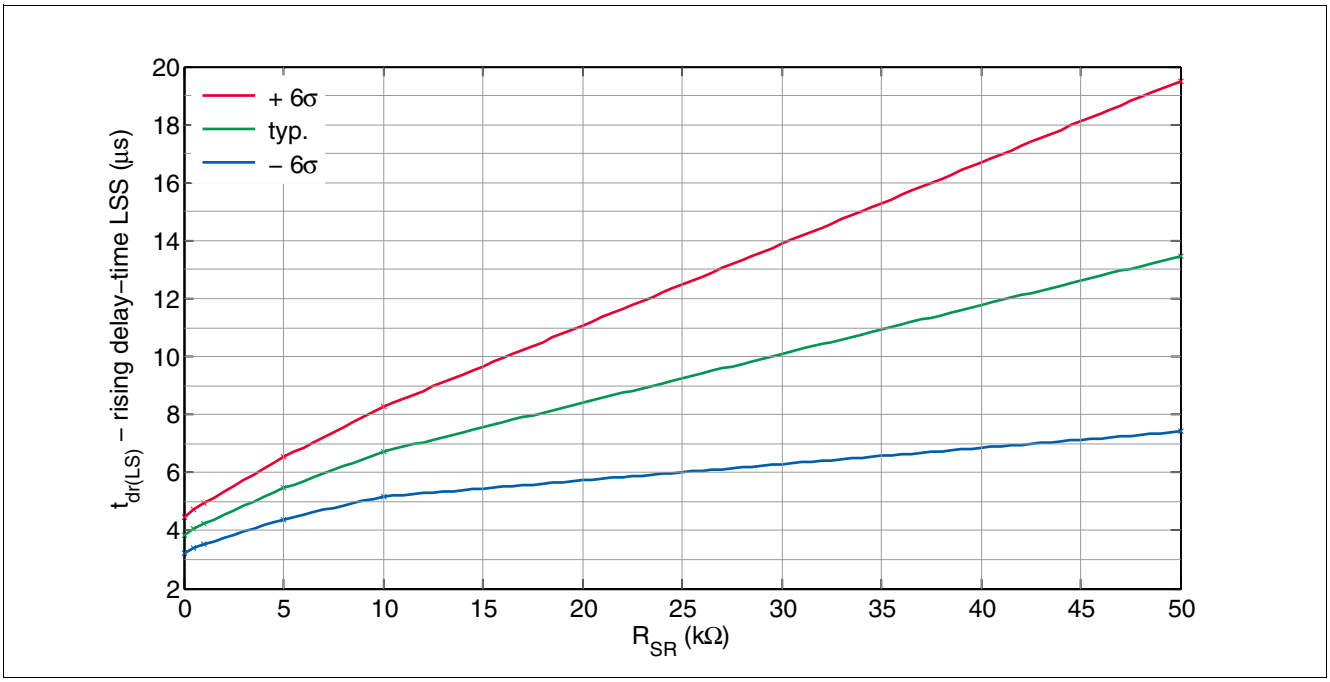

Figure 44 Dependency of the slew rate resistor R_{SR} on the rising delay time of the low side switch $t_{df(HS)}$: BTN8962TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

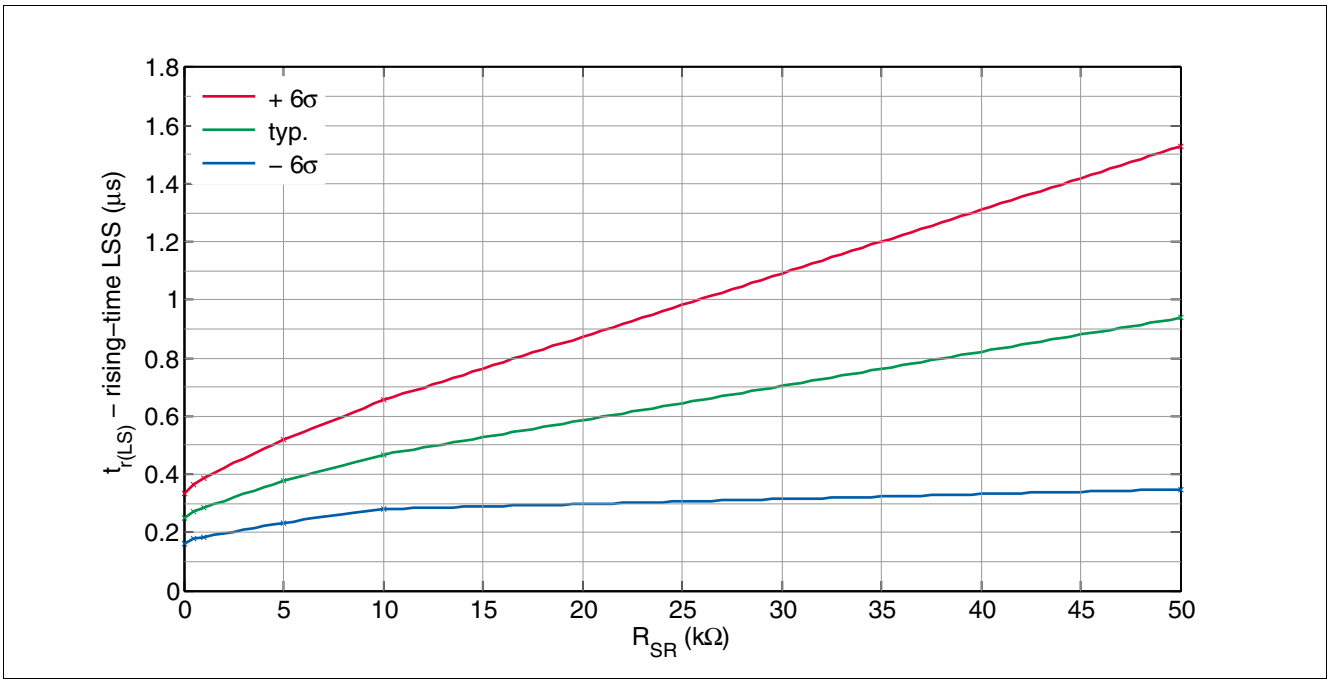

Figure 45 Dependency of the slew rate resistor R_{SR} on the rising time of the low side switch $t_{f(HS)}$: BTN8962TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

6.3.2 BTN8982TA

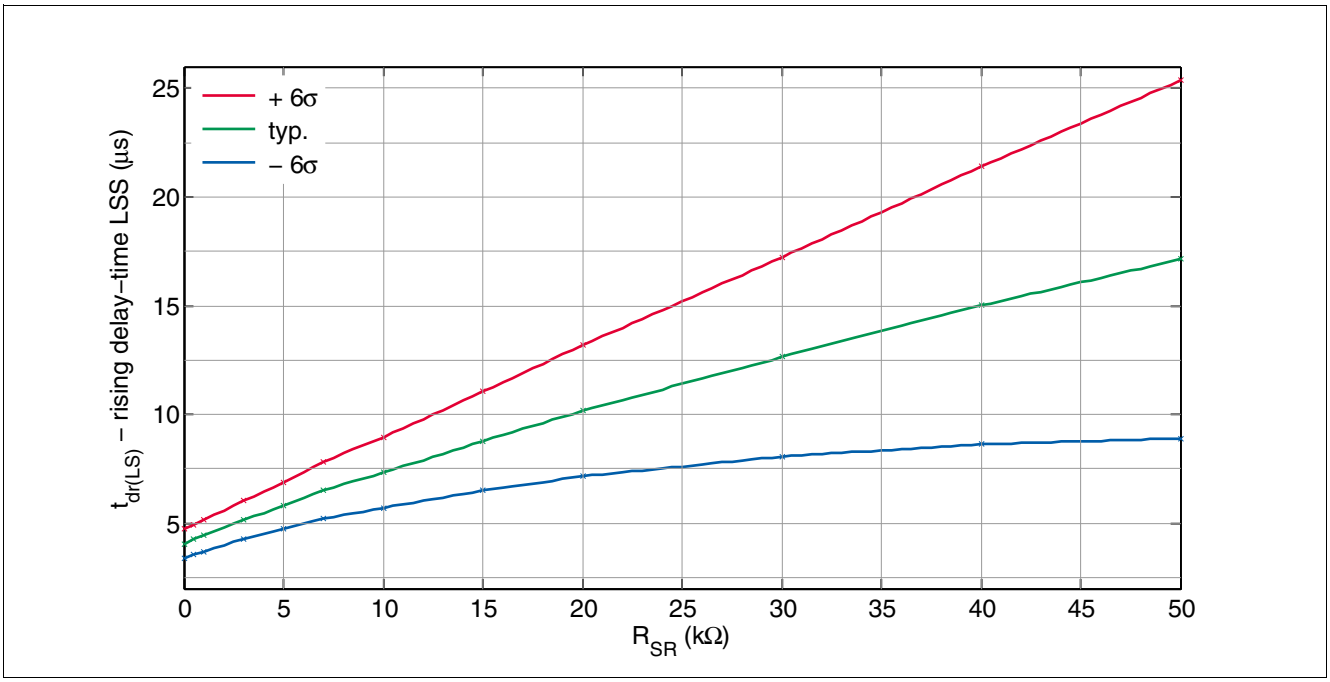

Figure 46 Dependency of the slew rate resistor R_{SR} on the rising delay time of the low side switch $t_{df(HS)}$: BTN8982TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

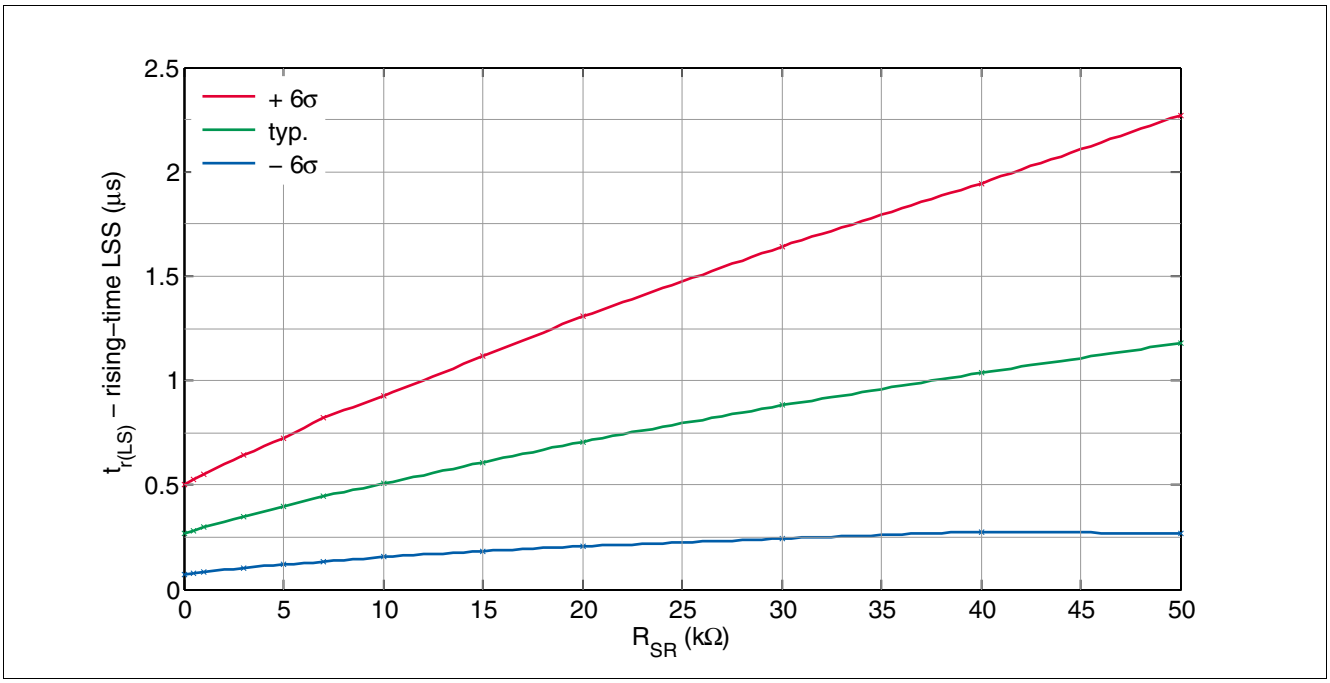

Figure 47 Dependency of the slew rate resistor R_{SR} on the rising time of the low side switch $t_{f(HS)}$: BTN8982TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

6.4 Timing behavior for falling edge on low side switch

The dependencies of the resistor R_{SR} on the delays are shown in **Figure 48** (BTN8962TA) / **Figure 50** (BTN8982TA) for $t_{df(LS)}$, **Figure 49** (BTN8962TA) / **Figure 51** (BTN8982TA) for $t_{f(LS)}$, based on the data sheet's definition, which is shown in **Figure 31**.

6.4.1 BTN8962TA

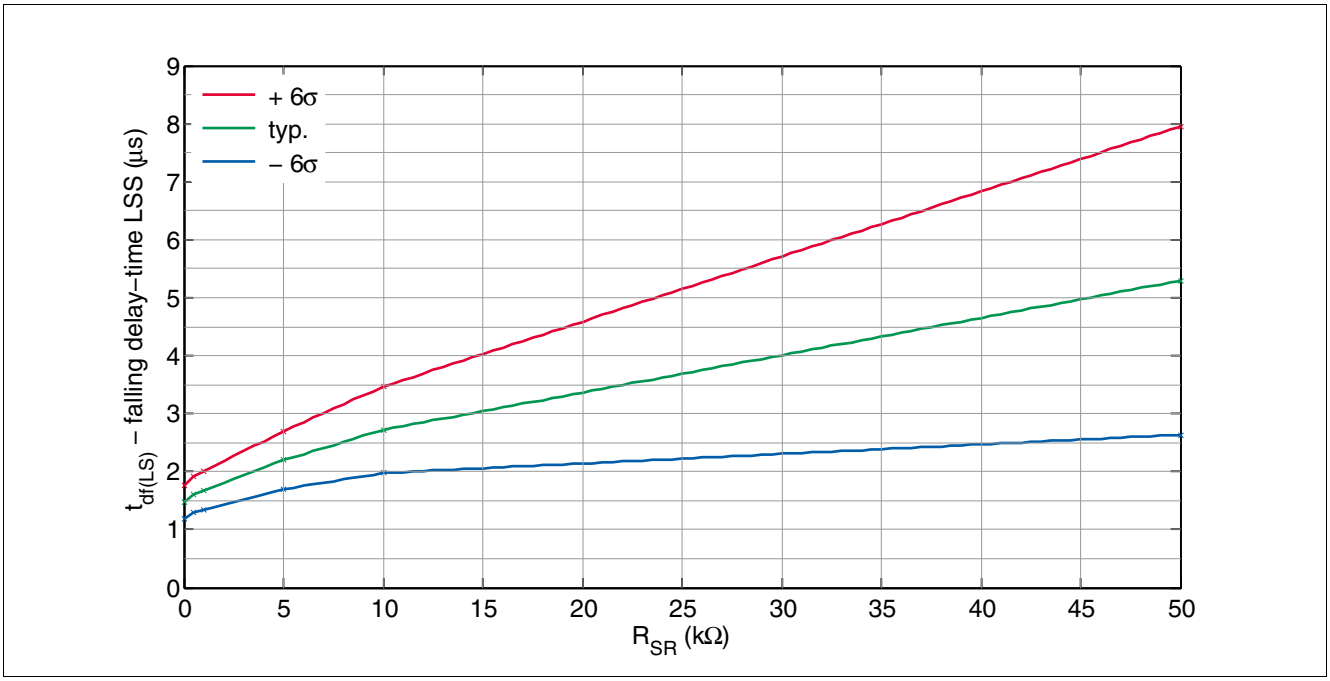

Figure 48 Dependency of the slew rate resistor R_{SR} on the falling delay time of the low side switch $t_{df(LS)}$: BTN8962TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

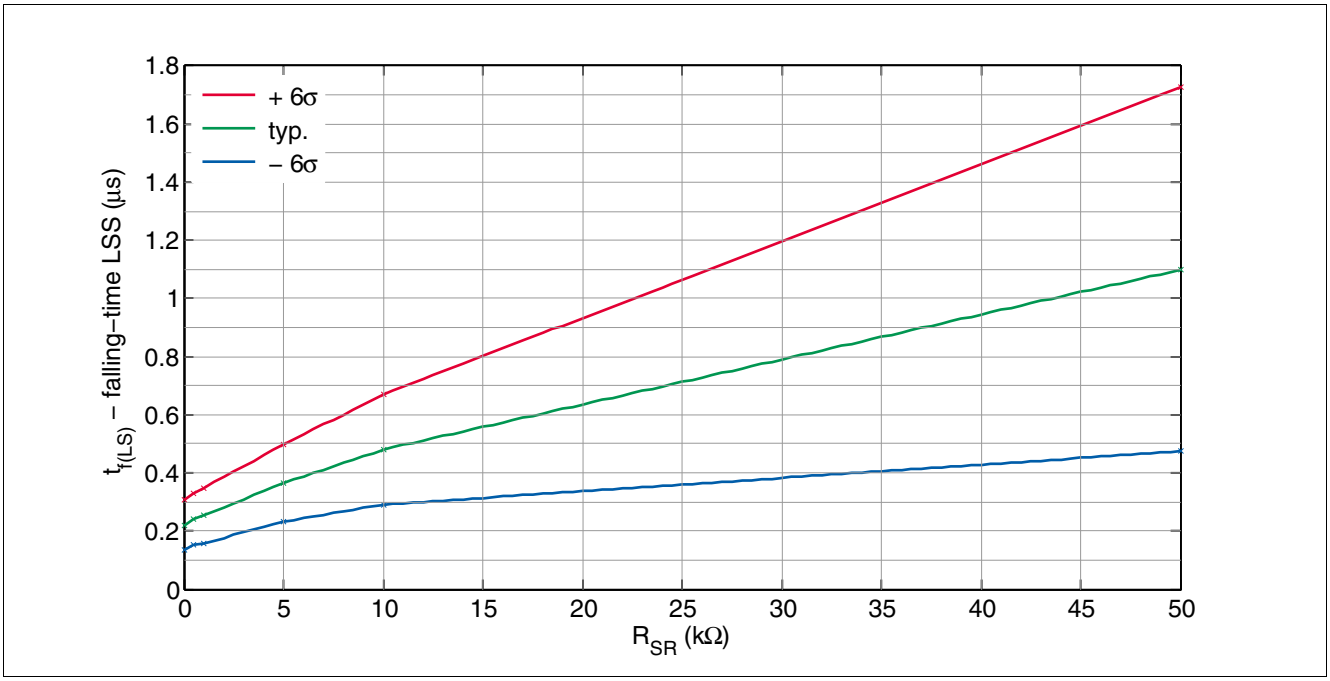

Figure 49 Dependency of the slew rate resistor R_{SR} on the falling time of the low side switch $t_{f(LS)}$: BTN8962TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

6.4.2 BTN8982TA

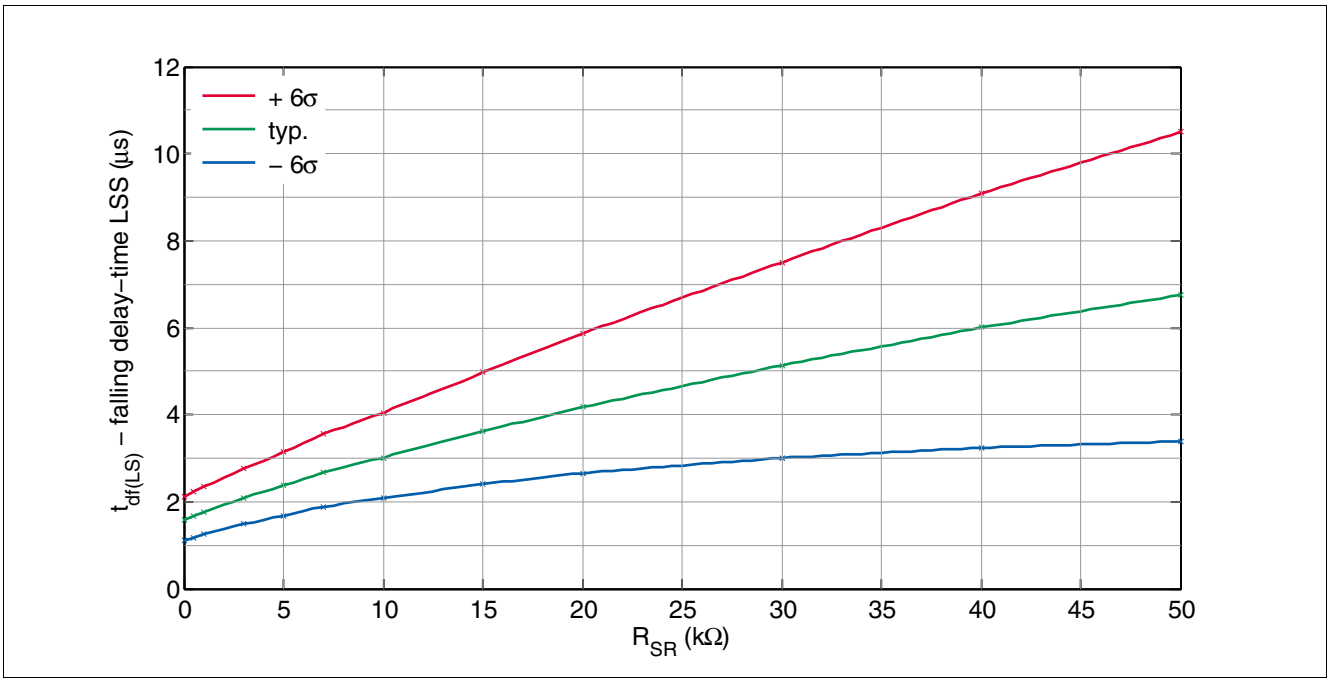

Figure 50 Dependency of the slew rate resistor R_{SR} on the falling delay time of the low side switch $t_{df(LS)}$: BTN8982TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

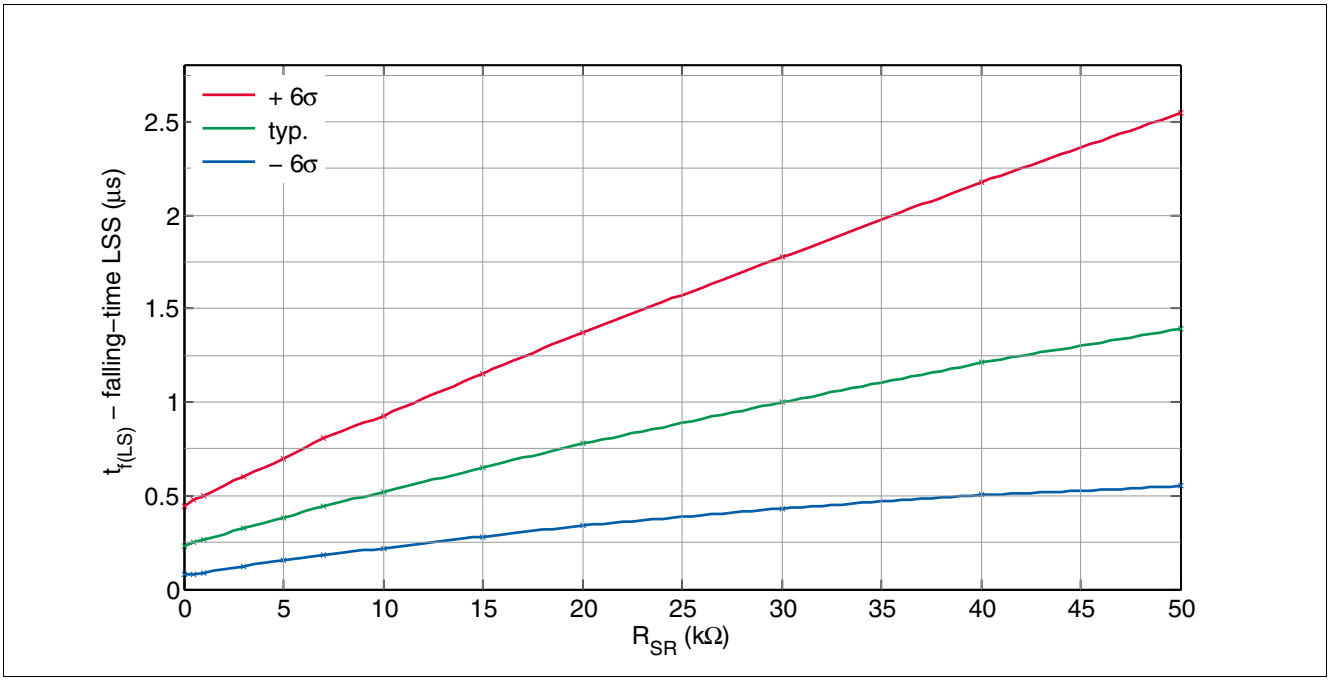

Figure 51 Dependency of the slew rate resistor R_{SR} on the falling time of the low side switch $t_{f(LS)}$: BTN8982TA (V_S = 13,5 V, R_{load} = 2 Ω, 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

6.5 Error of total delay time

The resulting relative error for the ±6σ values, compared to the typical $t_{x(HS),total}$ value, is summarized in **Figure 52** (BTN8962TA) / **Figure 53** (BTN8982TA). The error is calculated as follows:

$$rel.error = \frac{t_{x(HS),min/max} - t_{x(HS),typ}}{t_{x(HS),typ}} \quad (6.3)$$

This parameter spread needs to be taken into account especially for short PWM cycle times, respectively high PWM frequencies. If the relative $t_{r(HS),total}$ / $t_{f(HS),total}$ error is in the same order of magnitude as the application's PWM cycle time, a separate calibration can be considered to measure the delay times of the individual BTx9yz devices.

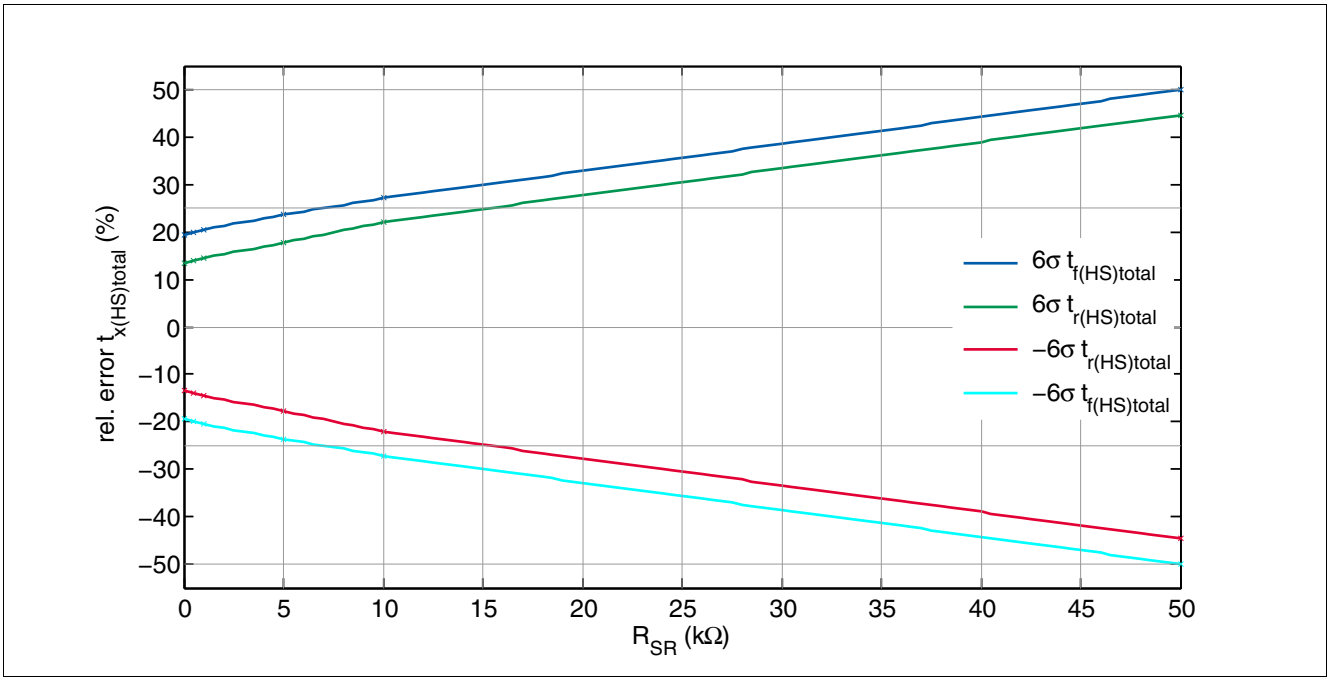

Figure 52 Relative error of the total delay time $t_{r(HS),total}$ for rising and $t_{f(HS),total}$ for falling edges. Relative error according to Equation (6.3) for BTN8962TA (V_S = 13,5 V, R_{load} = 2 Ω 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

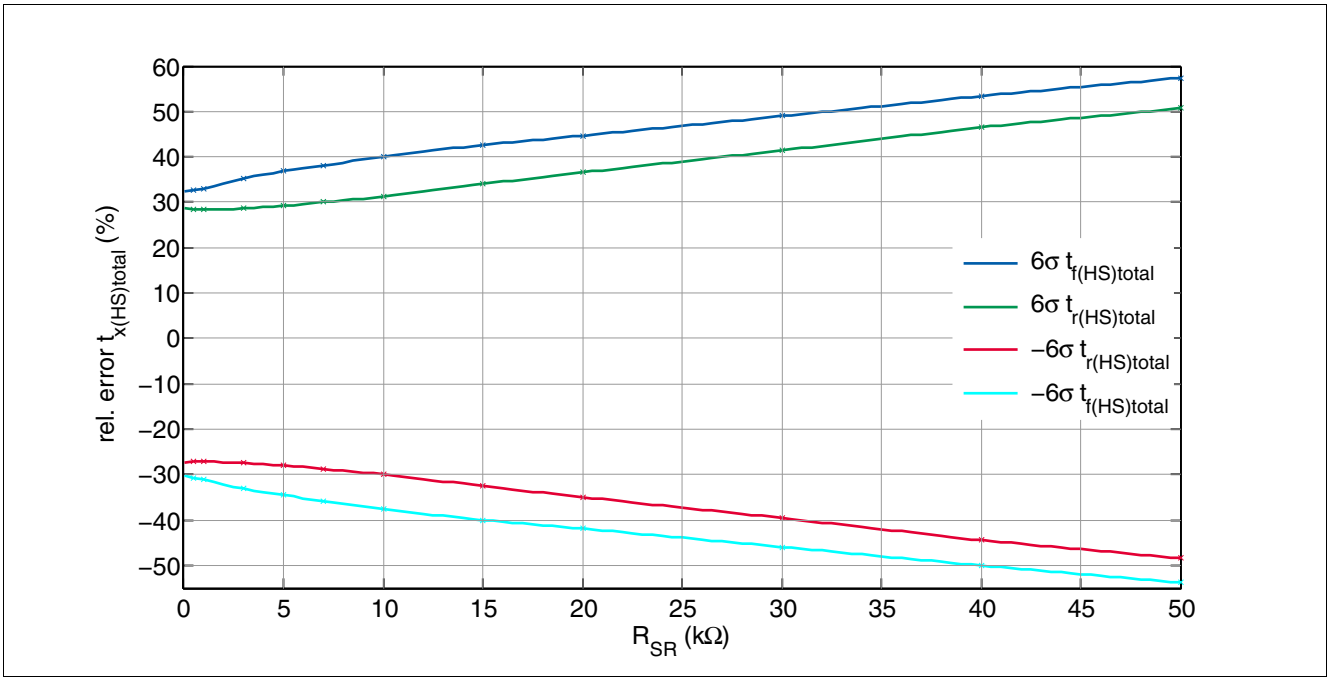

Figure 53 Relative error of the total delay time $t_{r(HS),total}$ for rising and $t_{f(HS),total}$ for falling edges. Relative error according to Equation (6.3) for BTN8982TA (V_S = 13,5 V, R_{load} = 2 Ω 30 µH < L_{load} < 40 µH (in series to R_{load}), single pulse)

6.6 Delay time calibration

One possibility to determine the total rising time $t_{r(HS),total}$ and the falling time $t_{f(HS),total}$ respectively, is by measuring the time once in an end of line test. For such a (single) measurement, the influence of certain parameters like the supply voltage or the load current has to be considered as well and the test setup has to be adjusted accordingly.

It is also possible to use continuous calibration during operation. With such a method, the influence of changing outside parameters is constantly taken into account.

In the following two chapters, an output voltage (**Chapter 6.6.1**) and current sense based calibration (**Chapter 6.6.2**) is suggested.

6.6.1 Output voltage based calibration

This method can be implemented if both the supply voltage V_S and the BTN8960 /62 /80 /82's output voltage V_{OUT} at the OUT-pin are measured. In that case it would be possible to measure the time between setting the IN input pin from low to high (or from high to low for $t_{f(HS),total}$) and the point of time, the output voltage V_{OUT} is greater than or equal to 0,8 V_S. The measurement procedure is illustrated in **Figure 54**.

The procedure for the total falling delay time $t_{f(HS),total}$ measurement can be performed in a similar fashion: the delay time between the falling edge of the IN-pin and the lower deviation of 20 % of the $V_{OUT} \approx V_S$ voltage level is considered.

If these two voltage levels are monitored during operation, an online calibration can be performed periodically, too.

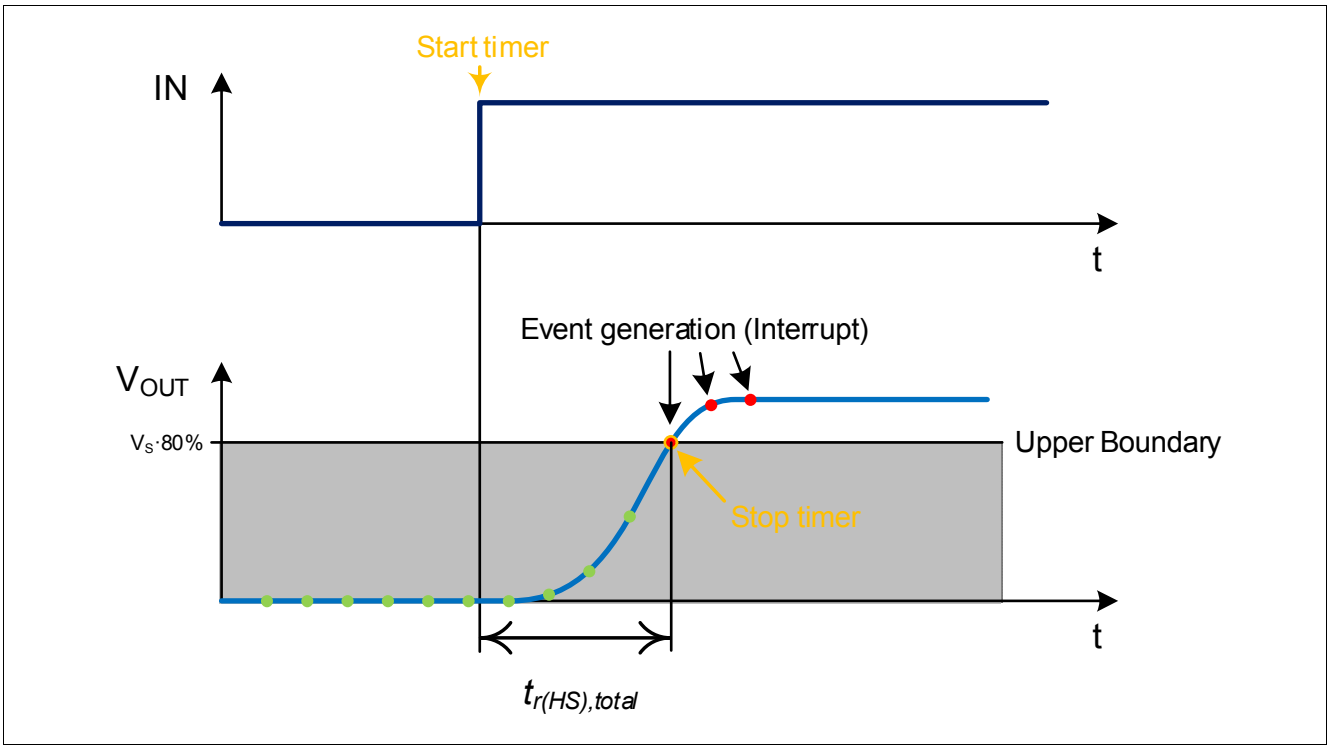

Figure 54 Measurement procedure for the total rising time $t_{r(HS),total}$ based on two voltage measurements

6.6.2 Current sense based calibration

Two different calibration methods are available when only the current sense signal is monitored. One of these can be implemented as an end of line test, while the other is performed during live operation.

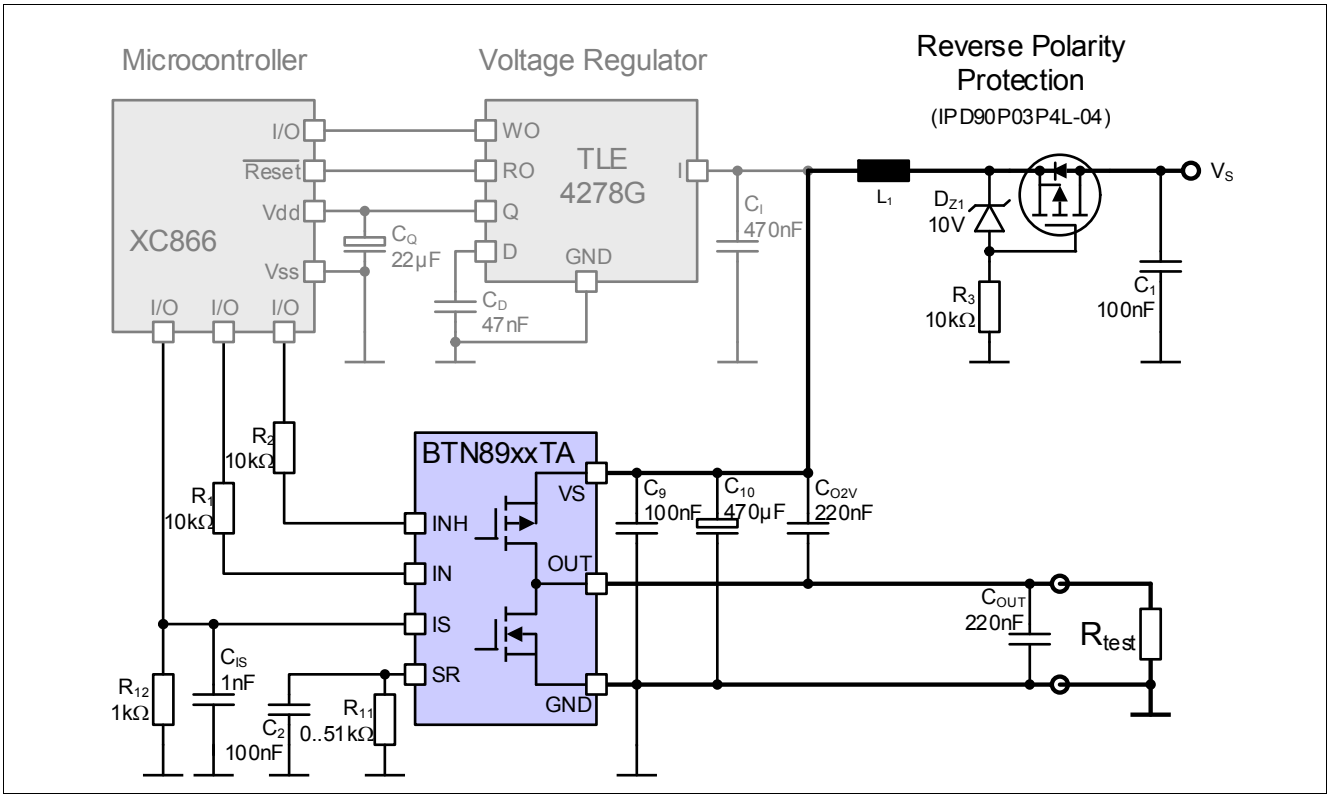

Figure 55 End of line test setup for timing calibration with ohmic load R_{test}

To determine the delay for a rising edge $t_{r(HS),total}$, the voltage limit is set to the corresponding current level, which is reached with a voltage drop of 80 % of $V_{OUT} \approx V_S$ over the test resistor R_{test}, as shown in the test setup in **Figure 55**. As this test is based on the concurrency of the output voltage and current I_L, only an ohmic load should be used. This setup results in the direct proportional context of $I_L = V_S/R_{test}$ and with the current sense function from **Figure 5.5**:

(6.4)

$$I_{IS} = \frac{I_L}{dk_{ILIS}} + I_{IS(offset)} = \frac{V_s}{dk_{ILIS} \cdot R_{test}} + I_{IS(offset)}$$

The resulting voltage V_{ADC} on the microcontroller's ADC input pin (according to **Figure 55**):

(6.5)

$$V_{ADC} = R_{12} \cdot I_{IS} = \frac{V_s \cdot R_{12}}{dk_{ILIS} \cdot R_{test}} + I_{IS(offset)} \cdot R_{12}$$

This means that the comparator threshold should be set to a corresponding voltage level of:

(6.6)

$$V_{ADC,80\%V_s} = 0,8 \cdot \left(\frac{V_s \cdot R_{12}}{dk_{ILIS} \cdot R_{test}} + I_{IS(offset)} \cdot R_{12} \right)$$

This procedure allows to measure the input delay $t_{r(HS),total}$ with a microcontroller's ADC in a predefined end of line test, with a known resistor R_{test}. The test is summarized in **Figure 56**. The time measurement is started in parallel to the rising edge of the IN input pin. If the voltage level of V_{ADC}, as described in **Equation (6.6)**, is reached, the resulting delay time $t_{r(HS),total}$ can be calculated.

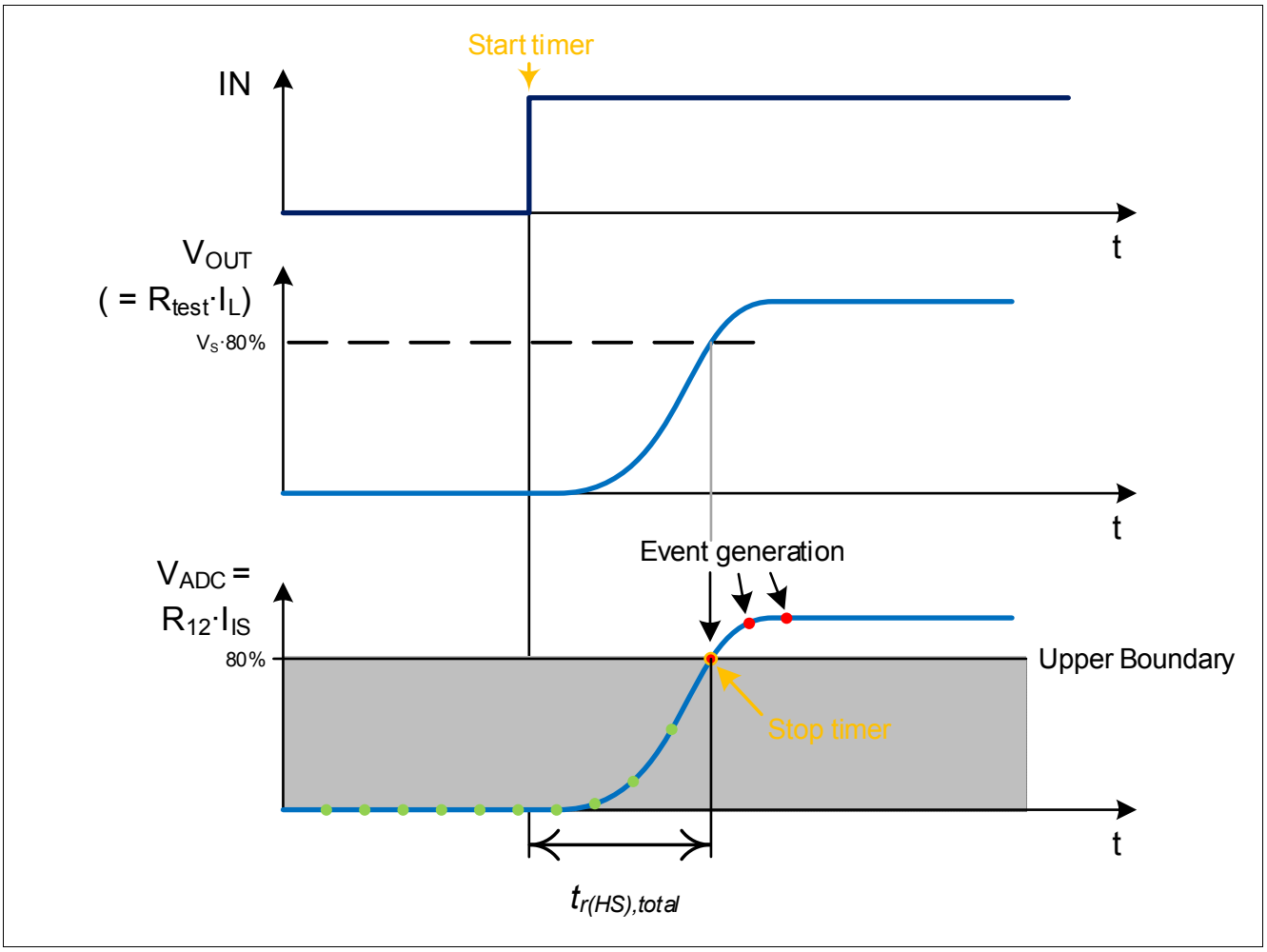

Figure 56 Measurement procedure for the total rising time $t_{r(HS),total}$ based on a current sense measurement

This procedure, which is described here for a rising edge, can be implemented in a similar manner to measure the total delay for a falling edge, $t_{f(HS),total}$, on the IN-pin, too.

6.7 ADC Timing for current measurement

One way to measure the current value for motor control applications is in the center of the PWM duty cycle. The corresponding measuring time frame is summarized in **Figure 57**. Based on the value of resistor R_{SR}, the time frame is limited by the worst case (min./max.) switching times, $t_{f(HS),total,min}$ and $t_{r(HS),total,max}$. Alternatively, the timing could be based on the delay time calibration/measurement described in the previous **Chapter 6.6**.

6.7.1 Current sense ADC timing

Based on **Figure 57**, the time window for an ADC measurement $t_{h(HS),meas}$ for a high output signal can be calculated as follows:

(6.7)

$$t_{h(HS),meas} = T_{ON} + t_{df(HS),min} - t_{r(HS),total,max}$$

As previously described, the on-time T_{ON} is based on the following relationship:

(6.8)

$$T_{ON} = T_{PWM} \cdot DC$$

T_{PWM} is the PWM-period-time (T_{PWM} = 1 / f_{PWM}) and DC corresponds to the duty cycle. This results in:

(6.9)

$$t_{h(HS),meas} = T_{PWM} \cdot DC + t_{df(HS),min} - t_{r(HS),total,max}$$

If the measurement should be started in the center of the ADC time window $t_{h(HS),meas}$, the sample delay t_{sample} has to be set to the following:

(6.10)

$$t_{sample} = t_{r(HS),total,max} + \frac{t_{h(HS),meas}}{2}$$

If the ADC measurement time window should be placed right in the center of $t_{h(HS),meas}$ for a given ADC conversion time t_{ADC}, the sample delay time t_{sample} can be calculated as follows:

(6.11)

$$t_{sample} = t_{r(HS),total,max} + \frac{t_{h(HS),meas} - t_{ADC}}{2}$$

This measurement scenario is illustrated in **Figure 57**.

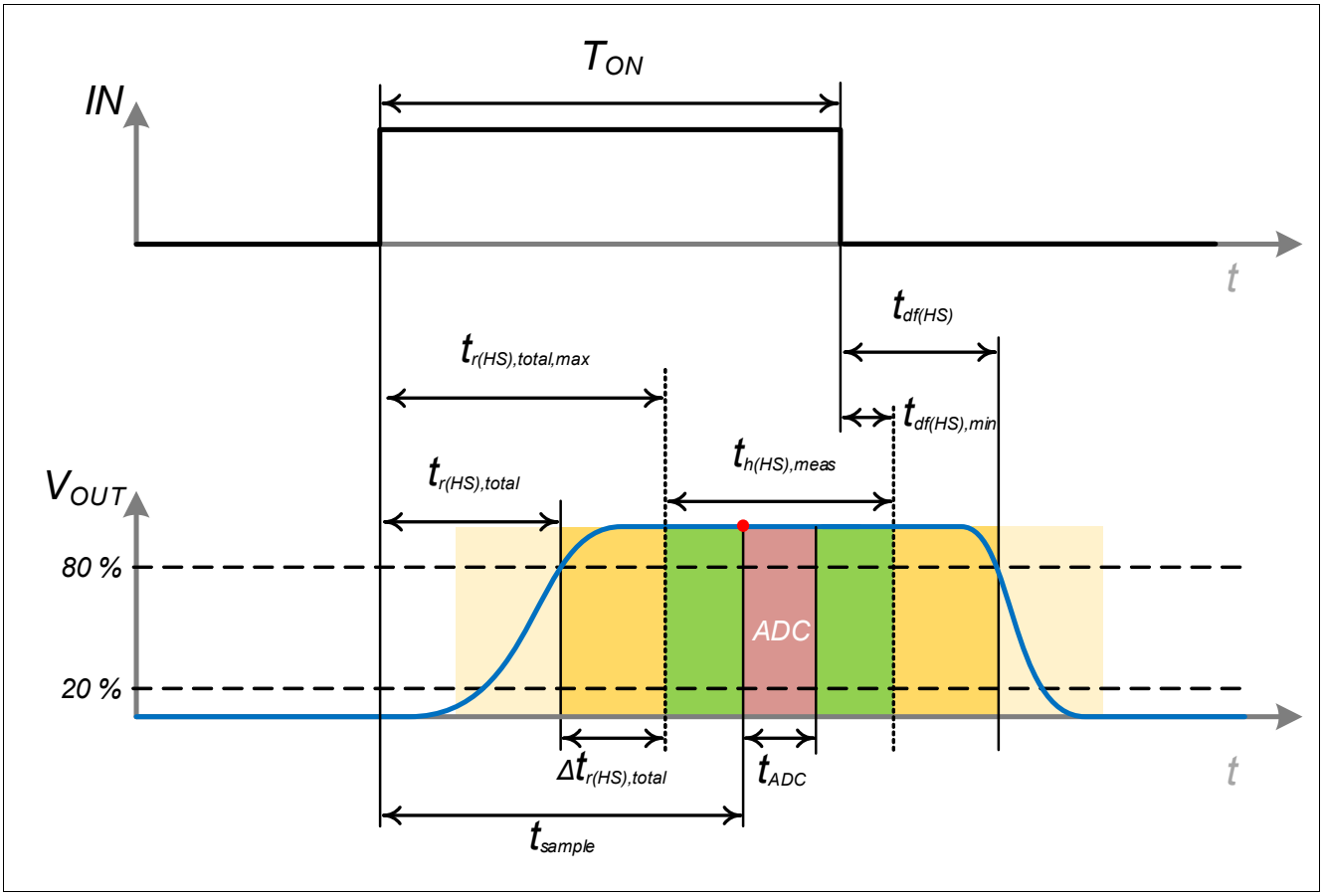

Figure 57 Timing for current measurement for high input on IN-pin, with ideal ADC sampling time window

6.7.2 Offset current calibration ADC timing

With an additional ADC measurement at low input signals, an online compensation of the IS-pin's offset current $I_{IS(offset)}$ can be executed. Based on **Figure 58** and comparable to the current measurement in the previous **Chapter 6.7.1**, the different sampling timings for a low input level can be calculated in a similar fashion. The time window of the ADC measurement $t_{f(HS),meas}$ for a low output signal can be calculated as follows:

(6.12)

$$t_{f(HS),meas} = T_{PWM} \cdot (1 - DC) + t_{dr(HS),min} - t_{f(HS),total,max}$$

If the ADC measurement should be triggered right in the center of the time window $t_{h(HS),meas}$, the required sample delay t'_{sample} can be calculated according to **Figure 58**:

(6.13)

$$t'_{sample} = t_{f(HS),total,max} + \frac{t_{f(HS),meas}}{2}$$

The resulting trigger point with the sample delay time t'_{sample} is marked in **Figure 58** (red).

If the ADC sampling window should be placed in the center of $t_{h(HS),meas}$, the sample delay time t'_{sample} should be set to:

(6.14)

$$t'_{sample} = t_{f(HS),total,max} + \frac{t_{l(HS),meas} - t_{ADC}}{2}$$

In the case of a fault condition, the IS-pin will provide a constant current of $I_{IS(lim)}$, instead of the current sense functionality. This current $I_{IS(lim)}$ can be clearly distinguished from the lower offset current $I_{IS(offset)}$. Further details are described in **Chapter 5.5.1.1**.

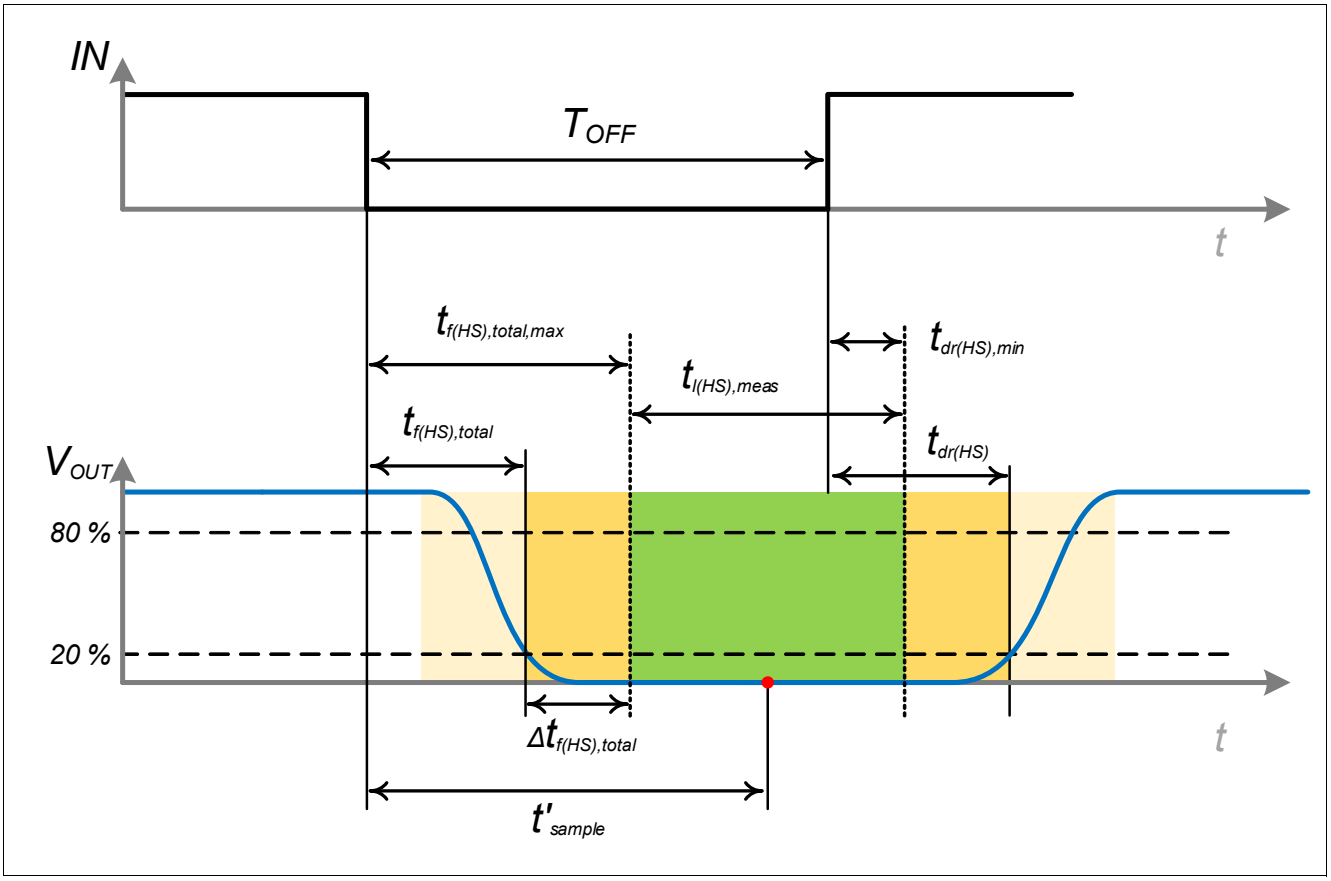

Figure 58 Timing for current measurement for low input on IN-pin

6.8 Allowed PWM setup for current sense ADC measurements

Based on the previous **Chapter 6.7**, a relationship between the lowest possible duty cycle DC_{min}, corresponding to the minimal time $T_{ON,min}$, and the PWM frequency can be set up. The worst case (max.) ADC conversion time window is $t_{ADC,max}$. For a worst case analysis, the following assumption must be respected in any case, as the time window for the ADC measurement $t_{h(HS),meas}$, according to **Equation (6.9)**, has to be greater than $t_{ADC,max}$:

(6.15)

$$t_{ADC,max} \leq T_{PWM} \cdot DC + t_{df(HS),min} - t_{r(HS),total,max}$$

For certain typical values for resistor R_{SR} (1 kΩ 5 kΩ 10 kΩ) and certain maximal ADC conversion times $t_{ADC,max}$, the minimal duty cycles should be respected, as shown in **Figure 59** (BTN8962TA) / **Figure 62** (BTN8982TA) for

R_{SR} = 1 kΩ, **Figure 60** (BTN8962TA) / **Figure 63** (BTN8982TA) for R_{SR} = 5 kΩ and **Figure 61** (BTN8962TA) / **Figure 64** (BTN8982TA) for R_{SR} = 10 kΩ.

6.8.1 BTN8962TA

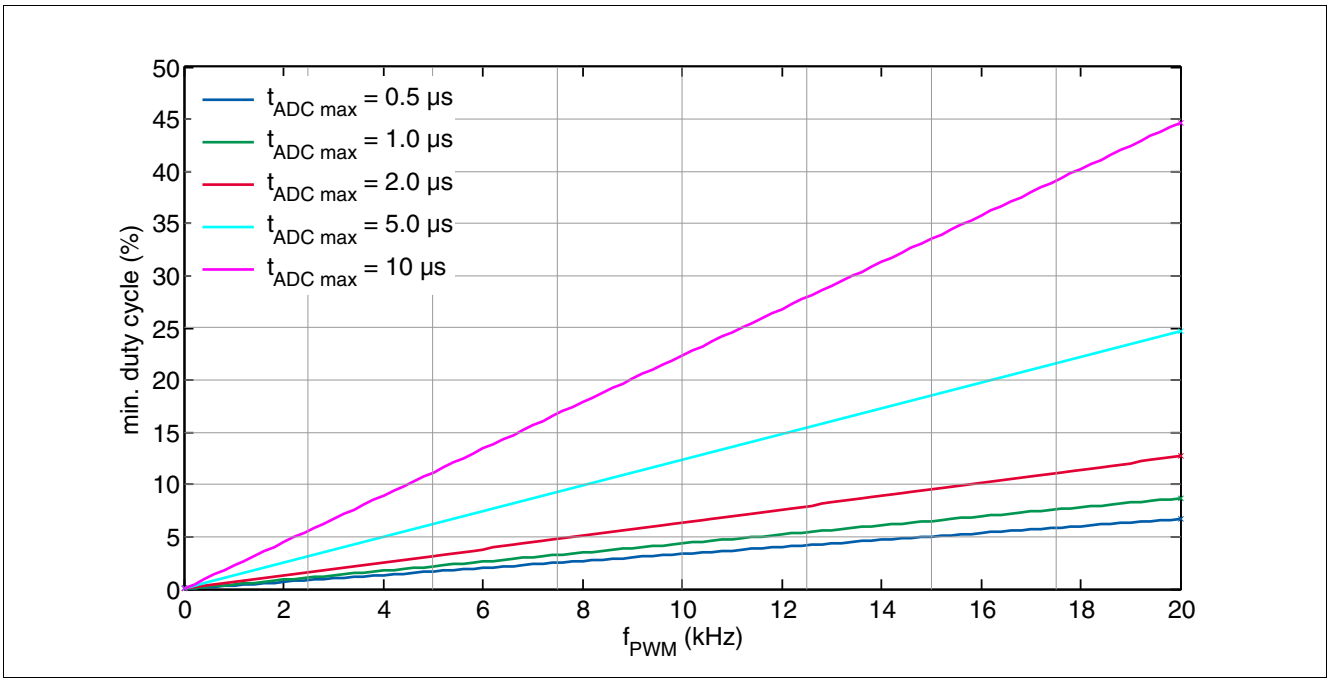

Figure 59 Minimal allowed duty cycle DC_{min} for a given PWM frequency f_{PWM}, a ADC conversion time t_{ADC} and R_{SR} = 1 kΩ, for BTN8962TA

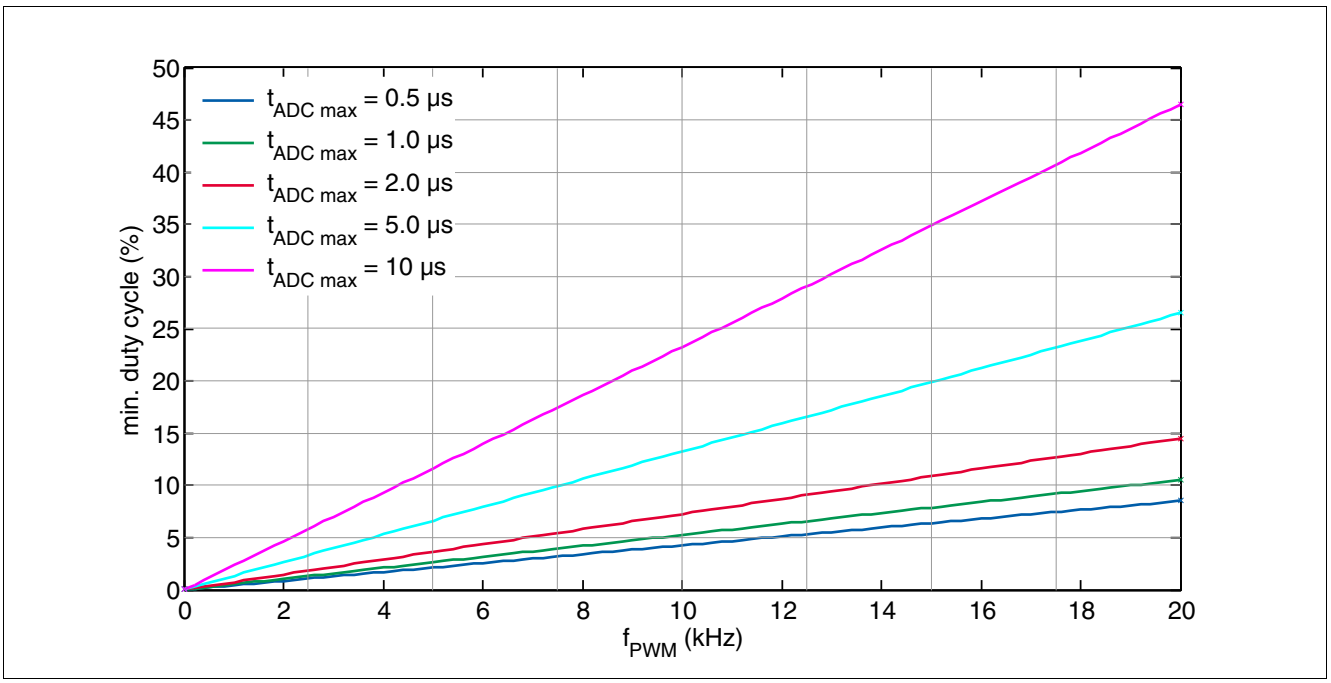

Figure 60 Minimal allowed duty cycle DC_{min} for a given PWM frequency f_{PWM}, a ADC conversion time t_{ADC} and R_{SR} = 5 kΩ, for BTN8962TA

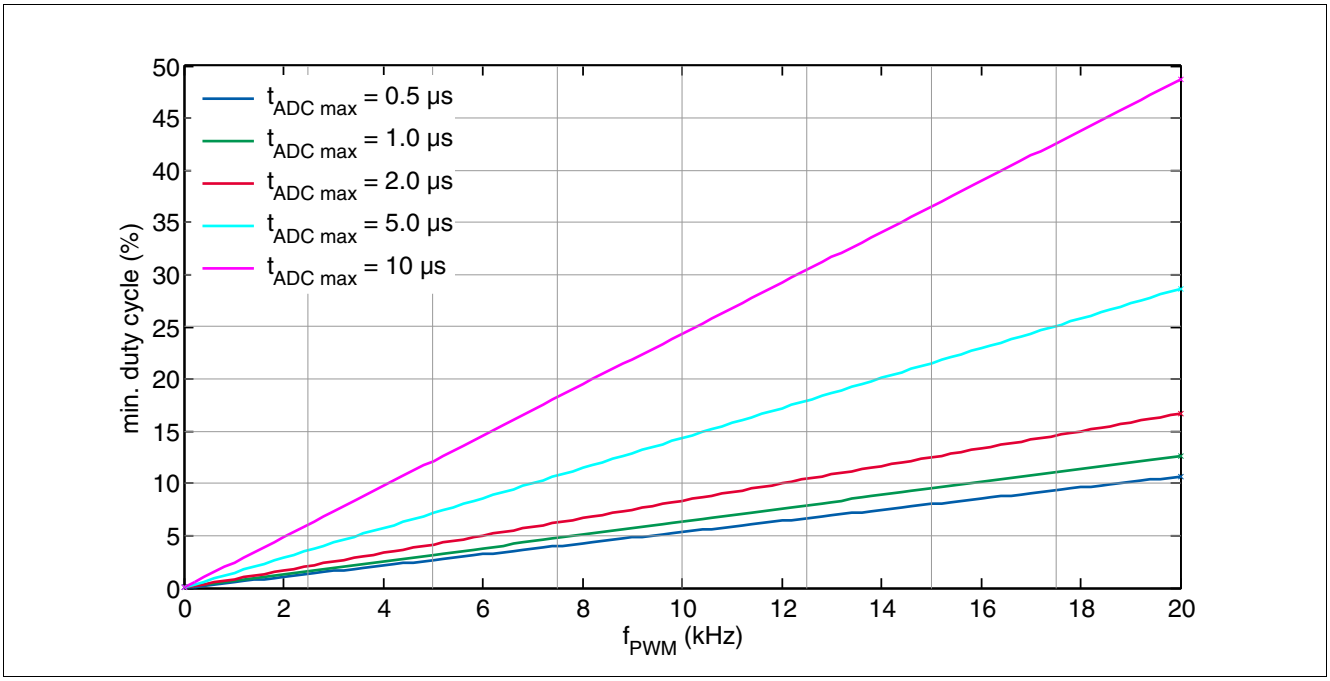

Figure 61 Minimal allowed duty cycle DC_{min} for a given PWM frequency f_{PWM}, a ADC conversion time t_{ADC} and R_{SR} = 10 kΩ, for BTN8962TA

6.8.2 BTN8982TA

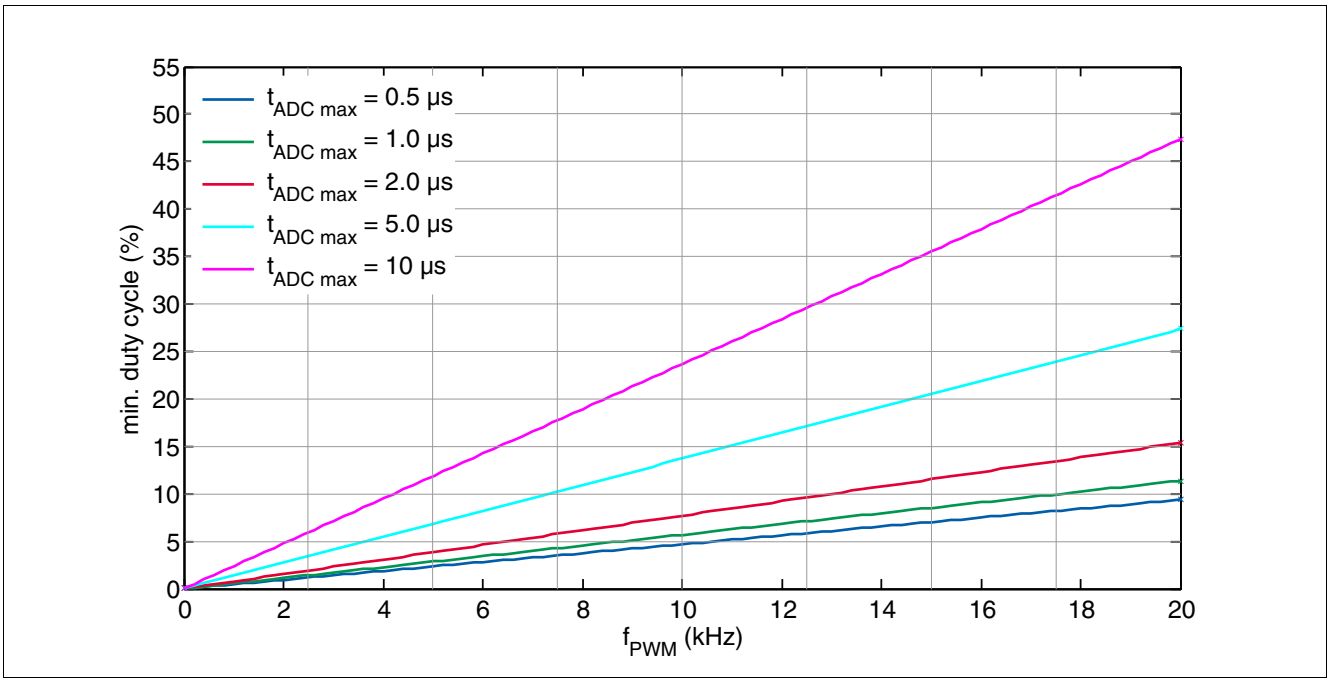

Figure 62 Minimal allowed duty cycle DC_{min} for a given PWM frequency f_{PWM}, a ADC conversion time t_{ADC} and R_{SR} = 1 kΩ, for BTN8982TA

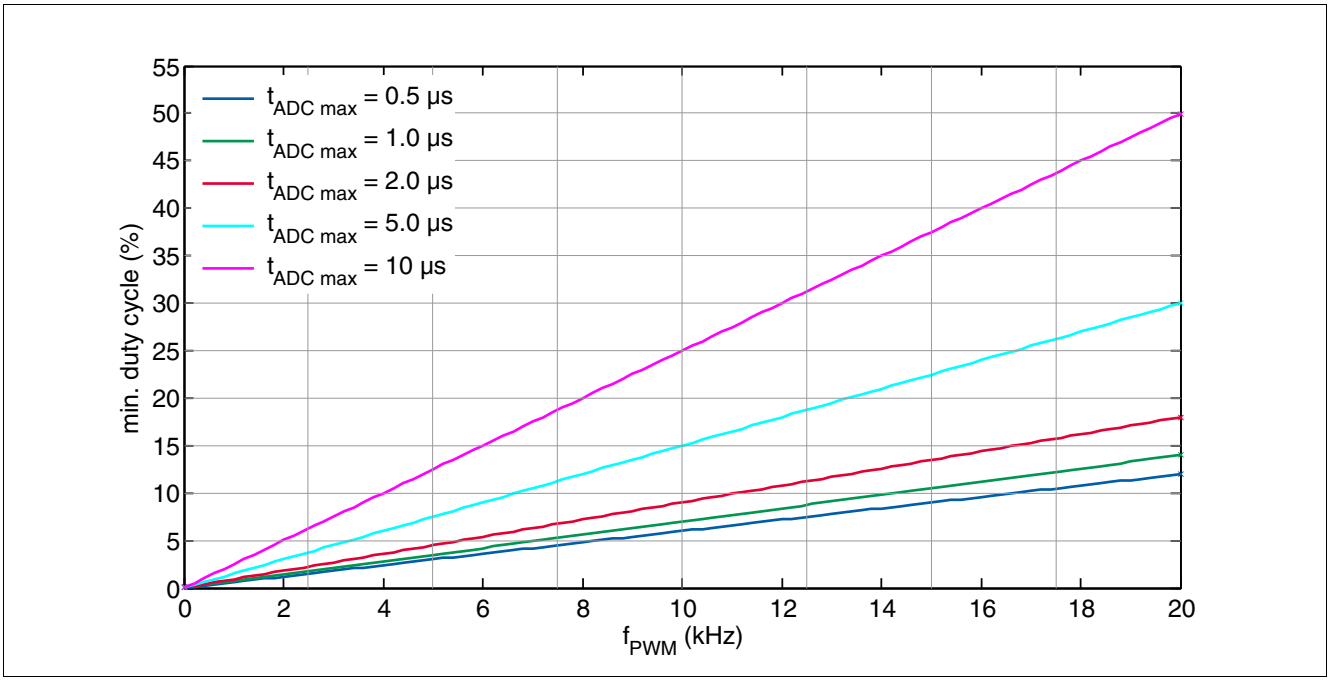

Figure 63 Minimal allowed duty cycle DC_{min} for a given PWM frequency f_{PWM}, a ADC conversion time t_{ADC} and R_{SR} = 5 kΩ, for BTN8982TA

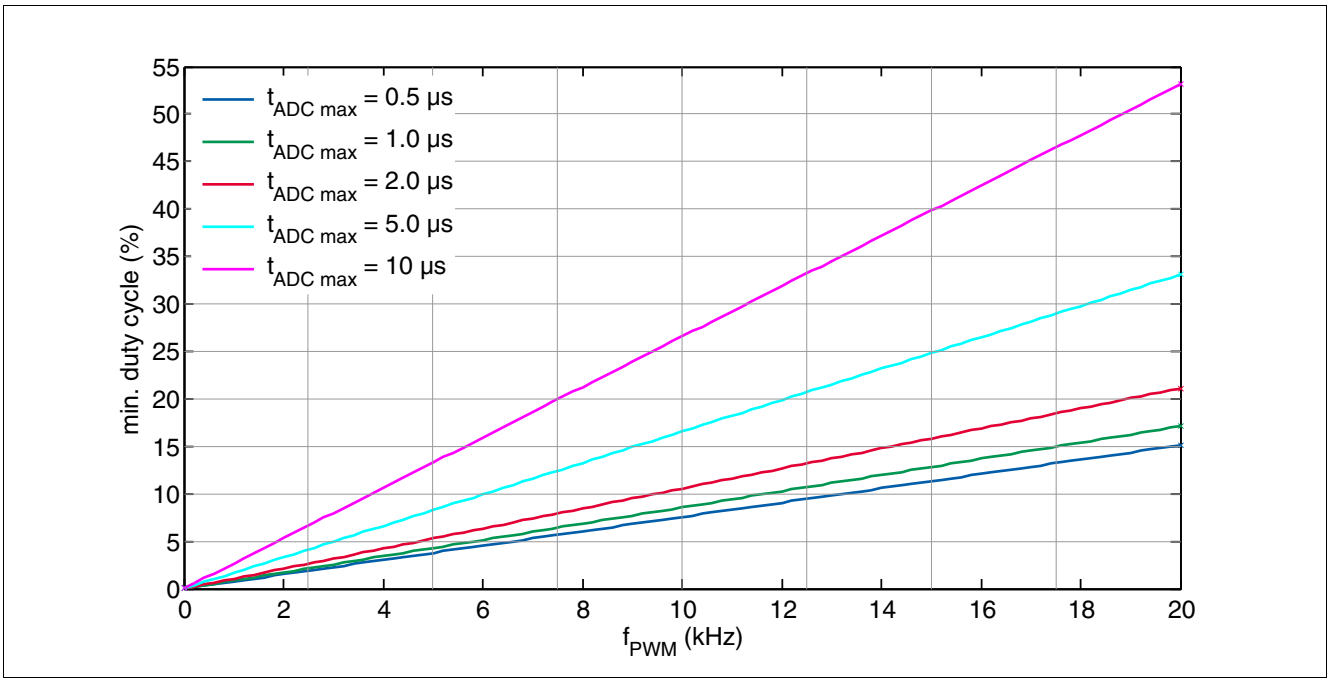

Figure 64 Minimal allowed duty cycle DC_{min} for a given PWM frequency f_{PWM}, a ADC conversion time t_{ADC} and R_{SR} = 10 kΩ, for BTN8982TA

6.8.3 Example calculation

For an example application with the BTN8962TA ,the following parameter values are assumed:

- PWM frequency f_{PWM}= 20 kHz, resulting in T_{PWM}= 1 / f_{PWM} = 50µs
- DC_{min}= 25 %
- R_{SR} = 1 kΩ resulting in $t_{df(HS),min}$ = 1,971 µs and $t_{r(HS),total,max}$ = 4,321 µs

This setup results in the max. ADC conversion time window $t_{ADC,max}$:

(6.16)

$$t_{ADC,max} = T_{PWM} \cdot DC + t_{df(HS),min} - t_{r(HS),total,max}$$

(6.17)

$$t_{ADC,max} = 50\mu s \cdot 0,25 + 1,971\mu s - 4,321\mu s \approx 10,2\mu s$$

7 Power dissipation

The device dissipates some power. This power dissipation is generated in the top chip and in the individual MOSFETs. The high currents in the MOSFETs generate most of the power dissipation. The following consideration is based on several assumptions, so the result is ultimately an estimation which should help you understand the general trend.

The power dissipation in the MOSFETs consists mainly of conducted losses and switching losses. Losses in the body diode only occur during the cross current protection phase. They are therefore not taken into consideration.

7.1 Power dissipation of the control chip (top chip)

The control chip consumes a certain amount of current, and this causes power dissipation.

In DC-mode the following equation describes the power dissipation in the control chip:

(7.1)

$$P_{CC-DC} = (I_{Vs(ON)} + I_{IS}) \cdot V_S$$

In PWM-mode, an additional current is needed to charge/discharge the MOSFET gates. This leads to the following PWM power dissipation:

(7.2)

$$P_{CC-PWM} = Q_{tot} \cdot V_S \cdot f_{PWM}$$

The gate charges for the BTN89xx are specified in the table below:

Table 2 Q_{tot} of BTN896x and BTN898x

Product	Total gate charge
BTN8960 /62	450 nC
BTN8980 /82	550 nC

Power dissipation in the control chip can be calculated as follows:

(7.3)

$$P_{CC} = P_{CC-DC} + P_{CC-PWM} = (I_{Vs(ON)} + I_{IS}) \cdot V_S + Q_{tot} \cdot V_S \cdot f_{PWM}$$

7.2 Conduction power dissipation

In the ON-state, a MOSFET has a specific R_{ON} which is listed in the data sheet. R_{ON} is different for the high side (HS) and the low side (LS) MOSFETs. This means that R_{ON} must be selected according to the driving situation. A current flowing through this transistor generates the following conducted losses:

(7.4)

$$P_{CL} = I^2 \cdot R_{ON}$$

In case the NovalithIC™ is driven in a static condition, **Equation (7.4)** can be used to estimate the static conducted losses for the high side or low side MOSFET.

7.3 Power dissipation due to switching

With PWM control, switching losses need to be taken into account because they generate most of the power dissipation for high PWM frequencies. The NovalithIC™ devices are designed to drive motors or other inductive loads. This chapter deals with switching losses that are generated while driving an inductive load.

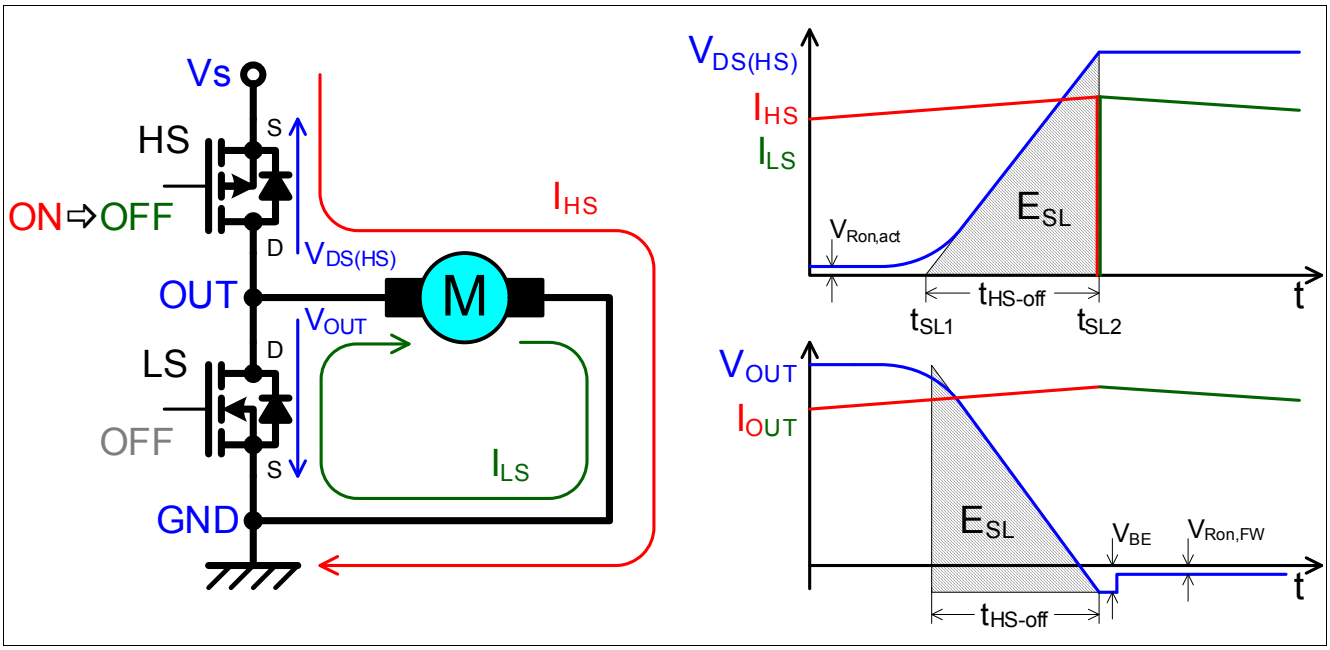

Figure 65 High Side switching scenario of BTN8960 /62 /80 /82

The current in an inductor cannot be changed abruptly (rule of Lenz). As shown in **Figure 65**, the current in the high side (HS) MOSFET is driven by the motor inductance as long as the OUT voltage drops one V_{BE} below GND and the current is flowing through the body diode of the low side (LS) MOSFET. This means that the current I_{HS} is flowing in the high side (HS) MOSFET, even though this is in linear mode during $t_{HS\text{-}off}$.

The NovalithIC™ has a cross-current protection mechanism which ensures that an output MOSFET is turned on only when the other one is off. This causes a free wheeling current through the MOSFET body diode (V_{BE} in **Figure 65**) before the resistive path is switched on. The power dissipation caused by the body diode is negligible and thus not taken into account in this estimation.

The rise- and fall- time in the data sheet is the period during which the output voltage decreases from 80% to 20%. In order to determine the switching losses, we need to determine the time required to decrease the output voltage from 100% to 0%. The $t_{HS\text{-}off}$ can be estimated from the data sheet parameters with the **Equation (7.5)** accordingly.

(7.5)

$$t_{HS-off} = \frac{t_{f(HS)}}{0.5}$$

Factor 0.5 is related to ΔV_{OUT} from 0% to 100%

For the other switching times ($t_{HS\text{-}on}$, $t_{LS\text{-}off}$ and $t_{LS\text{-}on}$) **Equation (7.5)** can be used to perform the same calculation using the corresponding data sheet parameters ($t_{r(HS)}$, $t_{f(LS)}$ and $t_{r(LS)}$).

Other assumptions, with a minor effect on the result, include the following:

- The load current during the switching process is constant.
- V_{OUT} and $V_{DS(HS)}$ have linear behaviour.

- The switching times are assumed as equal and in the following always referred to as $t_{HS\text{-}off}$.

The switching energy E_{SL} is shown in **Figure 65** and can be estimated using **Equation (7.6)** below:

(7.6)

$$E_{SL} = \int_{t_{SL\,1}}^{t_{SL\,2}} V_S \cdot I_{OUT} \cdot dt = \frac{V_S \cdot I_{OUT}}{2} \cdot t_{HS-off}$$

From the switching energy E_{SL} the average power loss P_{SL} can be determined with two switching times per PWM period. This is shown in **Equation (7.7)**:

(7.7)

$$\overline{P_{SL}} = \frac{V_S \cdot I_{OUT}}{2} \cdot 2 \cdot t_{HS-off} \cdot f_{PWM} = V_S \cdot I_{OUT} \cdot t_{HS-off} \cdot f_{PWM}$$

7.4 Entire power dissipation of the MOSFETs

The average power dissipation in PWM-mode consists of the switching losses plus the conducted losses, as shown in **Figure 66**. We must take into account that the losses occur in the high side (HS) and low side (LS) MOSFET. In the example of **Figure 65**, where the motor is connected to GND, the switching losses occur in the high side (HS) MOSFET. The conducted losses occur in the high side (HS) MOSFET during the ON-phase and in the low side (LS) MOSFET in the free wheeling phase, as shown in **Figure 66**.

In PWM-mode, the PWM-period-time is:

(7.8)

$$T_{PWM} = \frac{1}{f_{PWM}}$$

The duty cycle (DC) of the PWM-mode is the relation between the ON-time and the PWM-period-time in percent.

(7.9)

$$DC = \frac{T_{ON}}{T_{PWM}}$$

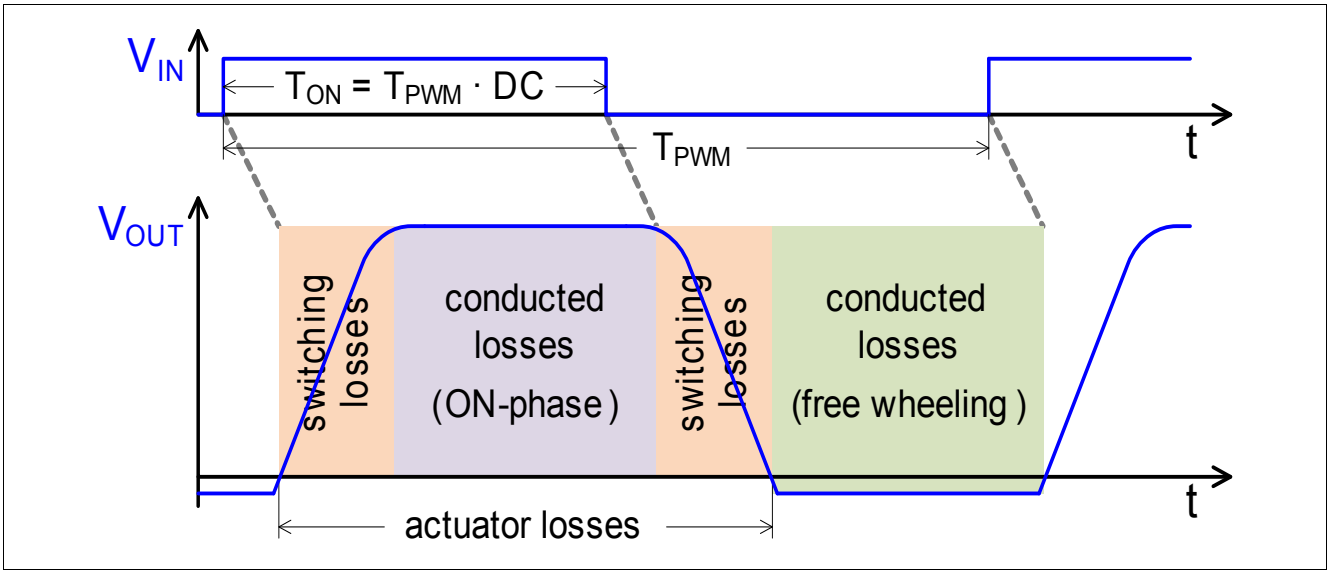

Figure 66 Entire power dissipation of BTN8960 /62 /80 /82 with the motor connected to GND

In **Chapter 7.4.2** and **Chapter 7.4.3** the power dissipation is estimated separately for the high side (HS) and low side (LS) MOSFET.

7.4.1 PWM control and the duty cycle constraints

If t_{FW} is close to or below zero, no freewheeling occurs. V_{OUT} does not go below GND. This means that only switching losses are generated. Thus, a duty cycle generating $t_{FW} \leq 0$ is insufficient to control the motor current and therefore not taken into account in the following calculations. In this case, the high side (HS) MOSFET should be permanently on.

The same is valid for $t_{ON} \leq 0$. In this case, the low side (LS) MOSFET should be permanently on.

Extremely low or high duty cycle values required by real applications can be achieved by increasing the switching speed and/or by increasing T_{PWM}.

7.4.2 Entire power dissipation in the actuator MOSFET

In the motor-to-GND scenario the actuator MOSFET is the high side (HS) MOSFET, as in **Figure 65** and in motor-to-V_s scenario, the actuator MOSFET is the low side (LS) MOSFET. The entire power dissipation consists of two times the switching losses plus the cunducted losses in the ON-phase, as shown in **Figure 66**. The time of the ON-phase in PWM-mode is provided by the following formulae:

(7.10)

$$t_{ON} = T_{ON} - t_{HS-on}$$

As mentioned in "**Other assumptions,**" on **Page 65** switching times are assumed as equal and named as t_{HS-off}:

(7.11)

$$t_{ON} = T_{ON} - t_{HS-off}$$

Equation for estimate the total conducted energy in the actuator MOSFET:

(7.12)

$$E_{act} = 2 \cdot E_{SL} + E_{ON} = V_S \cdot I_{OUT} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON,act} \cdot t_{ON}$$

From **Equation (7.12)** the average power dissipation in the actuator MOSFET can be determined by multiplying **Equation (7.12)** by f_{PWM}:

(7.13)

$$\overline{P_{act}} = E_{act} \cdot f_{PWM} = (V_S \cdot I_{OUT} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON,act} \cdot t_{ON}) \cdot f_{PWM}$$

Equation (7.13) is an estimation of the average power dissipation in the actuator MOSFET. In **Figure 65**, this is the high side (HS) MOSFET.

7.4.3 Entire power dissipation in the freewheeling MOSFET

In the motor-to-GND scenario , the freewheeling MOSFET is the low side (LS) MOSFET, as in **Figure 65**, and in the motor-to-V_s scenario, the freewheeling MOSFET is the high side (HS) MOSFET. The entire power dissipation consists of the conducted losses in the freewheeling phase, as shown in **Figure 66**. The duration of the freewheeling phase in PWM-mode is provided by the equation below:

(7.14)

$$t_{FW} = T_{PWM} - T_{ON} - t_{HS-off}$$

Important note: For the proper use of **Equation (7.14)** refer to **Chapter 7.4.1**.

Equation to determine the entire freewheeling energy in the freewheeling MOSFET:

(7.15)

$$E_{FW} = I_{OUT}^2 \cdot R_{ON,FW} \cdot t_{FW} = I_{OUT}^2 \cdot R_{ON,FW} \cdot (T_{PWM} - T_{ON} - t_{HS-off})$$

From **Equation (7.15)** the average power dissipation in the freewheeling MOSFET can be determined by multiplying **Equation (7.15)** by f_{PWM}:

(7.16)

$$\overline{P_{FW}} = E_{FW} \cdot f_{PWM} = I_{OUT}^2 \cdot R_{ON,FW} \cdot (T_{PWM} - T_{ON} - t_{HS-off}) \cdot f_{PWM}$$

Equation (7.16) is an estimation of the average power dissipation in the freewheeling MOSFET. In **Figure 65**, this is the low side (LS) MOSFET.

7.5 Entire power dissipation in the NovalithIC™

To determine the entire power dissipation in the NovalithIC™, combine **Equation (7.13)**, **Equation (7.16)** and **Equation (7.3)**.

(7.17)

$$\overline{P_{Nova}} = \overline{P_{act}} + \overline{P_{FW}} + P_{CC}$$

Equation (7.17) is the average of the different power losses in one PWM period, as shown in **Figure 66**, plus the power losses in the control chip.

7.6 Simplifications

Because the losses in the control chip are typically negligible in comparison with the losses in the MOSFETs, they are neglected in this simplification.

Taking into account that the high side (HS) and the low side (LS) MOSFET are in a similar R_{ON} range, the equation for determining the entire power dissipation in the NovalithIC™ can be significantly reduced by using the same R_{ON} for both the high side (HS) and the low side (LS) MOSFET. The more conservative approach is to use the higher R_{ON} of both.

The idea behind this is to have the same R_{ON} for the conducted losses of the ON- and the freewheeling phase, according to **Figure 66**. Due to this simplification the energy in one PWM- period is two times the switching losses E_{SL} and R_{ON} losses during the remaining time:

(7.18)

$$E_{Nova} = 2 \cdot E_{SL} + P_{CL} \cdot (T_{PWM} - 2 \cdot t_{HS-off})$$

(7.19)

$$E_{Nova} = 2 \cdot \frac{V_S \cdot I_{OUT}}{2} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON} \cdot (T_{PWM} - 2 \cdot t_{HS-off})$$

From the the simplyfied NovalithIC™ energy to the simplified NovalithIC™ power dissipation by multiplying **Equation (7.19)** by f_{PWM}:

(7.20)

$$\overline{P_{Nova,S}} = (V_S \cdot I_{OUT} \cdot t_{HS-off} + I_{OUT}^2 \cdot R_{ON} \cdot (T_{PWM} - 2 \cdot t_{HS-off})) \cdot f_{PWM}$$

8 Thermal Performance

The PCB used for the simulation is compliant with JEDEC 2s2p (JESD 51-5, JESD 51-7) and JEDEC 1s0p (JESD 51-3), as described in **Table 3**. For 1s0p, a cooling area of 600 mm² and 300 mm² is additionally considered.

Table 3 PCB specification

Dimensions	76.2 × 114.3 × 1.5 mm³	λ_{therm} [W/m • K]
Material	FR4	0.3
Metalization	JEDEC 2s2p (JESD 51-7) + (JESD 51-5) JEDEC 1s0p (JESD 51-3) + Cooling Area	388
Cooling Area	600 mm², 300 mm², footprint	
Thermal Vias	Ø = 0.3 mm; plating 25 µm; 40 pcs.	
Package Attach [50 µm]	Solder	55

The cross section of JEDEC 2s2p is shown in **Figure 67**.

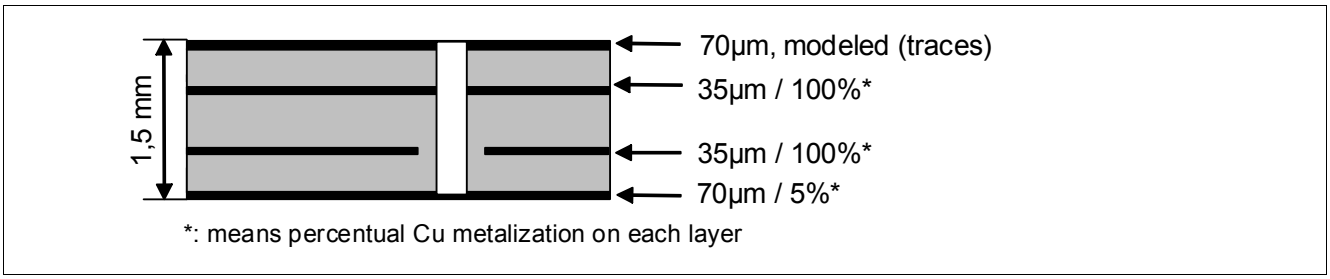

Figure 67 Cross section JEDEC 2s2p

The cross section of JEDEC 1s0p is shown in **Figure 68**.

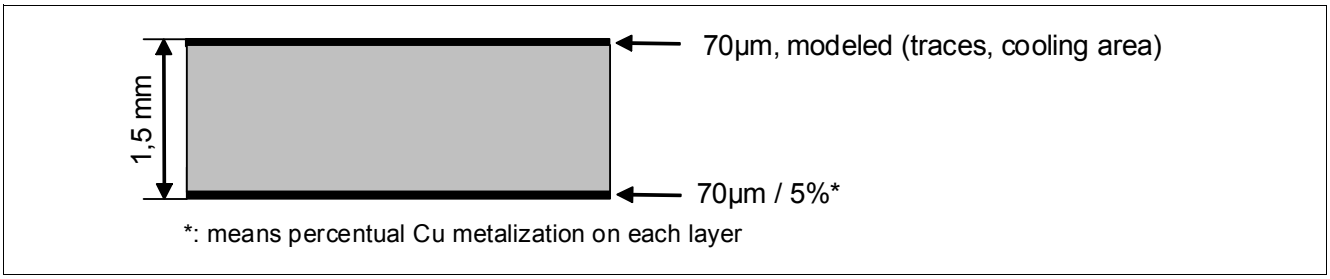

Figure 68 Cross section JEDEC 1s0p

8.1 Zth simulation results

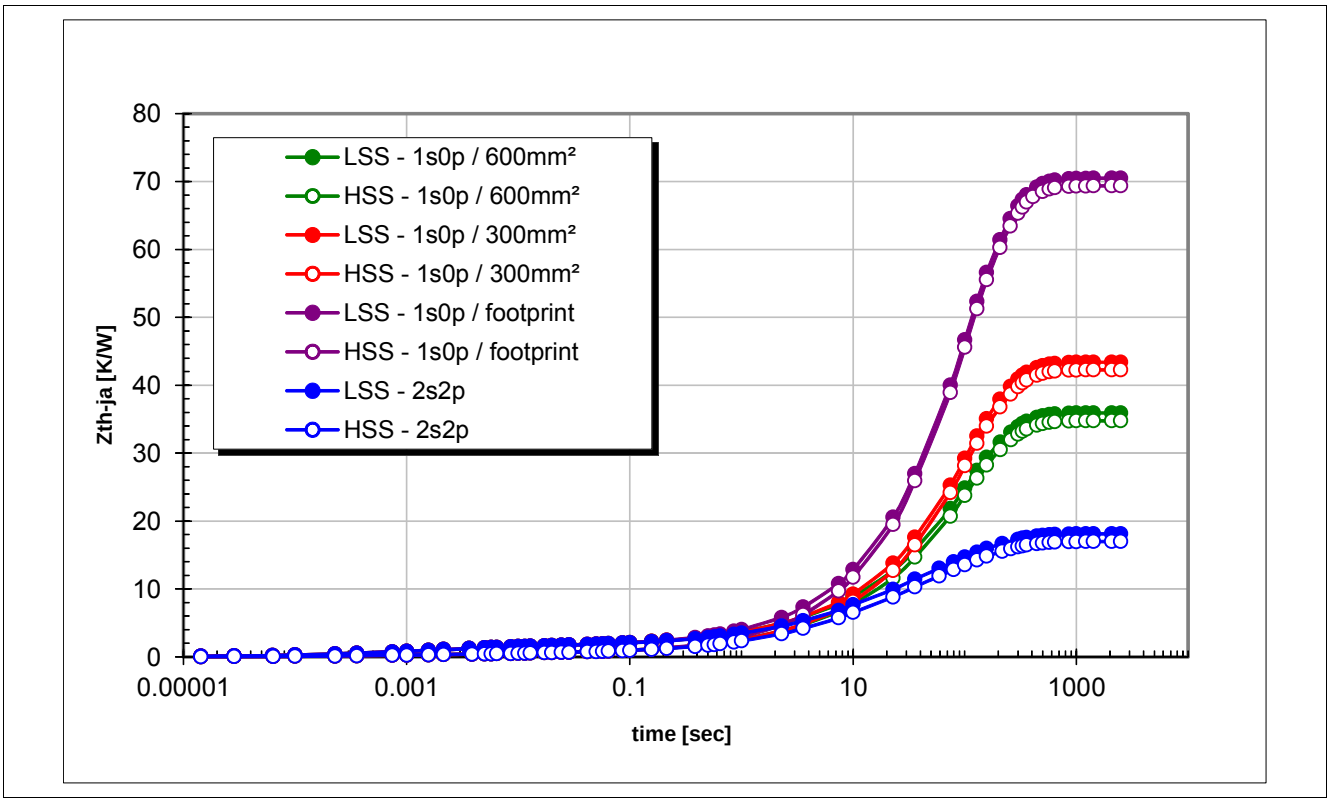

Figure 69 $Z_{th\text{-}ja}$ **for BTN8960/62, in PG-TO263-7-1, (LSS: low side switch, HSS: high side switch)**

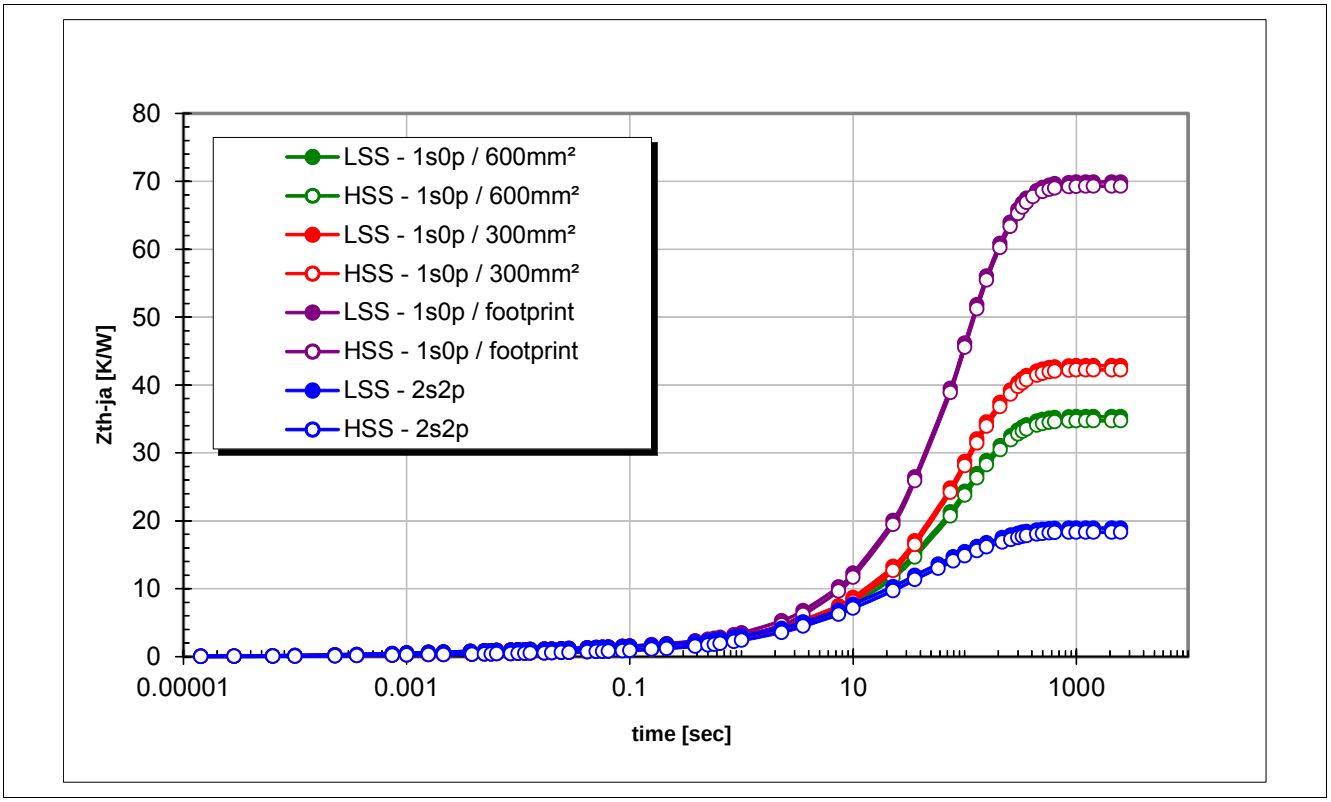

Figure 70 $Z_{th\text{-}ja}$ **for BTN8980/82, in PG-TO263-7-1, (LSS: low side switch, HSS: high side switch)**

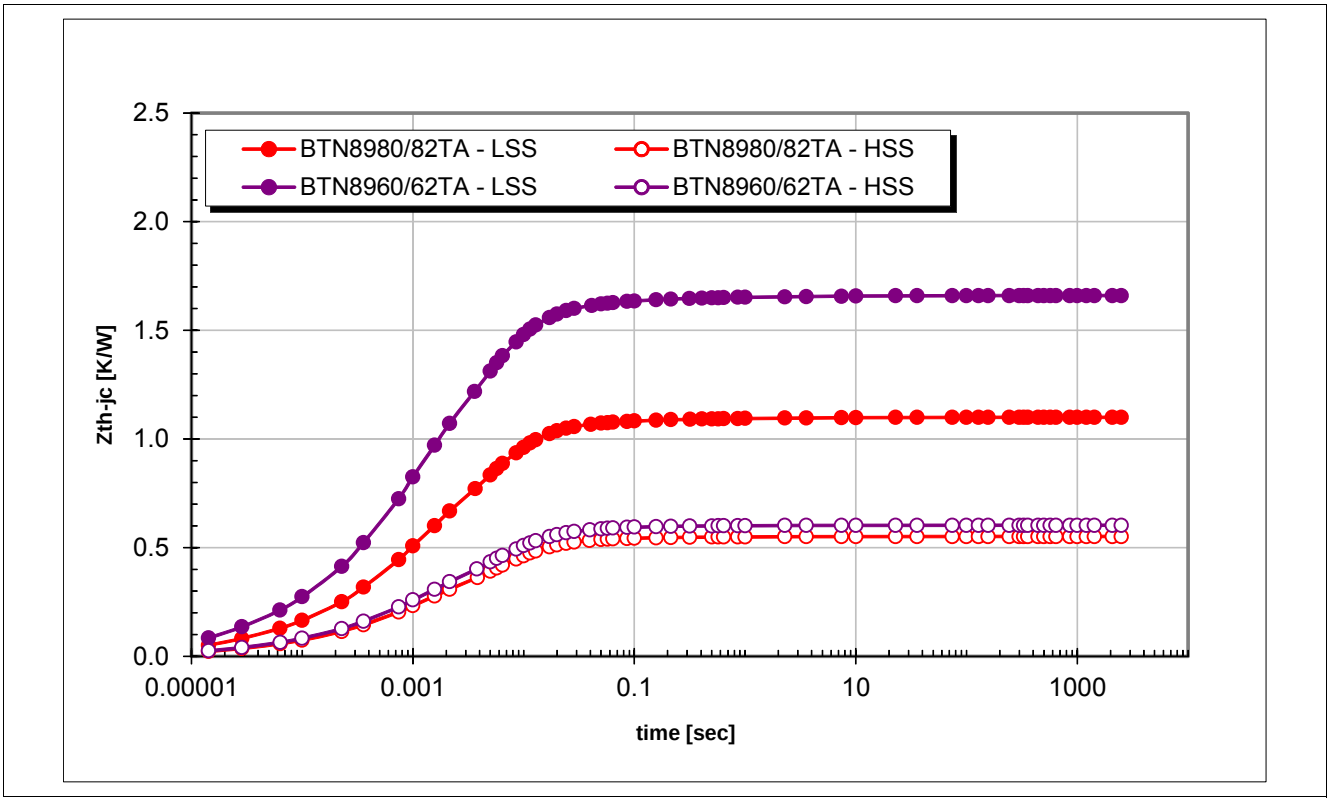

Figure 71 $Z_{th\text{-}jc}$ **for BTN8960/62/80/82, in PG-TO263-7-1, (LSS: low side switch, HSS: high side switch)**

8.2 Thermal RC-network

The thermal behavior of the BTN89xy can be simulated based on the thermal RC-network shown in **Figure 72**. The abbreviations can be found in **Table 4**.

Table 4 Abbreviations for the thermal RC-network of BTN89xy

Abbreviation	Description (temperature level)
GND	thermal ground, corresponds to ambient temperature
CC	Control chip with temperature sensor for overtemperature detection
LS	low side MOSFET
HS	high side MOSFET

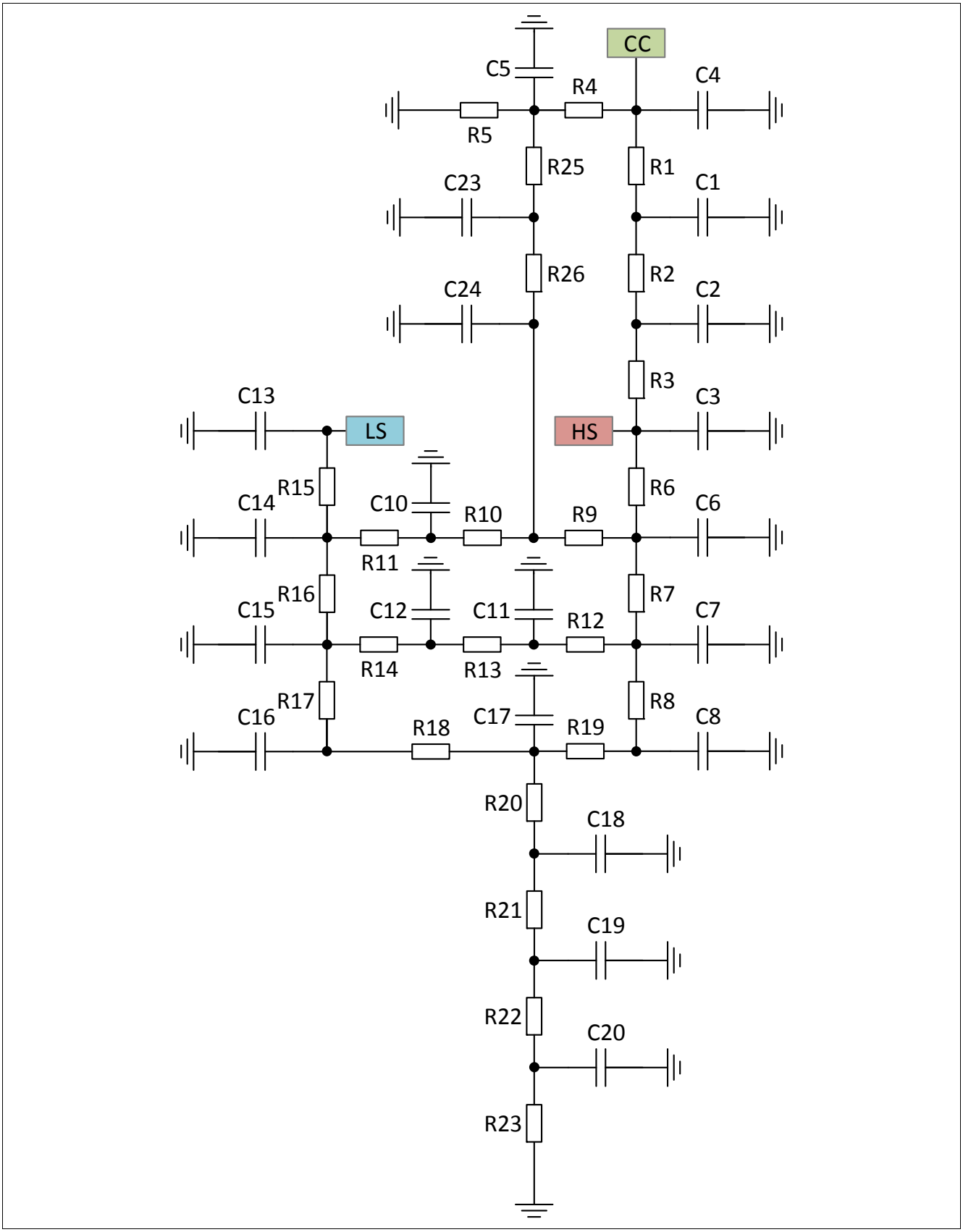

Figure 72 Schematic of the thermal RC-network for BTN89xy

8.2.1 Parameters for BTN8960/62

For the thermal RC-network, which is shown in **Figure 72**, the values of the BTN8960/62 for the resistors can be found in **Table 5** and for the capacities in **Table 6**, depending on the test condition (PCB).

Table 5 Thermal RC-network resistor values for BTN8960/62

Parameter	1s0p	2s2p	300 mm²	600 mm²
R1	4.13479	6.14635	4.36197	3.28848
R2	9.49529	6.99412	8.86409	10.2156
R3	6.04676	6.24923	6.00779	5.73654
R4	1997.68	1999.98	9989.45	9989.4
R5	24.6962	14.3669	26.5405	23.2126
R6	0.765526	0.825716	0.784931	0.793983
R7	709.461	21.7132	712.375	703.027
R8	24.0397	959.748	98.4013	83.6365
R9	0.509237	0.277148	0.267684	0.257237
R10	0.0201271	0.219217	0.159445	0.17652
R11	0.0134086	0.753008	0.0120334	0.0123115
R12	48.4465	75.4798	187.262	157.461
R13	2.15834	0.703103	41.9972	47.1135
R14	827.333	312.256	793.297	744.845
R15	1.89889	1.16198	1.93861	1.90089
R16	5.67666	1.27492	3.89945	3.75373
R17	30.7871	257.22	3.29846	4.09169
R18	954.388	1715.55	685.267	466.671
R19	0.666271	183.372	1.66419	2.4898
R20	9.17544	11.5243	49.7984	49.454
R21	8.86655	132.758	4.50777	5.96947
R22	3.64248	4.55264	20.7864	22.0143
R23	1.54282	47.1593	9.53249	12.2849
R25	0.0115874	0.0111131	0.0120082	0.0107333
R26	59.2163	3.41491	16.2884	10.0589

Table 6 Thermal RC-network capacitor values for BTN8960/62

Parameter	1s0p	2s2p	300 mm²	600 mm²
C1	9.01E-07	8.11E-06	9.00E-06	1.33E-05
C2	0.0096747	0.00768932	0.00857854	0.0093771
C3	0.00328475	0.00461763	0.00376799	0.00326148
C4	0.00117103	0.0011541	0.0011511	0.00116079
C5	1.92349	0.419775	2.01168	2.98621
C6	0.259815	0.361034	0.236595	0.25227
C7	2.30445	1.17886	0.502516	0.85818
C8	0.0924509	0.169357	0.147342	0.233769
C10	0.0759261	0.000081424	0.146105	0.138098
C11	0.874947	0.681589	0.005741	0.00594316
C12	0.0219339	0.641786	0.40078	0.441664
C13	0.00211971	0.00072605	0.00200476	0.00193489
C14	0.0518487	0.0149359	0.0742448	0.0420656
C15	0.45993	0.0446105	0.746801	0.67808
C16	0.264822	0.17218	0.253172	0.228248
C17	2.00613	0.960968	0.182447	0.152115
C18	0.0477427	0.157112	0.3562	0.3517
C19	2.21387	7.70672	1.95155	1.56875
C20	5.75675	17.92	2.706	1.05419
C23	0.482909	0.455128	0.00175319	0.00109187
C24	0.00483449	0.00210439	0.0014892	0.00143505

8.2.2 Parameters for BTN8980/82

For the thermal RC-network, which is shown in **Figure 72**, the values of the BTN8980/82 for the resistors can be found in **Table 7** and for the capacities in **Table 8**, depending on the test condition (PCB).

Table 7 Thermal RC-network resistor values for BTN8980/82

Parameter	1s0p	2s2p	300 mm²	600 mm²
R1	14.7357	14.607	14.5115	14.4932
R2	1.41757	2.99853	0.892556	0.662104
R3	4.68444	2.59111	4.77943	5.04297
R4	417.267	996.831	999.052	962.665
R5	112.975	18.9927	52.4443	41.5135
R6	0.631354	0.586299	0.663352	0.592812
R7	32.786	17.7176	12.9216	10.8754
R8	238.436	60.6471	141.19	133.593
R9	0.010794	0.253683	0.0664578	0.0534714
R10	0.697554	0.0136973	0.843804	0.729177
R11	0.457247	0.800679	0.0121925	0.527079
R12	3.16907	0.309781	0.0990132	0.729318
R13	0.863968	608.83	4.30397	0.308658
R14	122.484	743.102	993.339	108.893
R15	0.922458	0.943908	1.03571	0.725828
R16	63.0068	28.9428	23.0979	13.6581
R17	16.2261	14.9297	20.1678	13.6112
R18	14.9109	0.01	18.7873	15.8732
R19	269.376	711.221	999.114	998.955
R20	31.986	15.9504	33.3671	24.8793
R21	14.5539	11.788	2.37429	2.66703
R22	19.4019	24.147	18.495	13.1898
R23	15.6402	1.70354	20.424	20.3062
R25	0.0102647	0.0180739	0.0147595	0.0992122
R26	5.9597	2.67745	2.46301	2.16571

Table 8 Thermal RC-network capacitor values for BTN8980/82

Parameter	1s0p	2s2p	300 mm²	600 mm²
C1	0.0109887	0.0122742	0.0117668	0.0114942
C2	4.38961E-06	1.75918E-06	1.13147E-05	0.00010077
C3	0.00361686	0.00382319	0.00452151	0.00335106
C4	0.00117385	0.00118004	0.0011766	0.00117587
C5	0.0144137	0.400558	0.186452	0.249974
C6	0.064702	0.0424699	0.0426304	0.0280119
C7	0.124171	0.0566395	0.407592	0.66619
C8	0.0184178	0.840657	0.061641	0.224521
C10	0.127647	0.0215798	0.0135012	0.130117
C11	0.219454	0.965128	0.201947	0.289226
C12	0.0757321	0.0222976	0.280791	0.460985
C13	0.0020413	0.00210601	0.00223527	0.0013234
C14	0.0489809	0.0743878	0.105303	0.018626
C15	0.28671	0.102	0.411468	0.464271
C16	0.00598831	0.0157598	0.00766389	0.00254175
C17	0.000668051	0.171968	0.0555266	0.0541936
C18	0.801461	3.05061	1.75168	0.000842353
C19	0.00214924	4.84858	0.365562	0.0312806
C20	5.63547	6.30449	2.98494	7.0397
C23	0.348292	0.184817	0.3862	0.261893
C24	0.0995441	0.242926	0.180138	0.116301

9 Revision History

Revision	Date	Changes
0.4	2015-07-02	**Page 19**, **Figure 10**: Motor shunt replaced. **Page 67**, **Figure 66**: TON and DC new description. **Chapter 5.5** added. **Chapter 6** added. **Chapter 8** added. Style Guide update (EDD41). Editorial changes.
0.3	2014-08-29	**Page 18** - **Chapter 4.3**: Added. **Page 20** - **Chapter 7.2**: Text update. **Page 64** - **Chapter 7**: Added. **Chapter 2**: Updated application circuits (C1 and DC-link)
0.2	2013-01-16	**Page 5** - **Chapter 2**: Added benefits. **Page 6** - **Figure 2**; **Page 7** - **Figure 3**; **Page 12** - Other Components: Changed resistor name from R_1 to R_3 and C_{IS}-value to 1nF and C_{IS}-text. **Page 14**: Updated **Figure 7**. **Page 6** - **Figure 2**, **Page 7** - **Figure 3**: Update value of C1. **Page 12** - **Figure 6**: Update footnote of figure. **Page 21**: New **Chapter 5**.
0.1	2012-07-09	Initial release.

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