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# Chapter 8-3
# Register Allocation

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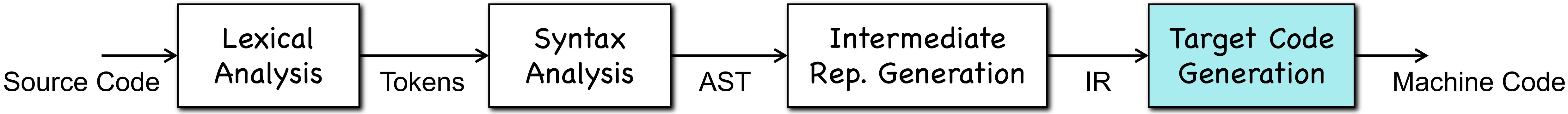

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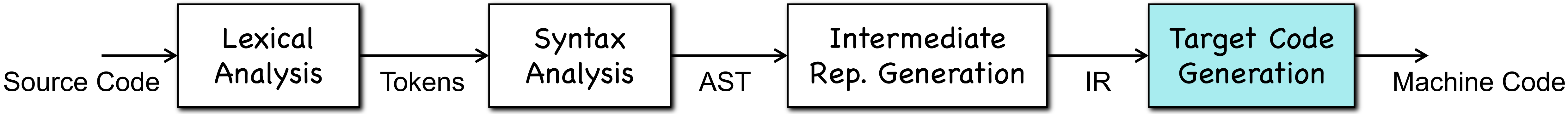


- Speed: Registers > Memory
- Physical machines have limited number of registers
- **Register allocation**: ∞ virtual registers ➞ k physical registers

# PART I: Local Register Allocation

# Register Allocation

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# Register Allocation

- Speed: Registers > Memory
- Physical machines have limited number of registers
- **Register allocation**: ∞ virtual registers → k physical registers

- **Requirement:**
  - Produce correct code using k or fewer registers
  - Minimize loads, stores, and space to hold spilled values
  - Efficient register allocation (O(n) or O(nlogn))

# Register Allocation

- Two values CANNOT be mapped to the same register wherever they are both **live** (before their last use)

```
LD   R1, y            // R1 = y
LD   R2, z            // R2 = z
SUB  R1, R1, R2       // R1 = R1 - R2
ST   x, R1            // x = R1
```

**x = y - z**

# Register Allocation

- Two values CANNOT be mapped to the same register wherever they are both **live** (before their last use)

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- Two values CANNOT be mapped to the same register wherever they are both **live** (before their last use)

- **Spilling**:
  - saves a value from a register to memory
  - the register is then free for other values
  - we can load the spilled value from memory to register when necessary

# Local Register Allocation

- Register allocation in a block

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- **MAXLIVE**: the maximum of values live at each instruction
  - **MAXLIVE ≤ k** --- Allocation is trivial
  - **MAXLIVE > k** --- Values must be spilled to the memory

# MAXLIVE

```
1. LD    R1    #1028        // R1 <- 1028
2. LD    R2    *R1          // R2 <- contents(R1), assume y
3. MUL   R3    R1    R2     // R3 <- 1028 * y
4. LD    R4    x            // R4 <- x
5. SUB   R5    R4    R2     // R5 <- x−y
6. LD    R6    z            // R6 <- z
7. MUL   R7    R5    R6     // R7 <- z * (x-y)
8. SUB   R8    R7    R3     // R8 <- z * (x-y) – 1028 * y
9. ST    *R1   R8           // contents(R1) <- z * (x-y) – 1028 * y
```

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6. LD   R6   z           // R6 <- z
7. MUL  R7   R5    R6    // R7 <- z * (x-y)
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6. LD    R6   z            // R6 <- z
7. MUL   R7   R5    R6     // R7 <- z * (x-y)
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6. LD    R6   z          // R6 <- z
7. MUL   R7   R5    R6   // R7 <- z * (x-y)
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1. LD    R1    #1028      // R1
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3. MUL   R3    R1    R2   // R1 R2 R3
4. LD    R4    x          // R1 R2 R3 R4
5. SUB   R5    R4    R2   // R1    R3    R5
6. LD    R6    z          // R1    R3    R5 R6
7. MUL   R7    R5    R6   // R1    R3          R7
8. SUB   R8    R7    R3   // R1                   R8
9. ST    *R1   R8         //
```

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6. LD     R6     z              // R1    R3    R5 R6
7. MUL    R7     R5      R6     // R1    R3          R7
8. SUB    R8     R7      R3     // R1                   R8
9. ST     *R1    R8             //
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3. MUL    R3    R1     R2    // R1  R2  R3
4. LD     R4    x            // R1  R2  R3  R4
5. SUB    R5    R4     R2    // R1      R3      R5
6. LD     R6    z            // R1      R3      R5  R6
7. MUL    R7    R5     R6    // R1      R3              R7
8. SUB    R8    R7     R3    // R1                          R8
9. ST     *R1   R8           //
```

**MAXLIVE = 4**

# MAXLIVE

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6. LD     R6    z             // R1    R3    R5 R6
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**MAXLIVE = 4**

Enough to have 4 registers

# Local Register Allocation

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5. SUB   R5   R4    R2   // R1    R3    R5
6. LD    R6   z          // R1    R3    R5 R6
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8. SUB   R8   R7    R3   // R1                   R8
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if k ≥ 4, e.g., k = 4

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5. SUB   R2   R4    R2     // R1    R3    R2
6. LD    R4   z            // R1    R3    R2 R4
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6. LD    R6    z            // R1    R3    R5 R6
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if k < 4, e.g., k = 3

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5. SUB   R5    R4    R2     // R1    R3    R5
6. LD    R6    z            // R1    R3    R5 R6
7. MUL   R7    R5    R6     // R1    R3          R7
8. SUB   R8    R7    R3     // R1                   R8
9. ST    *R1   R8           //
```

**Spill R3 by** ST v R3

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1. LD    R1    #1028       // R1
2. LD    R2    *R1         // R1 R2
3. MUL   R3    R1    R2    // R1 R2 R3
4. LD    R4    x           // R1 R2 R3 R4
5. SUB   R5    R4    R2    // R1    R3    R5
6. LD    R6    z           // R1    R3    R5 R6
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6. LD   R6   z          // R1          R5 R6
7. MUL  R7   R5   R6    // R1                R7
8. SUB  R8   R7   R3    // R1                   R8
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6. LD    R6    z            // R1          R5 R6
7. MUL   R7    R5    R6     // R1                R7
8. SUB   R8    R7    R3     // R1                   R8
9. ST    *R1   R8           //
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**Spill R3 by** ST v R3

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**Reload R3 by** LD R3 v

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6. LD    R6   z           // R1          R5 R6
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8. SUB   R8   R7    R3    // R1                   R8
9. ST    *R1  R8          //
```

**Spill R3 by** <u>ST v R3</u>

**MAXLIVE = 4**

if k < 4, e.g., k = 3

**Reload R3 by** <u>LD R3 v</u>

# Why R3? Many Heuristic Methods

```
1. LD    R1   #1028       // R1
2. LD    R2   *R1         // R1 R2
3. MUL   R3   R1    R2    // R1 R2 R3
4. LD    R4   x           // R1 R2 R3 R4
5. SUB   R5   R4    R2    // R1    R3    R5
6. LD    R6   z           // R1    R3    R5 R6
7. MUL   R7   R5    R6    // R1    R3          R7
8. SUB   R8   R7    R3    // R1                   R8
9. ST    *R1  R8          //
```

**Spill R3 by** ST v R3

**MAXLIVE = 4**

if k < 4, e.g., k = 3

# Spill Value, Next Use, Farthest

```
1. LD     R1    #1028         // R1
2. LD     R2    *R1           // R1 R2
3. MUL    R3    R1     R2     // R1 R2 R3
4. LD     R4    x             // R1 R2 R3 R4
5. SUB    R5    R4     R2     // R1    R3    R5
6. LD     R6    z             // R1    R3    R5 R6
7. MUL    R7    R5     R6     // R1    R3          R7
8. SUB    R8    R7     R3     // R1                   R8
9. ST     *R1   R8            //
```

**Spill R1 by** ST v R1

**MAXLIVE = 4**

if k < 4, e.g., k = 3

# PART II: Global Register Allocation

# Global Register Allocation

- Local register allocation does not capture reuse of values across multiple basic blocks

- Global allocation often uses the **graph-coloring** paradigm

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- Global allocation often uses the **graph-coloring** paradigm
  - Build a **conflict/interference graph**
  - Find a **k-coloring** for the graph, or change the code to a nearby problem that it can color

# Global Register Allocation

- Local register allocation does not capture reuse of values across multiple basic blocks
- Global allocation often uses the **graph-coloring** paradigm
  - Build a **conflict/interference graph**
  - Find a **k-coloring** for the graph, or change the code to a nearby problem that it can color
  - **NP-complete** under nearly all assumptions, so heuristics are needed

# K-Coloring

- **Vertex Coloring**: assign a color to each vertex such that no edge connects vertices with the same color.

# K-Coloring

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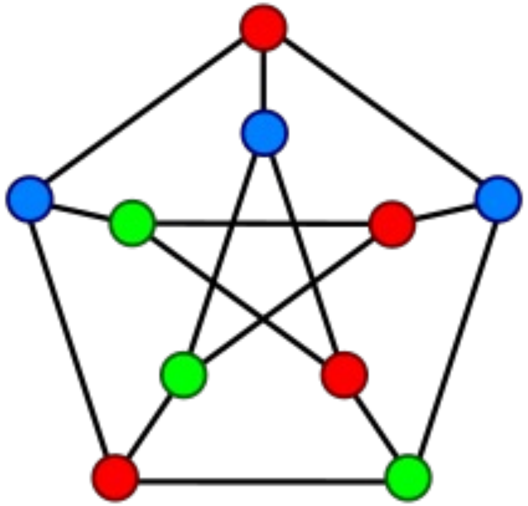

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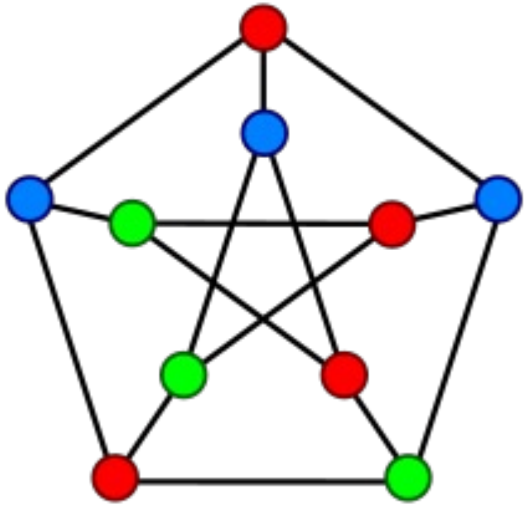
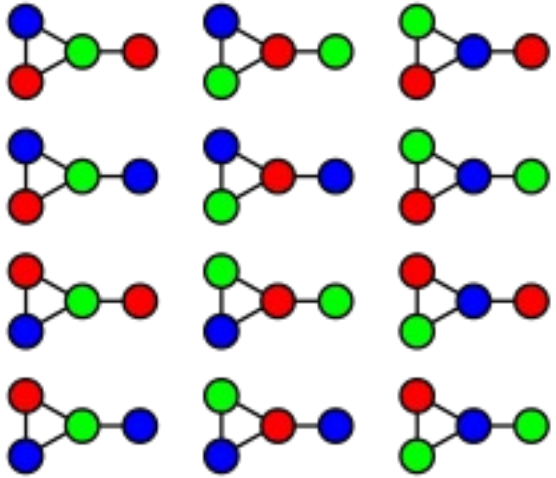
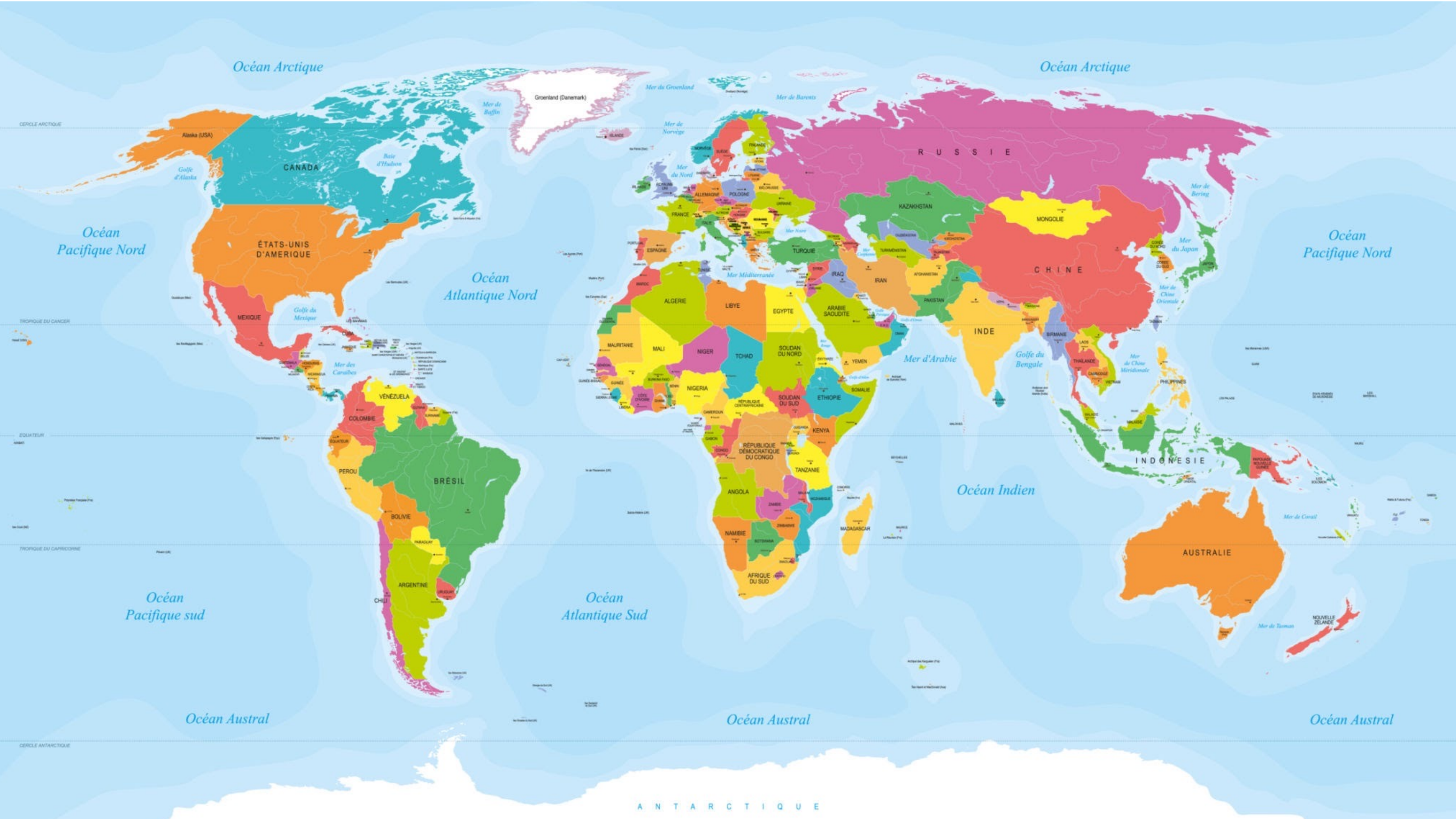




**3-coloring in 12 ways**



Océan Arctique
Océan Arctique
Groenland (Danemark)
Mer du Groenland
Mer de Barents
Mer de Baffin
Mer de Norvège
CERCLE ARCTIQUE
Alaska (USA)
CANADA
Baie d'Hudson
Golfe d'Alaska
ISLANDE
Mer du Nord
NORVÈGE
SUÈDE
FINLANDE
IRLANDE
ALLEMAGNE
POLOGNE
BÉLORUSSIE
UKRAINE
FRANCE
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ESPAGNE
PORTUGAL
R U S S I E
Mer de Bering
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MONGOLIE
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PAKISTAN
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Mer de Chine Orientale
MAROC
ALGERIE
LIBYE
EGYPTE
ARABIE SAOUDITE
MEXIQUE
Golfe du Mexique
TROPIQUE DU CANCER
CUBA
INDE
Mer d'Arabie
Golfe du Bengale
BIRMANIE
THAILANDE
Mer de Chine Méridionale
PHILIPPINES
MAURITANIE
MALI
NIGER
TCHAD
SOUDAN DU NORD
YEMEN
Mer des Caraïbes
SENEGAL
NIGERIA
ETHIOPIE
SOMALIE
VÉNÉZUELA
COLOMBIE
SOUDAN DU SUD
RÉPUBLIQUE CENTRAFRICAINE
CAMEROUN
EQUATEUR
KENYA
RÉPUBLIQUE DÉMOCRATIQUE DU CONGO
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INDONESIE
PEROU
BRÉSIL
ANGOLA
Océan Indien
ZAMBIE
MOZAMBIQUE
MADAGASCAR
BOLIVIE
NAMIBIE
BOTSWANA
ZIMBABWE
Mer de Corail
PARAGUAY
TROPIQUE DU CAPRICORNE
AUSTRALIE
ARGENTINE
AFRIQUE DU SUD
CHILI
URUGUAY
Océan Pacifique sud
Océan Atlantique Sud
NOUVELLE ZÉLANDE
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A N T A R C T I Q U E

# K-Coloring for Register Allocation

- Map graph vertices onto virtual registers
- Map colors onto physical registers

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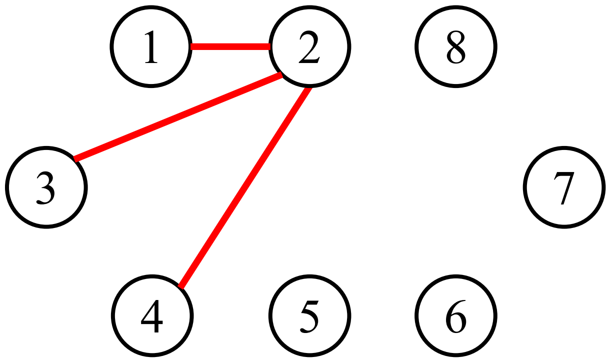
- **Map graph vertices onto virtual registers**
- **Map colors onto physical registers**

- From live ranges construct a **conflict graph**
- Color the graph so that no two neighbors have the same color
- If graph needs more than $k$ colors – Spilling

# Conflict Graph

- **Vertex**: virtual registers;
- **Edges**: virtual registers that have overlapping live range

```
1. LD     R1    #1028         // R1
2. LD     R2    *R1           // R1 R2
3. MUL    R3    R1     R2     // R1 R2 R3
4. LD     R4    x             // R1 R2 R3 R4
5. SUB    R5    R4     R2     // R1    R3    R5
6. LD     R6    z             // R1    R3    R5 R6
7. MUL    R7    R5     R6     // R1    R3          R7
8. SUB    R8    R7     R3     // R1                   R8
9. ST     *R1   R8            //
```

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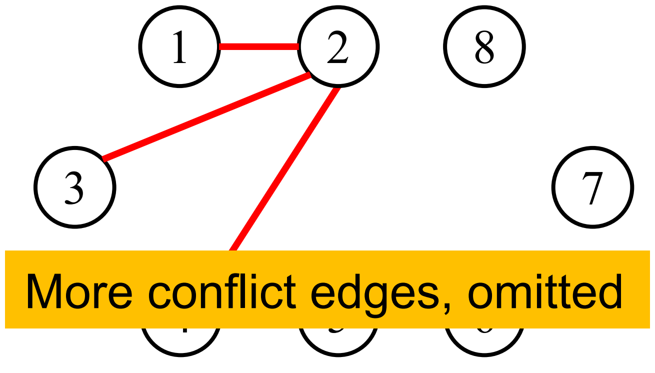


Conflict Graph

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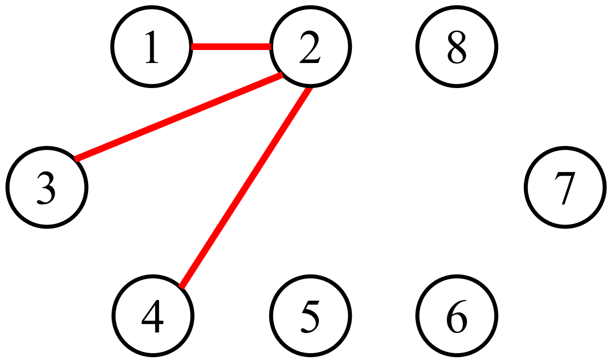
If we can use k, e.g., 4, colors, to color the graph, the 8 virtual registers can be replaced by 4 physical registers.




Conflict Graph

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- **Vertex**: virtual registers;
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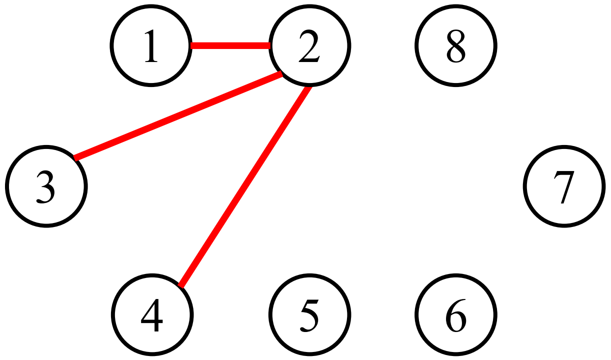
If we have to use 5 colors to color the graph, but only k = 4 physical registers are available, spilling is necessary.




Conflict Graph

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- A vertex whose degree < k is always k-colorable

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- Chaitin's Algorithm
- ACM SIGPLAN Symposium on Compiler Construction (1982)

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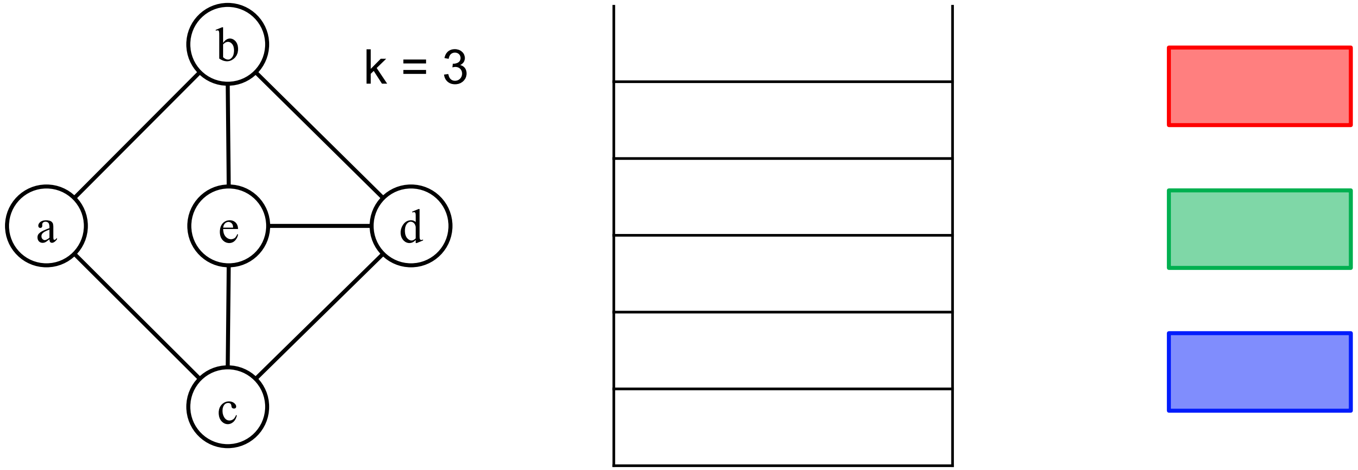

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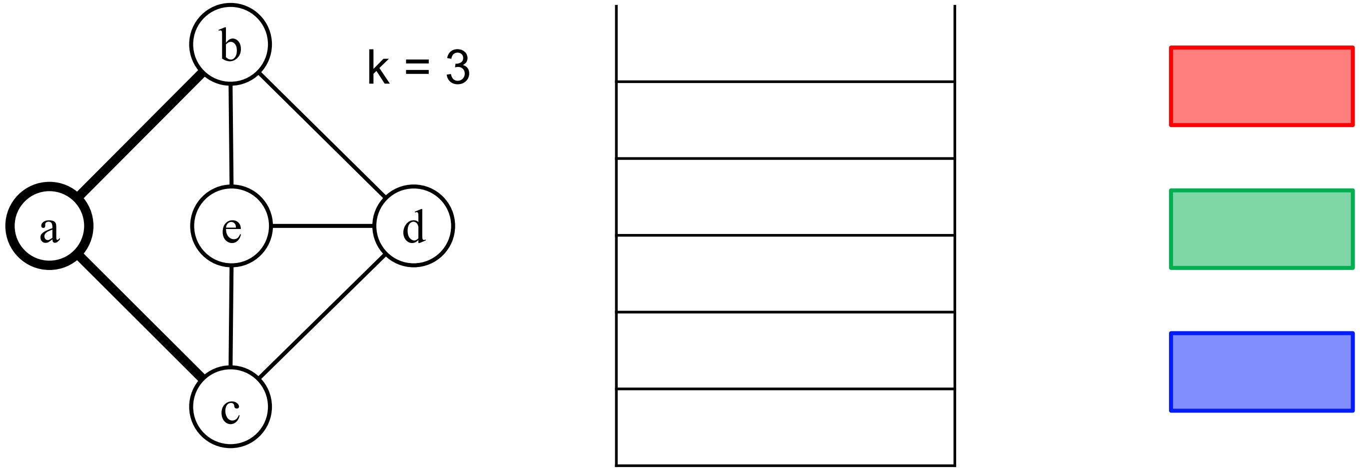

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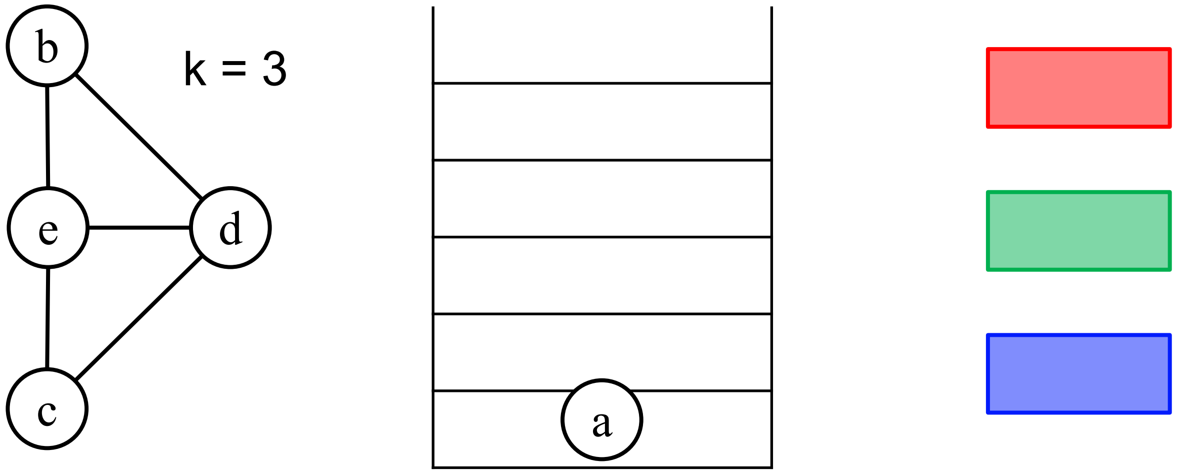

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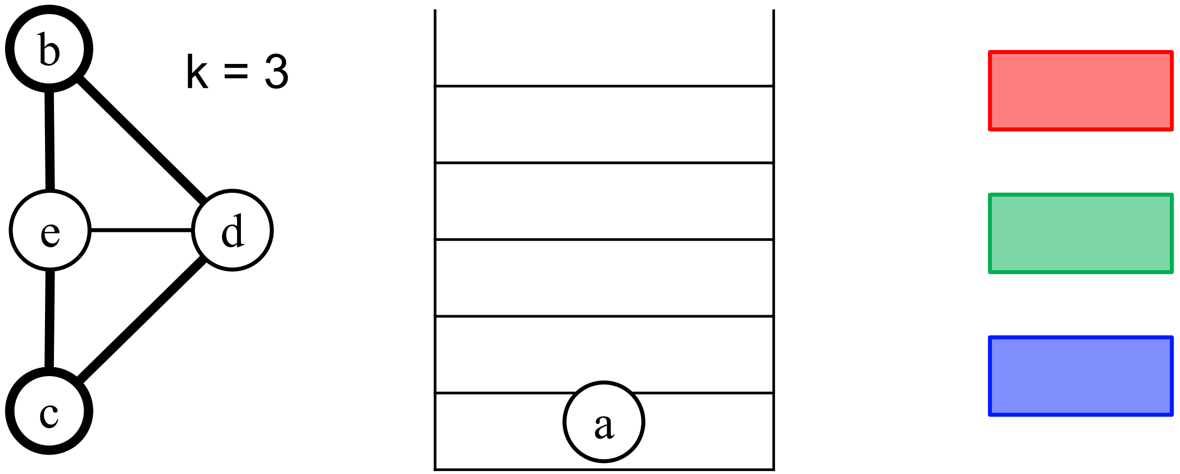

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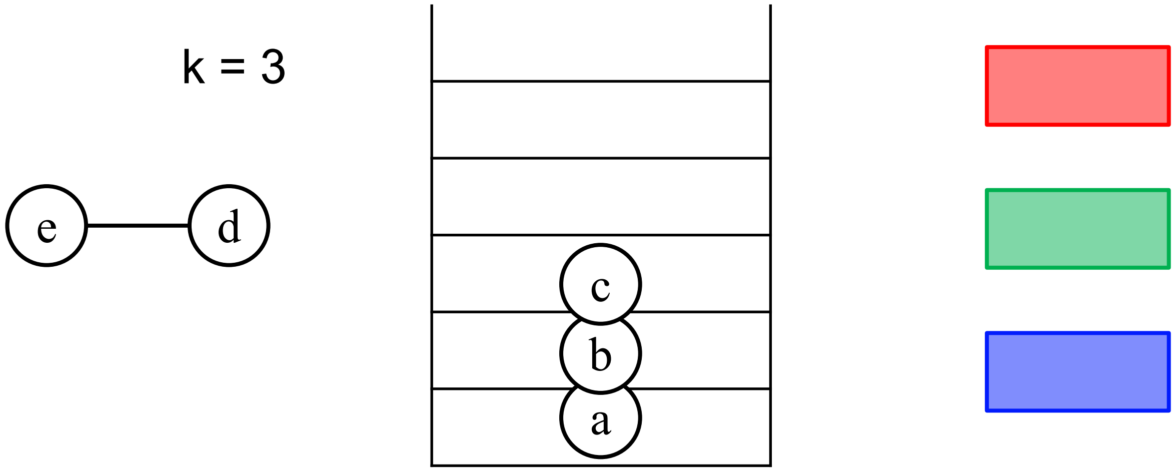

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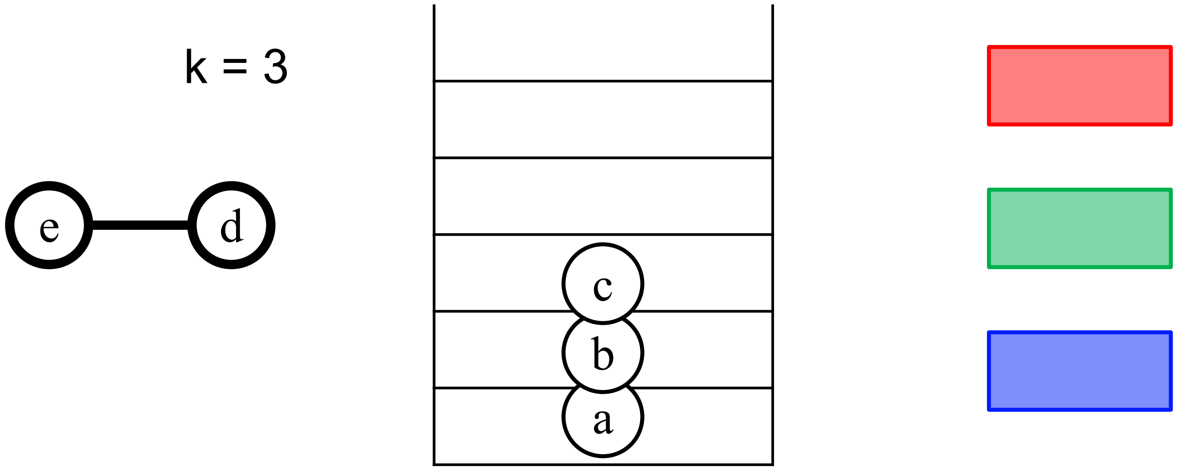

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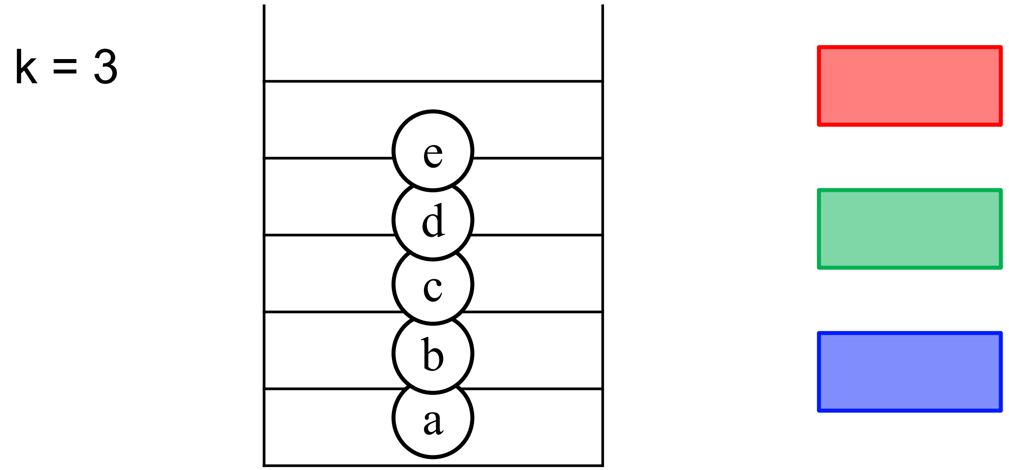

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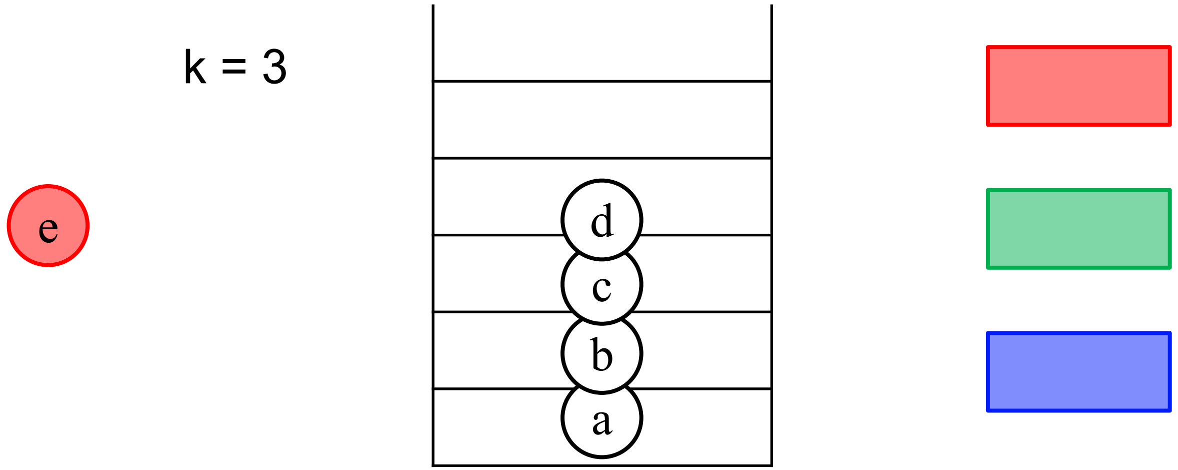

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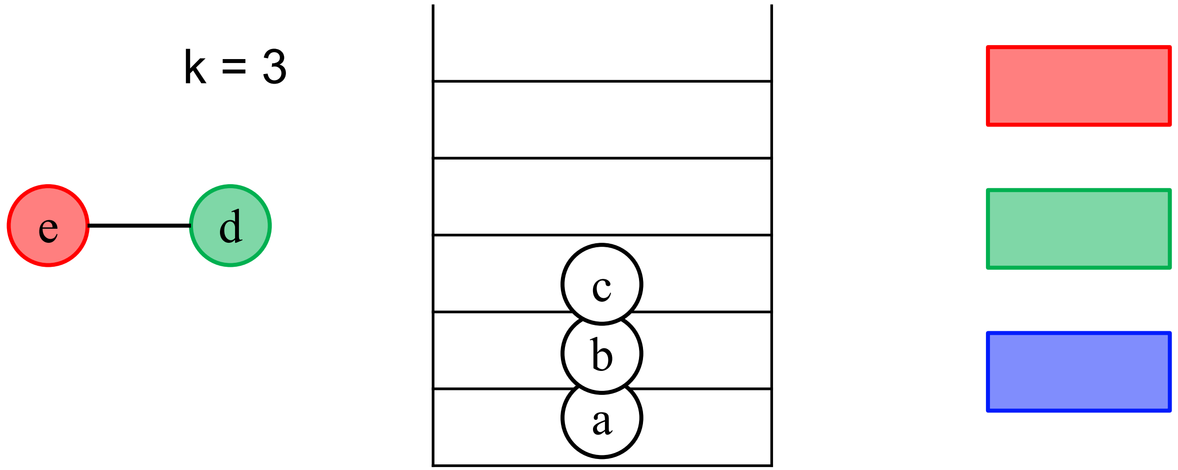

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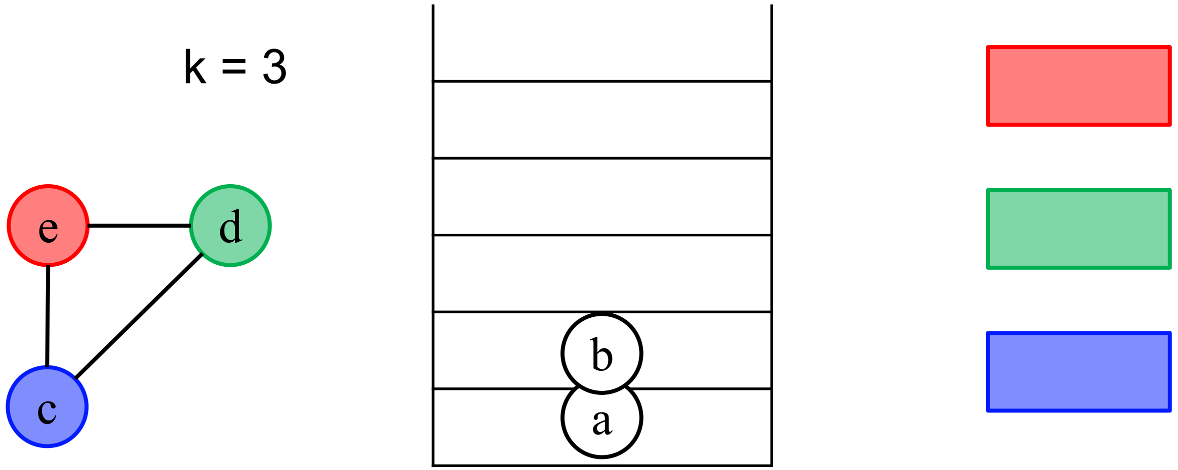

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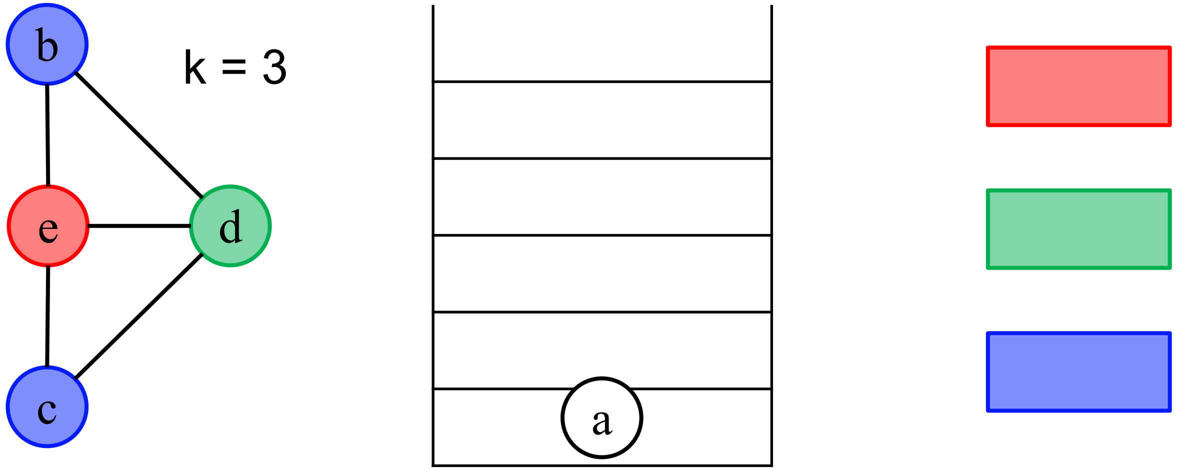

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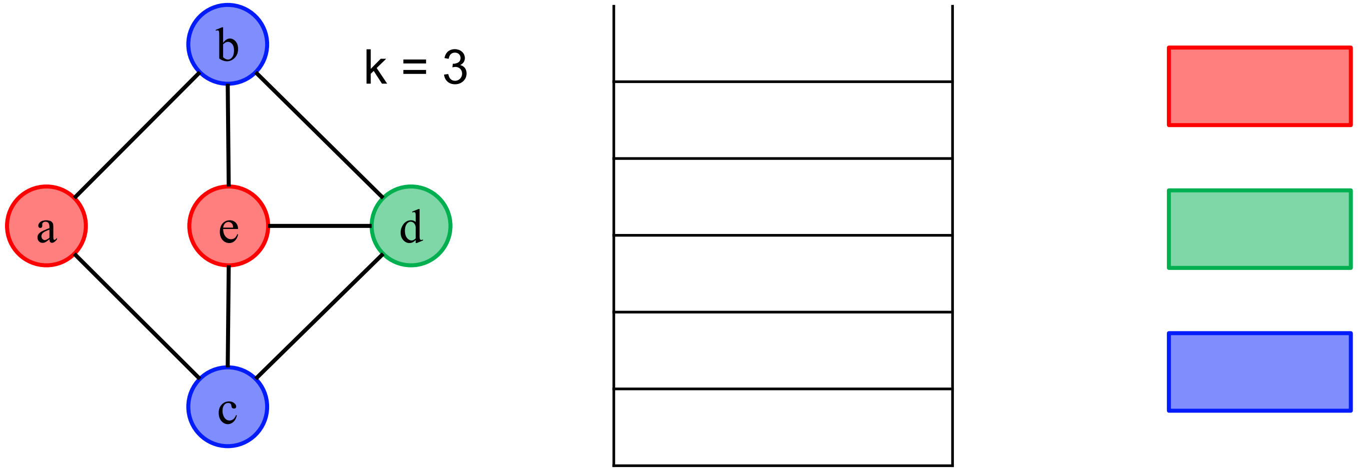

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  - remove the vertex from the graph
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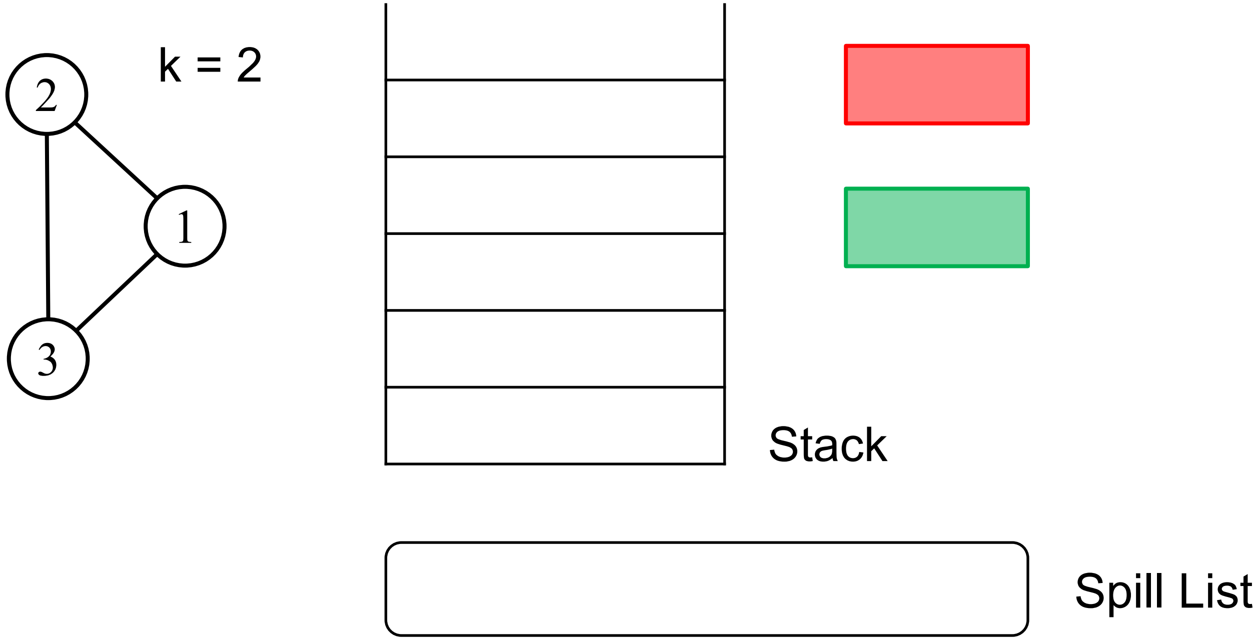
- If the spill list is not empty, insert spill code, rebuild conflict graph, and retry allocation.

# Chaitin’s Algorithm

```
1. LD   R1  #1028       // R1
2. LD   R2  *R1         // R1 R2
3. MUL  R3  R1    R2    // R1 R2 R3
4. ST   x   R3          // R1 R2
5. ST   y   R2          // R1
6. ST   z   R1          //
```



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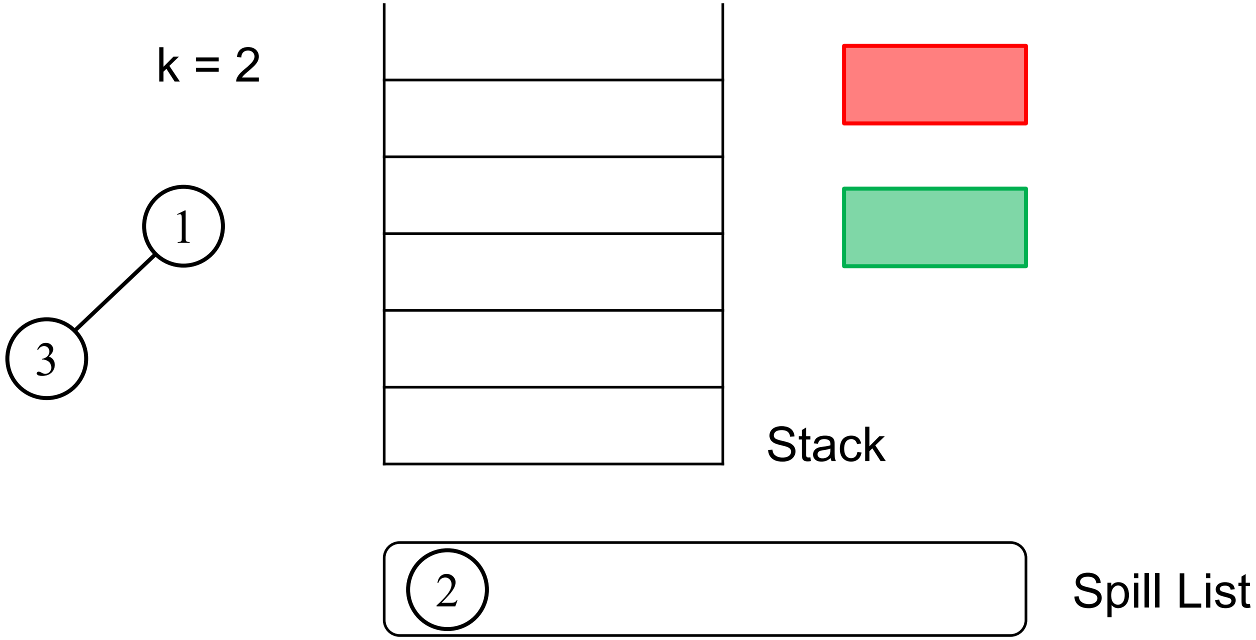

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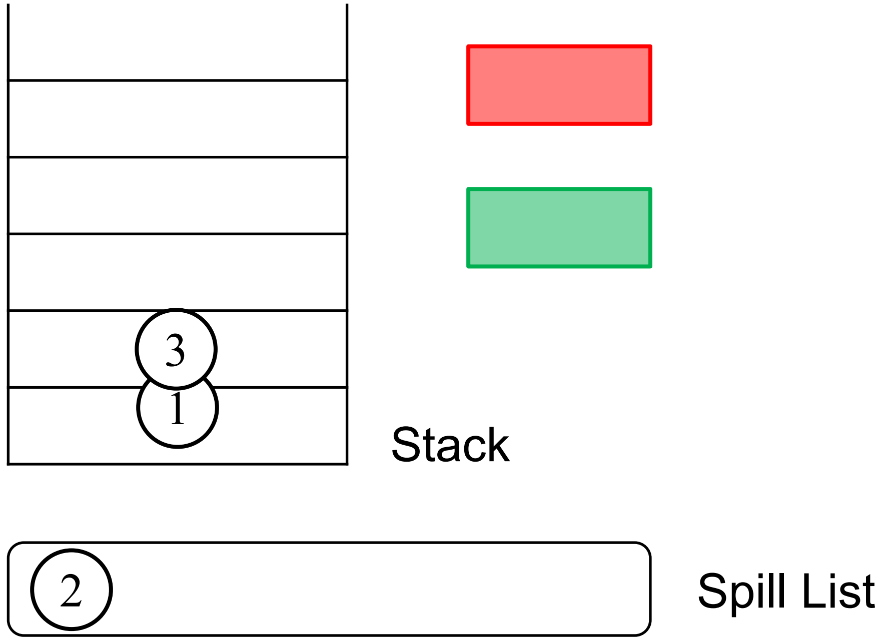
k = 2



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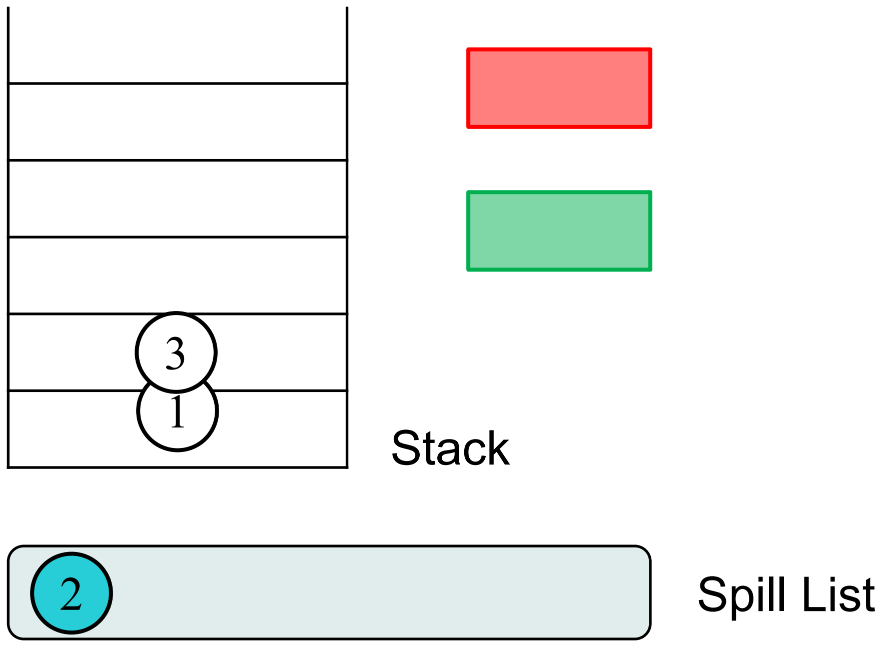


Spill R2!

# Chaitin's Algorithm

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1. LD   R1  #1028        // R1
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3. ST   a   R2           // R1
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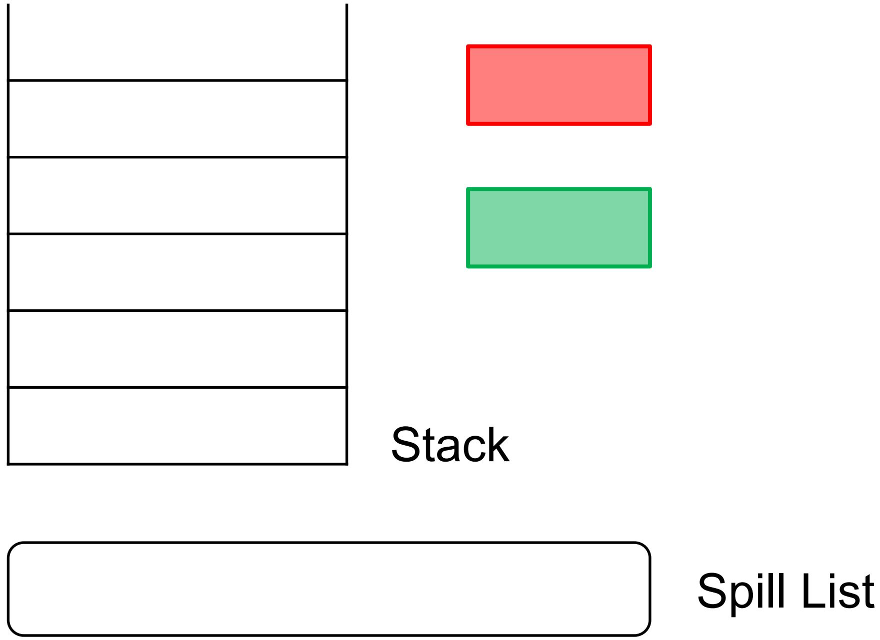
5. ST   x   R3           // R1
6. LD   R2  a            // R1 R2
7. ST   y   R2           // R1
8. ST   z   R1           //
```

k = 2



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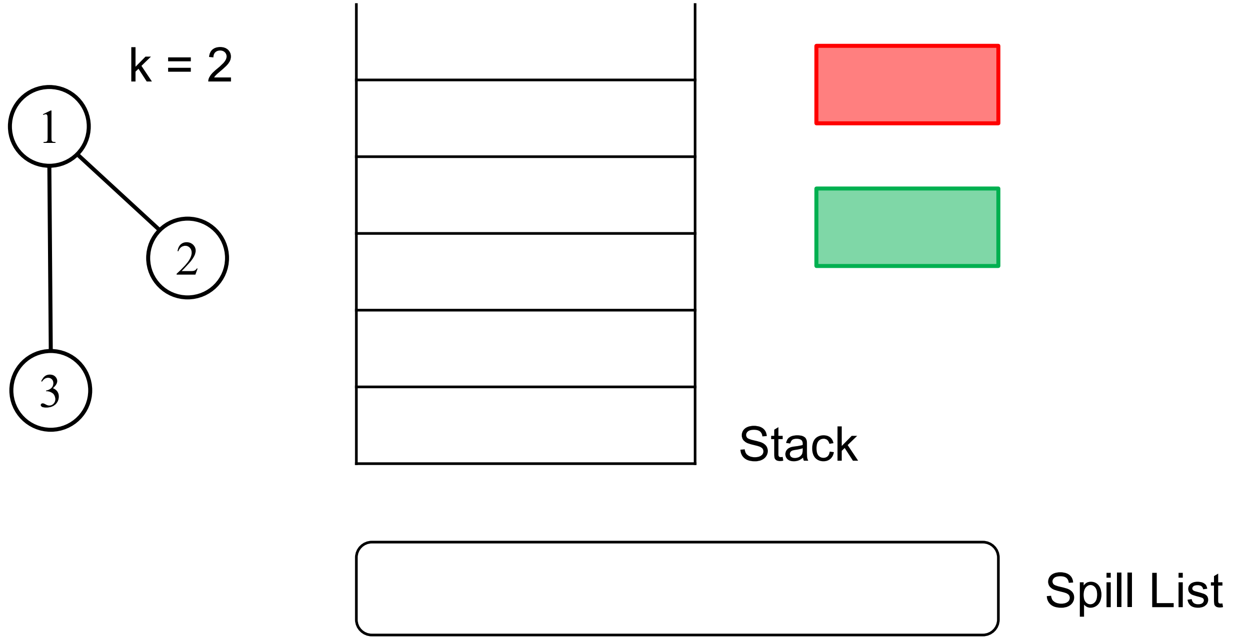

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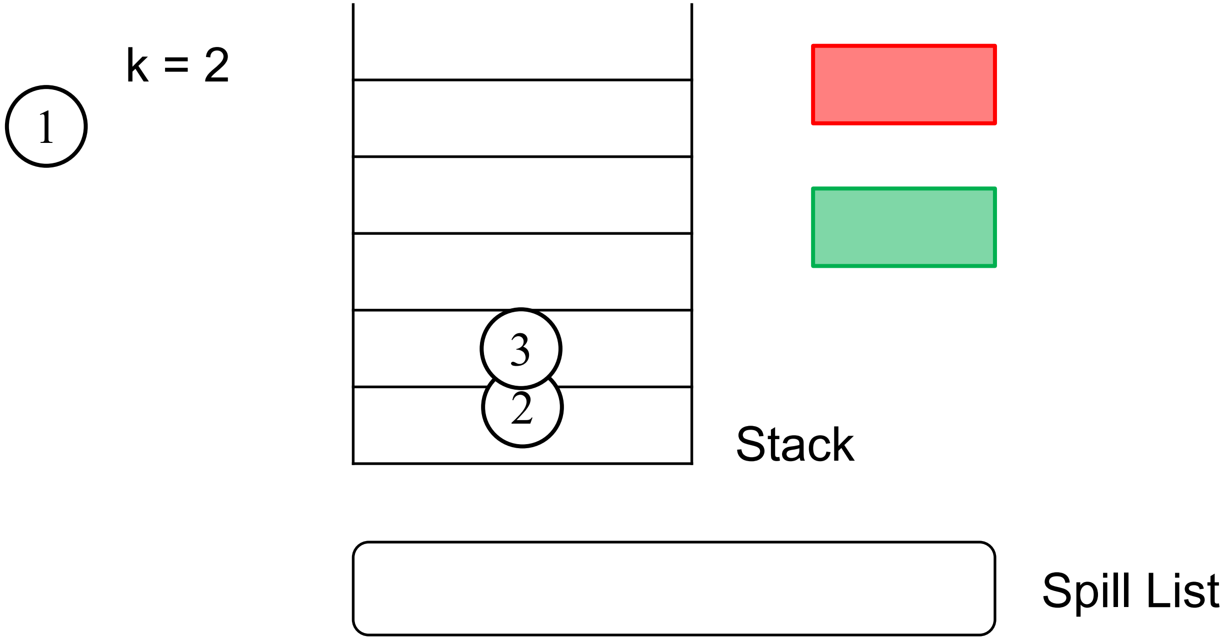

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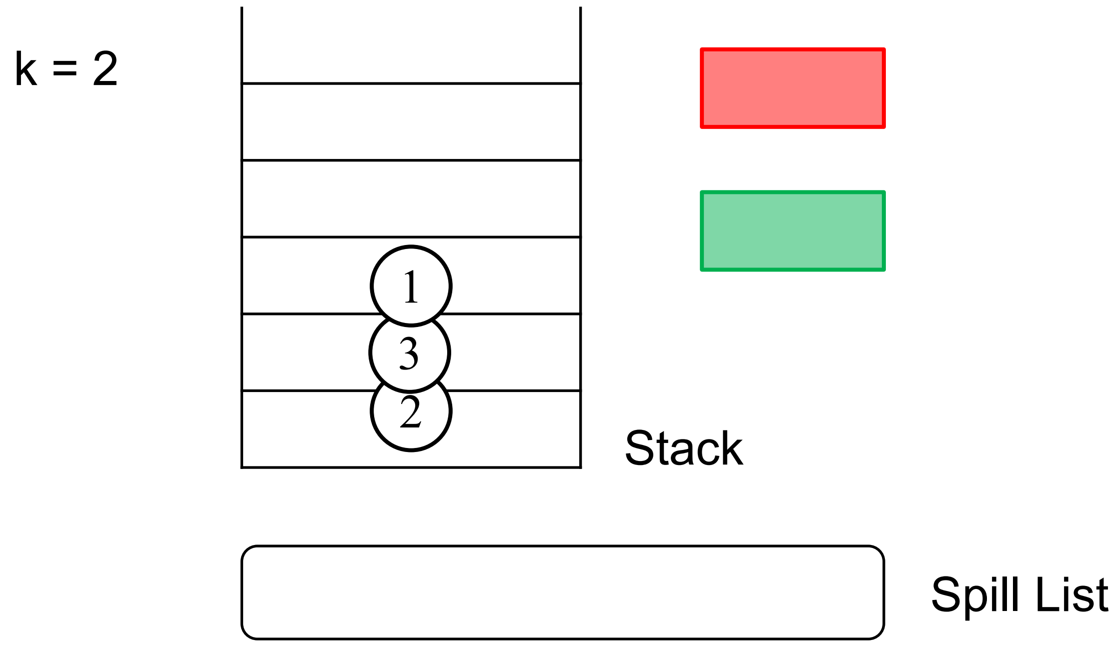

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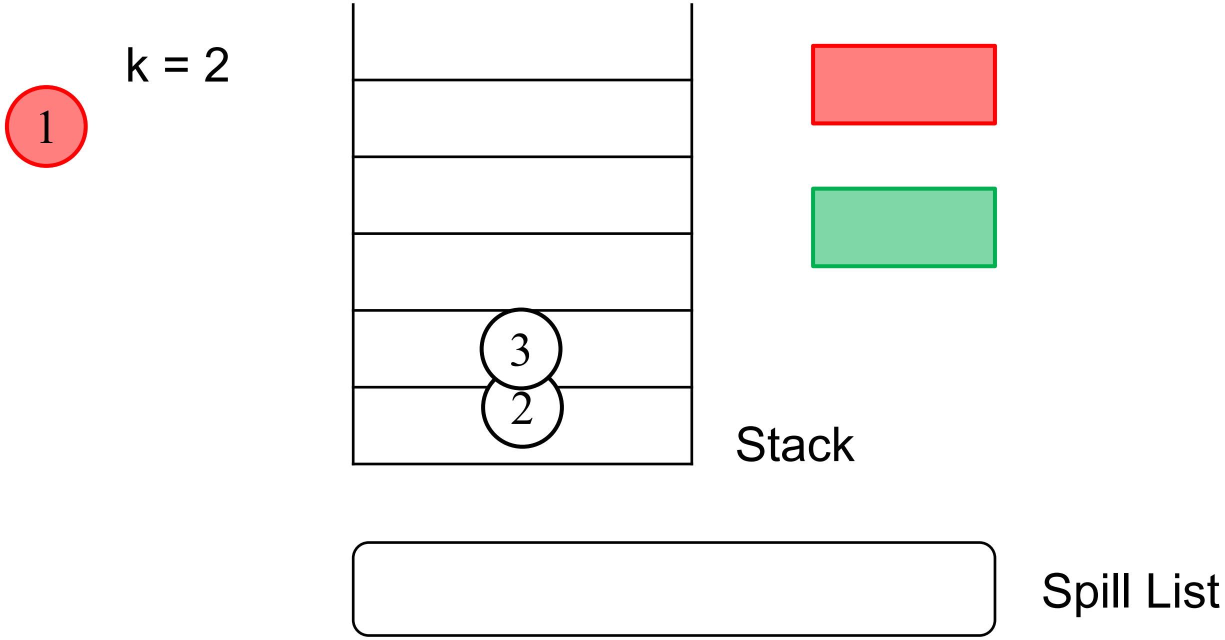
7.  ST    y    R2             // R1
8.  ST    z    R1             //
```



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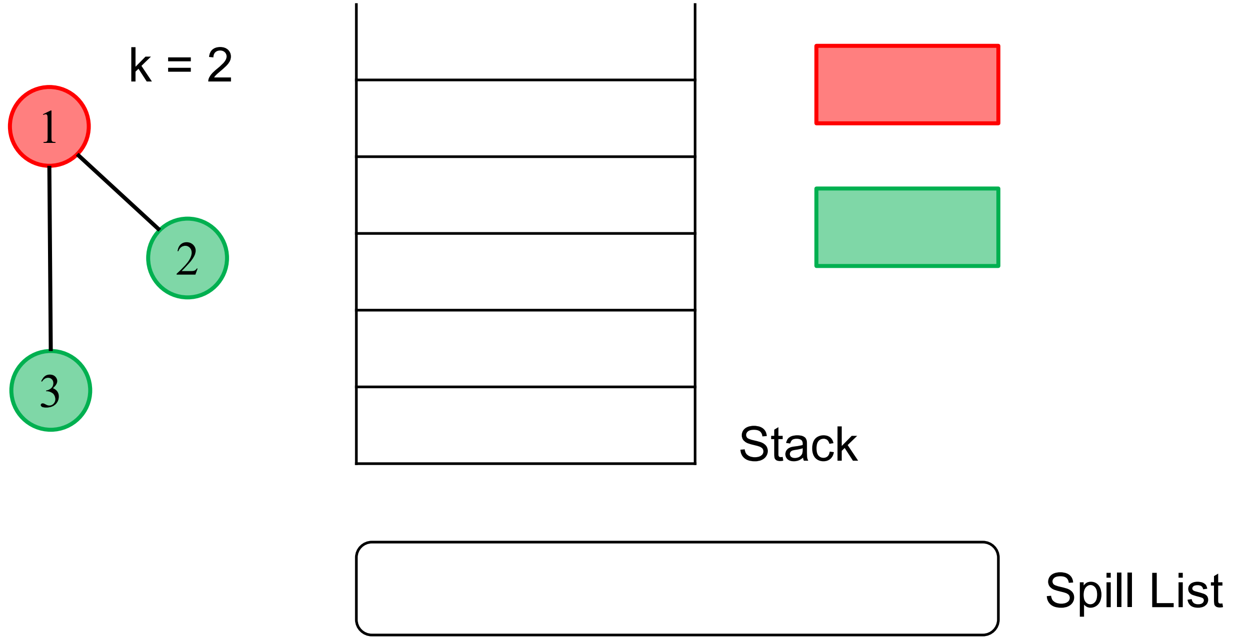

# Chaitin's Algorithm

Replace R1 with $R_{red}$
Replace R2/R3 with $R_{green}$

```
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3. ST   a   R2          // R1
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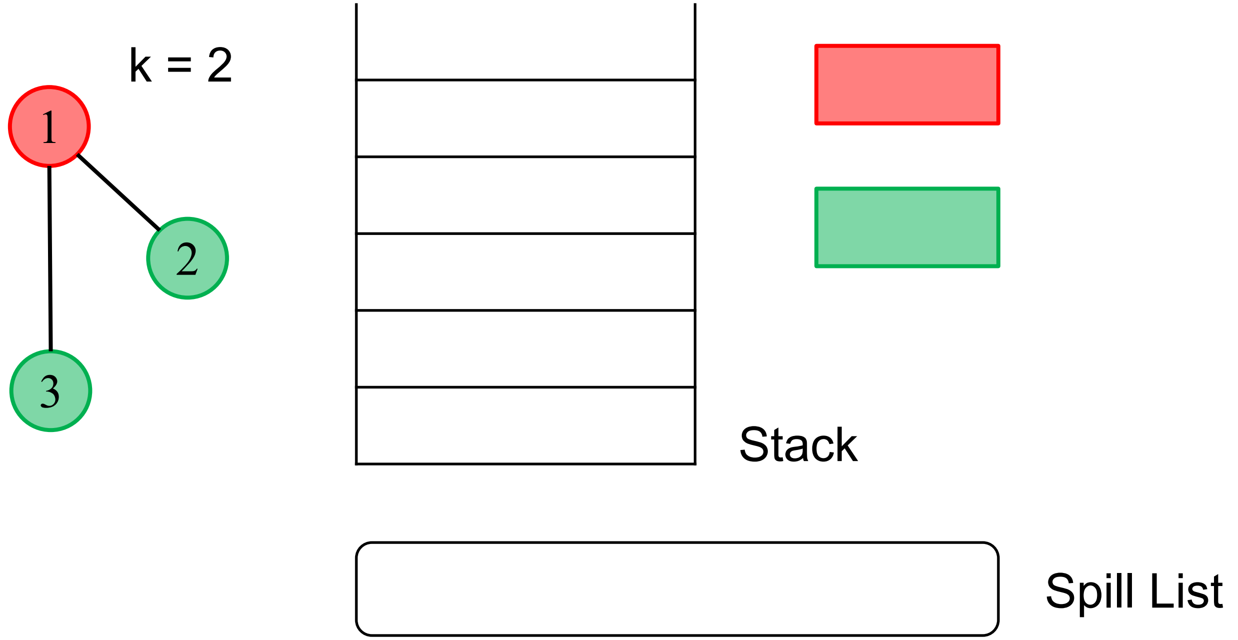

# Chaitin's Algorithm

Replace R1 with $R_{red}$
Replace R2/R3 with $R_{green}$

```
1. LD   Rred     #1028
2. LD   Rgreen   *Rred
3. ST   a        Rgreen
4. MUL  Rgreen   Rred     Rred
5. ST   x        Rgreen
6. LD   Rgreen   a
7. ST   y        Rgreen
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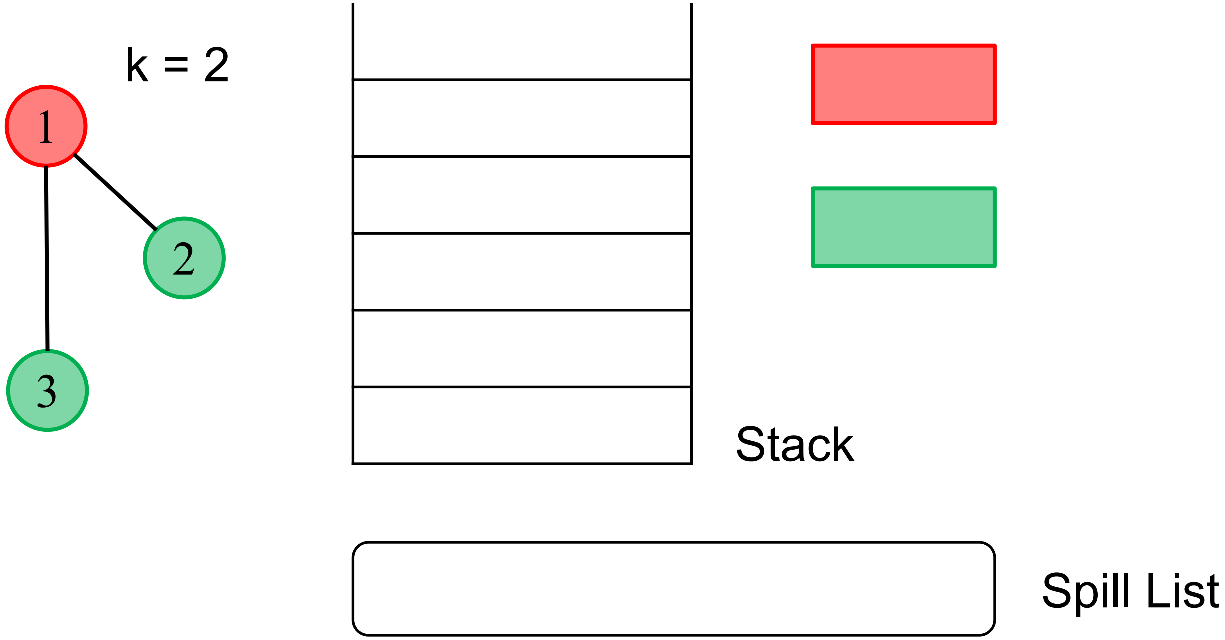
```



# Chaitin-Briggs Algorithm

- When Chaitin’s algorithm reaches a state where every vertex has a degree ≥ k
- Choose a vertex immediately to spill
  - put the vertex into a spill list
  - …

# Chaitin-Briggs Algorithm

- When Chaitin’s algorithm reaches a state where every vertex has a degree ≥ k
- Choose a vertex immediately to spill
  - put the vertex into a spill list
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- **Briggs**:
  - Degree of a vertex is a **loose** upper bound on colorability
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# Chaitin-Briggs Algorithm

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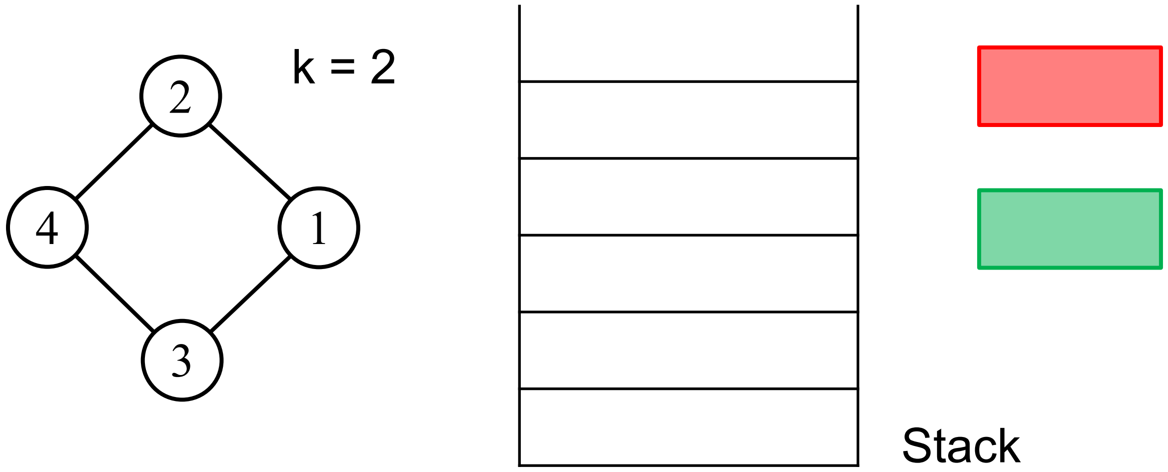
- **Briggs**:
  - Degree of a vertex is a **loose** upper bound on colorability
  - A vertex whose degree < k is **always** k-colorable
  - A vertex whose degree ≥ k **may also be** k-colorable

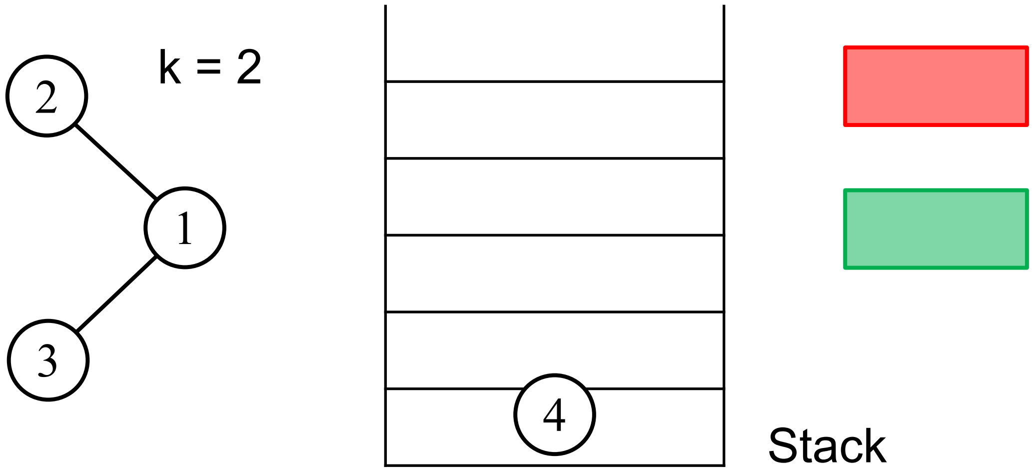
# Chaitin-Briggs Algorithm

- When Chaitin's algorithm reaches a state where every vertex has a degree ≥ k
- Choose a vertex immediately to spill
  - ~~put the vertex into a spill list~~
  - ~~…~~
- **Briggs**:
  - Push the vertex (to spill) to the stack.
  - We may have a color available when it is popped.

# Chaitin-Briggs Algorithm



# Chaitin-Briggs Algorithm



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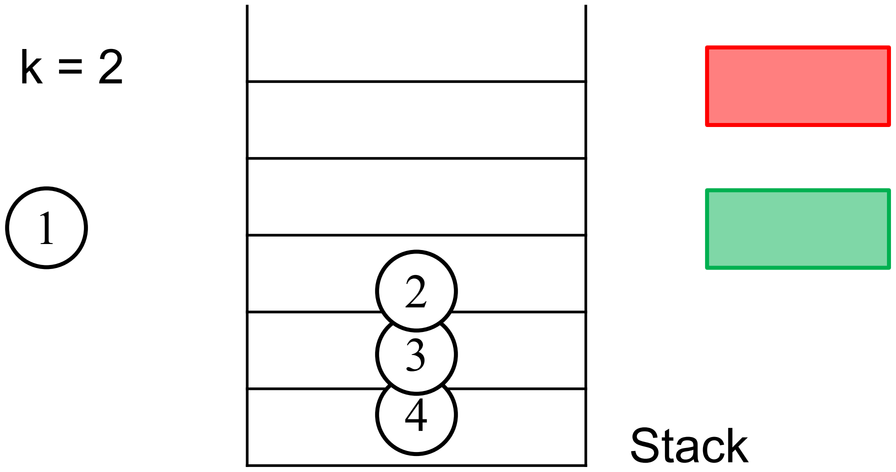

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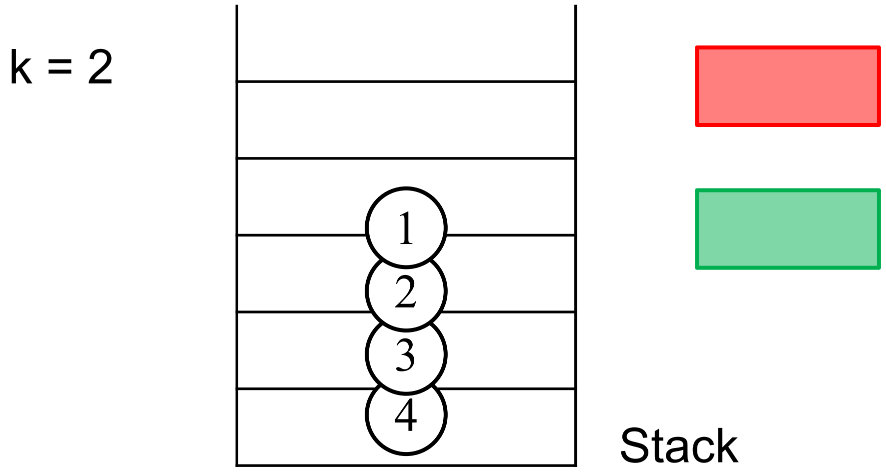

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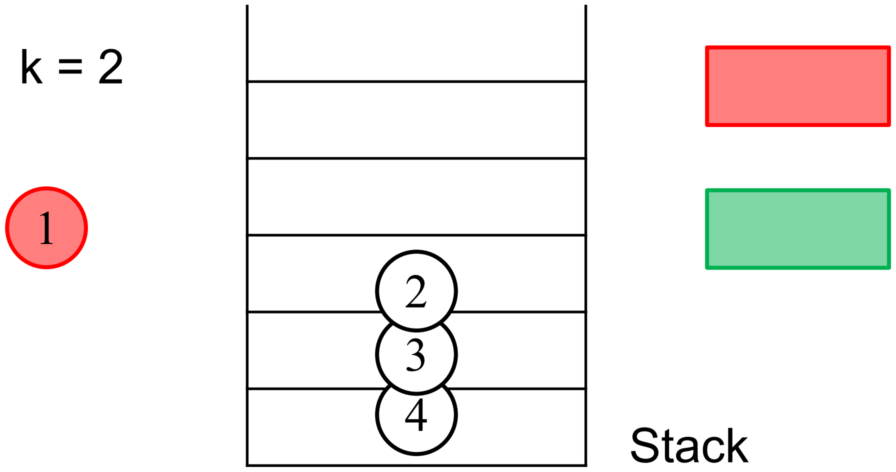

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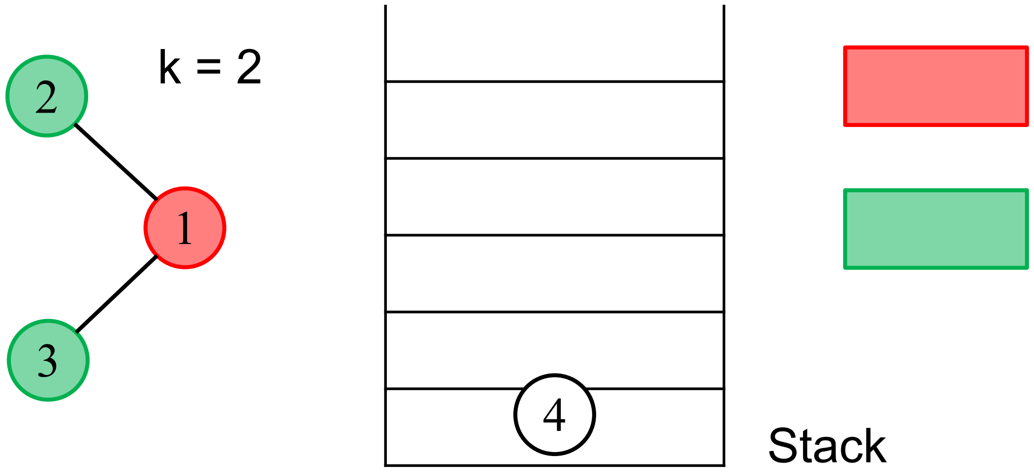

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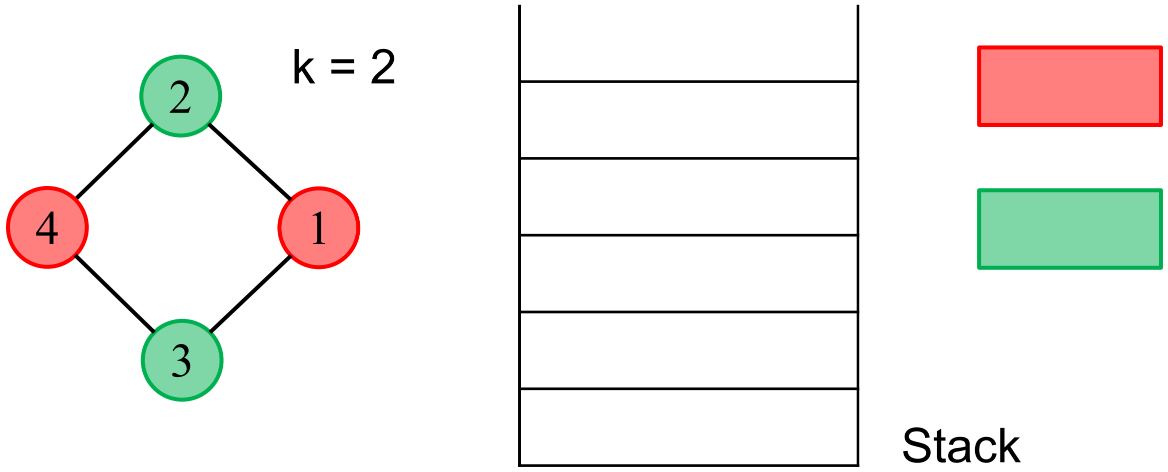

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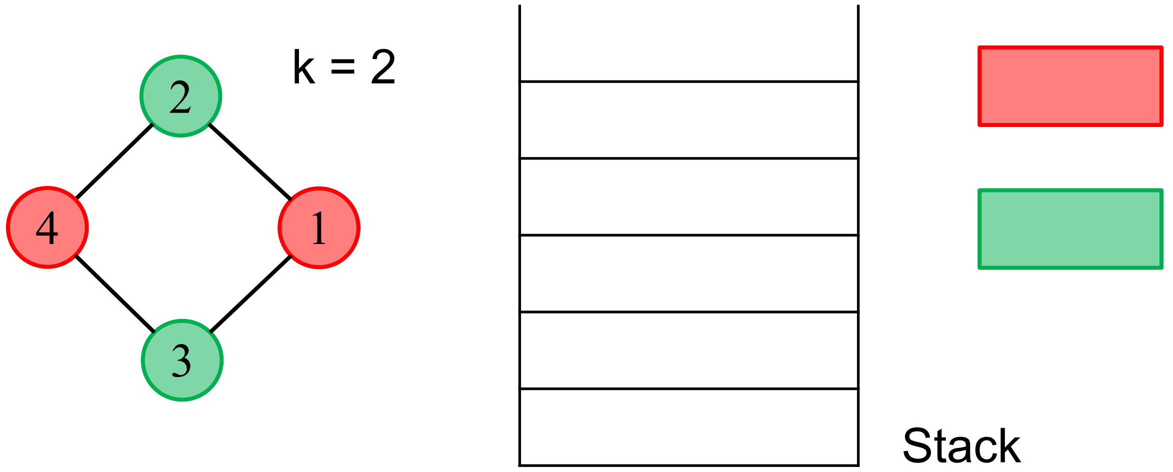
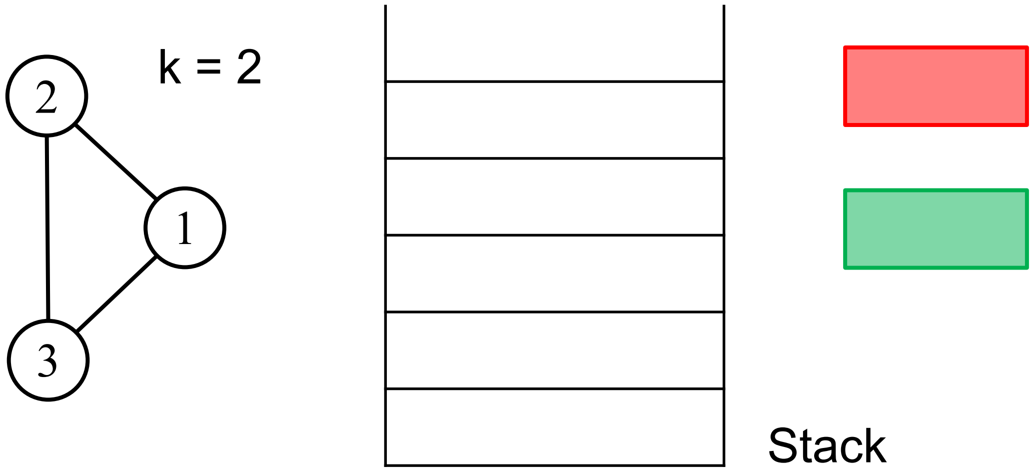



Sometimes, it is not necessary to spill!

# Chaitin-Briggs Algorithm



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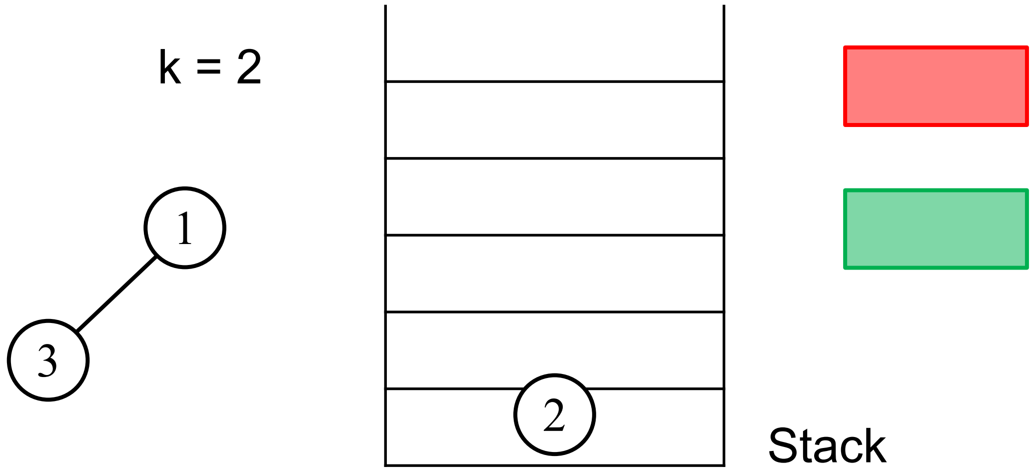

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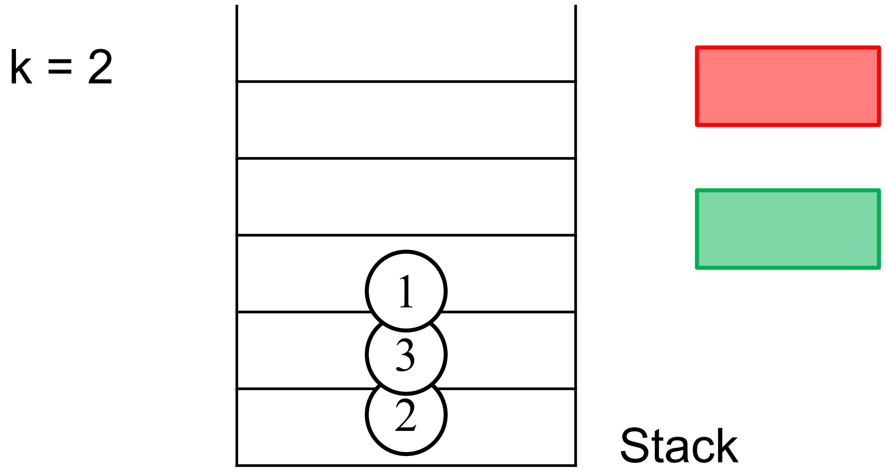

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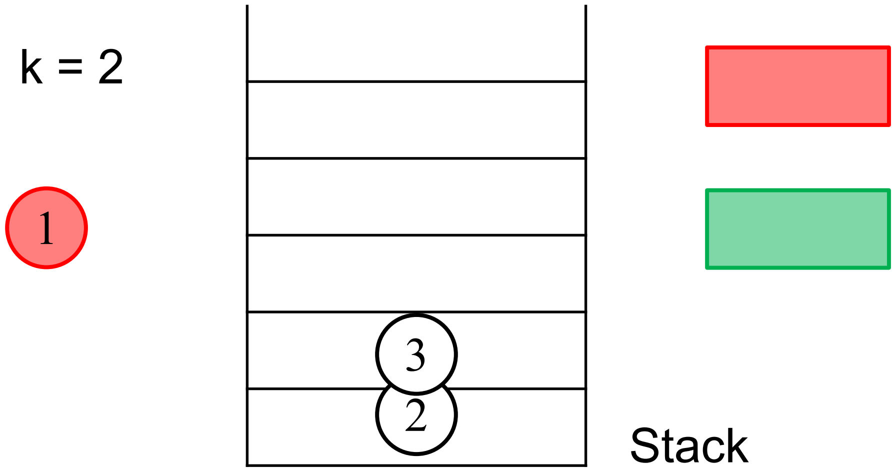

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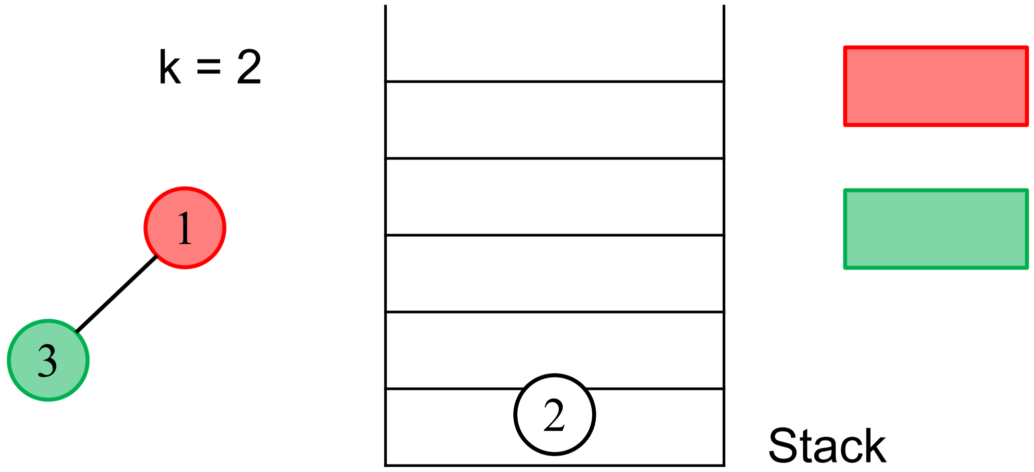

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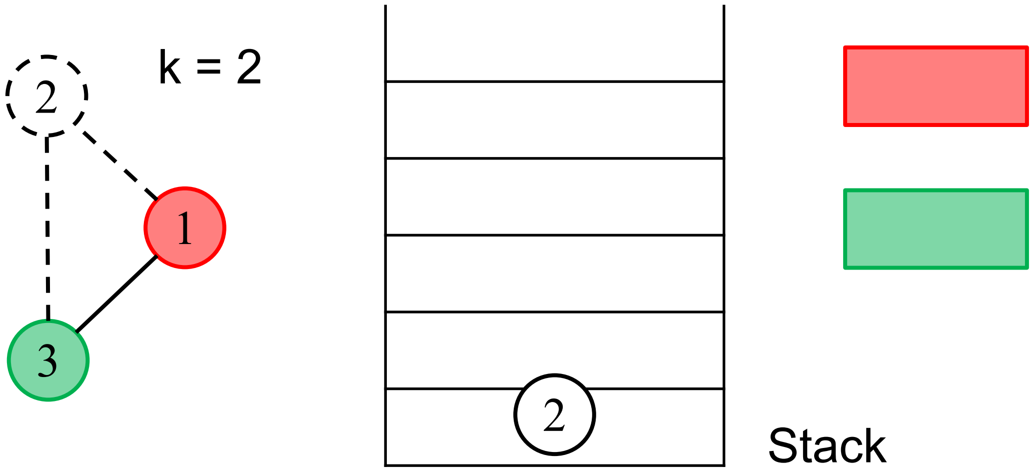


When there is not any available color, spill it.

# Chaitin-Briggs Algorithm

- Compared to Chaitin’s algorithm, Chitin-Briggs algorithm delays the spill operation
  - saves a spill list
  - reduces spill code

# Spill Candidates

- Minimize spill cost, *i.e.*, the loads/stores needed
  - *e.g.*, avoid inner loops

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# Spill Candidates

- Minimize spill cost, *i.e.*, the loads/stores needed
  - *e.g.*, avoid inner loops
- The higher the degree of a vertex
  - The greater the chance that spilling it will help coloring
- Don’t spill a value which is defined immediately followed by use
  - Spilling does not decrease live range

# Alternative Spilling

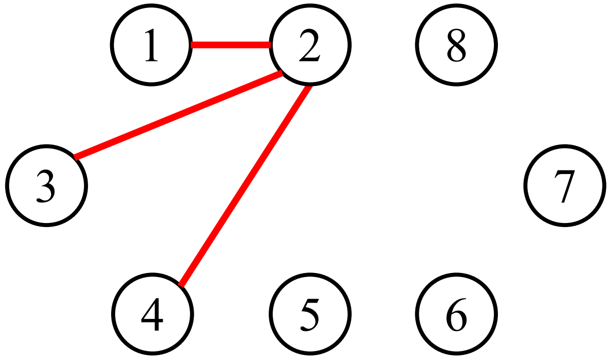
- Splitting Live Ranges, Coalescing Virtual Registers, etc.

# Alternative Spilling

- Splitting Live Ranges, Coalescing Virtual Registers, etc.

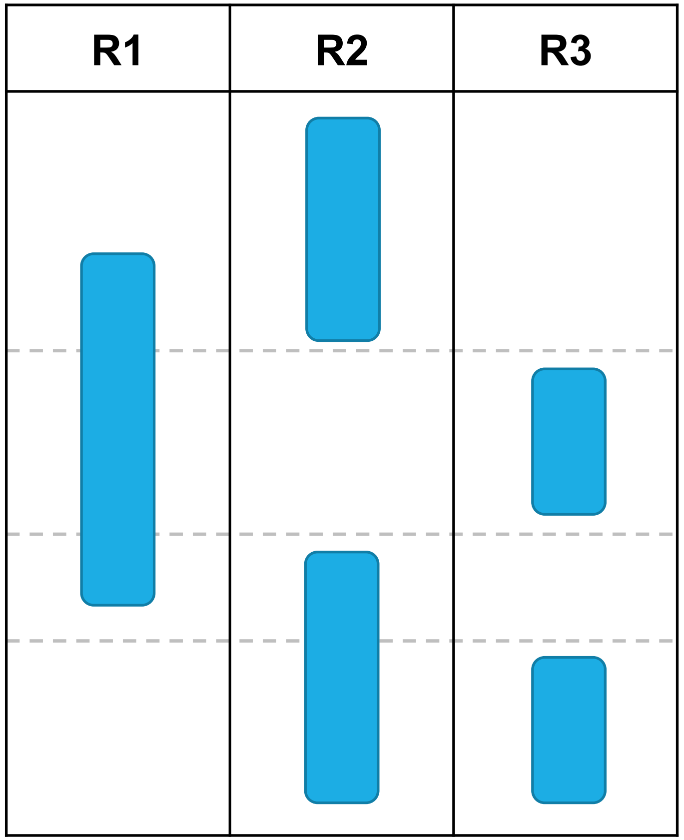
- Recall the **conflict graph**:

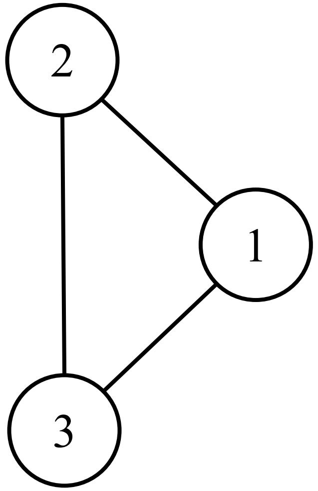
```
1. LD    R1    #1028        // R1
2. LD    R2    *R1          // R1 R2
3. MUL   R3    R1     R2    // R1 R2 R3
4. LD    R4    x            // R1 R2 R3 R4
5. SUB   R5    R4     R2    // R1    R3    R5
6. LD    R6    z            // R1    R3    R5 R6
7. MUL   R7    R5     R6    // R1    R3          R7
8. SUB   R8    R7     R3    // R1                   R8
9. ST    *R1   R8           //
```




**Conflict Graph**

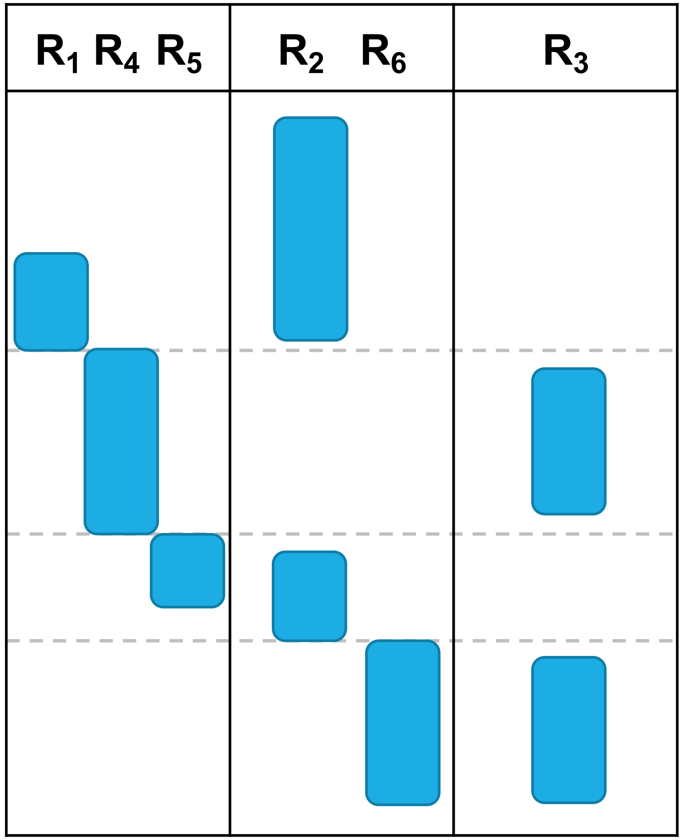
# Splitting Live Range

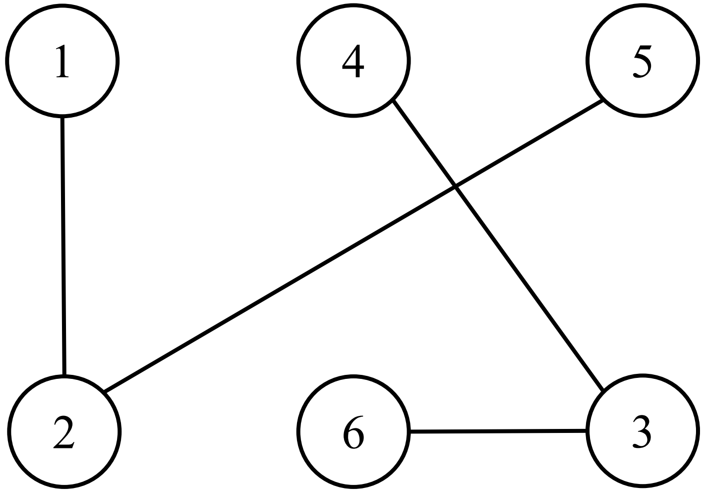



The conflict graph is not 2-colorable!

# Splitting Live Range

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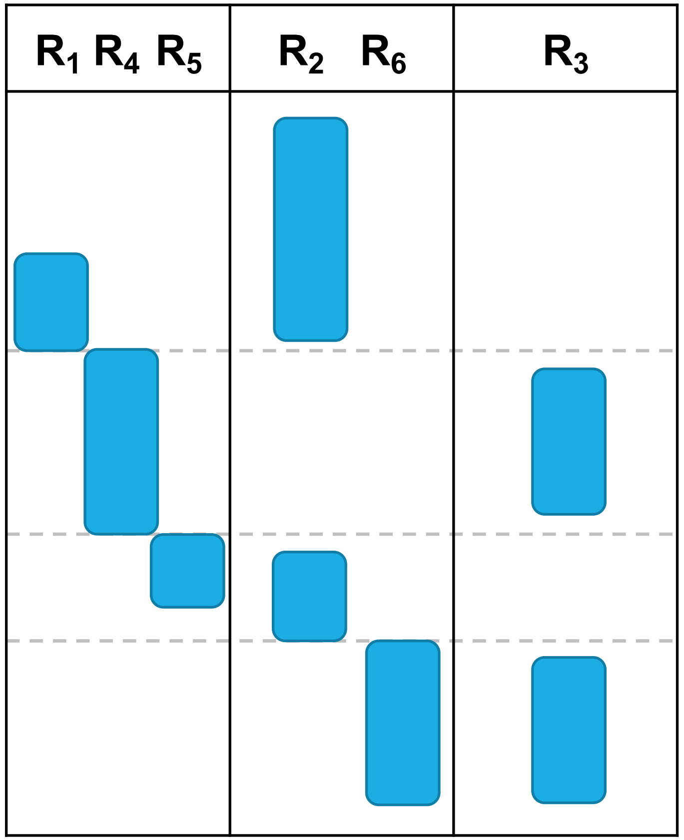
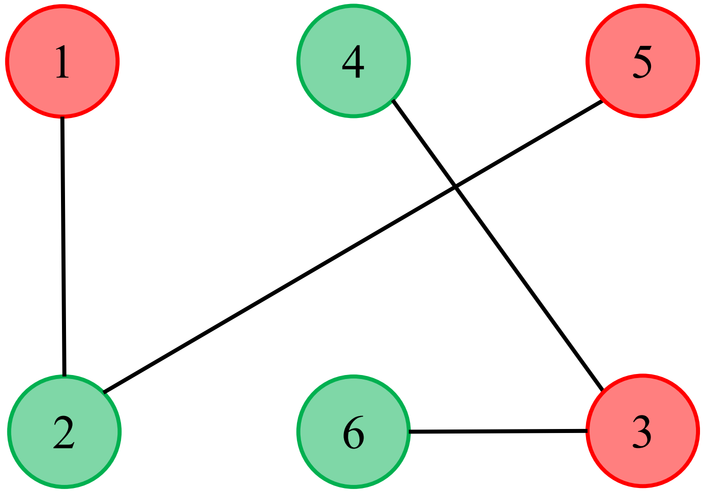
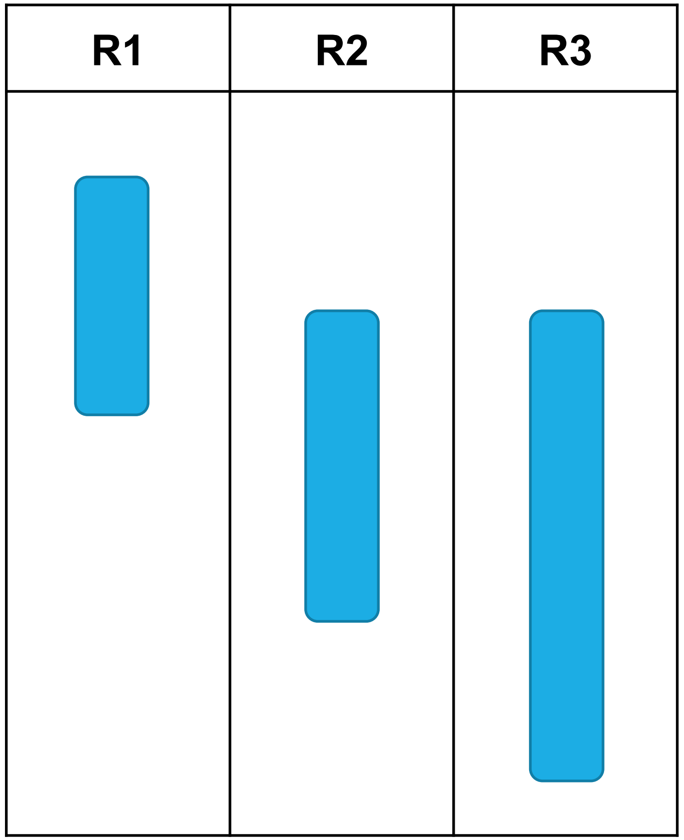
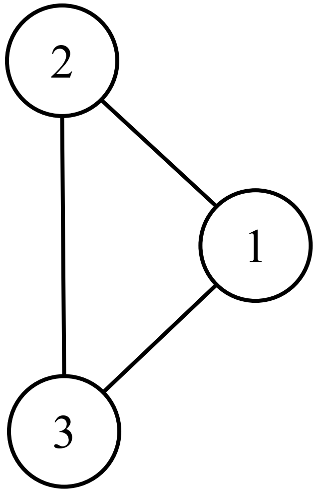



The conflict graph is 2-colorable!

# Coalescing Virtual Registers



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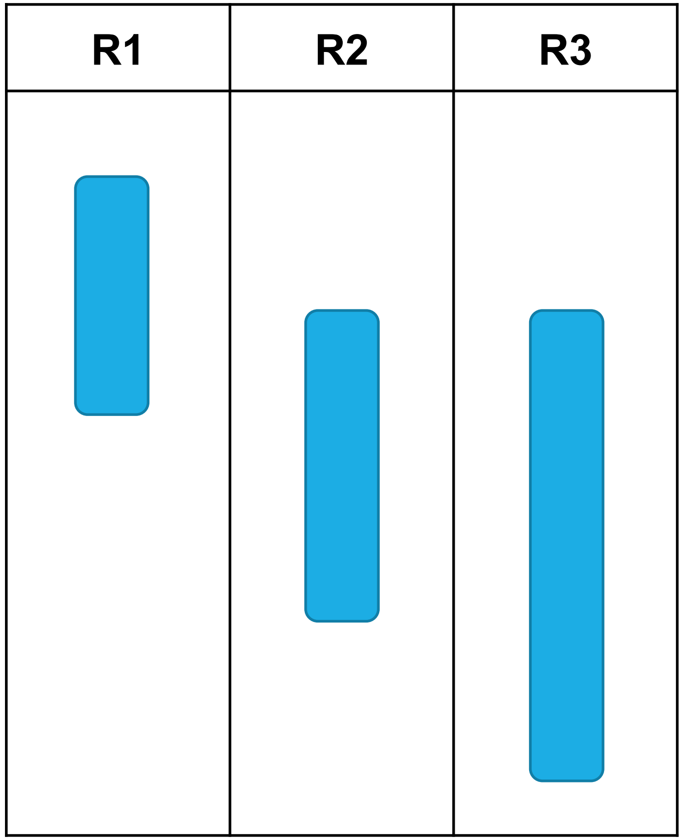
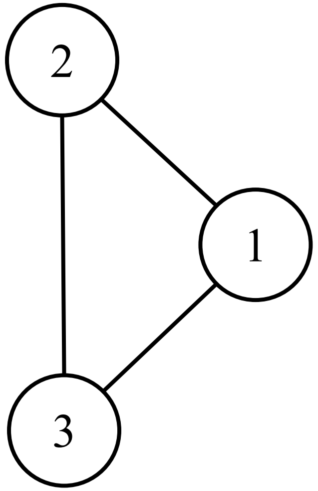



Assume R1 = R2 by LD R2 R1



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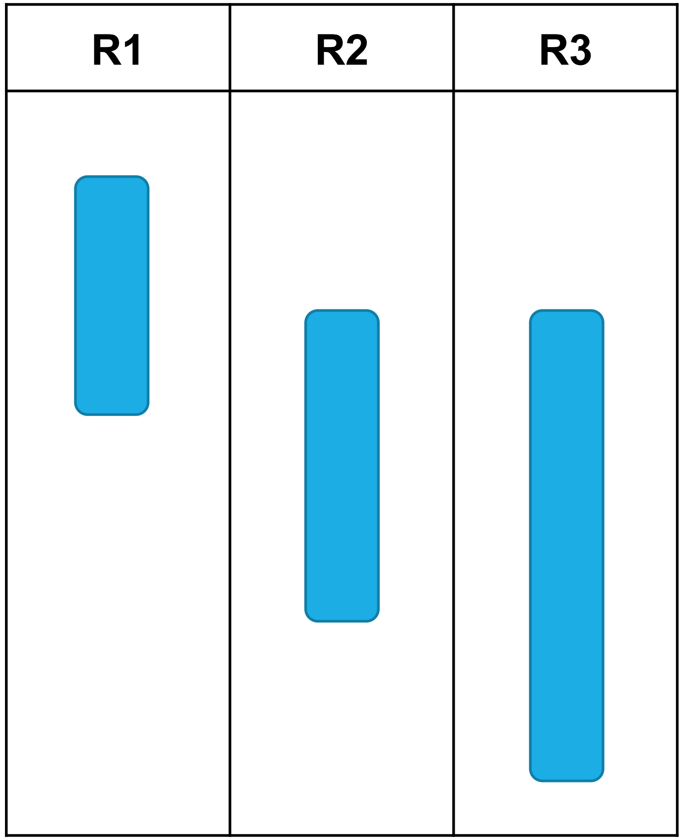


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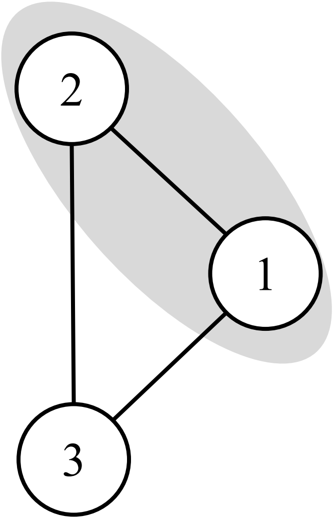

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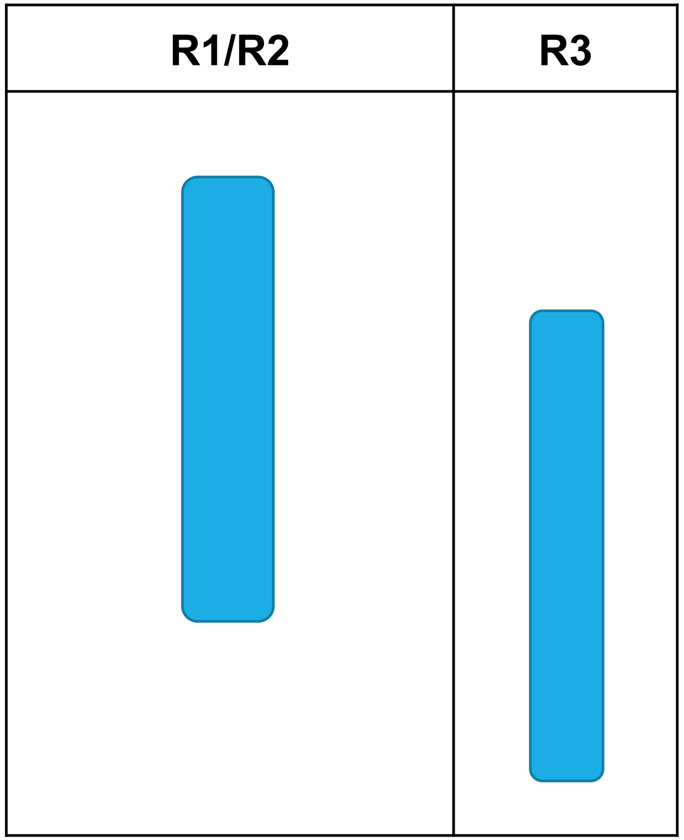


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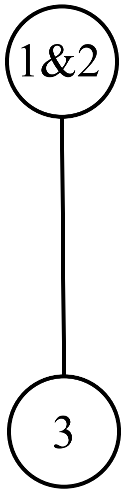

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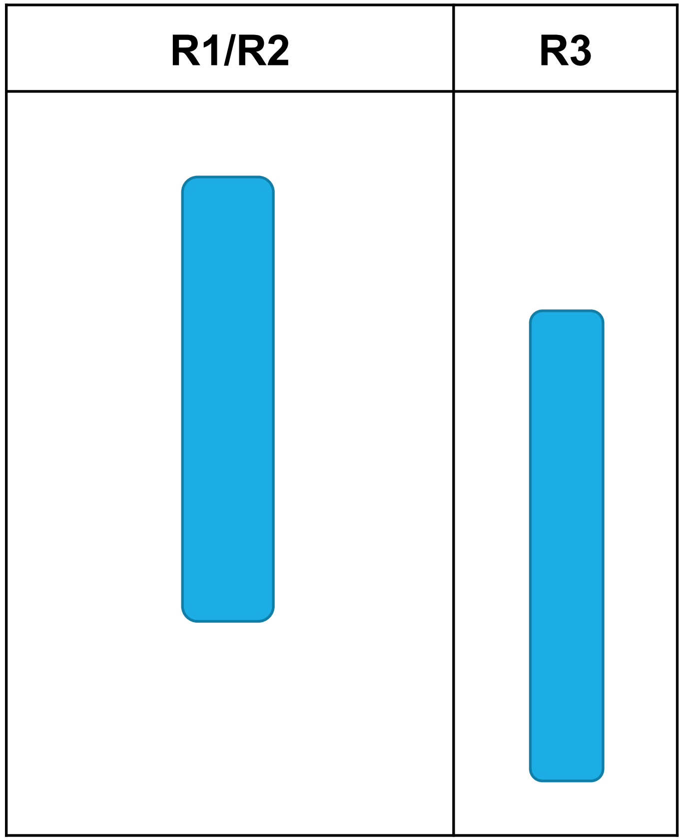


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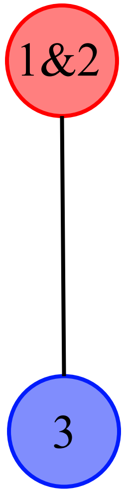
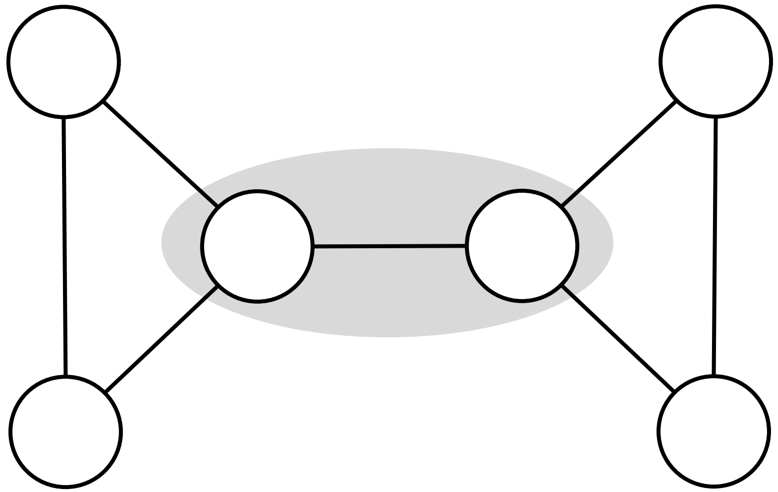


# Coalescing Doesn’t Always Work



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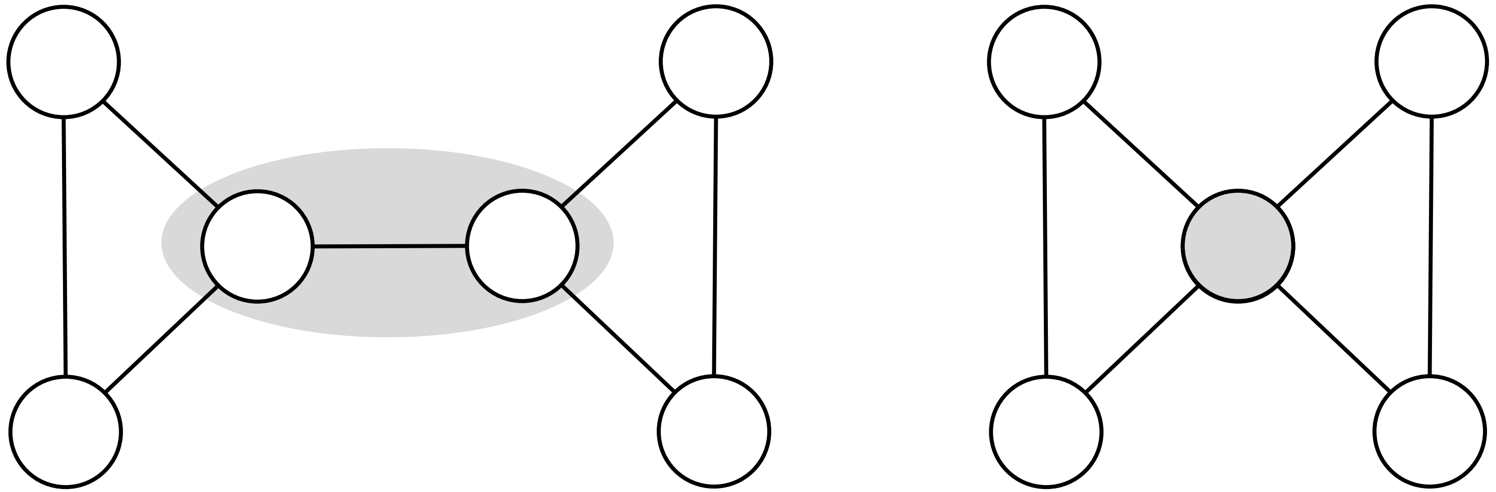

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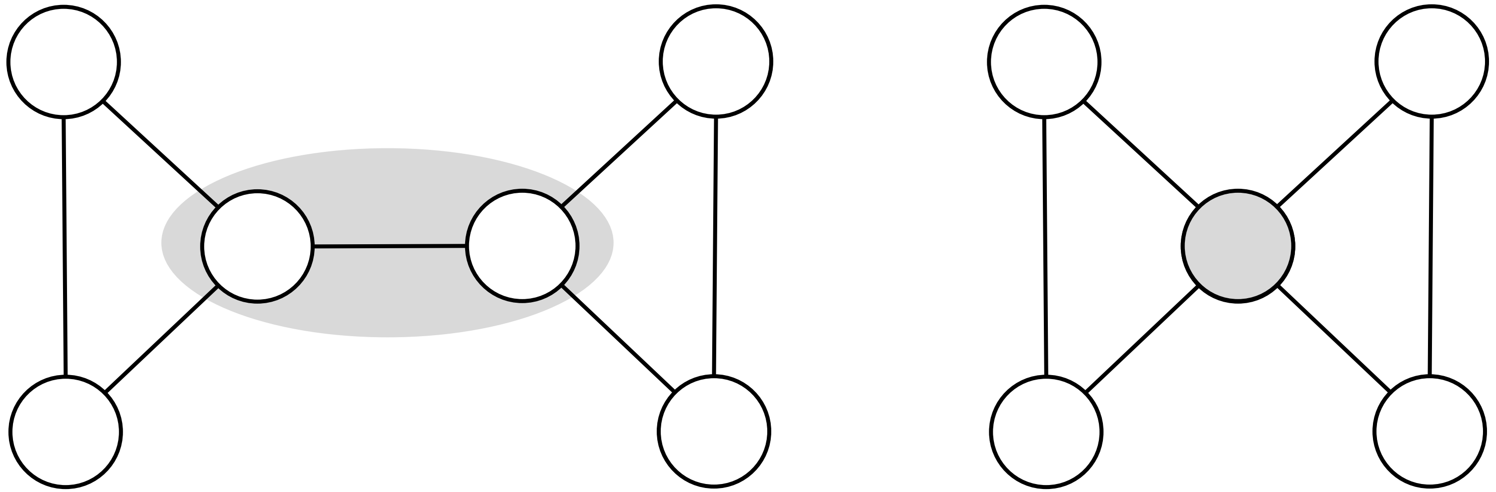
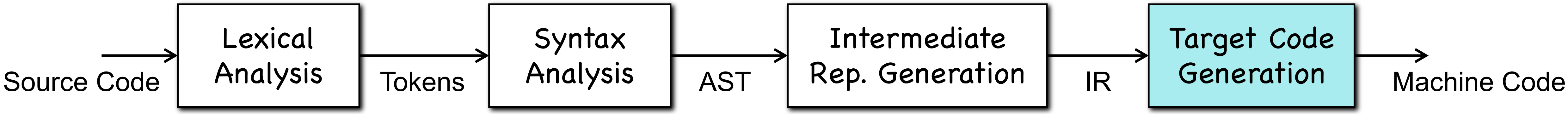


A vertex such that its degree < k is always k-colorable → Degree: 3 → 4
Harder to color

# Summary




- Speed: Registers > Memory
- Physical machines have limited number of registers
- **Register allocation**: ∞ virtual registers ➞ k physical registers
  - Part I – Local Register Allocation
  - Part II – Global Register Allocation

# THANKS!