The chassis for the IBM 1410 1411 CPU appears in manual 223-6900-2 (Customer Engineering Instruction - Reference: Standard Modular System) as SMS Module IV (Figures 15, 16 and 17 on pages 13 and 14). A similar diagram appears in the IBM 1410 System Fundamentals Customer Engineering Instruction Reference S223-2589 on page 104, figure 120. There is one notable error regarding row “T”, vs. Y and Z discussed below.

A 1411 CPU had four frames, named D, C, B and A from left to right as viewed from the wiring side. A frame Z with additional memory could be interposed between frames B and A, and a frame E with expanded features (e.g., 1412/1419 MICR support) could exist to the left of frame E. Frame A contained the power supplies, frame B contained memory.

There are 4 panels in a 1411 frame. From the wiring side, the top two are labeled 2 and 1, left to right, and the bottom two are labeled 4 and 3, left to right. At the bottom is an I/O panel, numbered 7 (not visible in the photo below).

Each of the four panels has rows A, B, C, D, E, F, G, H, J, K top to bottom, and each row has card slots 1 through 28, RIGHT TO LEFT from the wiring side.

Typically the two inside columns in each panel are often used to interconnect panels 1 with 2, and then 3 with 4 (these interconnect cables are on the card side, and thus are not visible in the photo below). Typically the two outside columns in each panel are often used to connect inter-frame cables for two adjacent frames.

The I/O panel has two rows, labeled U and L (for upper and lower, I suppose).

The documentation indicates there are four rows labelled “T”, one each at the bottom of panels 1 and 2, and the other two at the top of panels 3 and 4. HOWEVER, the ALDs tell a different story. In the ALDs it appears that the two at the bottom of panels 1 and 2 are labelled Z and the two at the top of panels 3 and 4 are labelled Y, based on the Edge Connector lists at the bottom of each ALD. An example is in the IBM 1410 System Fundamentals Customer Engineering Instruction Reference, S223-2589, figure 70 and page 74 (it was this that allowed me to deduce that the “T” was no longer accurate by the time the ALD’s were produced).

So in the Edge Connector lists one typically sees things like:

11C1Z07D --- 11C3Y07D (In 1411 frame C, a wire interconnect from the Z interconnect row D in column 07 to the Y interconnect row D, also in column 7).

11C1H28H --- 11D1H02H (A 1411 Frame C panel 1 to frame D panel 1, row H, interconnect – ~~which makes me wonder if one of those two frames had the panel numbering swapped left for right – because otherwise the two panels one would not have been adjacent. Something to watch for. It was this way in the actual ALD, as well.~~)

The panel labelling can be seen in this photo of an IBM 1410 that had resided at either Wisconsin DOT or the Department of Administration. Since this has the CE panel, the exposed frame is the “D” frame.



I am missing some things and noticed some “extra” things in my drawings. Things that are underlined are potentially serious – will have to be “re-engineered” from other sources, such as similar registers, the ILD’s, etc.

Volume 1 (Power – so this is not a big issue)

98.11.60.0 Universal Regulator Supply (Missing)

98.15.11.0 Processor Unit Meter (Present, not in index for Volume 1)

0473821 W/D (Wiring Diagram) Suffix A (Missing)

0473381 W/D Suffix ? (Missing)

0473491 W/D Suffix ? (Missing)

Volume 2

11.04.07.0 1411 Gate D Panel 2 (Sheet 1 is missing.)

11.04.07.3 1411 Gate D Panel 2 Cable and Edge Connector Location (Missing)

11.04.09.0 1411 Gate D Panel 4 (Duplicate sheet where Sheet 1 of Panel 2 should be)

11.10.26.1 Logic Gate Ring Extension X (Present, not in index)

11.40.01.1 Process Time Meter Controls (Present, not in index)

11.40.02.1 1\* Automatic Start (Present, not in index)

Volume 3

**12.30.04.1 2ND and 3RD Scan Ctrl (Missing)**

Volume 4

13.64.03.1 F CH Full Control (Missing)

13.64.09.1 7-8 Bit Even-Odd Parity Unit (Present, not in index)

13.65.01.1 1401 Error Latches (Apparently mislabeled as 13.65.01.2 in index)

13.72.07.1 F CH Fast File Controls (Present, not in index. Two sheets)

14.04.01.0 CKT CD Loc Chart 11B2 2 Sheets (Missing) **[BUT: See 25.04.01.0, Volume 9]**

Volume 5

14.18.04.1 Zone Adder 16K (The page after 14.18.05.1 appears to be another copy of 14.18.05.1, even though the name is hard to make out, the schematic matches the following page. The first of the two appears to be a later E.C. level. Appears to be for 1401 mode).

**14.30.01.1 1410 Logic (Missing. This and the next two are *not* covered in the ILDs)**

**14.30.02.1 1410 Logic**

**14.30.02.2 1410 Logic**

Volume 6

15.41.06.1 Channel Character Detection (Missing)

Volume 7

15.70.34.0 Reference Page 1410 To 7361 and 1311 (Present, not in index)

15.70.35.0 Reference Page 1410 To 1405 (Present, not in index)

Volume 8

Nothing missing or added.

Volume 9

25.04.01.0 Circuit Card Location Chart Frame 11 Gate B Panel 2 (Present, not in index)

25.04.02.0 Circuit Card Location Chart Frame 11 Gate B Panel 3 (Present, not in index)

25.04.03.0 Circuit Card Location Chart Frame 11 Gate B Panel 4 (Present, not in index)

25.22.03.1 Load Sharing Matrix Switch X 00-2 (Present, not in index)

25.42.03.1 Load Sharing Matrix Switch Y 00-2 (Present, not in index)

25.94.01.0 X-Address Line Termination Side D

25.94.02.0 X-Address Line Termination Side B

25.94.03.0 Y-Address Line Termination Side C

25.94.04.0 Y-Address Line Termination Side A

31.04.01.0 CKT CD Location Chart (Missing?)

31.04.02.0 Circuit Card Location Chart Frame 11 Gate B Panel 4 (Present, not in index)

35.10.01.1 Character Selection FEAT-ACC (Present, not in index)

Volume 10

40.10.03.1 Off-Normal Ind + Storage Scan S (two versions, different E.C. levels)

Circuit Card Location Chart Notes

* There are numbers (e.g., “4 5 6 7 \*”) at the bottom of some cells – I do not yet know what that means. (Example 11C1A02)
* If there are too many connections on a given card, it displays the page number in the chart, but not the coordinates of the gate on the chart – I am adding those back in manually.