

# S100D Datasheet

## Model S100D

- True VGA ToF camera module
- Compact design

S100D image



## Revision History

Rev.	Date	Ref. Page	Description
01	2020-09-09	-	Draft write
02	2021-01-21		Added I2C protocol Added register map Added embedded data information Data format change Added cover glass guide
03	2021-06-02	9, 22 29	Storage temperature, Rockchip information Host board connector
04	2021-07-15	36	Changed Host board connector
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06	2023-08-29	23 28 34~39	Change contents of Software Modifying information(mechanical drawings) Delete content related to U300

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## 1. Introduction

### 1.1. ToF 3D camera technology overview

3D time-of-flight (ToF) cameras illuminate an object or a scene with a modulated light source and observe the light reflected from the object. This is achieved via a laser diode illuminator and a receiver. The phase shift between the emitted light and reflected light is measured and translated to distance. This camera can measure an object's distance by pixel unit.

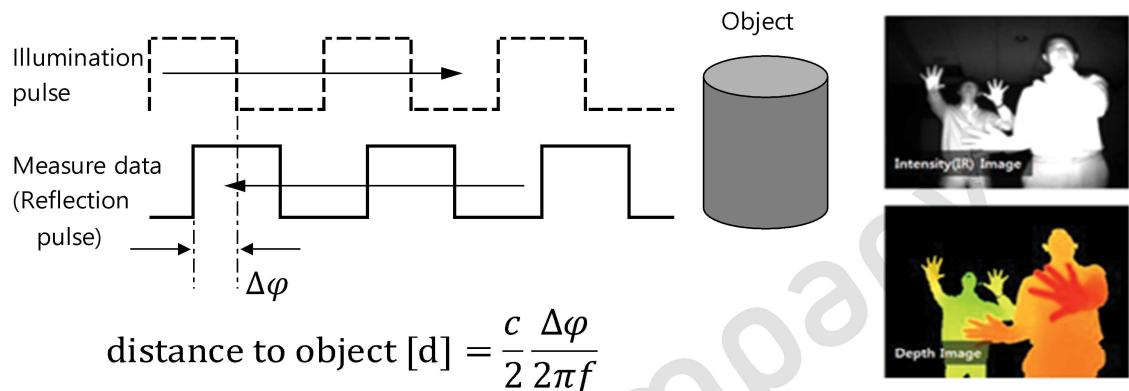


Figure 1 Principles of indirect Time of Flight

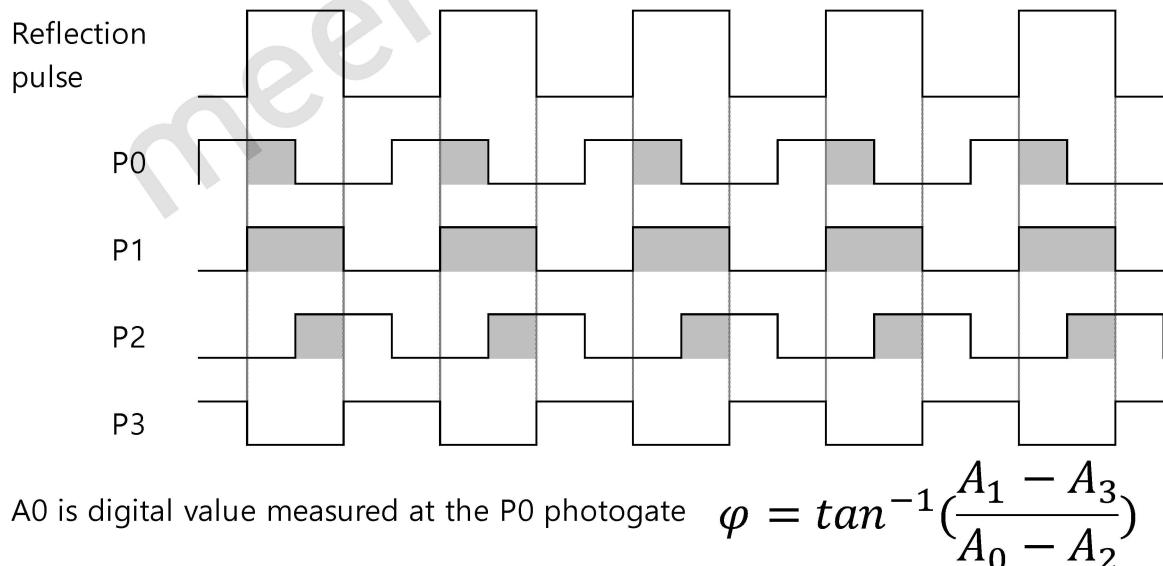


Figure 2 ToF demodulation using 4-phase sampling

## 1.2. System block diagram

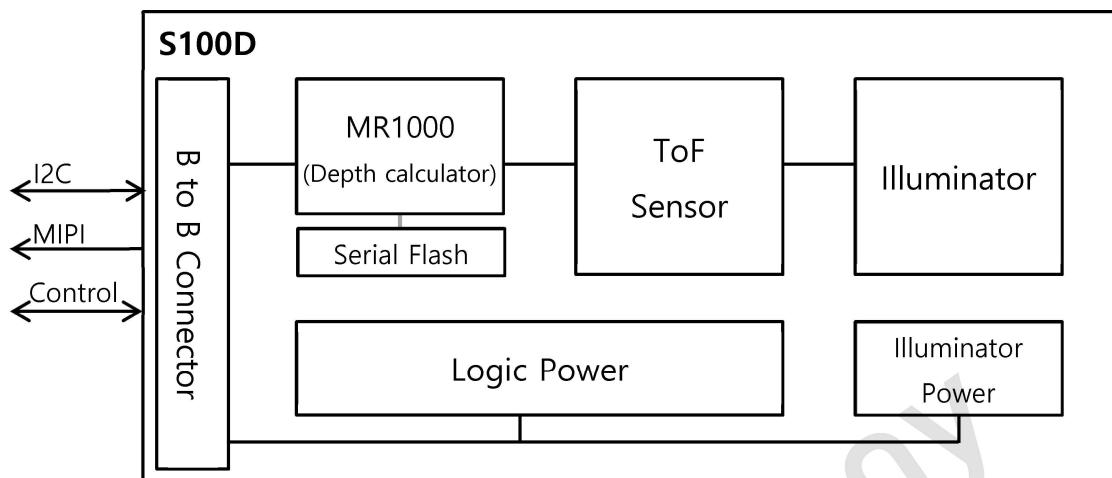


Figure 3 System block diagram

Parts	Summary
Illuminator	2W VCSEL(package with PD)
ToF sensor	VGA, 4 phase data out, global shutter
MR1000	Depth calculation
Serial Flash	MR1000 bootloader, calibration parameter
Power	Illuminator/Sensor/MR1000 Power
B to B Connector	Connector for host interface

Table 1 Main parts specification summary

## **2. General Specification**

### **2.1. Specification**

ToF Sensor			
Type of sensor	Samsung System LSI S5K33DXX		
Resolution	VGA (640x480), unit pixel size : 7.0 $\mu\text{m}$ x 7.0 $\mu\text{m}$		
ToF Illumination			
Source	2W VCSEL		
Wavelength	940 nm		
Modulation frequency	80 MHz, 100 MHz		
Measurement range	0.2 ~ 4.0 m (Principle range : ~ 7.5 m)		
ToF module Optics			
FOV (H x V)	60° x 45°		
F/number	1.4		
Accuracy			
0.2 ~ 0.5 m	< ±10 mm	※ Measurement condition - Target : flat screen of >70 % reflectivity - Target area : 7x7 central pixels - Number of data acquisition : 20 frames - Ambient illumination : normal indoor - Ambient temperature : 23 ~ 25°C	
0.5 ~ 4.0 m	< ±1% by distance		
Interface			
Control interface	I2C 400 Kbps		
Data interface	MIPI CSI-2 2 lanes, 500 Mbps/lane		
Power			
Input	DC 5V 3A		
Power consumption	Average 1.5 W, peak 15 W		
Temperature			
Operating temperature	0 ~ 40°C		
Storage temperature	-20 ~ 70°C		
Mechanics			
Dimensions	60.0 x 15.0 x 10.1 mm <sup>3</sup>		
Weight	4.9 g		

**Table 2 Information of general specification**

### **3. Component Specification**

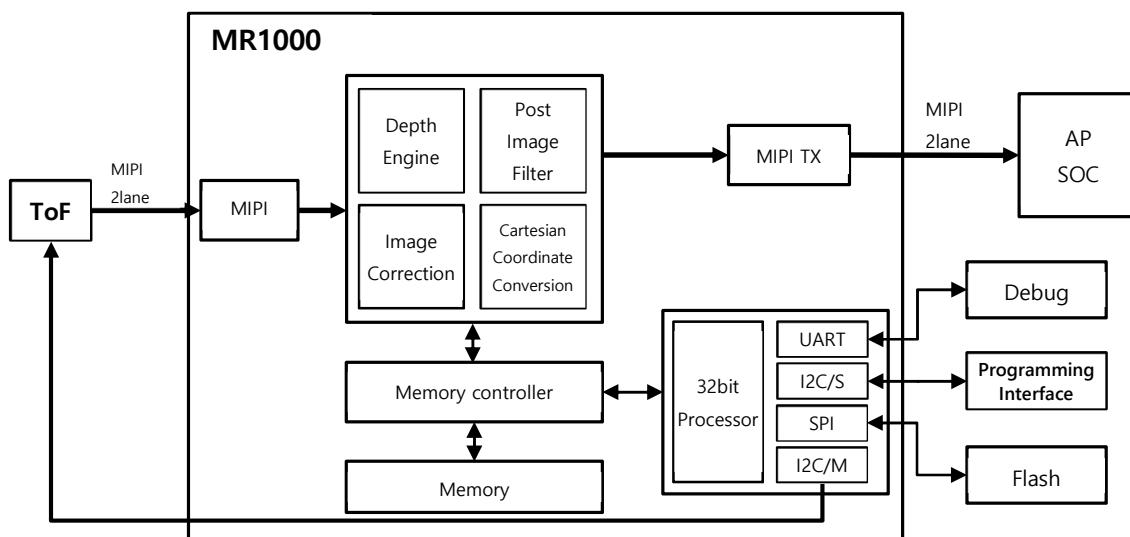
#### **3.1. Main component specification**

ToF sensor	VGA, 4:3 ratio, Active area 1/3.2"
	Electric global shutter
	ADC accuracy : 10-bit
ToF MR1000	Depth calculator, Max frame rate : 30fps
ToF illuminator	Illuminator wavelength : 940 nm
	SIP configuration : VCSEL, diffuser, VCSEL driver IC, PD
	Laser compliance : Eyesafety class 1
ToF Lens	F number : 1.4
	Focal Length : 3.92mm
	Horizontal Field of View : 60°
	Vertical Field of View : 45°
	Diagonal Field of View : 72°

**Table 3 Main components description**

#### **3.2. MR1000 calculating depth**

There are 2 lanes of each Rx/Tx of MIPI on-chip in MR1000. It also contains depth engine, image correction, post image filter, Cartesian coordinate conversion and memory for frame buffer as well as memory controller.



**Figure 4 MR1000 block diagram**

## **4. Functional Specifications**

### **4.1. MIPI CSI-2 output**

- Support MIPI DPHY v1.1 and MIPI CSI-2 v1.1 RAW10
- 80Mbps to 500Mbps with 2-lane selectable

### **4.2. High speed depth calculation using MR1000**

- Support resolution VGA
- Depth calculation in spherical coordinate
- Amplitude/Intensity data ouput
- Depth correction
- Temperature compensation
- Low motion blur(Single frequency mode)
- Noise/TNR/spatial filter selectable
- Cartesian coordinate conversion(Point cloud)

## 5. Operation

### 5.1. Initialization

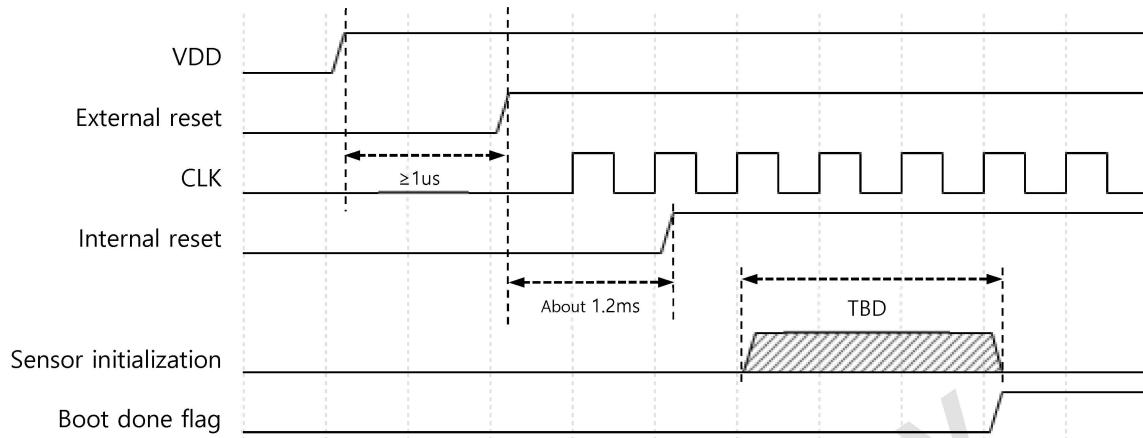


Figure 5 Power on sequence, sensor boot time

After power on, and when external reset is "High", CLK comes in and internal reset will be "High" after 1200 us (CLK at 24 MHz standard). All processes will work when the internal reset is high. Booting is complete if the status of the boot done flag is '1'. Proceed with protocol work after checking boot done register status.

### 5.2. Operation(Boot) Mode

Mode	Description	Switching time	Power consumption
S3	Sleep mode : Minimum power consumption	off → S3 100 ms under	280 mW
S2	Retention mode : Minimum boot time	S3 → S2 1150 ms	340 mW
S1	Stand-by mode : Active ready	S2 → S1 290 ms	430 mW

Table 4 Operation mode description

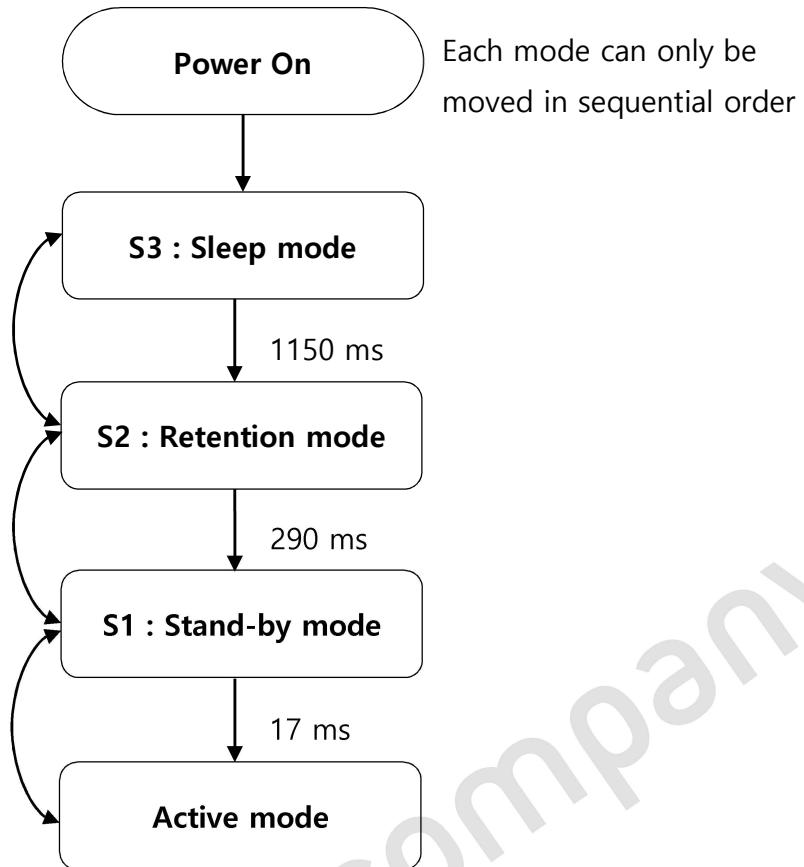


Figure 6 Boot mode diagram

## 6. I2C Control Protocol

### 6.1. Protocol description

Description	Start		Length		CMD		Address					Check sum		Data
Size(Byte)	2		2		2		4					2		0~63
Byte order	0	1	2	3	4	5	6	7	8	9	10	11	12-76	
	L	H	L	H	L	H	L	H	L	H	L	H	L-H	

Table 5 Protocol header

Action	Start	Length	CMD	Address	Check sum	Data
Register setting	0xB0A1	0x0002	0x0006	0x0000****	0x0000	0x****
Illumination	0xB0A1	0x0001	0x0007	0x00000000	0x0000	1:ON, 0:OFF
MIPI TX Mode	0xB0A1	0x0001	0x0009	0x00000000	0x0000	0 : 2560 1 : 1280 2 : 640
MIPI TX reset	0xB0A1	0x0001	0x000A	0x00000000	0x0000	1
Auto exposure	0xB0A1	0x0001	0x000C	0x00000000	0x0000	1:ON, 0:OFF
Sleep mode	0xB0A1	0x0001	0x000D	0x00000000	0x0000	0 : Active 1 : S1 2 : S2 3 : S3
Register reset (default)	0xB0A1	0x0001	0x000E	0x00000000	0x0000	1

Table 6 Protocol action

## 6.2. Example

Slave address 0xE0 (Write)

0xE1 (Read)

Ex1) Register write (address 0x1122, data 0x33445566)

Protocol name	Slave	Start		Length		CMD		Address				Check sum	Data	
	-	0	1	2	3	4	5	6	7	8	9	10	11	12
Byte order(Write)	-	0	1	2	3	4	5	6	7	8	9	10	11	12
Register write	0xE0	0xA1	0xB0	0x01	0x00	0x06	0x00	0x22	0x11	0x00	0x00	0x00	0x00	0x66554433
Illumination on	0xE0	0xA1	0xB0	0x01	0x00	0x07	0x00	0x00	0x00	0x00	0x00	0x00	0x00	1
MIPI TX mode 0	0xE0	0xA1	0xB0	0x01	0x00	0x09	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0
MIPI TX reset	0xE0	0xA1	0xB0	0x01	0x00	0x0A	0x00	0x00	0x00	0x00	0x00	0x00	0x00	1
Auto exposure on	0xE0	0xA1	0xB0	0x01	0x00	0x0C	0x00	0x00	0x00	0x00	0x00	0x00	0x00	1
Auto exposure off	0xE0	0xA1	0xB0	0x01	0x00	0x0C	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0
Sleep mode active	0xE0	0xA1	0xB0	0x01	0x00	0x0D	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0
Sleep mode S1	0xE0	0xA1	0xB0	0x01	0x00	0x0D	0x00	0x00	0x00	0x00	0x00	0x00	0x00	1

Table 7 Protocol write

Protocol name	Slave	Address				Slave	Return size	Description
Byte order(Write)	-	0	1	2	3	-	-	
Register read	0xE0	0xA1	0xB2	0x11	0x22	0xE1	4	read address(0x2211)
Product name	0xE0	0xA1	0xB3	0xF0	0xF2	0xE1	8	000S100D(ASCII)
Firmware version	0xE0	0xA1	0xB3	0xF1	0xF2	0xE1	5	year/month/day/major/minor
Serial number	0xE0	0xA1	0xB3	0xF2	0xF2	0xE1	6	
Boot done	0xE0	0xA1	0xB3	0xF1	0xF1	0xE1	1	0 : not boot, 1 : boot

Table 8 Protocol read

## 7. MIPI Interface

### 7.1. MIPI TX specification

- MIPI D-PHY 1.17 Nov 2011 compliant
- Forward (Unidirectional) high-speed only (LPDT/ULPS not support)
- HS diff. swing 200mV, HS common level 200mV
- Raw 10 data type supported
- Resolution mode
  - mode 0 : 2560x961
  - mode 1 : 1280x961
  - mode 2 : 640x961
- Frame rate : 30 fps
- MIPI CSI-2 2-lane (500Mbps/lane)
- First line : embedded frame head

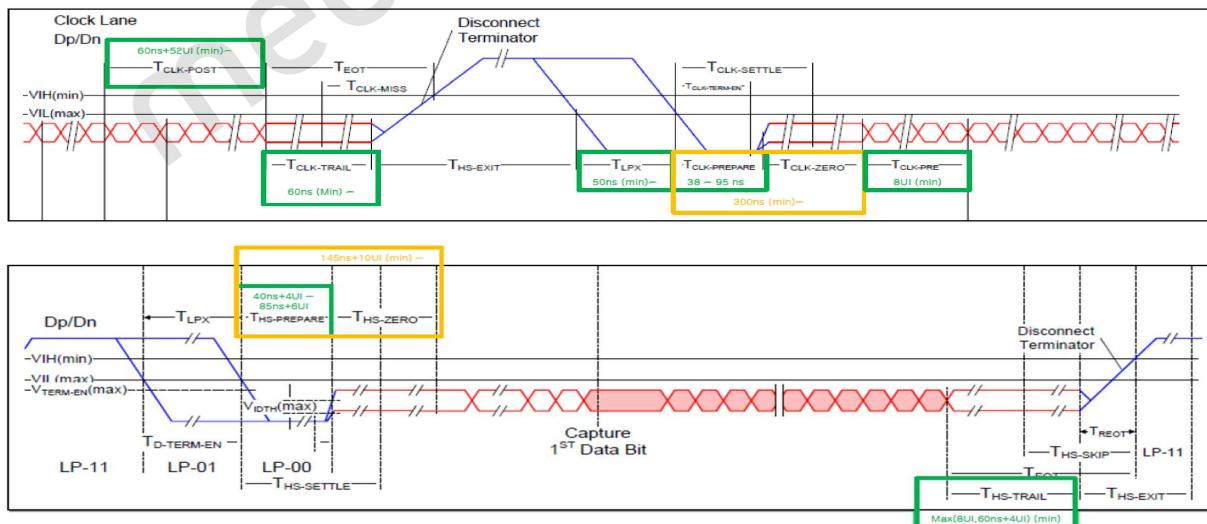


Figure 7 MIPI TX operation TX signal timing

## 8. Register Map

### 8.2. Register information

\*1 : filter3    \*2 : remove flying pixel    \*3 : filter2    \*4 : filter1    \*5 : filter3\_ctrl

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default value	Access						
0x0028	amp_max_limit										amp_min_limit										0xFFFF0000						R/W													
0x0029	depth_max_limit										depth_min_limit										0xFFFF0000						R/W													
0x002A	scat_threshold										Reserved										0x00000200						R/W													
0x0030	depth_error_threshold																				0xFFFFFFFF						R/W													
0x0031	Reserved										*1 *2 *3 *4						0x0DAC000F						R/W																	
0x0033	Reserved										g_offset						0x80000000						R/W																	
0x0039											flying_pixel_threshold										0x0000FFFF						R/W													
0x003A											temporal_mblur						0x02000020						R/W																	
0x003B											mci_thresh						0x00000000						R/W																	
0x003D	multi_freq_ctrl																				0xFF000C80						R/W													
0x0042	*5																				0x00001D4C						R/W													
0x0046	set_tx_mode	data_format_sel	vcycle_dly								hcycle_dly						0x10003032						R/W																	
0x0041		firm_rev_no																			-						R													
0x00AD											BD						-						R																	
0x0127	Reserved										mci_flag						-						R																	

Table 9 Register information

### 8.3. Register description

#### 8.2.1. Amplitude threshold control registers

Register Name	Address	Bit	Default	Description
amp_max_limit	0x0028	[31:16]	0xFFFF	More than the set value, depth = 0 if(amplitude > amp_max_limit) depth = 0 else depth = depth
amp_min_limit	0x0028	[15:0]	0x0000	Less than the set value, depth = 0 if(amplitude < amp_min_limit) depth = 0 else depth = depth

Table 10 Amplitude threshold register setting

### 8.2.2. Depth threshold control registers

Register Name	Address	Bit	Default	Description
depth_max_limit	0x0029	[31:16]	0xFFFF	More than the set value, depth = 0 if(depth > depth_max_limit) depth = 0 else depth = depth
depth_min_limit	0x0029	[15:0]	0x0000	Less than the set value, depth = 0 if(depth < depth_min_limit) depth = 0 else depth = depth

**Table 11 Depth threshold register setting**

### 8.2.3. Scattering threshold control registers

Register Name	Address	Bit	Default	Description
scat_threshold	0x002A	[31:16]	0xFFFF	scat amplitude = Internally calculated value if(scat amplitude < scat_threshold) depth = 0 else depth = depth
Reserved	0x002A	[15:0]	0x0200	Do not change

**Table 12 Scattering threshold register setting**

### 8.2.4. Depth error threshold control registers

Register Name	Address	Bit	Default	Description
depth_error_threshold	0x0030	[31:0]	0xFFFFFFFF	error coefficient = Internally calculated value if(error coefficient > depth_error_threshold) depth = 0 else depth = depth

**Table 13 Depth error threshold register setting**

### 8.2.5. Image filter control registers

Register Name	Address	Bit	Default	Description
Reserved	0x0031	[31:16]	0x0DAC	Do not change
Reserved	0x0031	[0]	0x1	Do not change
Reserved	0x0042	[15:0]	0x1D4C	Do not change
filter 3	0x0031	[4]	0x0	noise filter 3 on/off 1 = on, 0 = off
filter3_ctrl	0x0042	[31]	0x0	noise filter 3 change 1 = gaussian filter, 0 = default filter
remove flying pixel	0x0031	[3]	0x1	remove flying pixel on/off 1 = on, 0 = off
flying pixel_threshold	0x0039	[15:0]	0xFFFF	flying pixel coefficient = Internally calculated value if(flying pixel coefficient > flying pixel_threshold) depth = 0 else depth = depth
filter 2	0x0031	[2]	0x1	noise filter 2 on/off 1 = on, 0 = off
filter 1	0x0031	[1]	0x1	noise filter 1 on/off 1 = on, 0 = off

**Table 14 Image filter register setting**

### 8.2.6. Depth offset control registers

Register Name	Address	Bit	Default	Description
Reserved	0x0033	[31:16]	0x8000	Do not change
g_offset	0x0030	[15:0]	0x0000	Global offset value, Adds or subtracts from the depth value according to the set value (scale : 1mm).

**Table 15 Depth offset register setting**

### 8.2.7. Motion blur control registers

Register Name	Address	Bit	Default	Description
temporal_mblur	0x003A	[7:0]	0x20	Temporal motion blur weight The motion blur is reduced as smaller input value (Input value range : 0x00 ~ 0xFF) As the input value decreases, the deviation of depth increases.
multi_freq_ctrl	0x003D	[31:23]	0x30	Multi-frequency motion blur weight The motion blur is reduced as smaller input value (Input value range : 0x00 ~ 0xFE) When set to 0xFF, multi-Frequency motion blur is completely removed, but aliasing always occurs. As the input value decreases, aliasing for moving objects increases.
multi_freq_ctrl	0x003D	[22:16]	0x01	Do not change

**Table 16 Motion blur register setting**

### 8.2.8. Multi camera interference control registers

Register Name	Address	Bit	Default	Description
mci_thresh	0x003B	[12:0]	0x00	mci threshold value mci_flag is generated by comparing the difference value between a the previous frame and the current frame. The difference value is the average value of a specific area. if ( frame (N-1) - frame(N)  > mci thres value) mci_flag = '1' else mci_flag = '0'
mci_flag	0x0127	[3:0]	0x00	mci_flag consists of 4 bits, and each bit is the area information as follows. mci_flag[0] : area 1(left up side) mci_flag[1] : area 2(right up side) mci_flag[2] : area 3(left down side) mci_flag[3] : area 4(right down side)

**Table 17 Multi camera interference reducing register setting**

### 8.2.9. Output data format control registers

Register Name	Address	Bit	Default	Description
set_tx_mode	0x0046	[31:28]	0x1	MIPI TX Resolution Selection 0x1 : XYZA 2560 * 961 0x2 : ZA 1280*961 0x4 : Z 640* 961
data_format_sel	0x0046	[0]	0x0	set_dist_sel[0] : Depth Output Selection 0x1 : R(Radial distance) 0x0 : Z(Point cloud)
		[1]	0x0	set_dist_sel[1] : Amplitute Output Selection 0x0 : Amplitute 0x1 : Intensity
		[3:2]	0x0	set_dist_sel[3:2] : MIPI TX Frame Selection 0x1 : 15 Fps 0x2 : 7.5 Fps default : 30 Fps
vcycle_dly	0x0046	[23:12]	0x000	vertical delay value Use it when setting the MIPI TX mode.
hcycle_dly	0x0046	[11:0]	0x000	horizontal delay value Use it when setting the MIPI TX mode.

**Table 18 Output data format register setting**

### 8.2.10. Information register

Register Name	Address	Bit	Default	Description
firm_rev_no	0x0041	[27:16]	0x21	firmware version information
BD	0x00AD	[0]	0x1	Boot status information 0x01 : idle, 0x01 : Boot done
sleep mode	TBD	TBD	TBD	sleep mode status information

**Table 19 Module information register**

## 9. System Integration

### 9.1. System level block diagram

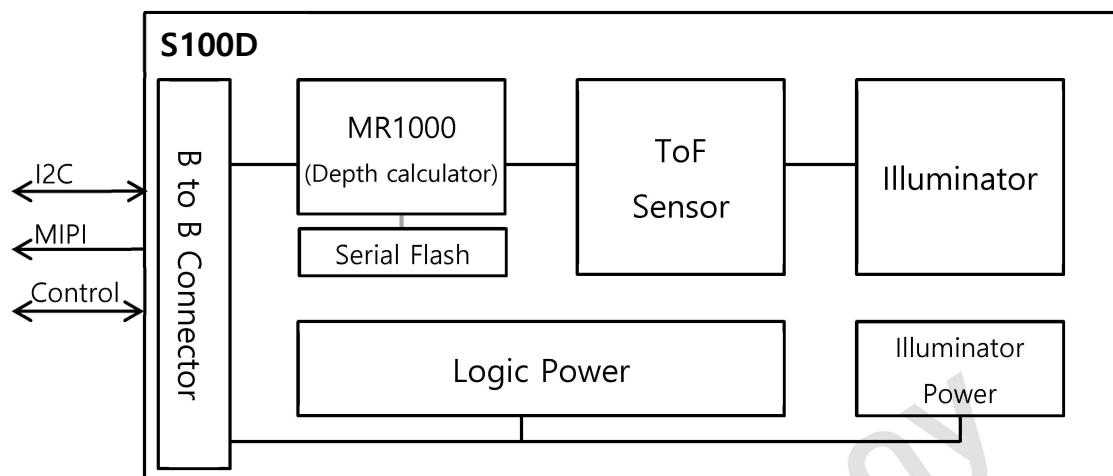


Figure 8 S100D system block diagram

### 9.2. System power

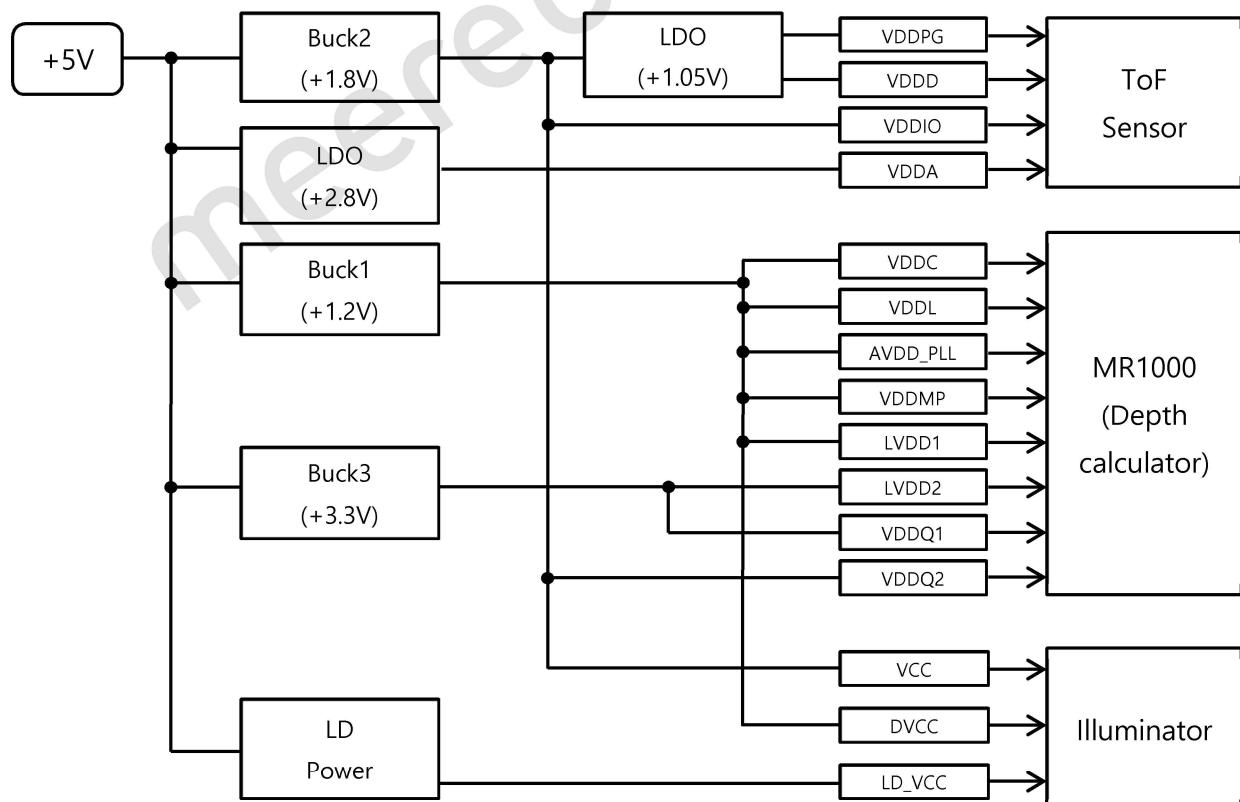


Figure 9 S100D system power

### 9.3. B to B connector pin map(BBR50-04001-001)

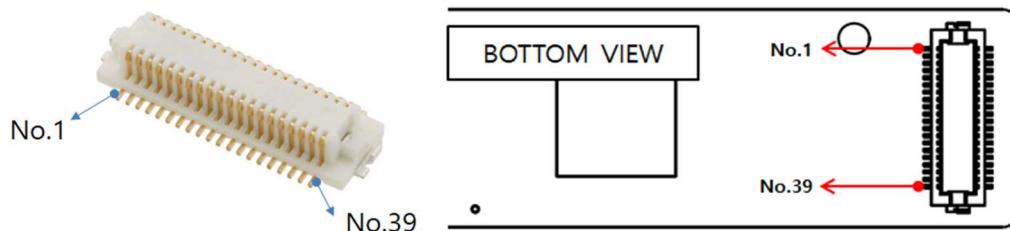


Figure 10 B to B connector No.1 position

Name	No.		Name
+5V	1	2	GND
+5V	3	4	GND
+5V	5	6	GND
+5V	7	8	GND
+5V	9	10	GND
+5V	11	12	GND
+5V	13	14	GND
GND	15	16	GND
LVDS_RX_P	17	18	LVDS_TX_P
LVDS_RX_N	19	20	LVDS_TX_N
GND	21	22	GND
MIPI_DATA0_P	23	24	Boot done
MIPI_DATA0_N	25	26	RESET
GND	27	28	LD Enable
MIPI_CLK_P	29	30	GPIO0
MIPI_CLK_N	31	32	GPIO1
GND	33	34	GPIO2
MIPI_DATA1_P	35	36	I2C_SDA
MIPI_DATA1_N	37	38	I2C_SCL
GND	39	40	Sync Input

Table 20 B to B connector pin map

#### 9.4. B to B connector pin information

Name	Description	Electrical Characteristics
+5V	ToF Module Power Input	5V/3A
MIPI_DATA0_N	MIPI data lane 0(negative)	MIPI
MIPI_DATA0_P	MIPI data lane 0(positive)	MIPI
MIPI_CLK_N	MIPI clock lane(negative)	MIPI
MIPI_CLK_P	MIPI clock lane(positive)	MIPI
MIPI_DATA1_N	MIPI data lane 1(negative)	MIPI
MIPI_DATA1_P	MIPI data lane 1(positive)	MIPI
LVDS_TX_P	Differential modulation clock output(positive)	LVDS
LVDS_TX_N	Differential modulation clock output(negative)	LVDS
LVDS_RX_P	Differential modulation clock input(negative)	LVDS
LVDS_RX_N	Differential modulation clock input(positive)	LVDS
Boot done	Booting Done : Active High	1.8V
RESET	Reset : Active Low	1.8V
LD ENABLE	Laser Diode(VCSEL) Enable : Active Low	1.8V
GPIO	General Purpose I/O	1.8V
I2C_SDA	I2C Serial Data(Slave)	1.8V
I2C_SCL	I2C Serial Clock(Slave)	1.8V
Sync Input	Second camera SYNC signal : Input	1.8V

Table 21 B to B connector pin information

## 10. Design Guidelines

### 10.1. LVDS line PCB design guide(Mandatory)

- Assign those two pair of pins as close as possible, to be connected in the shortest path on the host PCB.
- Line length should be the same.
- Design with an impedance of 100 ohm.

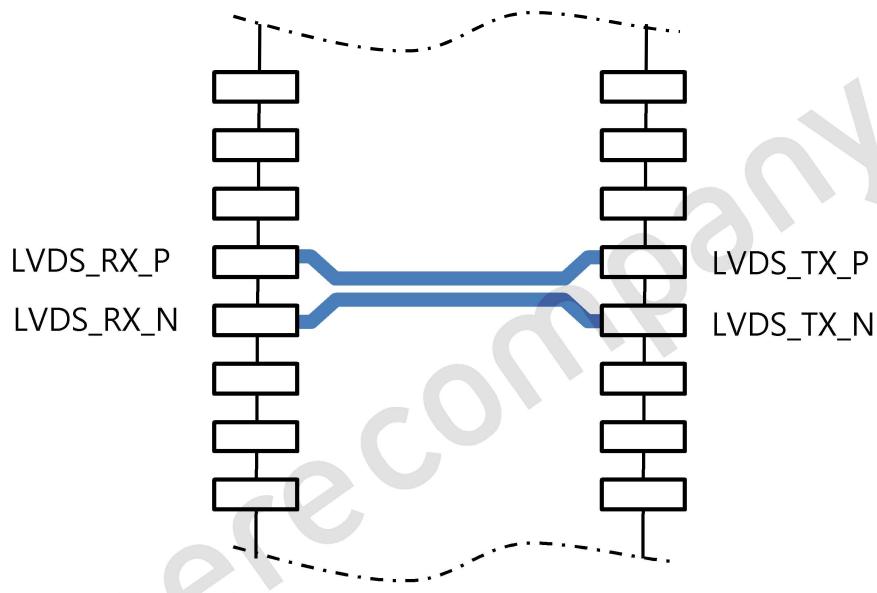


Figure 11 Host PCB LVDS line design guide

### 10.2. MIPI signals artwork guide

- Keep the length difference of the differential traces less than 1mm.
- Design with an impedance of  $100 \Omega$

### 10.3. Notes on design

- Design the host PCB, the connector pin 1 position should not be changed
- The specified power must be supplied to the ToF camera module

## 11. Mechanical Drawings

### 11.1.Schematic

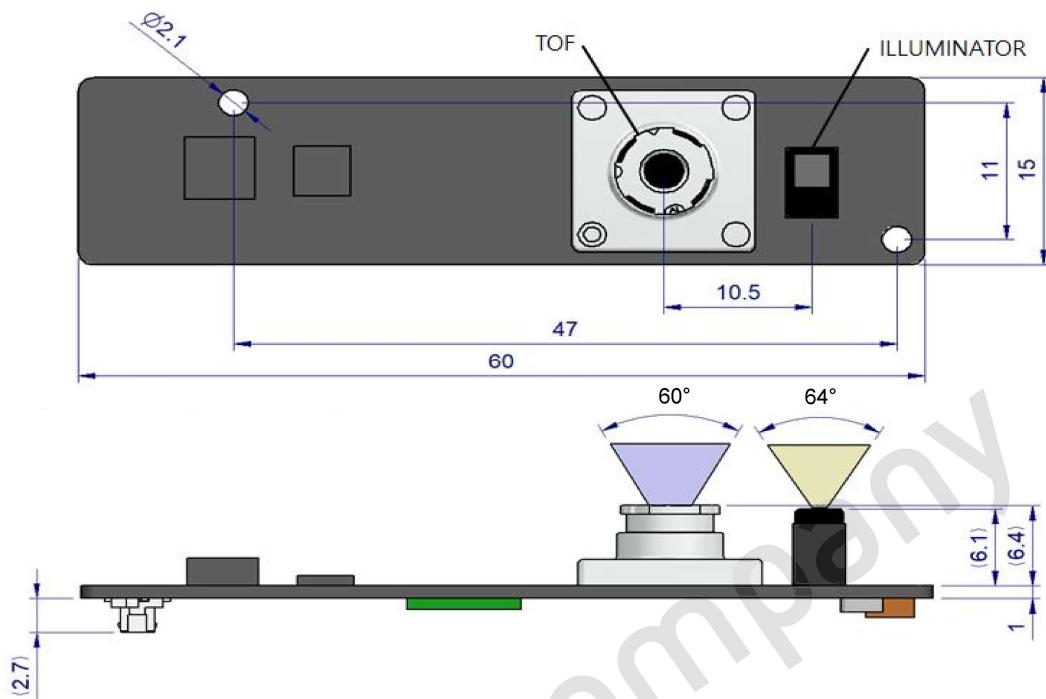


Figure 12 S100D dimension and schematic

### 11.2.Physical z=0 plane

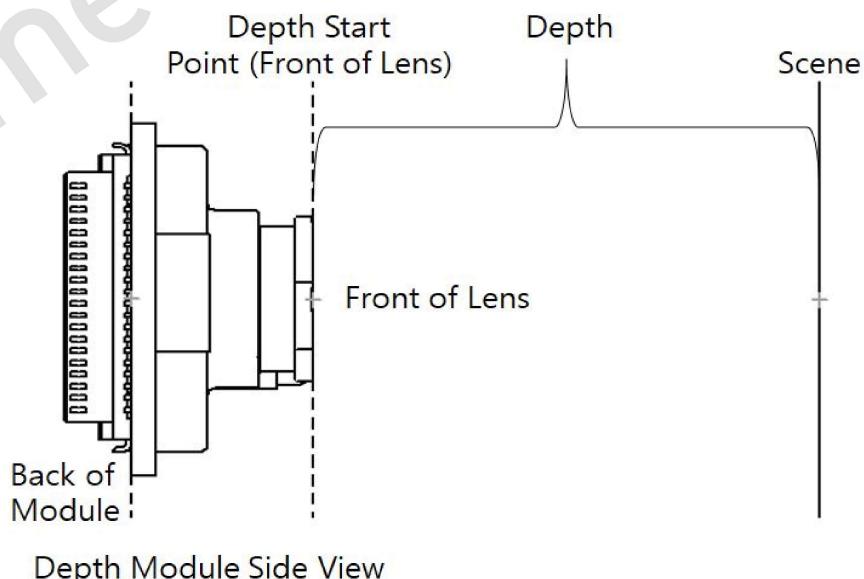


Figure 13 Physical z=0 plane

## 12. Connector Drawings

### 12.1. S100D B to B connector drawing(BBR50-04001-001)

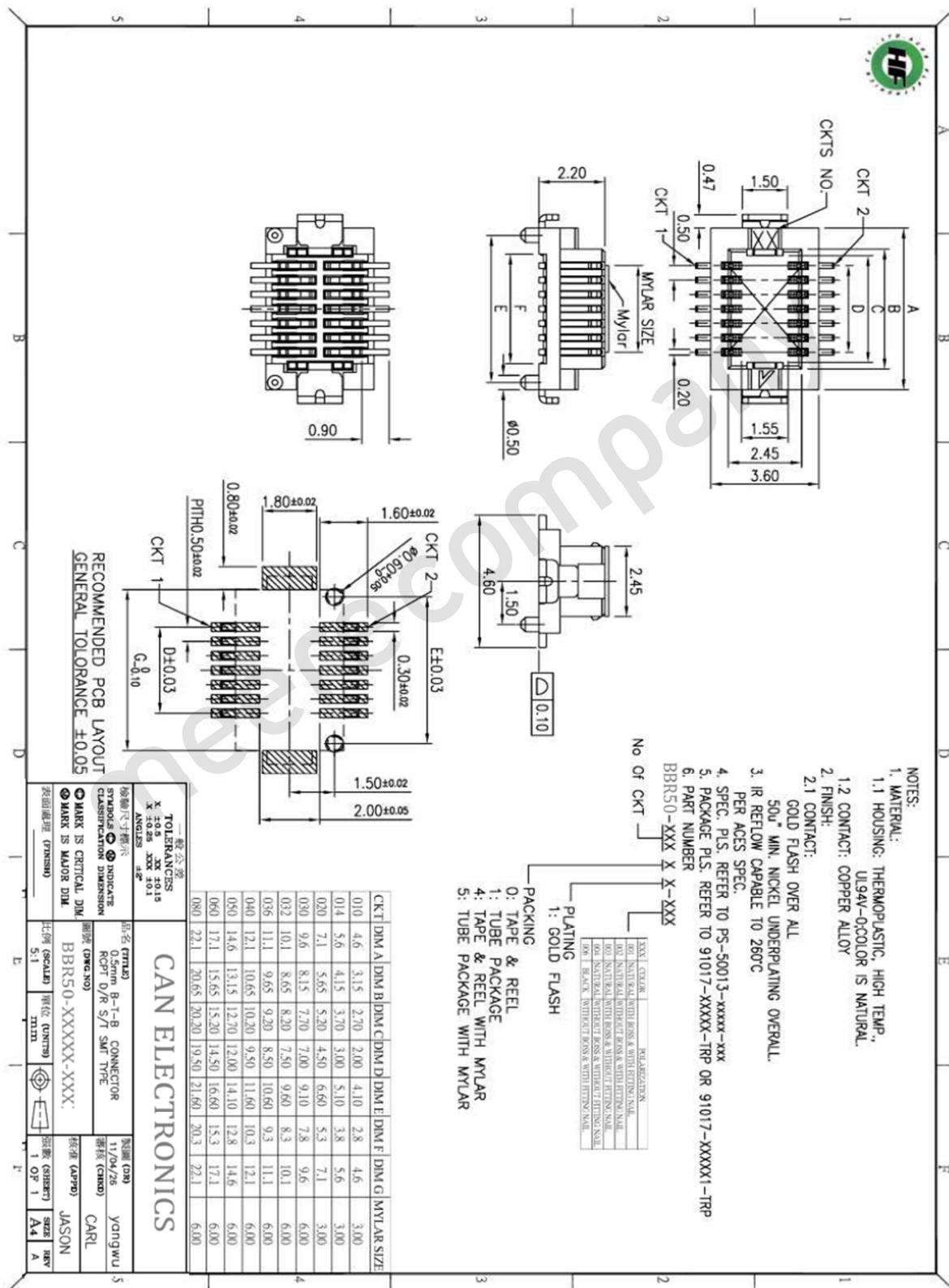
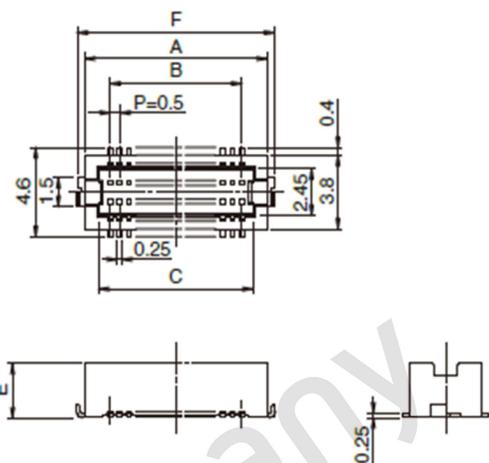
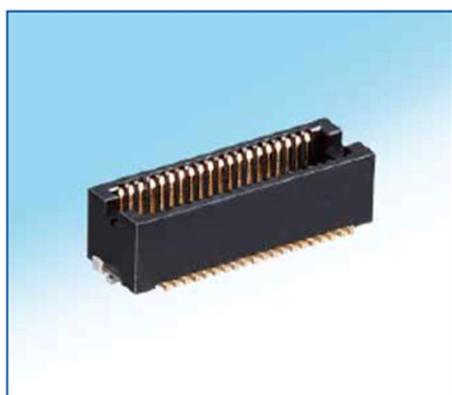


Figure 14 S100D connector

## 12.2. Host board connector drawing (DF12NB(5.0)-40DP-0.5V(51))

### ■Header With Solder Tab



●Stacking Height : 3.5 to 5mm Product

Unit : mm

Part No.	HRS No.	No. of Pos.	A	B	C	E	F	Remarks	RoHS
DF12NB(3.5)-20DP-0.5V(51)	537-0493-0 51	20	7.2	4.5	5.7	2.8	8.1	With Solder Tab	YES
DF12NB(3.5)-30DP-0.5V(51)	537-0494-0 51	30	9.7	7.0	8.2		10.6		
DF12NB(3.5)-36DP-0.5V(51)	537-0495-0 51	36	11.2	8.5	9.7		12.1		
DF12NB(3.5)-40DP-0.5V(51)	537-0496-0 51	40	12.2	9.5	10.7		13.1		
DF12NB(3.5)-50DP-0.5V(51)	537-0497-0 51	50	14.7	12.0	13.2		15.6		
DF12NB(3.5)-60DP-0.5V(51)	537-0498-0 51	60	17.2	14.5	15.7		18.1		
DF12NB(4.0)-20DP-0.5V(51)	537-0592-0 51	20	7.2	4.5	5.7		8.1		
DF12NB(4.0)-30DP-0.5V(51)	537-0593-0 51	30	9.7	7.0	8.2		10.6		
DF12NB(4.0)-32DP-0.5V(51)	537-0594-0 51	32	10.2	7.5	8.7		11.1		
DF12NB(4.0)-36DP-0.5V(51)	537-0595-0 51	36	11.2	8.5	9.7		12.1		
DF12NB(4.0)-40DP-0.5V(51)	537-0596-0 51	40	12.2	9.5	10.7		13.1		
DF12NB(4.0)-50DP-0.5V(51)	537-0597-0 51	50	14.7	12.0	13.2		15.6		
DF12NB(4.0)-60DP-0.5V(51)	537-0598-0 51	60	17.2	14.5	15.7		18.1		
DF12NB(5.0)-20DP-0.5V(51)	537-0877-0 51	20	7.2	4.5	5.7	4.3	8.1		
DF12NB(5.0)-30DP-0.5V(51)	537-0878-0 51	30	9.7	7.0	8.2		10.6		
DF12NB(5.0)-36DP-0.5V(51)	537-0879-0 51	36	11.2	8.5	9.7		12.1		
DF12NB(5.0)-40DP-0.5V(51)	537-0880-0 51	40	12.2	9.5	10.7		13.1		
DF12NB(5.0)-50DP-0.5V(51)	537-0881-0 51	50	14.7	12.0	13.2		15.6		
DF12NB(5.0)-60DP-0.5V(51)	537-0882-0 51	60	17.2	14.5	15.7		18.1		

Note : Please order the embossed tape packaging product per reel. (1,000pcs/reel)

Figure 15 Host board Connector

## 13. Certification

### 13.1. Eye safety

Standard	Result
IEC 60825-1:2014 (Third Edition)	Class 1

Table 22 Eye safety standard information

## Appendix A : Data Format

### A.1. Data format - Raw 10 bits (16 bits unsigned int)

The S100D has 3 output modes as shown in the table below.( Default : mode 0), Each (Z/R) and (Amplitude/Intensity) is selectable and the default is Z, Amplitude.

mode	Resolution	Position(Z/R selectable)			IR(selectable)
		X	Y	Z / R	Amplitude / Intensity
mode 0	2560 x 961	O	O	O	O
mode 1	1280 x 961	-	-	O	O
mode 2	640 x 961	-	-	O	-

Table 23 Data mode

#### A.1.1. 1 pixel format

Each mode has a different pixel size. Attention is required in these situations.

Mode 0 (64bits): 1pixel (16bits X, 16bits Y, 16bits Z, 16bits A)

Mode 1 (32bits): 1pixel (16bits R, 16bits A)

Mode 2 (16bits): 1pixel (16bits R)

#### A.1.2. 16 bits data format

Complexly, it imports two 10-bit raw MIPI data to convert one 16-bit. The 16-bit data generated becomes a component of the pixel.

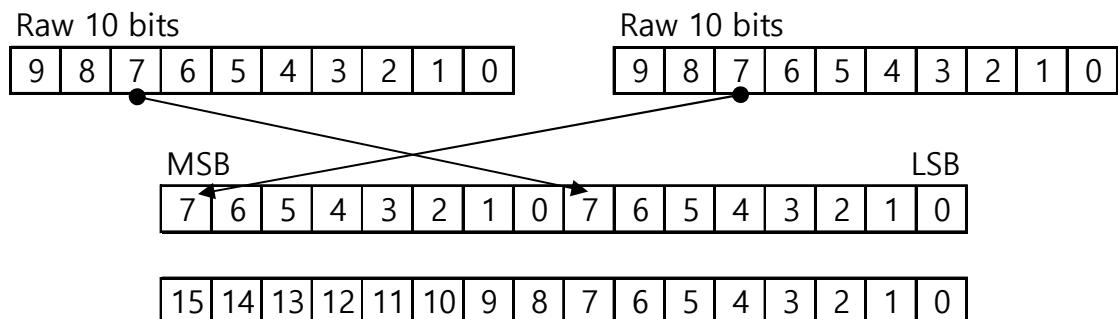


Figure 16 Data reconstruction (2 MIPI Raw 10 bits to 16 bits data)

## A.2. Mode example

Expression rule

**X - \* \_ # \$**

X : data information

\* : pixel x index

# : pixel y index

\$ : L(LSB) H(MSB)

**Em - #**

Em : embedded data

# : data index

mode 0

Em-0	Em-1	Em-2	Em-3	Em-4	Em-5	Em-6	Em-7
X-0_0_L	X-0_0_H	Y-0_0_L	Y-0_0_H	Z-0_0_L	Z-0_0_H	A-0_0_L	A-0_0_H
X-320_0_L	X-320_0_H	Y-320_0_L	Y-320_0_H	Z-320_0_L	Z-320_0_H	A-320_0_L	A-320_0_H
:	:	:	:	:	:	:	:
X-0_479_L	X-0_479_H	Y-0_479_L	Y-0_479_H	Z-0_479_L	Z-0_479_H	A-1_479_L	A-1_479_H
X-320_479_L	X-320_479_H	Y-320_479_L	Y-320_479_H	Z-320_479_L	Z-320_479_H	A-320_479_L	A-320_479_H

total 961 lines Raw10bits

2560 Raw 10bits(320 pixels)

Em-2552	Em-2553	Em-2554	Em-2555	Em-2556	Em-2557	Em-2558	Em-2559
X-319_L	X-319_H	Y-319_L	Y-319_H	Z-319_0_L	Z-319_0_H	A-319_0_L	A-319_0_H
X-639_0_L	X-639_0_H	Y-639_0_L	Y-639_0_H	Z-639_0_L	Z-639_0_H	A-639_0_L	A-639_0_H
:	:	:	:	:	:	:	:
X-319_479_L	X-319_479_H	Y-319_479_L	Y-319_479_H	Z-319_479_L	Z-319_479_H	A-319_479_L	A-319_479_H
X-639_479_L	X-639_479_H	Y-639_479_L	Y-639_479_H	Z-639_479_L	Z-639_479_H	A-639_479_L	A-639_479_H

mode 1

Em-0	Em-1	Em-2	Em-3	Em-4	Em-5	Em-6	Em-7
R-0_0_L	R-0_0_H	A-0_0_L	A-0_0_H	R-1_0_L	R-1_0_H	A-1_0_L	A-1_0_H
R-320_0_L	R-320_0_H	A-320_0_L	A-320_0_H	R-321_0_L	R-321_0_H	A-321_0_L	A-321_0_H
:	:	:	:	:	:	:	:
R-0_479_L	R-0_479_H	A-0_479_L	A-0_479_H	R-1_479_L	R-1_479_H	A-1_479_L	A-1_479_H
R-320_479_L	R-320_479_H	A-320_479_L	A-320_479_H	R-321_479_L	R-321_479_H	A-321_479_L	A-321_479_H

total 961 lines Raw10bits

1280 Raw 10bits(320 pixels)

Em-1272	Em-1273	Em-1274	Em-1275	Em-1276	Em-1277	Em-1278	Em-1279
R-318_0_L	R-318_0_H	A-318_0_L	A-318_0_H	R-319_0_L	R-319_0_H	A-319_0_L	A-319_0_H
R-638_0_L	R-638_0_H	A-638_0_L	A-638_0_H	R-639_0_L	R-639_0_H	A-639_0_L	A-639_0_H
:	:	:	:	:	:	:	:
R-318_479_L	R-318_479_H	A-318_479_L	A-318_479_H	R-319_479_L	R-319_479_H	A-319_479_L	A-319_479_H
R-638_479_L	R-638_479_H	A-638_479_L	A-638_479_H	R-639_479_L	R-639_479_H	A-639_479_L	A-639_479_H

mode 2

Em-0	Em-1	Em-2	Em-3	Em-4	Em-5	Em-6	Em-7
R-0_0_L	R-0_0_H	R-1_0_L	R-1_0_H	R-2_0_L	R-2_0_H	R-3_0_L	R-3_0_H
R-320_0_L	R-320_0_H	R-321_0_L	R-321_0_H	R-322_0_L	R-322_0_H	R-323_0_L	R-323_0_H
:	:	:	:	:	:	:	:
R-0_479_L	R-0_479_H	R-1_479_L	R-1_479_H	R-2_479_L	R-2_479_H	R-3_479_L	R-3_479_H
R-320_479_L	R-320_479_H	R-321_479_L	R-321_479_H	R-322_479_L	R-322_479_H	R-323_479_L	R-323_479_H

total 961 lines Raw10bits

640 Raw 10bits(320 pixels)

Em-632	Em-633	Em-634	Em-635	Em-636	Em-637	Em-638	Em-639
R-316_0_L	R-316_0_H	R-317_0_L	R-317_0_H	R-318_0_L	R-318_0_H	R-319_0_L	R-319_0_H
R-636_0_L	R-636_0_H	R-637_0_L	R-637_0_H	R-638_0_L	R-638_0_H	R-639_0_L	R-639_0_H
:	:	:	:	:	:	:	:
R-316_479_L	R-316_479_H	R-317_479_L	R-317_479_H	R-318_479_L	R-318_479_H	R-319_479_L	R-319_479_H
R-636_479_L	R-636_479_H	R-637_479_L	R-637_479_H	R-638_479_L	R-638_479_H	R-639_479_L	R-639_479_H

Figure 17 Output mode examples

### A.3. Embedded line data description

Data index	Bus_width	Name	Description
Em-0	8	rev_no[7:0]	MR1000 Revision number
Em-6	8	frame_count[7:0]	frame_count[7:0]
Em-7	8	frame_count[15:8]	frame_count[15:8]
Em-8	1	filter3_on[7]	filter3_on/off
	1	remove_flying_pixel_on[6]	remove_flying_pixel_on/off
	1	filter2_on[5]	filter2_on/off
	1	filter1_on[4]	filter1_on/off
Em-12	8	set_firm_rev_no[7:0]	firmware Revision number
Em-17	8	tof_temp[7:0]	ToF temperature = tof_temp[15:0] * 256
Em-18	8	tof_temp[15:8]	
Em-19	8	drv_temp[7:0]	drive IC temperature = drv_temp[15:0] * 256
Em-20	8	drv_temp[15:8]	
Em-21	8	amp_max_limit[7:0]	amp_max_limit
Em-22	8	amp_max_limit[15:8]	
Em-23	8	amp_min_limit[7:0]	amp_min_limit
Em-24	8	amp_min_limit[15:8]	
Em-25	8	depth_max_limit[7:0]	depth_max_limit
Em-26	8	depth_max_limit[15:8]	
Em-27	8	depth_min_limit[7:0]	depth_min_limit
Em-28	8	depth_min_limit[15:8]	
Em-29	8	mci_thresh[7:0]	mci_thresh
Em-30	8	mci_thresh[15:8]	
Em-35	4	mci_flag[3:0]	mci_flag
Em-38	8	scat_threshold[7:0]	scat_threshold
Em-39	8	scat_threshold[15:8]	
Em-40	8	flying pixel_threshold[7:0]	remove_flying_pixel_thresh
Em-41	8	flying pixel_threshold[15:8]	
Em-42	8	temporal_mblur[7:0]	temporal_mblur
Em-43	8	multi_freq_ctrl[7:0]	multi_freq_ctrl
Em-68	4	data_format_sel[3:0]	data_format_sel[3:0]
Em-73	8	g_offset[7:0]	global_offset
Em-74	8	g_offset[15:8]	

Table 24 Embedded line data description

## Appendix B : Cover Glass Assy' Guide

When using the cover glass, it is recommended to place it as close to the lens as possible.  
And it is necessary to place a light barrier between RX and TX to minimize light spread.

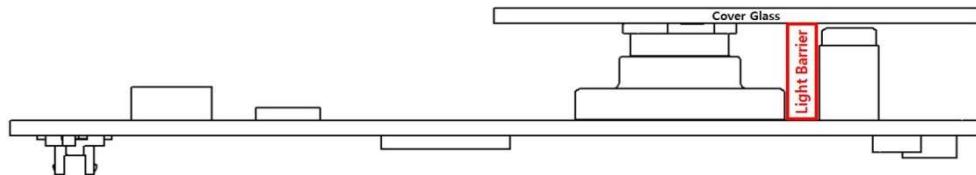


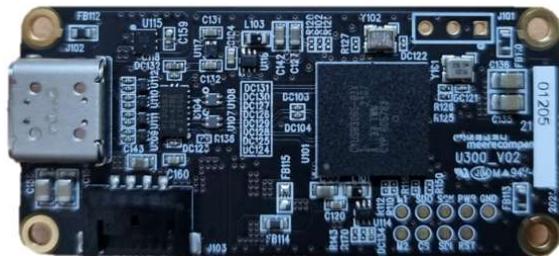
Figure 18 Example image of use of cover glass

# USB Interface Solution

## Model U300

- USB3.0 Bridge Board

U300 image



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## 1. Introduction

### 1.3. System block diagram

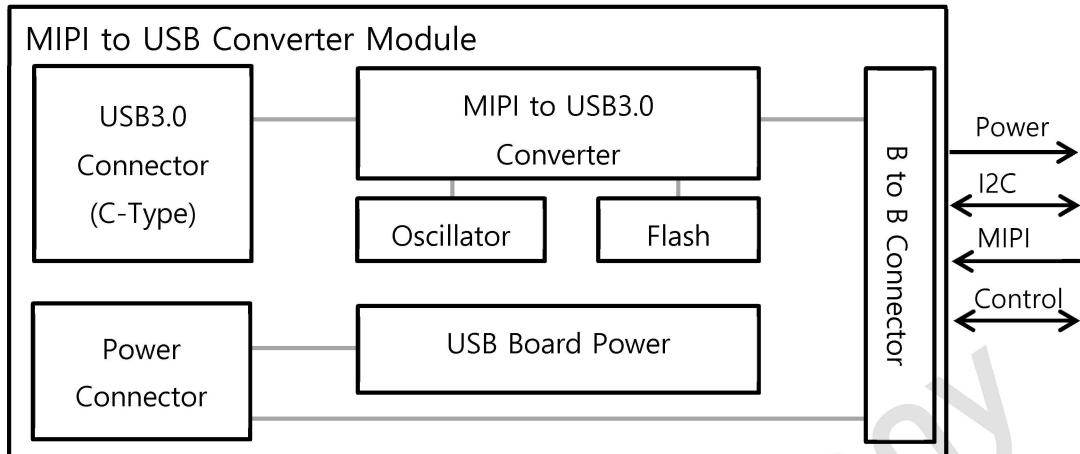


Figure 1 System block diagram

- MIPI to USB3.0 Converter(CYUSB3065)
  - 5-Gbps USB 3.0 PHY
  - MIPI CSI-2 RX interface: Supports up to four data lanes(use 2 lanes)
  - Supports the following video data formats: RAW 8/10/12/14(use 10 bit)
- USB Board Power
  - Input Voltage: 5V
  - Output Voltage: 3.3V(Power of USB3.0 Mux IC), 1.8V(Vddio), 1.2V(Vdd)
- Oscillator
  - System Clock: 19.2 MHz
  - Watchdog timer Clock: 32 kHz
- Flash
  - Boot from SPI
  - Compatible with S25FS064S, S25FS128S, S25LFL064L, W25Q-series

## **2. General Specification**

### **2.2. Specification**

<b>USB interface</b>	
Compliance	USB 3.0
Data rate	5 Gbps
Connector	USB-C type
<b>MIPI interface</b>	
Compliance	CSI-2
lane	2 lane
Data rate	Max 2Gbps
<b>Memory &amp; Clock</b>	
Memory	4Mb Serial Flash
Clock	System
	19.2 MHz( $\pm 150$ ppm)
Clock	Watchdog
	32 kHz( $\pm 200$ ppm)
<b>Control Interface</b>	
Control interface	I2C 400 Kbps
Data interface	MIPI CSI-2 2 lanes, 500 Mbps/lane
<b>Power(Adaptor)</b>	
Input Voltage Range	90~264V(Rated 100~240V) 50/60Hz
Output Voltage	4.75~5.25V(Rated 5V)
Current	Max 5A(25W)
Safety	CE, UL/cUL, KC, UKCA, CB
<b>Temperature</b>	
Operating temperature	0 ~ 40°C
Storage temperature	-20 ~ 70°C
<b>Mechanics</b>	
Dimensions	50.0 x 23.0 x 8.6 mm <sup>3</sup>
Weight	5.4 g

**Table 1 Information of general specification**

### **3. Functional Specification**

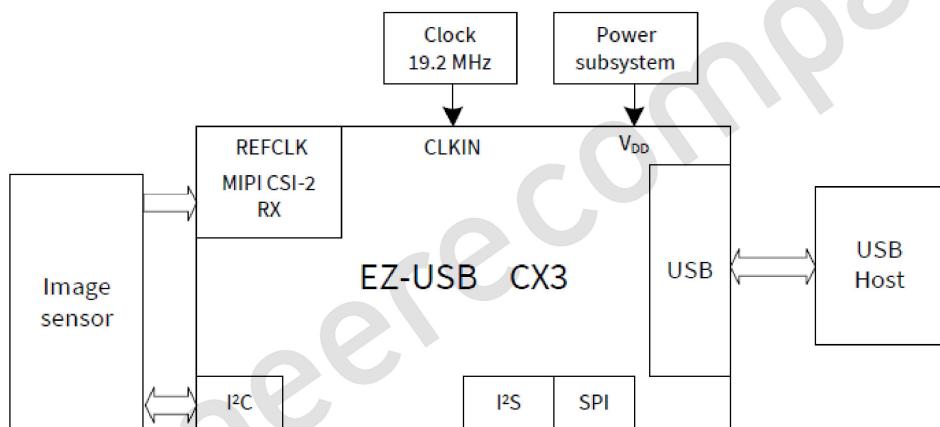
#### **3.1. Boot options**

CYUSB3065 can load boot images from various sources, selected by the configuration of the PMODE pins. Following are boot options:

- Boot from USB
- Boot from I<sup>2</sup>C
- Boot from SPI

In U300 system, Boot from SPI is set to Default.

#### **3.2. CYUSB3065 block diagram**



**Figure 2 CYUSB3065 block diagram**

The signal is transmitted to CX3 through the image sensor and MIPI CSI-2 interface, and the transmitted signal is converted to USB signal format and output to the USB 3.0 connector.

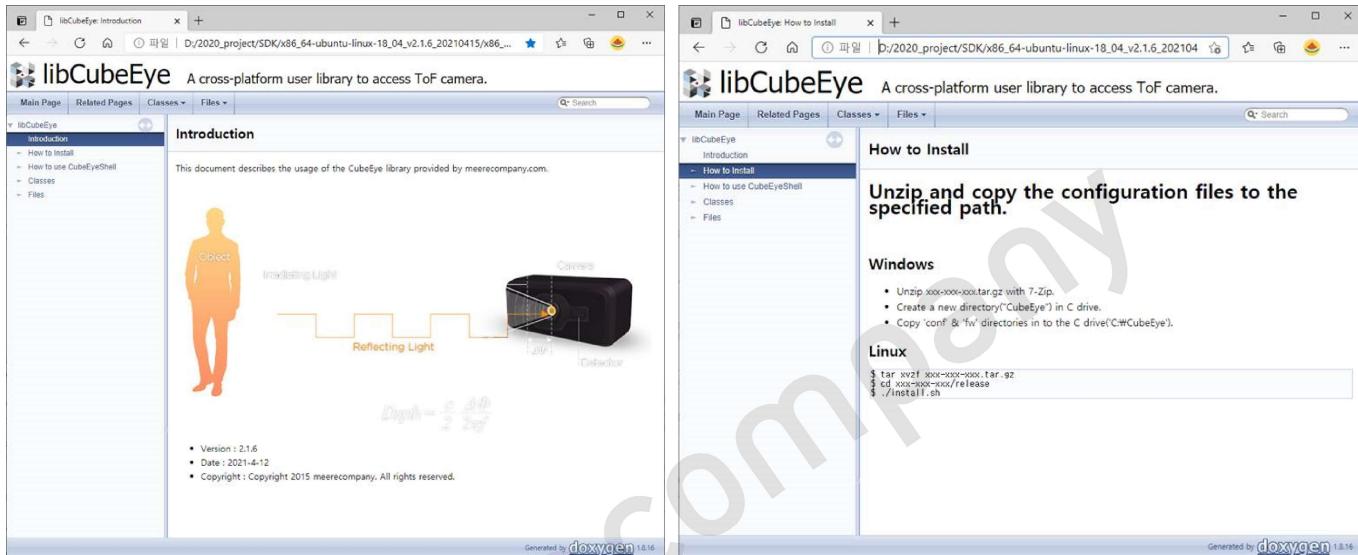
## 4. Software(SDK)

### 4.1 CubeEye SDK application

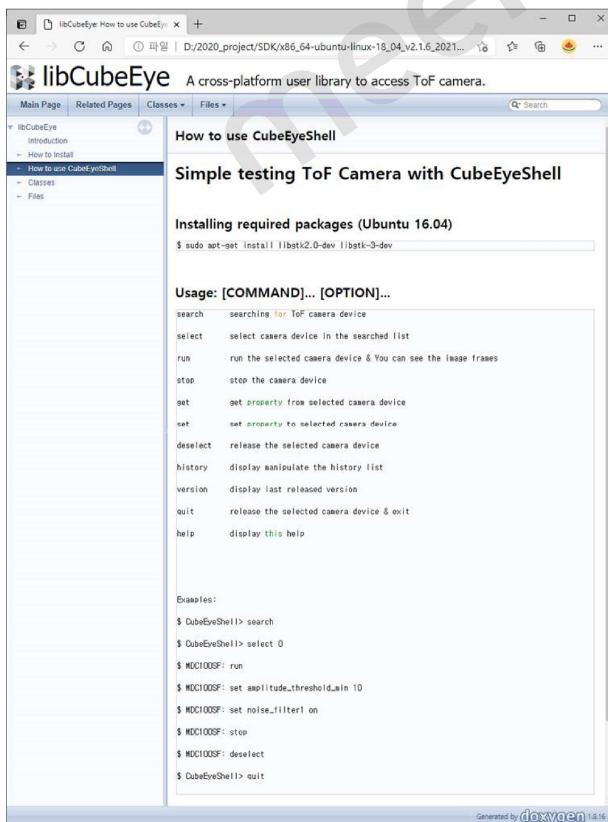
1. Execute '/release/doc/html/index.html' of SDK from <http://www.cube-eye.co.kr/en/#/support/main.asp?sub=download>

-Refer to the 'SDK User Guide for Windows & Linux'

2. Check 'how to install'



3. Execute CubeEyeShell : Click 'how to use CubeEyeShell'



## 5. Design Guidelines

### 5.1 USB line PCB design guide(CYUSB3065)

- Minimize the trace length of USB lines as much as possible (< 3 inches(7.62cm))
- The polarity can be swapped on the USB 3.0 differential pairs. Polarity detection is done automatically by the USB 3.0 PHY during link training,
- Tie the R\_USB2 pin to ground through a 1% 6.04-k $\Omega$  precision resistor.
- USB 3.0 traces require additional AC coupling capacitors (0.1  $\mu$ F) placed on the SS\_TX lines.

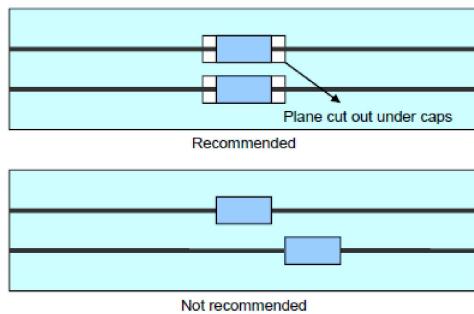


Figure 3 AC coupling capacitor of SS\_TX

- Keep the USB signal line impedance at 90  $\Omega$  differential ( $\pm 7\%$ )
- Fill the space between the two differential pairs with ground. Maintain a minimum of 2W space between the ground and the differential pairs, where W = trace width
- Keep the crystal trace as short as possible. Place the crystal within 2 cm from FX3/SX3
- Keep the power traces away from Hi-Speed data and clock lines.
- Power trace widths should be  $\geq 25$  mils to reduce inductance
- Do not place any Hi-Speed signal and reset signal trace near to the crystal.
- Keep trace spacing between differential pairs consistent to avoid impedance mismatches as shown in the Figure 18.

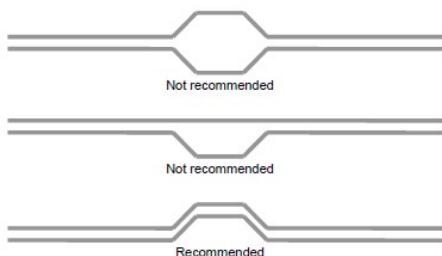


Figure 4 Impedance mismatching

## 6. Mechanical Drawings

### 6.1 Schematic

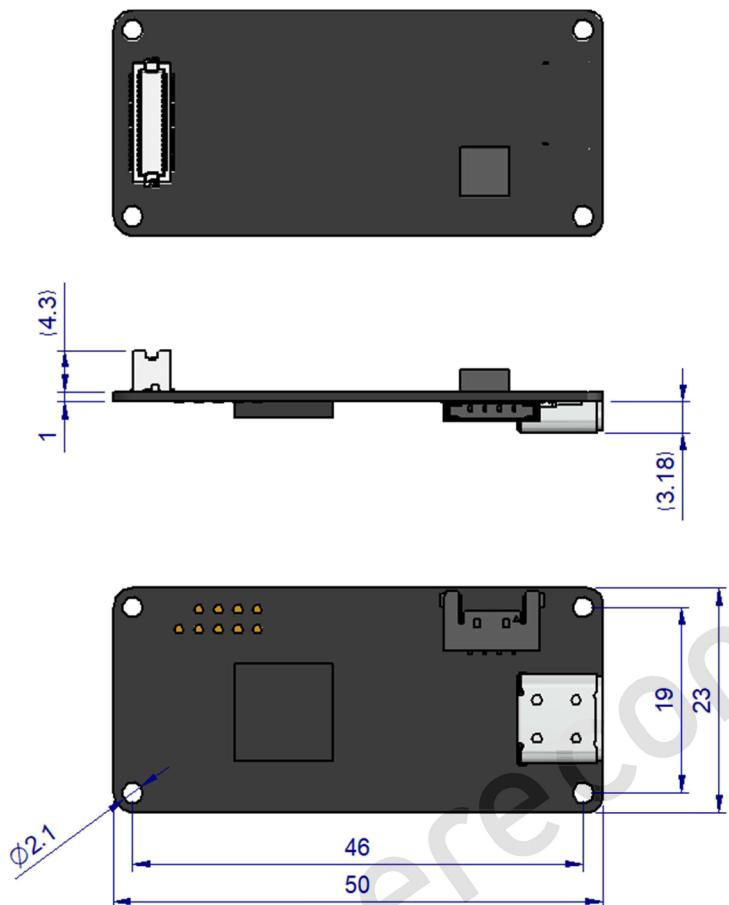


Figure 5 U300 dimension

## 7. Connector Drawings

### 7.1 U300 connector drawing (DF12NB(5.0)-40DP-0.5V(51))

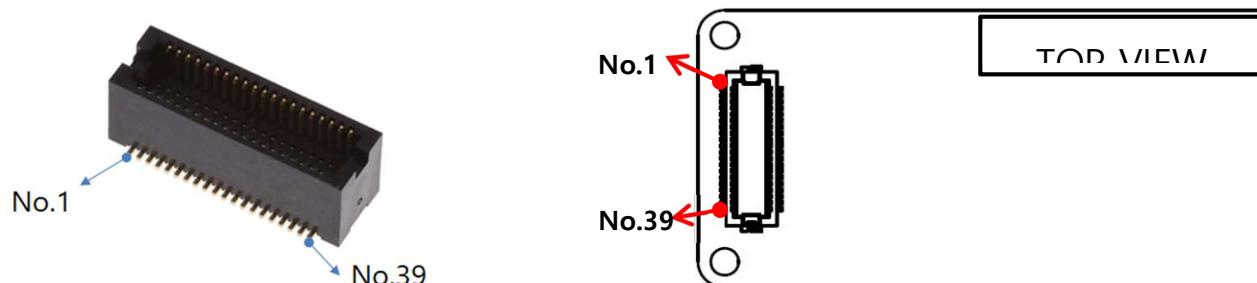


Figure 6 U300 B to B connector

Name	No.		Name
GND	1	2	+5V
GND	3	4	+5V
GND	5	6	+5V
GND	7	8	+5V
GND	9	10	+5V
GND	11	12	+5V
GND	13	14	+5V
GND	15	16	GND
LVDS_RX_P	17	18	LVDS_TX_P
LVDS_RX_N	19	20	LVDS_TX_N
GND	21	22	GND
Boot done	23	24	MIPI_DATA0_P
RESET	25	26	MIPI_DATA0_N
N.C	27	28	GND
GPIO0	29	30	MIPI_CLK_P
GPIO1	31	32	MIPI_CLK_N
GPIO2	33	34	GND
I2C_SDA	35	36	MIPI_DATA1_P
I2C_SCL	37	38	MIPI_DATA1_N
N.C	39	40	GND

Table 2 U300 B to B connector pin map

## 7.2 U300 connector pin information

Name	Description	Electrical Characteristics
+5V	ToF Module Power Input	5V/3A
MIPI_DATA0_N	MIPI data lane 0(negative)	MIPI
MIPI_DATA0_P	MIPI data lane 0(positive)	MIPI
MIPI_CLK_N	MIPI clock lane(negative)	MIPI
MIPI_CLK_P	MIPI clock lane(positive)	MIPI
MIPI_DATA1_N	MIPI data lane 1(negative)	MIPI
MIPI_DATA1_P	MIPI data lane 1(positive)	MIPI
LVDS_RX_P	Differential modulation clock input(positive)	LVDS
LVDS_RX_N	Differential modulation clock input(negative)	LVDS
LVDS_TX_P	Differential modulation clock output(negative)	LVDS
LVDS_TX_N	Differential modulation clock output(positive)	LVDS
Boot done	Booting Done : Active High	1.8V
RESET	Reset : Active Low	1.8V
GPIO	General Purpose I/O	1.8V
I2C_SDA	I2C Serial Data(Slave)	1.8V
I2C_SCL	I2C Serial Clock(Slave)	1.8V

Table 3 U300 connector pin information

## ***8. Accessories & Connection***

## 8.1 Accessories

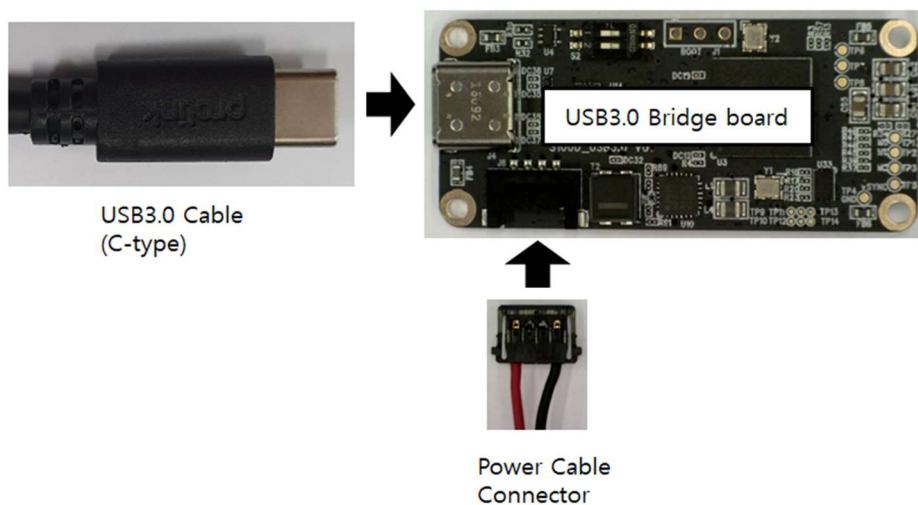
- Adaptor + AC power cable(selected by country)
  - DC Jack converter cable
  - USB3.0 Cable(A to C type)



**Figure 7 U300 cable composition**

## 8.2 Cable connection

- Power Cable/USB Cable connection



**Figure 8 U300 cable connection**

## 9. Package

### 9.1 Package Material



No.	Part name
#1	Carton Box - E100(Siemens Healthcare)
#2	UNIT BOX-S100D,S110D,MDC200DW
#3	TRAY TOP-S100D,S110D+U300
#4	TRAY BOTTOM-S100D+U300,S110D,MDC200DW
#5	Quick guide - S100D,S110D

Figure 9 U300 package material



Figure 10 U300 packing with contents(S110D+U300)

## Appendix A : Application of U300

### A.1 S100D on U300

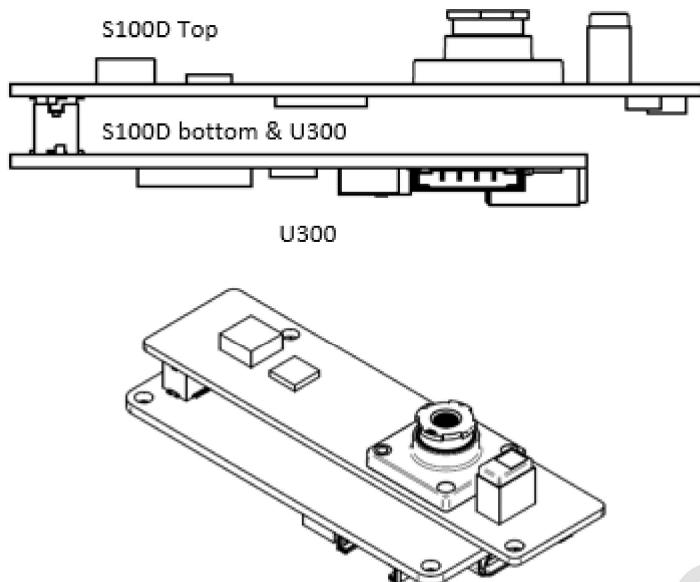


Figure 11 U300 assembly with S100D

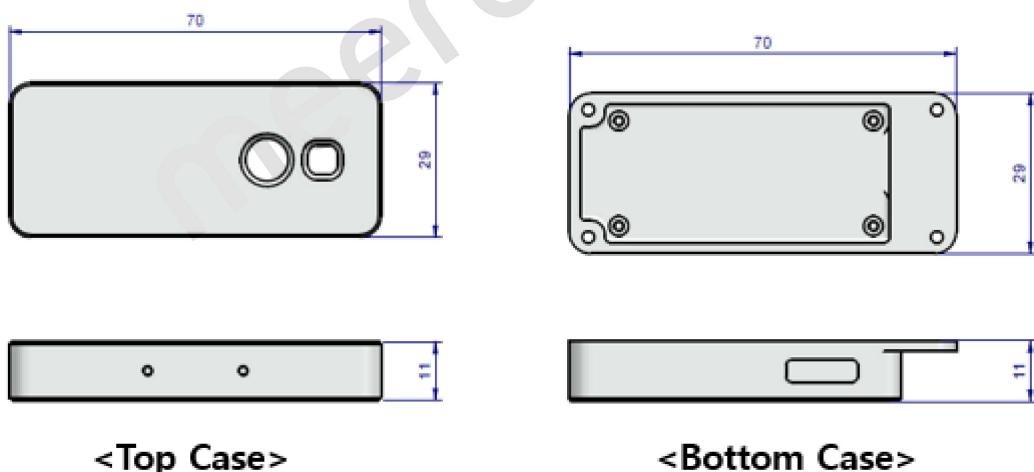


Figure 12 Case of U300 + S100D