Transcript

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Transcript

```
# Errors: 0, Warnings: 0
# Compile of addsub.sv was successful.
# Errors: 0, Warnings: 0
# Compile of counter_down.sv was successful.
# Errors: 0, Warnings: 0
# Compile of mux2.sv was successful.
# Errors: 0, Warnings: 0
# Compile of mux3.sv was successful.
# Errors: 0, Warnings: 0
# Compile of mux5.sv was successful.
# Errors: 0, Warnings: 0
# Compile of register.sv was successful.
# Errors: 0, Warnings: 0
# Compile of right_shift_register.sv was successful.
# Errors: 0, Warnings: 0
# Compile of robertsonstest.sv was successful.
# Errors: 0, Warnings: 0
# Compile of robs_control_unit_micro.sv was successful.
# Errors: 0, Warnings: 0
# Compile of robsmult.sv was successful.
# Errors: 0, Warnings: 0
# Compile of upc_reg.sv was successful.
# Errors: 0, Warnings: 0
# Compile of register_hl.sv was successful.
# Errors: 0, Warnings: 0
# Compile of rom.sv was successful.
# Errors: 0, Warnings: 0
# Compile of robs_data_path.sv was successful.
VSIM 43> vsim -gui work.robertsonstest
# End time: 13:03:13 on Oct 21,2021, Elapsed time: 0:01:29
# Errors: 0, Warnings: 3
# vsim -gui work.robertsonstest
# Start time: 13:03:13 on Oct 21,2021
# Loading sv_std.std
# Loading work.robertsonstest
# Loading work.robsmult
# Loading work.robs_control_unit_micro
# Loading work.upcreg
# Loading work.mux5
# Loading work.rom
```

Transcript

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Transcript

```
# vsim -gui work.robertsonstest
# Start time: 13:03:13 on Oct 21,2021
# Loading sv_std.std
# Loading work.robertsonstest
# Loading work.robsmult
# Loading work.robs_control_unit_micro
# Loading work.upcreg
# Loading work.mux5
# Loading work.rom
# Loading work.robs_datapath
# Loading work.register
# Loading work.register_hl
# Loading work.right_shift_register
# Loading work.mux2
# Loading work.mux3
# Loading work.addsub
# Loading work.counter_down
add wave -position insertpoint sim:/robertsonstest/*
add wave -position insertpoint sim:/robertsonstest/uut/*
add wave -position insertpoint sim:/robertsonstest/#INITIAL#41/*
add wave -position insertpoint sim:/robertsonstest/#ALWAYS#81/*
VSIM 47> run -all
# Simulation succeeded 0000 = 0000 = 00 * 00
# Simulation succeeded      0 =      0 =    0 *    0
# Simulation succeeded 001e = 001e = 05 * 06
# Simulation succeeded     30 =     30 =    5 *    6
# Simulation succeeded ffdd = ffdd = 07 * fb
# Simulation succeeded    -35 =    -35 =    7 *   -5
# Simulation succeeded ffe2 = ffe2 = fb * 06
# Simulation succeeded    -30 =    -30 =   -5 *    6
# Simulation succeeded ffc8 = ffc8 = f9 * 08
# Simulation succeeded    -56 =    -56 =   -7 *    8
# Simulation succeeded 001e = 001e = fb * fa
# Simulation succeeded     30 =     30 =   -5 *   -6
# Simulation succeeded 0024 = 0024 = f7 * fc
# Simulation succeeded     36 =     36 =   -9 *   -4
# clock cycles =     1008051, test cycles =           7, score =       16384 /       16384
# ** Note: $stop    : C:/Users/Albert/Desktop/Course Related/cse 140L/Project_Folder_qPrime_modelsim/Lab_1/Starter_Verilog/robertsonstest.sv(77)
#    Time: 10080515 ns  Iteration: 0  Instance: /robertsonstest
# Break in Module robertsonstest at C:/Users/Albert/Desktop/Course Related/cse 140L/Project_Folder_qPrime_modelsim/Lab_1/Starter_Verilog/robertsonstest.sv line 77
```

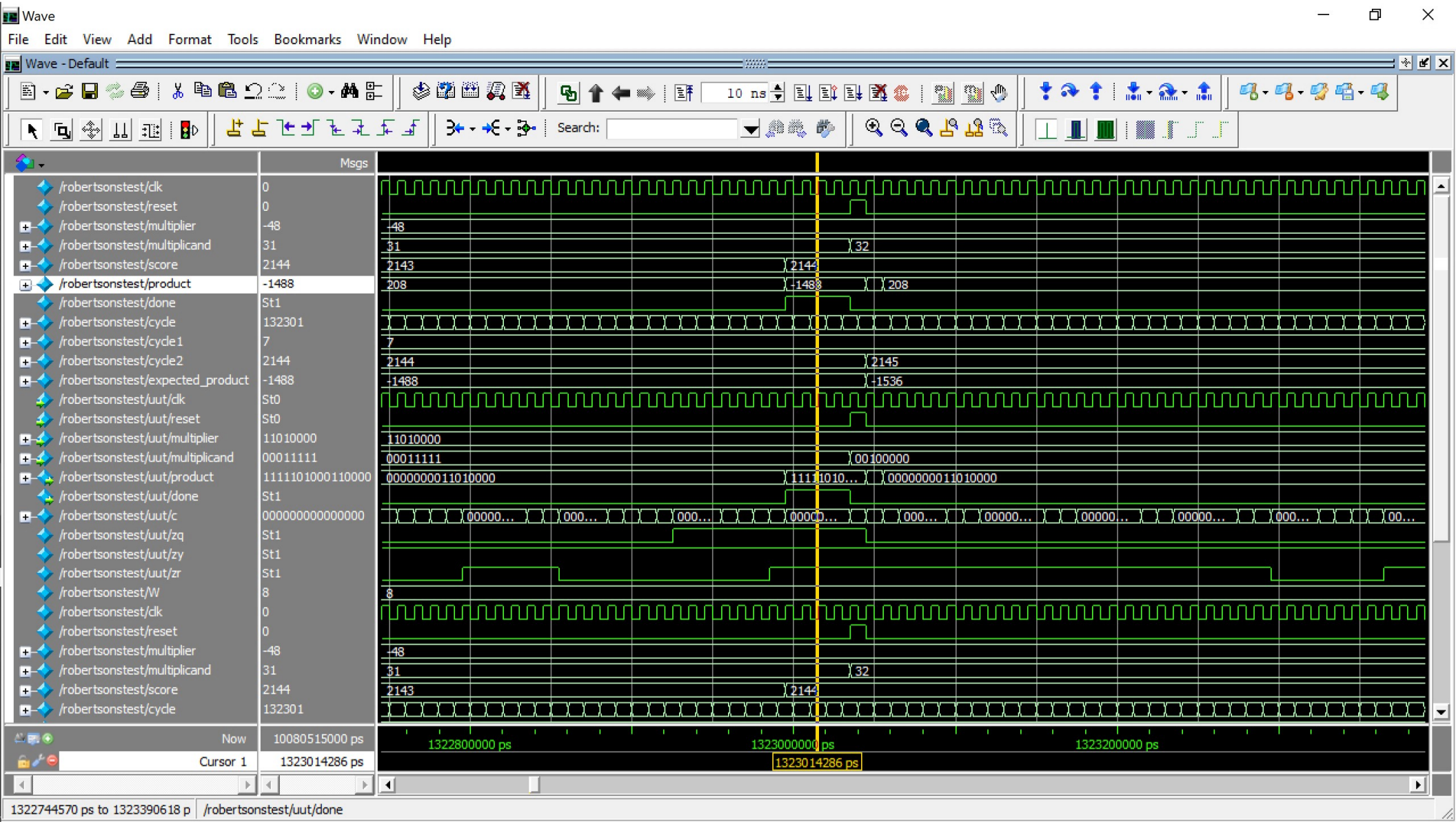
Transcript

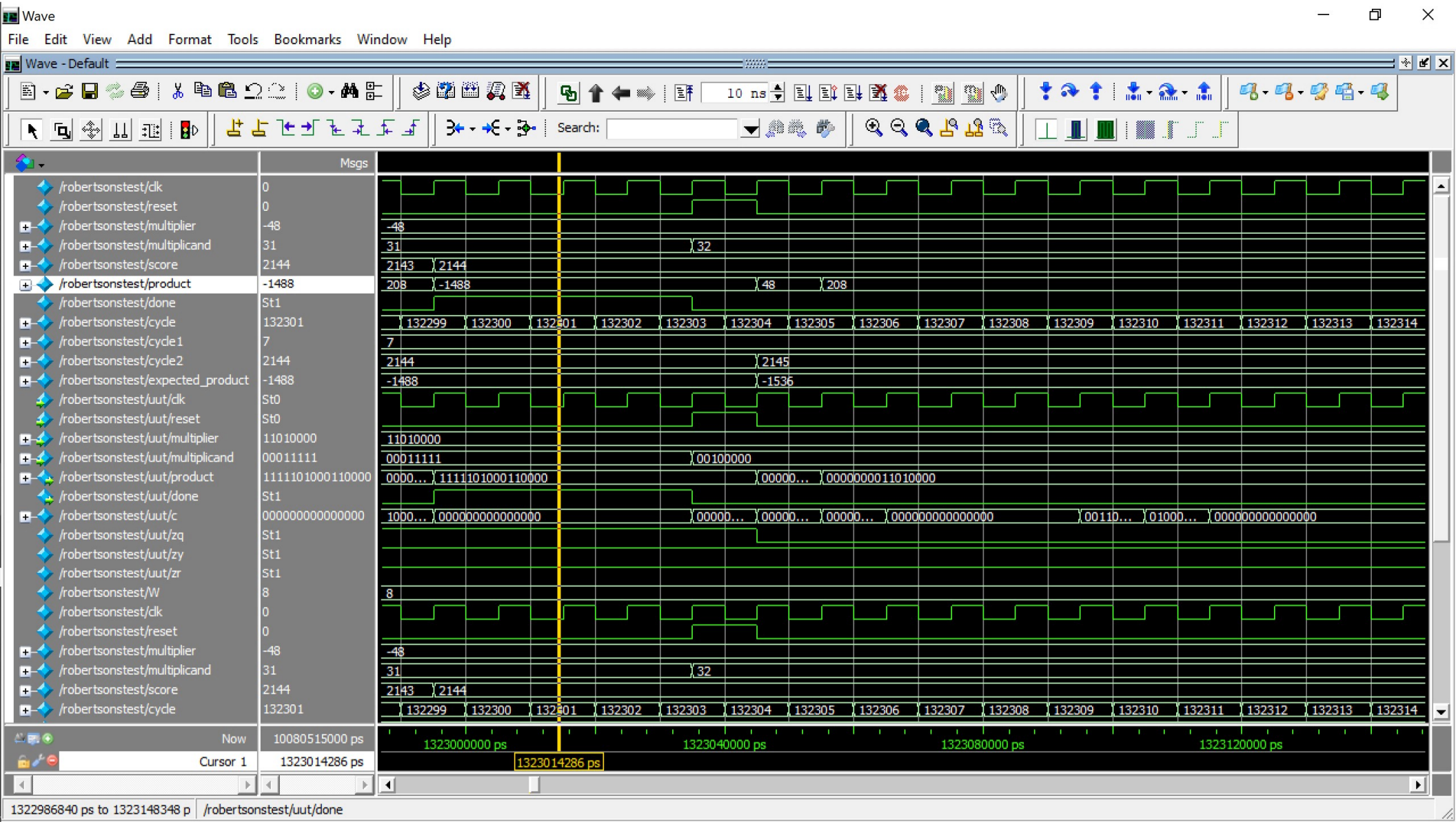
File Edit View Bookmarks Window Help

Transcript

```
# Simulation succeeded      0 =      0 =    0 *    0
# Simulation succeeded 001e = 001e = 05 * 06
# Simulation succeeded     30 =     30 =    5 *    6
# Simulation succeeded ffdd = ffdd = 07 * fb
# Simulation succeeded    -35 =    -35 =    7 *   -5
# Simulation succeeded ffe2 = ffe2 = fb * 06
# Simulation succeeded    -30 =    -30 =   -5 *    6
# Simulation succeeded ffc8 = ffc8 = f9 * 08
# Simulation succeeded    -56 =    -56 =   -7 *    8
# Simulation succeeded 001e = 001e = fb * fa
# Simulation succeeded     30 =     30 =   -5 *   -6
# Simulation succeeded 0024 = 0024 = f7 * fc
# Simulation succeeded     36 =     36 =   -9 *   -4
# clock cycles =     1008051, test cycles =           7, score =       16384 /       16384
# ** Note: $stop    : C:/Users/Albert/Desktop/Course Related/cse 140L/Project_Folder_qPrime_modelsim/Lab_1/Starter_Verilog/robertsonstest.sv(77)
#    Time: 10080515 ns  Iteration: 0  Instance: /robertsonstest
# Break in Module robertsonstest at C:/Users/Albert/Desktop/Course Related/cse 140L/Project_Folder_qPrime_modelsim/Lab_1/Starter_Verilog/robertsonstest.sv line 77
VSIM 48> restart
# Break key hit
VSIM 49> run -all
# Simulation succeeded 0000 = 0000 = 00 * 00
# Simulation succeeded      0 =      0 =    0 *    0
# Simulation succeeded 001e = 001e = 05 * 06
# Simulation succeeded     30 =     30 =    5 *    6
# Simulation succeeded ffdd = ffdd = 07 * fb
# Simulation succeeded    -35 =    -35 =    7 *   -5
# Simulation succeeded ffe2 = ffe2 = fb * 06
# Simulation succeeded    -30 =    -30 =   -5 *    6
# Simulation succeeded ffc8 = ffc8 = f9 * 08
# Simulation succeeded    -56 =    -56 =   -7 *    8
# Simulation succeeded 001e = 001e = fb * fa
# Simulation succeeded     30 =     30 =   -5 *   -6
# Simulation succeeded 0024 = 0024 = f7 * fc
# Simulation succeeded     36 =     36 =   -9 *   -4
# clock cycles =     1008051, test cycles =           7, score =       16384 /       16384
# ** Note: $stop    : C:/Users/Albert/Desktop/Course Related/cse 140L/Project_Folder_qPrime_modelsim/Lab_1/Starter_Verilog/robertsonstest.sv(77)
#    Time: 10080515 ns  Iteration: 0  Instance: /robertsonstest
# Break in Module robertsonstest at C:/Users/Albert/Desktop/Course Related/cse 140L/Project_Folder_qPrime_modelsim/Lab_1/Starter_Verilog/robertsonstest.sv line 77

VSIM 50>
```


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/robertsonstest/clk 0
/robertsonstest/reset 0
/robertsonstest/multiplier -48
/robertsonstest/multiplicand 31
/robertsonstest/score 2144
/robertsonstest/product -1488
/robertsonstest/done St1
/robertsonstest/cycle 132301
/robertsonstest/cycle1 7
/robertsonstest/cycle2 2144
/robertsonstest/expected_product -1488
/robertsonstest/uut/clk St0
/robertsonstest/uut/reset St0
/robertsonstest/uut/multiplier 11010000
/robertsonstest/uut/multiplicand 00011111
/robertsonstest/uut/product 1111101000110000
/robertsonstest/uut/done St1
/robertsonstest/uut/c 0000000000000000
/robertsonstest/uut/zq St1
/robertsonstest/uut/zy St1
/robertsonstest/uut/zr St1
/robertsonstest/W 8
/robertsonstest/clk 0
/robertsonstest/reset 0
/robertsonstest/multiplier -48
/robertsonstest/multiplicand 31
/robertsonstest/score 2144
/robertsonstest/cycle 132301
Now 10080515000 ps
Cursor 1 1323014286 ps
1322800000 ps
1323000000 ps
1323200000 ps
1323014286 ps
1322744570 ps to 1323390618 p
/robertsonstest/uut/done


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/robertsonstest/clk 0
/robertsonstest/reset 0
/robertsonstest/multiplier -48
/robertsonstest/multiplicand 31
/robertsonstest/score 2144
/robertsonstest/product -1488
/robertsonstest/done St1
/robertsonstest/cycle 132301
/robertsonstest/cycle1 7
/robertsonstest/cycle2 2144
/robertsonstest/expected_product -1488
/robertsonstest/uut/clk St0
/robertsonstest/uut/reset St0
/robertsonstest/uut/multiplier 11010000
/robertsonstest/uut/multiplicand 00011111
/robertsonstest/uut/product 1111101000110000
/robertsonstest/uut/done St1
/robertsonstest/uut/c 0000000000000000
/robertsonstest/uut/zq St1
/robertsonstest/uut/zy St1
/robertsonstest/uut/zr St1
/robertsonstest/W 8
/robertsonstest/clk 0
/robertsonstest/reset 0
/robertsonstest/multiplier -48
/robertsonstest/multiplicand 31
/robertsonstest/score 2144
/robertsonstest/cycle 132301
Now 10080515000 ps
Cursor 1 1323014286 ps
1323000000 ps
1323040000 ps
1323080000 ps
1323120000 ps
1323014286 ps
1322986840 ps to 1323148348 p
/robertsonstest/uut/done

RTL Viewer - C:/Users/Albert/Desktop/Course Related/cse 140L/Project_Folder_qPrime_modelsim/Lab_1/Starter_Verilog/robsmult - robsmult

File Edit View Tools Window Help

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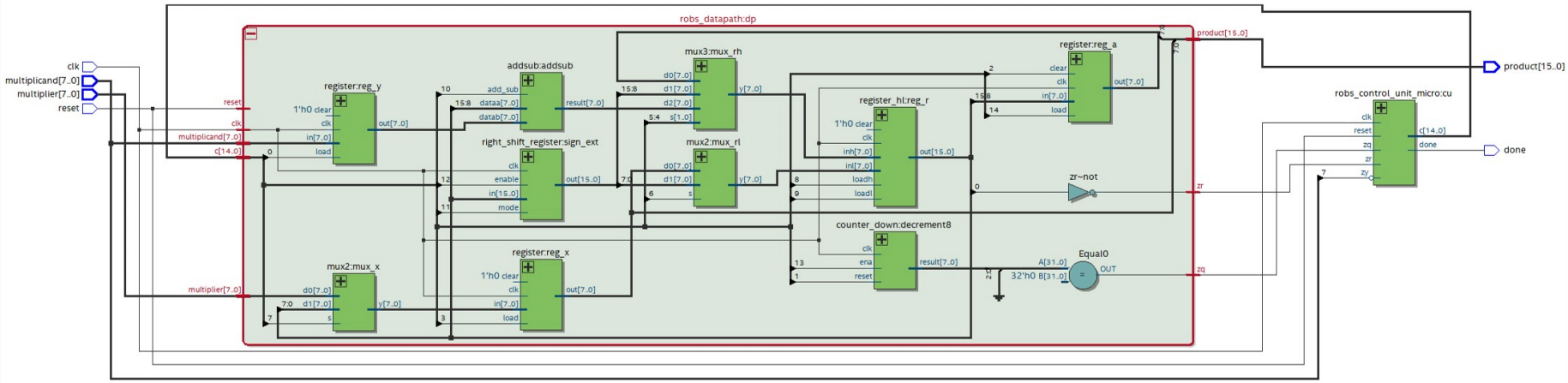
Page: 1 of 1

Netlist Navigator

- robsmult
  - Instances
    - robs_control_ui
    - robs_datapath:d
  - Ports

robsmult:1



100% 00:00:01

RTL Viewer - C:/Users/Albert/Desktop/Course Related/cse 140L/Project_Folder_qPrime_modelsim/Lab_1/Starter_Verilog/robsmult - robsmult

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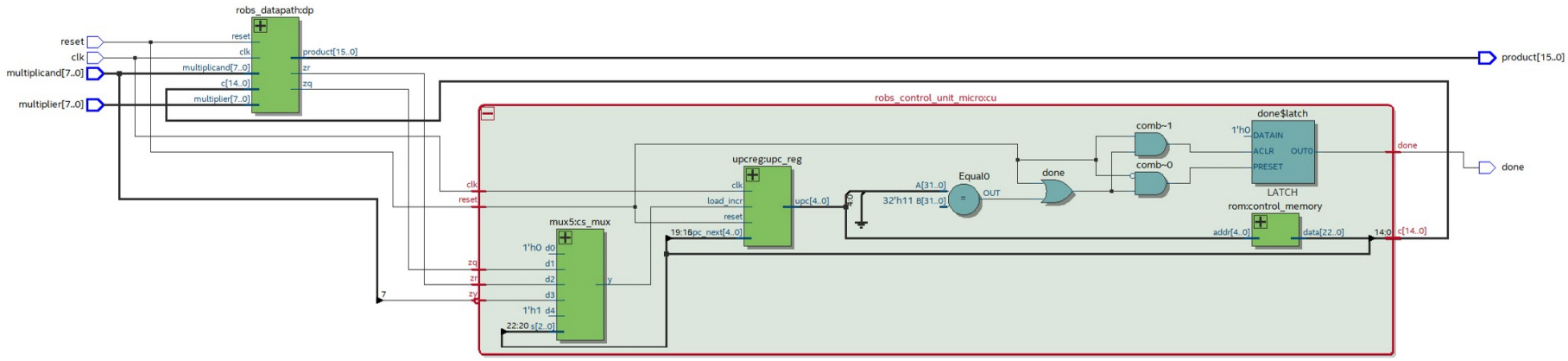
Page: 1 of 1

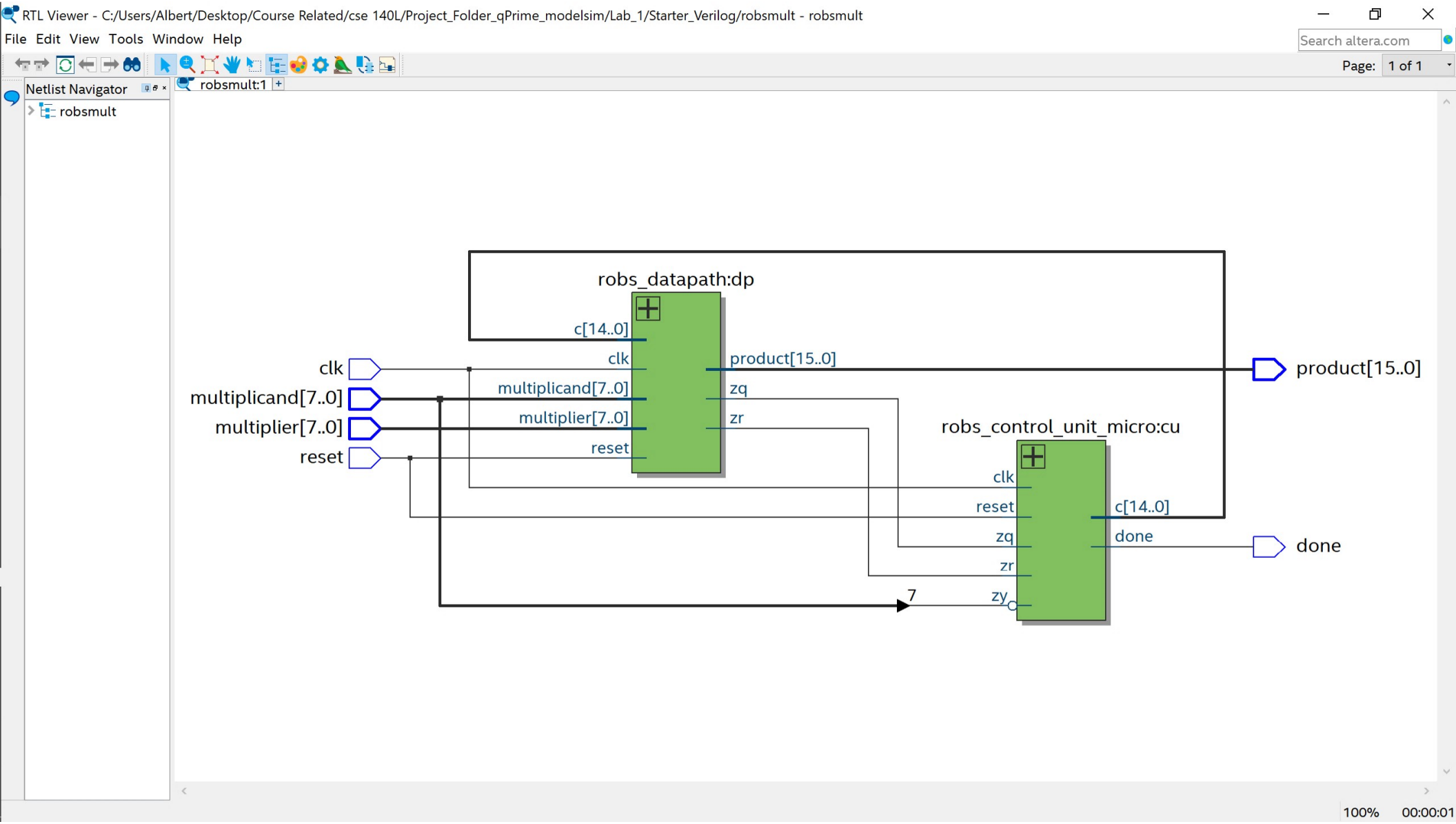
Netlist Navigator

- robsmult
  - Instances
    - robs_control_ui
    - robs_datapath:d
  - Ports

robsmult:1



100% 00:00:01


RTL Viewer - C:/Users/Albert/Desktop/Course Related/cse 140L/Project_Folder_qPrime_modelsim/Lab_1/Starter_Verilog/robsmult - robsmult
File Edit View Tools Window Help
Search altera.com
Page: 1 of 1
Netlist Navigator
robsmult
robsmult:1
robs_datapath:dp
c[14..0]
clk
multiplicand[7..0]
multiplier[7..0]
reset
product[15..0]
zq
zr
robs_control_unit_micro:cu
clk
reset
zq
zr
zy
c[14..0]
done
7
clk
multiplicand[7..0]
multiplier[7..0]
reset
product[15..0]
done
100%
00:00:01