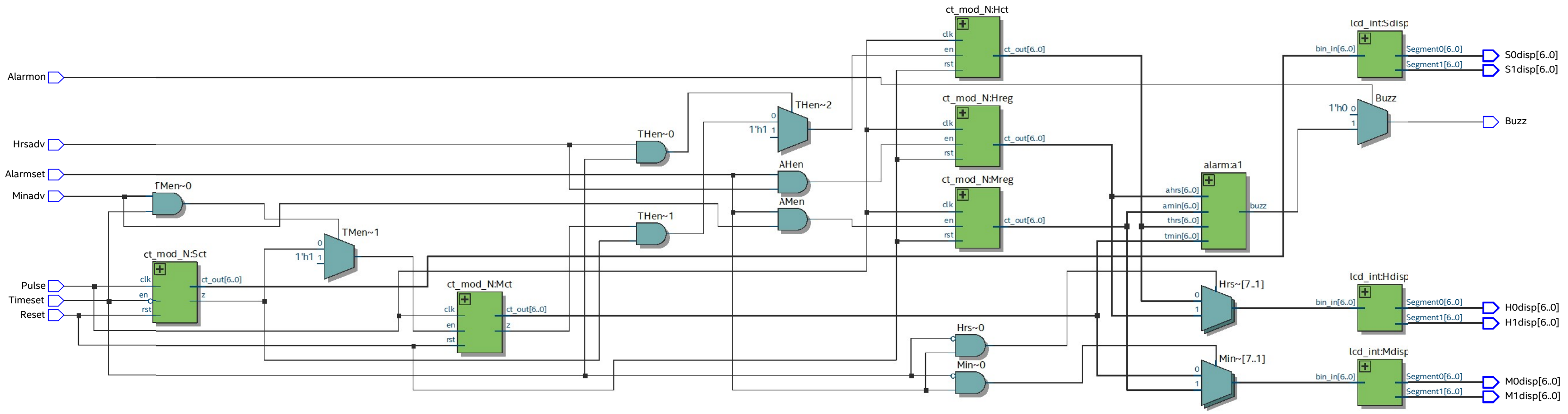
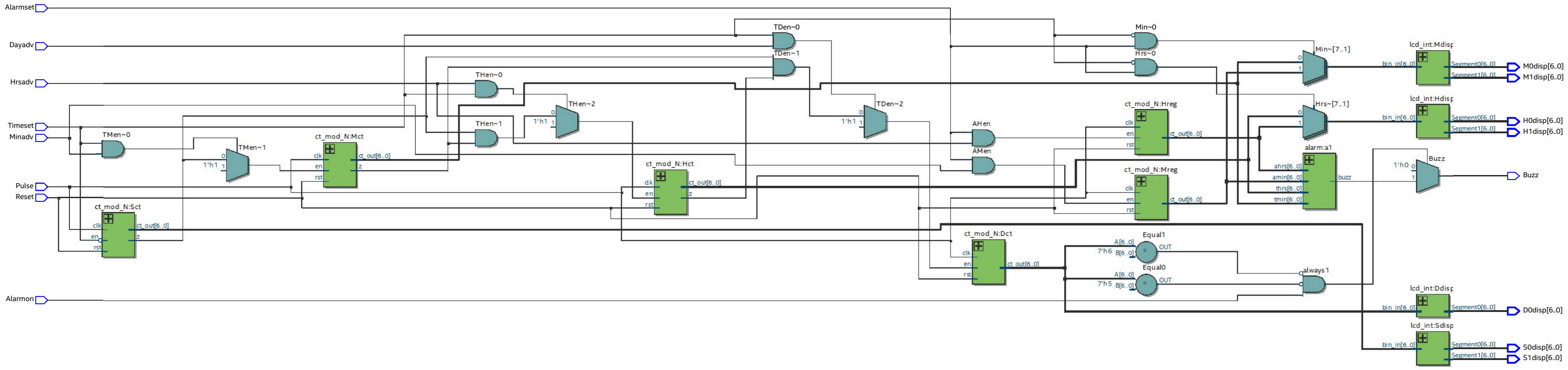
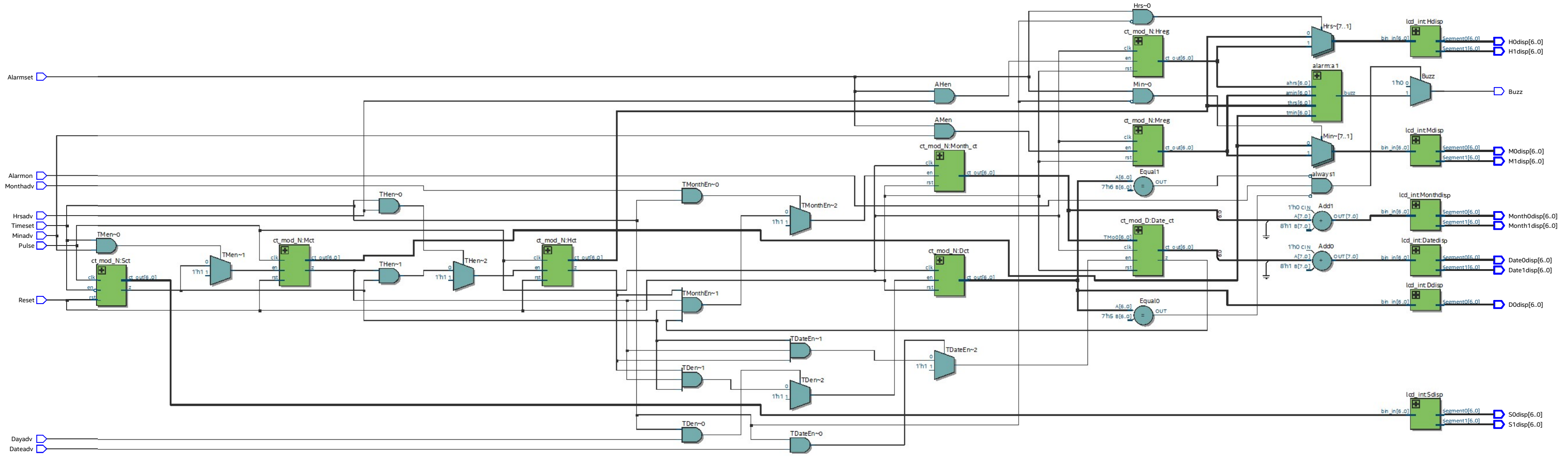

Alarmon
Hrsadv
Alarmset
Minadv
Pulse
Timeset
Reset
TMen~0
TMen~1
0
1'h1 1
ct_mod_N:Sct
clk
en
rst
ct_out[6..0]
z
ct_mod_N:Mct
clk
en
rst
ct_out[6..0]
z
THen~0
THen~1
THen~2
0
1'h1 1
AHen
AMen
ct_mod_N:Hct
clk
en
rst
ct_out[6..0]
ct_mod_N:Hreg
clk
en
rst
ct_out[6..0]
ct_mod_N:Mreg
clk
en
rst
ct_out[6..0]
Hrs~0
Min~0
alarm:a1
ahrs[6..0]
amin[6..0]
thrs[6..0]
tmin[6..0]
buzz
Hrs~[7..1]
0
1
Min~[7..1]
0
1
Buzz
1'h0 0
1
lcd_int:Sdisp
bin_in[6..0]
Segment0[6..0]
Segment1[6..0]
S0disp[6..0]
S1disp[6..0]
Buzz
lcd_int:Hdisp
bin_in[6..0]
Segment0[6..0]
Segment1[6..0]
H0disp[6..0]
H1disp[6..0]
lcd_int:Mdisp
bin_in[6..0]
Segment0[6..0]
Segment1[6..0]
M0disp[6..0]
M1disp[6..0]


Alarmset
Dayadv
Hrsadv
Timeset
Minadv
Pulse
Reset
Alarmon
TMen~0
TMen~1
0
1'h1 1
ct_mod_N:Sct
clk
en
rst
ct_out[6..0]
z
ct_mod_N:Mct
clk
en
rst
ct_out[6..0]
z
THen~0
THen~1
THen~2
0
1'h1 1
ct_mod_N:Hct
clk
en
rst
ct_out[6..0]
z
TDen~0
TDen~1
TDen~2
0
1'h1 1
AHen
AMen
Min~0
Hrs~0
ct_mod_N:Hreg
clk
en
rst
ct_out[6..0]
ct_mod_N:Mreg
clk
en
rst
ct_out[6..0]
ct_mod_N:Dct
clk
en
rst
ct_out[6..0]
Equal1
A[6..0]
7'h6 B[6..0]
OUT
Equal0
A[6..0]
7'h5 B[6..0]
OUT
always1
Min~[7..1]
0
1
Hrs~[7..1]
0
1
alarm:a1
ahrs[6..0]
amin[6..0]
thrs[6..0]
tmin[6..0]
buzz
Buzz
1'h0 0
1
lcd_int:Mdisp
bin_in[6..0]
Segment0[6..0]
Segment1[6..0]
M0disp[6..0]
M1disp[6..0]
lcd_int:Hdisp
bin_in[6..0]
Segment0[6..0]
Segment1[6..0]
H0disp[6..0]
H1disp[6..0]
Buzz
lcd_int:Ddisp
bin_in[6..0]
Segment0[6..0]
D0disp[6..0]
lcd_int:Sdisp
bin_in[6..0]
Segment0[6..0]
Segment1[6..0]
S0disp[6..0]
S1disp[6..0]

Date: November 11, 2021

Project: top_level_lab2_part3



Revision: top_level_lab2_part3

The given testbench was used to test the alarm clock.
Functionality of testbench;

the main testbench file lab2_part1_tb.sv ;
which consists of four blocks of alarm functionality tests.
initalizes core clock variables (such as those for display) locally , and assigns them with values to those such as Reset,Clk,Timeset,etc...
-top_level_lab2_part1 module is called to bring in our top-level logic.
-in each block of tests, display_tb() is called with its specified display parameters hours, minutes, seconds (each of 2bits).

As such,
-in the first block of tests (indicated by display() call), we see the inital current time after setting.
-in the second block, we begin setting the alarm (set alarm button is pressed - on).
as such, the current alarm time is displayed (before setting).
-in the third block, we actually set the alarm time with test values, display the newly set alarm time, and then stop setting the alarm (alarmset pressed again - off).
-in the fourth block, we have set the current time to just before the alarm time will go off. We display current time as it refreshes, then we see that the buzzer goes off for a duration beginning at the previously set alarm time. Finally, we continue with regular time display for some additional minutes to ensure our alarm and regular clock were properly working.

lab2_part1_display_tb.sv formats the outputs of given clock data into digits for display (as seen in the transcript) ; numerical 0-6 values are given a corresponding text representation (drawn out).

Much like how hours, minutes, and seconds were implemented.
Days (of the week) was implemented by adding the following functionailities ;
- An enable for timeset day which is on when Timeset and advancing of days is true, otherwise enable is set to the zero flags tracing rollovers.
- Days variable for output display, and assigning it to regular time
- A days counter, of mod 7 (for 7 days a week) which re-freshed regular clock time (incrementing it), and provided a flag when rollover of days.
- A display driver which took the inputs of Days, and corresponded a one bit 'segment' to actually represent the display in testbench outputs.
- Finally, we updated the condition for when the buzzer may ring.

Adding two conditions: that aslong as it is not day 5/6 (sat or sun), buzzer can ring.

Two enhancements were added to our clock; Date and Month.

The additional date enhancement allows our clock to now track and subsquently display the day of the month.
It's implementation includes ;
-Enable variable for clock time Date
-Assignment of display Date to regular clock Date, which is updating (incrementing) with every pulse.
-Variable date mod counter that selects from mod 28/30/31 days in a month, depending on the input provided by value of current month.
-Display lcd driver for Date, to display the current date as provided by our clock. As a result of implementing a mod counter, we feed the (Date value + 1) into the display driver, such that we don't end up displaying a 0th of the month.

The Month enhancement provides our clock with a method to track the current month of the cycle as a 2 digit decimal value.
implemented with the following pieces of functionality;
-Enable variable for clock time Month
-Assignment of display Month to regular clock Month
-Fixed mod 12 counter (for 12 months in a year),
-Display lcd driver to display the current month of our clock. Due to implementation of a mod counter, we feed (value of Month with + 1), such that we don't end up displaying a month 0 as the first month and month 11 as the last month of the year.

```
# WARNING: No extended dataflow license exists
run -all
# buzz = 0                    0
# buzz = 1                 1000
# buzz = 0                 5000
# display current time after setting
#  _   _    _   _    _   _
# | |   |  |_  |_   | |  _|
# |_|   |   _|  _|  |_| |_
# display alarm time before setting
#  _   _    _   _    _
# | | | |  | | | |  | | |_|
# |_| |_|  |_| |_|  |_|   |
# display alarm time after setting
#  _   _    _            _
# | | |_|  | |   |    | |_|
# |_| |_|  |_|   |    |  _|
# display current time after setting alarm
#  _   _    _   _    _
# | |   |  |_  |_    _|   |
# |_|   |   _|  _|  |_    |
#  _   _    _   _    _
# | |   |  |_  |_    _|   |
# |_|   |   _| |_|  |_    |
#  _   _    _   _    _
# | |   |  |_    |    _|   |
# |_|   |   _|   |  |_    |
#  _   _    _   _    _
# | |   |  |_  |_|   _|   |
# |_|   |   _| |_|  |_    |
#  _   _    _   _    _
# | |   |  |_  |_|   _|   |
# |_|   |   _|  _|  |_    |
#  _   _    _   _    _
# | | |_|  | | | |   _|   |
# |_| |_|  |_| |_|  |_    |
# buzz = 1               845000
#  _   _    _        _
# | | |_|  | |   |   _|   |
# |_| |_|  |_|   |  |_    |
# buzz = 0               965000
#  _   _    _   _    _
# | | |_|  | |  _|   _|   |
# |_| |_|  |_| |_   |_    |
#  _   _    _   _    _
# | | |_|  | |  _|   _|   |
# |_| |_|  |_|  _|  |_    |
#  _   _    _        _
# | | |_|  | | |_|   _|   |
# |_| |_|  |_|   |  |_    |
#  _   _    _   _    _
# | | |_|  | | |_    _|   |
# |_| |_|  |_|  _|  |_    |
# ** Note: $stop    : C:/Users/Albert/Desktop/Course Related/cse
140L/Project_Folder_qPrime_modelsim/Lab_2/Lab 2 Verilog/part1/lab2_part1_tb.sv(109)
#    Time: 4368 ns  Iteration: 0  Instance: /lab2_part1_tb
# Break in Module lab2_part1_tb at C:/Users/Albert/Desktop/Course Related/cse
140L/Project_Folder_qPrime_modelsim/Lab_2/Lab 2 Verilog/part1/lab2_part1_tb.sv line
109
```

```
# Errors: 0, Warnings: 0
# Compile of alarm.sv was successful.
# Errors: 0, Warnings: 0
# Compile of ct_mod_N.sv was successful.
# Errors: 0, Warnings: 0
# Compile of lab2_part2_display_tb_file.sv was successful.
# Errors: 0, Warnings: 0
# Compile of lab2_part2_tb_file.sv was successful.
# Errors: 0, Warnings: 0
# Compile of lcd_int3.sv was successful.
# Errors: 0, Warnings: 0
# Compile of top_level_lab2_part2.sv was successful.
vsim -gui work.lab2_part2_tb_file
# End time: 18:48:56 on Nov 11,2021, Elapsed time: 0:00:46
# Errors: 0, Warnings: 7
# vsim -gui work.lab2_part2_tb_file
# Start time: 18:48:56 on Nov 11,2021
# Loading sv_std.std
# Loading work.lab2_part2_tb_file_sv_unit
# Loading work.lab2_part2_tb_file
# Loading work.lab2_part2_top_level
# Loading work.ct_mod_N
# Loading work.lcd_int
# Loading work.alarm
# WARNING: No extended dataflow license exists
add wave -position insertpoint sim:/lab2_part2_tb_file/sd/*
run -all
# ** Note: $stop    : C:/Users/Albert/Desktop/Course Related/cse
140L/Project_Folder_qPrime_modelsim/Lab_2/Lab 2
Verilog/part2/lab2_part2_tb_file.sv(90)
#    Time: 263348 us  Iteration: 0  Instance: /lab2_part2_tb_file
# Break in Module lab2_part2_tb_file at C:/Users/Albert/Desktop/Course Related/cse
140L/Project_Folder_qPrime_modelsim/Lab_2/Lab 2 Verilog/part2/lab2_part2_tb_file.sv
line 90
```

```
  |  |_| |_|  |_|  _|  |_    |    BUZZ!!!

      _   _    _   _    _   _
|_|  | | |_|  | | |_    _|  _|
  |  |_| |_|  |_|  _|  |_  |_     BUZZ!!!

      _   _    _   _    _   _
|_|  | | |_|  | | |_    _|  _|
  |  |_| |_|  |_|  _|  |_   _|    BUZZ!!!

      _   _    _   _    _
|_|  | | |_|  | | |_    _| |_|
  |  |_| |_|  |_|  _|  |_    |    BUZZ!!!

      _   _    _   _    _   _
|_|  | | |_|  | | |_    _| |_
  |  |_| |_|  |_|  _|  |_   _|    BUZZ!!!

      _   _    _   _    _   _
|_|  | | |_|  | | |_    _| |_
  |  |_| |_|  |_|  _|  |_  |_|    BUZZ!!!

      _   _    _   _    _   _
|_|  | | |_|  | | |_    _|   |
  |  |_| |_|  |_|  _|  |_    |    BUZZ!!!

      _   _    _   _    _   _
|_|  | | |_|  | | |_    _| |_|
  |  |_| |_|  |_|  _|  |_  |_|    BUZZ!!!

      _   _    _   _    _   _
|_|  | | |_|  | | |_    _| |_|
  |  |_| |_|  |_|  _|  |_   _|    BUZZ!!!

      _   _    _   _    _   _
|_|  | | |_|  | | |_    _| | |
  |  |_| |_|  |_|  _|   _| |_|    BUZZ!!!

      _   _    _   _    _
|_|  | | |_|  | | |_    _|   |
  |  |_| |_|  |_|  _|   _|   |    BUZZ!!!

      _   _    _   _    _   _
|_|  | | |_|  | | |_    _|  _|
  |  |_| |_|  |_|  _|   _| |_     BUZZ!!!

      _   _    _   _    _   _
|_|  | | |_|  | | |_    _|  _|
  |  |_| |_|  |_|  _|   _|  _|    BUZZ!!!
```

```
      _   _     _   _     _
|_|  | | |_|  | | |_    _| |_|
  |  |_| |_|  |_|  _|   _|   |   BUZZ!!!

      _   _     _   _     _   _
|_|  | | |_|  | | |_    _| |_
  |  |_| |_|  |_|  _|   _|  _|   BUZZ!!!

      _   _     _   _     _   _
|_|  | | |_|  | | |_    _| |_
  |  |_| |_|  |_|  _|   _| |_|   BUZZ!!!

      _   _     _   _     _   _
|_|  | | |_|  | | |_    _|   |
  |  |_| |_|  |_|  _|   _|   |   BUZZ!!!
(5=Saturday) Day increase successfully by hours reaching 24
 _    _   _    _   _    _   _
|_   | |   |  |_  |_|  |_  |_|
 _|  |_|   |   _| |_|   _| |_|
 _    _   _    _   _    _   _
|_   | |   |  |_  |_|  |_  |_|
 _|  |_|   |   _| |_|   _|  _|
 _    _   _    _   _    _   _
|_   | |   |  |_  |_|  | | | |
 _|  |_|   |   _|  _|  |_| |_|
 _    _   _    _   _    _
|_   | |   |  |_  |_|  | |   |
 _|  |_|   |   _|  _|  |_|   |
 _    _   _    _   _    _   _
|_   | |   |  |_  |_|  | |  _|
 _|  |_|   |   _|  _|  |_| |_
 _    _   _    _   _    _   _
|_   | |   |  |_  |_|  | |  _|
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|_   | |   |  |_  |_|  | | |_|
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 _|  |_|   |   _|  _|  |_|  _|
 _    _   _    _   _    _   _
|_   | |   |  |_  |_|  | | |_
 _|  |_|   |   _|  _|  |_| |_|
 _    _   _    _   _    _   _
|_   | |   |  |_  |_|  | |   |
 _|  |_|   |   _|  _|  |_|   |
 _    _   _    _   _    _   _
|_   | |   |  |_  |_|  | | |_|
 _|  |_|   |   _|  _|  |_| |_|
# Errors: 0, Warnings: 0 C:/Users/Albert/Desktop/Course Related/cse
140L/Project_Folder_qPrime_modelsim/Lab_2/Lab 2
Verilog/part3/top_level_lab2_part3.sv Line: 189
# WARNING: No extended dataflow license exists
run -all
# 5': before setting. '010100000', Jan 1,                 4000
#  _        _        _    _   _    _   _
# | |   |  | |   |  | |  | | | |  | | | |
# |_|   |  |_|   |  |_|  |_| |_|  |_| |_|
# 5':after setting,'1231', manually increment date/month successful
68000
#      _    _        _    _   _    _   _
#   |  _|   _|   |  | |  | | | |  | | | |
#   | |_    _|   |  |_|  |_| |_|  |_| |_|
# 5': '010100',passively increment date/month successful, also testing range month
1-12, date from 1            172868000
#  _        _             _   _    _   _
# | |   |  | |   |    |  | | | |  | | | |
# |_|   |  |_|   |    |  |_| |_|  |_| |_|
# 5'---------------testing mod-----------
# testing Feb has 28 days:'0228'            172926000
#  _   _    _   _         _   _    _   _
# | |  _|   _| |_|    |  | | | |  | | | |
# |_| |_    |_  |_|    |  |_| |_|  |_| |_|
# 0301
#  _   _    _        _    _   _    _   _
# | |  _|  | |   |   _|  | | | |  | | | |
# |_|  _|  |_|   |  |_   |_| |_|  |_| |_|
# testing April has 30 days: '0430'            345788000
#  _        _   _    _    _   _    _   _
# | | |_|   _| | |   _|  | | | |  | | | |
# |_|   |   _| |_|  |_   |_| |_|  |_| |_|
# 5 points: 0501            518588000
#  _   _    _        _    _   _    _   _
# | | |_   | |   |   _|  | | | |  | | | |
# |_|  _|  |_|   |   _|  |_| |_|  |_| |_|
# ** Note: $stop    : C:/Users/Albert/Desktop/Course Related/cse
140L/Project_Folder_qPrime_modelsim/Lab_2/Lab 2 Verilog/part3/lab2_part3_tb.sv(101)
#    Time: 518688 ns  Iteration: 0  Instance: /lab2_part3_tb
# Break in Module lab2_part3_tb at C:/Users/Albert/Desktop/Course Related/cse
140L/Project_Folder_qPrime_modelsim/Lab_2/Lab 2 Verilog/part3/lab2_part3_tb.sv line
101
```