Adrian Bao

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Education

UC Berkeley June 2022 – May 2025
Bachelor of Arts in Computer Science *Berkeley, CA*

Experience

Undergraduate Student Instructor Aug 2024 – Present
University of California, Berkeley *Berkeley, CA*

- Created and gave lectures about Docker and Kubernetes to over 60 students
- Designed interactive labs and quizzes to maximize knowledge retention
- Assisted students with technical questions on in-person and online channels
- Managed grading and course logistics

Data Center Manager Intern May 2024 – Aug 2024
Amazon Web Services, Inc. *Columbus, OH*

- Implemented Lambda-based scheduling features in global ticketing system
- Enabled scheduled ticket automation actions with EventBridge Scheduler
- Created insightful metrics analytics and visualizations with Sagemaker
- Designed JTAG-based debugging tool to troubleshoot malfunctioning devices
- Increased data center cluster-wide SLA compliance by 8%

Software Development Engineer Intern Oct 2023 – Dec 2023
YiVal, Inc. *Berkeley, CA*

- Led and managed multinational team of software engineers
- Implemented and enhanced multi-modal generative AI models and algorithms
- Optimized code deployment and testing with CI/CD system by 30%
- Developed internal and external technical documentation and blog posts

Student Researcher Aug 2019 – Mar 2023
Stanford University *Stanford, CA*

- Created Nvidia Jetson Nano robot with Pytorch AI obstacle-avoiding model
- Created R models to represent and analyze effects of temperature on insulin growth
- Created Q-learning model to optimize the amplification of inverting amplifiers
- Created a neural network that solved anti-bot CAPTCHA challenges

Projects

x86 Operating System | *C, Assembly (x86)* Aug 2024 - Dec 2024

- Implemented file, process, and math syscalls
- Implemented priority scheduling and donation
- Implemented user-level threading
- Implemented buffer cache
- Implemented Unix FFS-style file system pointers

RISC-V SoC Design | *Logisim, Vivado, Verilog* Mar 2024 - Present

- Designed single-core RISC-V CPU in Logisim
- Implemented ALU, RegFile, Immediate Generator, and Datapath
- Implemented 2-stage pipelining
- Implemented comprehensive unit tests
- Currently implementing RISC-V SoC on a Zynq-7000 FPGA

Technical Skills

Frameworks: ESP-IDF, OpenOCD, FreeRTOS, Pytorch
Languages: C/C++, Verilog, Python, Java, JavaScript/TypeScript
Developer Tools: Git, Docker, Kubernetes, Linux, AWS, Vitis, Vivado