Qian Cui

Personal Data

Place and Date of Birth:	China | 18 June 1984
Phone:	+86 13811860684
email:	cuibuaa@gmail.com

Work Experience

Jan 2013 - Present	**Embedded Engineer** at **Samsung Electronics**, Beijing Develop Linux wireless driver and software architecture of firmware for Samsung wiGig (*a new wireless technology based on 60Ghz*) chip. A report for this work: Samsung wiGig News Port kernel to Samsung devices, responsible for optimization of power management on heterogeneous system (ARM A15 and A7)
Dec 2009 - Dec 2012	**FPGA Engineer** at **Space Star Co. Ltd**, Beijing Design parallel architecture and high-speed I/O solution including FPGA logic and hardware circuit

Education

Sep 2007 - Dec 2009	Master of Computer Architecture in Computer Science **BeiHang University**, Beijing Thesis: "High-Performance Data Exchange Mechanism for PSDM (Prestack Depth Migration) Hardware Accelerator"
Sep 2003 – Jul 2007	Undergraduate Degree in Computer Science **BeiHang University**, Beijing Thesis: "Application in Distributed Systems with Domain Specific Languages Click"

Projects

Nov 2013 - Present	**wiGig wireless Linux driver and software architecture** Optimize cache access efficiency during DMA operation Optimize DMA operation by pipelined DMA ring Optimize socket transmission for jumbo frames Get final throughput: 3.0Gbps in UDP, 2.5Gbps in TCP
Jan 2013 - Oct 2013	**Kernel porting and power optimization for Samsung Exynos 5410 chip (four A15 cores and four A7 cores)** Port kernel and uboot to Exynos 5410 chip Analyse and optimize network performance with a thread monitoring the net throughput to choose different mechanisms (*only A7/only A15/mixed*)
May 2011 - Dec 2012	**High-Speed prototype system based on PCI/PCI-E bus** Design DMA Engine based on Weighted Round Robin strategy, achieving up to 9Gbps throughput Design hardware circuit and software of data capture system based on PCI/PCI-E bus(*including FPGA logic and driver*)

Jan 2010 - Apr 2011	**Optimization Viterbi and RS decoding algorithm** Implement Viterbi decoding parallel architecture based on Ping-Pong buffering strategy Implement RS decoding parallel architecture based on interleaving dividing strategy
Oct 2008 - Dec 2009	**863 project "Reconstruction Accelerator"** Design a duplex mode memory controller based on fair schedule strategy Design a parallel architecture for PSDM (*Prestack Depth Migration*) algorithm
Sep 2007 - Sep 2008	**Wormhole Router on SOC** Design a new network modeling tool DClick for network on chip

Issued Patents

Jun 2011	CN 102361460 A (*in Chinese*) General high-speed parallel cycle interleaving Viterbi decoding method Translated by Google
Sep 2010	CN 101969358 A (*in Chinese*) High-speed parallel RS decoding method for space communication Translated by Google

Publications

- Qian Cui, Xiaopeng Gao, Xiang Long. Design and Implementation of PCI Express DMA Controller Based on Weighted Round Robin Policy (*in Chinese*). Microcomputer Information, 2010, 26(23):147-149.
- Zhe Zhang, Qian Cui, Xiaopeng Gao, Xiang Long. Modeling Network Application for Multi-Core Architecture (*in Chinese*). Microelectronics & Computer, 2007, 24(10):39-42.

Awards

- Excellent Master's Thesis (17/203), *BeiHang University* 2010
- Second Prize for FengRu Cup Contest (6/57), *BeiHang University* 2006

Skills

- Over 50,000 Lines: C/Verilog/Shell
- Over 10,000 Lines: Python/Java
- TOFEL: Total 83/120 Reading 19 Listening 26 Speaking 18 Writing 20