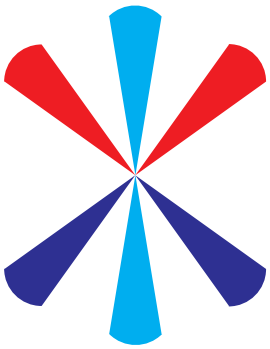

Calterah Alps CAL77S244-AB/IB Hardware Design Guide

Release 1.0

Calterah Semiconductor

Oct 09, 2020

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CHAPTER

ONE

ABOUT THIS DOCUMENT

The purpose of this document is to help Calterah's customers to start a design based on Alps AiP (CAL77S244-AB/IB).

Calterah Alps family includes:

- CAL77S224-AE, a 2T4R radar sensor chip
- CAL77S244-AE, a 4T4R radar sensor chip
- CAL77S244-AB/IB, antenna-in-package (AiP) radar sensor chips with 4 TX and 4 RX antenna array embedded in the package.

  The difference between CAL77S244-IB and CAL77S244-AB is that CAL77S244-IB is an industrial product and does not support CAN or CAN FD functions, while CAL77S244-AB supports CAN and CAN FD functions.

This document focuses only on CAL77S244-AB/IB. For information about hardware design based on CAL77S224-AE and CAL77S244-AE, refer to *Calterah Alps CAL77S224-AE/CAL77S244-AE Hardware Design Guide*.

CHAPTER

TWO

SCHEMATIC DESIGN

2.1 System Block Diagram

Alps AiP is an innovative design with 4 TX and 4 RX antenna array embedded in the package. Alps AiP inherits all Alps 4T4R radar SoC features. Fig. 2.1 and Fig. 2.2 illustrates the connections and parts for Alps CAL77S244-AB and CAL77S244-IB respectively. The solid line parts are necessary.

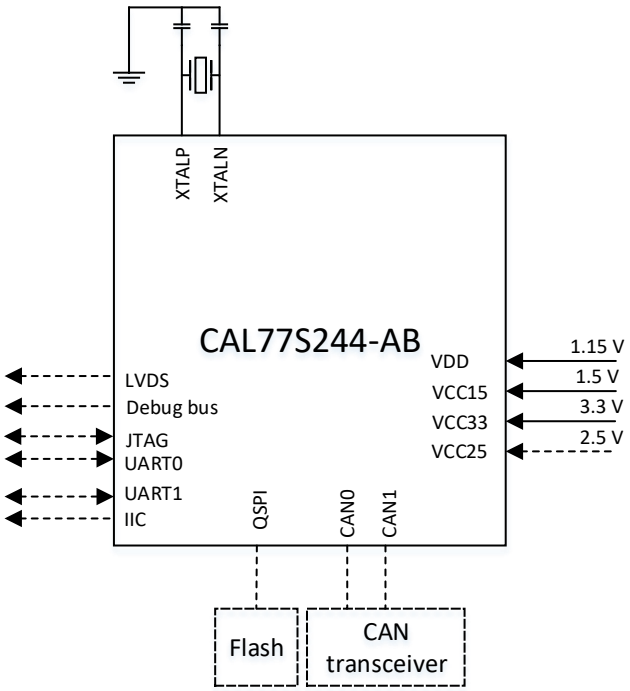

Fig. 2.1: Alps CAL77S244-AB System Block Diagram

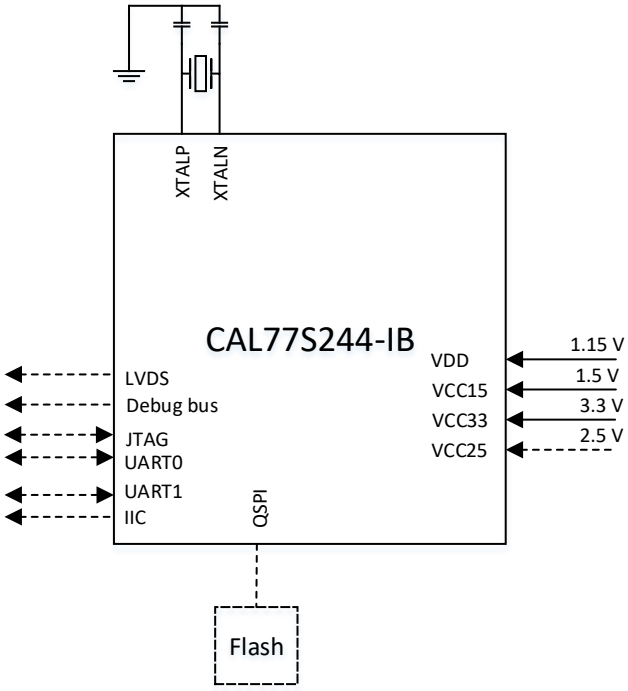

Fig. 2.2: Alps CAL77S244-IB System Block Diagram

2.2 Power Supply

For full features, Alps needs four power supplies for normal operation: 1.15 V, 1.5 V, 2.5 V and 3.3 V. Connect the power pins according to Table 2.1. If you do not use OTP writing function, leave the VDD25_OTP pin floating.

Table 2.1: Power Pin Connection Checklist

Supply	Blocks Powered by Supply	Relevant I/Os
3.3 V	Digital I/Os, Buffers, DACs, PFD, Charge Pump, VGA1, VGA2, CBC, LVDS, POR	VDD33_LVDS, VDD33_ADC, VDD33_FMCWPLL, VDD33_REFPLL, VDD33_CBC, VDD33_RX
2.5 V	OTP memory	VDD25_OTP
1.5 V	Amplifiers, Comparators, VCO, MMD, Mixers, LO, TIA, TX, PA, PMU	VDD15_ADC, VDD15_FMCWPLL, VDD15_REFPLL, VDD15_VCO, VDD15_LO, VDD15_CBC, VDD15_RXN, VDD15_RXS, AVDD15_TX
1.15 V	CPU, SRAMs, Digital Logic	VDD

Table 2.2 gives the current consumption of each power supply rail for Alps AiP. The 1.5-V power supply should come from LDO. If you use LDO, pay attention to the LDO power dissipation.

Table 2.2: Current Consumption under Each Power Supply Rail

Parameter	Description	Min	Typ	Max	Unit
I_{DD33}	Total current under 3.3-V supply	/	140	180	mA
I_{DD25}	Total current under 2.5-V supply	/	40	/	mA
I_{DD15}	Total current under 1.5-V supply	/	1050	1300	mA
I_{DD11}	Total current under 1.15-V supply	/	260	600[1]	mA

Alps SoC power-on timing is shown in Fig. 2.3.

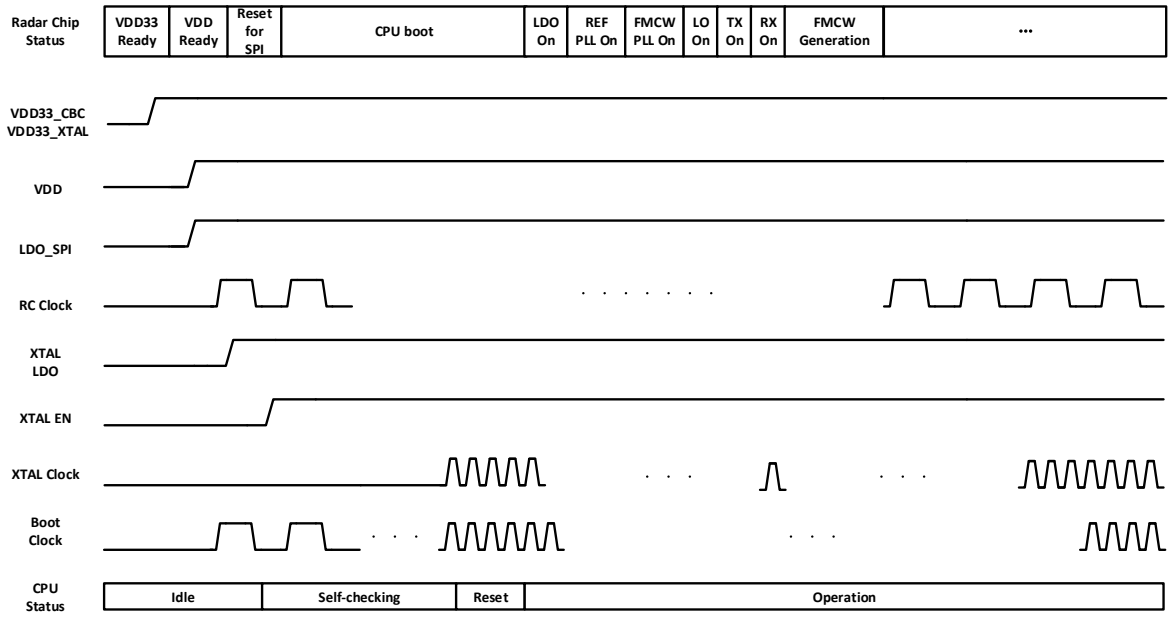

Fig. 2.3: Alps Power-on Timing

Note: The VDD power supply should only be powered on after VDD33 reaches its minimum requirement of being 3.14 V.

2.3 Clock

A 50-MHz clock source is required for Alps. Crystal, oscillator and external clock sources are supported. When a crystal is used, two load capacitors are necessary. The capacitance depends on the crystal used. 3.3pF is used in the reference design with a TXC AY50000001 crystal. Table 2.3 lists the electrical characteristics of the clock crystal. To get more qualified devices, refer to the Second Source List provided by Calterah.

[1] Maximum instantaneous peak current is up to 850 mA.

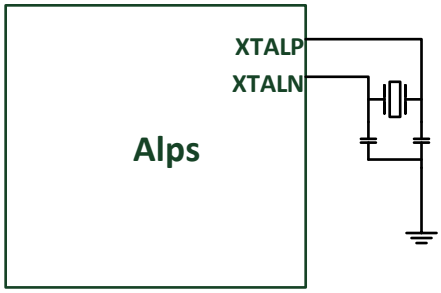

Fig. 2.4: Crystal Clock Source

Table 2.3: Crystal Electrical Characteristics

Description	Symbol	Min	Typ	Max	Unit
Nominal frequency	FL	/	50	/	MHz
Load capacitance	CL	/	4	/	pF
Operating temperature	/	-40	/	125 (for CAL70S244-AB) 105 (for CAL70S244-IB)	°C
Effective resistance	Rr	/	/	55	Ω
Drive level	DL	/	/	200	μW

When the oscillator or external clock is from an external device, the input should be a 2.5- to 3.3-V CMOS compatible signal with DC coupling. The phase noise of the oscillator or external clock should satisfy the specifications shown in Table 2.4. The clock signal should be connected to XTALP, and XTALN should be left floating.

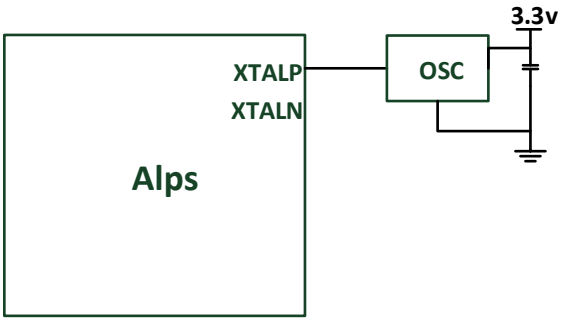

Fig. 2.5: Oscillator Clock Source

Table 2.4: Phase Noise Specifications of Oscillator and External Clock

Description	Max
Phase noise @ 1 kHz	-132 dBc/Hz
Phase noise @ 10 kHz	-146 dBc/Hz
Phase noise @ 100 kHz	-155 dBc/Hz
Phase noise @ 1 MHz	-155 dBc/Hz

2.4 SPI Interfaces

Alps includes five groups of SPI interfaces as shown in Table 2.5. Alps QSPI is connected with the flash. The SPI Slave1 can only be used as analog control SPI, which can control analog modules even if the digital core is not working. The SPI Slave1 **cannot** be used for SPI data transmission for the CPU. Refer to *Calterah Alps CAL77S244-AB/IB Datasheet* for the pin mux functions.

Table 2.5: Five Groups of SPI in Alps AiP

Group Description	Pin Number	Ball Location
SPI Master0	SPI_M0_CLK	V16
	SPI_M0_SEL	V15
	SPI_M0_MOSI	T13
	SPI_M0_MISO	V13
SPI Master1	SPI_M1_MISO	T11
	SPI_M1_MOSI	U10
	SPI_M1_SEL_0	T10
	SPI_M1_SEL_1	V9
	SPI_M1_SEL_2	T9
	SPI_M1_CLK	U9
QSPI	QSPI_M_DAT_0	U8
	QSPI_M_DAT_1	U7
	QSPI_M_DAT_2	V5
	QSPI_M_DAT_3	T8
	QSPI_M_SEL	U4
	QSPI_M_CLK	T7
SPI Slave0	SPI_S_CLK	P16
	SPI_S_MISO	P18
	SPI_S_SEL	R18
	SPI_S_MOSI	P15
SPI Slave1	SPI_S1_MISO	R16
	SPI_S1_MOSI	R17
	SPI_S1_SEL	T18
	SPI_S1_CLK	R15

2.5 LVDS Interfaces

Alps LVDS signal includes six differential pairs:

- LVDS1OP and LVDS1ON
- LVDS2OP and LVDS2ON

- LVDS3OP and LVDS3ON
- LVDS4OP and LVDS4ON
- LVDSCLKP and LVDSCLKN
- LVDSFRMP and LVDSFRMN

LVDS is used for outputting Alps ADC RAW data for further analysis done by the data capture system. LVDS works in DDR mode and the LVDSCLK frequency is 200 MHz. Each LVDS channel has a data rate of 400 MHz. Add a 100-ohm termination resistor depending on the LVDS receiver.

2.6 Debug Bus Interfaces

Alps has debug bus interfaces, including GPIO_DAT[19:0], GPIO_CLK, and GPIO_VAL. The debug bus can be used for outputting ADC RAW data or the FFT results after FFT. The maximum output GPIO_CLK frequency is 100 MHz. Debug bus pins have mux functions. Refer to *Calterah Alps CAL77S244-AB/IB Datasheet* for pin mux functions.

2.7 Other Interfaces

The RSTN_HARD signal should be pulled-up to 3.3 V by a resistor of 10k ohm.

The TEST_EN signal should be pulled-down to ground by a resistor of 1k ohm. When the TEST_EN signal is pulled-up, Alps enters the test mode.

The CAN_CLK_EXT is used for external clock input for the CAN module of Alps CAL77S244-AB.

The default status of the ERROR and SAFE STATE pins is high output. When an error occurs, the output is low.

2.8 Test Functions

Alps provides test functions for sanity check on the final product. There are 4 analog test pins: TPANA, VIO, TESTMUXP, and TESTMUXN. TPANA is an output pin which can output the control voltage curve of VCO. VIO can be used to test reference PLL performance. TESTMUXP and TESTMUXN can be used for 2 different purposes. One is using them as differential input of analog baseband. The analog baseband characteristics can be obtained with a proper input signal. The other is using them as IQ IF input signal on the mixer. The up-converted signal will be transmitted by TX and the reflected signal will be received by RX. This test function can be used to verify that the entire signal path is working normally.

2.9 Auxiliary ADCs

Alps includes two Auxiliary ADCs (AUX ADCs) for customers. The input voltage range of AUX ADCs is 0.5 V-2.5 V. TESTMUXP, TESTMUXN, and TPANA can be used for any AUX ADC input with internal multiplexing. For more detailed register settings, refer to *Calterah Alps Radio User Guide*.

2.10 Other Peripheral Functions

The Alps supports the following peripheral functions:

- JTAG * 1

- UART * 2
- I^{2}C master * 1
- CAN * 2

Note: CAL77S244-IB does not support CAN functions.

- PWM * 2

2.11 Strapping Pin Functions

The boot loader checks the status of strapping IOs to decide which specific mode to enter. By default, the strapping pins are set to weak pull up. To change the SOP mode, one needs to add the pull down option to the board schematic design.

Refer to Table 2.6 for the strapping pin values for each mode. SOP[0], SOP[1], and SOP[5] control the security status, which should match the system security setting. The default status of SOP[0], SOP[1] and SOP[5] pins should be high.

Make sure that UART boot mode is achieved through the UART0 interface, CAN boot mode is achieved through the CAN0 interface, and SPI boot mode is achieved through the SPI_S_SALVE interface.

Table 2.6: Strapping Pin Settings

SOP	Pad	Function	Description
SOP[5]	SPI_S_CLK	Security disable	0: Do not disable Security 1: Disable Security
SOP[4]	SPI_M1_SEL_2	Boot	000: Flash boot mode 100: UART boot mode 101: SPI boot mode 110: CAN boot mode[2]
SOP[3]	SPI_M1_SEL_1		
SOP[2]	SPI_M1_SEL_0		
SOP[1]	SPI_M1_MOSI	EMU	00: MODE0 Normal 01: MODE1 Bypass PreTest 10: MODE2 Bypass SS1 and SS2 11: MODE3 Bypass PreTest, SS1 and SS2
SOP[0]	SPI_M1_MISO		

2.12 Unused Pins

Function pins should be left floating with a test pad when its related function is not used.

[2] Alps CAL77S244-IB does not support CAN functions.

CHAPTER

THREE

LAYOUT CONSIDERATION

3.1 PCB Stack-Up

The four RX antennas and four TX antennas are located in Alps AiP package as shown in Fig. 3.1. The antenna direction of polarization is vertical.

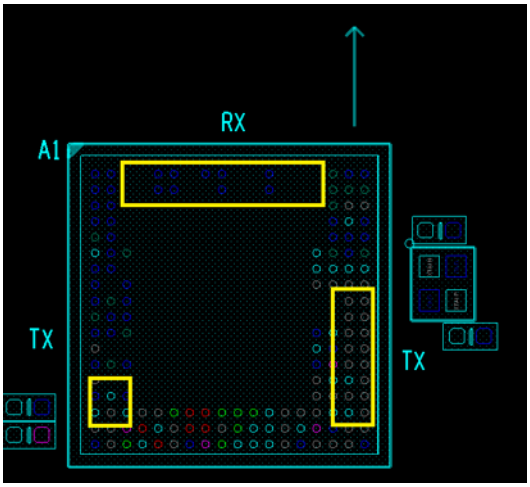

Fig. 3.1: Alps AiP Antenna Array

Alps AiP package is optimized for cost-efficient PCB. All signals can be fanned out easily without any special manufacture process.

The PCB for Alps AiP can be designed as 4 layers with through-VIAs, using standard FR4.

- Alps AiP should be placed on the top layer. And to enhance heat dissipation, sufficient VIAs should be placed under Alps AiP chip as shown in Fig. 3.2.
- The second layer and the third layer can be used for power supplies and signal lines.
- The bottom layer can be used for placing the power IC and power supplies.

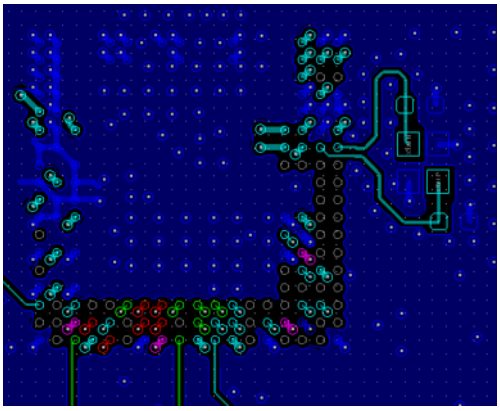

Fig. 3.2: Top Layer with Alps AiP and Sufficient Through-VIAs under Chip

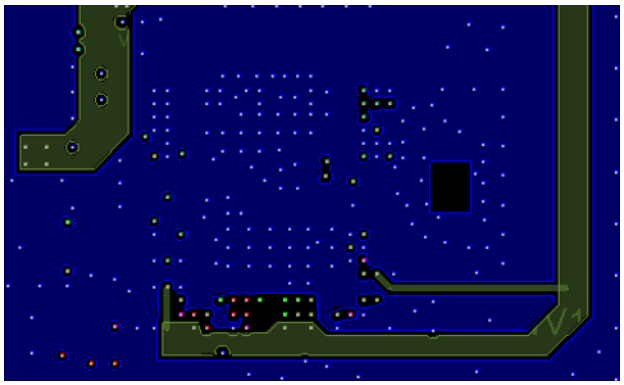

Fig. 3.3: The Second Layer

3.2 Power Supply Connection

Power supply can be routed as plane or trace. When 4 TX channels are all on at the same time, the maximum sinking current is about 1300 mA from 1.5 V. Pay attention to current-carrying capability to avoid temperature rise and voltage drop.

When placing decoupling capacitors, make sure to put them close to corresponding pins. Especially for AVDD15_REFPLL, AVDD15_FMCWPLL, and AVDD15_VCO, to get better PLL performance, the decoupling capacitors must be placed as close as possible to their corresponding power pins. To get a better thermal dissipation performance, put as many ground VIAs as possible in chip area.

DCDC may interfere the sensitive sources, such as the crystal, oscillator, oscillator supply, and LDO output. Generally, the DCDC LX node and DCDC input power are the dirtiest because of the current discontinuity. Pay attention to this point and refer to the documentation provided by the supplier of the used power IC. Fig. 3.4 displays the reference design of PMIC layout.

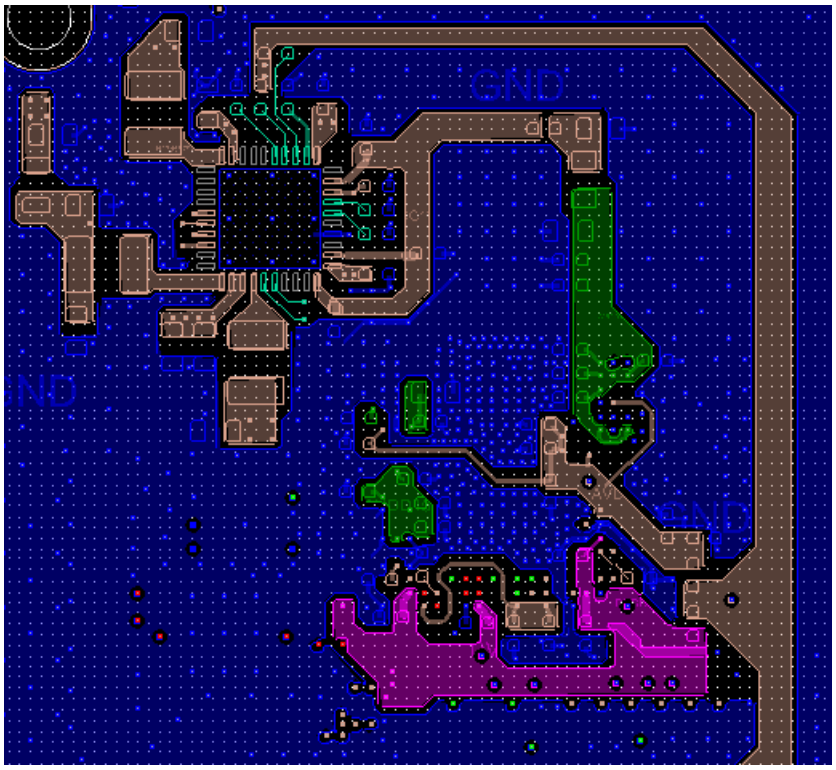

Fig. 3.4: PMIC Layout in Reference Design

Different power planes should avoid direct coupling, including adjacent layer coupling and the same layer coupling. The AVDD15 power plane should be well protected, kept away from the DCDC LX node and DCDC input power planes. Fig. 3.5 displays the layout of different power planes in the reference design.

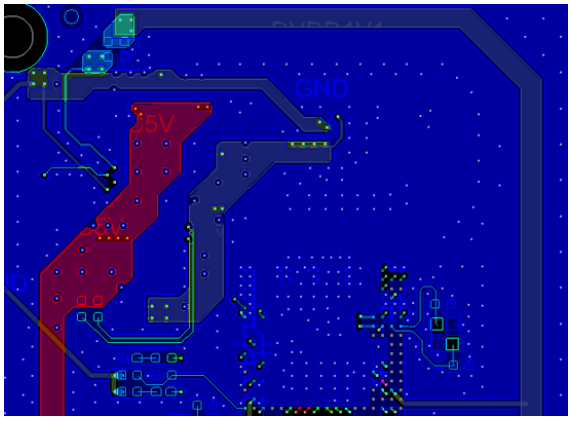

Fig. 3.5: Layout of Different Power Lanes in Reference Design

3.3 Clock

When a crystal is used, the trace routed to the crystal should be as short as possible and the copper under the signal pad is recommended to be cut out to reduce parasitic capacitance and heat propagation. Fig. 3.6 displays the crystal layout in the reference design.

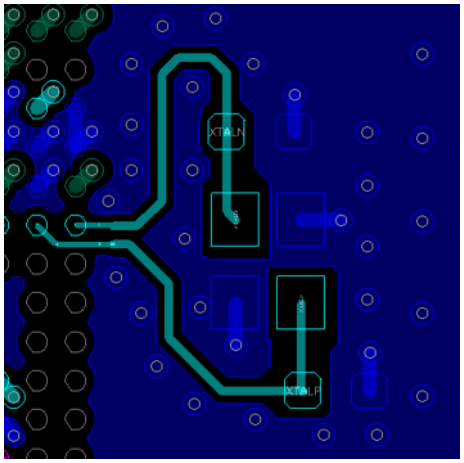

Fig. 3.6: Crystal Layout in Reference Design

When an oscillator is used, the clock signal line should be protected by ground and it should not go parallel with analog signals for a long distance, even if they are not in the same layer.

Try to increase the distance between the crystal or oscillator and the interfering source such as DCDC converter.

3.4 Digital Interfaces

In the layout design, the six pairs of differential LVDS signal lines should have an equal length with minimum spacing. The LVDSCLK should be shielded by the ground.

In the layout design, the debug bus traces should be routed with the length differences less than 100 mil.

3.5 Thermal Design

Thermal design must ensure that the operating junction temperature of Alps AiP chip is below 125°C. See Table 3.1 for thermal resistance characteristics of Alps AiP.

Table 3.1: Thermal Resistance Characteristics

Thermal Metrics	°C/W
ΘJA Junction-to-Free_air	58.06
ΘJMA Junction-to-Moving_Air	NA
ΨJT Junction-to-Package_top	2.39
ΨJB Junction-to-Board	3.64

Thermal design is highly relevant with system design. Besides expanding the PCB size, the following gives some other suggestions for your reference:

- On the back of Alps AiP, do not place heat sources (such as PMIC, LDO, and flash). It is OK to place some passive components, but it is better to place a big ground plane.
- Place as many ground holes under Alps AiP as possible. Note that through holes have better heat dissipation than blind holes.
- Use the metal back cover to conduct the heat of PCBA.

- Add solder mask for better heat dissipation.
- Reduce unnecessary power dissipation with proper design, such as reducing LDO input voltage.
- Combined with the in-chip temperature sensor, the software can dynamically adjust the number of TX channels, power level, and duty cycle for power saving when necessary.
- Thermal simulation is recommended for evaluating the system thermal condition.

APPENDIX

A

REVISION HISTORY

Table A.1: Revision History

Revision	Description	Author
0.9/ February 2020	Preliminary release for the mass production version of Alps AiP (CAL77S244-AB/IB).	pwang
1.0/ October 2020	Official release for the mass production version.	pwang

APPENDIX

B

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