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CMOS MMIC Ready for Road – A Technology Overview

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While solving the challenges of integrating high frequency front ends on CMOS process, TI has leveraged the traditional advantages of CMOS solutions in terms of higher transistor density and low power to create a compelling family of mmWave devices. This application report enumerates some of these challenges, respective solutions and advantages of CMOS as leveraged in TI mmWave Sensing devices.

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1 Introduction

Over the years, complementary metal-oxide semiconductor (CMOS) technology has been popular for wireless transceiver chips with integrated radios, as evidenced by multiple chipsets in volume production. These integrated circuits (ICs) enable a variety of applications such as *Bluetooth*®, wireless local area networks (LAN), GPS and, 4G Long Term Evolution (LTE) operating in a range of frequencies up to 6 GHz. However, circuits in the millimeter-wave (mmWave) regime (30-300GHz) have been the domain of heterojunction technologies such as silicon germanium (SiGe) bipolar CMOS (BiCMOS), as operation in themmWave regime requires faster transistors and high-quality passives.

Given technology scaling and Moore's Law, transistors using ultra-deep submicron CMOS technology now boast high-enough unity current gain frequency (f_T) and maximum oscillation frequency (f_{MAX}) numbers (metrics of transistor speed). Coupled with innovations at the circuit/architecture level, CMOS is now well-positioned to be the key technology that enables volume production in the mmWave frequency range.

2 MMICs Using CMOS Technology

Several factors are critical to designing and ramping a high-performance fully integrated millimeter-wave integrated circuit (MMIC) to production. From a radio frequency (RF)/mmWave perspective, the transistor speed as characterized by f_T/f_{MAX} – and the passives and metallization offered by the process – are vital to enabling benchmark performance numbers in key RF modules such as low-noise amplifiers (LNAs), power amplifiers (PAs) and voltage-controlled oscillators (VCOs).

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The benefits of integration are well-known from both a cost and features perspective. Therefore, in addition to RF capabilities, the process node should also be conducive to the design and integration of high-performance analog/mixed-signal modules such as data converters and digital IPs that enable differentiated signal-processing capabilities. capabilities. In markets such as automotive, where safety is paramount, it is imperative that designers understand the reliability aspects of the process. In this document, current state-of-the-art CMOS technology is reviewed against these metrics to demonstrate readiness to ramp high-performance MMICs.

2.1 Scaling With CMOS

CMOS scaling from the perspective of digital circuits has resulted in a steady decrease in transistor channel length (L_g). This reduction in channel length has resulted in an increase in raw transistor speeds, as measured by the f_T and f_{MAX}. The parameters f_T and f_{MAX} are inversely proportional to L_g and have been steadily increasing with technology scaling, as shown in Figure 1 [1]. f_T is a good metric for analog/mixed-signal circuits.

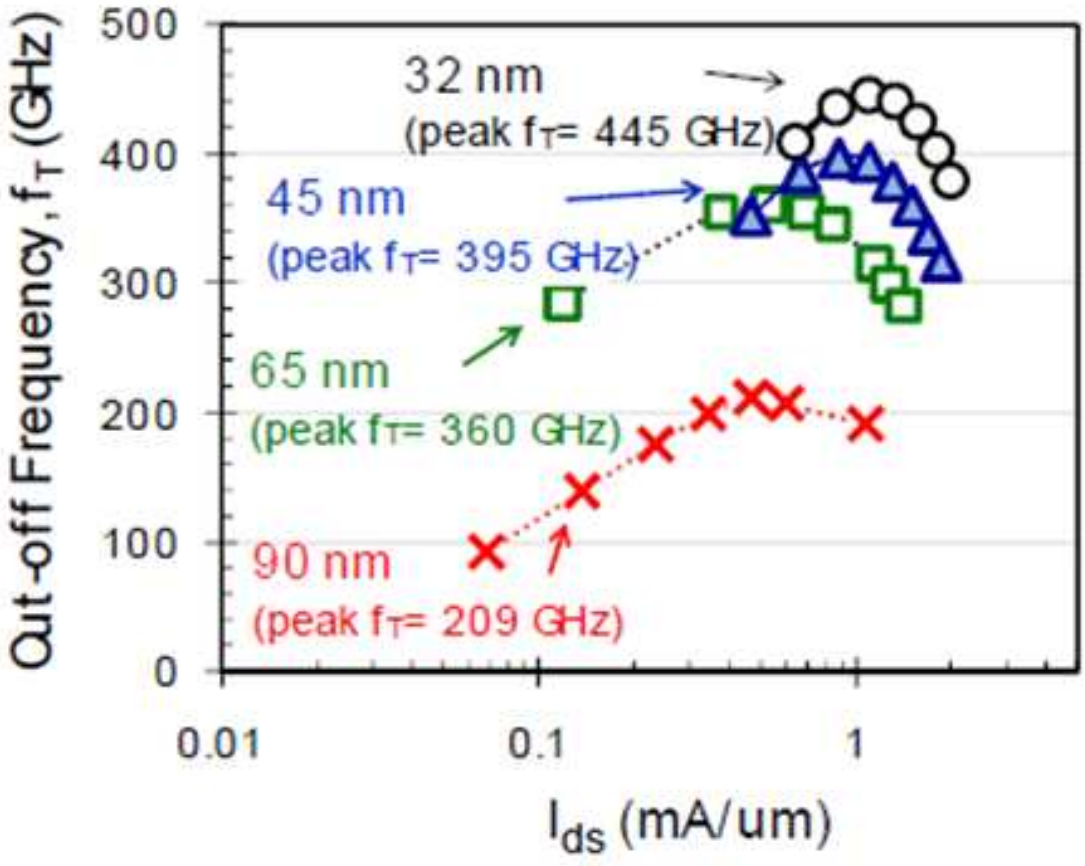

Figure 1. Scaling Trends of f_T in CMOS

However, the parameter f_{MAX} is a more relevant metric with which to understand transistor capabilities in mmWave frequencies. Although f_T is more a function of process technology, f_{MAX} is highly dependent on layout techniques that minimize gate and source/drain resistance and parasitic losses. Consequently, it's possible to achieve an f_{MAX} higher than f_T [2].

Another key consideration, especially in the design of LNAs, is the minimum achievable noise figure (NF_{min}). With NF_{min} inversely proportional to f_T, technology scaling results in a lowering of NF_{min} as well. Like f_{MAX}, NF_{min} also depends on good layout techniques. Using layout optimization techniques and best practices developed at Texas Instruments (TI), devices with f_{MAX} = ~300 GHz and NF_{min} <4dB at 77 GHz in TI's 45 nm CMOS technology node are able to be demonstrated. TI's mmWave sensor portfolio leverages these devices.

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2.2 Synthesizing Data Converters and Passive Elements in CMOS

Aside from device speeds, the next key consideration in the design of high-performance mmWave circuits is the quality of passives: inductors, transformers, transmission lines and capacitors. These are highly dependent on the metallization offered by the process. Technology scaling from a digital perspective drives thinner interconnects and metal stacks closer to the substrate – two trends that result in lossy passives. However, with minimal cost impact, most mixed-mode CMOS processes offer access to one to two layers of thicker higher-level metals. Using these metals, along with techniques to reduce substrate losses, inductors with quality factors in excess of 15 are achievable. have been demonstrated. Also achievable using vertical coupling, are low-loss transformers with coupling factors >0.7 in mmWave frequencies.

Using the available metal layers, high-density and high-Q capacitors are commonly implemented as metal-insulator-metal (MIM) capacitors. The inherent MOS capacitor serves as a tunable capacitor for VCOs if you address the issue of lower Q at mmWave frequencies using proper frequency planning with the choice of VCOs and multipliers.

CMOS technology scaling results in reduced supply voltage and self-gain (gm/gds) in transistors, trends that are a challenge for analog/mixed-signal circuits. But given the push for integration, innovations have resulted in architectures that take advantage of the benefits of CMOS. Examples range from the popular switched-capacitor technique of the past to more recent examples of digitally assisted analog [3] where taking advantage of easy access to digital signal processing (DSP) corrects unavoidable analog impairments in CMOS, thereby creating high-performance circuits.

3 RF performance

In the data-converter context, the research focus in the past decade has been on architectures attractive to CMOS implementation such as delta-sigma modulators and successive approximation register (SAR) analog-to-digital converters (ADCs). These converters now boast bandwidths in excess of 100 MHz with superior power efficiency and are consequently the data-converter architecture of choice for integrated transceivers [4].

3.1 Challenges

It is not possible to avoid mentioning flicker noise (1/f noise) in the context of CMOS technology. Flicker noise is a low-frequency noise mechanism that occurs because of imperfections in the silicon-silicon dioxide (Si-SiO2) interface. Flicker noise and its dependence on total device area have been well documented, and there are a number of techniques to mitigate/reduce flicker noise, such as chopping and correlated double sampling. Technology scaling results in an improvement in the control of the Si-SiO2 interface, thereby leading to a reduction in flicker noise (normalized to unit area) with process scaling [1] [5].

Operating under a reduced supply voltage and remaining within supply ratings are also necessary to mitigate long-term reliability issues brought about by degradation mechanisms such as negative-bias temperature instability (NBTI), positive-bias temperature instability (PBTI) and channel hot-carrier injection (CHCI). There are many studies behind the fundamental physics of these degradation mechanisms, and models and simulation techniques exist to predict their impact [6]. It might appear that circuits such as PAs, which benefit from an increased supply voltage, would be at a disadvantage in CMOS technology. However, using impedance transformation and on-chip power combining have resulted in CMOS PA designs that reliably deliver >12dBm of output power at mmWave frequencies [7].

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4 CMOS Enables Integration of More Digital Content

The numerous benefits of scaling in the digital context are self-evident and are the key drivers for technology scaling. These have enabled integrated transceivers with increased digital content, including microcontrollers and even dedicated DSPs. TI's single-chip solution for automotive radar in the 76 GHz – 81 GHz band, the AWR1642, is one such example.

Figure 2 shows a block-level representation of the AWR1642 chipset. The level of integration that CMOS enables is clearly evident. From an analog signal-chain perspective, the chip includes four receiver chains (LNA to ADC), two transmitter chains with an integrated PA, a synthesizer capable of delivering fast ramps for frequency-modulated continuous wave (FMCW) radar operation, integrated references and temperature sensors. The digital content on the chip includes the necessary digital processing for the ADCs, TI's custom DSP for radar processing, an Arm® Cortex®-R4F microcontroller and a host of interface protocols such as Camera Serial Interface (CSI) and low-voltage differential signaling (LVDS).

In addition to the rich feature set that such a high level of integration provides, having mmWave, analog and digital circuits on the same die allows for built-in self-test (BIST) and monitoring capabilities. For example, the AWR1642 has circuits that communicate seamlessly between mmWave/analog/digital boundaries, and can detect and warn in the event that a receiver chain experiences a saturation event or a transmitter encounters a ball-break at its output. These are key differentiating features in the safety-critical automotive market.

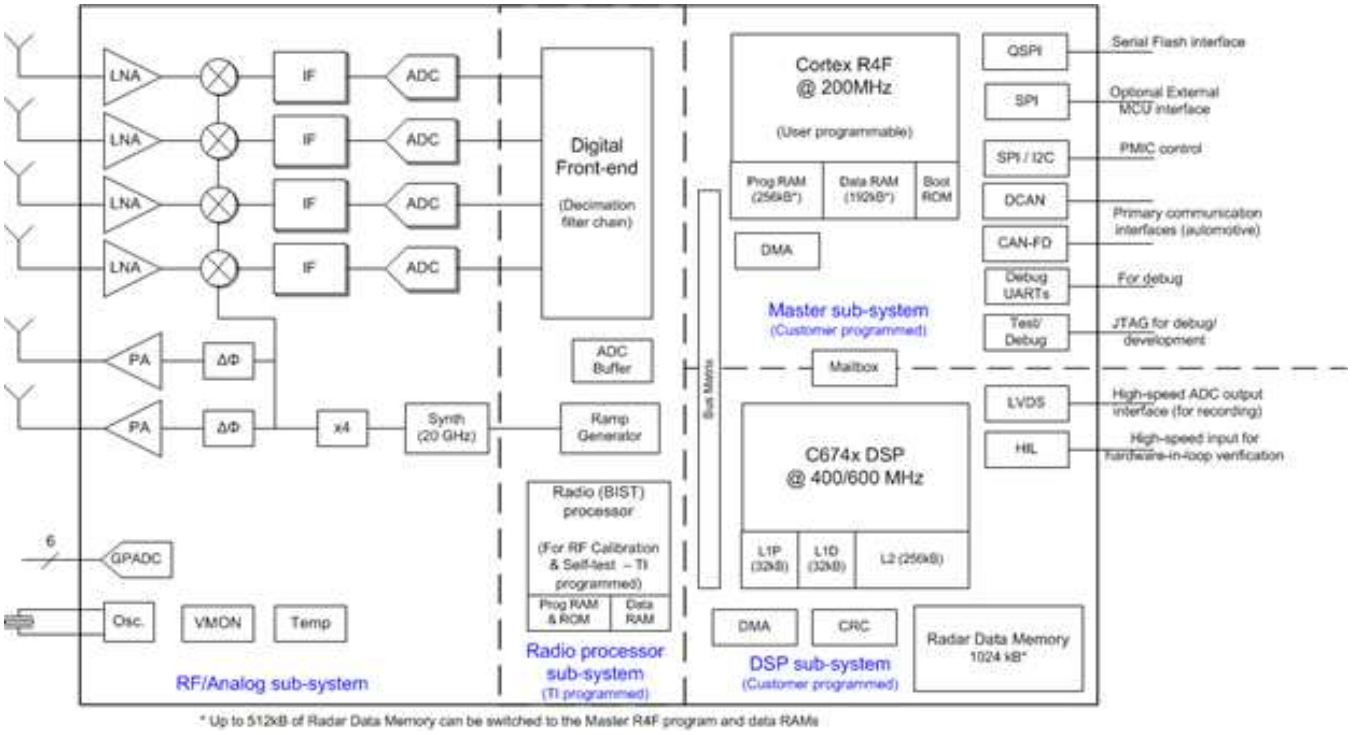

Figure 2. Block Diagram of TI's Single-Chip Transceiver for Automotive Radar

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5 Summary

In summary, digital scaling has resulted in high-speed transistors that make mmWave circuits feasible in CMOS technology. Sustained innovations have resulted in analog circuits and architectures uniquely suited for CMOS technology that deliver high performance by amplifying the advantages of scaling. The integration benefit of CMOS technology enables the co-existence of multiple classes of circuits, and itself offers a platform for further innovation.

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