Firmware Compiling Script Application Note

Calterah Semiconductor

Date	Version	Description	Author
2020.08.21	V0.1.0	First version	Xudong Ran
2020.09.29	V0.1.1	Add AES enable function	Xudong Ran
2020.10.13	V0.1.2	Fix typing errors	Xudong Ran

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CHAPTER

ONE

INTRODUCTION

Calterah provides multiple boot and executing features for various usage scenarios. These features are implemented using conditional compilation by macros. Three-stage boot (SYSTEM_BOOT_STAGE) is for OTA function. XIP (FLASH_XIP, LOAD_XIP_TEXT_EN) method is to extend total amount of memory by executing programs in Flash. Boot split (ELF_2_MULTI_BIN) feature is to reduce boot time by loading split boot into ICCM. Baseband boot acceleration (ACC_BB_BOOTUP) is to reduce time of initialization by writing value to the register instead of executing logic function. Other features, such as tool chain selection (TOOLCHAIN), radar cascade mode (BOARD), flash vendor selection (FLASH_TYPE), are also included. A python compiling script is used to simplify all these macro combinations. This document is to introduce the usage of the compiling script. This document applies to Alps and Rhine series only.

CHAPTER

TWO

USAGE

Requirements:

1. Python version >=3.6.5
2. Use the following command to install python modules pyserial, cryptography, and numpy.
   pip install pyserial, cryptography, numpy

Parameters:

python make_bin.py -s 3 -m xip -sp true -v giga -ba false -tc gnu -c false -aes false

-s: two-stage/3-stage boot sequence selection, 2/3, default value is 2
-m: executing method selection, ram/xip, default value is ram
-sp: whether to split boot file, true/false, default value is false
-v: flash vendor used on board, s25fls/giga/micron/winbond/microchip, default value is s25fls
-ba: whether to enable baseband boot acceleration feature, true/false, default value is false
-tc: tool chain selection, gnu/mw, default value is gnu
-c: cascade mode enable, true/false, default value is false
-aes: enable aes encryption, true/false, default value is false

Commonly Used Command:

Two-stage RAM
python make_bin.py –s 2 –m ram

Two-stage XIP
python make_bin.py –s 2 –m xip

Three-stage RAM
python make_bin.py –s 3 –m ram

Three-stage XIP
python make_bin.py –s 3 –m xip

Three-stage Boot-split XIP
python make_bin.py –s 3 –m xip –sp true

Note:

1. If non-Cypress flash used on radar board, please add parameter –v [vendor]. eg. –v giga
2. If baseband boot acceleration is enabled, please make sure that baseband_bb_bootup.h

is already in calterah/common/baseband/ folder, and the add parameter –ba true to compile firmware