

# Calterah Alps CAL77S244-AE Datasheet

*Release 1.0*

Calterah Semiconductor

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**CHAPTER  
ONE**

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## **INTRODUCTION**

Calterah Alps 4T4R radar sensor chip (CAL77S244-AE) is an integrated single-chip frequency-modulated continuous wave (FMCW) radar sensor capable of operation in 76- to 81-GHz band. The device is built with advanced low-power 40-nm CMOS process and packaged with low-loss eWLB technology. Its unprecedented level of integration not only significantly simplifies product implementation and development, but also enables extremely compact design. Calterah Alps 4T4R is an ideal solution for ultra-low-power, self-aware, accurate radar sensing applications in the automotive area.

Calterah Alps 4T4R is designed for FMCW radar system with 4 TX and 4 RX. It implements RF system with 4 TX channels, 4 RX channels, built-in Phase Locked Loop (PLL), and analog-to-digital converters (ADCs). It also integrates Calterah radar signal processing subsystem, which implements radar algorithms, including fast Fourier transform (FFT), constant false alarm rate (CFAR) detectors, direction of arrival (DoA) estimators, and other advanced features. The Alps device includes a high-performance and low-power ARC EM6-based processor with exclusive 576-KB memory, which is responsible for radio configuration, baseband control, and other heavyweight application-level algorithms. Simple programming interfaces accommodate a wide variety of radar sensor applications. Additionally, along with the device, a complete radar sensor platform solution is provided, including reference hardware design, semi-turnkey software platform, and user documentation.

Besides CAL77S244-AE, Alps family also includes:

- CAL77S224-AE, a 2T4R radar sensor chip.  
For details, refer to *Calterah Alps CAL77S224-AE Datasheet*.
- CAL77S244-AB, an antenna-in-package (AiP) radar sensor chip with 4 TX and 4 RX antenna array embedded in the package.  
For details, refer to *Calterah Alps CAL77S244-AB Datasheet*.
- CAL77S244-IB, another AiP radar sensor chip with 4 TX and 4 RX antenna array embedded in the package.

The difference between CAL77S244-IB and CAL77S244-AB is that CAL77S244-IB is an industrial product and does not support CAN or CAN FD functions, while CAL77S244-AB supports CAN and CAN FD functions.

For details, refer to *Calterah Alps CAL77S244-IB Datasheet*.

### **1.1 Features**

- Four-channel 77-GHz/79-GHz transmitter
  - Maximum output power: 12 dBm
  - Phase shifter
  - Supports binary phase shift keying (BPSK) modulation
  - TX power detectors

## 1.1. Features

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- Four-channel 77-GHz/79-GHz receiver
  - Linearity (OP1dB) > 11 dBm
  - Conversion gain 34 dB to 76 dB at 5.0 MHz
  - Integrated high-pass filters
  - Typical single-sideband (SSB) noise figure: 12 dB at 5.0 MHz
  - Baseband IF peak detectors
  - Baseband output driver
- 77-GHz/79-GHz frequency synthesizer
  - Bandwidth 0.8/3 MHz with integrated loop filter
  - Supports 50-MHz crystal/reference clock for 76 GHz to 81 GHz
  - Supports configurable FMCW signal generation
  - Supports output synchronization signal
- Four-channel analog-to-digital converters (ADCs)
  - Sampling rates: up to 50 MSPS
- Power management
  - Built-in low-dropout regulator (LDO) network
- Four-channel low-voltage differential signaling (LVDS) data interface
- Built-in self-test
- CPU
  - 32-KB I-Cache
  - 32-KB D-Cache
  - 32-KB instruction close coupled memory (ICCM)
  - 32-KB data close coupled memory (DCCM)
  - Timer × 2
  - Watchdog timer
  - Single precision floating point unit (FPU)
  - 16 MPU regions
- Memory
  - Baseband: 2 MB
    - \* 1 MB could be shared with CPU in static share mode
  - CPU: 576 KB
- Peripherals
  - Controller area network (CAN)/CAN FD × 2
  - Universal asynchronous receiver/transmitter (UART) × 2
  - Inter-integrated circuit (I<sup>2</sup>C) master
  - Quad serial peripheral interface (QSPI) master



- Serial peripheral interface (SPI) master × 2
- SPI slave/QSPI slave
- General purpose input/output (GPIO)
- One-time programmable (OTP) memory
- Timer × 4
- Pulse width modulator (PWM) × 2
- Baseband
  - Virtual array frame
    - \* Time-division modulation (TDM)
    - \* Binary-phase modulation (BPM)
  - Digital decimation: up to factor of 16
  - Anti-interference
  - Configurable FFT sizes: up to 2048
  - Configurable CFAR window size: up to 21×21
  - Configurable CFAR type:
    - \* Cell averaging (CA)
    - \* Ordered statistics (OS)
    - \* Smallest order and greatest order (SOGO)
    - \* Noise reference (NR)
  - Output objects: up to 1024 objects
  - Multi-object DoA: up to 4 objects per bin
  - Auto gain control (AGC)
  - Super resolution support
  - Frame interleaving
- Error management unit (EMU)
- Automotive AEC-Q100
- ISO 26262 ASIL B-capable

## 1.2 Applications

- Automotive radar systems
- Industrial radar systems



## 1.3 Chip Block Diagram

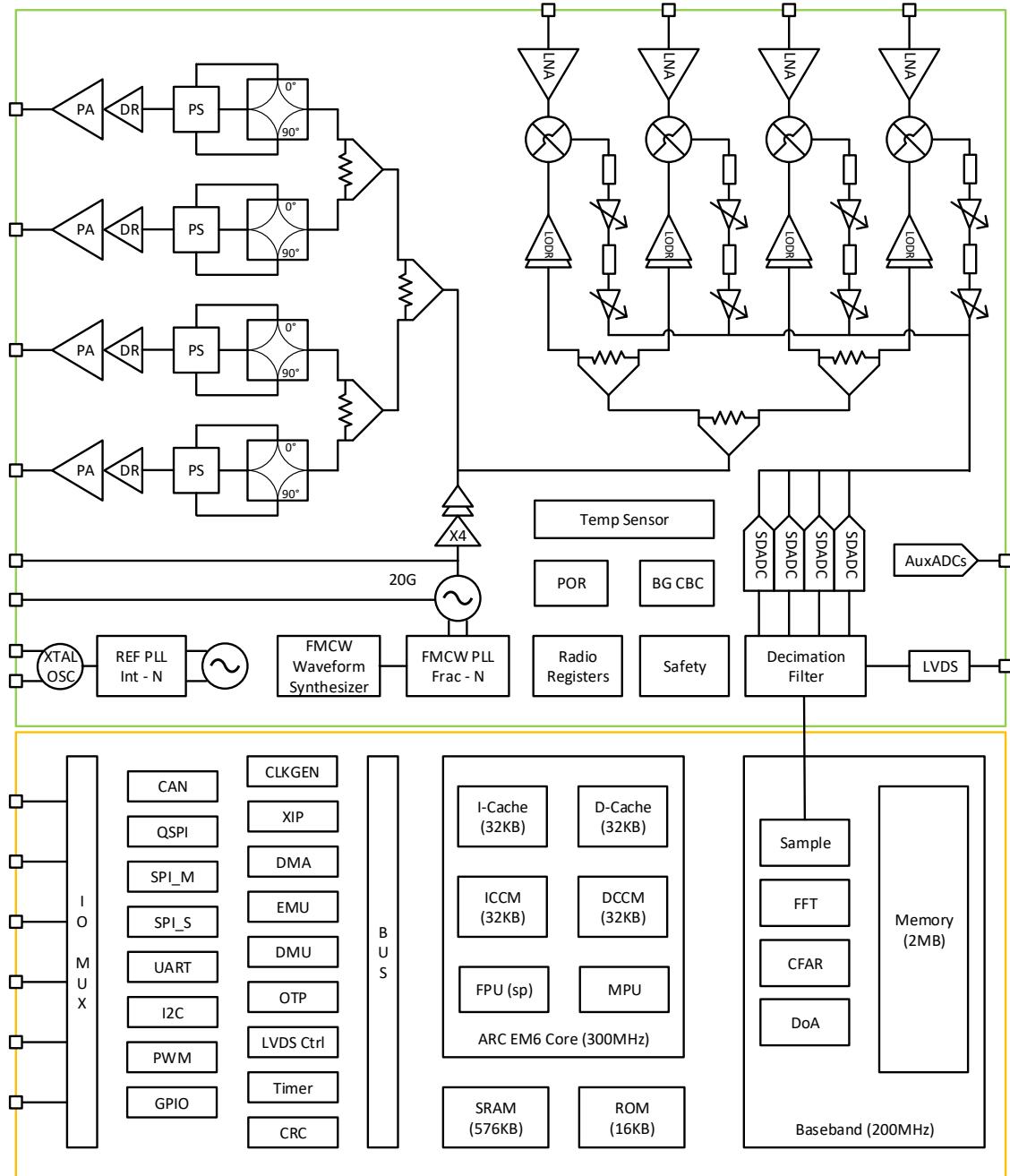


Fig. 1.1: Chip Block Diagram

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**CHAPTER  
TWO**

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**DEVICE INFORMATION**

## **2.1 Pinout**

Fig. 2.1 shows a top view of the layout and arrangement of the signal pads.

## 2.1. Pinout

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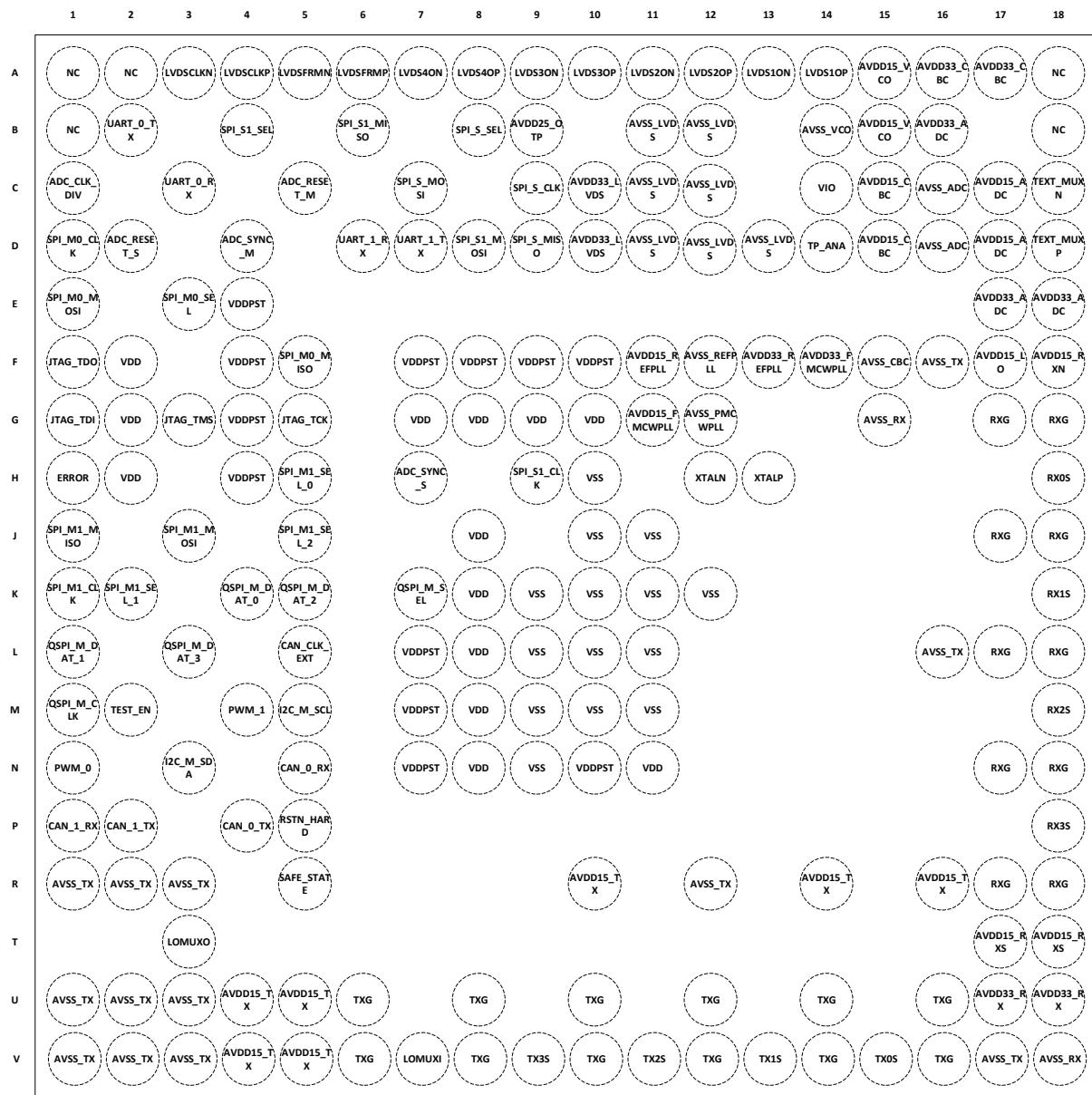


Fig. 2.1: Chip Pin Diagram (Top View)

You can view the functional description of each pin in [Table 2.1](#) and the pin multiplexing in [Table 2.2](#).

Table 2.1: Chip Signal Definitions

Pin Name	Ball Location	Description	Pin Type	Level(V)
LVDS1OP	A14	Differential IF output Channel 1 (10 KHz-20 MHz)/	AO	0-2.5
LVDS1ON	A13	Differential LVDS output Channel 1 (400 M)	AO	0-2.5
LVDS2OP	A12	Differential IF output Channel 2 (10 KHz-20 MHz)/	AO	0-2.5
LVDS2ON	A11	Differential LVDS output Channel 2 (400 M)	AO	0-2.5
LVDS3OP	A10	Differential IF output Channel 3 (10 KHz-20 MHz)/	AO	0-2.5
LVDS3ON	A9	Differential LVDS output Channel 3 (400 M)	AO	0-2.5
LVDS4OP	A8	Differential IF output Channel 4 (10 KHz-20 MHz)/	AO	0-2.5
LVDS4ON	A7	Differential LVDS output Channel 4 (400 M)	AO	0-2.5
LVDSFRMP	A6	Differential LVDS output frame (20 M)	AO	0-2.5
LVDSFRMN	A5		AO	0-2.5
LVDSCLKP	A4	Differential LVDS output clock (200 M)	AO	0-2.5
LVDSCLKN	A3		AO	0-2.5
TEST_MUXN	C18	Differential test signal input	AI	0-2.5
TEST_MUXP	D18		AI	0-2.5
XTALP	H13	Crystal oscillator input	AI	0-2.5
XTALN	H12	Crystal oscillator input	AI	0-2.5
TP_ANA	D14	DC test signal	AO	0-3.3
VIO	C14	PLL test signal output	AO	0-2.5
AVDD15_ADC	D17, C17	1.5-V power supply	P	1.5
AVDD15_VCO	A15, B15	1.5-V power supply	P	1.5
AVDD15_FMCWPLL	G11	1.5-V power supply	P	1.5
AVDD15_CBC	C15, D15	1.5-V power supply	P	1.5
AVDD15_RXN	F18	1.5-V power supply	P	1.5
AVDD15_LO	F17	1.5-V power supply	P	1.5
AVDD15_REFPLL	F11	1.5-V power supply	P	1.5
AVDD15_RXS	T17, T18	1.5-V power supply	P	1.5
AVDD15_TX	R16, R14, R10, U4, U5, V4, V5	1.5-V power supply	P	1.5
AVDD25 OTP	B9	2.5-V power supply	P	2.5
AVDD33_ADC	B16, E18, E17	3.3-V power supply	P	3.3
AVDD33_FMCWPLL	F14	3.3-V power supply	P	3.3
AVDD33_REFPLL	F13	3.3-V power supply	P	3.3
AVDD33_CBC	A16, A17	3.3-V power supply	P	3.3
AVDD33_LVDS	C10, D10	3.3-V power supply	P	3.3
AVDD33_RX	U18, U17	3.3-V power supply	P	3.3

Continued on next page

Table 2.1 – continued from previous page

Pin Name	Ball Location	Description	Pin Type	Level(V)
VDDPST	E4, F4, F7, F8, F9, F10, G4, H4, L7, M7, N10, N7	3.3-V power supply	P	3.3
DVDD	F2, G10, G9, G8, G7, G2, H2, J8, K8, L8, M8, N11, N8	1.15-V power supply	P	1.15
AVSS_CBC	F15	DC ground	P	0
AVSS_LVDS	B11, B12, C11, C12, D11, D12, D13	DC ground	P	0
AVSS_VCO	B14	DC ground	P	0
AVSS_FMCWPLL	G12	DC ground	P	0
AVSS_REFPLL	F12	DC ground	P	0
AVSS_ADC	C16, D16	DC ground	P	0
DVSS	H10, J10, J11, K9, K10, L9, L11, K11, K12, M9, M10, M11, N9, L10	DC ground	P	0
AVSS_RX	G15, V18	DC ground	P	0
AVSS_TX	F16, L16, R12, R1, R2, R3, U1, U2, U3, V1, V2, V3, V17	DC ground	P	0
TXG	V6, U6, U8, V8, U10, V10, U12, V12, U14, V14, U16, V16	RF ground	RFO	0
RXG	G18, G17, J18, J17, L18, L17, N18, N17, R18, R17	RF ground	RFI	0
LOMUXO	T3	20-GHz LO output	RFO	/
LOMUXI	V7	20-GHz LO input	RFI	/
RX0	H18	77-GHz RX input Channel 0	RFI	/
RX1	K18	77-GHz RX input Channel 1	RFI	/
RX2	M18	77-GHz RX input Channel 2	RFI	/
RX3	P18	77-GHz RX input Channel 3	RFI	/
TX3	V9	77-GHz TX output Channel 3	RFO	/
TX2	V11	77-GHz TX output Channel 2	RFO	/
TX1	V13	77-GHz TX output Channel 1	RFO	/
TX0	V15	77-GHz TX output Channel 0	RFO	/
SPI_S_CLK	C9	SPIS serial clock	DIO	0-3.3
SPI_S_MISO	D9	SPIS master input slave output	DIO	0-3.3
SPI_S_SEL	B8	SPIS slave selection signal	DIO	0-3.3
SPI_S_MOSI	C7	SPIS master output slave input	DIO	0-3.3

Continued on next page



Table 2.1 – continued from previous page

Pin Name	Ball Location	Description	Pin Type	Level(V)
SPI_S1_MISO	B6	SPIS master input slave output	DIO	0-3.3
SPI_S1_MOSI	D8	SPIS master output slave input	DIO	0-3.3
SPI_S1_SEL	B4	SPIS slave selection signal	DIO	0-3.3
SPI_S1_CLK	H9	SPIS serial clock	DIO	0-3.3
UART_0_TX	B2	UART0 TX signal	DIO	0-3.3
UART_0_RX	C3	UART0 RX signal	DIO	0-3.3
UART_1_TX	D7	UART1 TX signal	DIO	0-3.3
UART_1_RX	D6	UART1 RX signal	DIO	0-3.3
ADC_RESET_M	C5	ADC reset master output	DIO	0-3.3
ADC_RESET_S	D2	ADC reset slave input	DIO	0-3.3
ADC_SYNC_M	D4	ADC sync master output	DIO	0-3.3
ADC_SYNC_S	H7	ADC sync slave input	DIO	0-3.3
ADC_CLK_DIV	C1	ADC clock	DIO	0-3.3
SPI_M0_CLK	D1	SPI M0 serial clock	DIO	0-3.3
SPI_M0_SEL	E3	SPI M0 slave selection signal	DIO	0-3.3
SPI_M0_MOSI	E1	SPI M0 master out slave in	DIO	0-3.3
SPI_M0_MISO	F5	SPI M0 master in slave out	DIO	0-3.3
JATG_TDO	F1	JTAG test data out	DO	0-3.3
JATG_TDI	G1	JTAG test data in	DIO	0-3.3
JATG_TMS	G3	JTAG test mode select	DIO	0-3.3
JATG_TCK	G5	JTAG test clock	DIO	0-3.3
ERROR	H1	Error signal output	DO	0-3.3
SPI_M1_MISO	J1	SPI M1 master in slave out	DIO	0-3.3
SPI_M1_MOSI	J3	SPI M1 master out slave in	DIO	0-3.3
SPI_M1_SEL_0	H5	SPI M1 slave selection signal	DIO	0-3.3
SPI_M1_SEL_1	K2	SPI M1 slave selection signal	DIO	0-3.3
SPI_M1_SEL_2	J5	SPI M1 slave selection signal	DIO	0-3.3
SPI_M1_CLK	K1	SPI M1 serial clock	DIO	0-3.3
QSPI_M_DAT_0	K4	QSPI input/output data	DIO	0-3.3
QSPI_M_DAT_1	L1	QSPI input/output data	DIO	0-3.3
QSPI_M_DAT_2	K5	QSPI input/output data	DIO	0-3.3
QSPI_M_DAT_3	L3	QSPI input/output data	DIO	0-3.3
QSPI_M_SEL	K7	QSPI slave selection signal	DO	0-3.3
QSPI_M_CLK	M1	QSPI serial clock	DO	0-3.3
TEST_EN	M2	Test mode enable	DI	0-3.3

Continued on next page



Table 2.1 – continued from previous page

Pin Name	Ball Location	Description	Pin Type	Level(V)
CAN_CLK_EXT	L5	CAN external clock	DIO	0-3.3
PWM_1	M4	PWM1 output	DIO	0-3.3
PWM_0	N1	PWM0 output	DIO	0-3.3
I2C_M_SDA	N3	I2CM data	DIO	0-3.3
I2C_M_SCL	M5	I2CM clock	DIO	0-3.3
CAN_1_RX	P1	CAN1 RX signal	DIO	0-3.3
CAN_1_TX	P2	CAN1 TX signal	DIO	0-3.3
CAN_0_RX	N5	CAN0 RX signal	DIO	0-3.3
CAN_0_TX	P4	CAN0 TX signal	DIO	0-3.3
SAFE_STATE	R5	Safe mode status	DO	0-3.3
RSTN_HARD	P5	Hard reset on board	DI	0-3.3
NC	A1, A18, B18, B1, A2	No connection	/	/







Table 2.2: Pin Multiplexing

Pin Name	Pin Type	Pin Control Address	Pin Control Value (0)	Pin Control Value (1)	Pin Control Value (2)	Pin Control Value (3)	Pin Control Value (4)	Reset State	Pull Up/Dn Type
TEST_EN	I	/	test_en_i	/	/	/	/	I	Pull Up
QSPI_M_CLK	O	/	qspi_m_clk_o	/	/	/	/	O(0)	/
QSPI_M_SEL	O	/	qspi_m_sel_o	/	/	/	/	O(0)	/
QSPI_M_DAT_3	IO	/	qspi_m_dat_3_io	/	/	/	/	I	Pull Up
QSPI_M_DAT_2	IO	/	qspi_m_dat_2_io	/	/	/	/	I	Pull Up
QSPI_M_DAT_1	IO	/	qspi_m_dat_1_io	/	/	/	/	I	Pull Up
QSPI_M_DAT_0	IO	/	qspi_m_dat_0_io	/	/	/	/	I	Pull Up
SPI_M1_CLK	IO	0xBA0204	spi_m1_clk_o	pwm_2_io	qspi_m1_clk_o		gpio_clk_o	I	Pull Up
SPI_M1_SEL_2	IO	0xBA0204	spi_m1_sel_2_o	pwm_3_io	qspi_m1_dat_3_io		gpio_val_io	I	Pull Up
SPI_M1_SEL_1	IO	0xBA0204	spi_m1_sel_1_o	pwm_4_io	qspi_m1_dat_2_io		gpio_dat_16_io	I	Pull Up
SPI_M1_SEL_0	IO	0xBA0204	spi_m1_sel_0_o	pwm_5_io	qspi_m1_sel_o		gpio_dat_15_io	I	Pull Up
SPI_M1_MOSI	IO	0xBA0204	spi_m1_mosi_o	pwm_6_io	qspi_m1_dat_0_io		gpio_dat_14_io	I	Pull Up
SPI_M1_MISO	IO	0xBA0204	spi_m1_miso_i	pwm_7_io	qspi_m1_dat_1_io		gpio_dat_13_io	I	Pull Up
SPI_S1_CLK	IO	0xBA023C	spi_s1_clk_i	/	fmcw_start_i	pwm_4_io	gpio_dat_12_io	I	Pull Up
SPI_S1_SEL	IO	0xBA0240	spi_s1_sel_i	/	/	pwm_5_io	gpio_dat_11_io	I	Pull Up
SPI_S1_MOSI	IO	0xBA0244	spi_s1_mosi_i	/	qspi_s_dat_3_io	pwm_6_io	gpio_dat_10_io	I	Pull Up
SPI_S1_MISO	IO	0xBA0248	spi_s1_miso_io	/	qspi_s_dat_2_io	pwm_7_io	gpio_dat_09_io	O(0)	/
UART_0_TX	O	0xBA0208	uart_0_tx_o	uart_1_tx_o	can_0_tx_o	can_1_tx_o	/	O(0)	/
UART_0_RX	I	0xBA0208	uart_0_rx_i	uart_1_rx_i	can_0_rx_i	can_1_rx_i	/	I	Pull Up
UART_1_TX	IO	0xBA020C	uart_1_tx_o	can_0_tx_o	can_1_tx_o	uart_0_tx_o	gpio_dat_08_io	I	Pull Up
UART_1_RX	IO	0xBA020C	uart_1_rx_i	can_0_rx_i	can_1_rx_i	uart_0_rx_i	gpio_dat_07_io	I	Pull Up
CAN_0_TX	IO	0xBA0210	can_0_tx_o	can_1_tx_o	uart_0_tx_o	pwm_2_io	gpio_dat_31_io	I	Pull Up
CAN_0_RX	IO	0xBA0210	can_0_rx_i	can_1_rx_i	uart_0_rx_i	pwm_3_io	gpio_dat_30_io	I	Pull Up
CAN_1_TX	IO	0xBA0214	can_1_tx_o	uart_0_tx_o	pwm_2_io	can_0_tx_o	gpio_dat_06_io	I	Pull Up
CAN_1_RX	IO	0xBA0214	can_1_rx_i	uart_0_rx_i	pwm_3_io	can_0_rx_i	gpio_dat_05_io	I	Pull Up
ADC_RESET_M	IO	0xBA0218	adc_reset_m_o	adc_sync_m_o	i2c_m_scl_io	pwm_0_io	gpio_dat_29_io	I	Pull Up
ADC_RESET_S	IO	0xBA0218	adc_reset_s_i	adc_sync_s_i	i2c_m_sda_io	pwm_1_io	gpio_dat_28_io	I	Pull Up
ADC_SYNC_M	IO	0xBA021C	adc_sync_m_o	i2c_m_scl_io	pwm_0_io	adc_reset_m_o	gpio_dat_27_io	I	Pull Up
ADC_SYNC_S	IO	0xBA021C	adc_sync_s_i	i2c_m_sda_io	pwm_1_io	adc_reset_s_i	gpio_dat_26_io	I	Pull Up
I2C_M_SCL	IO	0xBA0220	i2c_m_scl_io	pwm_0_io	adc_reset_m_o	adc_sync_m_o	gpio_dat_04_io	I	Pull Up
I2C_M_SDA	IO	0xBA0220	i2c_m_sda_io	pwm_1_io	adc_reset_s_i	adc_sync_s_i	gpio_dat_03_io	I	Pull Up
PWM_0	IO	0xBA0224	pwm_0_io	adc_reset_m_o	adc_sync_m_o	i2c_m_scl_io	gpio_dat_02_io	I	Pull Up
PWM_1	IO	0xBA0228	pwm_1_io	adc_reset_s_i	adc_sync_s_i	i2c_m_sda_io	gpio_dat_01_io	I	Pull Up

Continued on next page

Table 2.2 – continued from previous page

Pin Name	Pin Type	Pin Control Address	Pin Control Value (0)	Pin Control Value (1)	Pin Control Value (2)	Pin Control Value (3)	Pin Control Value (4)	Reset State	Pull Up/Dn Type
ADC_CLK_DIV	IO	0xBA022C	adc_clk_div_o	/	/	/	gpio_dat_25_io	I	Pull Up
CAN_CLK_EXT	IO	0xBA0230	can_clk_ext_i	/	/	/	gpio_dat_00_io	I	Pull Up
SPI_M0_CLK	IO	0xBA0234	spi_m0_clk_o	spi_s0_sel_i	/	/	gpio_dat_24_io	I	Pull Up
SPI_M0_SEL	IO	0xBA0234	spi_m0_sel_o	spi_s0_mosi_i	/	/	gpio_dat_23_io	I	Pull Up
SPI_M0_MOSI	IO	0xBA0234	spi_m0_mosi_o	spi_s0_miso_io	/	/	gpio_dat_22_io	I	Pull Up
SPI_M0_MISO	IO	0xBA0234	spi_m0_miso_i	spi_m0_clk_o	qspi_s_clk_i	/	gpio_dat_21_io	I	Pull Up
SPI_S0_CLK	IO	0xBA0238	spi_s0_clk_i	spi_m0_sel_o	qspi_s_sel_i	/	gpio_dat_20_io	I	Pull Up
SPI_S0_SEL	IO	0xBA0238	spi_s0_sel_i	spi_m0_mosi_o	qspi_s_dat_0_io	/	gpio_dat_19_io	I	Pull Up
SPI_S0_MOSI	IO	0xBA0238	spi_s0_mosi_i	spi_m0_miso_i	qspi_s_dat_1_io	/	gpio_dat_18_io	I	Pull Up
SPI_S0_MISO	IO	0xBA0238	spi_s0_miso_io	/	/	/	gpio_dat_17_io	I	Pull Up
ERROR	O	/	error_o	/	/	/	/	O(1)	/
JTAG_TCK	IO	0xBA024C	jtag_tck_i	/	pwm_4_io	/	/	I	Pull Up
JTAG_TMS	IO	0xBA024C	jtag_tms_i	/	pwm_5_io	/	/	I	Pull Up
JTAG_TDI	IO	0xBA024C	jtag_tdi_i	/	pwm_6_io	/	/	I	Pull Up
JTAG_TDO	O	0xBA024C	jtag_tdo_o	/	pwm_7_io	/	/	O(0)	/
RSTN_HARD	I	/	rstn_hard_i	/	/	/	/	I	Pull Up
SAFE_STATE	O	/	safe_state_o	/	/	/	/	O(1)	/

## **2.1. Pinout**

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**CHAPTER  
THREE**

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**SPECIFICATIONS**

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**Note:** All the specifications are at  $T_A = 25^\circ\text{C}$ ,  $VDD33 = 3.3 \text{ V}$ ,  $VDD 15 = 1.5 \text{ V}$ , and  $VDD = 1.15 \text{ V}$ , unless otherwise noted.

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### 3.1 Absolute Maximum Ratings

Table 3.1 shows all absolute maximum ratings. Without specification, voltages are referred to ground. Exceeding the ratings may cause malfunction or permanent damage.

Table 3.1: Maximum Ratings

Symbol	Description	Min	Max	Unit
$V_{\text{static\_max}}$	Supply voltage (static)	-0.3	3.63	V
$V_{\text{dyn\_max}}$	Supply voltage (dynamic) Nominal VCC +20%, for short time. If applied for extended time, lifetime is degraded.	-0.3	4	V
$V_{\text{digio\_max}}$	Digital supply voltage for IO (static, dynamic)	-0.3	3.63	V
$V_{\text{in\_max}}$	Voltage applied to all I/O pins	-0.3	3.63	V
$V_{\text{dig\_max}}$	Digital supply voltage (static, dynamic)	-0.3	1.21	V
$T_J$	Operating junction temperature range	-40	125	$^\circ\text{C}$
$T_{\text{STG\_before}}$	Storage temperature range before reflow soldering <sup>1</sup>	-55	150	$^\circ\text{C}$
$T_{\text{STG\_after}}$	Storage temperature range after the first reflow cycle <sup>1</sup>	-40	125	$^\circ\text{C}$

### 3.2 ESD Ratings

Table 3.2: ESD Ratings

Symbol	Description	Min	Max	Unit
HBM	ESD for human body model (HBM) digital I/O, analog, RF	-2000	2000	V
CDM	ESD for charged device model (CDM), conforming to AEC-Q100-011	-250	250	V
R1	HBM circuit description I	/	$\pm 1500$	$\Omega$

<sup>1</sup> Exposure for long time to very low or very high temperatures may affect product reliability.

### 3.3. Power Supply Specifications

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## 3.3 Power Supply Specifications

[Table 3.3](#) describes the four supply rails of Calterah Alps 4T4R and [Table 3.4](#) summarizes the power consumption under each supply rail.

Table 3.3: Power Supply Rails

Relevant I/Os	Blocks Powered by Supply	Min	Typ	Max	Unit
VDD33_LVDS, VDD33_ADC, VDD33_FMCWPLL, VDD33_REFPLL, VDD33_CBC, VDD33_RX	Digital I/Os, Buffers, DACs, PFD, Charge Pump, VGA1, VGA2, CBC, LVDS, PoR	3.14	3.3	3.47	V
VDD25 OTP	OTP	2.38	2.5	2.63	V
VDD15_ADC, VDD15_FMCWPLL, VDD15_REFPLL, VDD15_VCO, VDD15_LO, VDD15_CBC, VDD15_RXN, VDD15_RXS, AVDD15_TX	Amplifiers, Comparators, VCO, MMD, Mixers, LO, TIA, TX, PA, PMU	1.43	1.5	1.58	V
VDD	CPU, SRAMs, Digital Logic	1.10	1.15	1.21	V

Table 3.4: Current Consumption under Each Power Supply Rail

Parameter	Description	Min	Typ	Max	Unit
$I_{DD33}$	Total current under 3.3-V supply	/	140	180	mA
$I_{DD25}$	Total current under 2.5-V supply	/	40	/	mA
$I_{DD15}$	Total current under 1.5-V supply	/	1050	1300	mA
$I_{DD11}$	Total current under 1.15-V supply	/	260	600 <sup>2</sup>	mA

## 3.4 Power Consumption

Table 3.5: Average Power Consumption

Condition	Description	Min	Typ	Max	Unit
1TX, 4RX	Sampling: 20 MSPS, 50 ms/frame, 256 chirps/frame, 30 $\mu$ s/chirp, baseband/CPU active, RX/TX/LO/ADC/FMCW/PLL off during interframe	/	0.54	/	W
2TX, 4RX		/	0.58	/	
3TX, 4RX		/	0.64	/	
4TX, 4RX		/	0.7	/	
1TX, 4RX	Sampling: 20 MSPS, 50 ms/frame, 1024 chirps/frame, 30 $\mu$ s/chirp, baseband/CPU active, RX/TX/LO/ADC/FMCW/PLL off during interframe	/	1	/	
2TX, 4RX		/	1.2	/	
3TX, 4RX		/	1.4	/	
4TX, 4RX		/	1.6	/	

<sup>2</sup> Maximum instantaneous peak current is up to 850 mA.



### 3.5 Phase Locked Loop (PLL)

Table 3.6: PLL Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
$f_{PLL}$	PLL frequency range under 1G mode	76	/	77	GHz
	PLL frequency range under 4G mode	76	/	81	
Ramp_BW	PLL ramping bandwidth under 1G mode	1	/	/	GHz
	PLL ramping bandwidth under 4G mode	4	/	/	
Ramp_rate_up	PLL ramping up rate under 1G mode	/	/	50	MHz/ $\mu$ s
	PLL ramping up rate under 4G mode	/	/	250	
Ramp_rate_dn	PLL ramping down rate under 1G mode	/	/	70	MHz/ $\mu$ s
	PLL ramping down rate under 4G mode	/	/	400	
Ramp_time_idle	PLL idle time under 1G mode	3	/	/	$\mu$ s
	PLL idle time under 4G mode	1	/	/	
PN @ 1 MHZ	Phase noise at 1MHz offset under 1G mode	/	-93	/	dBc/Hz
	Phase noise at 1MHz offset under 4G mode	/	-90	/	

### 3.6 Local Oscillator (LO) MUX IN/OUT

Table 3.7: LO Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
LO_freq	LO frequency	19	/	20.25	GHz
LO_out	External LO output power in the master mode from 19G to 19.25G	/	-6	/	dBm
	External LO output power in the master mode from 19.25G to 20.25G	/	-7	/	dBm
LO_in_driven	External LO input power needed to fully drive the chip in the slave mode from 19G to 19.25G	/	-30	/	dBm
	External LO output power needed to fully drive the chip in the slave mode from 19.25G to 20.25G	/	-25	/	dBm



## 3.7 Transmitter (TX)

Table 3.8: Transmitter Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
<b>FREQUENCY AND NUMBER OF CHANNELS</b>					
N_ch_TX	Number of TX channels	/	4	/	/
f_TX	TX output frequency range	76	/	81	GHz
<b>Power</b>					
Pout	TX output power per channel	/	12	/	dBm
Pout_v	Output power variation due to Vdd	/	0.5	/	dB
Pout_slope	Output power frequency slope	-0.1	0	0.1	dB/100 MHz
Pout_ctrl	Output power control	/	8	/	dB
<b>PHASE SHIFTER</b>					
PS_ang	Phase shifter resolution	/	/	45	degrees
<b>LEAKAGE</b>					
Leak_LO_TX	RF leakage at TX port. All RF channels are disabled and LO is on	/	-36	/	dBm
<b>TX ON/OFF TIME</b>					
Time_TX	TX on/off switching time	/	2	2.5	$\mu$ s



## 3.8 Receiver (RX)

Table 3.9: Receiver Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
<b>FREQUENCY AND NUMBER OF CHANNELS</b>					
N_ch_RX	Number of RX channels	/	4	/	/
f_RX	RX input frequency range	76	/	81	GHz
<b>RXRF</b>					
CG_typical	RX conversion gain, LNA to VGA2, TIA = 500 ohm, LNA max gain, VGA1 + VGA2 = 30 dB at IF = 5 MHz	/	56	/	dB
CG_max	Maximum RX conversion gain at IF = 5 MHz, LNA/TIA/VGA1/ VGA2 maximum gain	/	73	/	dB
CG_min	Minimum RX conversion gain at IF = 5 MHz, TIA/VGA1/VGA2 minimum gain	/	32	/	dB
G_LNA	LNA gain control range	/	4	/	dB
G_LNA_step	LNA gain step	/	2	/	dB
G_TIA	TIA gain control range	/	12	/	dB
G_TIA_step	TIA gain step	/	6	/	dB
NF_RX	Single-sideband noise figure	/	12	/	dB
IP1dB	Input P1dB Power	/	-19	/	dBm
<b>LEAKAGE</b>					
Leak_LO_RX	RF leakage at RX port. All RF channels are disabled and LO is on	/	-32	/	dBm
<b>RXBB</b>					
G_VGA1	VGA1 gain	7	/	22	dB
G_VGA2	VGA2 gain	5	/	20	dB
G_step	VGA gain step	/	3	/	dB
OP1dB_RXBB	RX baseband output power 1-dB gain compression point Baseband gain=33 dB, IF=5 MHz	/	11	/	dBm
<b>FILTER</b>					
HP1_freq	The 1st high pass filter corner	12	/	200	kHz
HP1_order	The 1st high pass filter order	/	1	/	/
HP2_freq	The 2nd high pass filter corner	0.3	/	1	MHz
HP2_order	The 2nd high pass filter order	/	1	/	/
LP_freq	Low pass filter corner	/	15	/	MHz
<b>IF OUTPUT</b>					
IF_OUT	Output swing (DC couple, differential, Vp-p)	/	2.4	/	V
IF_LOAD_C	IF load capacitance (single-ended)	/	15	/	pF



## 3.9 Analog-to-Digital Converter (ADC)

Table 3.10: Sigma-Delta ADC Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
N_ch_ADC	Number of ADC channels	/	4	/	/
SNR @ 20 MS/s	Signal to noise ratio at sampling rate of 20 MSPS	/	65	/	dB
SNR @ 25 MS/s	Signal to noise ratio at sampling rate of 25 MSPS	/	62	/	dB
SNR @ 40 MS/s	Signal to noise ratio at sampling rate of 40 MSPS	/	62	/	dB
SNR @ 50 MS/s	Signal to noise ratio at sampling rate of 50 MSPS	/	59	/	dB
SFDR @ 20 MS/s	Spurious-free dynamic range at sampling rate of 20 MSPS	/	68	/	dB
SFDR @ 25 MS/s	Spurious-free dynamic range at sampling rate of 25 MSPS	/	68	/	dB
SFDR @ 40 MS/s	Spurious-free dynamic range at sampling rate of 40 MSPS	/	59	/	dB
SFDR @ 50 MS/s	Spurious-free dynamic range at sampling rate of 50 MSPS	/	59	/	dB

Table 3.11: Auxiliary ADC Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
N_AUXADC	Number of auxiliary ADCs	/	2	/	/
VR	Voltage range	0.5	/	2.5	V
ENOB @ 25 KS/s	Effective number of bits at the sampling rate of 20 KS/s	/	10	/	Bits
INL	Integral nonlinearity (best fit)	/	$\pm 2$	/	LSB
ERR_G	Gain error	/	$\pm 0.75\%$	/	/
ERR_O	Offset error	/	$\pm 4$	/	mV

## 3.10 CPU

Table 3.12: CPU Specifications

Parameter	Value	Unit
Clock Frequency	300	MHz
Address Size	24	Bits
Endianness	Little	/
I-Cache (Instruction Cache) Size	32	K-Byte
D-Cache (Data Cache) Size	32	K-Byte
ICCM (Instruction Closely Coupled Memory) Size	32	K-Byte
DCCM (Data Closely Coupled Memory) Size	32	K-Byte
Number of Timers	2	/
Number of Real-Time Counters	1	/
Watchdog Timer Width	32	Bits
FPU Type	Single precision	/
MPU Region	16	/



## 3.11 Baseband

Table 3.13: Baseband Specifications

Item	Value
Frame Type	Normal frame Virtual frame (TDM and BPM)
Digital Decimation	Up to factor of 16
Anti-Interference	Phase scrambling Frequency Hopping Chirp Shifting
FFT Size	Minimum FFT size is 64. Maximum range-domain FFT Size is 2048. Maximum Doppler-domain FFT size is 1024. Total 2D-FFT size needs to be less than 2 MB. Each complex data is represented in 32 bits.
CFAR Window Size	Up to $21 \times 21$ (Rectangular Window)
CFAR Type	CA (Cell Averaging) OS (Ordered Statistics) SOGO (Smallest Order and Greatest Order) NR (Noise Reference)
CFAR Objects	Up to 1024
Multi-Object DOA	Up to 4 objects per bin
Super Resolution Support	DML (Deterministic Maximum Likelihood)
Auto Gain Control	Programmable LUTs (Look Up Tables)
Frame Interleaving	Support up to 4 different types of frames

## 3.12 Thermal Resistance Characteristics for eWLB Package

Table 3.14: Thermal Resistance Characteristics

Thermal Metrics	°C/W
ΘJA Junction-to-Free_air	20.6
ΘJC Junction-to-Case	6.22
ΘJB Junction-to-Board	5.27
ΘJMA Junction-to-Moving_Air	NA
ΨJT Junction-to-Package_top	0.16
ΨJB Junction-to-Board	5.23



### **3.12. Thermal Resistance Characteristics for eWLB Package**

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## TIMING CHARACTERISTICS

### 4.1 Power on Timing

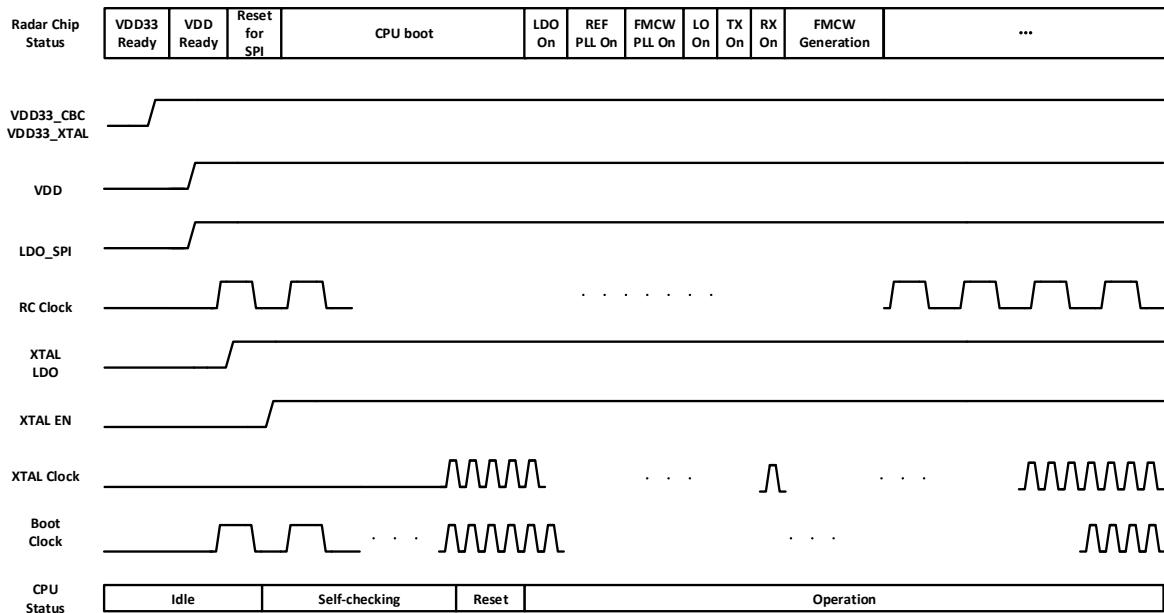


Fig. 4.1: Power on Timing

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**Note:** The VDD power supply should only be powered on after VDD33 reaches its minimum requirement of being 3.14 V.

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### 4.2 Low-Voltage Differential Signaling (LVDS)

Calterah Alps 4T4R integrates a 4-channel ADC and provides two flexible interface solutions:

- For I/Os: Serializer + LVDS interface protocol
- For internal processor: Paralleled interface protocol

## 4.2. Low-Voltage Differential Signaling (LVDS)

Fig. 4.2 shows the details of the interface solutions. The embedded LVDS of Calterah meets the ANSI/TIA/EIA-644-A standard.

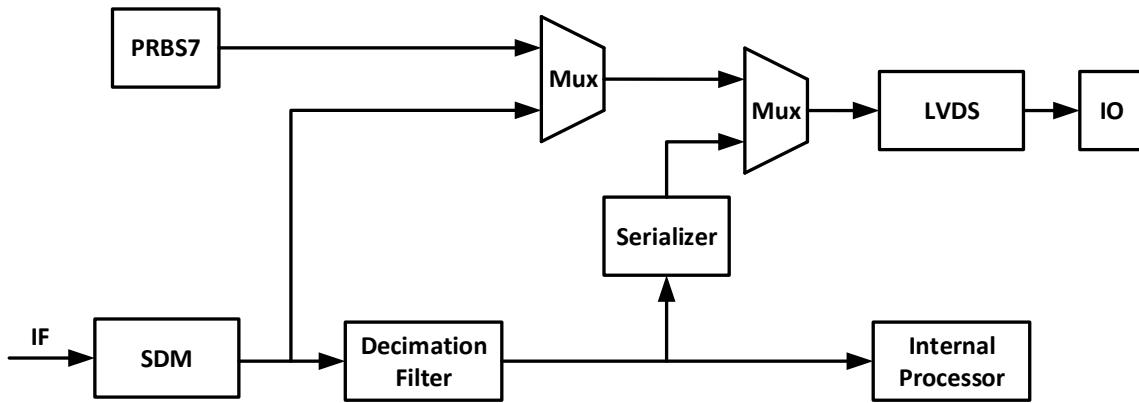


Fig. 4.2: Structure of 4-Channel ADC with Interface Solutions

The embedded ADC supports two working modes with different sampling rates and data widths.

- In one working mode, the LVDS provides two optional sampling rates: 20 MSPS and 25 MSPS. For the 20 MSPS clock, data width is 20 bits. For the 25 MSPS clock, data width is 16 bits.

Both 16-bit and 20-bit data adopt double date rate (sampling data at both falling and rising edges of the clock). Two's compliment is used as the data format.

- In the other working mode, the LVDS provides another two optional sampling rates: 40 MSPS and 50 MSPS. For the 40 MSPS clock, data width is 20 bits. For the 50 MSPS clock, data width is 16 bits. And the 20-bit data is reorganized to two channels of 10-bit data, and the 16-bit data is reorganized to two channels of 8-bit data.

Both 16-bit and 20-bit data adopt double date rate (sampling data at both falling and rising edges of the clock). Two's compliment is used as the data format.

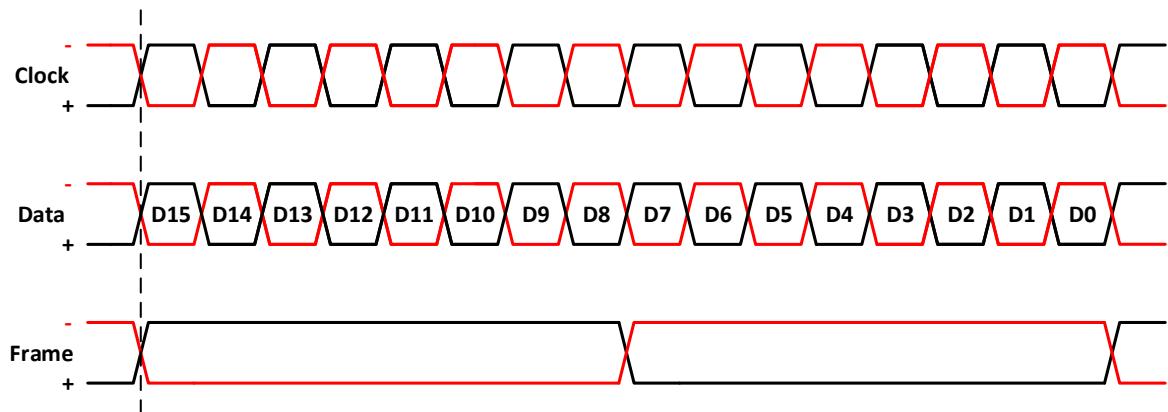


Fig. 4.3: 16-Bit Data with 25 MSPS Clock

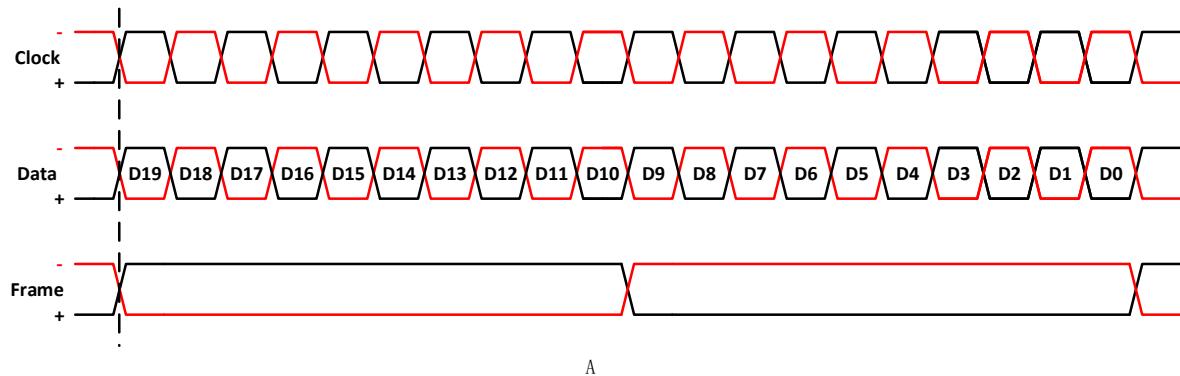


Fig. 4.4: 20-Bit Data with 20 MSPS Clock

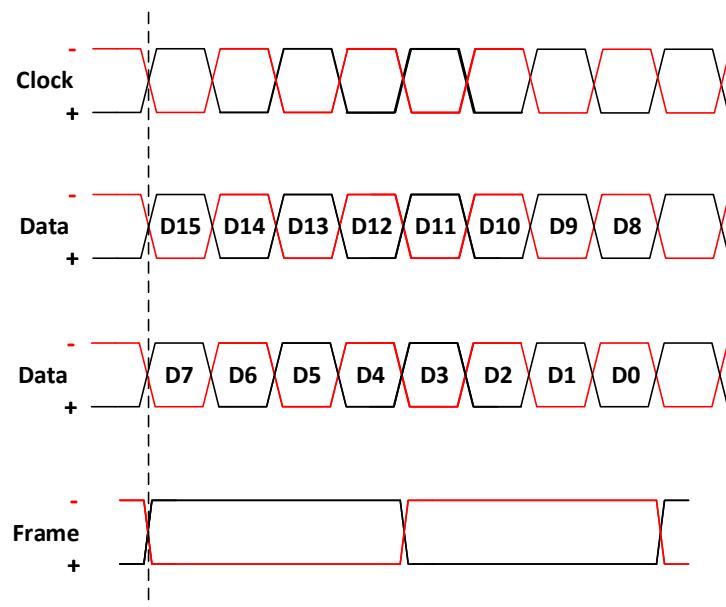


Fig. 4.5: 16-Bit Data with 50 MSPS Clock

### 4.3. General-Purpose Input/Output (GPIO)

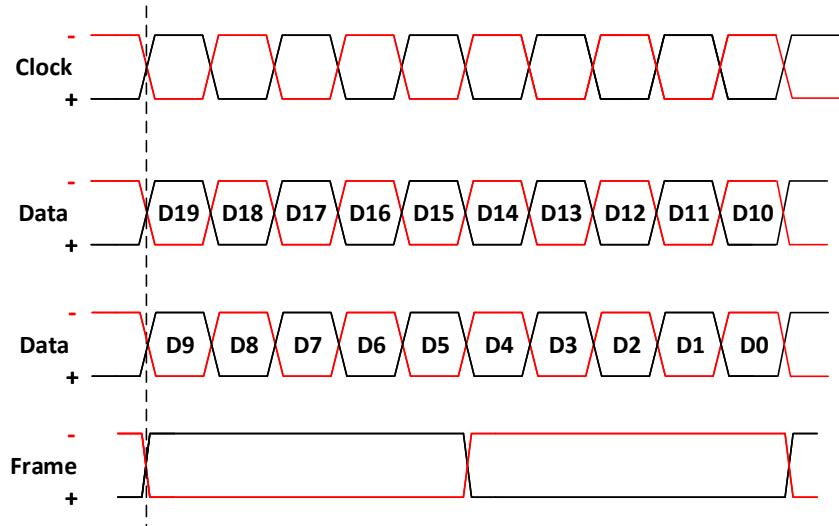


Fig. 4.6: 20-Bit Data with 40 MSPS Clock

Table 4.1: LVDS Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Data rate	DR	/	400	/	MHz	
Resistive Load (Differential)	$R_L$	/	100	/	Ohm	
Capacitive Load (Differential)	$C_L$	/	5	7.5	pF	
Common Mode Voltage	$V_{CM}$	1.125	1.25	1.375	V	
Output Voltage (Differential)	$V_{OUT}$	250	360	450	mV	
Rising Time (20% - 80%)	$T_r$	260	/	0.3 UI	ps	UI (Unit Interval)= 2.5 ns, 0.3 UI = 750 ps
Falling Time (20% - 80%)	$T_f$	260	/	0.3 UI	ps	UI (Unit Interval)= 2.5 ns, 0.3 UI = 750 ps
Output Voltage High	$V_{OH}$	/	/	1.6	V	
Output Voltage Low	$V_{OL}$	0.9	/	/	V	

### 4.3 General-Purpose Input/Output (GPIO)

Table 4.2 lists the switching characteristics of output timing relative to load capacitance<sup>1</sup>.

Table 4.2: Switching Characteristics of Output Timing versus Load Capacitance ( $C_L$ )

Parameter		Test Conditions	$VIOIN = 3.3$ V	Unit
$T_r$	Max rise time	$C_L = 25$ pf	1.7650	ns
		$C_L = 40$ pf	2.6300	ns
		$C_L = 70$ pf	4.3700	ns
$T_f$	Max fall time	$C_L = 25$ pf	1.6510	ns
		$C_L = 40$ pf	2.5360	ns
		$C_L = 70$ pf	4.3300	ns

<sup>1</sup> The rise/fall time is measured as the time taken by the signal to transition from 30% and 70% of  $VIOIN$  voltage.

## 4.4 Controller Area Network (CAN)

The CAN module performs communication according to ISO 11898. CAN FD with up to 64 data bytes is supported in CAN. Up to 64 dedicated Receive/Transmit Buffers and 64 configurable Receive/Transmit FIFOs are integrated in CAN.

Table 4.3: Dynamic Characteristics of CAN TX and RX Pins

Description	Min	Typ	Max	Unit
$t_{can\_tx}$ can_tx output delay	/	/	10	ns
$t_{can\_rx}$ can_rx input delay	/	/	10	ns

## 4.5 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter (UART) module is modeled after the industry-standard 16550. However, the register address space is relocated to 32-bit data boundaries for Advanced Peripheral Bus (APB) bus implementation.

### 4.5.1 Timing

Table 4.4: UART Timing Requirements

Description	Min	Typ	Max	Unit
Supported baud rate at 10 pF	/	921.6	/	Kb/s

## 4.6 Inter-Integrated Circuit Interface ( $I^2C$ )

$I^2C$  is a configurable, synthesizable, and programmable control bus that provides support for the communications between integrated circuits in a system. It is a simple two-wire bus with a software-defined protocol for system control, which is used in temperature sensors and voltage-level translators to EEPROMs, general-purpose I/O, A/D and D/A converters, CODECs, and many types of microprocessors.

### 4.6.1 Timing

Table 4.5:  $I^2C$  Timing Requirements

Description	Min	Typ	Max	Unit
Supported baud rate at 100 pF	/	100	3200	Kb/s

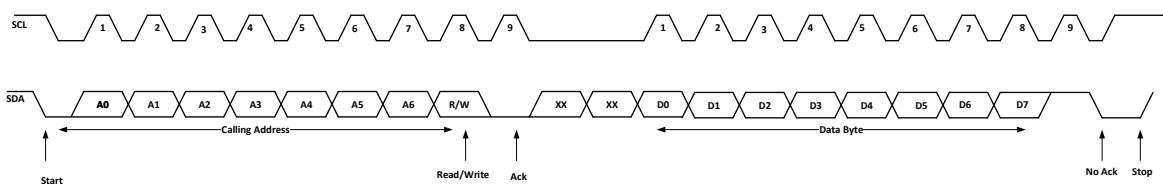


Fig. 4.7:  $I^2C$  Timing



## 4.7 Serial Peripheral Interface (SPI)

Serial Peripheral Interface (SPI) is a high-speed synchronous serial interface that allows a serial bit stream of programmed length (4 to 32 bits) to be shifted into or out of the device at an adaptive transfer rate.

### 4.7.1 Master SPI I/O Timings

Table 4.6: Master SPI I/O Timings

Notes	Symbol	Parameter	Min	Max	Unit
1	$t_{CLK}$	Clock cycle time	20	/	ns
2	$t_{CLK-High}$	Pulse duration clock high	8	/	ns
3	$t_{CLK-Low}$	Pulse duration clock low	8	/	ns
4	$t_{MOSI-SEL-Delay}$	Delay time, MOSI valid after falling edge of SEL	22	/	ns
5	$t_{MOSI-CLK-Delay}$	Delay time, MOSI valid after active edge of CLK	/	12	ns
6	$t_{MISO-Setup}$	Data setup time for MISO	13	/	ns
7	$t_{MISO-Hold}$	Data hold time for MISO	1	/	ns

**Note:** The reference clock is 400 MHz.

The numbers under the Notes heading refer to the corresponding numbers in Fig. 4.8.

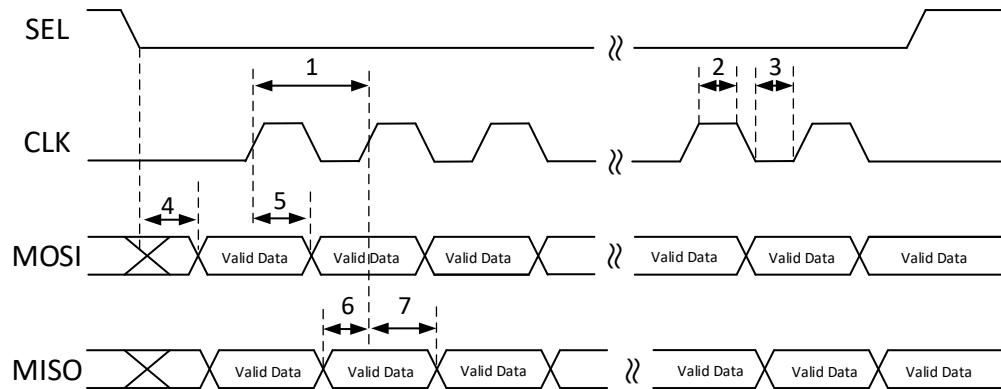


Fig. 4.8: Master SPI Timings

### 4.7.2 Slave SPI I/O Timings

Table 4.7: Slave SPI I/O Timings

Notes	Symbol	Parameter	Min	Max	Unit
1	$t_{CLK}$	Clock cycle time	20	/	ns
2	$t_{CLK-High}$	Pulse duration clock high	8	/	ns
3	$t_{CLK-Low}$	Pulse duration clock low	8	/	ns
4	$t_{MOSI-Setup}$	Data setup time for MOSI	4	/	ns
5	$t_{MOSI-Hold}$	Data hold time for MOSI	2	/	ns
6	$t_{MISO-SEL-Delay}$	Delay time, MISO valid after falling edge of SEL	15	/	ns
7	$t_{MISO-CLK-Delay}$	Delay time, MISO valid after active edge of CLK	/	19	ns

**Note:** The reference clock is 400 MHz.

The numbers under the Notes heading refer to the corresponding numbers in Fig. 4.9.

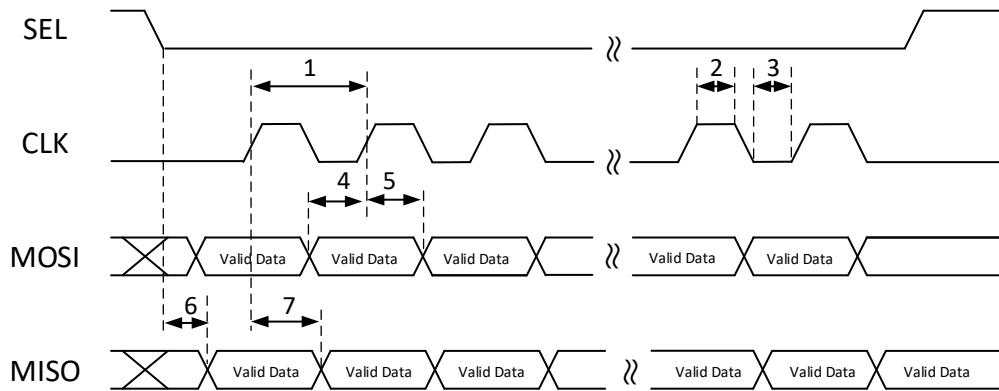


Fig. 4.9: Slave SPI Timings

### 4.8 Quad Serial Peripheral Interface (QSPI)

Quad Serial Peripheral Interface (QSPI) is an enhanced mode for SPI. Under this mode, the width of data line is changed to 4, so the data is shifted out and in on more than one line. Hence, the overall throughput is increased.

### 4.8.1 QSPI Master Mode I/O Timings

Table 4.8: QSPI I/O Timings

Notes	Symbol	Parameter	Min	Max	Unit
1	$t_{CLK}$	Clock cycle time	20	/	ns
2	$t_{CLK-High}$	Pulse duration clock high	8	/	ns
3	$t_{CLK-Low}$	Pulse duration clock low	8	/	ns
4	$t_{MOSI-SEL-Delay}$	Delay time, MOSI valid after falling edge of SEL	10	/	ns
5	$t_{MOSI-CLK-Delay}$	Delay time, MOSI valid after active edge of CLK	/	13	ns
6	$t_{MISO-Setup}$	Data setup time for MISO	10	/	ns
7	$t_{MISO-Hold}$	Data hold time for MISO	2	/	ns

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**Note:** The reference clock is 400 MHz.

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The numbers under the Notes heading refer to the corresponding numbers in Fig. 4.10.

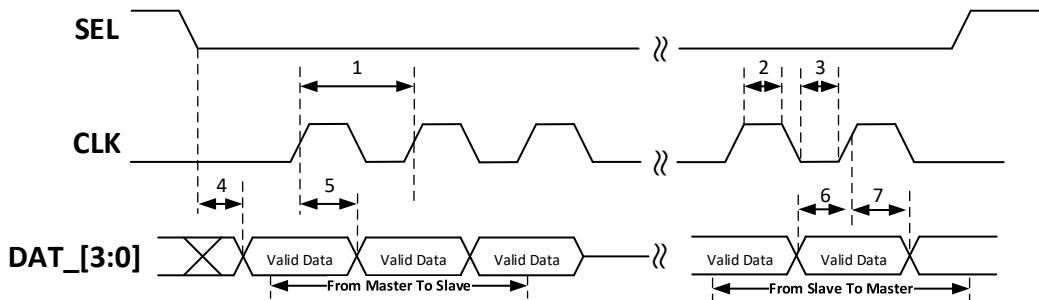


Fig. 4.10: Master QSPI Timings

## 4.9 Joint Test Action Group (JTAG) Interface

Table 4.9: JTAG Timings

Notes	Symbol	Parameter	Min	Typ	Max	Unit
1	$t_{cLK}$	Cycle time TCK	40	/	/	ns
2	$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	30	/	/	ns
	$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	30	/	/	ns
3	$t_h(TCK-TDI)$	Input hold time TDI valid from TCK high	0	/	/	ns
	$t_h(TCK-TMS)$	Input hold time TMS valid from TCK high	0	/	/	ns
4	$t_{su(TDO-TCK)}$	Input setup time TDO valid to TCK high	30	/	/	ns
5	$t_h(TCK-TDO)$	Input hold time TDO valid from TCK high	0	/	/	ns

The numbers under the Notes heading refer to the corresponding numbers in Fig. 4.11.

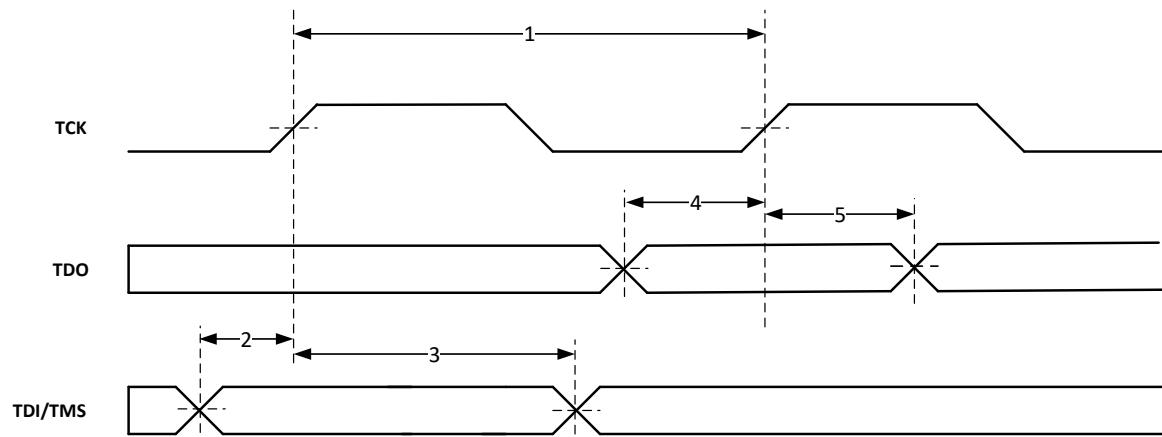


Fig. 4.11: JTAG Timing

#### **4.9. Joint Test Action Group (JTAG) Interface**

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## DETAILED DESCRIPTIONS

### 5.1 Radio Subsystem

The Radio subsystem integrates all the necessary RF, analog, and mixed-signal blocks for the radar frontend, including:

- 4 transmitter channels
- 4 receiver channels
- A frequency synthesizer with FMCW radar signal generator
- A reference PLL
- ADCs
- Baseband filters
- Variable-gain amplifiers
- Output drivers

It also includes temperature sensors, RF power detectors, on-chip low-dropout regulators (LDOs), and functional safety monitors to conform to the ISO 26262 standard. See [Fig. 5.1](#).

## 5.1. Radio Subsystem

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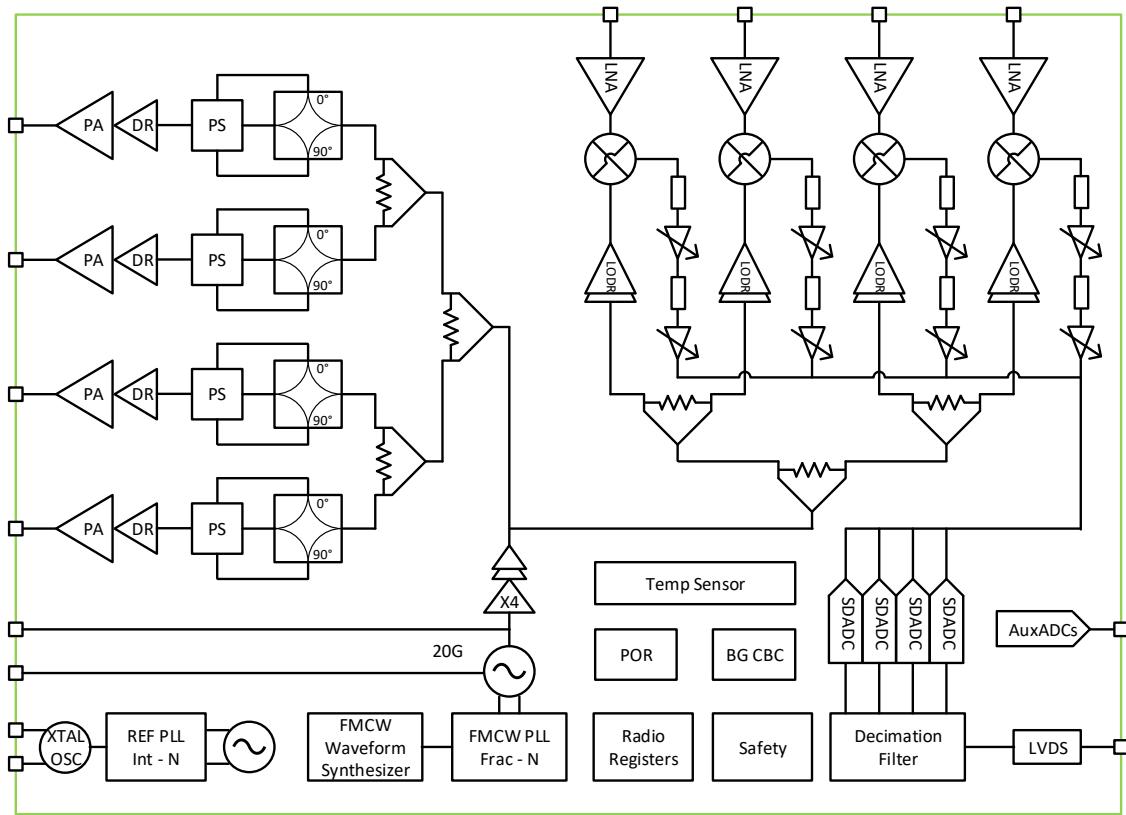


Fig. 5.1: Block Diagram of Radio Subsystem

### 5.1.1 Clock Generation

To boot up and provide a reference clock for Reference PLL, Calterah Alps requires an external crystal whose oscillating frequency is 50 MHz. The external crystal should be connected to the device I/Os. Fig. 5.2 shows the implementation of the external crystal.

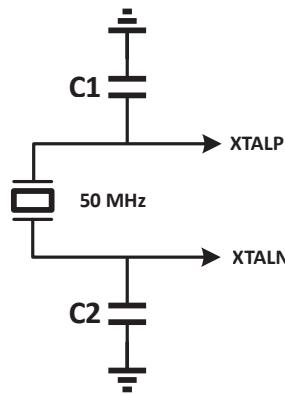


Fig. 5.2: Implementation of External Crystal

Table 5.1 lists the electrical characteristics of the clock crystal.

Table 5.1: Crystal Electrical Characteristics

Description	Symbol	Min	Typ	Max	Unit
Nominal frequency	FL	/	50	/	MHz
Load capacitance	CL	/	4	/	pF
Operating temperature	/	-40		125	°C
Effective resistance	Rr	/	/	55	Ω
Drive level	DL	/	/	200	μW

With the presence of the 50-MHz clock produced by the external crystal, Alps Clock Generation module generates 76- to 81- GHz clock signals for RF subsystem. The Clock Generation module contains a built-in oscillator circuit, a Reference PLL, a FMCW PLL, and a x4 frequency multiplier. The built-in oscillator circuit along with the external crystal produces a 50-MHz clock for the Reference PLL. The Reference PLL produces a 400-MHz/450-MHz clock for the FMCW PLL and 400-MHz/800-MHz ADC, a 300-MHz clock for CPU, a 5-MHz clock for auxiliary ADC (Aux ADC), which is used for safety monitoring, and a 12.5-MHz clock for the temperature sensor (TS). The FMCW PLL along with the x4 multiplier produces FMCW or fixed frequency clock signals for the Radio subsystem with high precision.

A built-in circuit is also included in the Clock Generation module to detect the presence of the crystal and the quality of the generated signals.

Fig. 5.3 shows the architecture of the clock generation module.



## 5.1. Radio Subsystem

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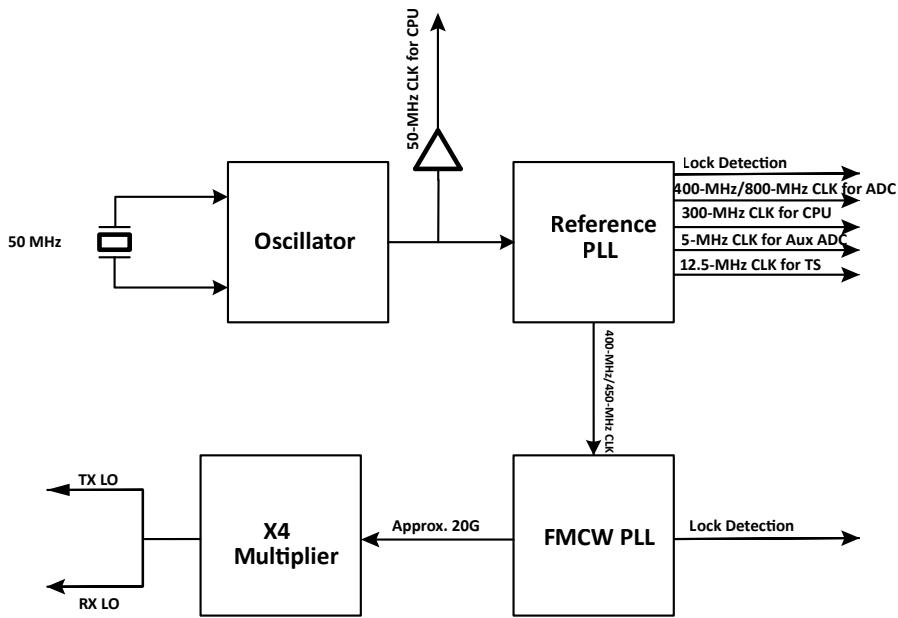


Fig. 5.3: Clock Subsystem

### 5.1.2 FMCW Waveform Synthesis

FMCW waveform generator in Calterah Alps radar chip is embedded with the following features for better radar ranging and anti-interference. All these features can be programmed and enabled independently.

- Virtual Array Mode (VAM)

VAM controls the on/off status and phase status of each TX channel, according to the user's configuration.

- Frequency Hopping Mode (FH)

FH enables the user to get different carrier frequencies and bandwidths for two adjacent chirps in the same frame.

- Phase Scramble Mode (PS)

PS provides the capability to rotate the phase by a degree of 180 in TX for each rotate.

- Chirp Shifting Mode (CS)

CS shifts both up ramp and down ramp by a specific time inside a chirp, while the total duration of one chirp keeps unchanged.

- Anti Velocity Ambiguity with Chirp Delay (Anti-VELAMB CD)

Anti-VELAMB CD extends some chirps' duration by a specific time, which is used for resolving velocity ambiguity.

- Auto Gain Control (AGC)

AGC adds 3 chirps at the beginning of each frame, and at the same time, hands over the gain control over RXBB in the radio part from radio registers to CPU.

- Frame Interleaving

FMCW waveform generator supports different frame types. Interleaving different types of frames enables achieving different applications simultaneously.

### 5.1.3 Local Oscillator (LO)

The Local Oscillator (LO) module consists of driving amplifiers and frequency multipliers. The device supports mux out and mux in functions for multi-chip cascading applications. See Fig. 5.4.

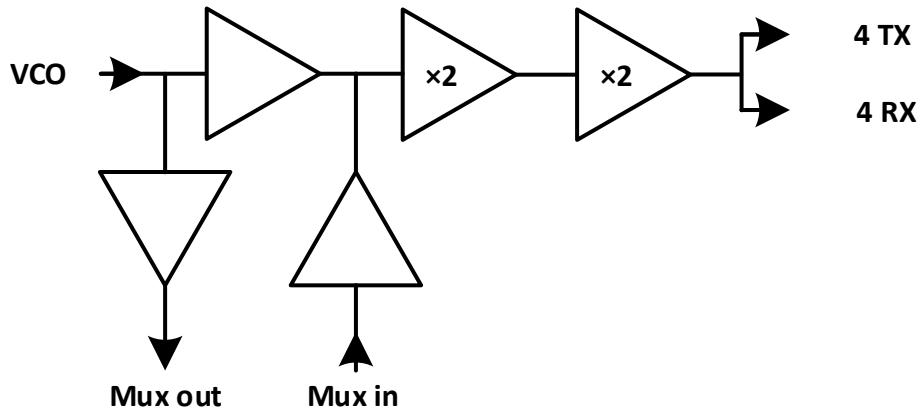


Fig. 5.4: LO Subsystem

### 5.1.4 Transmitter

The Transmitter module consists of 4 parallel transmitter chains, each with independent binary phase and amplitude control. All 4 transmitter channels can be operated at the same time. The device supports binary phase modulation for MIMO radar and interference mitigation. Each transmit chain can deliver 12 dBm at the antenna port on the PCB. See Fig. 5.5.

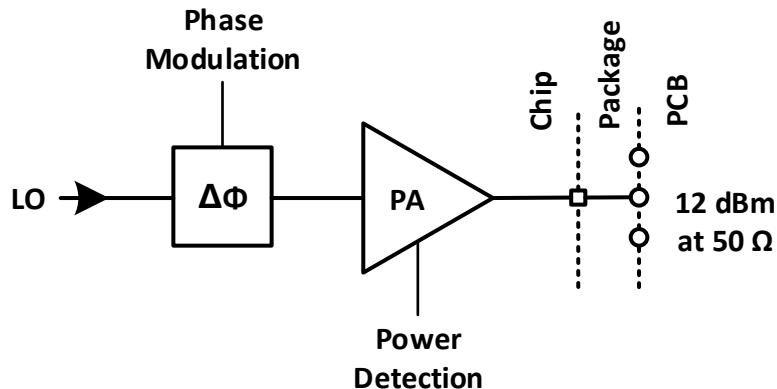


Fig. 5.5: Transmitter Subsystem (Per Channel)

### 5.1.5 Receiver

The Receiver module consists of 4 parallel channels. Each receiver channel consists of the following:

- A low-noise amplifier (LNA)
- A passive mixer
- A transimpedance amplifier (TIA)
- Two IF high-pass filters
- Two variable-gain amplifiers
- A sigma-delta modulator
- A decimation filter

All 4 receiver channels can be operated at the same time. An individual power-down option is also available. High-pass 1 has a 100-kHz normal cutoff frequency and can be configured to 12 kHz. High-pass 2 has a 500-kHz normal cutoff frequency. TIA, VGA1, and VGA2 are provided with an integrated saturation detector. Another saturation detector is inside the sigma-delta modulator.

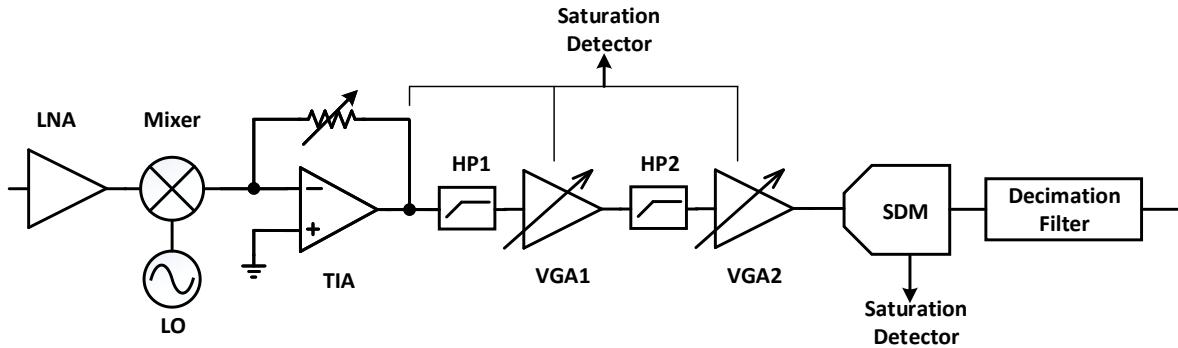


Fig. 5.6: RX Subsystem

### 5.1.6 Measurement Results



Fig. 5.7: Phase Noise at 76G in 1G Mode



## 5.1. Radio Subsystem



Fig. 5.8: Phase Noise at 76G in 4G Mode

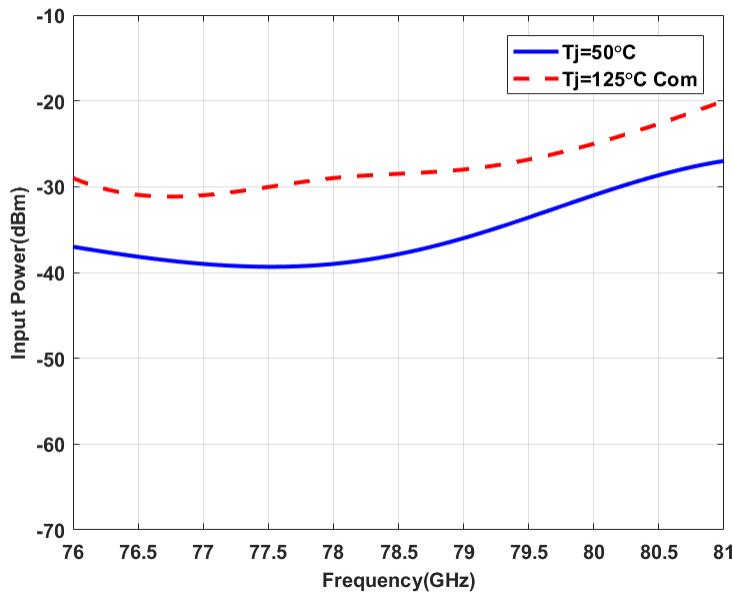


Fig. 5.9: LO Input Power with Compensation vs Frequency



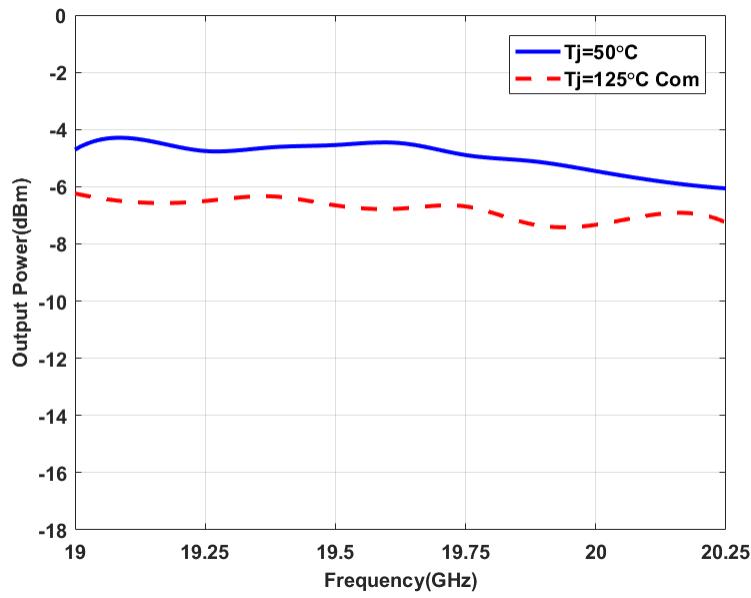


Fig. 5.10: LO Output Power with Compensation vs Frequency

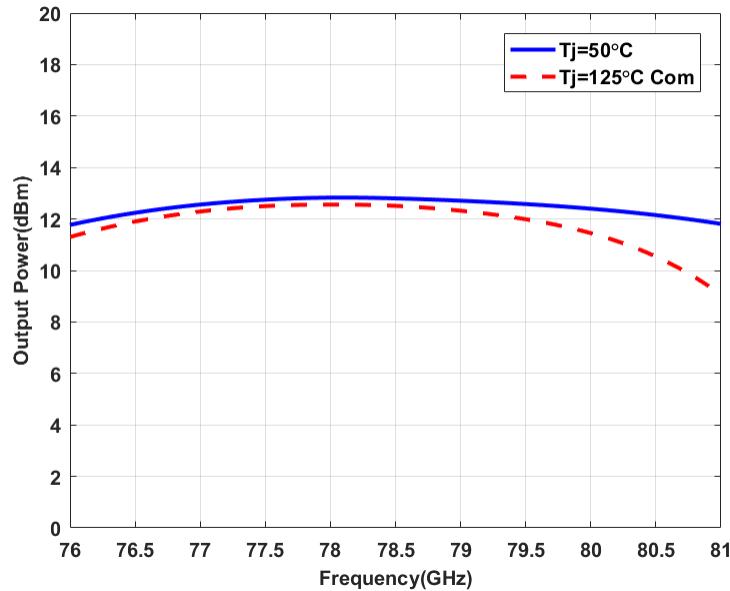


Fig. 5.11: TX Output Power with Compensation vs Frequency

## 5.1. Radio Subsystem

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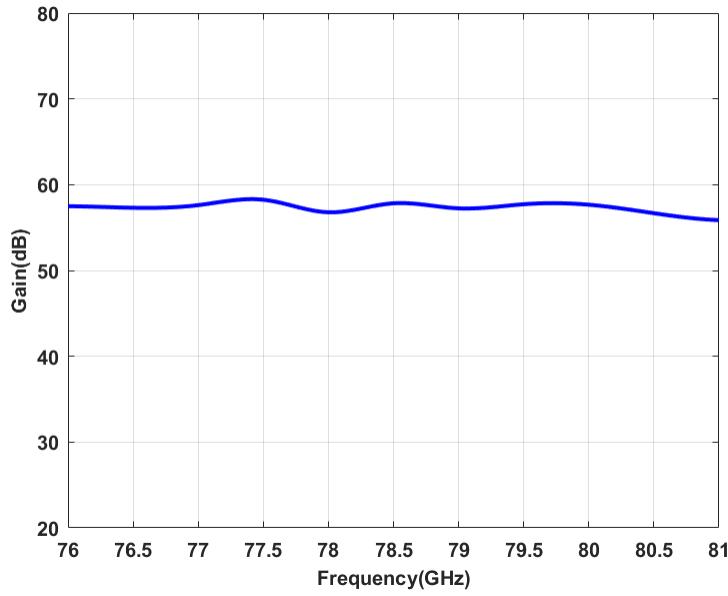


Fig. 5.12: RF Conversion Gain (CG\_typical) at  $T_A = 25^\circ\text{C}$

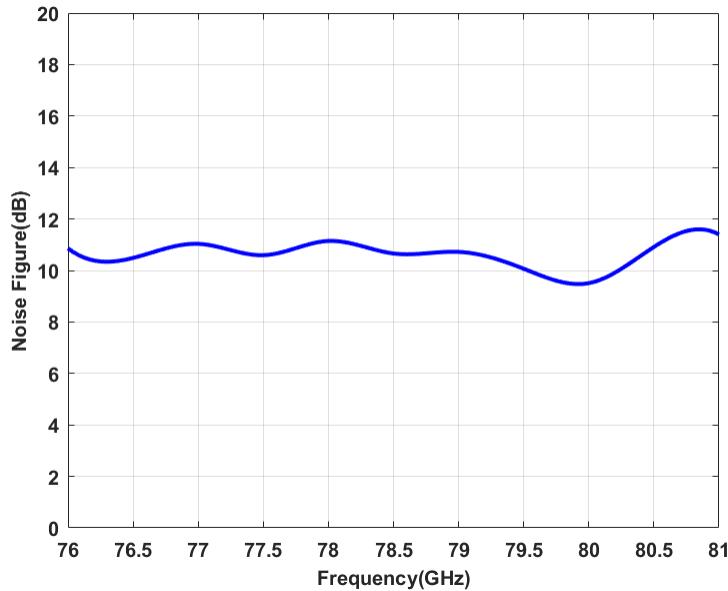
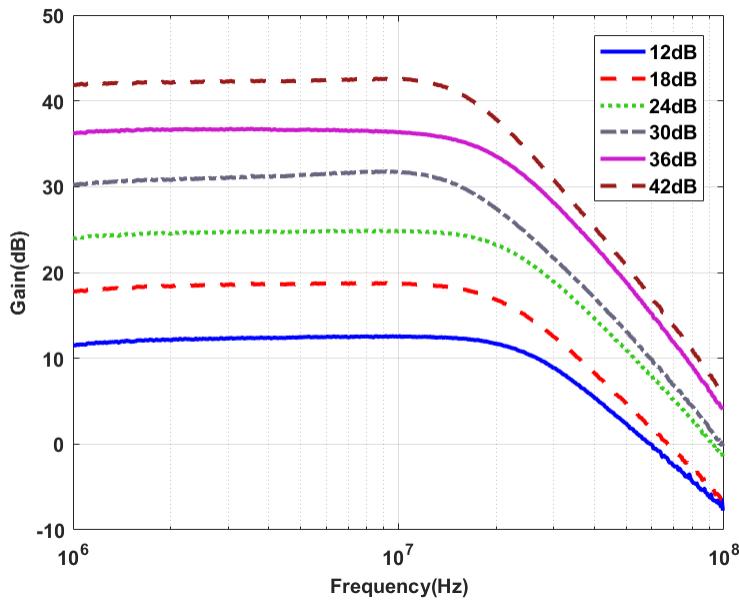


Fig. 5.13: Noise Figure (NF\_RX) at  $T_A = 25^\circ\text{C}$

Fig. 5.14: VGA Gain ( $G_{VGA1} + G_{VGA2}$ )

## 5.2 Processor Subsystem

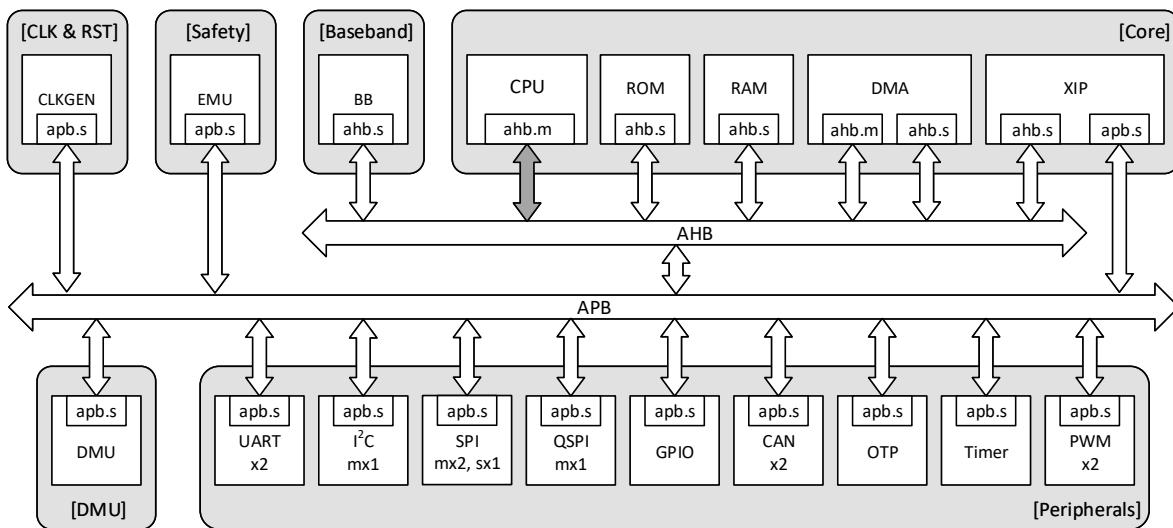


Fig. 5.15: Processor Subsystem

Fig. 5.15 briefly describes the processor subsystem, which can be divided into the following parts:

- Clock and reset
- Safety

## 5.2. Processor Subsystem

---

- Core
- Baseband
- Peripherals
- IO Mux

### 5.2.1 Clock and Reset

As illustrated by Fig. 5.16, all clocks in the processor subsystem are fed with three clocks from the radio subsystem, one boot clock used for boot, one 300-MHz clock, and one 400-MHz clock from PLL.

- Boot clock

The boot clock is used by the CPU to boot itself and to run programs to configure the radio subsystem. By default, the boot clock is connected to the RC clock. But there is an automatic switching from the RC clock to the XTAL clock once the XTAL clock is ready.

- 300-MHz clock

The 300-MHz clock is used as the main processor clock for the CPU, DMA, RAM, and ROM.

- 400-MHz clock

The 400-MHz clock is typically used as the reference clock for the peripherals and the baseband.

The clocks of Execute in Place (XIP), baseband (BB), and all peripherals can be individually gated, while individual soft resets for those modules are also supported.



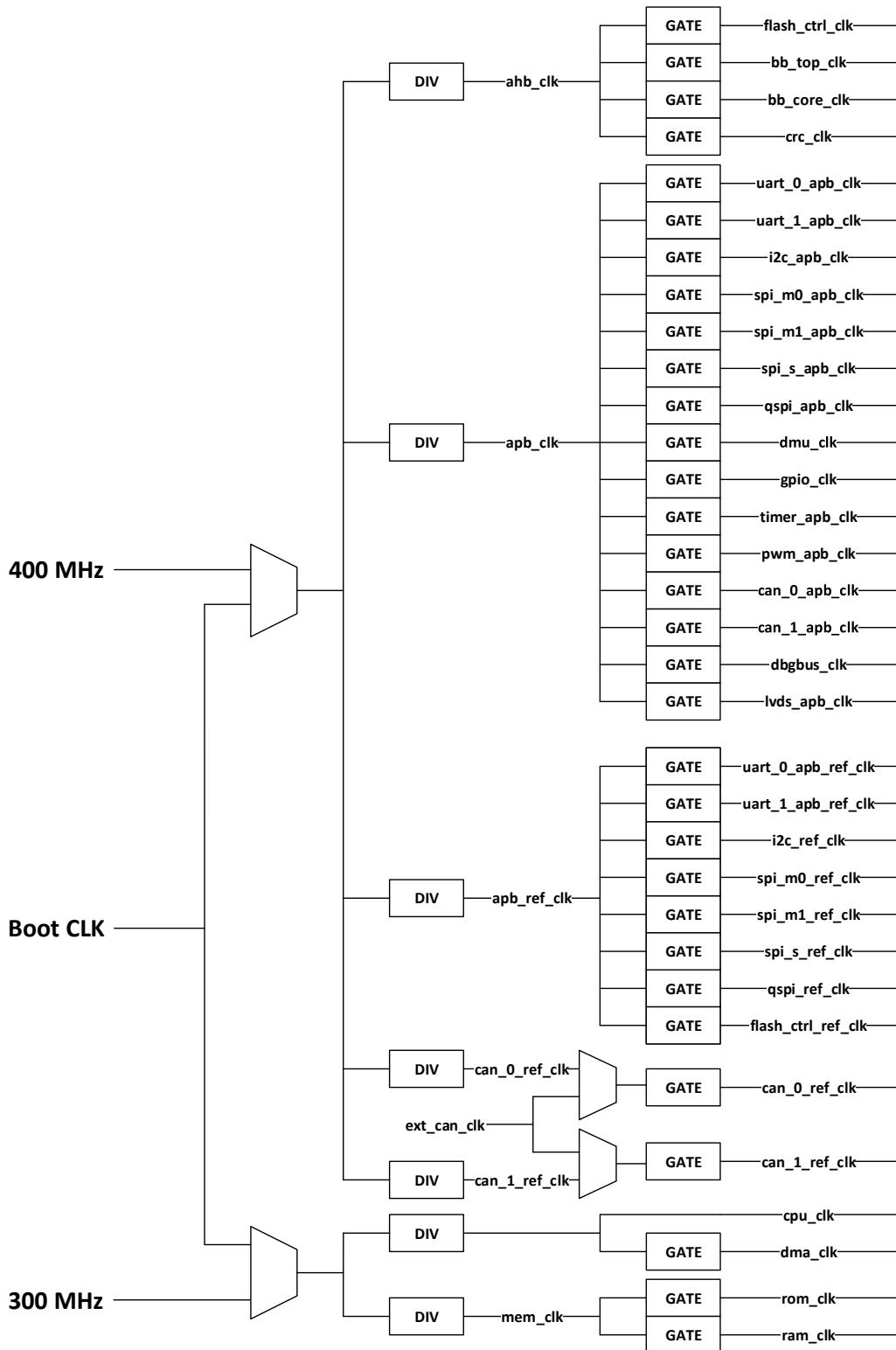


Fig. 5.16: Clock Organization

## 5.2. Processor Subsystem

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### 5.2.2 Safety

The safety module Error Management Unit (EMU) is at the top of the hierarchy of Alps. After PoR (power on reset) or external hard reset, the EMU starts the built-in self test (BIST), boots the system, and monitors the operation.

### 5.2.3 Core

The Core consists of one ARC CPU, one 16-KB ROM, one 576-KB RAM, one 8-Channel DMA, and one XIP module with 4-KB buffer. Since the ARC CPU normally runs at 300 MHz while the rest of the system runs at different frequencies, a cross-clock-domain bridge is adopted to connect them.

- ARC CPU

The ARC CPU integrated here is a little-endian CPU with a three-stage pipeline. The size of I-Cache, D-Cache, ICCM, and DCCM is all 32 KB. One real-time counter and two normal timers are integrated, as well as a watchdog timer. A single precision FPU is integrated which takes 2 clock cycles to finish a multiplication and 17 clock cycles to finish one division.

- ROM

The 16-KB ROM contains a pre-defined boot code. By executing it, CPU can boot from Flash, UART, SPI, and CAN.

- RAM

The RAM contains 576-KB space.

- DMA

The DMA module has 8 channels and one AHB master interface, which supports memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers, while either hardware handshaking or software handshaking interface is provided.

- XIP

The XIP module contains one 4-KB instruction buffer and one 512B data buffer.

The 4-KB instruction buffer can be mapped to 8 individual 16/32/64/128/256/512-byte spaces, or 4 individual 1024-byte spaces, or 2 individual 2048-byte spaces, or 1 individual 4096-byte space in the external flash.

The 512B data buffer can be mapped to 16/32/64/128/256/512-byte space in the external flash for read, or 256/52-byte space in the external flash for write.

XIP function can be manually turned on or off.

### 5.2.4 Baseband

Digital baseband is responsible for the processing of IF signals from the radio subsystem. It consists of four main parts, which are data sampling, FFT, CFAR, and DoA, and other advanced features.

- Data sampling

Data sampling serves for extracting valid ADC data in each chirp. Since the lowest sampling frequency is 20 MHz, a digital decimation filter is integrated to support SRR related applications.

- FFT

The 2D-FFT engine is configurable with range-FFT size ranging from 64 to 2048 points and Doppler-FFT size from 64 to 1024. But the product of the two FFT sizes is limited by the 2-MB FFT memory.

- CFAR

Two types of combination are supported in CFAR: coherent (or MIMO) and non-coherent (or SISO). The supported CFAR algorithms include CA, OS, SOGO, and NR. Up to 1024 objects can be reported by CFAR engine.

- DoA

DoA solves the angles of CFAR outputs. As a multi-object DoA, it searches up to 4 angles for each CFAR output.

- Advanced features

- Virtual array

This feature provides the capability to increase the resolution of DoA estimation by virtualizing more RX channels.

- Auto gain control

This feature prevents an RX channel from being saturated in an environment with large reflectors by ensuring that the system always uses the best RX Gain.

- Interference avoidance

This feature avoids interference during field usage by avoiding frequency and time collisions.

- Frame interleaving

This feature allows users to program up to four different types of frames at a time and use them for different application scenarios.

- Anti velocity ambiguity

This feature provides different solutions to solve the velocity ambiguity issue arising from sub-sampling at Doppler domain.

For detailed information and other features, refer to *Calterah Alps Radar Baseband User Guide*.

### 5.2.5 Peripherals

The Peripherals part contains two CANs, two UARTs, one master I<sup>2</sup>C, one slave SPI, two master SPIs, one master QSPI, one GPIO, one OTP memory, four timers, and two PWMs. All those peripherals are accessed through APB bus in one layer.

- CAN × 2

- Conform to ISO 11898.
  - CAN FD with up to 64 data bytes supported.
  - Up to 64 TX buffers, 64 RX buffers, 64 TX FIFOs, and 64 RX FIFOs.

- UART × 2

Two individual UARTs are integrated in the processor subsystem. Each UART has a 32-byte TX FIFO and a 32-byte RX FIFO. Baud rate is configurable, while the typical baud rate is 921,600.

- I<sup>2</sup>C master

The I<sup>2</sup>C master has an 8-byte TX FIFO and an 8-byte RX FIFO.

- QSPI master

The QSPI master has a 32-byte TX FIFO and a 32-byte RX FIFO. Transfer frequency is configurable, while the highest frequency is 50 MHz (refer to *QSPI Master Mode I/O Timings*).



## 5.2. Processor Subsystem

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- SPI master  $\times 2$

Two individual SPI masters are integrated in the processor subsystem. One SPI master has three selection lines, while the other has one selection line. Each of them has a 32-byte TX FIFO and a 32-byte RX FIFO. Transfer frequency is high configurable, while the highest frequency is 50 MHz (refer to [Master SPI I/O Timings](#)).

- SPI slave/QSPI slave

The SPI slave/QSPI slave has a 32-byte TX FIFO and a 32-byte RX FIFO. The maximum transfer frequency to which this SPI slave can respond is 50 MHz (refer to [Slave SPI I/O Timings](#)).

- GPIO
  - Up to 16 independently configurable signals.
  - With four ports A, B, C , and D, which are separately configurable.

- OTP Memory
  - Accessed through multiple sources
  - ECC protection
  - Program and read locks

- Timer  $\times 4$ 
  - Up to four programmable timers.
  - Support for two operation modes: free-running and user-defined count.
  - Support for independent clocking of timers.

- PWM  $\times 2$ 
  - Programmable pulse-width modulation of timer toggle outputs.
  - Pulse width modulation of timer toggle output with 0% and 100% duty cycle.

### 5.2.6 DMU

The debug management unit (DMU) is responsible for:

- Radio command
- ADC control
- DAC control
- Interrupts
- IO mux configuration

### 5.2.7 Processor Subsystem Memory Map



Table 5.2: Memory Map of Alps

Name	Mapping Space	Size (Byte)	Description
ROM	0x000000-0x003FFF	16 K	Boot ROM
ICCM	0x100000-0x107FFF	32 K	Instruction closely coupled memory
XIP (mem)	0x300000-0x6FFFFF	4 M/16 K	Memory interface of XIP; 4 M when XIP is on; 16 K when XIP is off, starting from 0x6FC000
RAM	0x770000-0x7FFFFFF	576 K	RAM
RAM (shared)	0x800000-0x9FFFFFF	2 M	Baseband shared memory
DCCM	0xA00000-0xA07FFF	32 K	data closely coupled memory
EMU	0xB00000-0xB00FFF	4 K	Register interface of EMU (Error Management Unit)
Timer	0xB10000-0xB100FF	256	Register interface of Timer
CLKGEN	0xB20000-0xB20FFF	4 K	Register interface of clock and reset management module
UART0	0xB30000-0xB300FF	256	Register interface of UART 0
UART1	0xB40000-0xB400FF	256	Register interface of UART 1
I2C_M	0xB50000-0xB500FF	256	Register interface of I <sup>2</sup> C master
SPI_M0	0xB60000-0xB600FF	256	Register interface of SPI master 0
SPI_M1	0xB70000-0xB700FF	256	Register interface of SPI master 1
SPI_S	0xB80000-0xB800FF	256	Register interface of SPI slave
QSPI_M	0xB90000-0xB900FF	256	Register interface of QSPI master
DMU (radio_ctrl)	0xBA0000-0xBA00FF	256	Register interface of radio configuration
DMU (debug_bus)	0xBA0100-0xBA01FF	256	Register interface of debug bus
DMU (io_mux)	0xBA0200-0xBA02FF	256	Register interface of IO mux
DMU (sys_config)	0xBA0300-0xBA03FF	256	Register interface of system configuration
DMU (sw_interrupt)	0xBA0400-0xBA04FF	256	Register interface of software interrupt
DMU (cpu_irq_mask)	0xBA0500-0xBA05FF	256	Register interface of CPU interrupt mask
CAN_0	0xBB0000-0xBB3FFF	16 K	Register interface of CAN 0
CAN_1	0xBC0000-0xBC3FFF	16 K	Register interface of CAN 1
PWM	0xBD0000-0xBD00FF	256	Register interface of PWM
GPIO	0xBE0000-0xBE00FF	256	Register interface of GPIO
OTP	0xBF0000-0xBF01FF	512	OTP memory

Continued on next page

Table 5.2 – continued from previous page

Name	Mapping Space	Size (Byte)	Description
BB (reg)	0xC00000-0xC0FFFF	64 K	Register interface of baseband
CRC (reg)	0xC10000-0xC100FF	256	Hardware CRC
DMA	0xC20000-0xC2003FF	16 K	Register interface of DMA
XIP (reg)	0xD00000-0xD001FF	512	Register interface of XIP
LVDS	0xD10000-0xD100FF	256	Register interface of LVDS
BB (mem)	0xE00000-0xFFFFFFFF	2 M	memory interface of baseband



## SAFETY MONITORING

### 6.1 Error Management Unit (EMU)

The error management unit (EMU) is at the top of the hierarchy of Alps. After PoR (power-on reset) or external hard reset, the EMU starts the BIST test, boots the system, and monitors the operation.

#### 6.1.1 Safety Pins

As shown in [Table 6.1](#), the ERROR and SAFE\_STATE pins indicate the safety states in function mode.

Table 6.1: Safety Pin

PIN	Description
ERROR	Test for safety failed. The chip enters the error state.
SAFE_STATE	Test for safety failed. The chip enters the reset state (safe state).

### 6.2 Analog Safety Mechanisms

The main safety monitoring and diagnostic mechanisms for the analog part available in CAL77S244 are listed below.

#### 6.2.1 RF BIST

[Fig. 6.1](#) shows the block diagram of RF BIST. A low-frequency testing signal  $f_{bb}$  is generated, up-converted to mmWave, and injected into 4 receiver channels. The default frequency of  $f_{bb}$  is 5 MHz and can be configured through SPI. Signal types of sinusoid and square-wave are supported.  $f_{bb}$  can also be output in differential or quadrature form to TESTMUX for additional testing purposes.

## 6.2. Analog Safety Mechanisms

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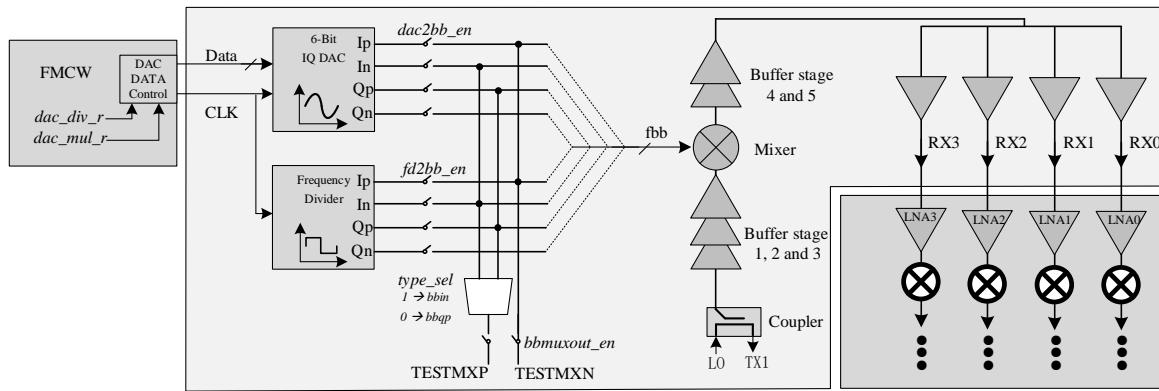


Fig. 6.1: RF BIST

### 6.2.1.1 RF Loop Test

Fig. 6.2 shows the signal flow of RF Loop Test. The testing signal  $f_{bb}$  is up-converted to mmWave and injected to 4 receiver channels. The carrier of mixer is coupled from LO path, so the testing signal will be down-converted by each receiver channel and sampled by ADCs. The functionality of receivers can be validated by comparing the ADC output levels of each channel.

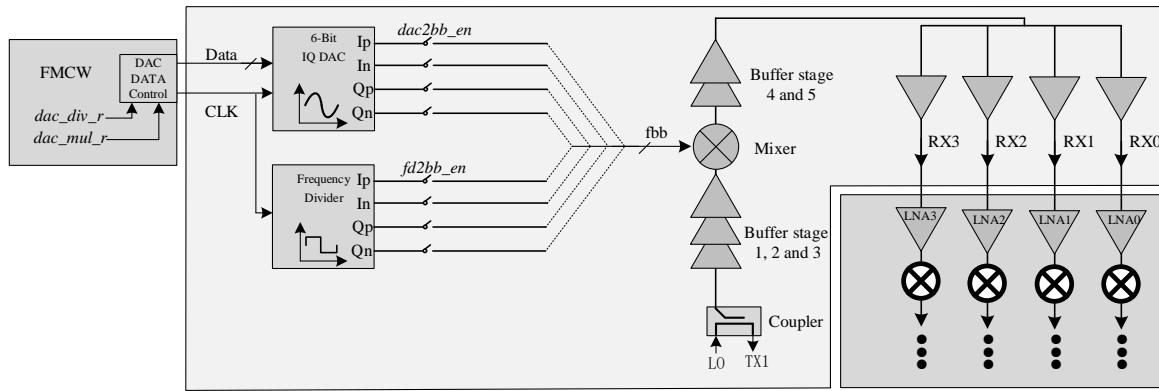


Fig. 6.2: RF Loop Test

### 6.2.1.2 IF Loop Test

Fig. 6.3 shows the signal flow of IF Loop Test. Differential testing signals are injected into analog baseband at selected points and output, through which the gain of each baseband block can be monitored.



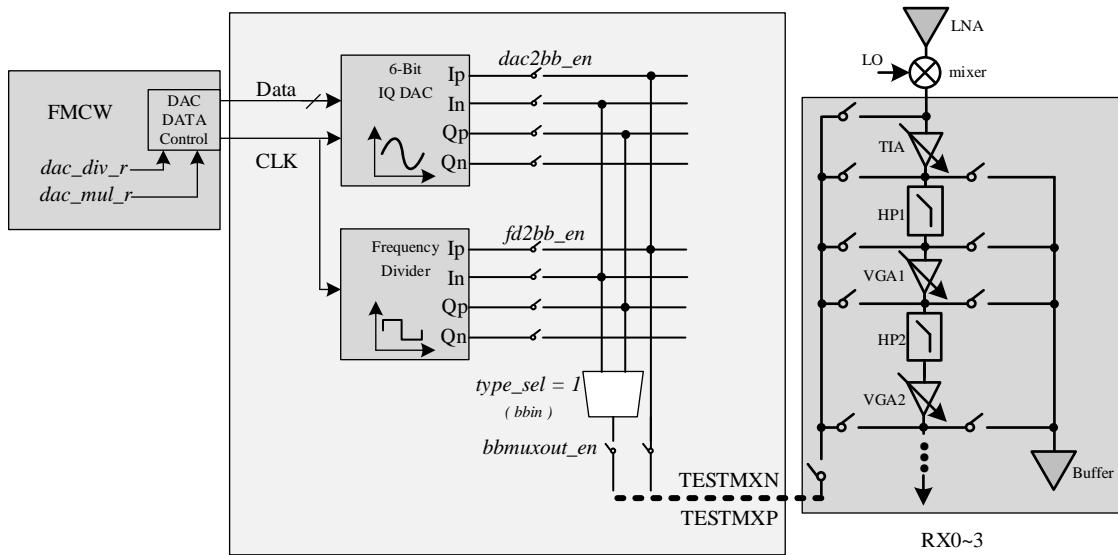


Fig. 6.3: IF Loop Test

## 6.2.2 Chirp Monitor

The chirp monitor monitors the quality of FMCW ramp waveforms by counting the output clock signal of FMCW VCO and comparing it to an ideal frequency ramp accordingly. If the frequency error exceeds the threshold set by the user, it will be reported to the CPU.

## 6.2.3 CPU Clock Lock Detector

This lock detector continually monitors the lock state of REFPLL.

## 6.2.4 TX Power Detector

TX Power Detector detects the power (voltage swing) at the output of each TX channel.

## 6.2.5 RXBB Saturation Detector

The differential outputs ( $V_{op}/V_{on}$ ) of TIA/VGA1/VGA2 are compared to a threshold, which is programmed through SPI. The comparison results will be summed up and sent to the CPU to indicate the saturation level of the RXBB analog output.

## 6.2.6 External Power Supply Monitor

External Power Supply Monitor monitors the 3.3V power supply, which is used for power-on reset and central bias circuitry, as well as the 1.1V power supply, which is used for digital circuitry. The voltage is compared to the programmed threshold range. When the supply is out of the threshold range, the error is detected and then reported to CPU.



## **6.3. Digital Safety Mechanisms**

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### **6.2.7 Internal LDO Monitor**

Different LDOs can be sampled sequentially by the auxiliary ADC through analog switch. The sampled result is then compared to a programmed threshold range. If the result is out of the range designed, Internal LDO Monitor sends an IRQ to the CPU. Otherwise, it will continue to process next LDO sample.

### **6.2.8 Bandgap Voltage Monitor**

There are two bandgap circuitry on chip. The VBG from circuitry A is compared to the programmed threshold range generated by circuitry B. When the VBG is out of the threshold range, an IRQ will be sent to the CPU.

### **6.2.9 Temperature Sensor**

A temperature sensor that covers a temperature range from -50°C to 150°C is integrated in the Alps chip. A voltage proportional to the absolute temperature generated by a dedicated bandgap is multiplexed to one of the two auxiliary ADCs, whose digital output indicates the temperature of the chip.

### **6.2.10 Auxiliary ADCs**

Two auxiliary ADCs are used to measure DC voltage. Each consists of a front-end buffer, a discrete-time sigma-delta modulator and a decimation filter, covering a voltage range from 0.5 V to 2.5 V. And multiple voltages from the external or within the chip can be multiplexed to the input of each ADC. Both ADCs have a 10-bit resolution.

## **6.3 Digital Safety Mechanisms**

### **6.3.1 Error Code Correction (ECC)**

All the internal RAMs and ROMs are protected by the Error Code Correction (ECC) module. While accessing the RAMs and ROMs, single-bit errors and double-bit errors are generated and sent to the Error Management Unit (EMU).

### **6.3.2 Cyclic Redundancy Check (CRC)**

The cyclic redundancy check (CRC) is error-detection code to detect accidental changes to raw data. Blocks of data entering the system get a short check value attached, based on the remainder of a polynomial division. The calculation is repeated at the receiver to check whether the value is correct or not.

### **6.3.3 SPI Loop Test**

SPI loop test is the internal test mode. In this mode, SPI\_M0 and SPI\_S are connected by internal logic.

### **6.3.4 Baseband Run-Time LBIST**

Baseband run-time logic BIST (LBIST) is triggered between frames. Whenever a logic circuit failure inside the baseband module is detected, an error interrupt shall be sent to EMU.

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## CHAPTER SEVEN

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### PACKAGE

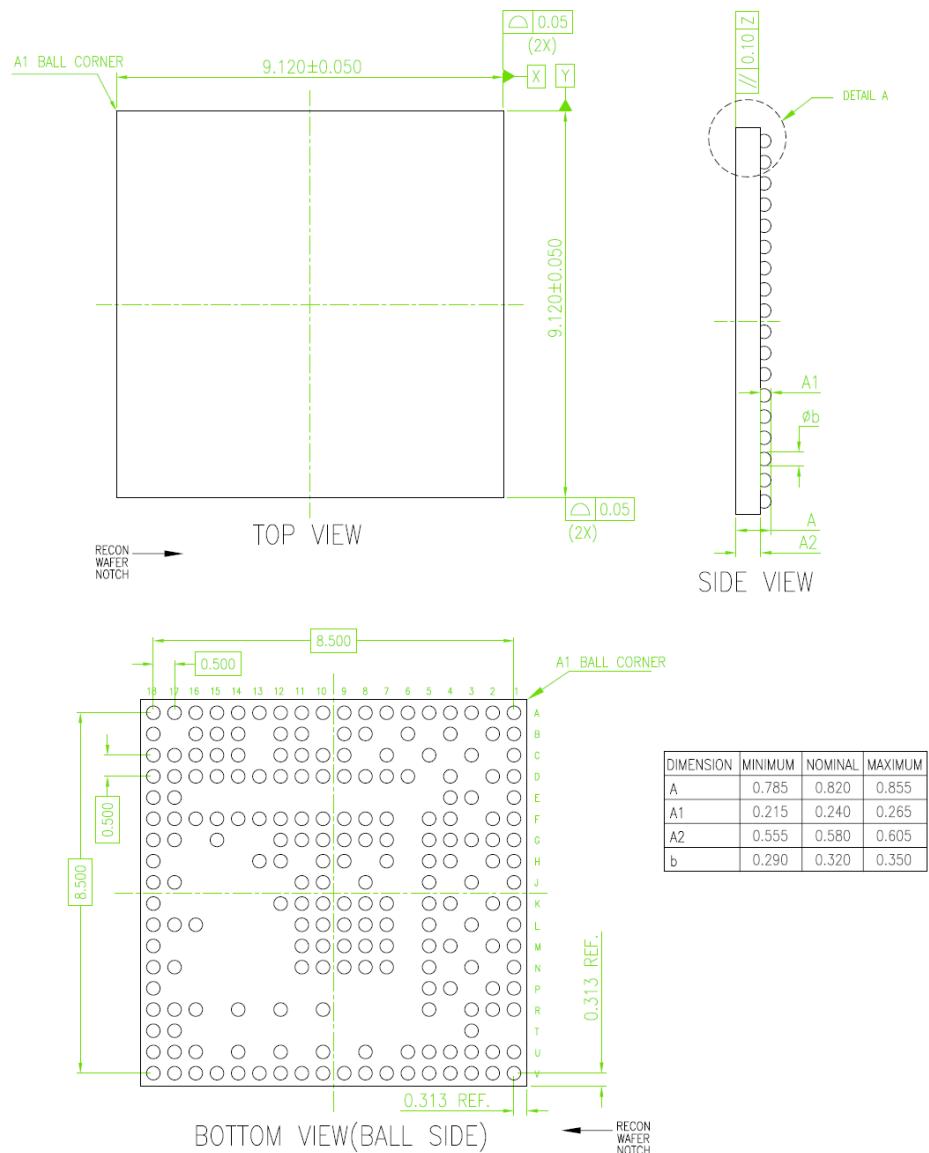
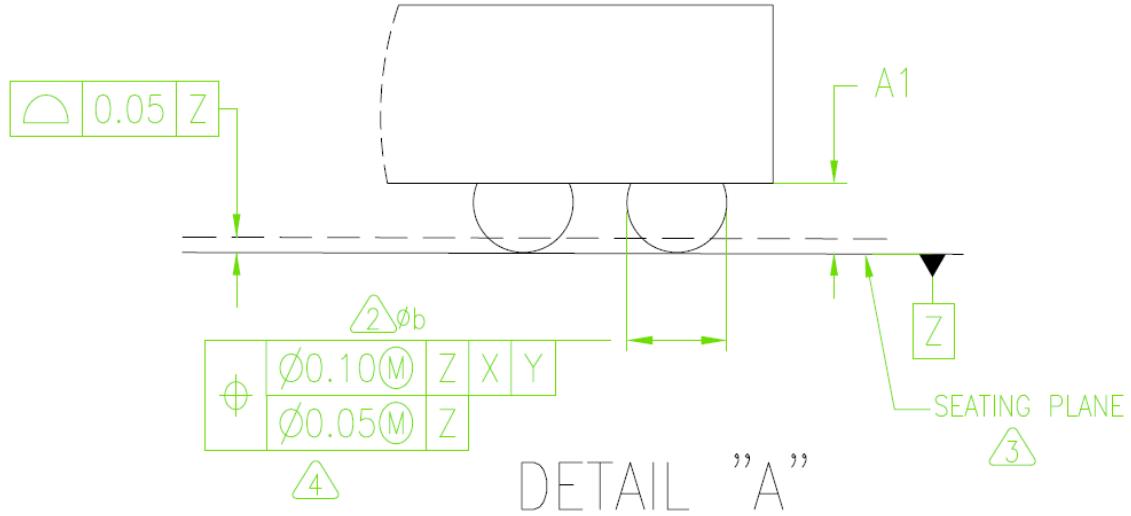


Fig. 7.1: Package Outline Drawing (POD) 1



NOTES:

1. DIMENSIONS AND TOLERANCE PER ASME Y 14.5M – 2009, JESD 95-1.
  2. DIMENSION IS MEASURED AT THE MAXIMUM BALL DIAMETER PARALLEL TO PRIMARY DATUM **Z**
  3. PRIMARY DATUM **Z** AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE BALL.
  4. BALL POSITION DESIGNATION PER JESD 95-1.
5. THE RAW SOLDER BALL SIZE IS 300um.

Fig. 7.2: Package Outline Drawing (POD) 2

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**APPENDIX  
A**

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**REVISION HISTORY**

Table A.1: Revision History

Revision	Description	Author
0.1 / June 2018	Initial release for Alps A sample.	pwang
0.2 / September 2018	<p>Updated the Chip Signal Definitions table.</p> <p>Updated the Pin Multiplexing table.</p> <p>Updated the block diagram of Radio Subsystem.</p> <p>Updated the style of page header and footer.</p>	pwang
0.3 / Jan 2019	<p>Added the Antenna in Package (AiP) chapter.</p> <p>Updated the Chip Signal Definitions table in the Device Information chapter.</p>	pwang
0.4 / March 2019	<p>In the Introduction chapter, updated the Features section and the Chip Block Diagram.</p> <p>Updated the Device Information chapter.</p> <p>Updated the Detailed Descriptions chapter.</p> <p>Updated the Package Outline Drawings in the Package chapter.</p> <p>Removed the Antenna in Package (AiP) chapter, because Alps ESB AiP information is currently unknown.</p> <p>Other minor changes.</p>	pwang
0.5 / July 2019	<p>Added the Thermal Resistance Characteristics for eWLB Package section.</p> <p>Updated electrical characteristics of power consumption, PLL, and ADC.</p> <p>Changed GPADC to Aux ADC.</p> <p>Updated the Phase Scrambling section.</p> <p>Updated timing characteristics of I<sup>2</sup>C, master SPI, slave SPI, and QSPI.</p> <p>Other minor changes.</p>	pwang

Continued on next page

Table A.1 – continued from previous page

Revision	Description	Author
0.9 / March 2020	<p>Updated the Introduction chapter.</p> <p>Updated the Device Information chapter.</p> <p>Updated the Electrical Characteristics chapter and renamed the chapter to Specifications.</p> <p>Updated the Timing Characteristics chapter.</p> <p>Updated the Detailed Descriptions chapter.</p> <p>Added the Safety Monitoring chapter.</p>	pwang
1.0 / July 2020	Official release for the mass production version.	pwang



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