1 Normal operation analysis

Definitions:

Definition. *A state graph consists of <V, S, T> where V is the set of finite signals $v_1..v_n$. S is the function $S : V \to \{0, 1\}$ which maps each variable to a boolean, an element of S is called a state. T is the set of all transitions in the state graph and $T \subseteq S \times S$.*

A transition has the additional constraint that only one signal is allowed to change between the two states in the transition.

Definition. *A transition $T(s_i, s_j)$ denotes a transition from the state s_i to s_j. Then there exists a signal w and any signal u where $u \neq w$ such that $s_i(w) \neq s_j(w)$ and $s_i(u) = s_j(u)$.*

State graphs can be implemented as an asynchronous circuit where the signals of a state graph V maps one-to-one to wires in the circuit. Then the set of states S can also describe the state of wires of the circuit. The circuit has a set of transitions. A transition of the circuit from a state $s_i \in S$, to a state $s_j \in S$ exists if and only if $T(s_i, s_j)$.

Definition. *A wire u in the circuit is **excited** in state s_i if $T(s_i, s_j)$ and $s_i(u) \neq s_j(u)$. Alternatively if one treats the output of wire u as a function of the current state s_i, then $f(s_i) \neq s_i(u)$*

Semi-modularity means once a wire is excited, it stays excited until it transitions to the excited value. Circuits that are semi-modular are also speed independent. Formally this can be defined as follows:

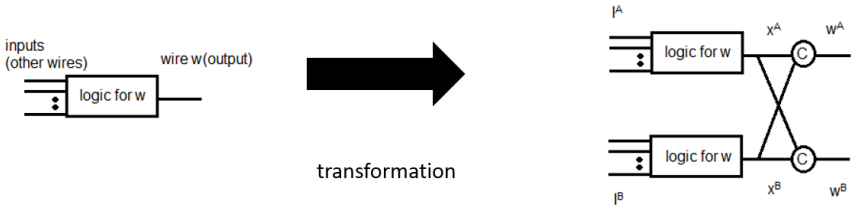
Definition. *An asynchronous circuit is **semi-modular** if for every s_i and s_j such that $T(s_i, s_j)$ holds, and let u and w be wires such that $s_i(u) \neq s_j(u)$ and $w \neq u$, then if $s_i(w)$ is excited, $s_j(w)$ is also excited*

Definition. ***Trace** σ of a circuit is a sequence of states of infinite length where σ_i is the i^{th} term of the sequence. $\sigma : \mathbb{N} \to S$ and $T(\sigma_i, \sigma_{i+1})$ for $\forall i \in \mathbb{N}$*

Definition. *Two circuits A and B are **equivalent** if the set of all traces from circuit A and circuit B are equal $\{\sigma^A | \sigma^A$ is a possible trace in $A\} = \{\sigma^B | \sigma^B$ is a possible trace in $B\}$ (Traces(A)= Traces(B)?).*

An additional property of the asynchronous circuit is that one can view each wire as a separate black box. For a wire w, inputs from the rest of the circuit (I_w and $I_w \subseteq$ V) feed into a gate and outputs the wire value w. We call the instantaneous value of the gate for w of a state s as $f_w(s|_I)$, where f is the function $f : [I \to \{0, 1\}] \to \{0, 1\}$ and $s|_I$ is the state s projected on the input variables I_w. If inputs to the gate remain constant, the output w will eventually take the value specified by $f_w(s|_I)$

We transform the circuit by making a duplicated copy of the gates to each wire, and connect the outputs of the duplicated gates to two c-elements. We label the duplicated circuit halves as circuit A and circuit B. Then for each wire w we add in intermediate wires x^A and x^B to label the output of the gate of w for circuits A and B respectively. x^A and x^B are also the inputs to two C-elements. We can (arbitrarily) label one of the C-element outputs as w^A and the other output as w^B. These then connect to other gates in circuit A and circuit B respectively. (Note that the outputs of the C-elements can be arbitrarily named and connected to the next gates, and the next gates can also be arbitrarily named A or B as long as it does not create any inconsistencies in the naming convention)



Because the transformed circuit has some extra wires, we want to define a correspondence to be able to compare between the wires of the original circuit and that of the duplicated circuit halves. For the duplicated circuit, a combined state is the pairing of the state of circuit A and the state of circuit B. It has quadruple the number of wires for each wire in the original circuit. The state graph for a duplicated circuit is defined on this combined state. We define the mapping $h^A : s^{full} \to s^A$ where s^{full} is the combined state of a duplicated circuit and s^A are made up of the wires w^A that correspond to the original wires w. h^B is similarly defined to map to s^B. Note that the $h(\sigma)$ mappings are overloaded for a trace, where it outputs a mapping for each of the states in a trace.For a trace in the duplicated circuit we project the full states onto a shortened list of wires (ie the wires corresponding to the original circuit). The resulting trace may have successive repeated states and we delete the repeats to obtain a valid trace on the shortened wires.
We want to show this circuit behaves similar to the original circuit under normal operation. In other words we want to prove that after applying either mapping of h^A or h^B, the resultant circuit and the original circuit are equivalent.

Theorem. *Starting from all valid initial states in the original circuit (and a predefined correspondence to the initial state in the duplicated circuit) and for all n, if σ is a trace in the duplicated circuit and σ_n is the sequence of the first n states of σ, then $h^A(\sigma_n)$ is a prefix of a trace in the original circuit (h might make the trace shorter, so the prefix will not be of length n).*

Proof. We prove this by induction on an expanded list of properties, and then show that these properties prove the original theorem is true. Without loss of generality we assume these properties hold for only the A half of the circuit. The same reasoning then applies to the B half of the circuit. We define an

induction hypothesis which is the conjunction of these three properties for some σ that is a trace in the duplicated circuit and $n \in \mathbb{N}$:

1. $h^A(\sigma_n)$ is a prefix of a trace in the original circuit. We define s_n as the n^{th} element of σ_n (the current state).

2. (If a wire is excited in the original circuit then exactly one of the gate or the c-element is excited in the duplicated half. If a wire is not excited, then neither the gates or the c-element is excited) If the duplicated circuit is in state s_n and the original circuit is in state $h^A(s_n)$, and for all wires w that are excited in this state $f_w(s_n|_I) \neq w$ in original circuit, then $f_w(s_n|_I) \neq x^A$ or $x^A \neq w^A$ in duplicated circuit (exactly one of these is true). In addition, if wire w is not excited in the original circuit $f_w(s_n|_I) = w$, then in the duplicated circuit half $f_w(s_n|_I) = x^A = w^A$.

3. For all output wires w in state s_n, if the corresponding output wire in A and B are different, this indicates that one of the c-elements to A or B is excited. For all output wires w, if $w^A \neq w^B$ then $x^A = x^B$

The base case is constructed as follows: given any initial state in the original circuit $s \in S$, for each wire w assign the values for the wires in the duplicated circuit according to $x^A = x^B = w^A = w^B = w$. This is s_0 in the duplicated circuit. It is simple to see that this initial state satisfies all three properties.
Next is the induction step, assume we are in a full state $s_k = (s_i^A\ s_j^B)$ and these three properties are true, we will prove each of the properties are true for $k+1$.

1. Due to property 2) we know that only wires excited in the original circuit in state s_i may have excited components. For all wires w that are excited in the original circuit, if logic gate is excited $f_w(s_i|_I) \neq x^A$ then a transition on x^A may occur. The value of w^A remains the same and $\mathrm{h}^A(s_k) = h^A(s_{k+1}).Otherwiseif\mathrm{x}^A \neq w^A$ then there are two cases, if $x^A = x^B$ and if $x^A \neq x^B$. Case 1: $x^A = x^B$ the c-element is excited and w^A can transition to the new value $w^A_{next} = x^A$. Case 2: $x^A \neq x^B$ and no transition can occur. The first case is the same as w transitioning in the original circuit and $T(h^A(s_k), h^A(s_{k+1}))$. Thus property 1 is true for $n+1$.

2. A transition may only take place in circuit A if the wire w is excited in the original. If $f_w(s_k) \neq x^A$ and a transition on x^A occurs then $f_w(s_{k+1}|_I) = x^A_{next}$ and $x^A_{next} \neq w^A_{next}$. If $x^A \neq w^A$ and $x^A = x^B$ and w^A transitions then $x^A_{next} = w^A_{next}$, in addition since $h^A(s_{k+1})$ is also a state in the original circuit (from above) then the set of newly excited wires are the same in the original circuit and circuit A. For all wires w in the newly excited set, since w was previously not excited, then $f_w(s_{k+1}) \neq x^A_{next}$ and $x^A_{next} = w^A_{next}$. Due to semi-modularity the wires excited at s_k is still excited at s_{k+1} in the original circuit with the exception of the wire that transitioned. In circuit A, if $f_w(s_k|_I) \neq x^A$ then $f_w(s_{k+1}|_I) \neq x^A_{next}$ since it is the same logic gates and inputs as the original circuit. And if $x^A \neq w^A$ then $x^A_{next} \neq w^A_{next}$ since no transitions occured in x^A or w^A. For a wire

w not excited in s_k and it is not excited in s_{k+1} in the original circuit, in circuit A we have $x^A = w^A$ then $x^A_{next} = w^A_{next}$ and $f_w(s_{k+1}|_I) = x^A_{next}$. Thus property 2 holds in any next state s_{k+1}

3. We will prove this property in $n+1$ by contradiction. Suppose this property is not true in a possible next state so $w^A_{next} \neq w^B_{next}$ and $x^A_{next} \neq x^B_{next}$. This means that in the current state if $w^A \neq w^B$ and $x^A = x^B$ then a transition on x^A or x^B occurs. Without loss of generality, assume $w^B = x^B$, then x^A cannot transition or it would violate property 2 above. Then x^B transitions. Because of assumption of 3 in state s^A_i, s^B_j there is a possible sequence of transitions on the inputs of wire w in circuits A and B so that they are equal. This means following a trace of h steps in the original circuit x^A_{k+h} can be excited which again violates property 2. Thus the initial assumption is false and this property is true in all possible next states. Therefore property 3 is true for $k+1$.

Finally there is always a transition available since if $w^A \neq w^B$ we can always use the trick above to produce a sequence of transitions so that $w^A = w^B$. And if the circuit is in this state there is a next availble transition following the original circuit. Thus the three properties are true for the step $k+1$. Induction follows. Property 1 is the original theorem which must also be true. □