Application Note AN4102

A Fairchild Power Switch based SMPS for Color Television Receivers

Introduction

A switched mode power supply (SMPS) typically consists of a power transformer, secondary side rectifier diodes, a switching semiconductor device, a control IC, and peripheral circuits. Besides its basic function of supplying power to the load on the secondary side, an SMPS may have to perform other, special functions, depending on the system. For example, an SMPS for a color television receiver must minimize the effect of switching noise on the screen and reduce power consumption in standby. If the level of integration of the switching circuitry is not high enough, then additional, separate circuits will be required to accommodate all functions; these additional components raise the overall SMPS cost and not uncommonly reduce reliability. The highly integrated Fairchild Power Switch (FPS) combines a high power MOSFET and control IC into one package and, moreover, enhances IC functionality. It includes protective functions, thereby minimizing the number of additional components needed in an SMPS. Fairchild Power Switch (FPS) is widely used in the power circuits of a variety of equipment, such as color TVs, printers, PCs, monitors, and, of course, battery chargers and ac adapters. The KA3S-series Fairchild Power Switch (FPS) series was first introduced for color TVs; the SMPS described in this application note uses a KA5Q-series Fairchild Power Switch (FPS). KA5Q-series Fairchild Power Switch (FPS) incorporates enhanced protection functions and has a much reduced power consumption in standby mode.

The most frequently used power circuits in household appliances are the flyback converter and the forward converter, both of which use the pulse width modulation (PWM) control method for fixed frequency switching. However, a general purpose PWM based SMPS cannot be used for a monitor or color TV, because the SMPS's switching noise would seriously affect the display quality. The switching noise would appear in the form of picture noise. To significantly reduce the effect of switching noise on the screen a power supply for a monitor has to be able to synchronize its switching frequency to an external signal, typically the monitor's horizontal sync flyback signal. Such a sync technique cannot be used in color TVs, however, since, unlike monitors, a color TV's horizontal deflection frequency is too low. Instead, an SMPS for a color TV makes use of the so called quasi resonant technique. In this technique a capacitor is added between the MOSFET drain and source, which lowers both the rising slope of the voltage Vds between the MOSFET's drain and source and the falling slope of the reverse voltage across the secondary side rectifier diodes when the MOSFET turns off. The shallower slopes reduce the dV/dt switching noise and switching loss, because the MOSFET turns on when Vds is at a minimum or zero. To comply with regulatory trends aimed at reducing standby power consumption, KA5Q-series Fairchild Power Switch (FPS) features a built in burst mode. Burst mode operation make it possible to reduce output voltages in standby to almost half those of the normal on mode. This can reduce standby input power demand to under 3W at 230Vac or, if few peripheral components are added, to possibly even 1.5W. Moreover, as implemented in the KA5Q-series, burst mode operation causes no audible noise and requires almost no additional components. To reduce losses further, KA5Q-series Fairchild Power Switch (FPS) has lower IC start up and operating currents than the KA3S-series, and quasi resonant operation can continue even in burst mode. Also, the KA5Q-series can perform primary side regulation using a built in error amplifier, which replaces the secondary side error amp and eliminates its peripheral circuits. Overall, the KA5Q-series incorporates five protection features to increase SMPS reliability:

- Pulse by pulse over current protection.
- Over voltage protection.
- Over load protection.
- Thermal protection.
- Over current latch.

This application note contains working design example (Section 8) of an SMPS for use with color TVs or other high power applications. It is a universal input supply adaptable to ac input voltages world wide, and uses the Fairchild Power Switch (FPS)'s burst mode capability to achieve very low standby power consumption: less than 2W at 230Vac. The SMPS features variable frequency, quasi resonant switching; current mode control; built in secondary side regulation; and an array of built in protection features, including pulse by pulse over current protection and shutdown, over voltage protection with auto restart, overload protection with auto restart, and thermal shutdown.

1. Quasi resonant Operation

When a hard switched SMPS is used for a color TV, the MOSFET generates a very high frequency current spike at turn on, and this spike shows up as noise on the screen. Also, because the MOSFET's output capacitance, Coss is small, a fast MOSFET turn off abruptly increases its drain to source voltage Vds at a high dV/dt. This generates a voltage spike that produces common mode noise on the secondary side, which again results in on screen noise. Figure 1 shows a flyback converter that uses the quasi resonant technique. Lm is the transformer's primary side magnetizing inductance, and D1 is the MOSFET body diode. Neither the inductor nor the diode is a physically separate component. They are integral and implicit to the transformer and MOSFET, respectively, and are shown in Figure 1 for explanatory purposes. Current Id, that flows to the MOSFET increases at a constant rate when the MOSFET is on.

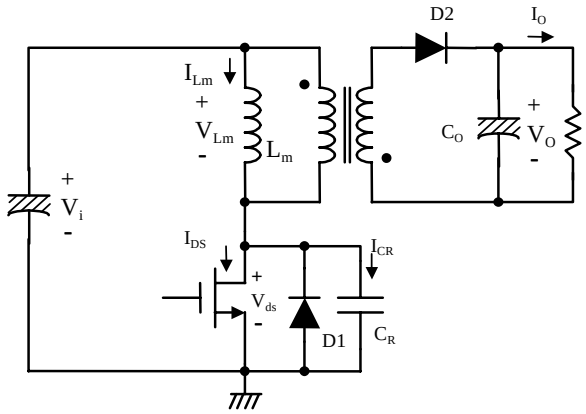


Figure 1. Simplified diagram of a flyback converter using the quasi resonant technique.

The MOSFET turns off when Id reaches the peak value (Ip in Figure 2) set by the control circuit, at which time the energy stored in the transformer in the form of flux charges capacitor Cr connected between the MOSFET's drain and source. This raises Vds. The rising slope of Vds increases as Ip increases and characteristic impedance Zr = (Lm/Cr)1/2 decreases. Cr, which is much larger than the MOSFET's output capacitance Coss, controls dV/dt when the MOSFET turns on and off, reducing it from what it would be otherwise. The charging of Cr continues until the secondary side rectifier diode D2 turns on, after which the transformer delivers current to the output. D2 is on for an interval proportional to Ip, during which Vds = Vin + nVo, (Figure 2).

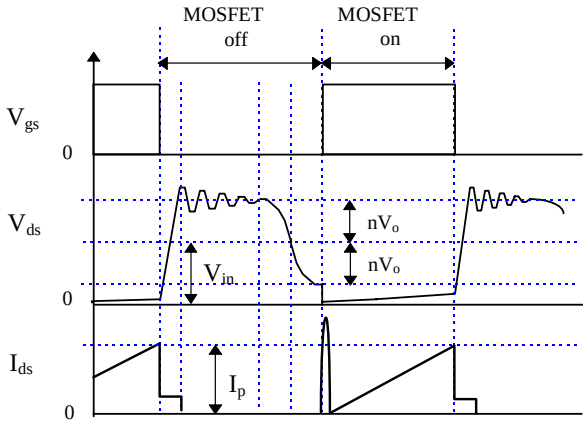


Figure 2. Waveforms for the circuit of Figure 1.

After all the energy stored in the transformer is delivered to the secondary side, Lm and Cr resonate and Vds starts to decrease. In the ideal case with no losses, the minimum value for Vds would be Vin - Vo. The actual value is slightly higher. At minimum Vds the sensing circuit turns on the MOSFET. (See Section 5 for a description of the sensing method.) Because the MOSFET is turned on when Vds, is minimum and not zero, the potential stored in Cr discharges as soon as the MOSFET turns on, which generates a large current spike. To reduce this spike, the Fairchild Power Switch (FPS)'s control IC is configured to slow the MOSFET's turn-on.The time required for Vds to reach minimum is $T_R (T_R = \pi\sqrt{LmCr})$, a fixed value independent of the input voltage or output current. Varying the switching frequency regulates the output voltage: the lower the switching frequency, the lower the input voltage and the higher the load current.

2. Secondary Side *vs*. Primary Side Regulation

Secondary side regulation requires an error amplifier and an opto coupler on the secondary side. The amplified error is transferred to the primary side through the opto coupler to control the MOSFET's on time and thereby precisely control the output voltage. The opto coupler also transfers the MCU signal received on the secondary side to the primary side to operate the burst mode. As explained in the following section, the burst mode allows low standby power to be achieved. Therefore, should it be necessary to guarantee a minimum standby power, an error amp and opto coupler would be required on the secondary side and the increased cost these components contribute to the design would have to be accepted. Primary side regulation is a method that regulates secondary side voltage indirectly, by controlling the primary side voltage. In the KA5Q-series Fairchild Power Switch (FPS), the error amp in the control IC senses

the IC's Vcc. This is compared internally to a built in reference. Use of this block may allow the secondary side opto coupler and error amplifier to be eliminated. Primary side regulation will be more cost effective than secondary side regulation. However, primary side regulation is not so precise as secondary side regulation, and its response to load variations is slow. Therefore, primary side regulation is advantageous only when considerations of lower cost out weigh the accompanying increase in standby power consumption and reduction in regulation performance.

3. Burst Mode Operation

The KA5Q-series Fairchild Power Switch (FPS)s burst mode capability allows all output voltages to be reduced to almost half those in normal (On mode) operation. It switches the Fairchild Power Switch (FPS)'s MOSFET by fixing the peak current (IP) flowing to it, exhibits a very low audible noise and makes possible an input power in standby mode of less than 2W at 230 Vac input. No external devices are required.

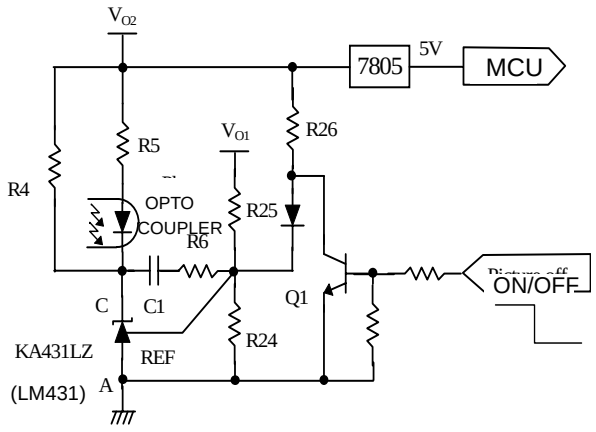


Figure 3. Reference diagram to demonstrate Fairchild Power Switch burst mode operation.

Figure 3 is a secondary side regulated circuit that demonstrates the Fairchild Power Switch (FPS)'s burst mode operation. Vo2 in the figure is a low value output voltage that also powers the MCU through the linear regulator 7805. Vo1 is the controlled output voltage that powers horizontal deflection and is the highest power output.

3.1 Burst mode operation in standby

Refer to Figure 3. When the picture on signal is low, Q1 turns off and Vo2 is applied directly through R26 and the diode to the LM431's reference pin, thereby increasing the voltage at this point and in turn increasing the current flow to the opto coupler. The voltage Vfb on the Fairchild Power Switch (FPS)'s feedback pin (pin 4) goes to zero (Figure 4; see also the complete circuit shown in Section 8), stopping the Fairchild Power Switch (FPS) MOSFET's switching action. As also shown in Figure 4, Vcc and Vo2 decrease to their respective levels as determined by R24, R26, and R25.

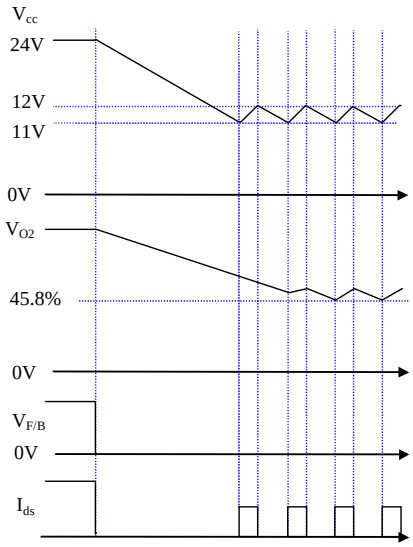


Figure 4. Normal (properly designed) burst mode operation, in which V_{cc} decreases faster than V_{o2}.

V_{CC}, which powers the Fairchild Power Switch (FPS) on the primary side, is regulated to 24V (see the circuit of Section 8, Fairchild Power Switch (FPS) pin 3). The operation of the burst mode controller depends on Vcc. If Vcc drops to 11V before the output voltages reduce to their respective levels as determined by R24, R26, and R25, the burst mode controller turns on; if it rises to 12V, the controller stops switching. The burst mode controller controls the MOSFET switching by restricting its peak current to a fixed value. This prevents the generation of audible noise and also maintains the Fairchild Power Switch (FPS)'s Vfb at 0V (Figure 4).

When the picture on signal goes high again, operation returns to the normal mode. The high picture on signal turns on Q1. Vo1, is divided by R24 and R25, and the resulting voltage is compared to the reference voltage in the error amplifier. Vfb increases, which regulates the MOSFET duty and output voltages increase to normal.

3.2 Design comments and a caution

Note that when the MOSFET stops switching (because the picture on signal has gone low), the output voltages decrease, but at different rates. The rates depend on output current and output capacitance. Because the example of the previous section is a real design, Figure 4 shows that Vcc decreases faster than Vo2.

Figure 5 however, shows how the burst mode would operate should Vo2 decrease faster than Vcc. Vo2 would decrease to the voltage set by R24, R26, and R25 before Vcc drops to 11V. The error amp would start to regulate, and the Fairchild Power Switch (FPS)'s Vfb, would increase slightly to a value just above 0V, as shown. Because the load is off, load current is low and Vfb is not at 0V, the MOSFET starts to switch

(see Ids, Figure 5), but the output voltage Vo2 remains at 45.8% of its normal mode voltage. When Vcc finally drops to 11V (45.8% of 24V, its normal mode level), the burst mode controller starts and Vcc and Vo2 increase. When Vcc rises to 12V, the MOSFET stops switching and the above operations repeat.

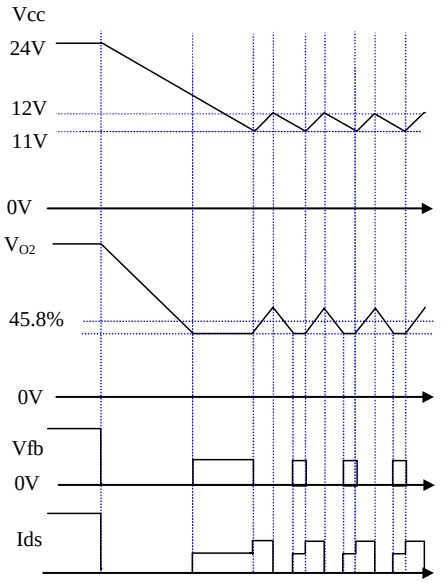


Figure 5. Abnormal burst mode operation in an improper design allowing V_{o2} to decrease faster than V_{cc}.

This kind of operation, where Vo2 decreases faster than Vcc extends the switching period and increases the switching loss. To prevent these effects, increase the value of the output rectifier capacitance (see, e.g., the circuit of Section 8 and Table 1, the parts list for that circuit).

4. Feedback Circuit Design

When secondary side regulation is used, the output voltage is determined by comparing the voltage to be controlled, Vo1, to the reference in the error amp. In this example it is 2. 5 V for an LM431. As shown in Figure 3, when the MCU picture on signal goes high, Q1 turns on and the diode in its collector turns off. Thus, R24 and R25 around the error amp are determined as follows

:

$$2.5 = \frac{R_{24}}{R_{24}+R_{25}}V_1$$

$$\therefore R_{25} = \frac{V_1 - 2.5}{2.5}R_{24}$$

In standby mode, however, with the picture on signal low, Q1 is off and the diode is on. Now R24, R25, and R26 determine the output voltage, which is calculated as follows:

$$2.5 = \frac{R_{24}//R_{26}}{R_{25}+R_{24}//R_{26}}V'_1 + \frac{R_{25}//R_{24}}{R_{26}+R_{25}//R_{24}}(V'_2 - 0.7)$$

$$\therefore R_{26} = \frac{R_{25}R_{24}(V'_2 - 0.7 - 2.5)}{2.5(R_{25}+R_{24}) - V'_1 R_{24}}$$

where, V1, and V2 are the normal mode output voltages, Vo1 and Vo2; an V'1 and V'2 are the desired control loop values for Vo1 and Vo2 in standby (45.8% of their normal mode values). This value is set since the Fairchild Power Switch (FPS) regulates its Vcc voltage to 11V in standby mode and Vcc is normally set to 24V in normal mode.

4.1.Transformer turns ratio

If Vo2 drops to V'2, before Vcc drops to 11V in standby mode, the error amp starts to feed back. If V'2 is too low, the MCU could be reset. Therefore, select V'2 such that the linear regulator (7805) can properly maintain the output. This means the turns ratio should be selected such that (11 / Vcc) > (V'2 / V2). In other words, the transformer should be designed so that Vo2 is maintained slightly higher than V'2. This allows the error amp output to saturate low, permitting the primary side Vfb to remain at ground level.

5. Fairchild Power Switch Sync Pin Circuitry Design

In quasi resonant operation, the voltage level at the Fairchild Power Switch (FPS) Sync pin (pin 5) determines when the MOSFET turns on. This should be when Vds is lowest.

Figure 6 shows the reference voltages, Vrh and Vrf for both normal and burst mode operation. They are used to detect the time required for the voltage across the MOSFET to reach its minimum. The MOSFET turns on when the Sync pin voltage becomes lower than Vrf.

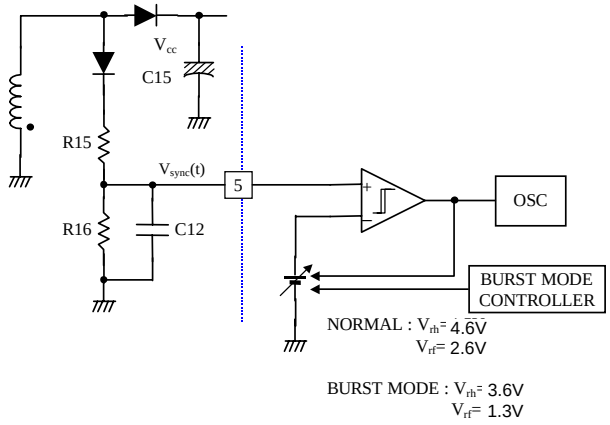


Figure 6. Reference voltages for normal and burst mode operation, V_{rh} and V_{rf}.

Figure 7 shows the waveform of Vsync in normal mode. The peak value of Vsync(t), when divided by R15 and R16 must be greater than the threshold voltage of the sync pin. In normal mode the threshold voltage is 4.6 V, and in standby mode it is 3.6V. Vsync(t) is the voltage across C15. It increases to Vc, which is the maximum voltage of Vsync(t) determined by the auxiliary winding voltage and the ratio of R15 and R16, after the MOSFET turns off. When the transformer current drops to zero, it drops exponentially as shown in Figure 7.

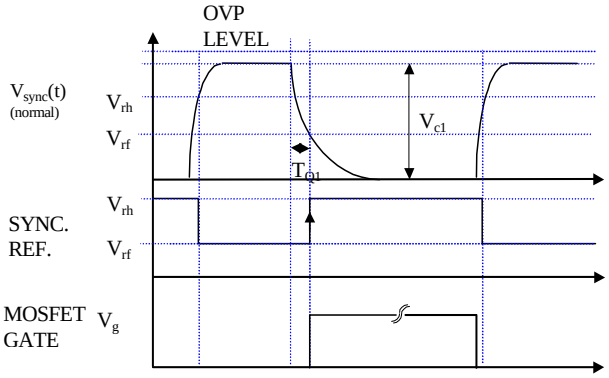


Figure 7. Normal mode waveforms for $V_{sync(t)}$.

The time t_Q that it takes for Vsync(t) to drop from Vc to Vrf , is calculated as follows:

$$t_Q = \tau 1n\left(1 - \frac{V_{rf}}{V_c}\right)^{-1}$$

$$where\ \tau = R_{16}C_{12} \qquad V_c = \frac{R_{16}}{R_{15} + R_{16}}V_{cc}$$

When t_{Q1} as calculated from Vc1 and Vrf1 equals t_{Q2} as calculated from Vc2 and Vrf2, the following relationship can be derived:

$$\frac{V_{rf1}}{V_{C1}} = \frac{V_{rf2}}{V_{C2}}$$

Therefore, $t_{Q1} = t_{Q2}$ and are independent of t, and t_Q will not change so long as the ratio of Vc to Vrf is constant. When the transformer flyback current becomes zero, Vds starts to decrease. The time required for the voltage across the MOSFET to drop to its minimum value is:

$$t_R = \pi\sqrt{L_m C_r}$$

The equation shows that the time required to drop to minimum voltage is a function of the primary inductance, Lm, and capacitance, C_r, across the MOSFET. This means that t_R is independent of changes in input and output voltage and does not change once the circuit is set.

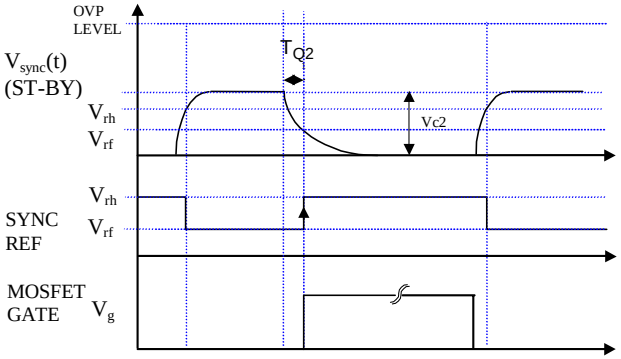


Figure 8. Stand by mode V_{sync} waveform.

The output voltage in standby drops to 45-50% of its value in normal mode, and so does Vc. Therefore, to guarantee quasi resonant operation in standby mode, t_Q must equal t_R, regardless of the mode. To achieve this, the reference in the Fairchild Power Switch (FPS)'s Sync pin comparator changes with the mode.

6. Protection

6.1 Over voltage protection

Refer to Figure 8. A problem in the feedback loop can be indicated either when switching shuts down or the output voltage is continuing to increase because it is not regulated. In response to increasing output voltage, a KA5Q-series Fairchild Power Switch (FPS) enters latch mode when the sync pin voltage reaches 12V (typ.) The Fairchild Power Switch (FPS) stops, and all output voltages start to drop. When Vcc reaches 9V, the Fairchild Power Switch (FPS) unlatches and restarts and Vcc again increases. Switching restarts when Vcc reaches 15V. This operation is called auto restart. Be careful of the rising slope of Vsync(t). Its time constant is C12x(R15//R16). If the time constant is too short, the waveform can oscillate causing an over voltage protection (OVP) malfunction. If Vc, the peak value of Vsync(t) approaches the OVP level (12V, typ.) and there are problems in the feedback loop. Output voltage overshoot is reduced but care must be taken so that the OVP does not malfunction due to a slight overshoot, etc. in the output voltage. If Vc is set too low, the Fairchild Power Switch (FPS)'s Primary Side Regulation (PSR) block can start before OVP and regulate Vcc. In that case operation continues, but with an abnormally increased output voltage.

6.2 Thermal shutdown

If the ambient temperature is high, or the temperature inside the device becomes too high due to abnormal operation, the junction temperature of the device can become too high. If it exceeds 150°C, the Fairchild Power Switch (FPS) enters latch mode and stops.

6.3 Over current latch

A short circuit in a secondary side rectifier diode or on a transformer pin is equivalent to a leakage inductor of several mH connected to the input bulk capacitor. A large current spike can flow through the MOSFET in the Fairchild Power Switch (FPS), and the MOSFET will be destroyed if the current is not turned off within a few hundred nanoseconds. Although ICs with current mode control generally have over current protection, it may not execute properly due to delays in the IC's internal blocks. Hence, besides using pulse by pulse over current protection to turn off the MOSFET, the Fairchild Power Switch (FPS) also uses an over current latch. This allows the Fairchild Power Switch (FPS) to turn off the MOSFET within 200 ns if the current flow is higher than the over current protection level threshold. The Fairchild Power Switch (FPS) also operates in latch mode to reduce stress on the MOSFET that would result from repeated auto restarts. Once the Fairchild Power Switch (FPS) enters latch mode, the input ac power is cut off. The Fairchild Power Switch (FPS) will unlatch and restart only when Vcc drops below 5V.

6.4 Over load protection (OLP)

Refer to Figure 9, next page. The feedback loop causes the voltage Vfb, on the Fairchild Power Switch (FPS) feedback pin to increase when the output current increases. In the case of a persistent overload condition, Vfb continues to increase because 5mA current source in the Fairchild Power Switch (FPS) charges the compensation capacitor attached to the FB pin. If this voltage reaches 7.5V, the MOSFET stops switching. The delay between Vfb reaching the over current protection level and when the MOSFET stops switching is calculated as follows:

$$t_{delay} = \frac{(7.5 - 3) \cdot C_{13}}{5 \times 10^{-6}} [sec]$$

Auto restart begins after overload protection triggers.

7. PCB Layout

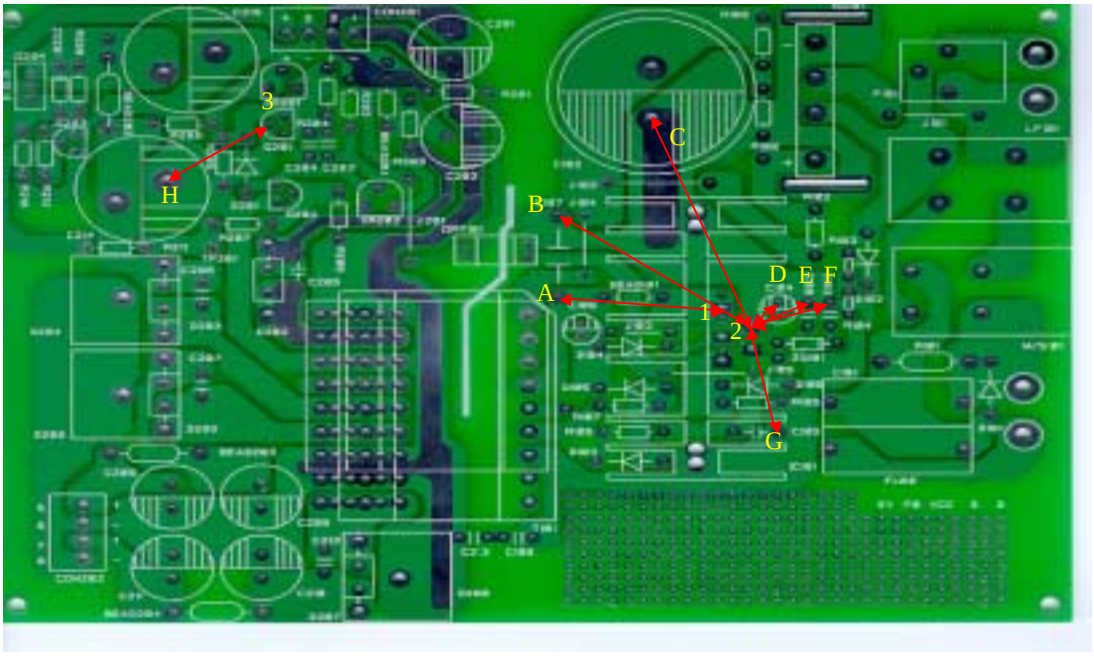


Figure 9.

A proper PCB layout not only reduces the set EMI, but also minimizes the noises that can produce device malfunction. Cautionary items when designing the PCB layout of the 5Q-series are as follows:

- The space between 2 pin in the 5Q-series and the bulk capacitor (DC link capacitor) - (Ground) terminal should be simple and close as possible. A thick pattern should be used.
  (C↔2 in the fig9, very important)
- PCB pattern should be made such that $C_{r\ is}$ as close as possible to pin 1,2. If not, pulse like current flow path becomes longer every time the switch turns on, worsening the noise.
  (A↔1, B↔2 in the fig9, very important)
- The distance between 2 pin in the 5Q-series and the negative terminal of Vcc capacitor should be close as possible.
  (D↔2 in the fig9, very important)
- The distance between 2 pin in 5Q-series and the negative terminal of Vcc capacitor should be close as possible.
  (E↔2 in the fig9,important)
- The distance between 2pin in the 5Q-series and the negative terminal of Vfb capacitor should be close as possible.
  (F↔2 in the fig9,important)
- The feedback loop PCB pattern should be simple and not be placed close to a comparatively high current flow connection or device. The connection between the ground of output which is regulated and the ground of secondary error Amp. is simple and close as possible.
  (H↔3 in the fig9, very important)
- when the primary side control is used, the transformer Vcc (pin 3) winding must be made so as to result in the best coupling coefficient between it and the most important winding.

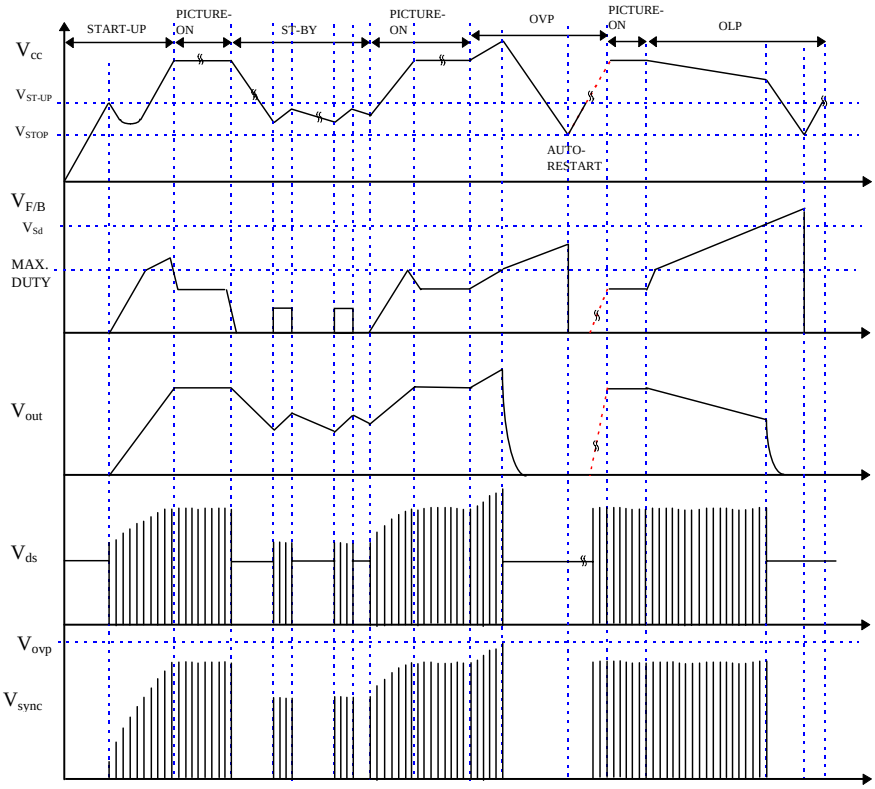
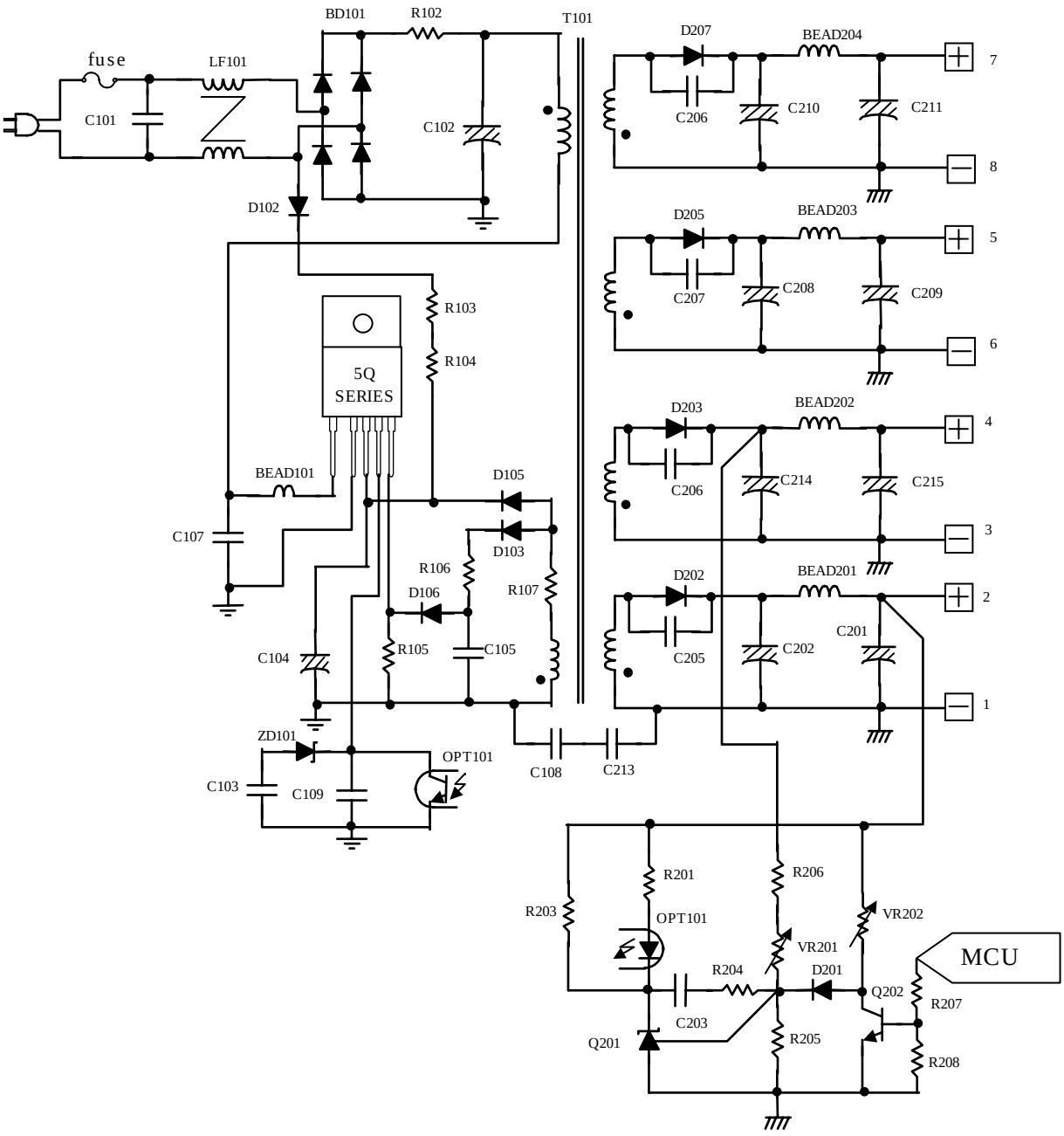


Figure 10. Operation Waveform.

8. KA5Q Fairchild Power Switch Based SMPS for a Color TV

8.1 Secondary Side Regulation.



8.2 Primary Side Regulation

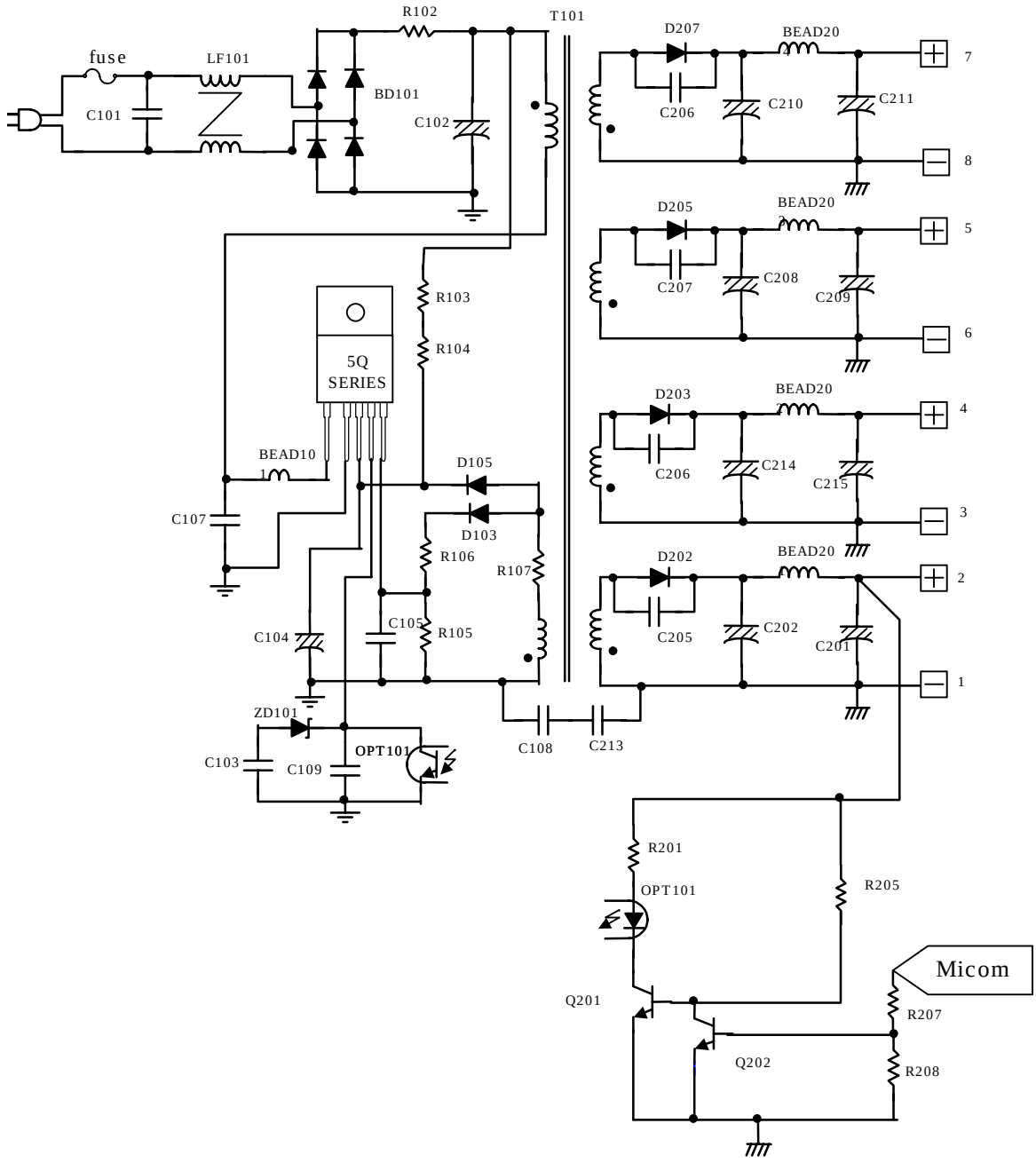


Table 1. Parts List for KA5Q based SMPS

Part #	Value	Rating	Note	Part #	Value	Rating	Note
[Resister]				C104	47μF	50V	electrolytic
R101	open	1/2W	-	C105	3.9nF	50V	film
R102	NTC	4.7Ω	-	C106	open	50V	electrolytic
R103	68kΩ	1/2W	-	C107	2.2nF	1000V	film
R104	68kΩ	1/2W	-	C108	560pF	2000V	film
R105	470Ω	1/4W	-	C109	47nF	50V	film
R106	600Ω	1/4W	-	C201	1000μF	50V	electrolytic
R107	10Ω	1/4W	-	C202	1000μF	50V	electrolytic
R108	open	1/4W	-	C203	22nF	50V	film
R109	open	1/4W	-	C204	open	50V	film
R201	1kΩ	1/4W	-	C205	470pF	1000V	film
R202	short	fuse	-	C206	470pF	1000V	film
R203	1kΩ	1/4W	-	C207	470pF	1000V	film
R204	40kΩ	1/4W	-	C208	1000μF	50V	electrolytic
R205	4.7kΩ	1/4W	-	C209	1000μF	50V	electrolytic
R206	220kΩ	1/4W	-	C210	1000μF	50V	electrolytic
R207	5kΩ	1/4W	-	C211	1000μF	50V	electrolytic
R208	5kΩ	1/4W	-	C212	470pF	1000V	film
VR201	30kΩ	box	-	C213	560pF	2000V	film
VR202	20 kΩ	box	-	C214	100μF (100W)	200V	electrolytic
[Diodes]				-	220μF (150W)	200V	electrolytic
D101	open	ZNR	-	-	330μF (200W)	200V	electrolytic
D102	1N4004	400V, 1A	-	-	330μF (270W)	200V	electrolytic
D103	1N4937	600V, 1A	-	C215	47μF (100W)	200V	electrolytic
D104	short	600V, 1A	-	-	100μF (150W)	200V	electrolytic
D105	1N4937	600 V, 1A	-	-	220μF (200W)	200V	electrolytic
D106	1N4148	75V, 0.15A	-	-	220μF (270W)	200V	electrolytic
D201	1N4148	75V, 0.15A	-	-	-	-	-
D202	D06U20S(100W)	200V, 6A	TO-220F	-	-	-	-
	D06U20S(150W)	200V, 6A	TO-220F	-	-	-	-
	D06U20S(200W)	200V, 10A	TO-220F	-	-	-	-

Table 1. Parts List for KA5Q based SMPS (continued)

Part #	Value	Rating	Note	Part #	Value	Rating	Note
[Diodes]				**[Beads]**			
D202	D06U20S(270W)	200V,20A	TO-220F	BEAD101	ferrite bead	-	-
D203	D10U60S	600V,10A	TO-220F	BEAD201	ferrite bead	-	-
	D20U60S(270W)	600V,20A	TO-220F	BEAD202	100 μH	5A	-
	open	-	-	BEAD203	ferrite bead	-	-
	D06U20S	200V,10A	TO-220F	BEAD204	ferrite bead	-	-
	open	-	-	-	-	-	-
	D06U20S	200V,10A	TO-220F	-	-	-	-
	open	-	-	-	-	-	-
[Zener]				**[Others]**			
ZD101	4.7V	0.5W	-	OPT101	H11A817A	-	Fairchild
	-	-	-	T101	EER3542	KA5Q0765RT	-
				-	EER4042	KA5Q12656RT	-
C101	220nF	275V	box	-	EER4942	KA5Q1265RT	-
C102	220μF (100W)	400V	electrolytic	-	EER5354	KA5Q1565RT	-
	330μF (150W)	400V	electrolytic	CON201	PWR CONN.	-	-
	470μF (200W)	400V	electrolytic	CON202	PWR CONN.	-	-
	560μF (270W)	400V	electrolytic	Q201	KA431LZ	-	-
C103	100nF	50V	film	Q202	C945	npn (E.B.C)	-

9. Example Transformer Design for Color TV SMPS

9.1 Define system specifications:

Output power, Po = 80W (125V,0.56A for B+ and 13V,0.76A)

$P_{B-OUT} = 70W, P_{13V-OUT} = 10W$

Input voltage, 85 to 265 V., (universal input), 60Hz
Efficiency $\eta \geq 80\%$
Core = EER3542 (Ae = 108mm2)

9.2. Calculate minimum dc input voltage, V_{inmin}:

The table below shows typical values of Vinmin, Lm, Fsmin for various Pin values. The maximum power input is

$$Pin\_max = \frac{Po}{efficiency} = \frac{80W}{0.8} = 100W$$

For 100W Pin_max, there are two option for capacitor value; 220uF or 330uF. Here, select the 220uF.
Then, 93V is the minimum dc input voltage.

Pin (W)	Cin [uF]	Vin_min [V]	Lm [uH]	Fs_min [kHz]
80	220	98	700 675 650	26.1 27.0 27.9
	330	105	700 675 650	28.0 29.0 30.0
100	220	93	600 575 550	23.6 24.5 25.6
	330	102	600 575 550	25.9 27.0 28.1
130	330	96	500 475 450	23.3 24.4 25.7
	470	103	500 475 450	25.0 26.3 27.6
150	330	93	400 375 350	26.6 28.2 30.0
	470	101	400 375 350	26.6 28.2 30.0
180	470	97	350 325 300	24.7 26.5 28.5
	560	101	350 325 300	25.7 27.5 29.6
200	470	94	325 300 275	23.4 25.3 27.4
	560	98	325 300 275	24.5 26.4 28.7

Pin (W)	Cin [uF]	Vin_min [V]	Lm [uH]	Fs_min [kHz]
240	560	94	275 250 225	23.3 25.5 28.1
	680	99	275 250 225	24.5 26.8 24.5
270	560	91	250 200	22.0 24.3
	680	96	250 200	23.4 25.9

However, because of voltage drops from the line filter, bridge diode, and NTC (negative thermal coefficient), set Vinmin to 100V to allow for a design margin and convenient calculation.

9.3 Determine turns ratio, $n = N_p/N_S$:

Turns ratio is a factor in determining Dmax, device operating voltage, and device and transformer dissipation.

$$n = \frac{650V + -\sqrt{2}V_{(acmax)} - 120}{V_o}$$

$$n = \frac{650 - \sqrt{2} \times 265 - 120}{125}$$

$$= 1.25$$

where Vo is the output voltage used for B+ (125V) and 120V is the margin voltage. It can be determined by the designer, or the transformer, etc.

9.4 Calculate maximum duty, Dmax:

$$D_{max} = \frac{V_o}{V_{inmin} + nV_o}$$

$$D_{max} = \frac{1.25 \times 125}{93 + 1.25 \times 125} = 0.62$$

9.5 Calculate transformer inductance, Lm:

Fs, is the minimum operating frequency at the

condition of maximum load and minimum input voltage. Therefore Fs, should be set around 25-40kHz. Vinmin

condition is calculated as above at operating frequency of any load. From the operating frequency, it is possible to

estimate the device and transformer dissipation. Using Fs = 30kHz we calculate Lm. Fs should be corrected to 30×10^3 in the equation below.

Following this there should be some explanation of the core gap calculation to give the correct flux density.

$$L_m = \frac{V_{in}^2 \times D_{max}^2}{2P_{in}f_s}$$

$$L_m = \frac{93^2 \times 0.62^2}{2 \times 100 \times 30K} = 554\mu H$$

Estimated gap length (l_g) is

$$l_g = \frac{N_p^2 \mu_o A_e}{Lm} \times 10^3$$

$$= \frac{63^2 \times 4\pi \times 10^{-7} \times 108 \times 10^{-6}}{620 \times 10^{-6}} \times 10^3$$

$$= 0.868mm$$

Ae is the cross sectional area of the core

$\mu_o = 4\pi \times 10^{-7}$

9.6 Calculate minimum primary turns, N_{pmin}:

The primary turns count must be made larger than Npmin to prevent the transformer from saturating below the Fairchild Power Switch (FPS) Ipeak specification.

$$N_{pmin} = \frac{V_{inmin} D_{max}}{(dB)(Ae)(Fsmin)}$$

$$N_{pmin} = \frac{93 \times 0.62 \times 10^6}{0.3 \times 108 \times 30K} \approx 59T$$

where dB is the absolute amount of flux density variation in the core.

9.7 Calculate the maximum current, I_{peak},.

At full load and at minimum Vin, Ipeak must be lower than the Ipeak specification of the device to be used.

$$I_{peak} = \frac{V_{inmin} D_{max}}{L_m f_{smin}}$$

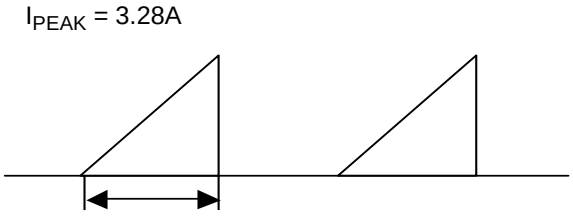
$$I_{peak} = \frac{93 \times 0.62}{554\mu H \times 30k} = 3.46A$$

9.8 Determine each output turns count:

- 125V output: N125V = Npmin./ n = 47turns
- Volts per turn: (125V + 1V) 50 turns = 2.68V / turn
- 13V output: (13V + 1V) / 2.68V / turn = 5.22 = 5turns
- Vcc winding: (24V + 1V) / 2.68V/turn = 9.32 = 9turns

9.9 Determine wire diameter

The copper coil's current capability is Idensity, 5A/mm . The rms current through primary Np is 1.479A in the example.



$$I_{rms} = I_{PEAK} \times \frac{1}{\sqrt{3}} \times \sqrt{D}$$

$$= 3.46A \times \frac{1}{\sqrt{3}} \times \sqrt{0.62}$$

$$= 1.577A$$

The wire diameter f of Np is 0.65mm.

$$Idensity;1mm^2 = Irms;\pi\left(\frac{\Phi}{2}\right)^2$$

$$5A;1mm^2 = 1.479A;\pi\left(\frac{\Phi}{2}\right)^2$$

$$\pi\left(\frac{\Phi}{2}\right)^2 = 0.295mm^2$$

$$\Phi \geq 0.613mm \Rightarrow 0.65mm$$

The rms current through secondary B+ is 1.246A in the example.

$$I_{B-rms} = \sqrt{\frac{P_{B-OUT} \times 2 \times (N_{pmin}/N_{125V})^2}{L_m \times f_{s-min}}} \times \frac{1}{\sqrt{3}} \times \sqrt{1-D}$$

$$= \sqrt{\frac{70W \times 2 \times 1.25^2}{554uH \times 30kHz}} \times \frac{1}{\sqrt{3}} \times \sqrt{0.38}$$

$$= 1.291A$$

The wire diameter f of B+ is 0.60mm.

$$5A;1mm^2 = 1.291A;\pi\left(\frac{\Phi}{2}\right)^2$$

$$\pi\left(\frac{\Phi}{2}\right)^2 = 0.258mm^2$$

$$\Phi = 0.573mm$$

Calculated as above, the wire diameter f of 13V bias winding is 1mm.

References

1. Transformer and Inductor Design Handbook. 2nd ed. Col. Wm. T. McLyman. Marcel Dekker, Inc., 1988.

2. Flyback converter design using Fairchild Power Switch. Application note AN4105. Fairchild Electronics, 2000.