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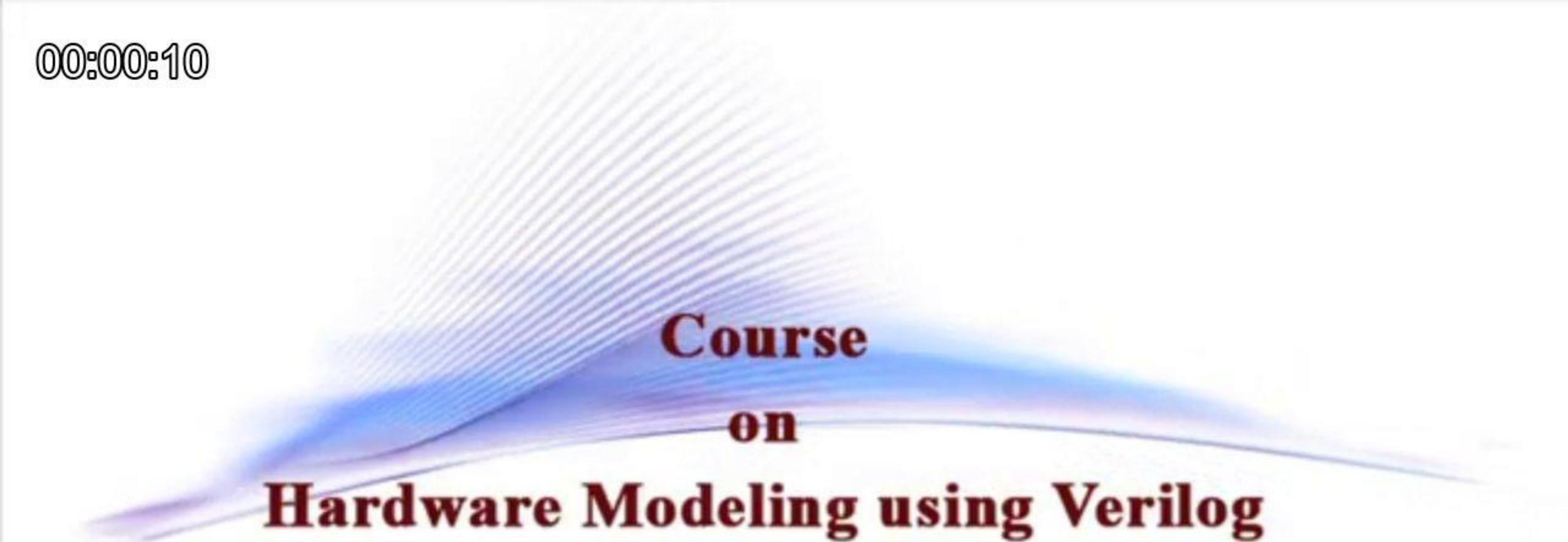


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00:00:08

**Course  
on  
Hardware Modeling using Verilog**

00:00:10



**Course  
on  
Hardware Modeling using Verilog**

00:00:12

by

**Prof. Indranil Sengupta**

Department of Computer Science and Engineering

Indian Institute of Technology Kharagpur

00:00:14

# **Lecture 04**

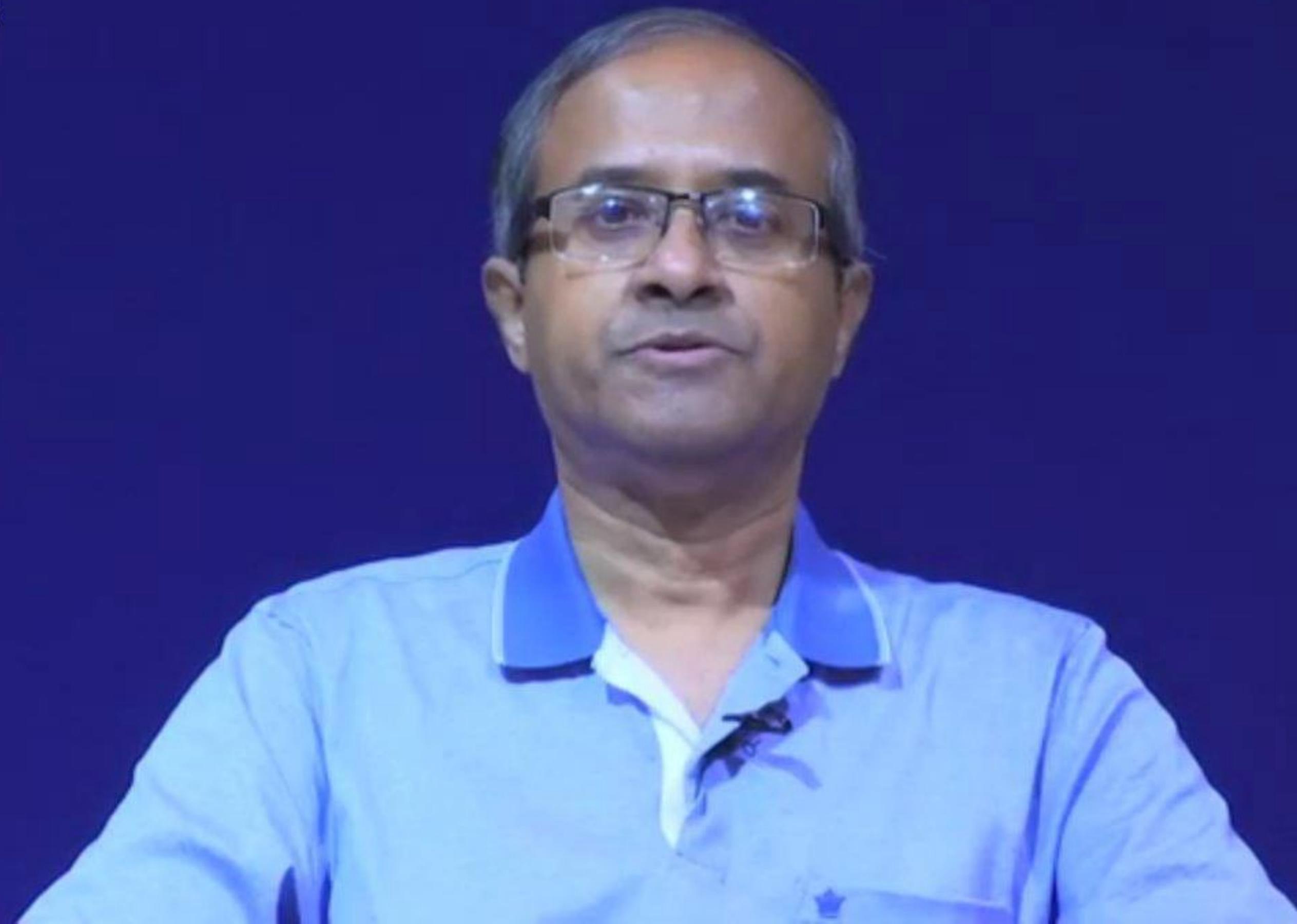
# **VLSI Design Styles ( Part 1 )**

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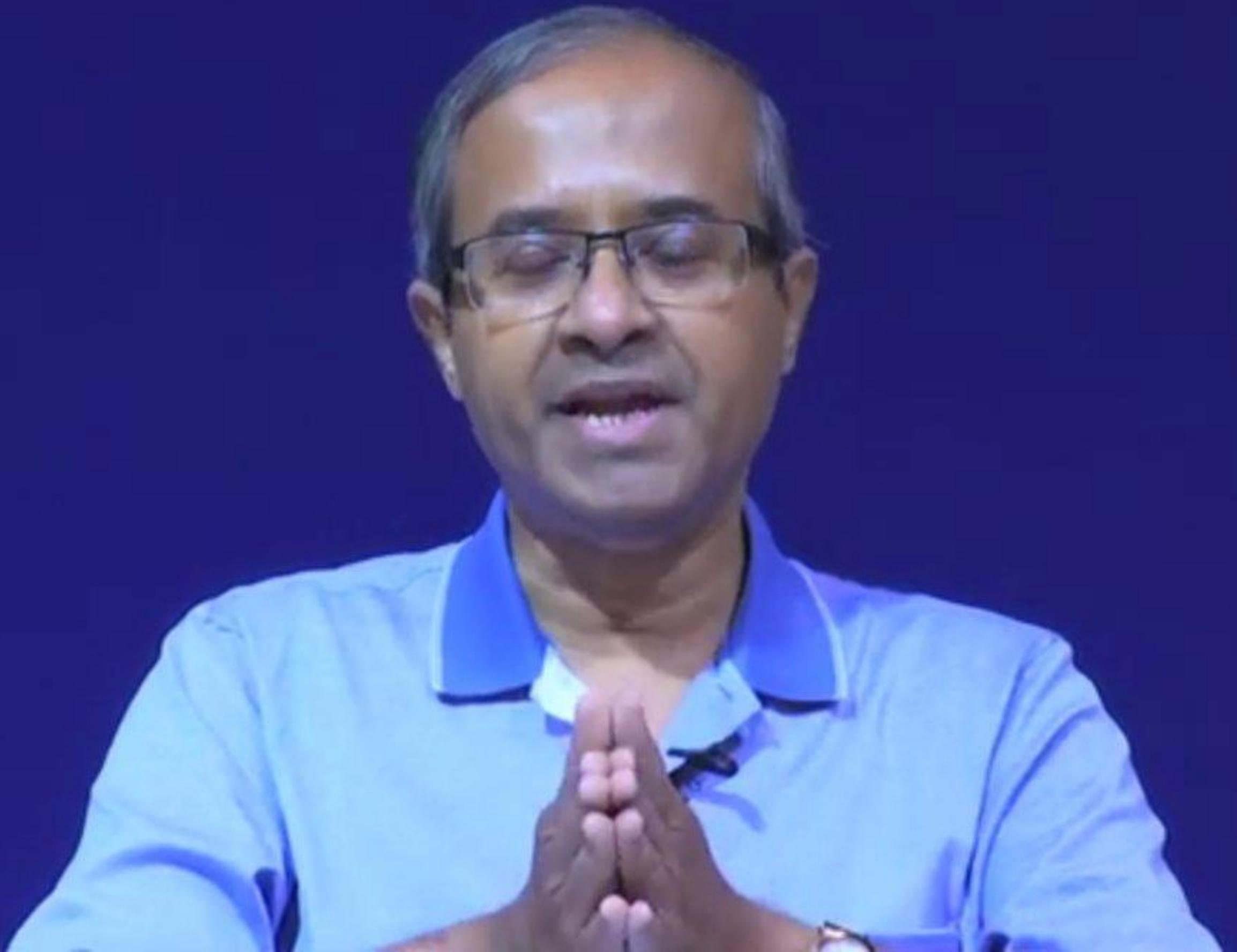
# Lecture 04

# VLSI Design Styles ( Part 1 )

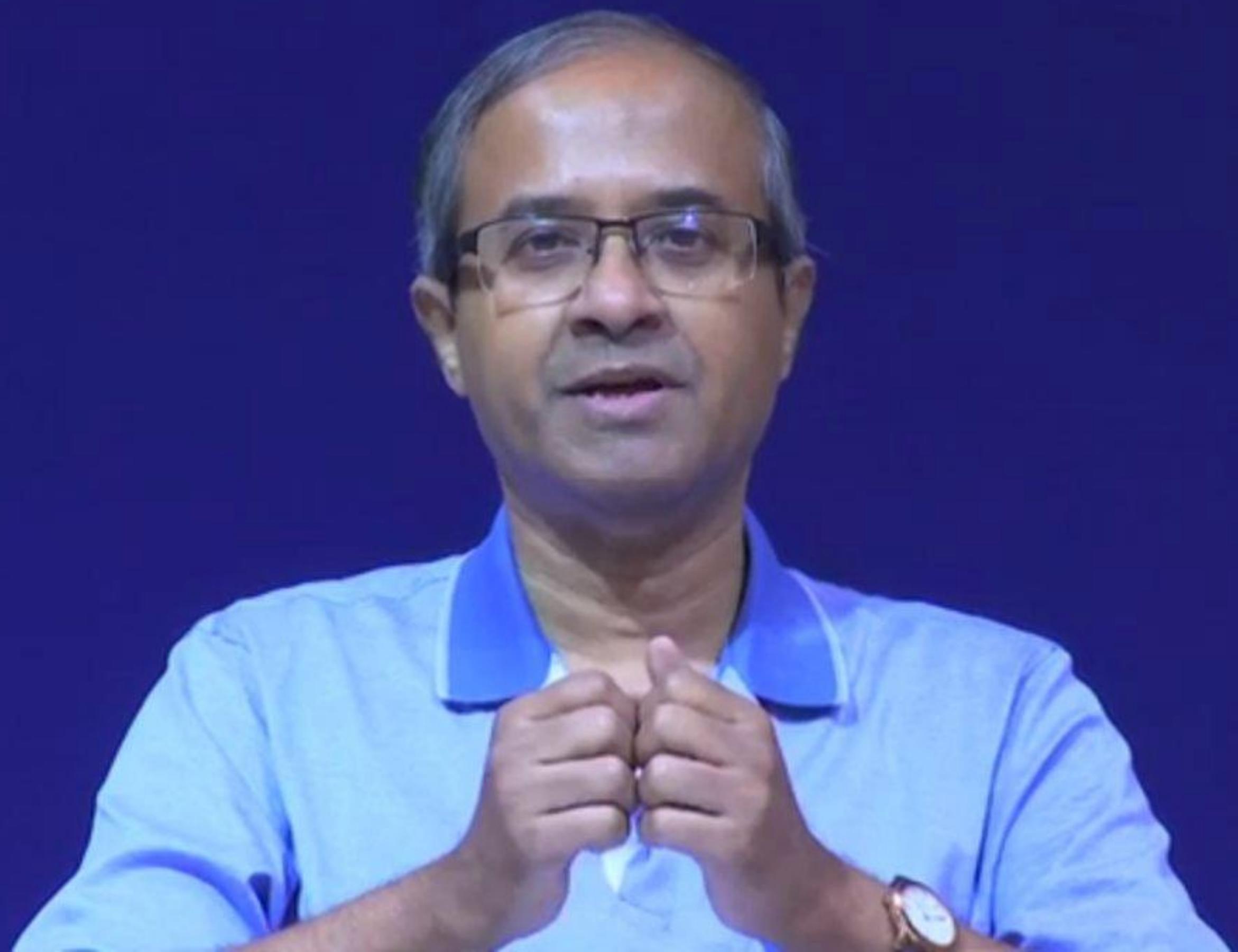
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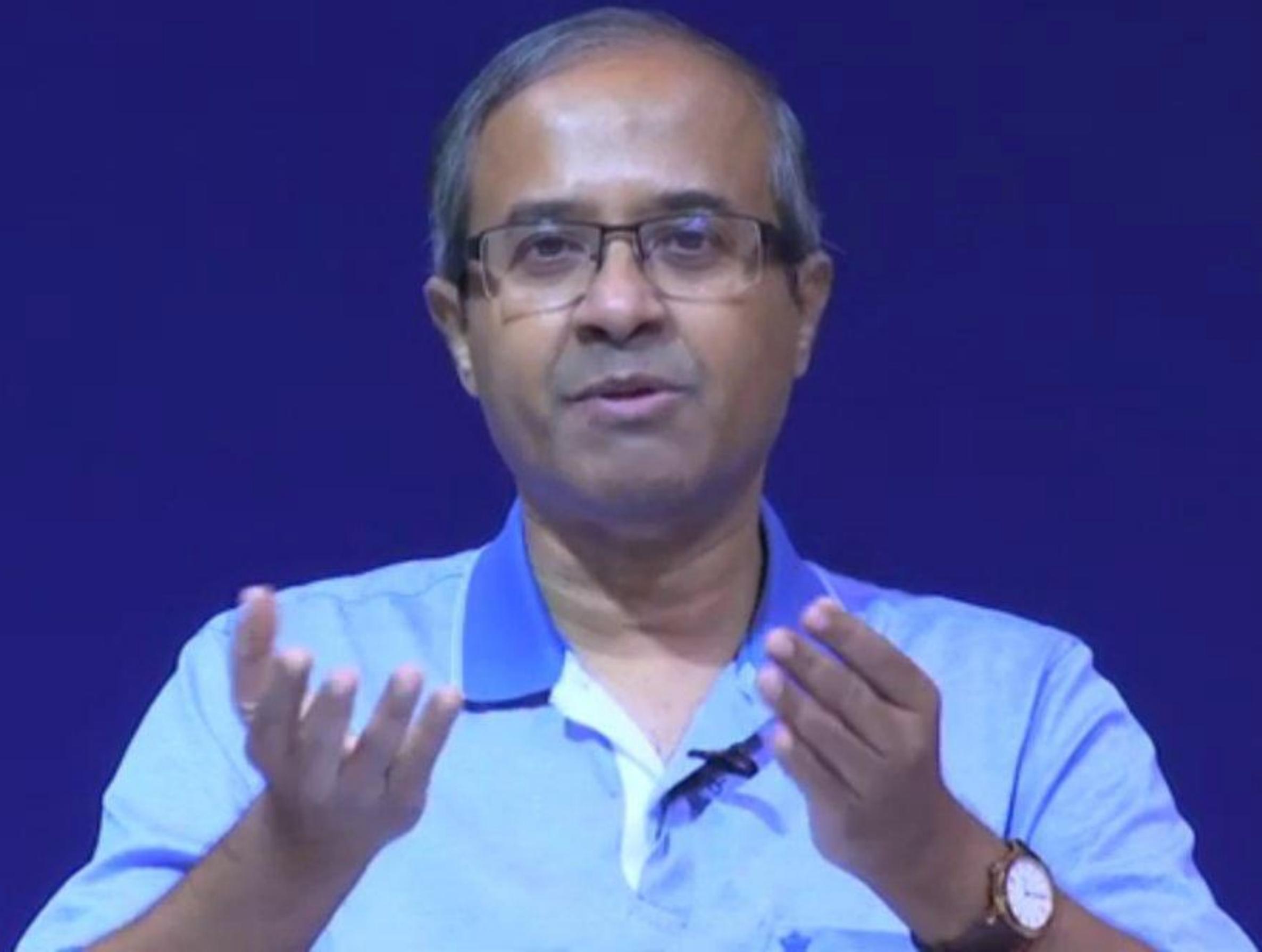
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## Lecture 04: VLSI DESIGN STYLES (PART 1)

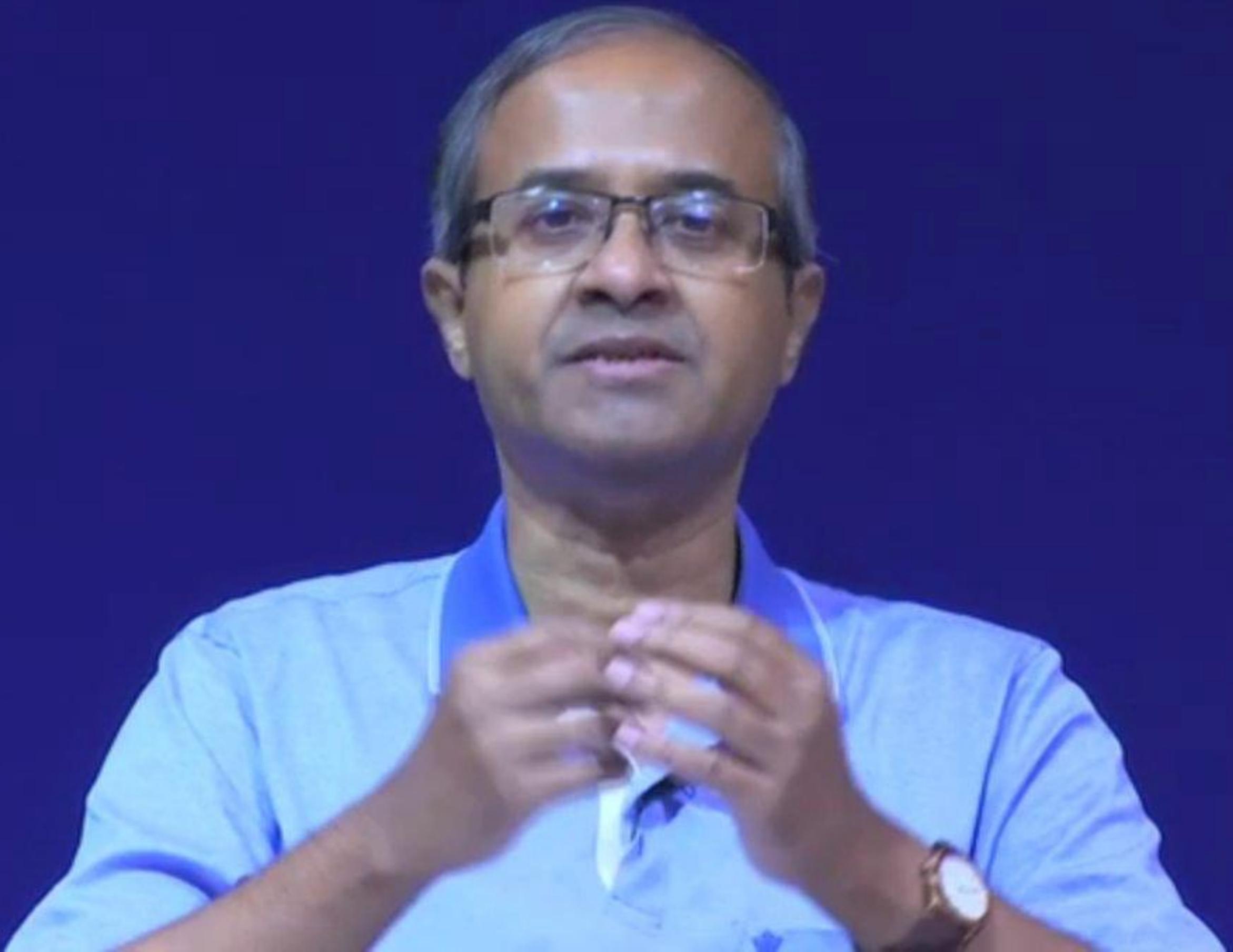
PROF. INDRANIL SENGUPTA

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

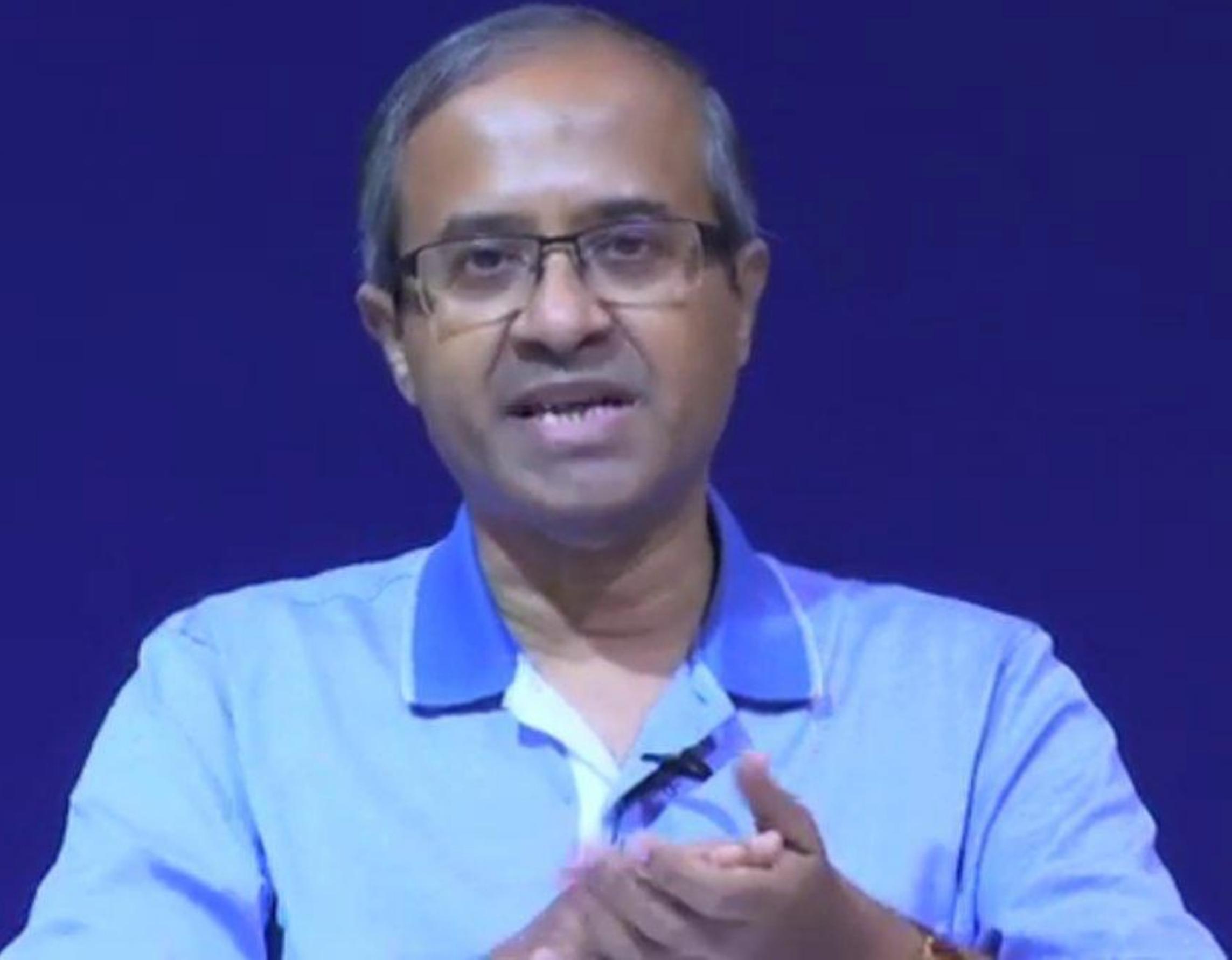
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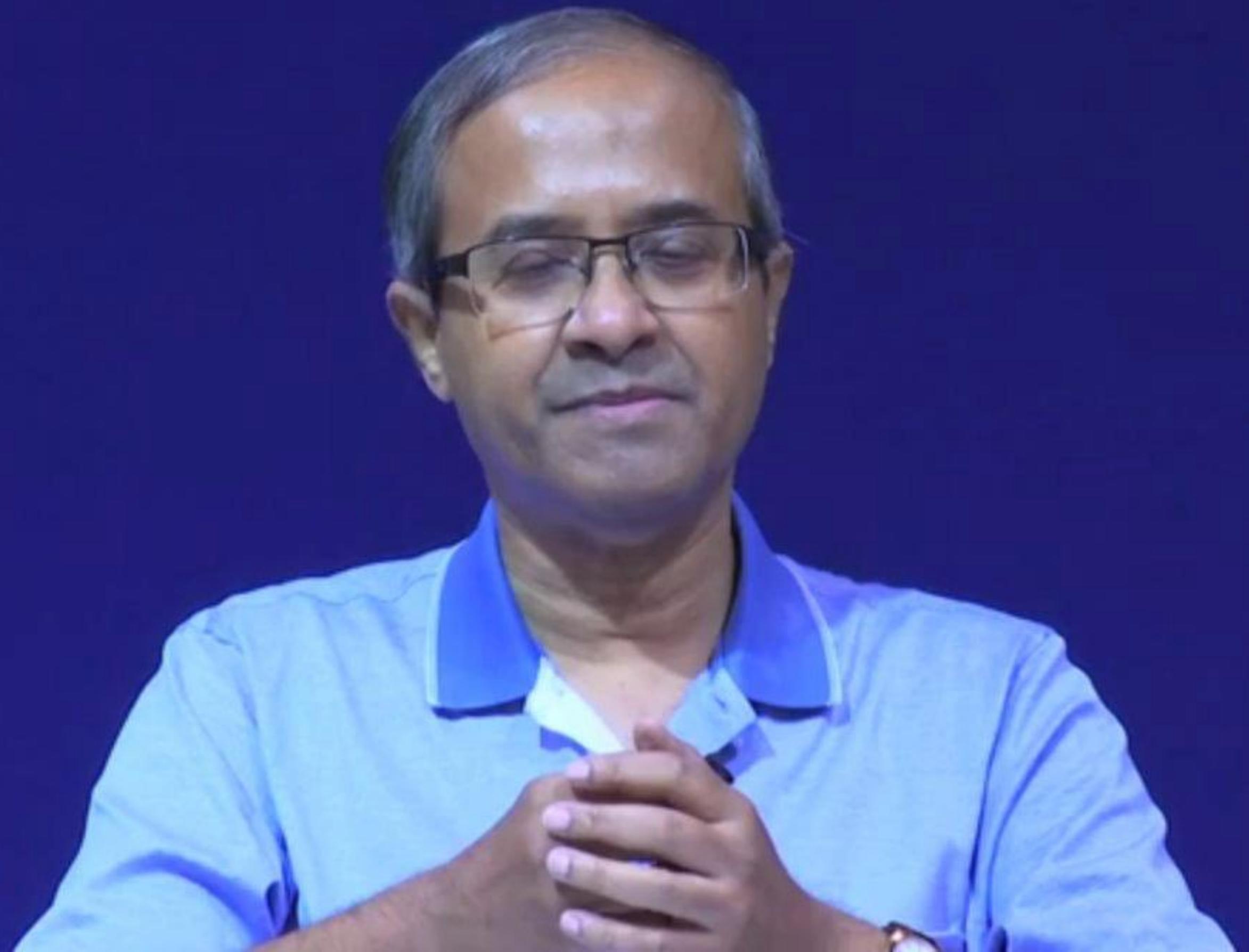
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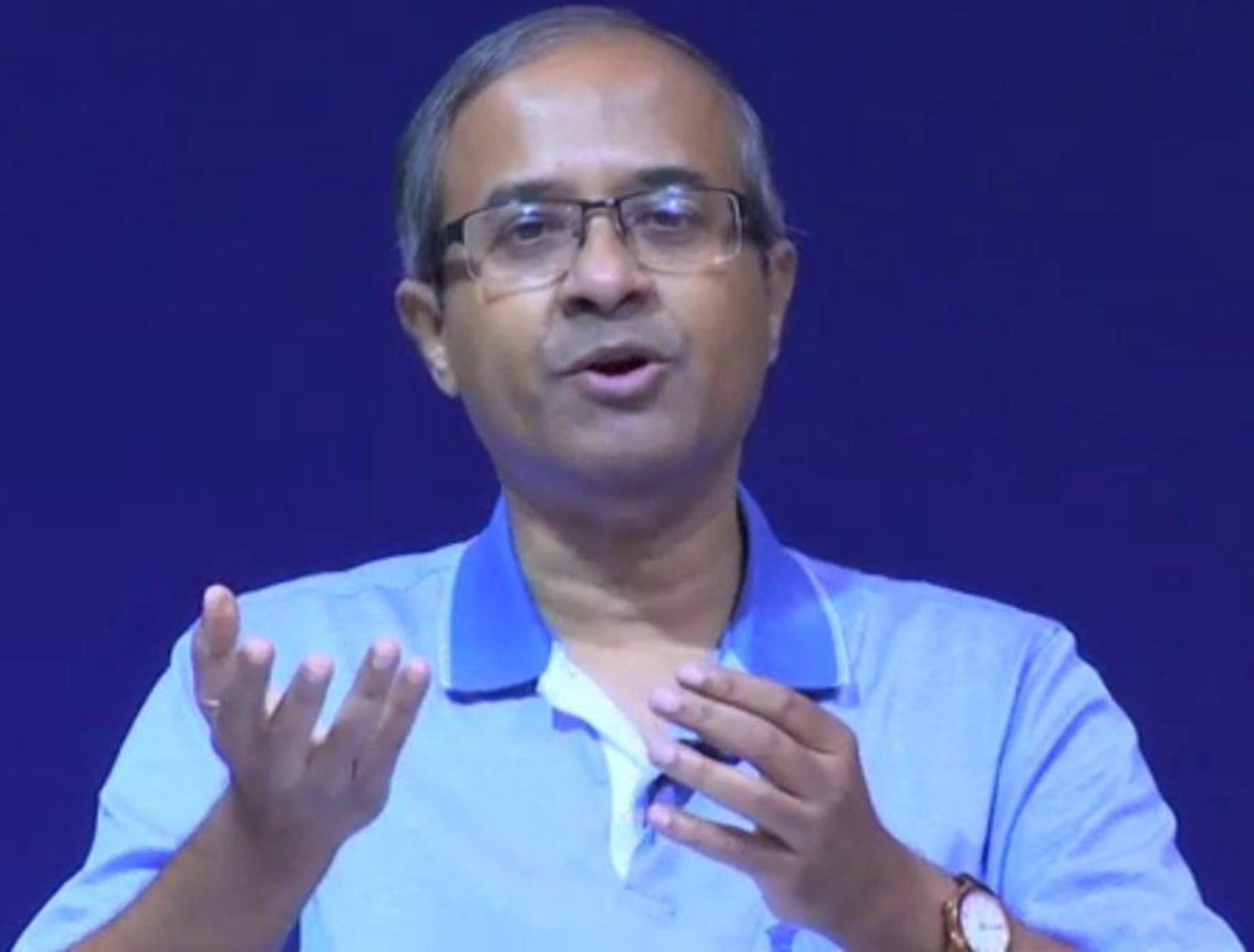
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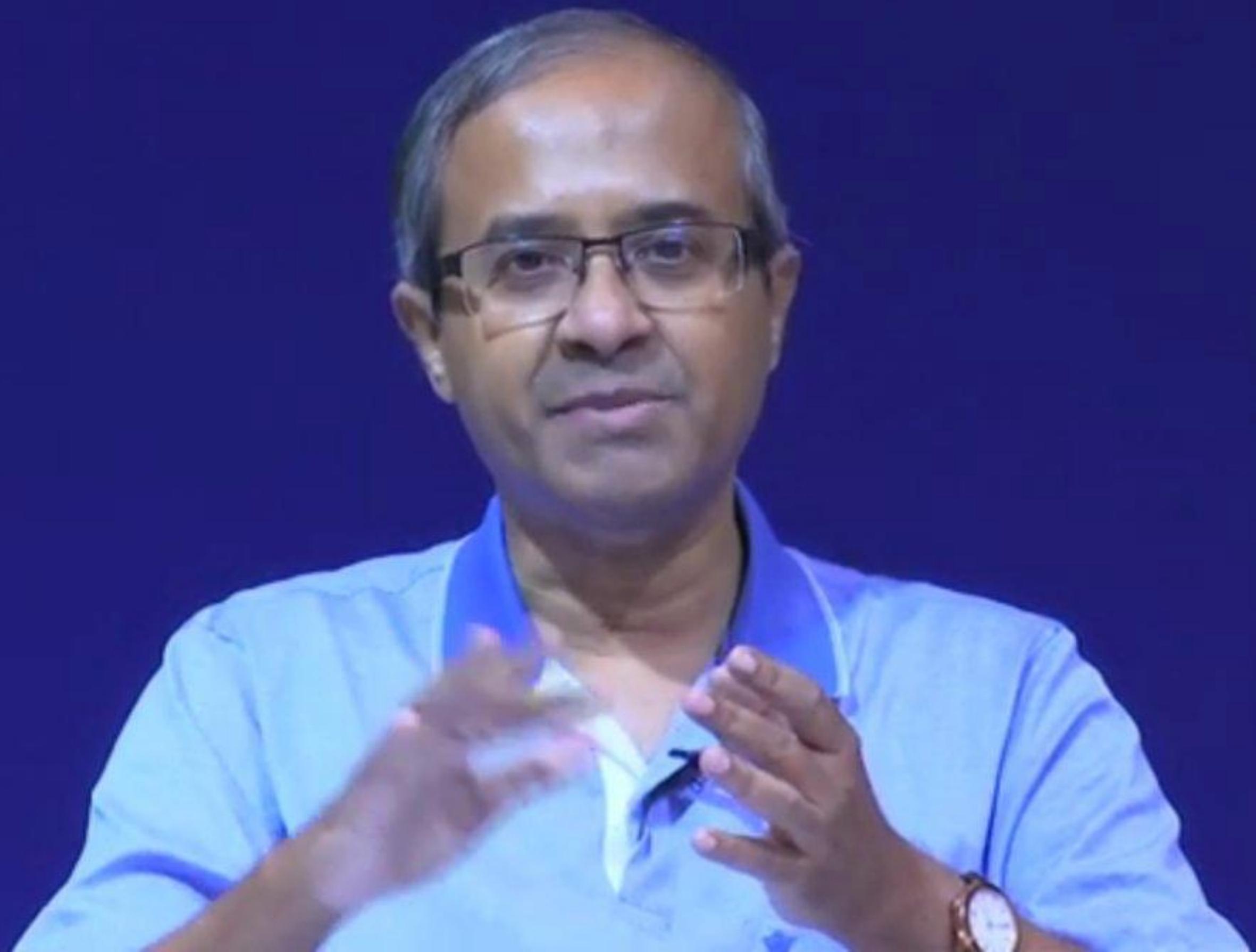
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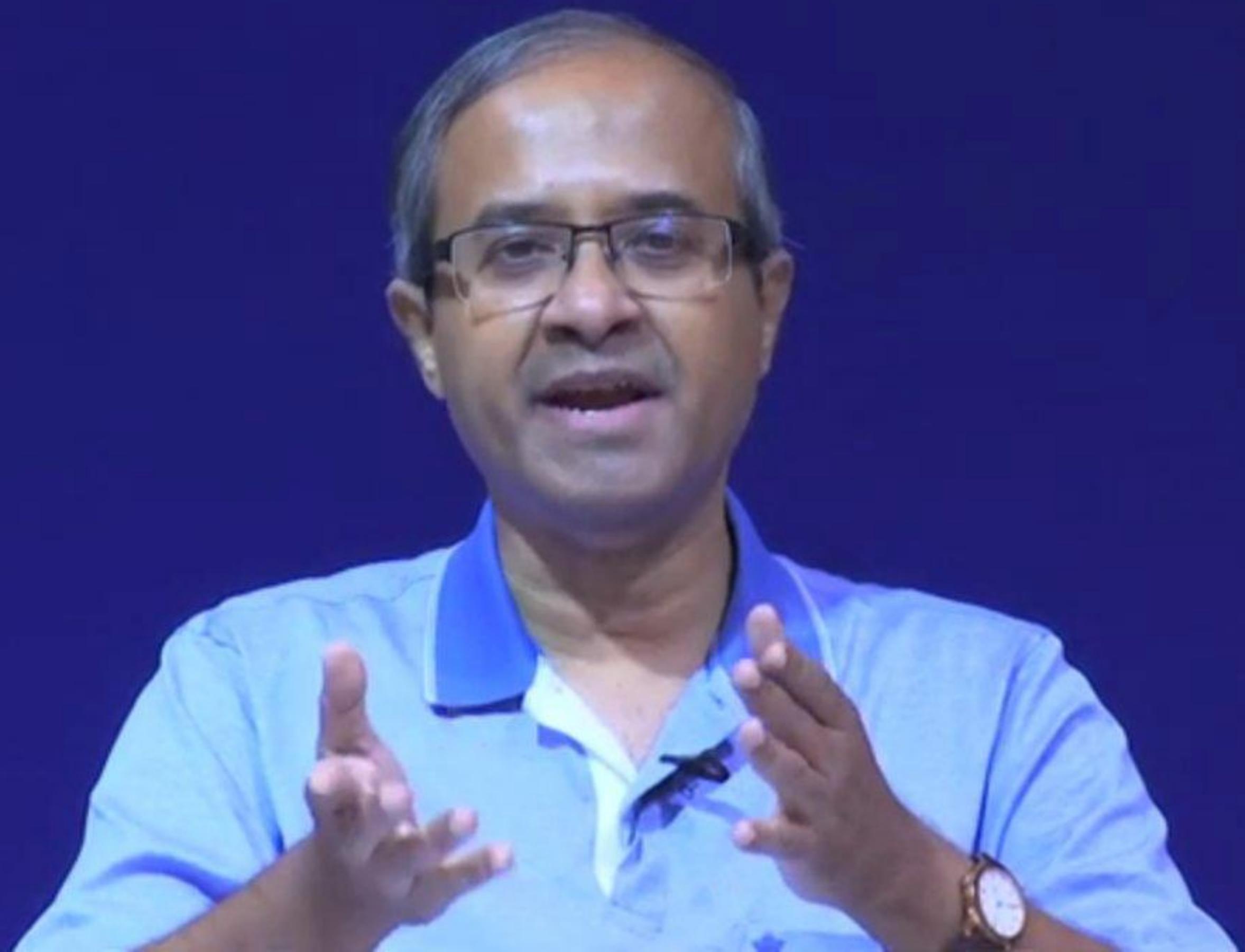
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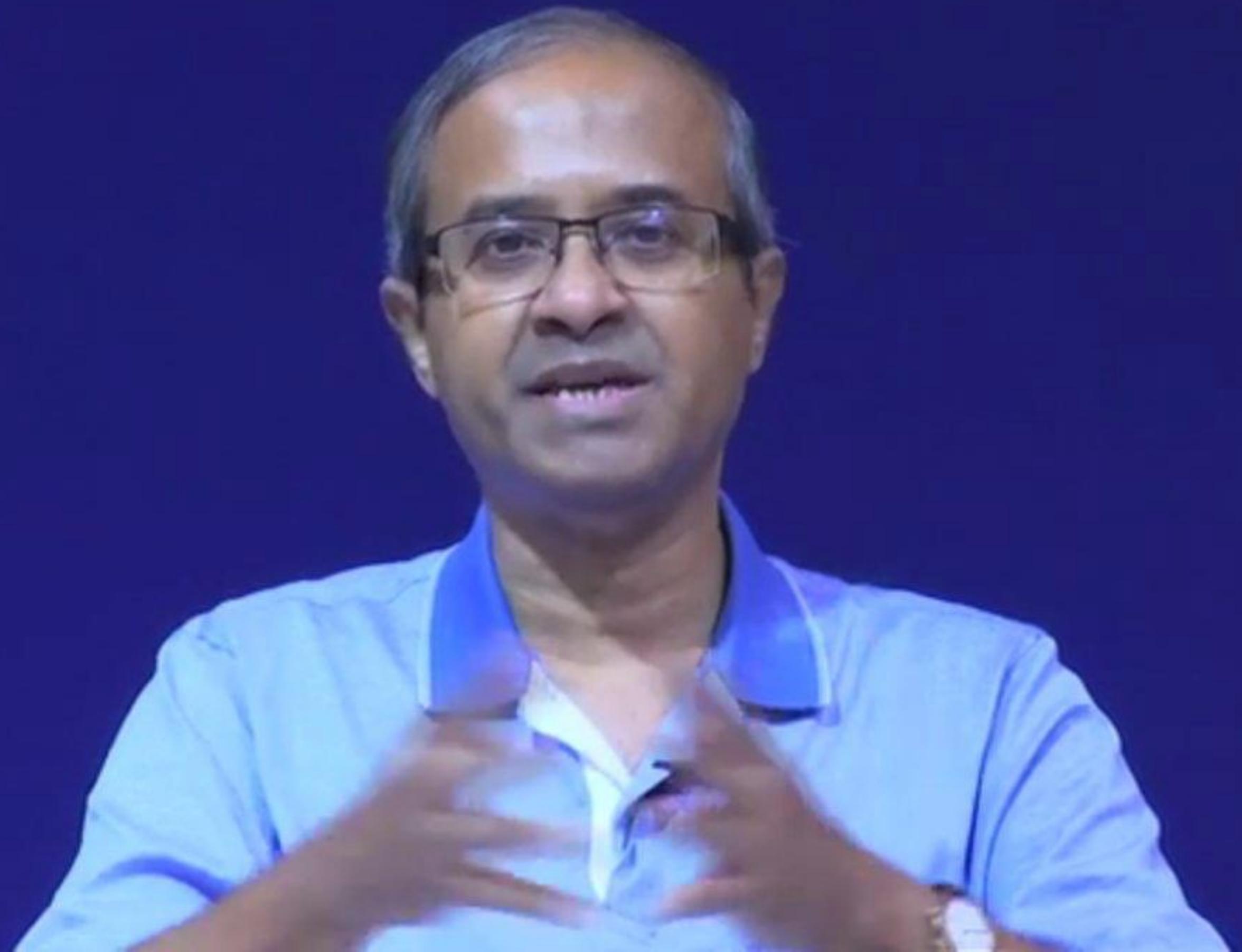
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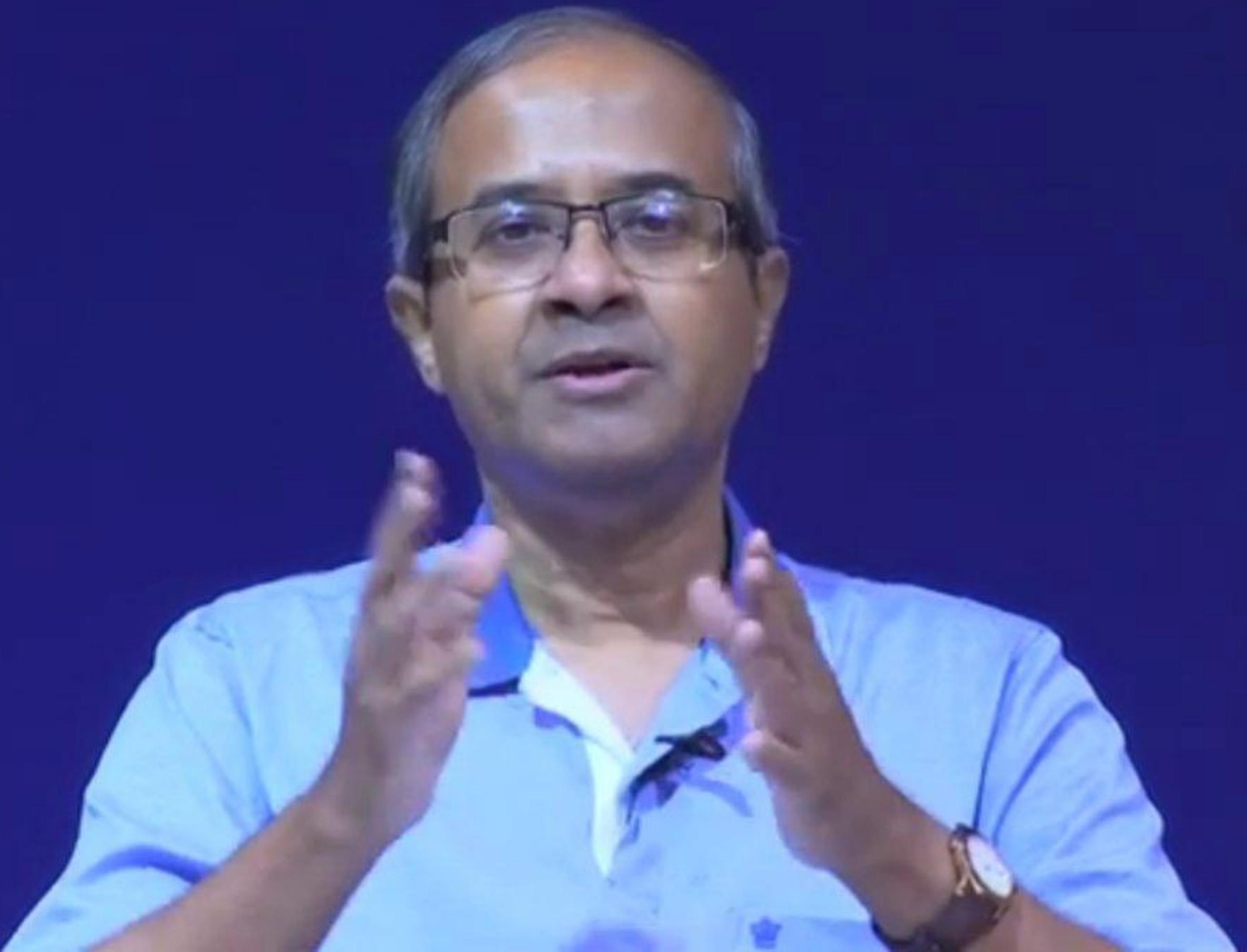
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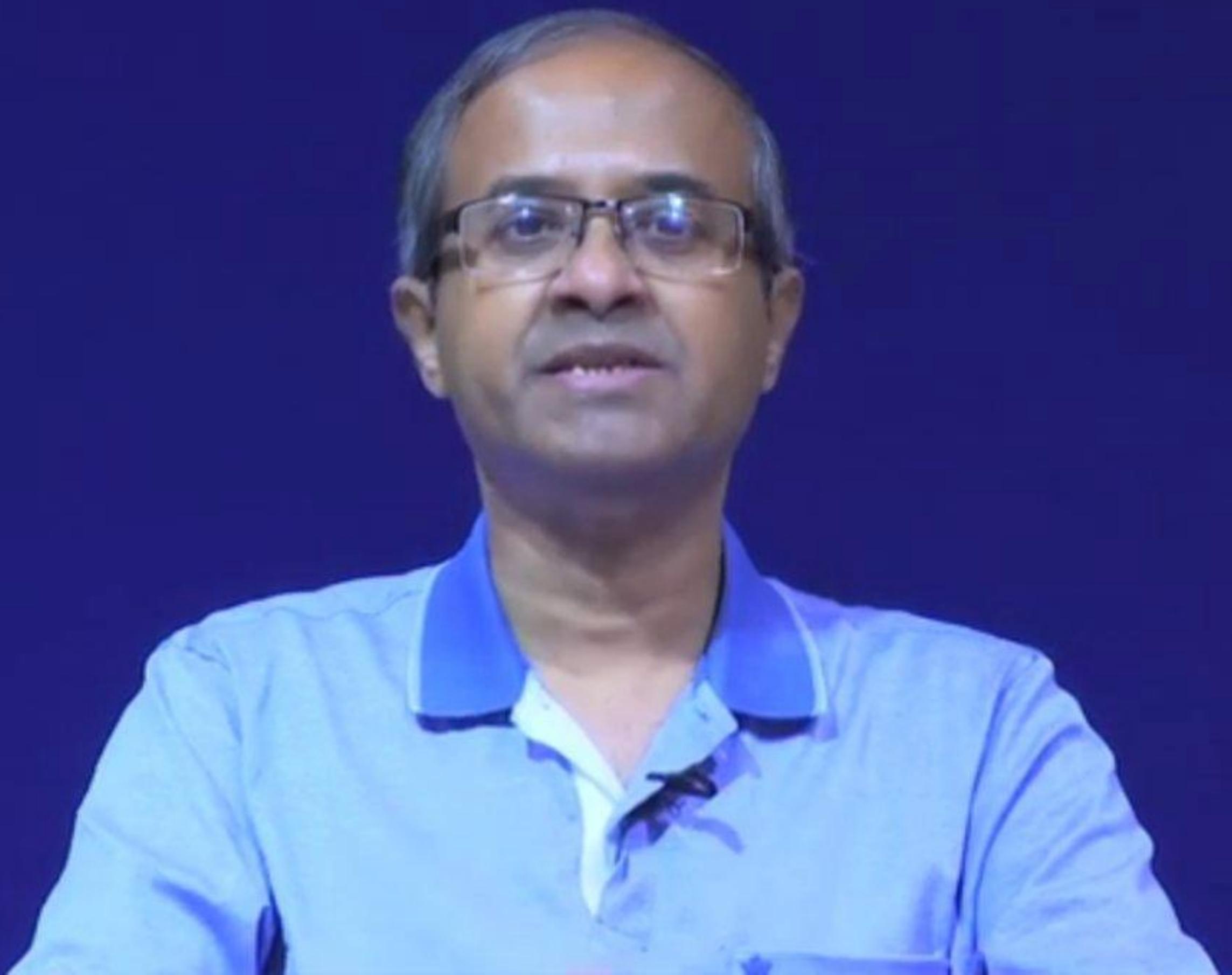
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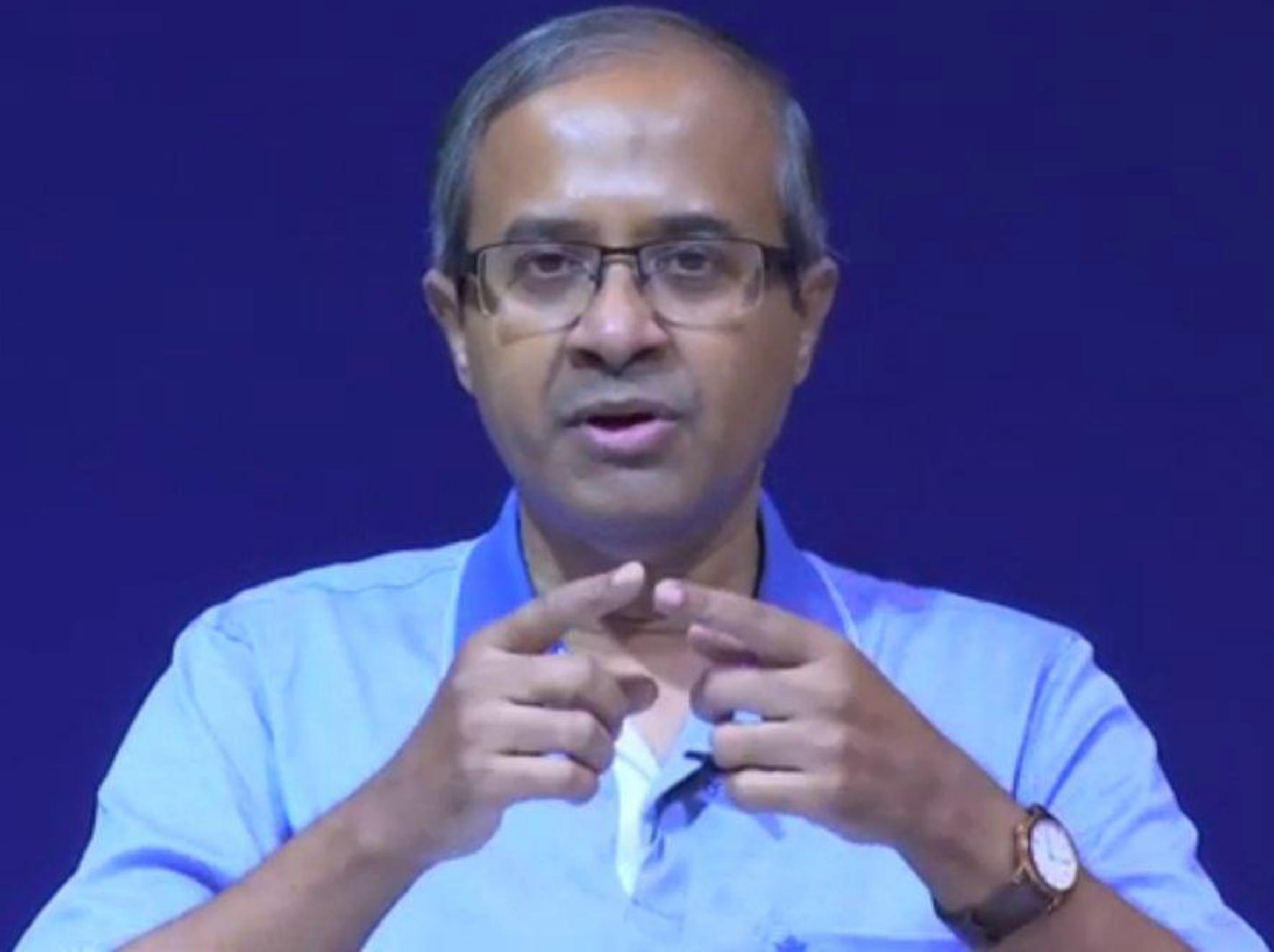
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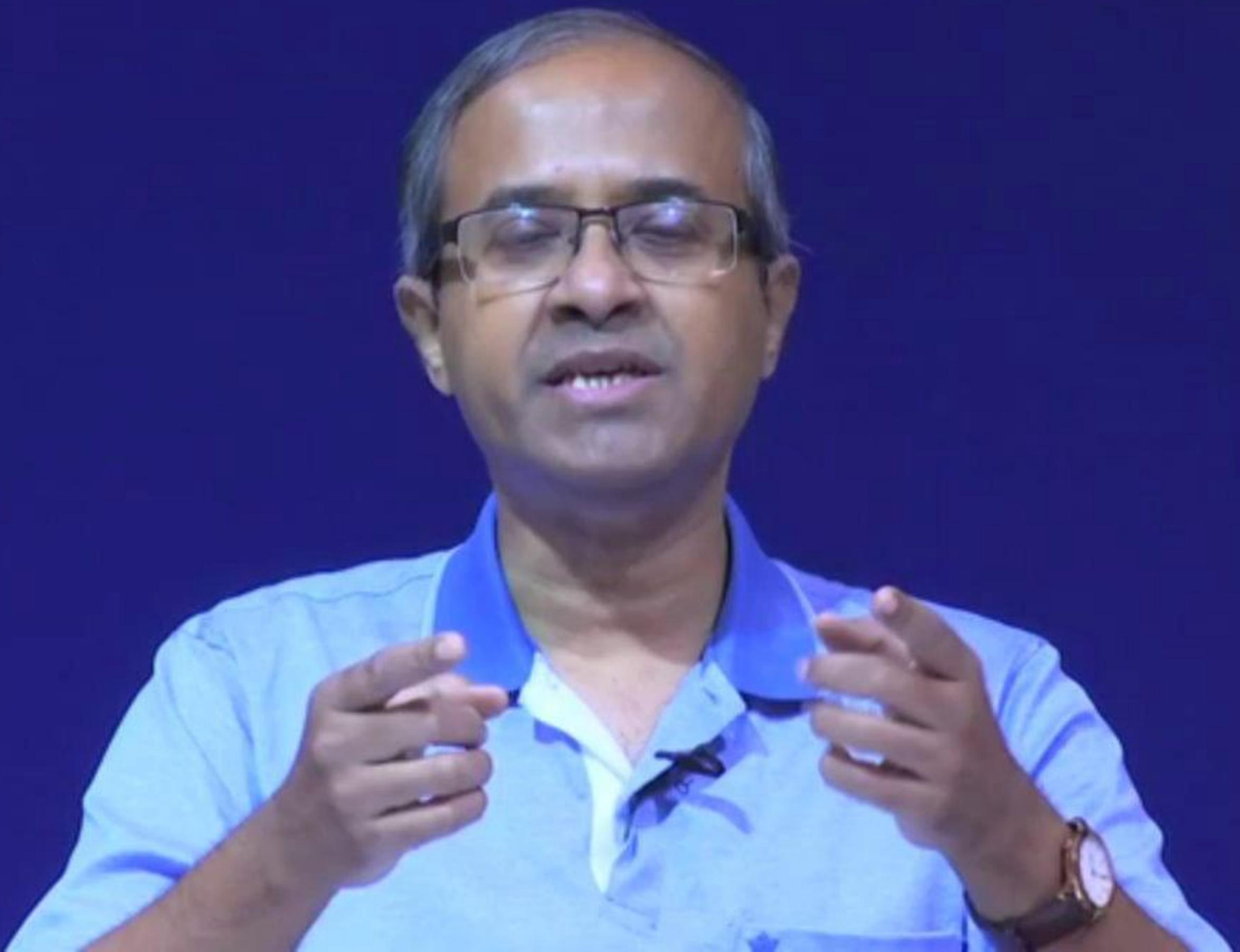
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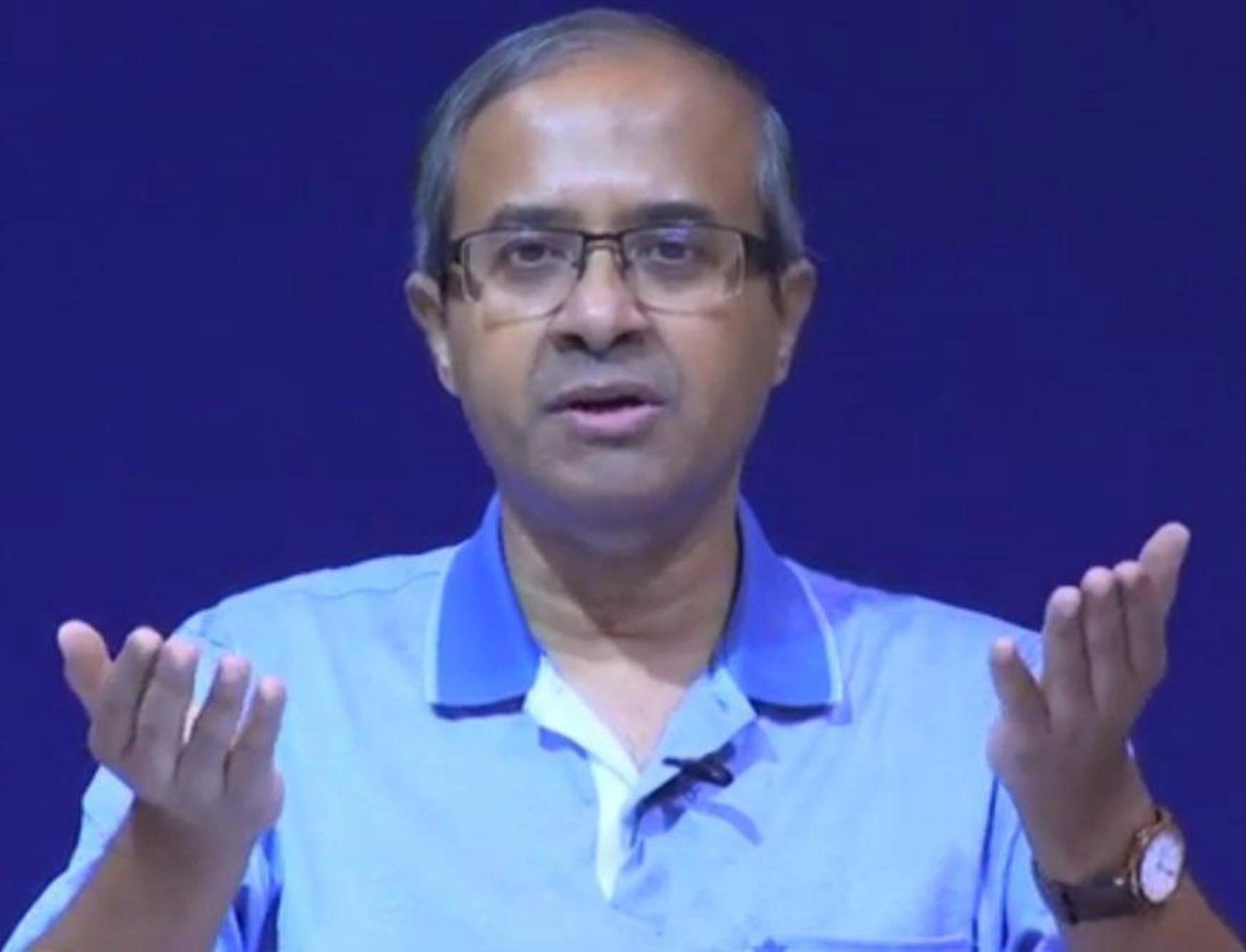
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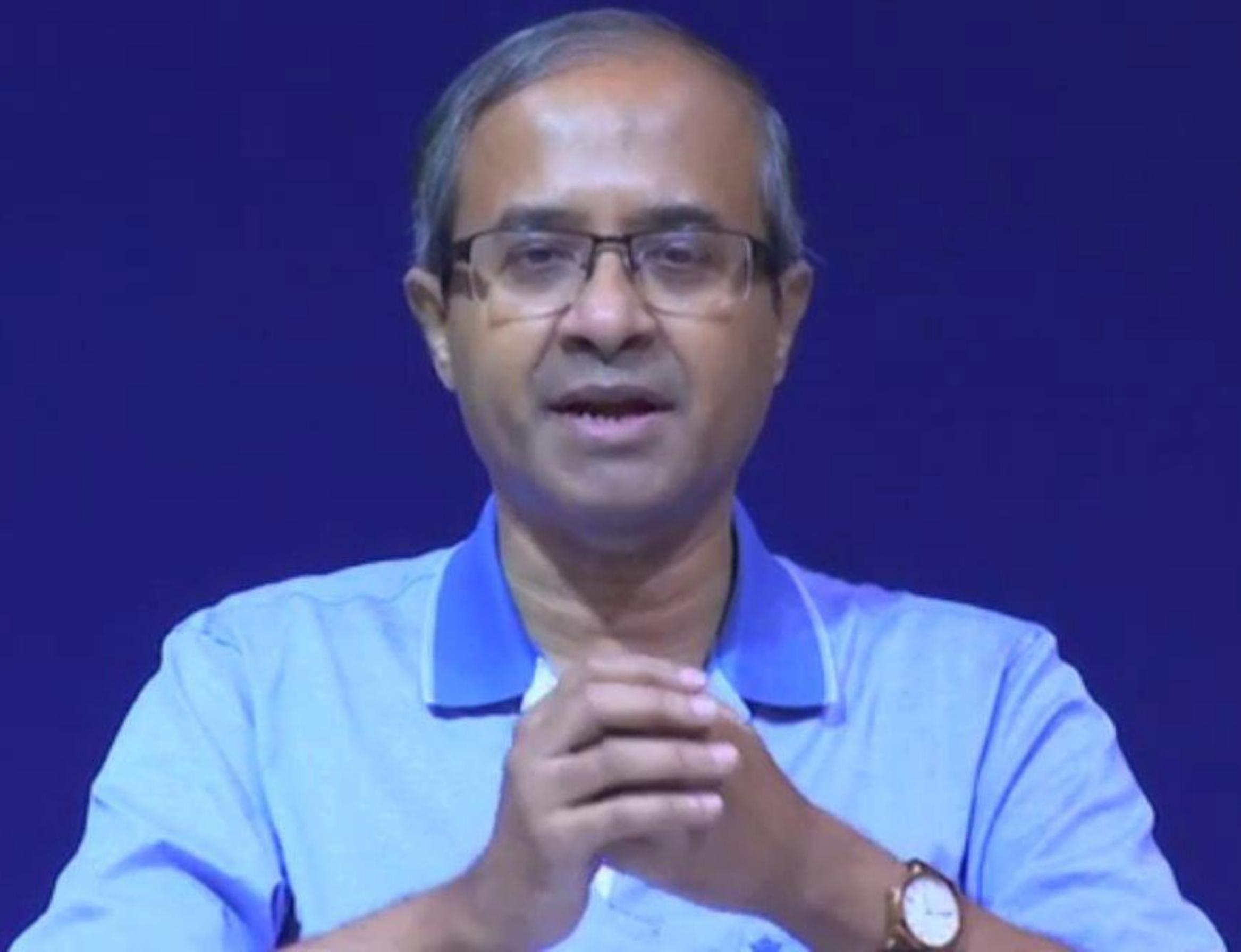
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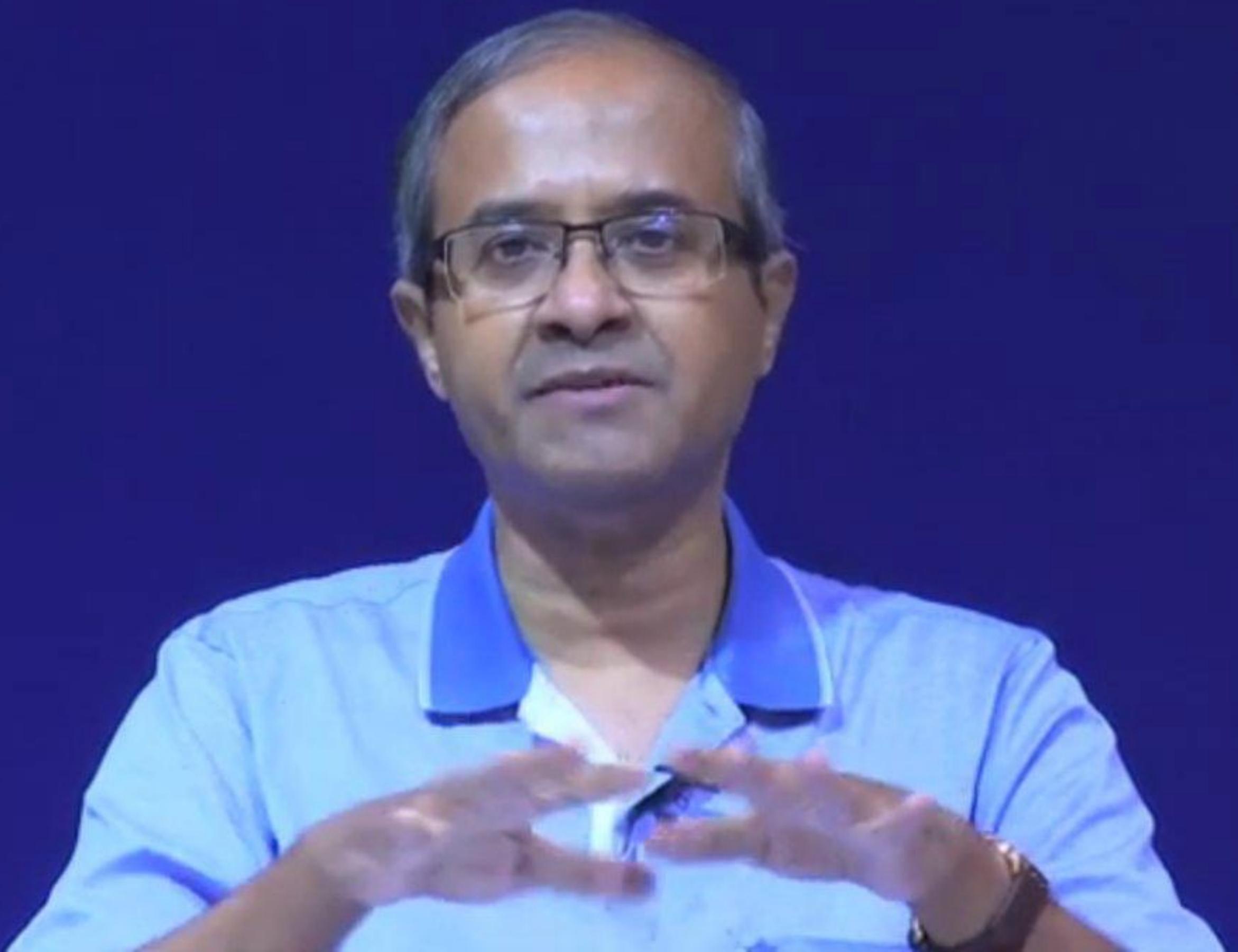
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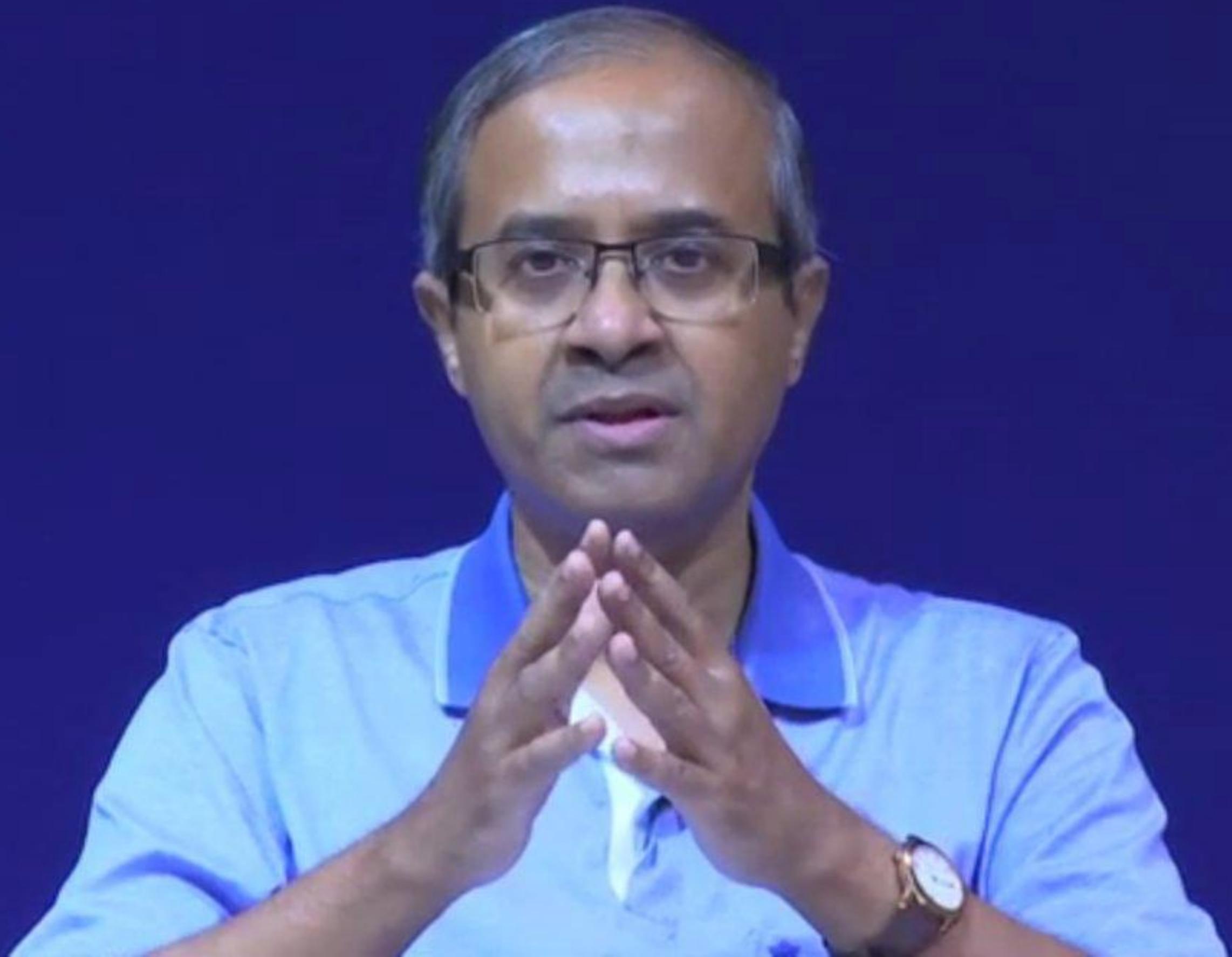
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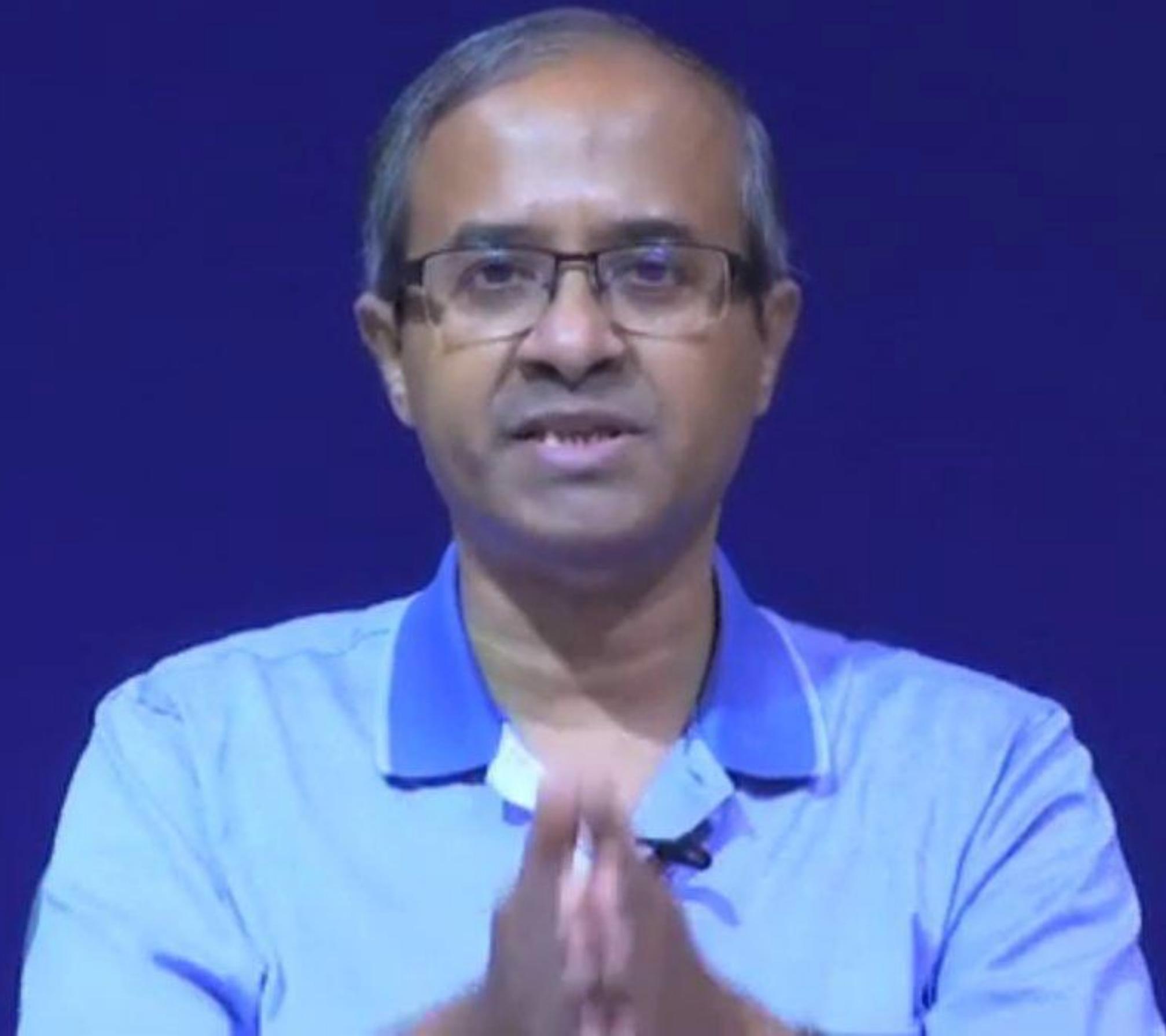
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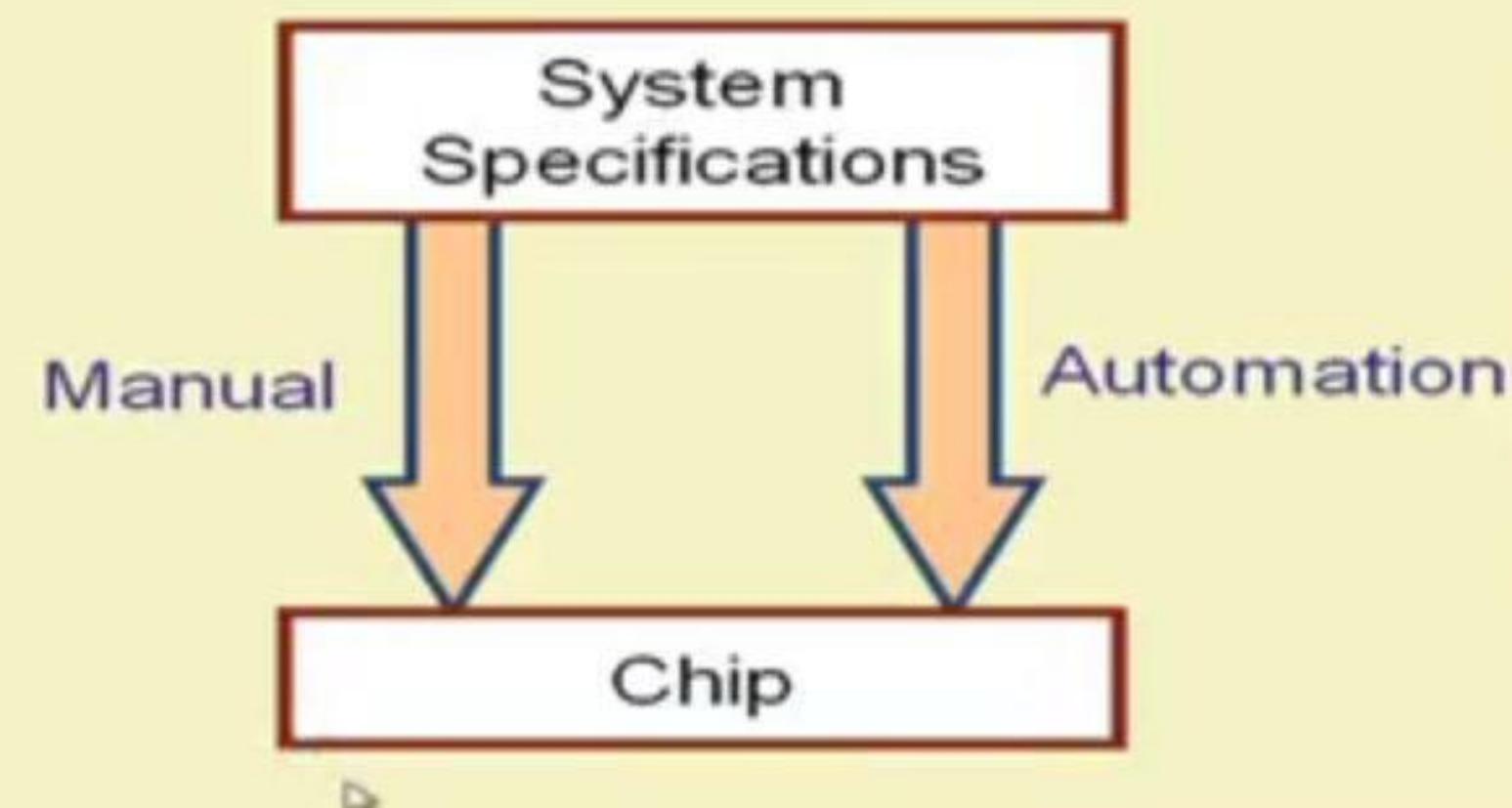


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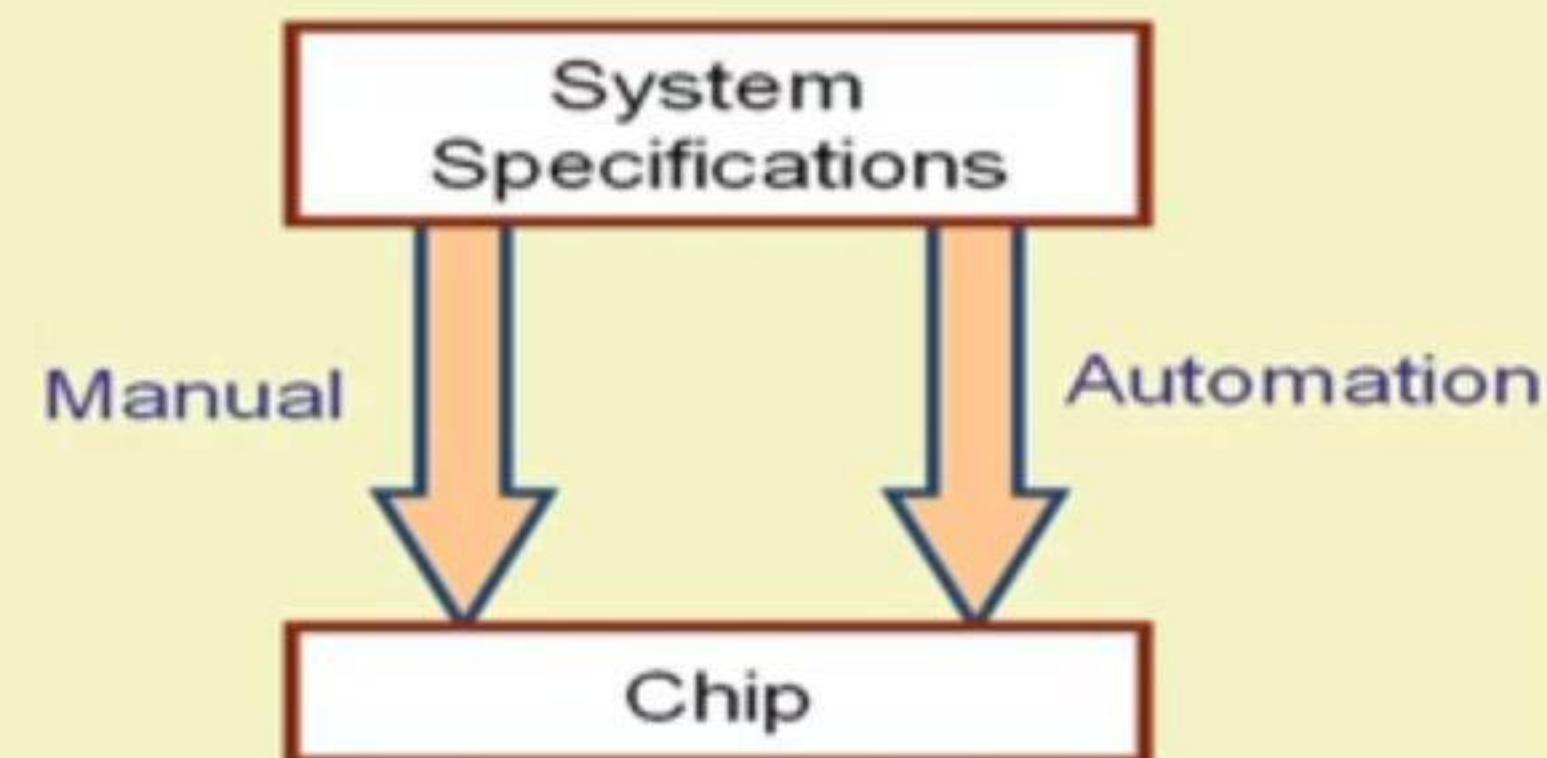
# VLSI Design Cycle

- Large number of devices
- Optimization requirements for high performance
- Time-to-market competition
- Cost



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## VLSI Design Cycle (contd.)

1. System specification
2. Functional design
3. Logic design
4. Circuit design
5. Physical design
6. Design verification
7. Fabrication
8. Packaging, testing, and debugging



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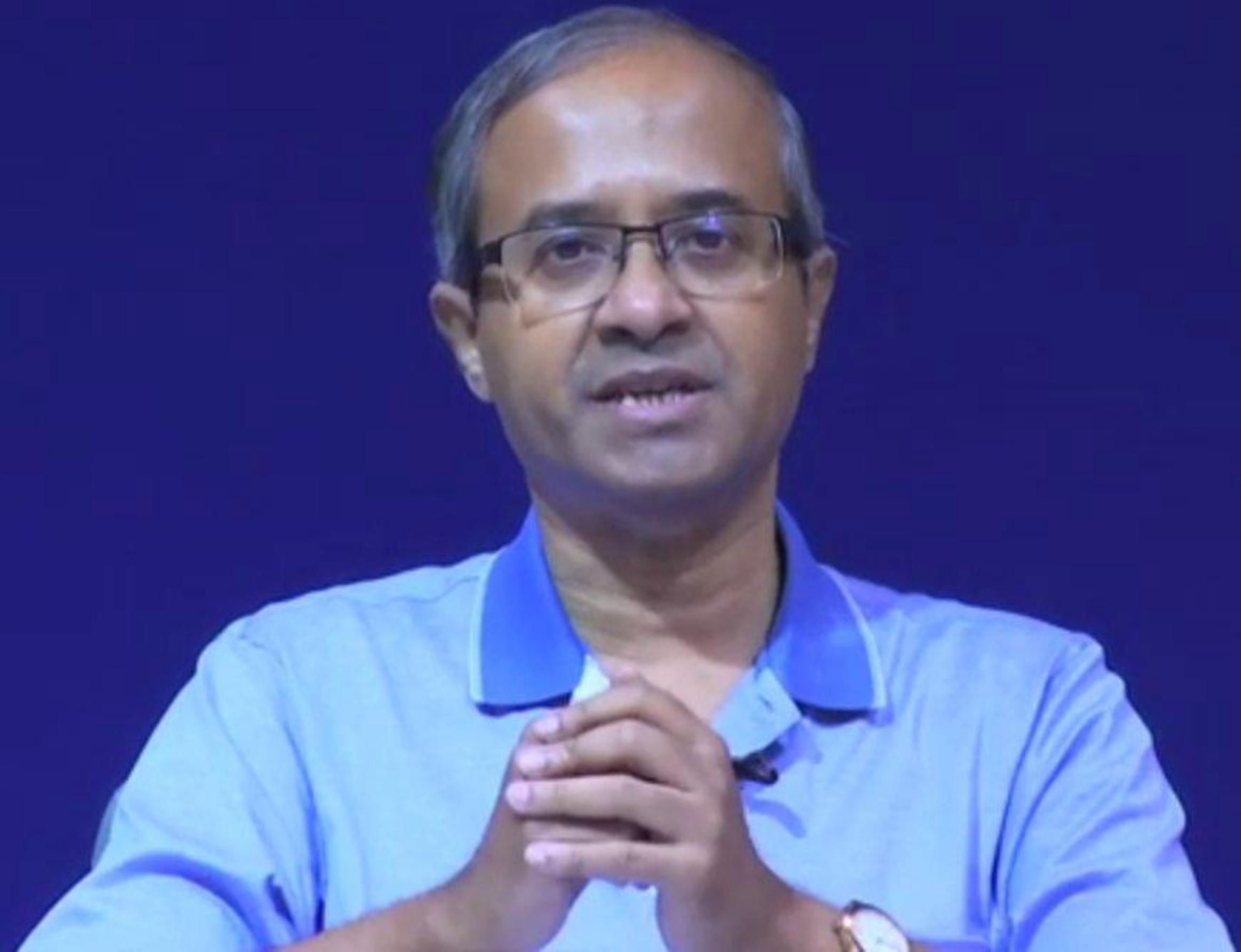


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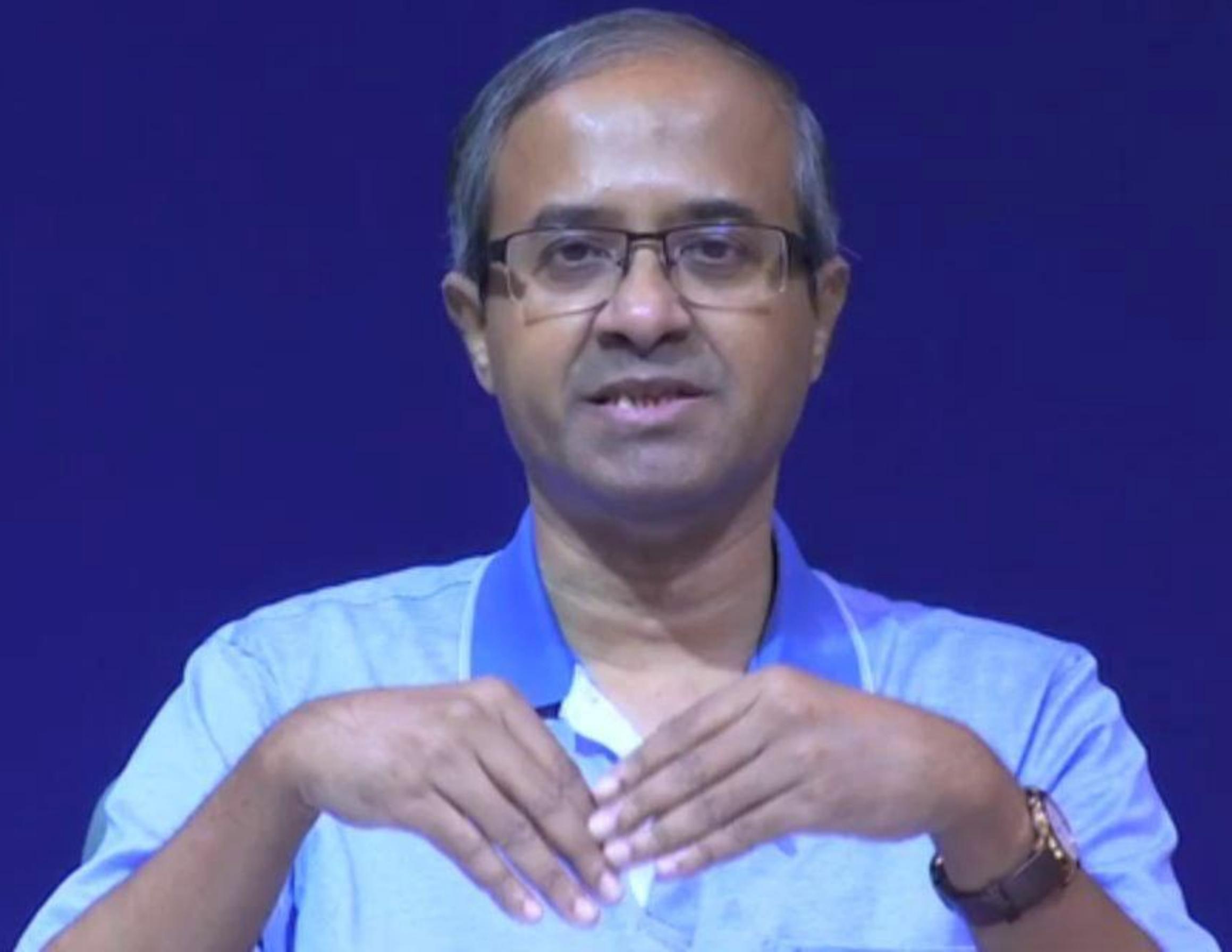
Hardware Modeling Using Verilog



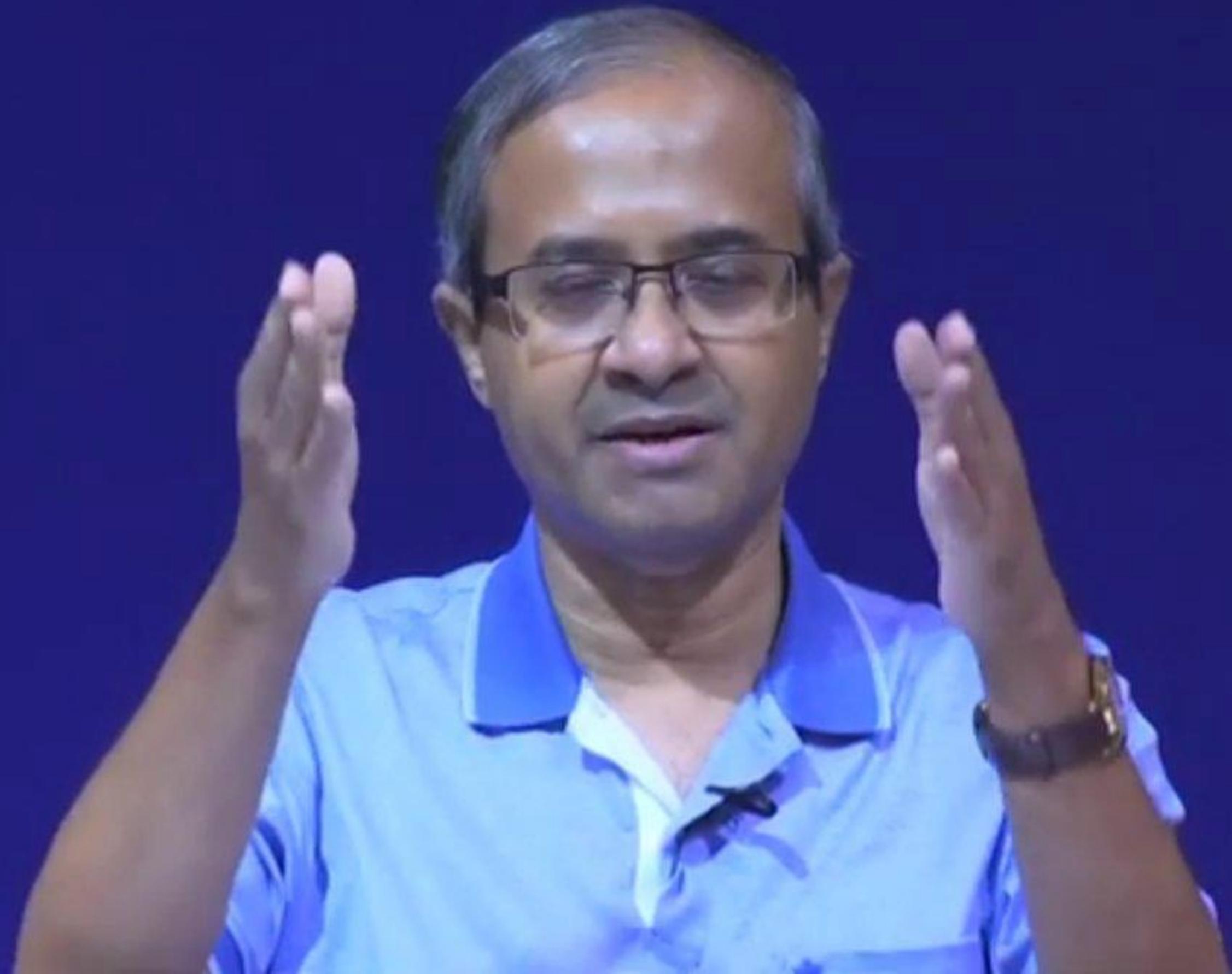
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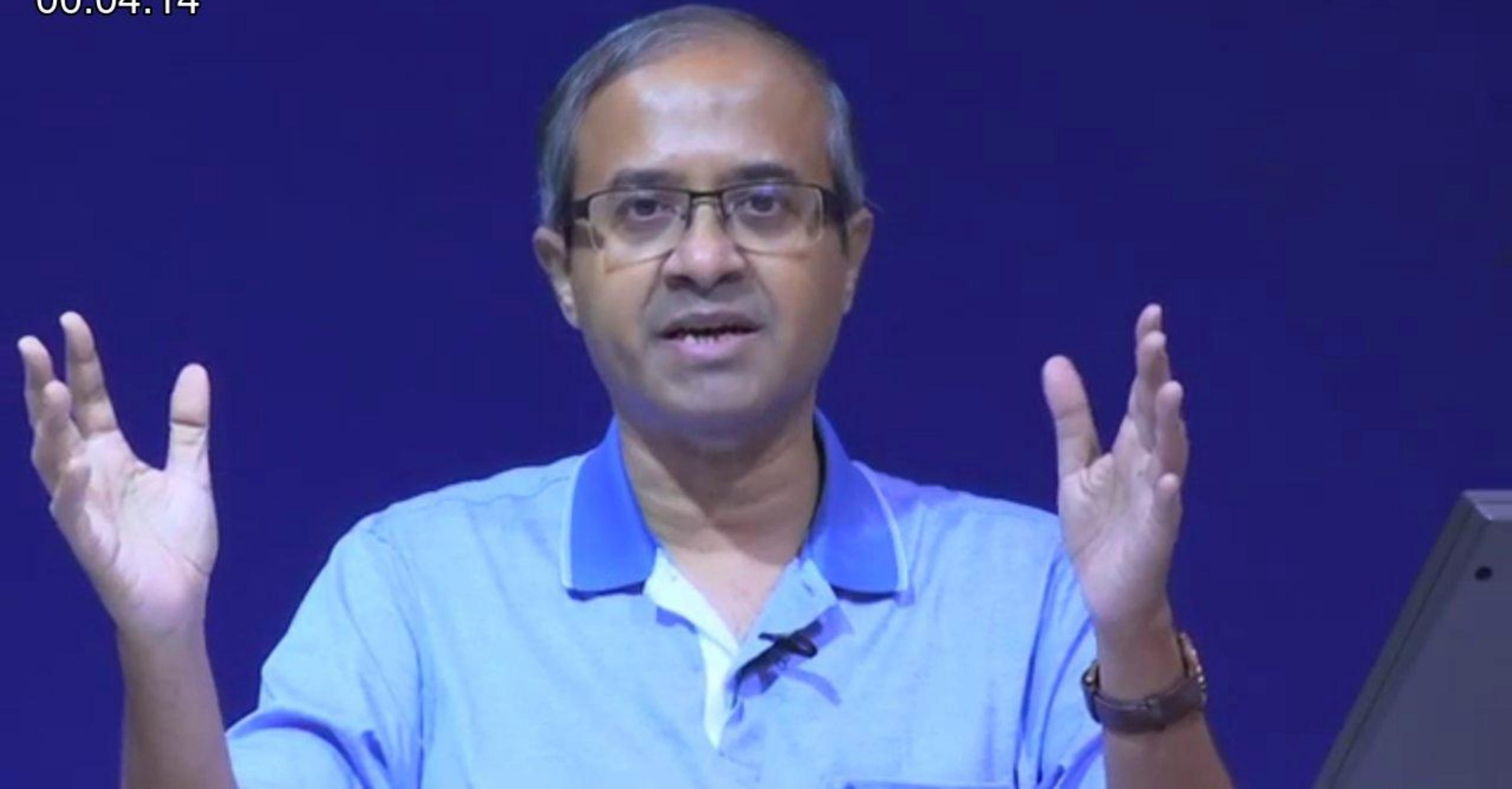


# Physical Design

- Converts a circuit description into a geometric description.
  - This description is used for fabrication of the chip.
- Basic steps in the physical design cycle:
  1. Partitioning, floorplanning and placement
  2. Routing
  3. Static timing analysis
  4. Signal integrity and crosstalk analysis
  5. Physical verification and signoff



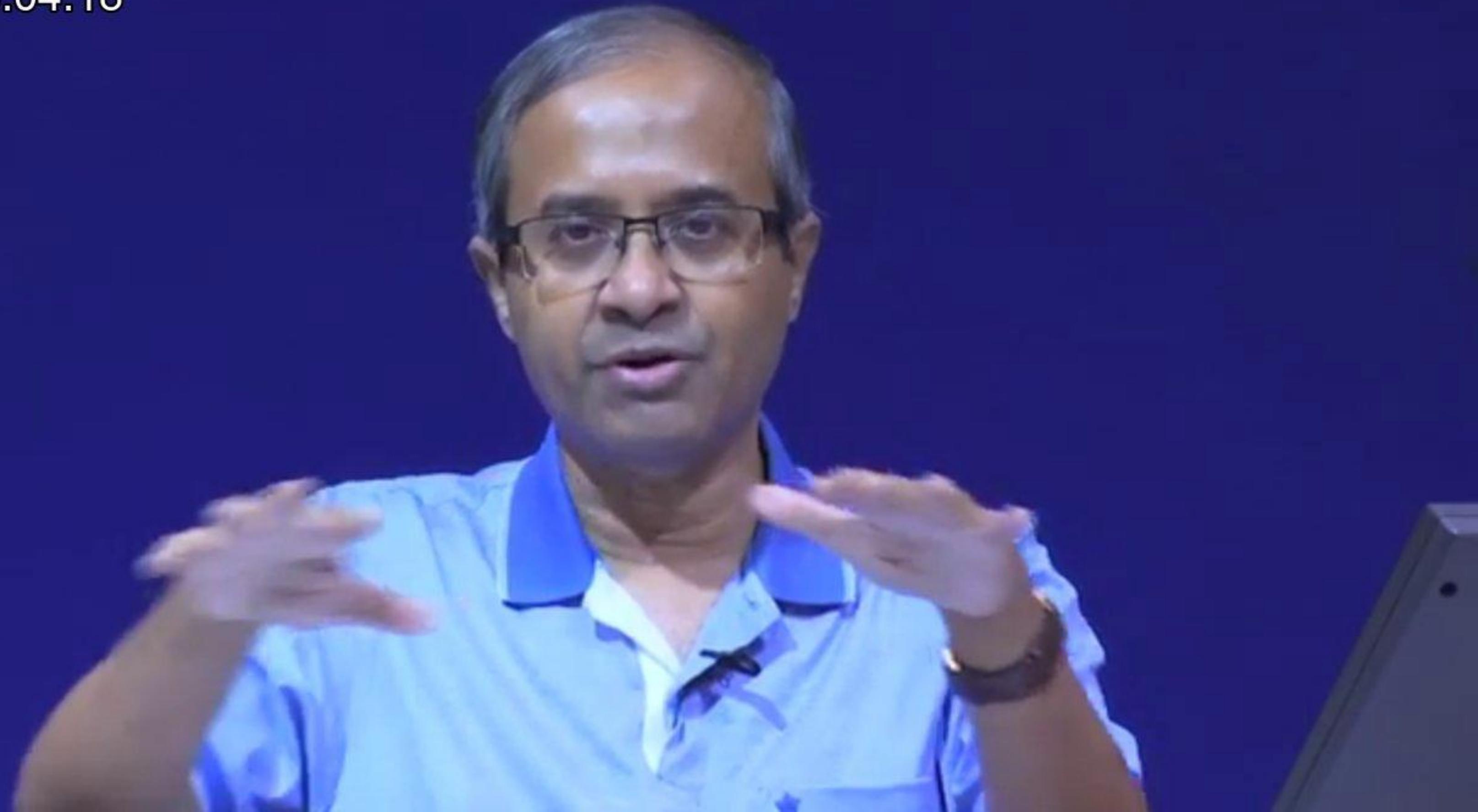
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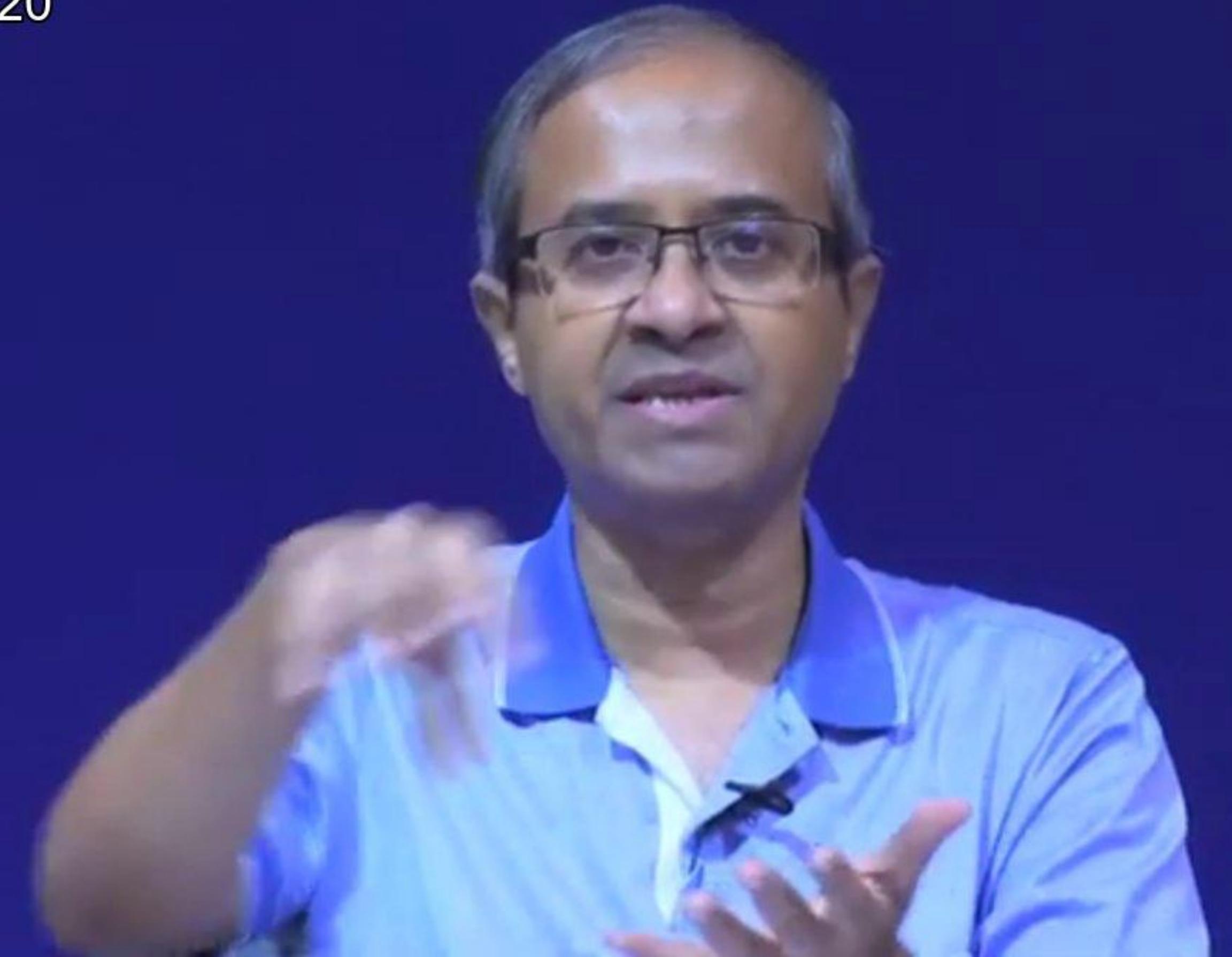
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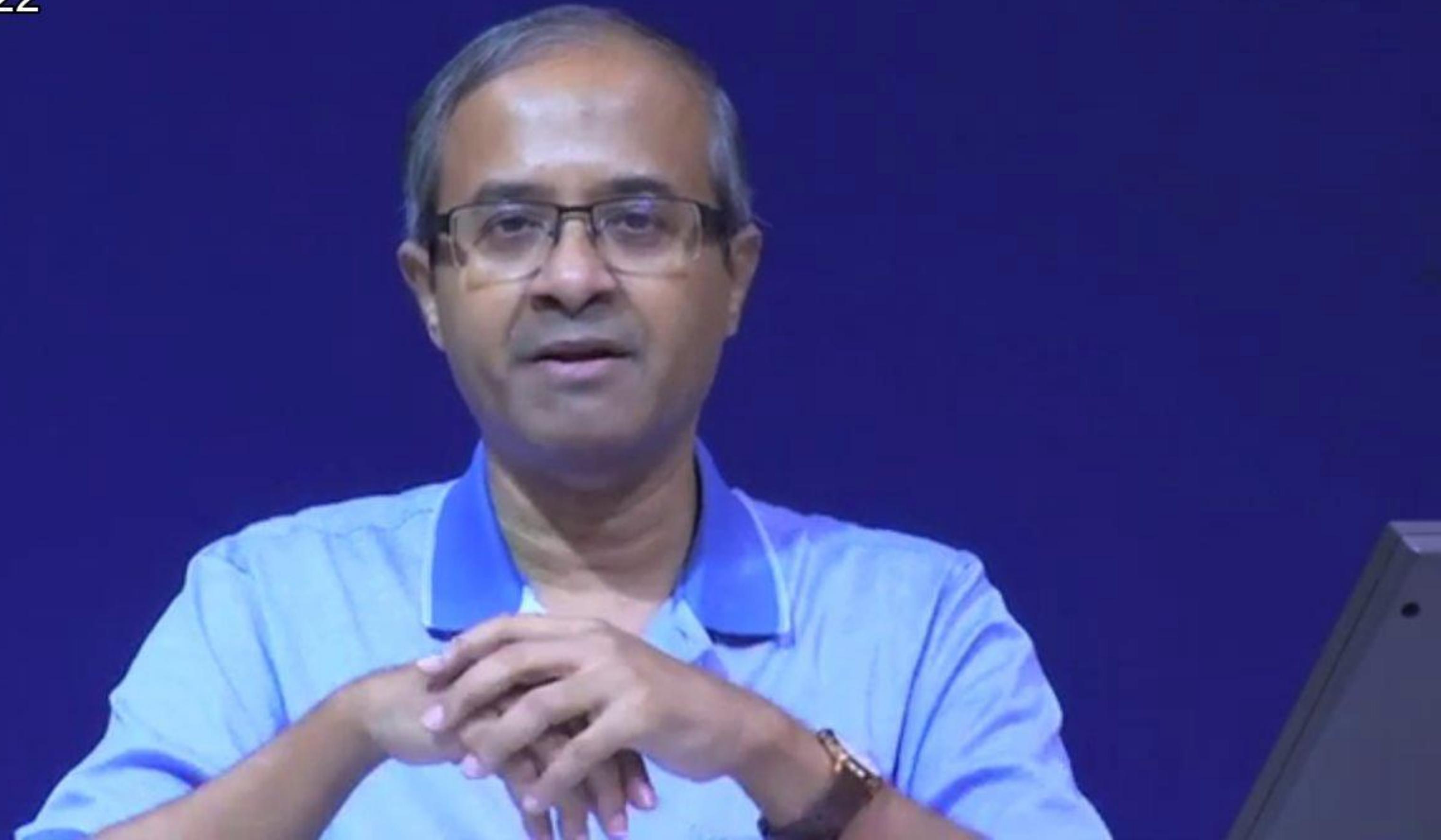
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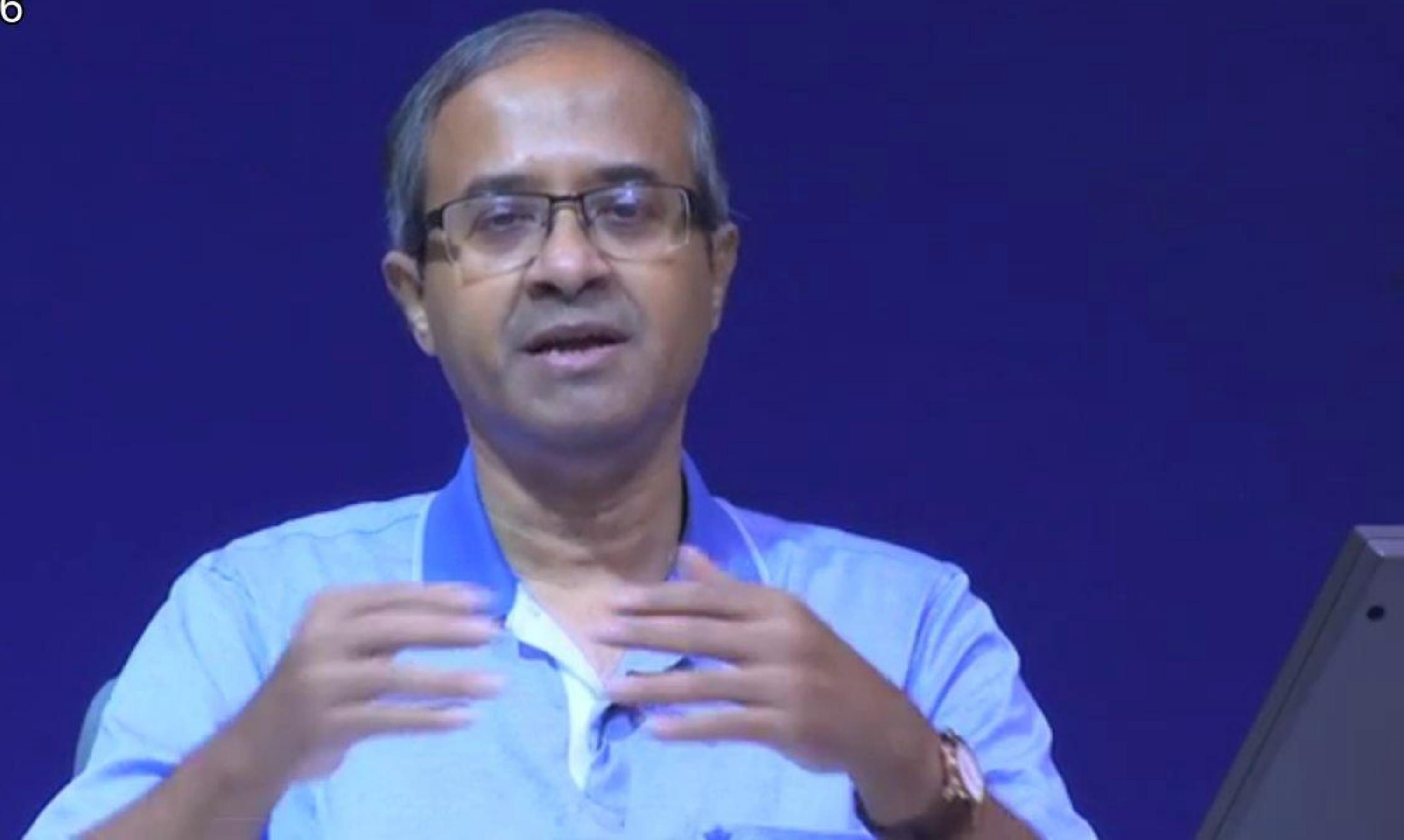
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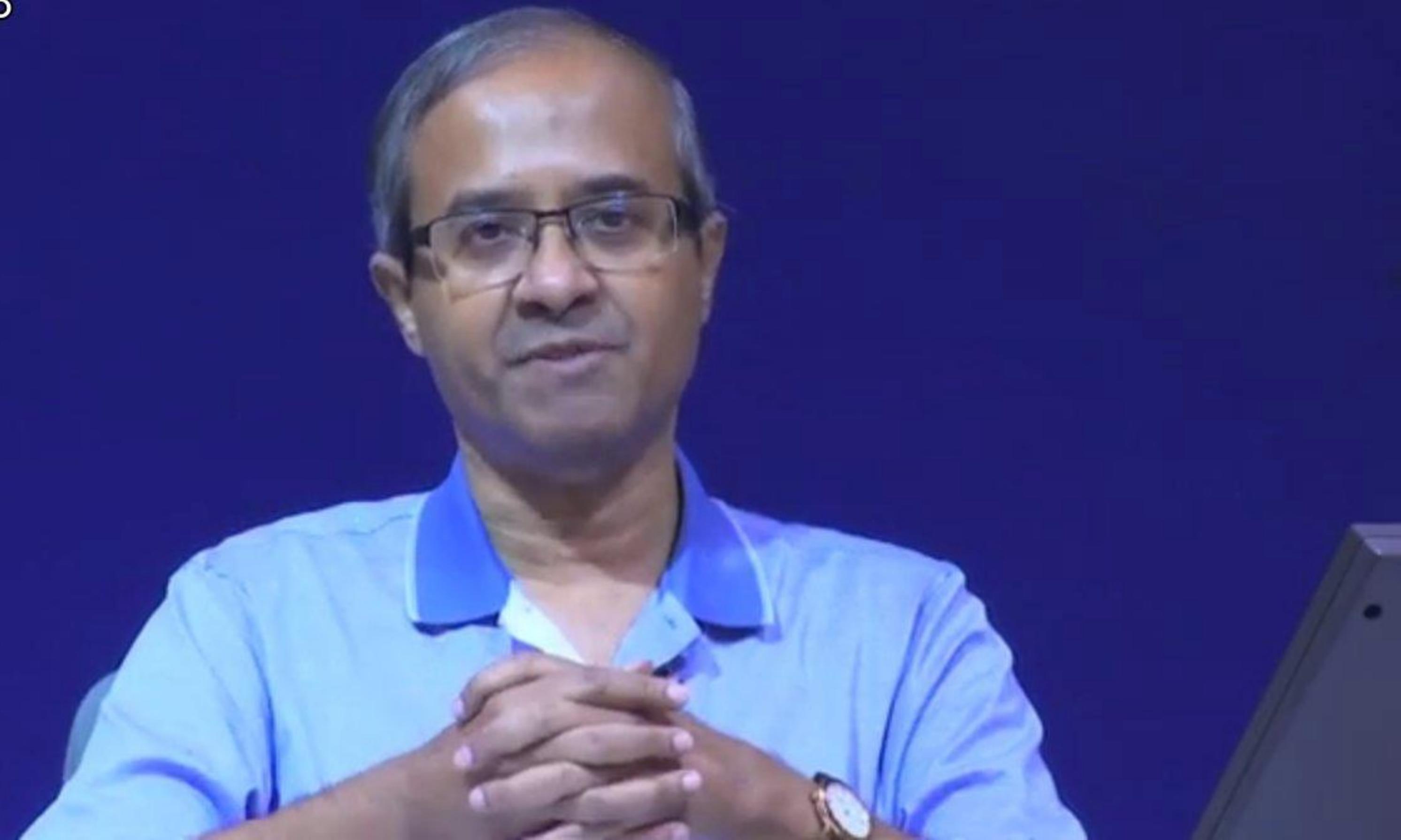
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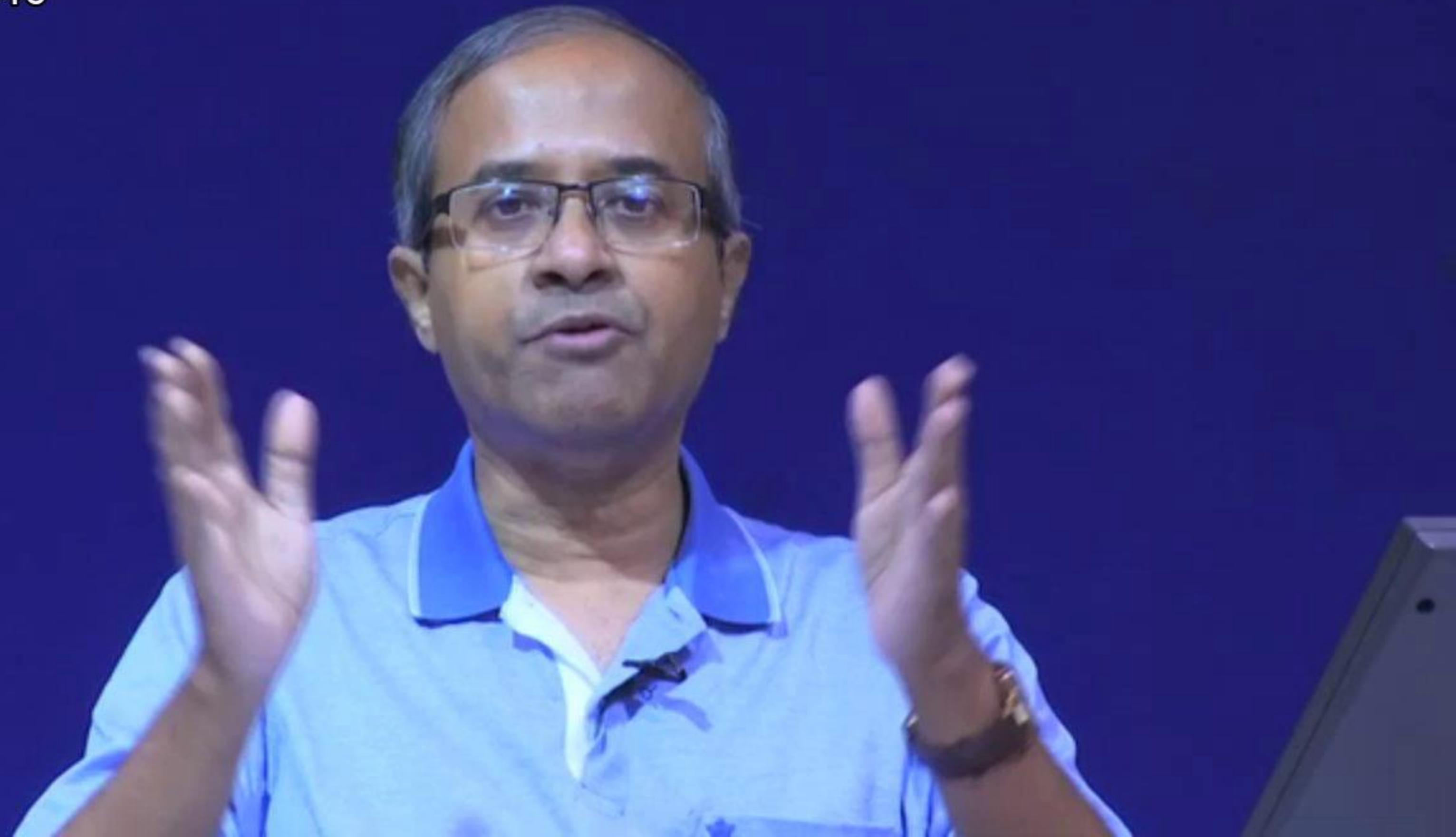
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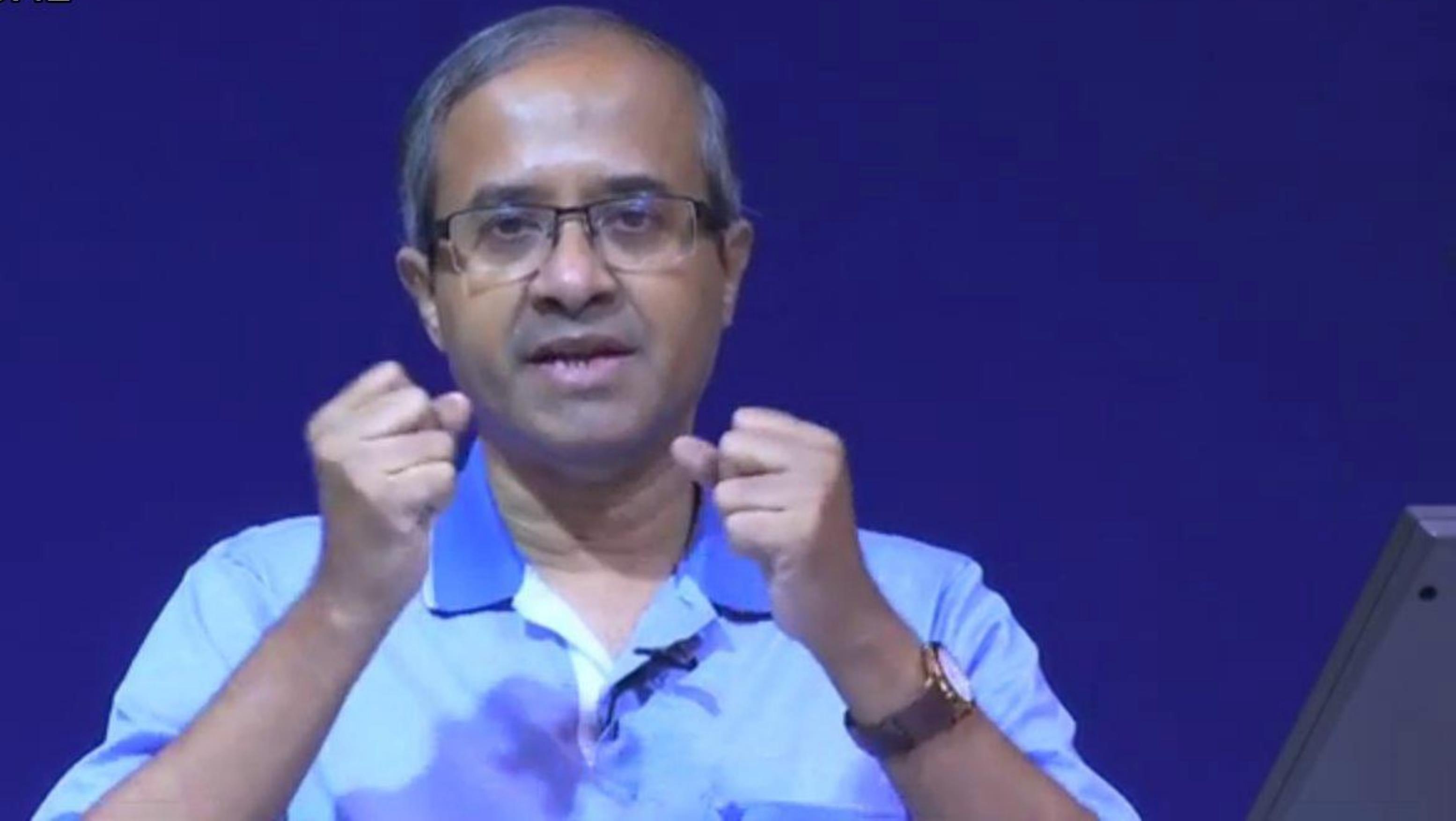
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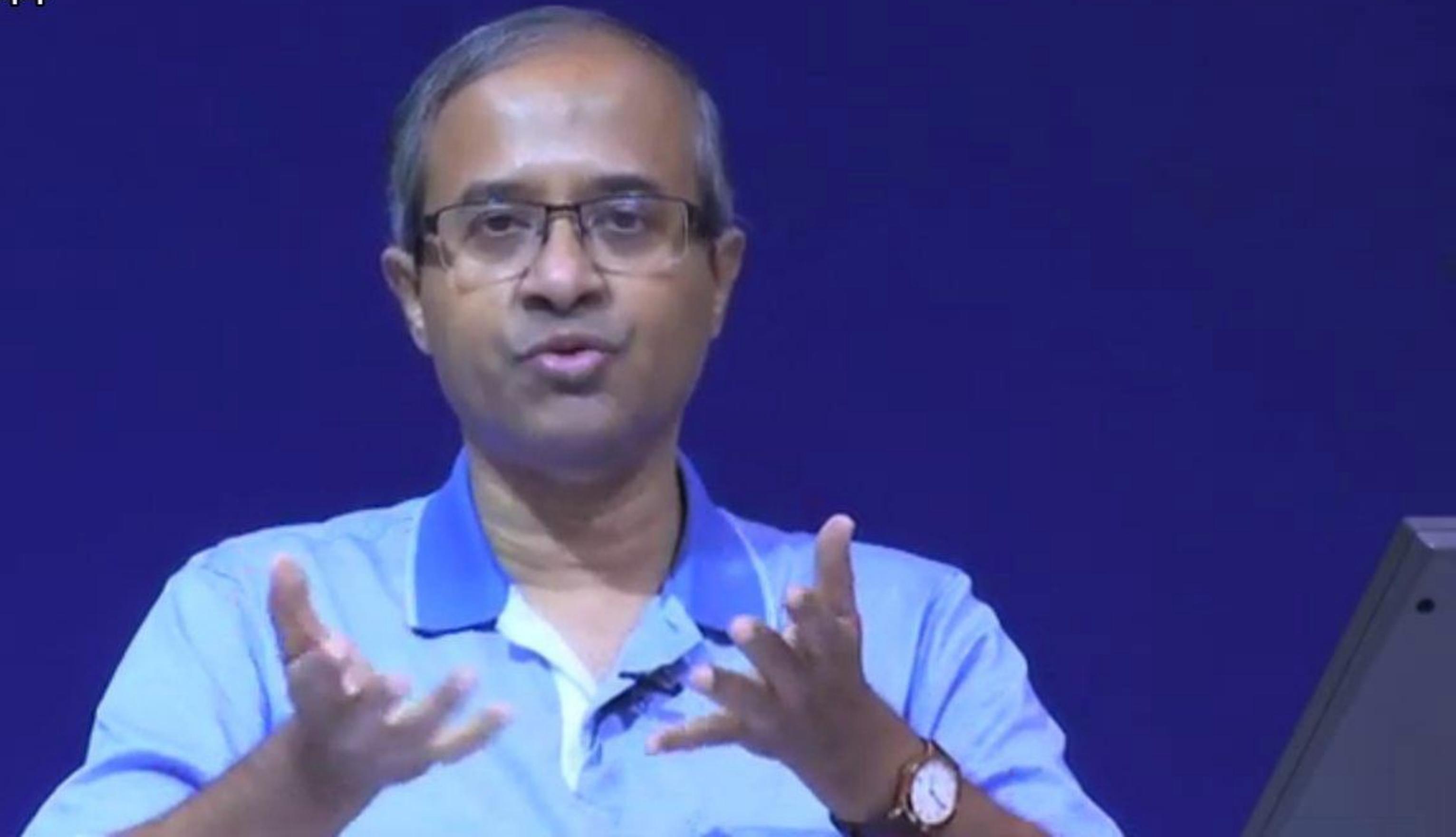
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# Field Programmable Gate Array (FPGA)



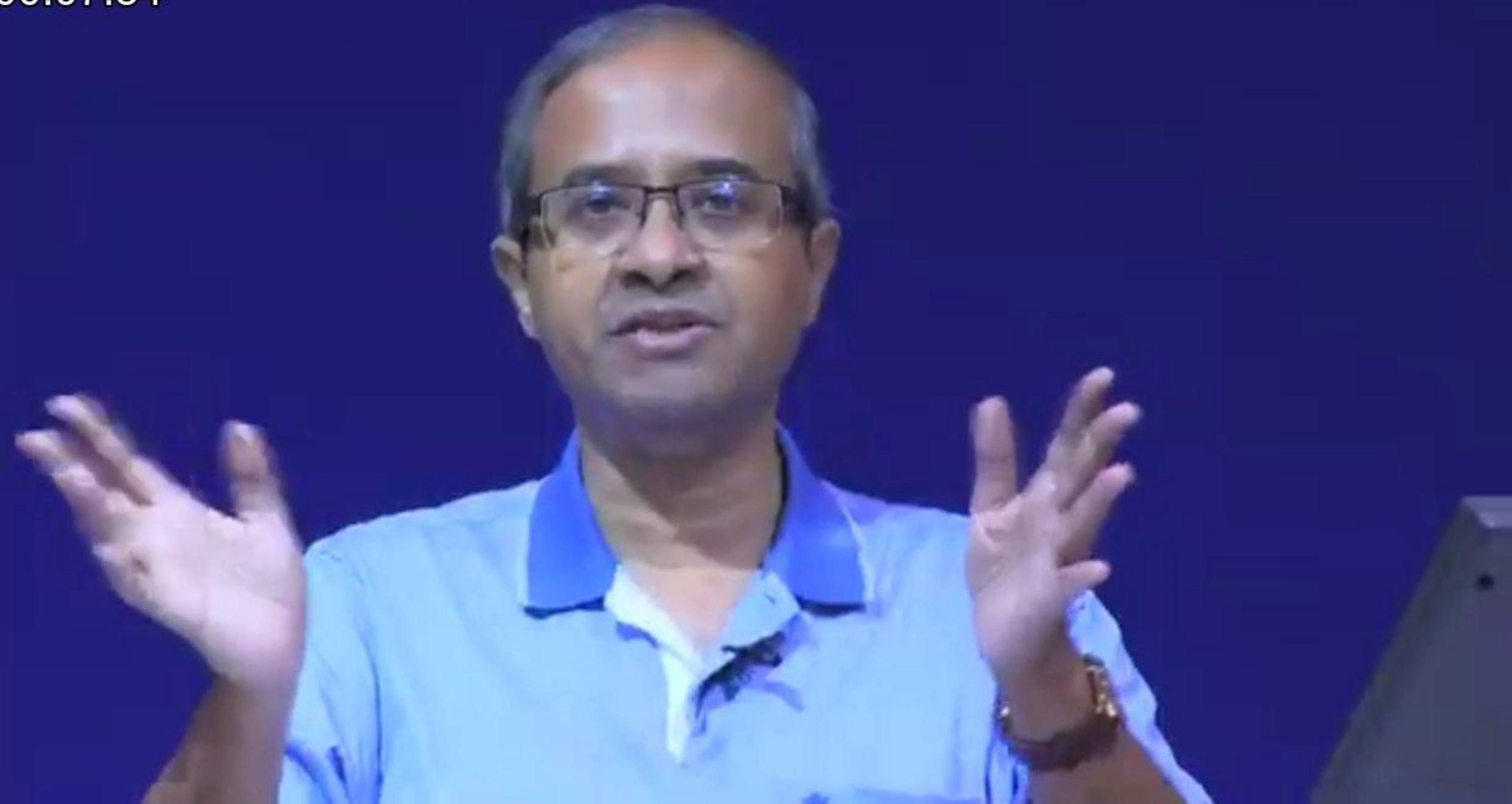
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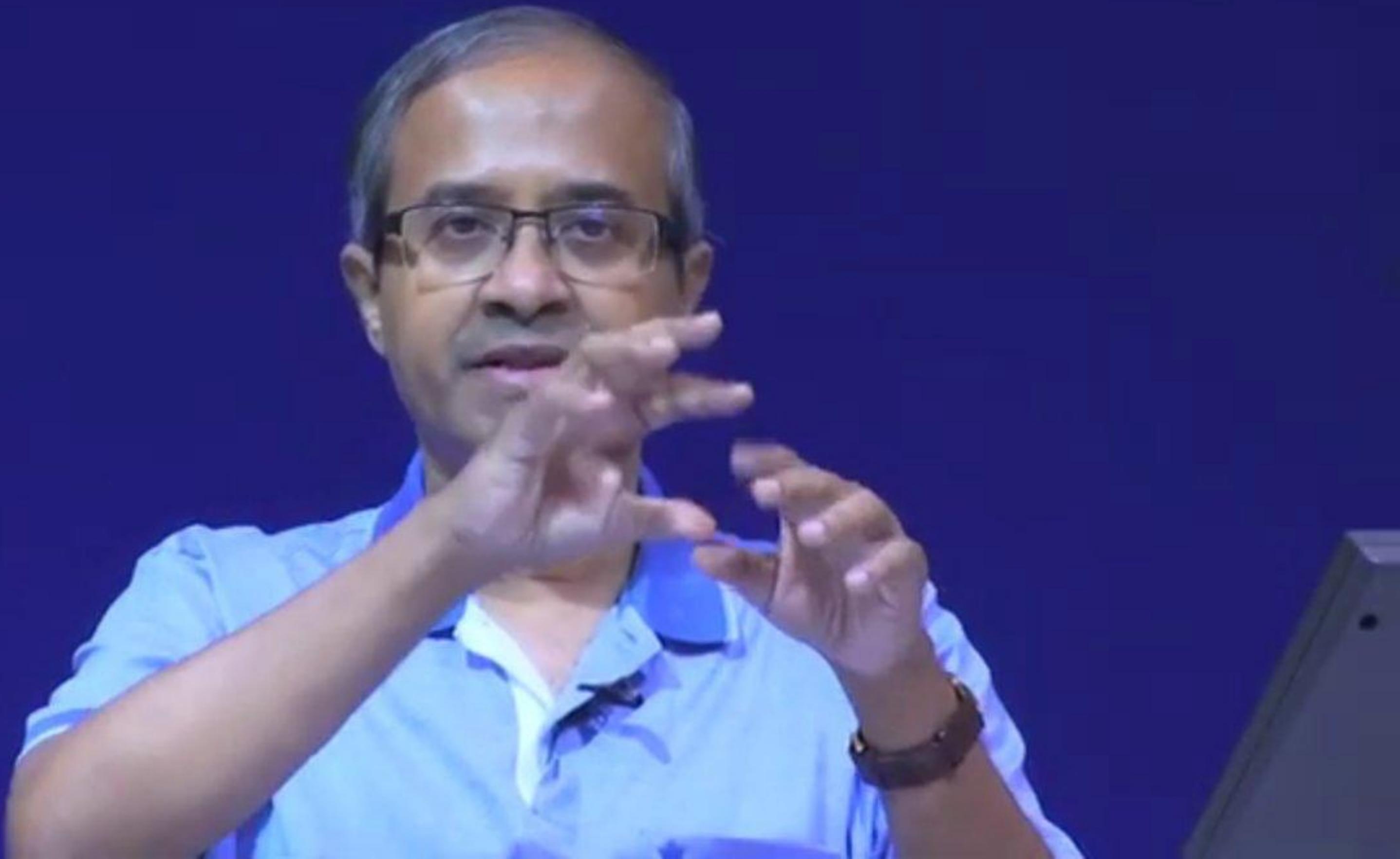
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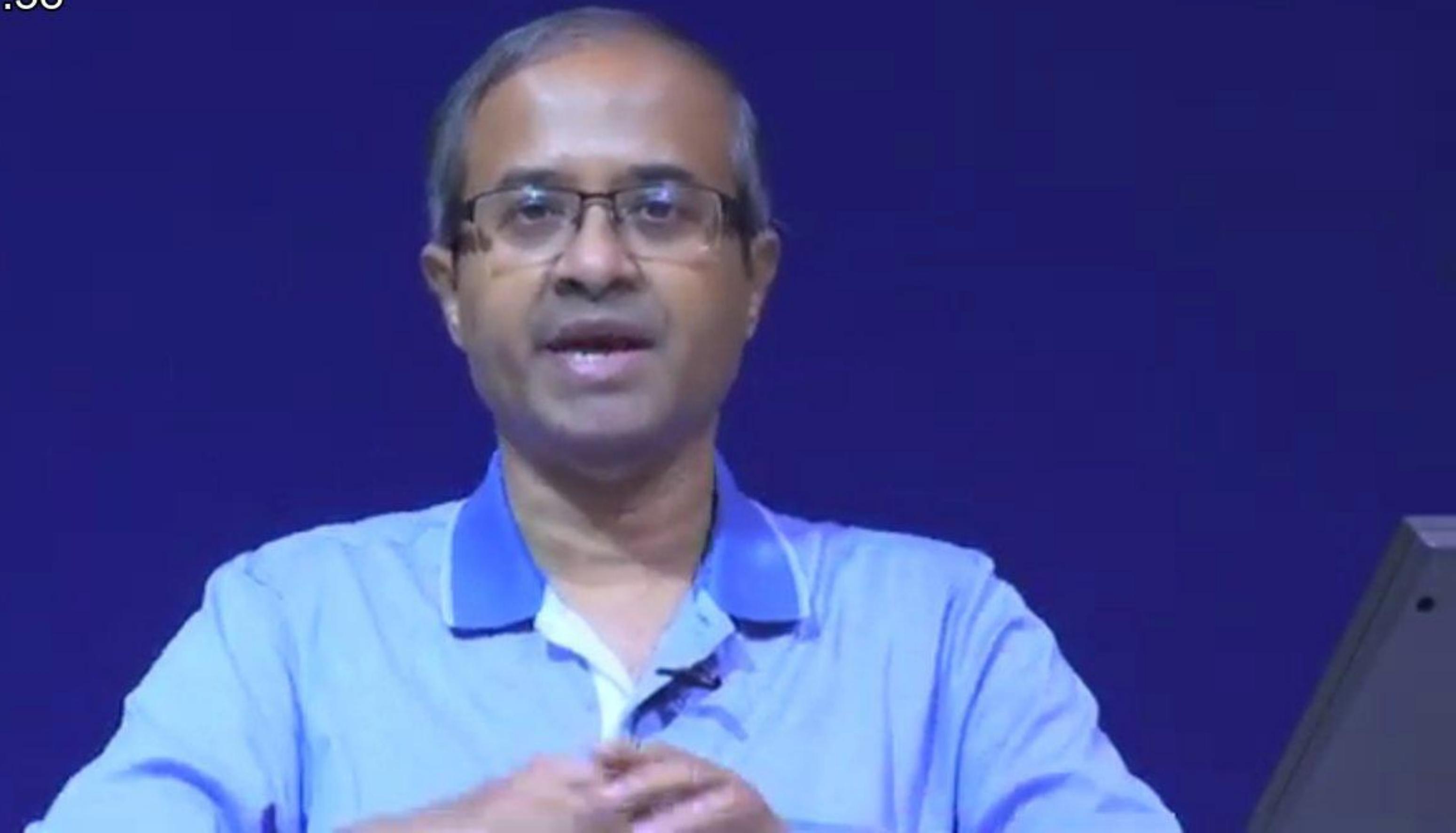
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## What does FPGA offer?

- User / Field Programmability.
  - Array of logic cells connected via routing channels.
  - Different types of cells:
    - Special I/O cells.
    - Logic cells (Mainly lookup tables (LUT) with associated registers).
  - Interconnection between cells:
    - Using SRAM based switches.
    - Using anti-fuse elements.



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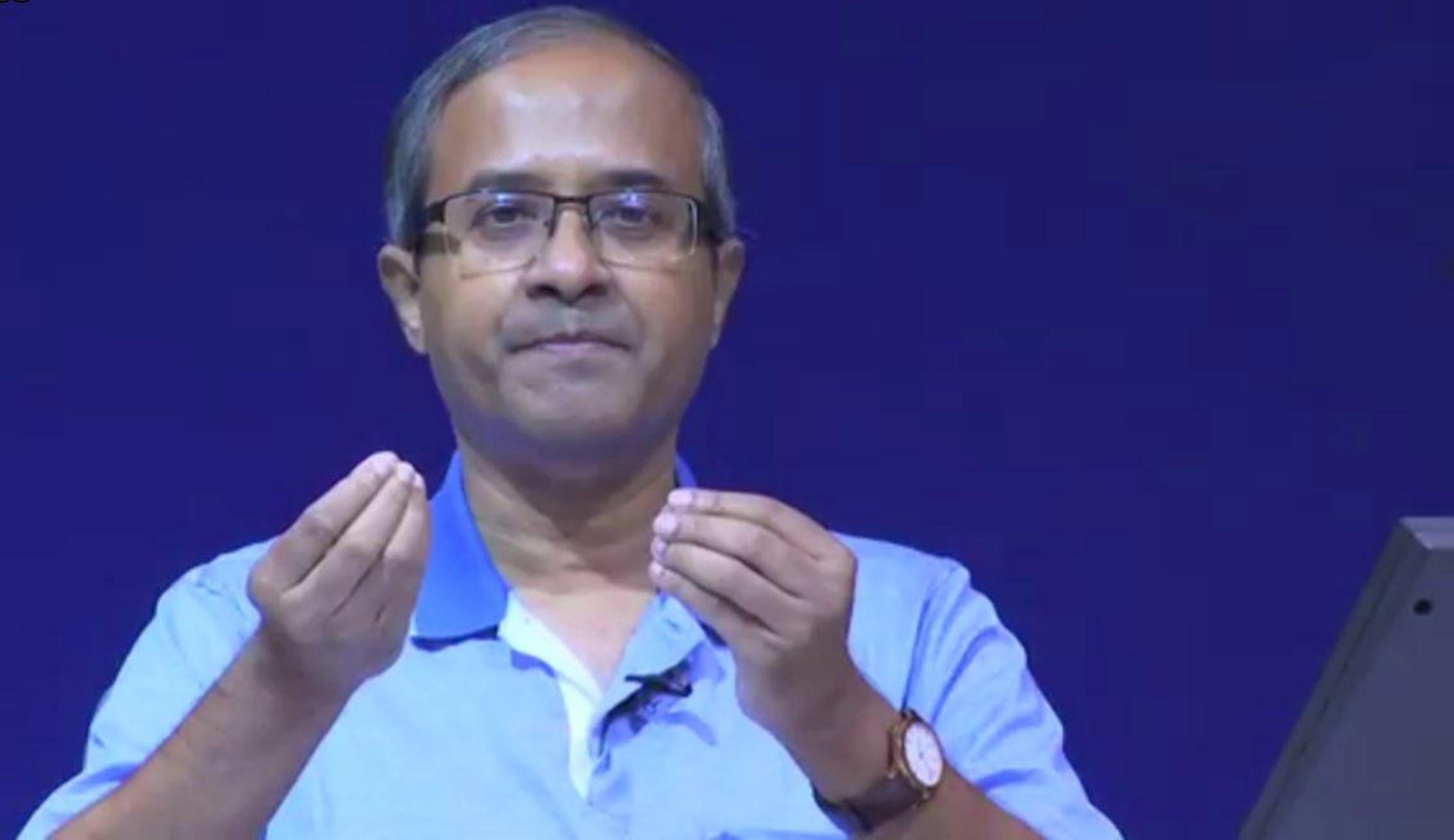
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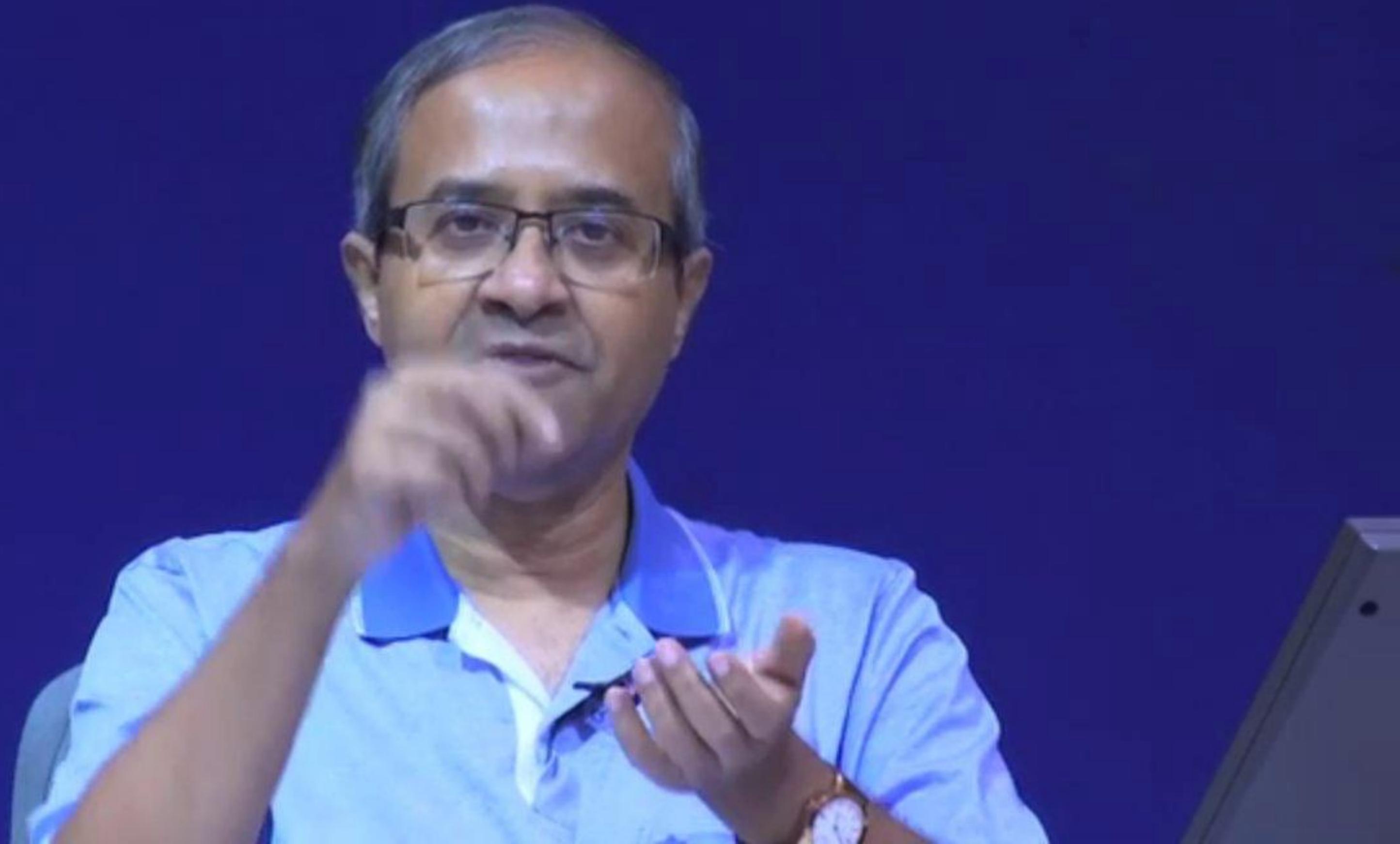
Hardware Modeling Using Verilog



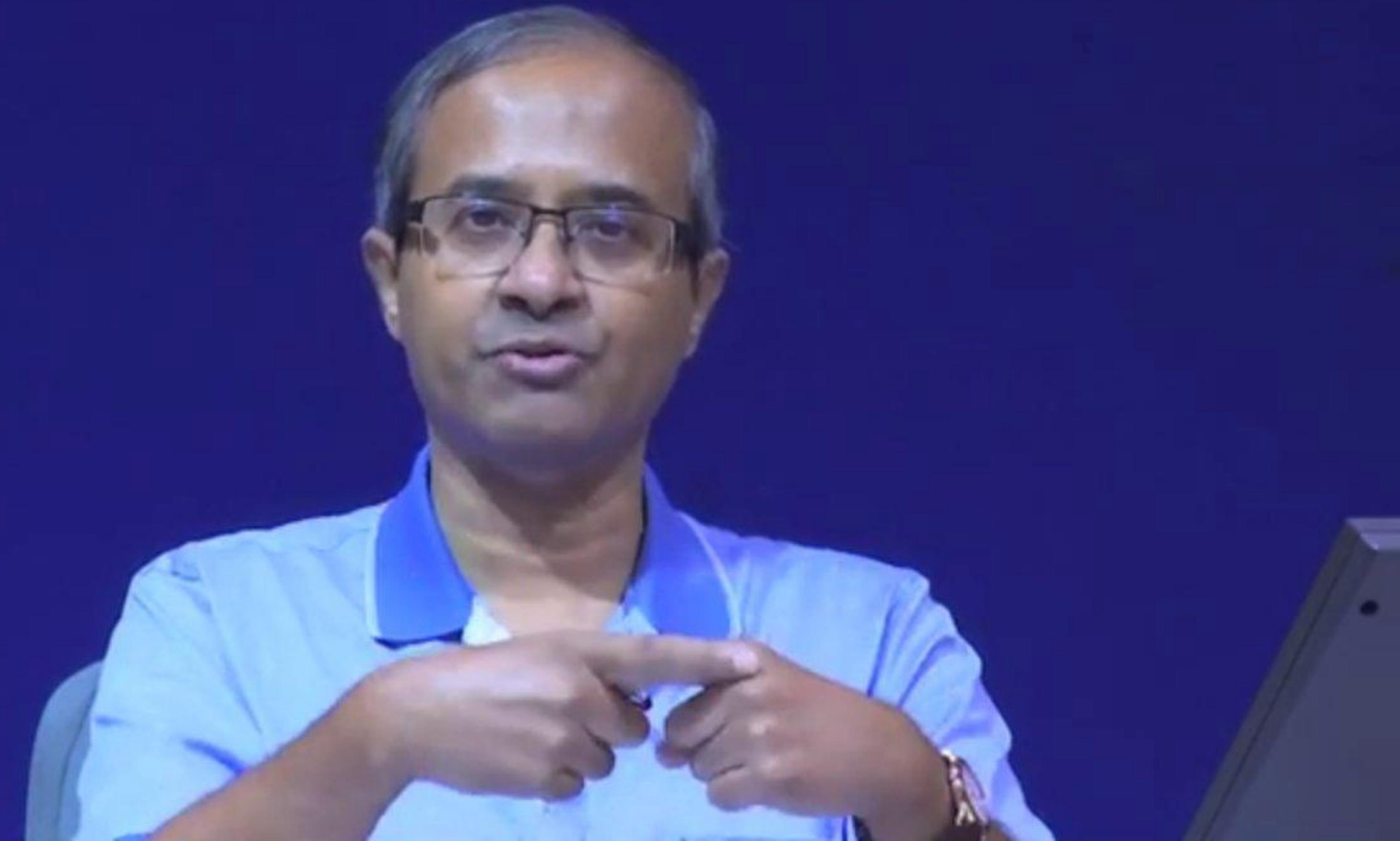
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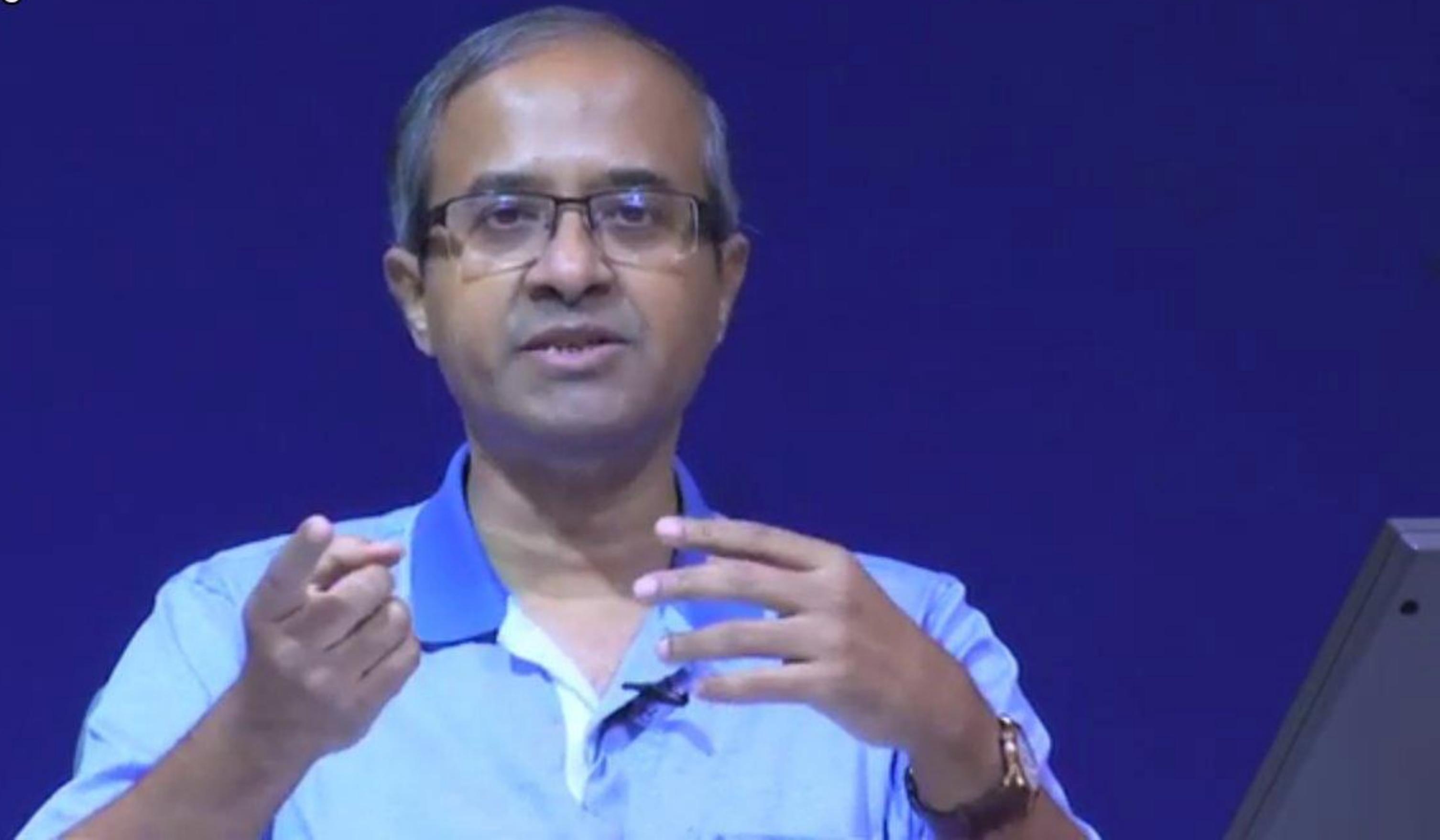
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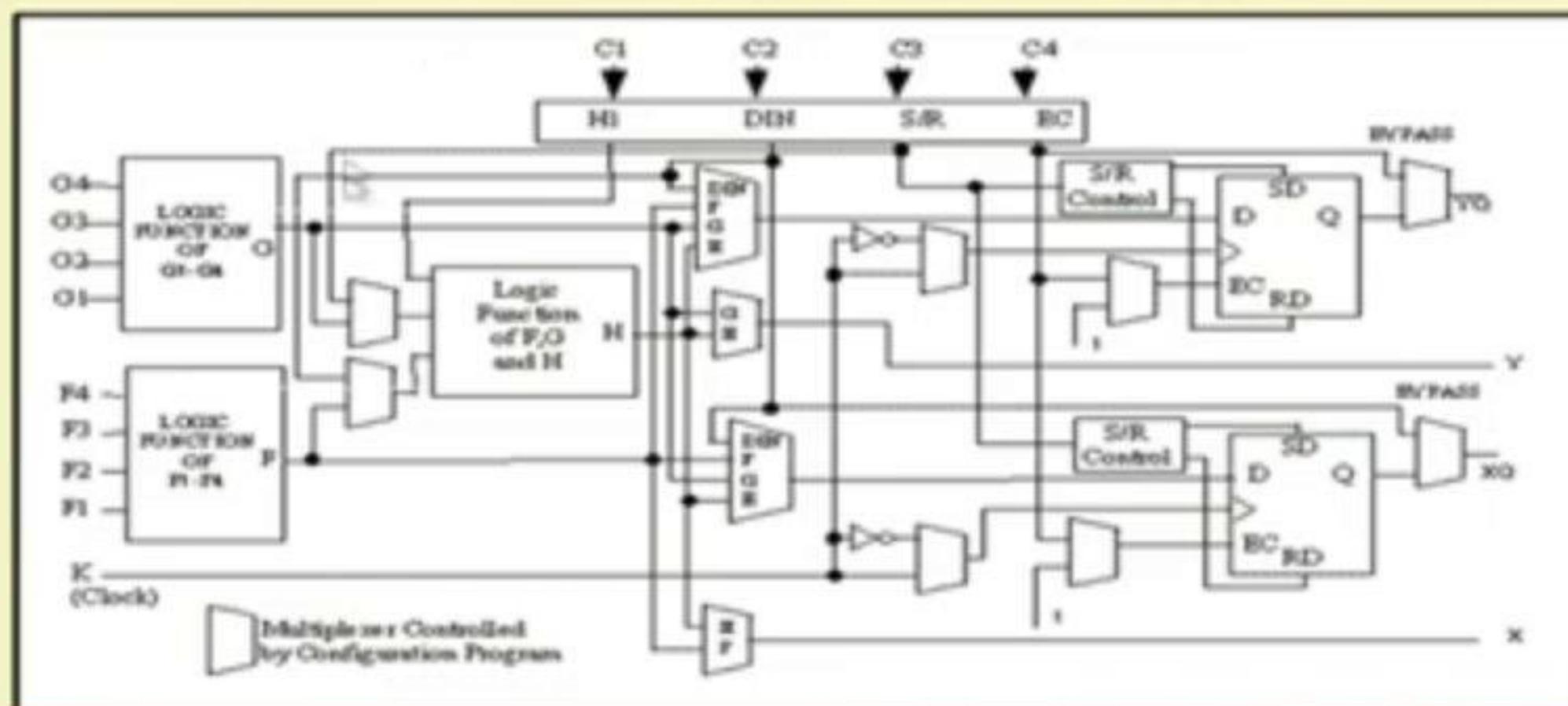
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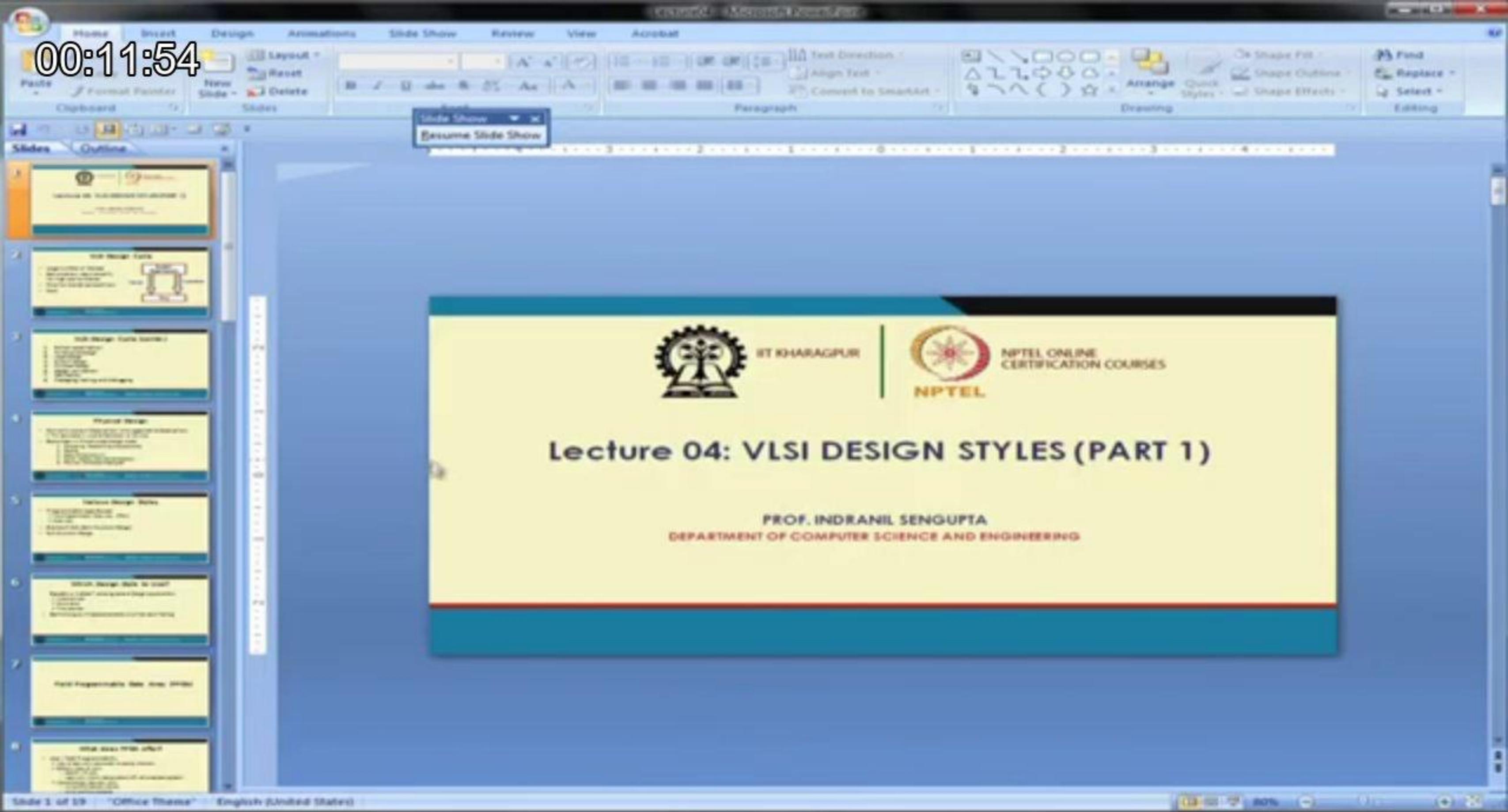
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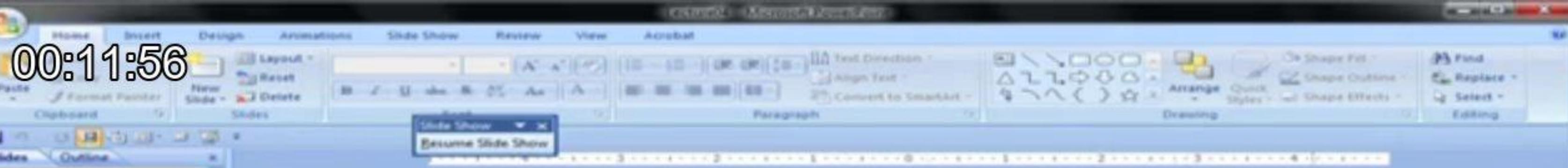


## XC4000E Configurable Logic Block



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Resume Slide Show

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## Lecture 04: VLSI DESIGN STYLES (PART 1)

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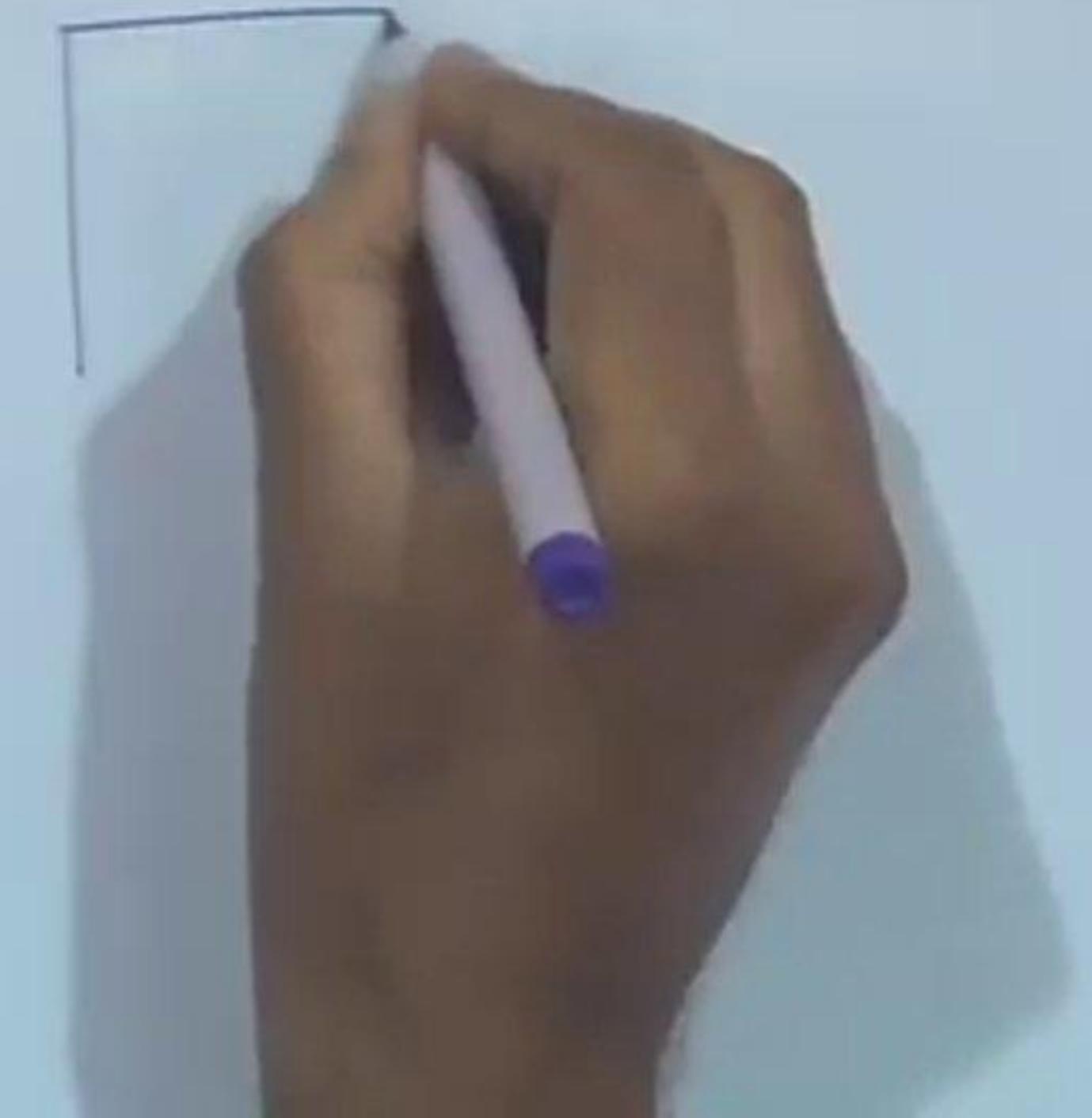


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16 X 1  
RAM

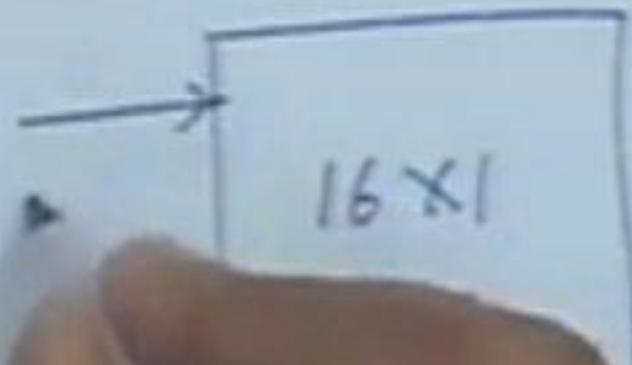


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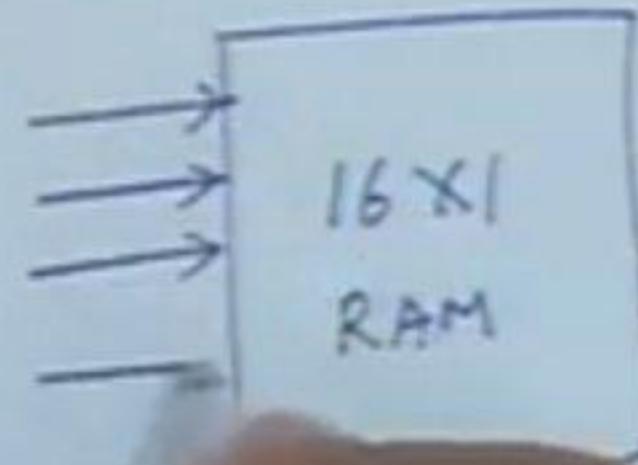
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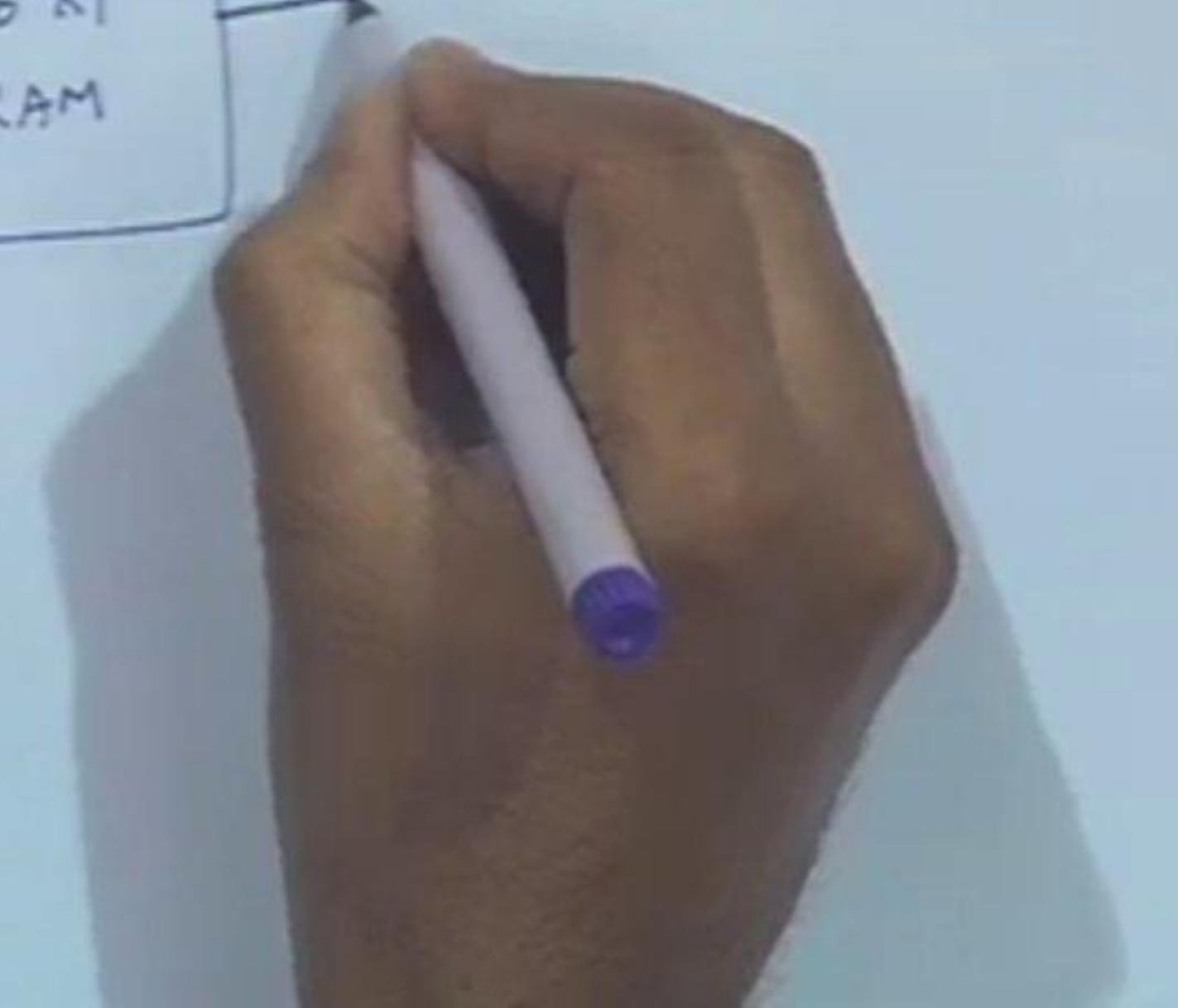
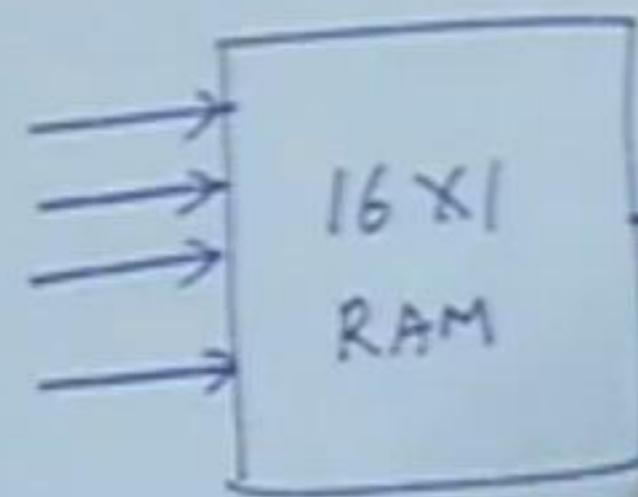
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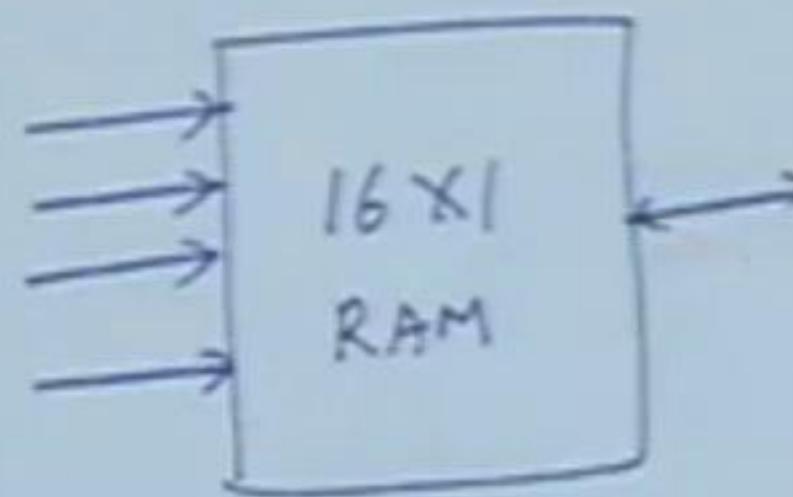
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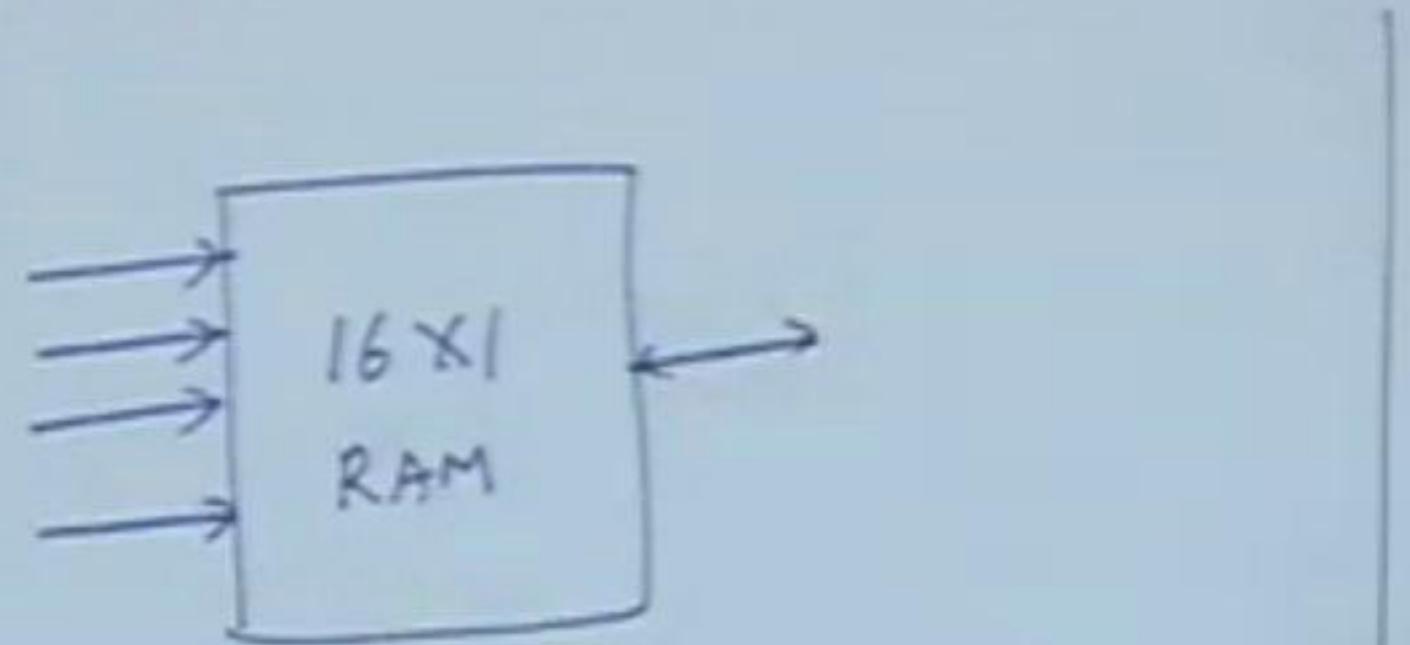
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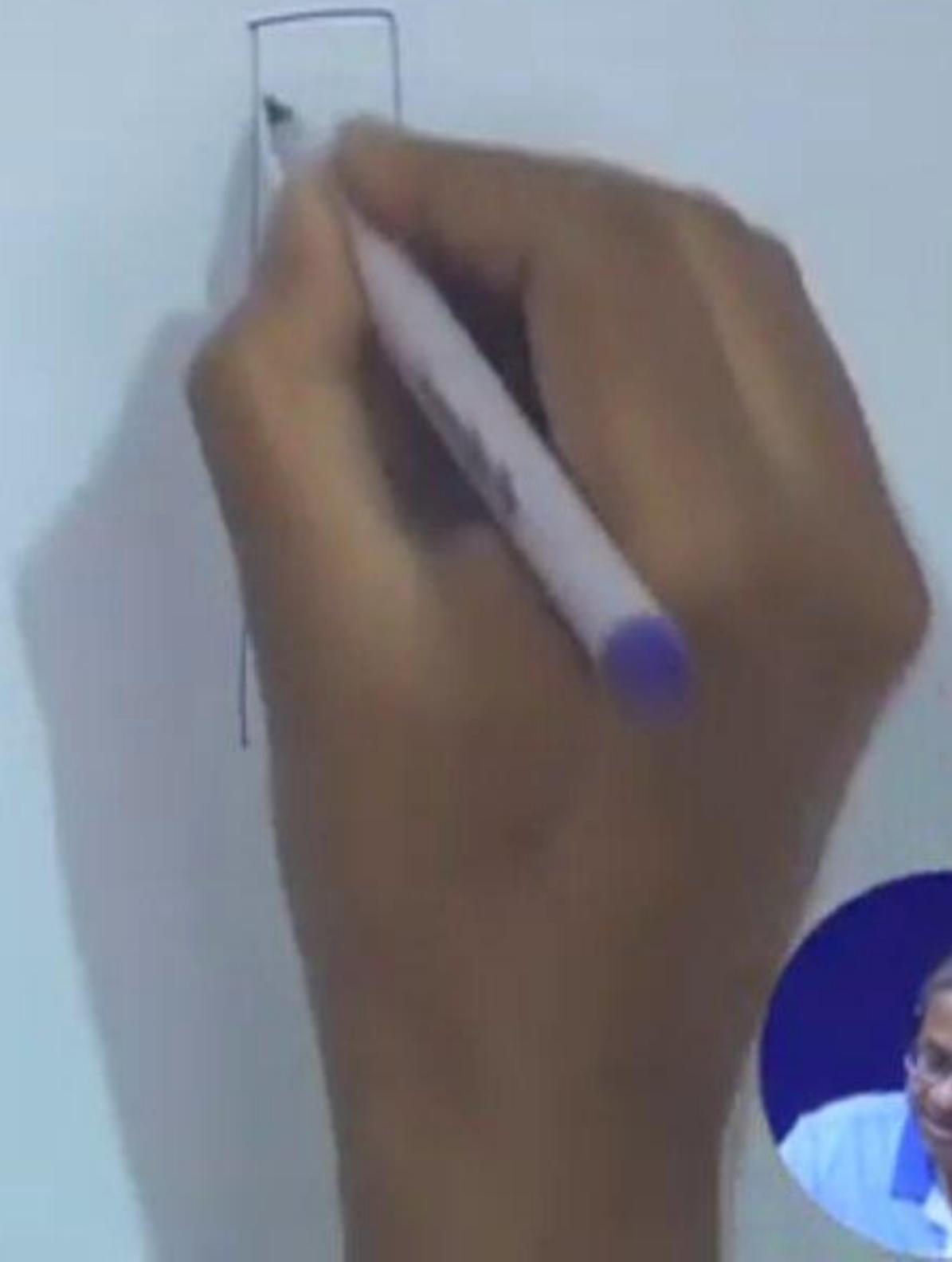
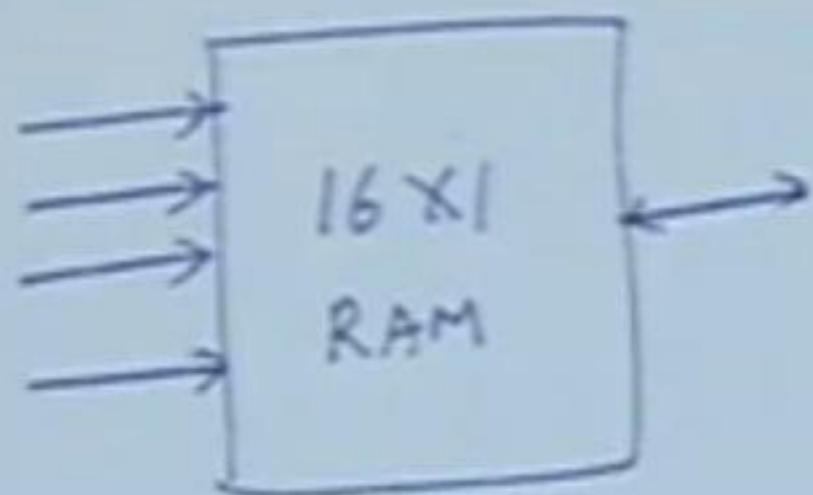
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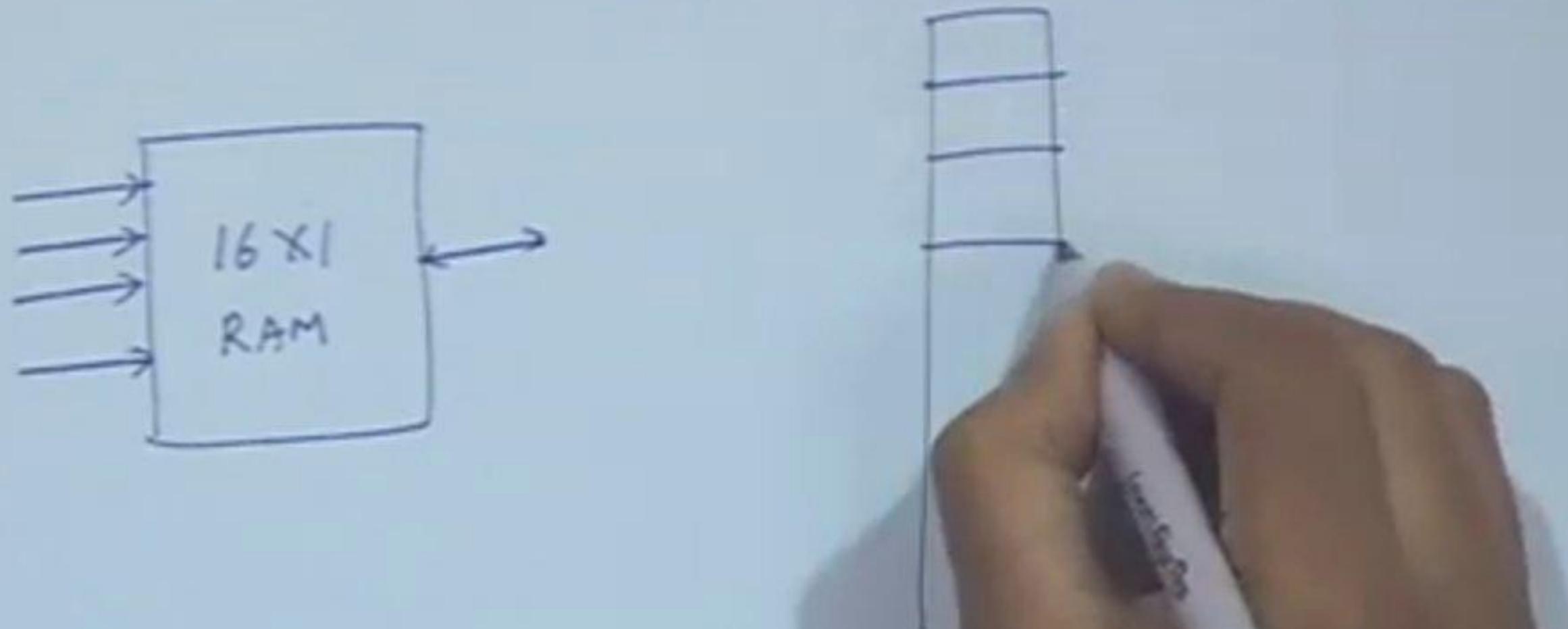
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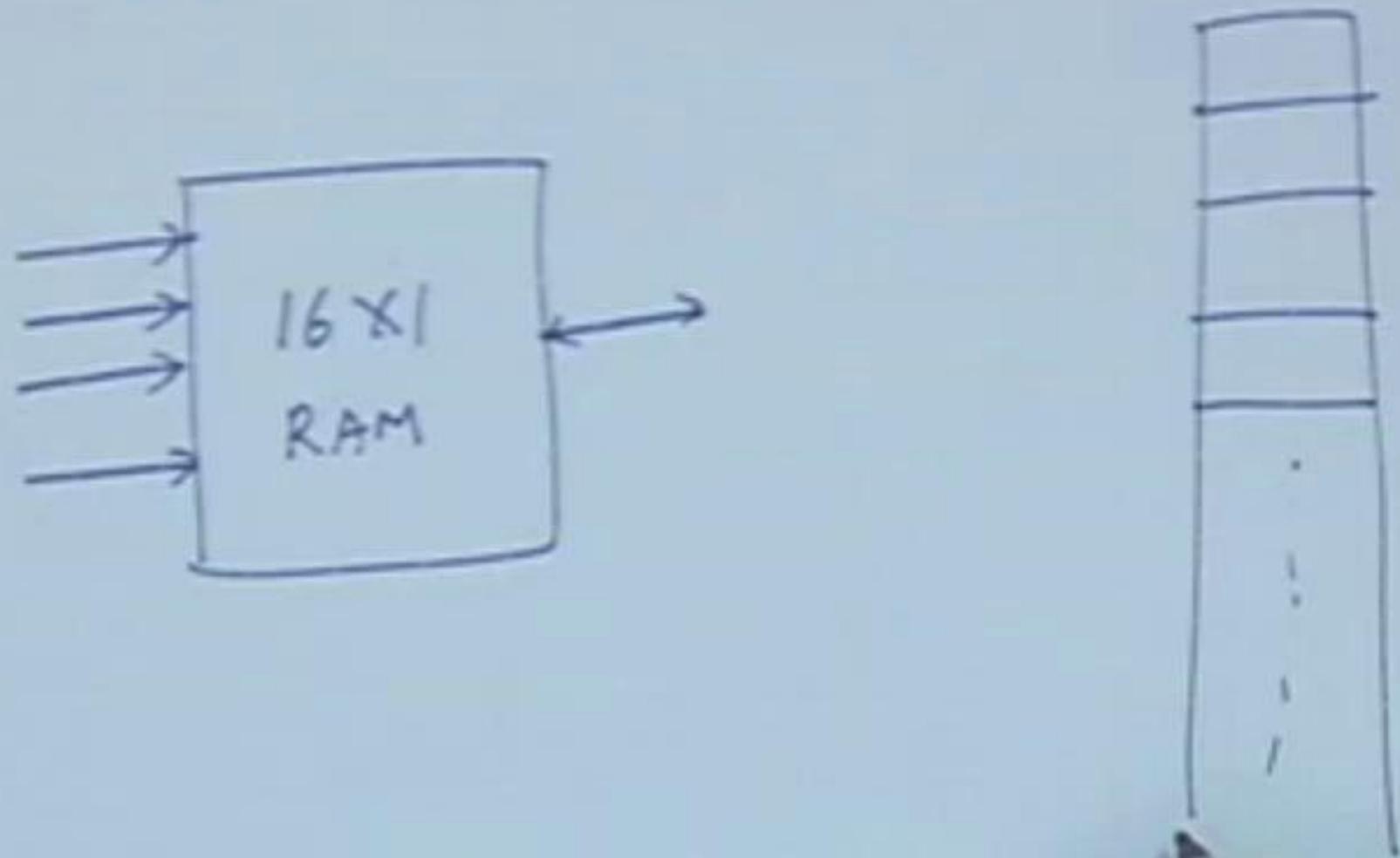
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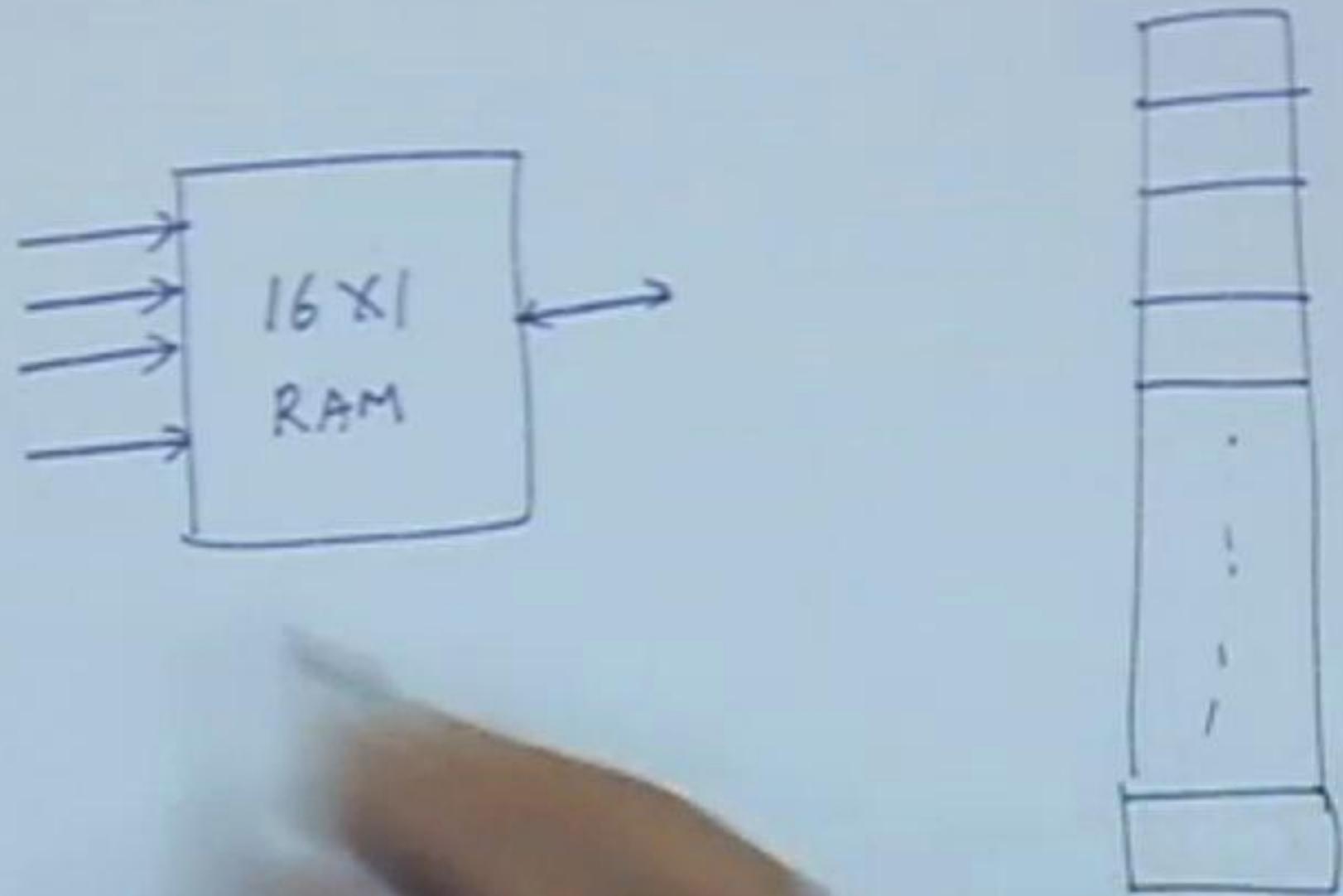
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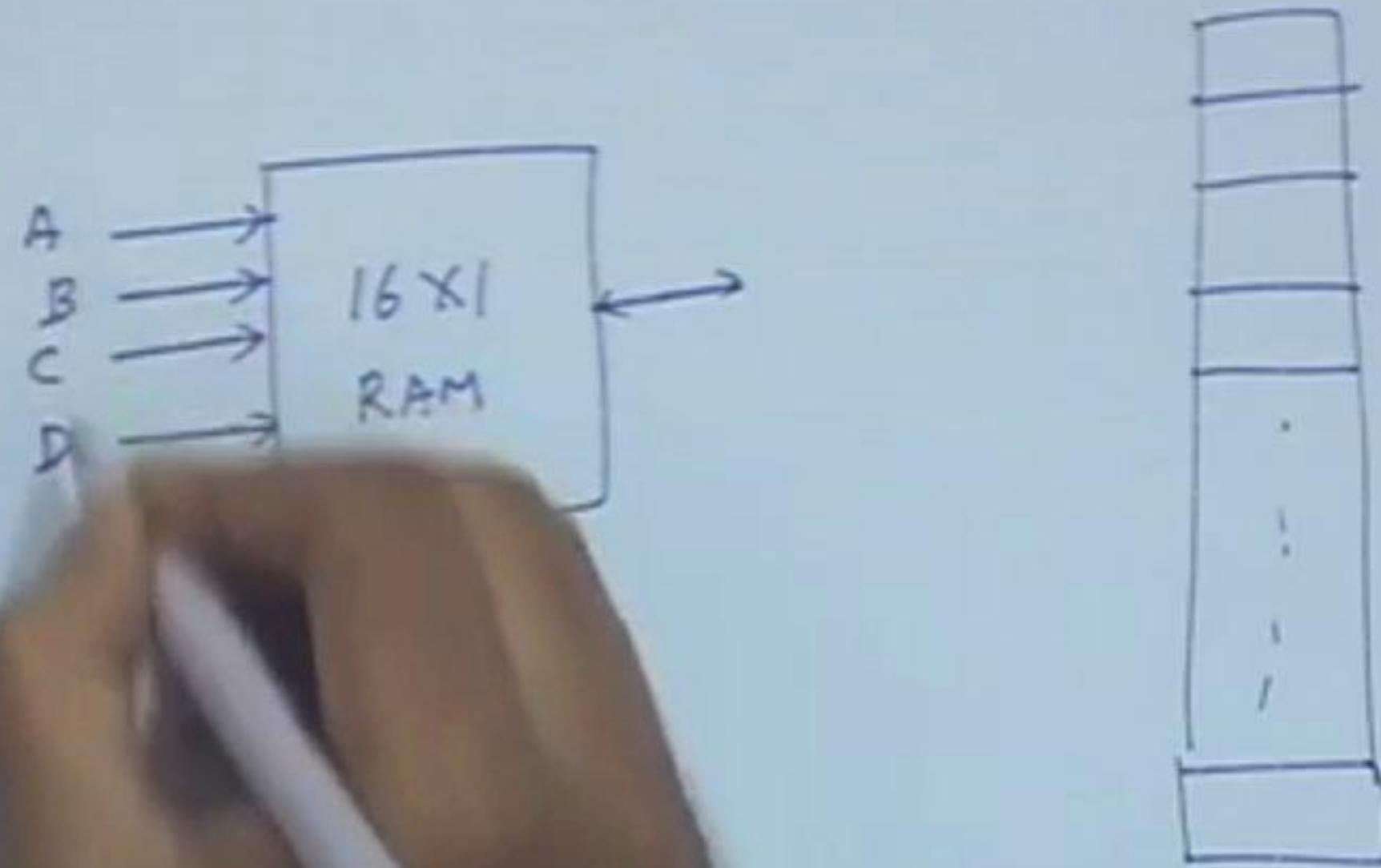
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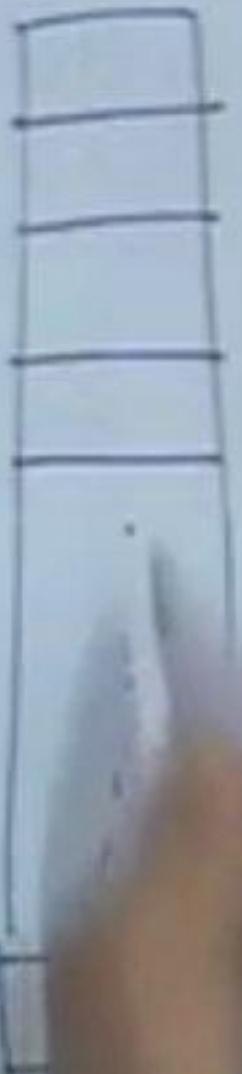
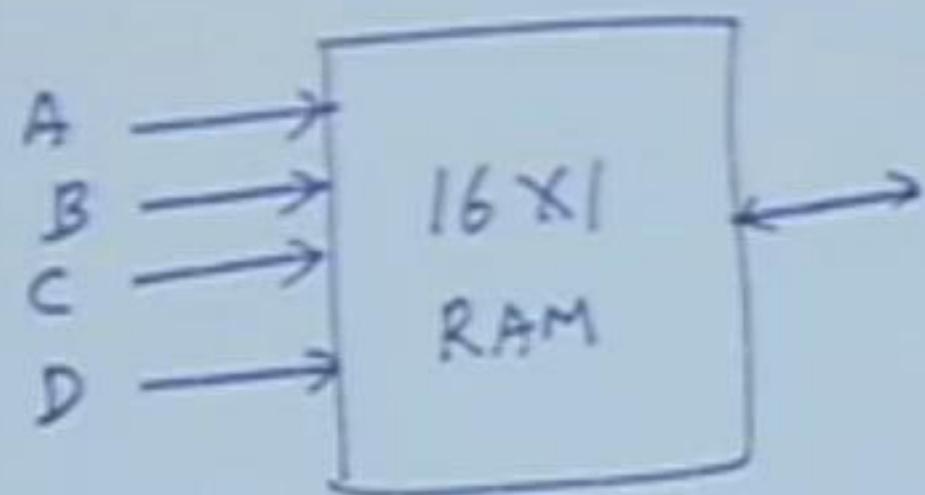
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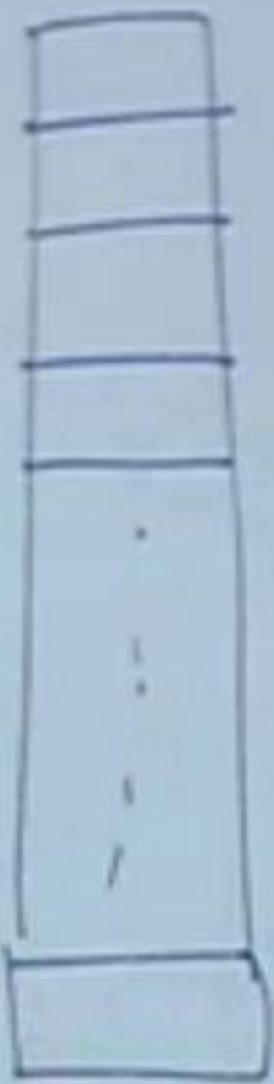
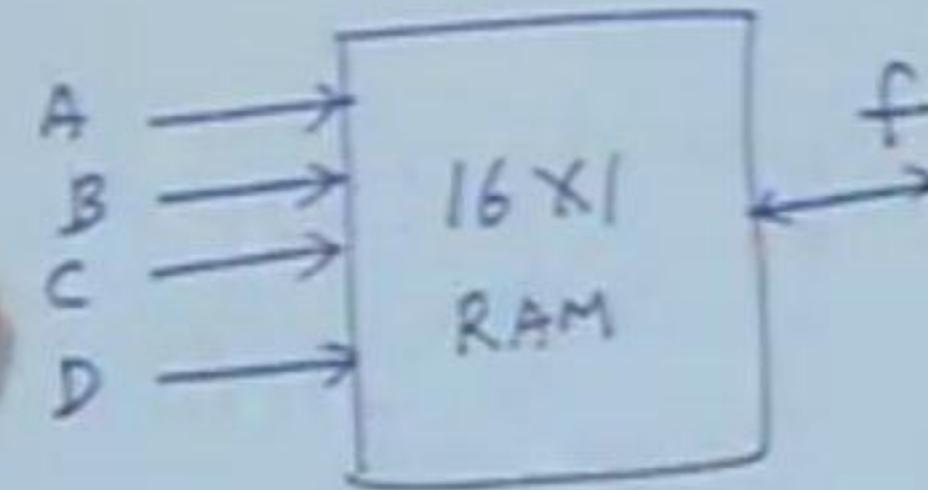
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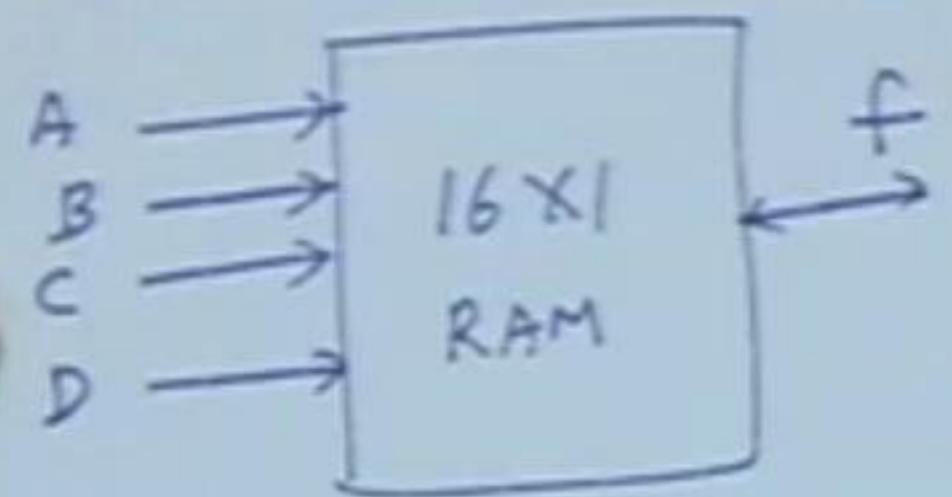
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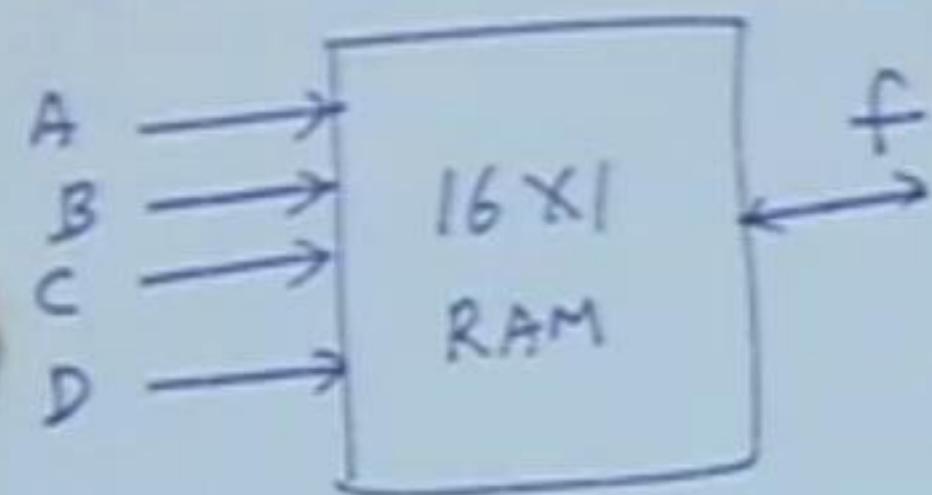
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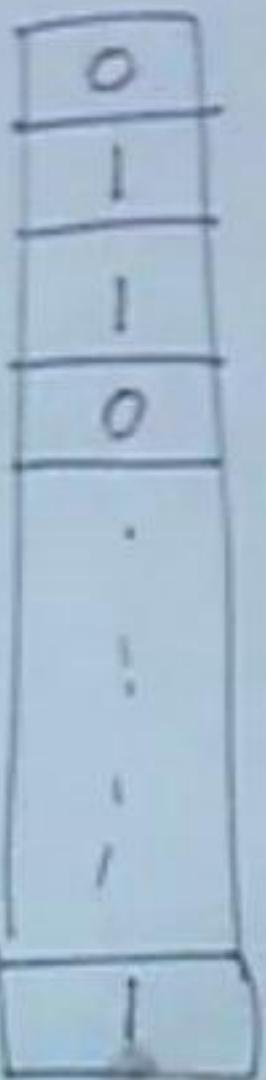
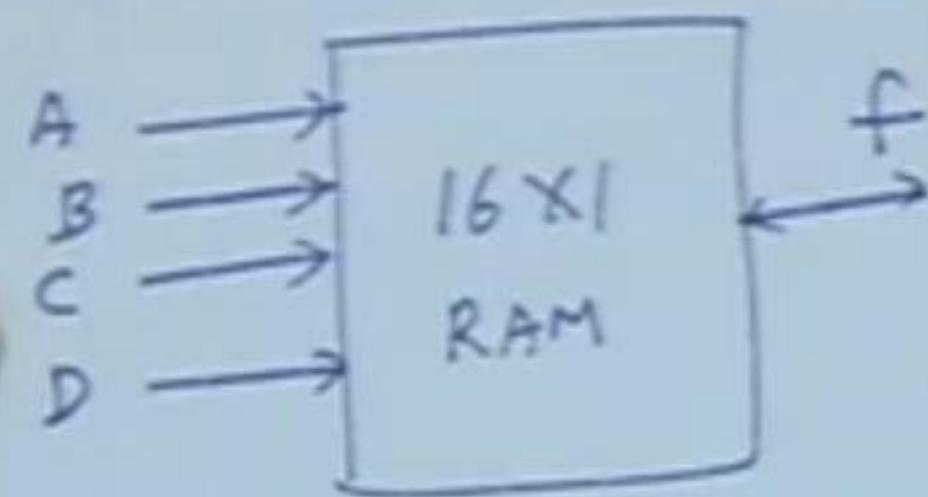
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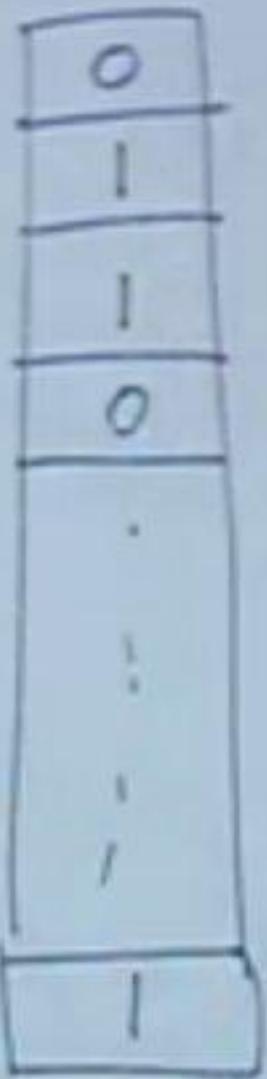
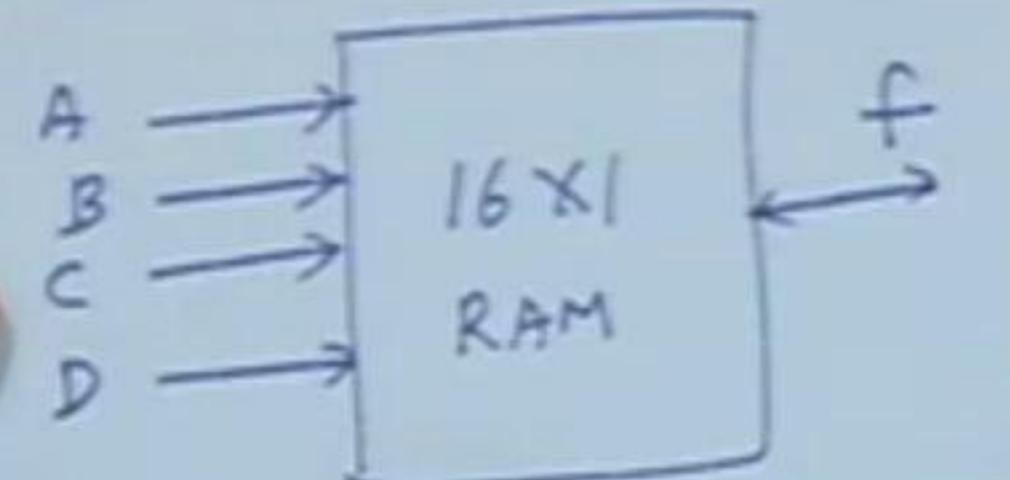
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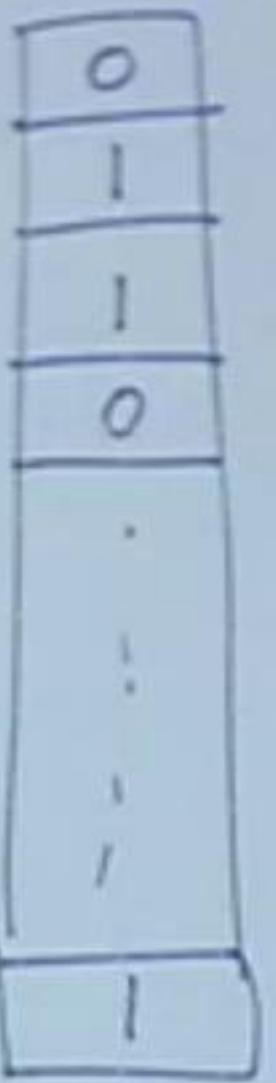
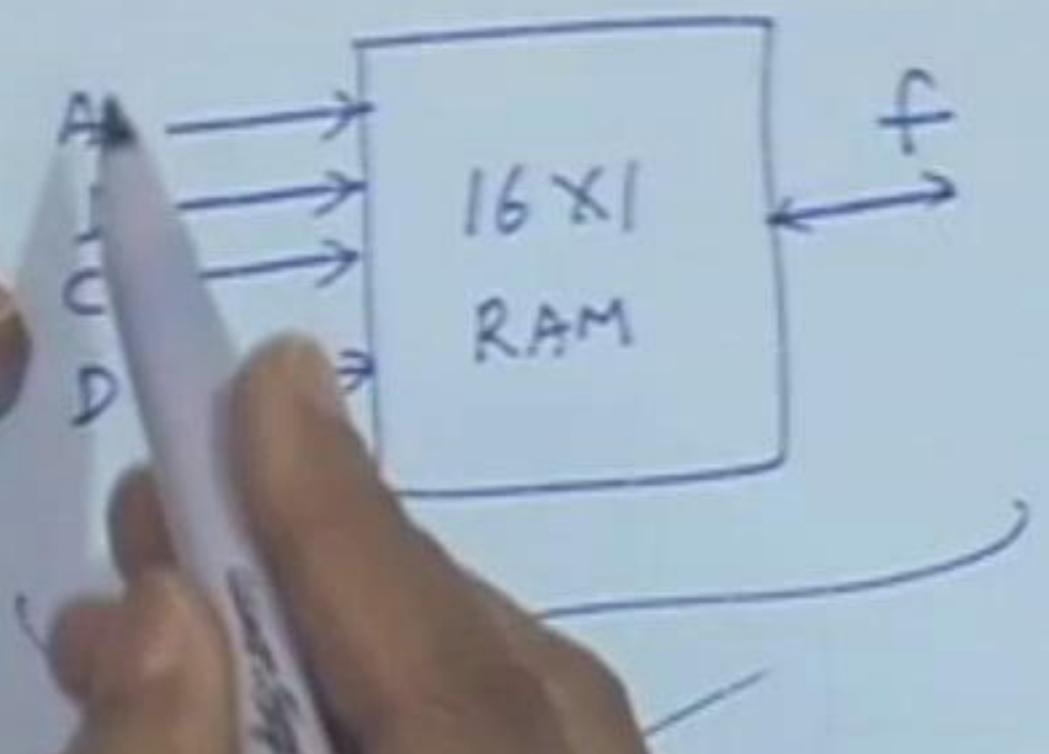
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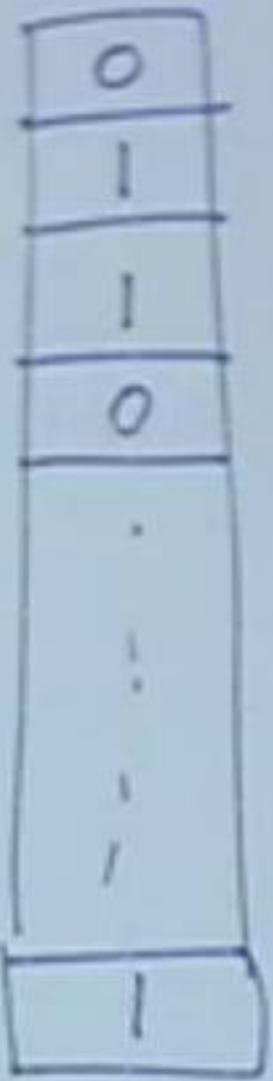
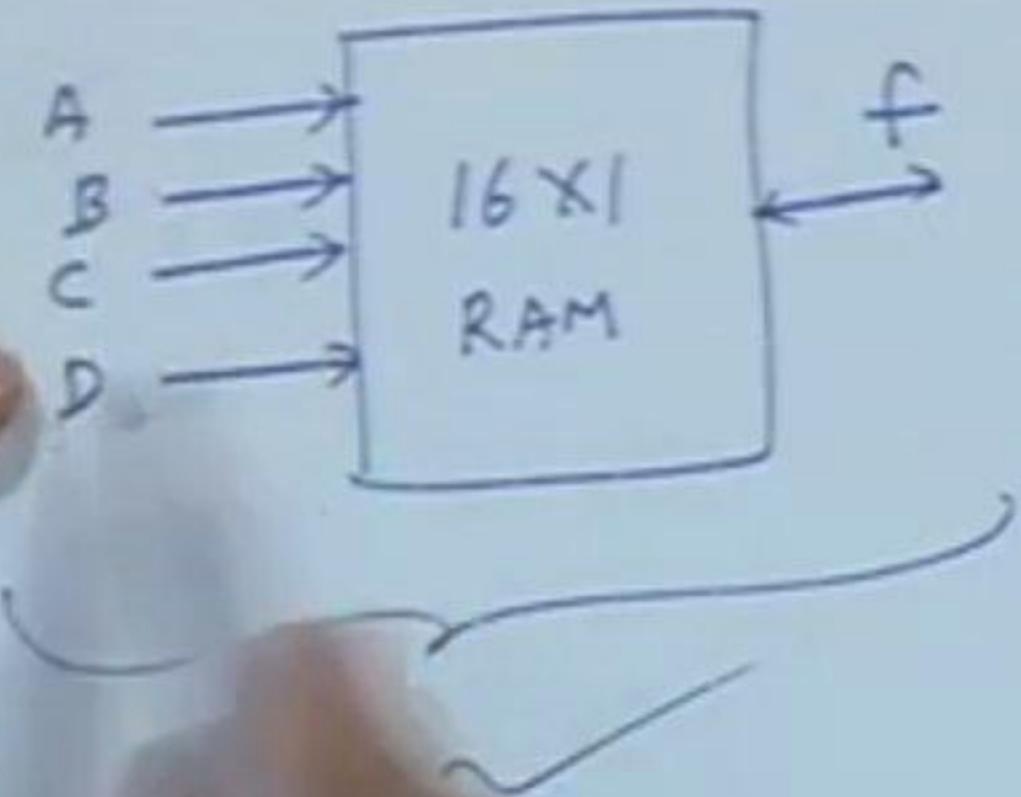
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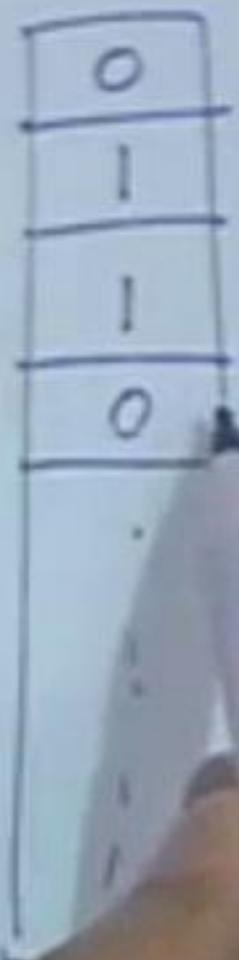
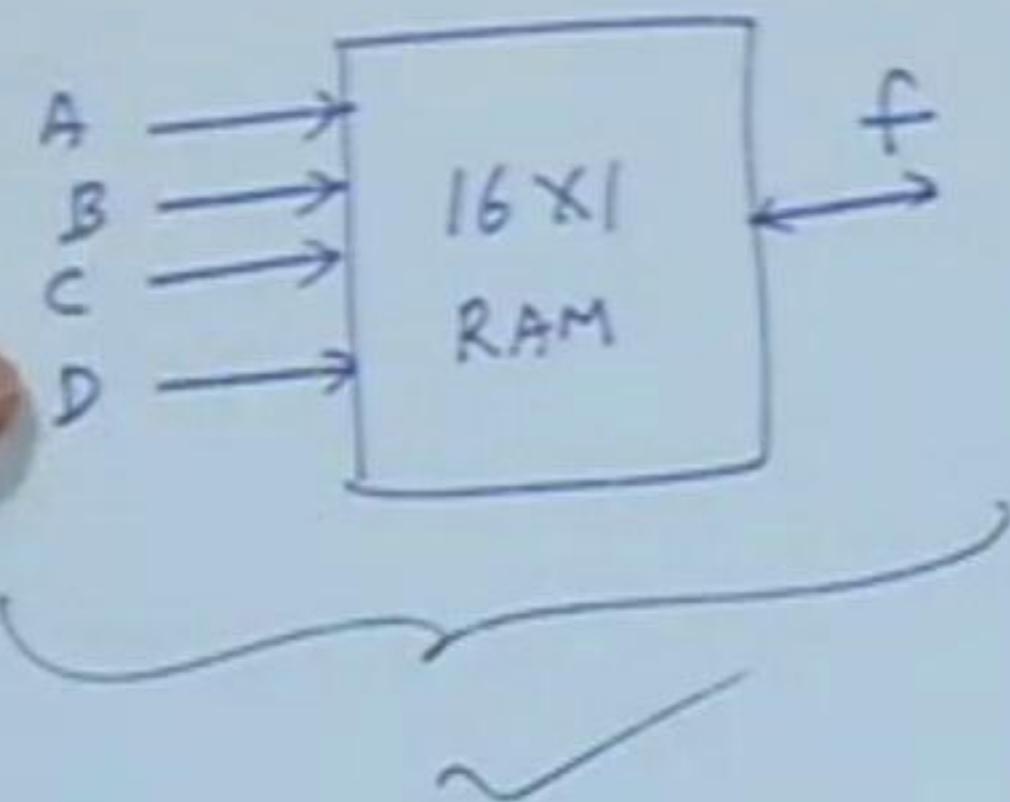
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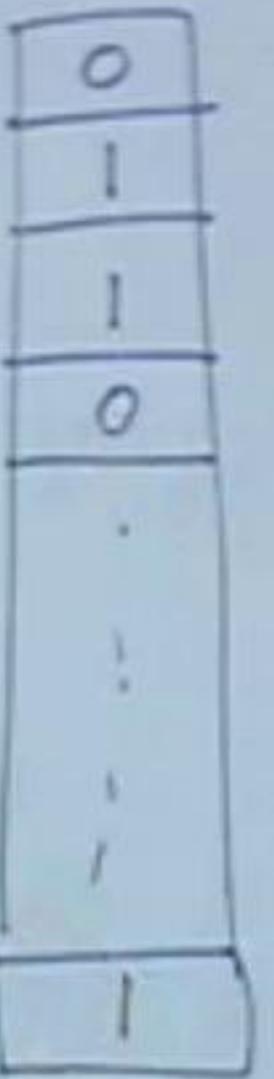
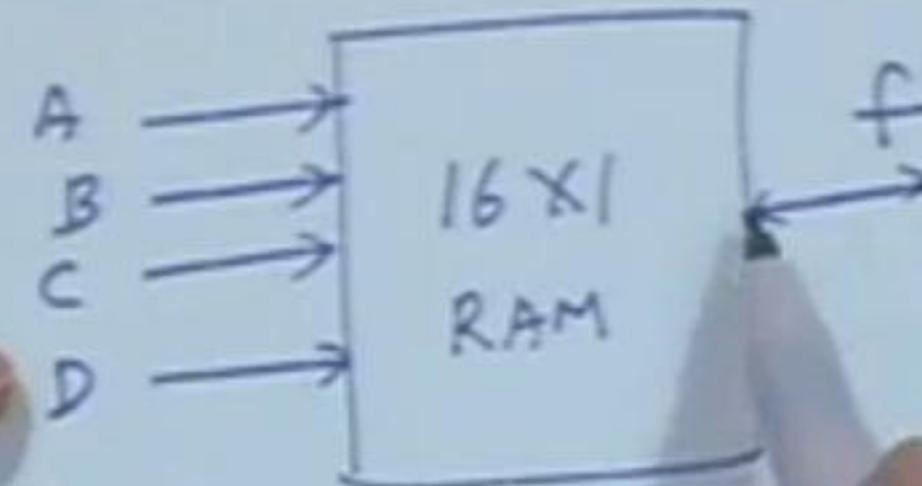
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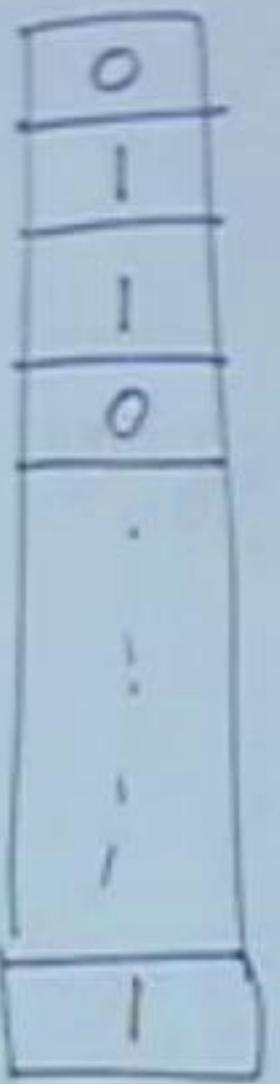
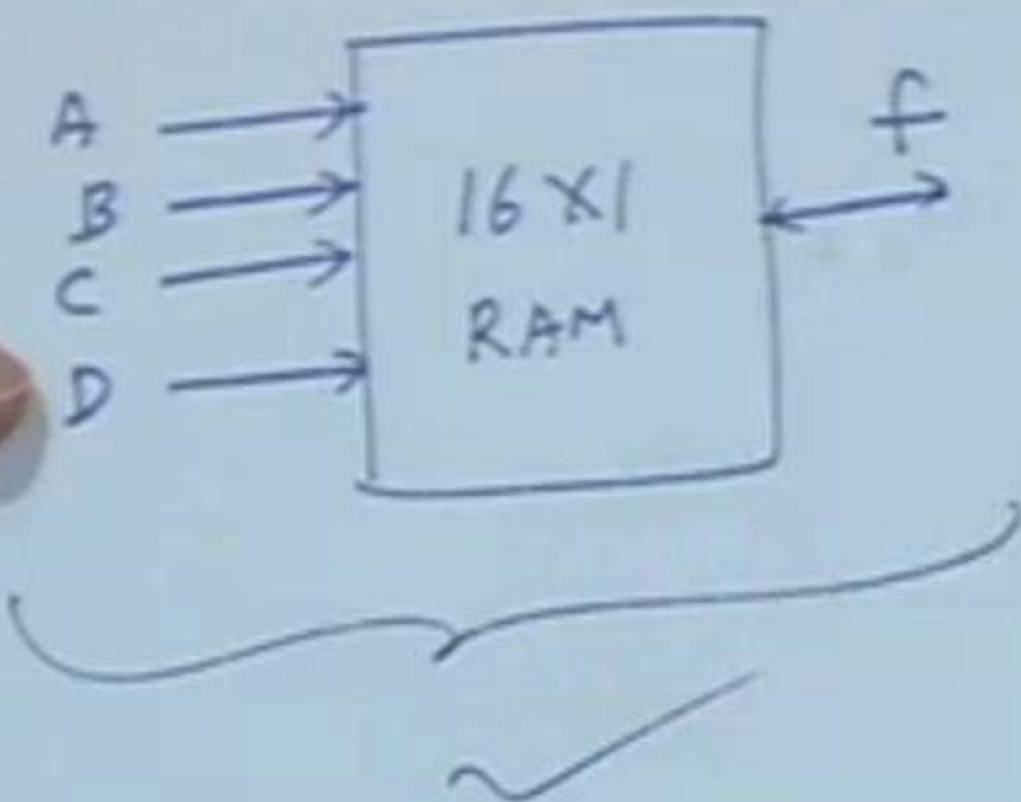
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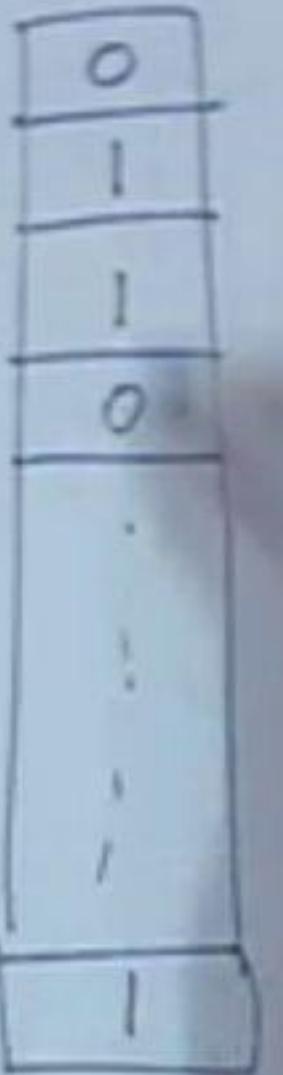
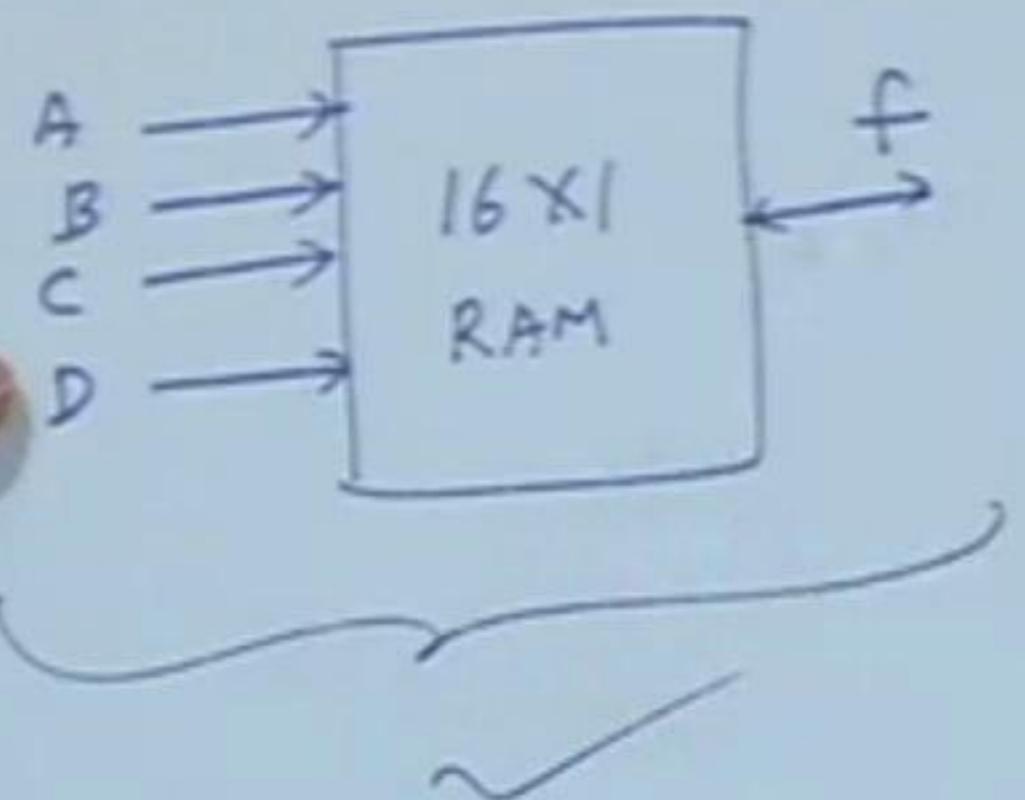
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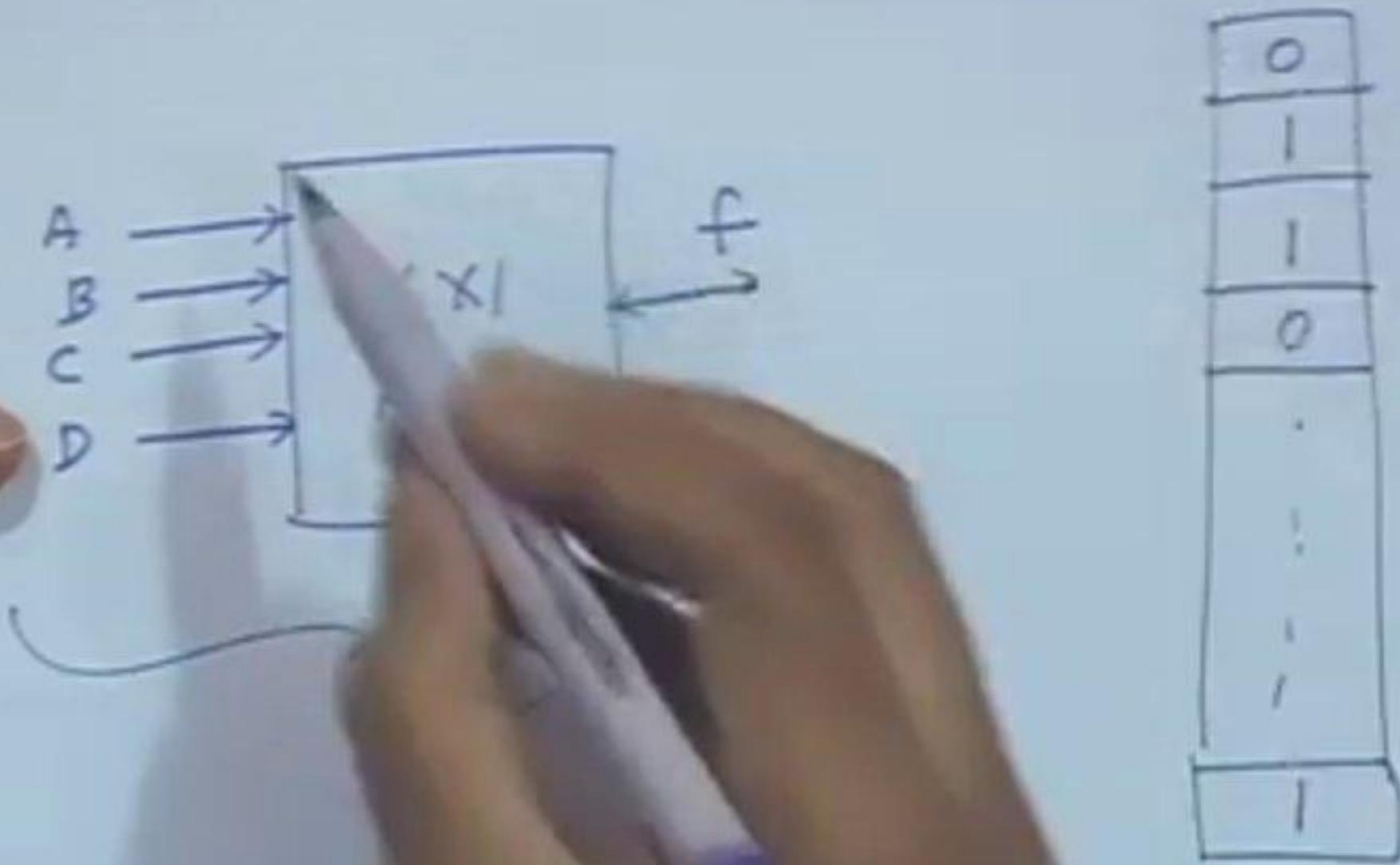
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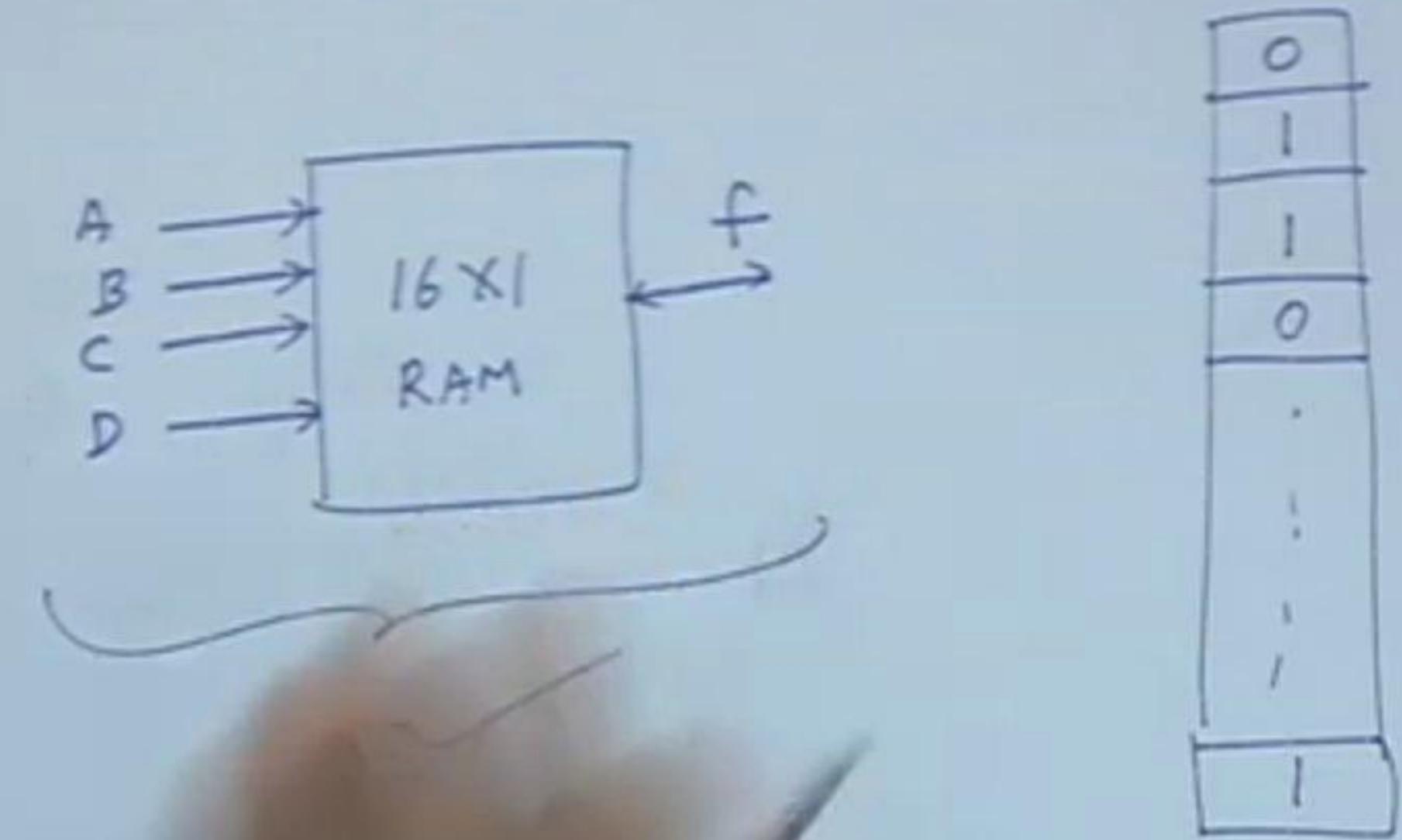
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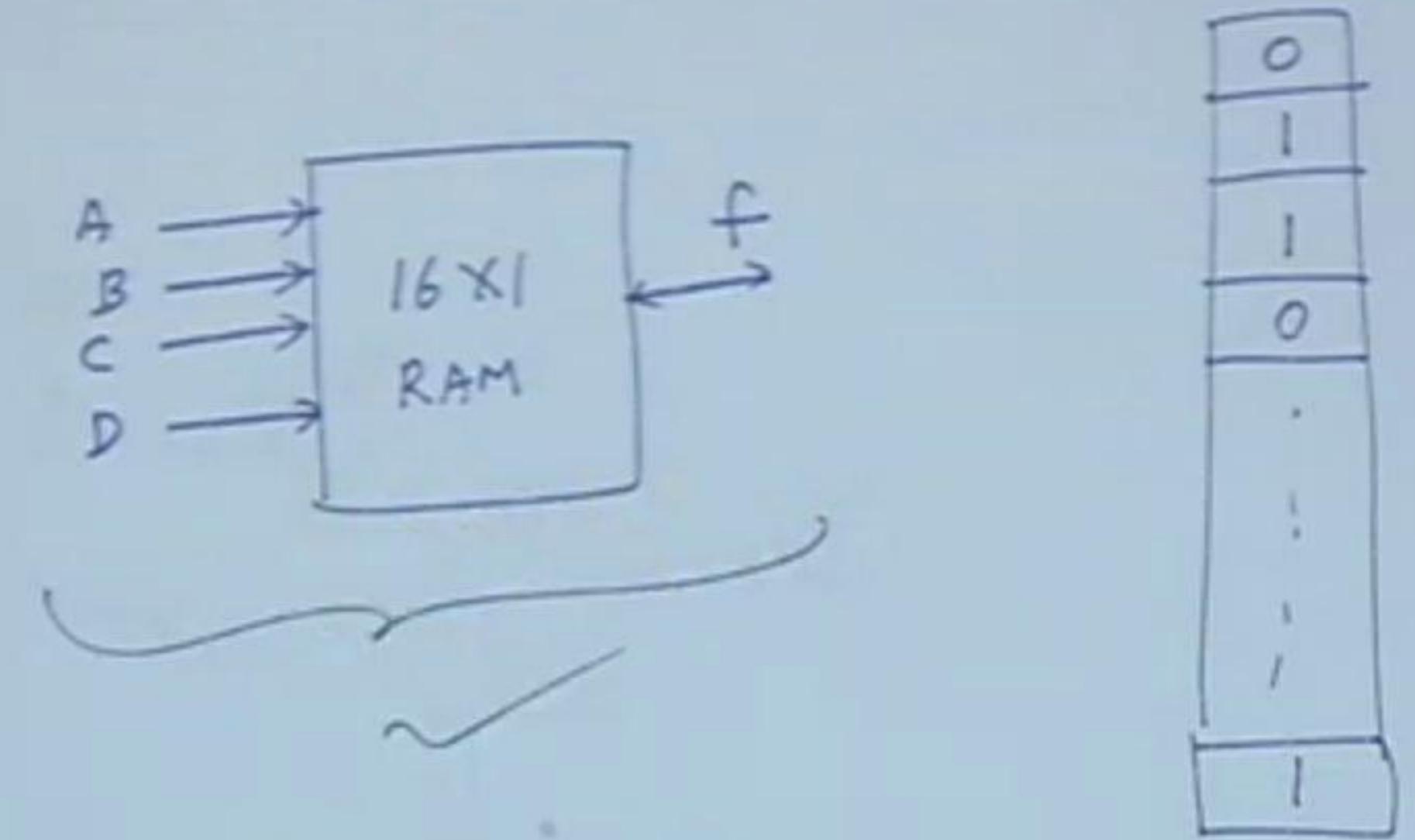
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00:14:10



00:14:12

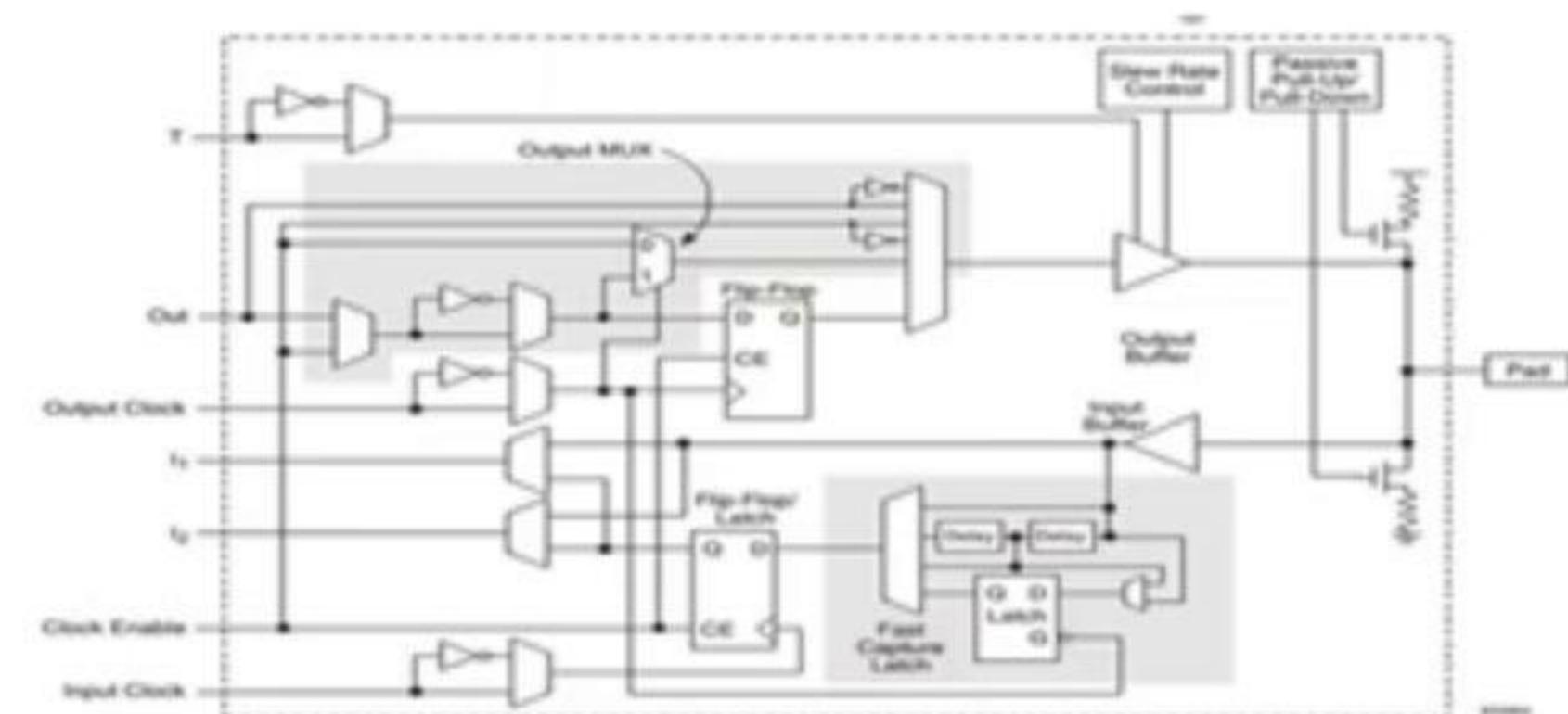


00:14:16



00:17:26

## XC4000X I/O Block Diagram



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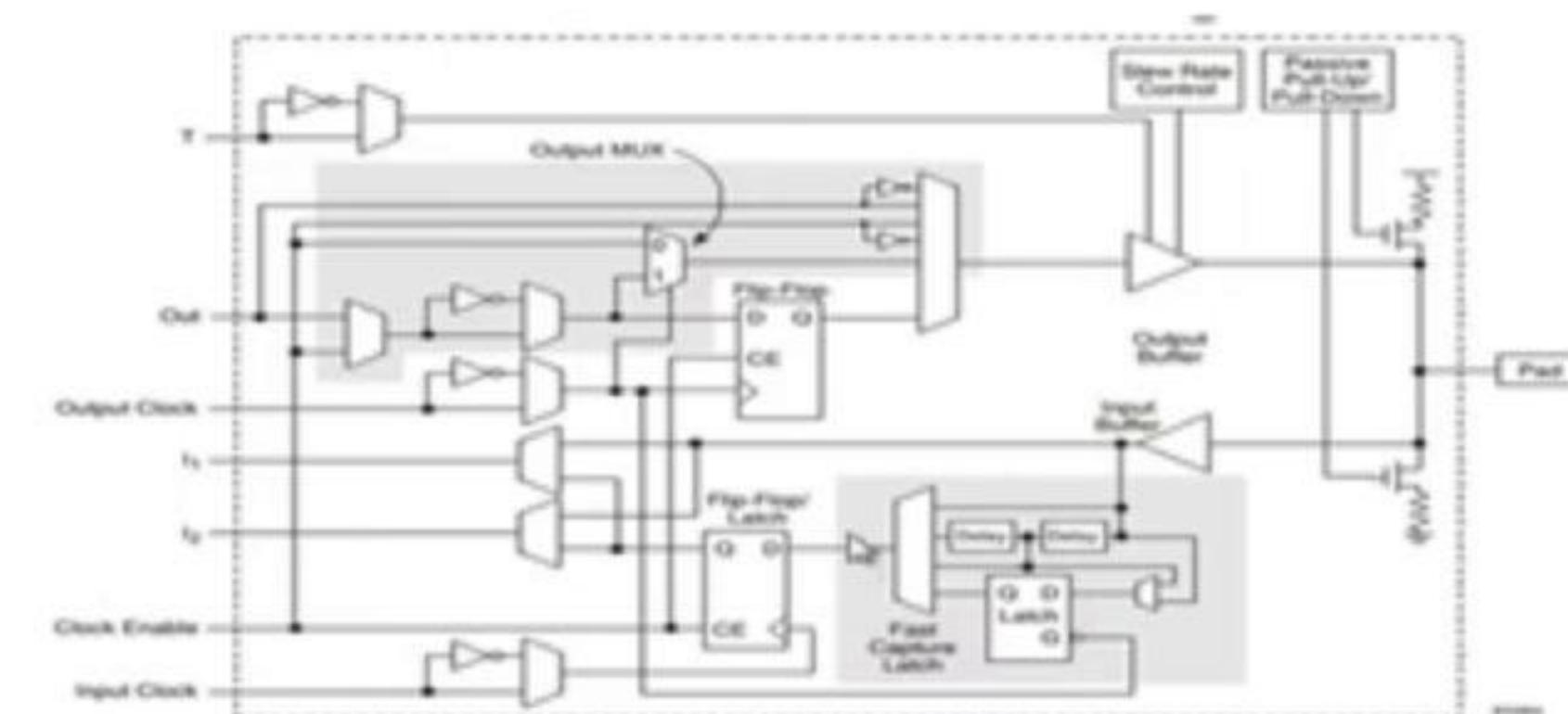


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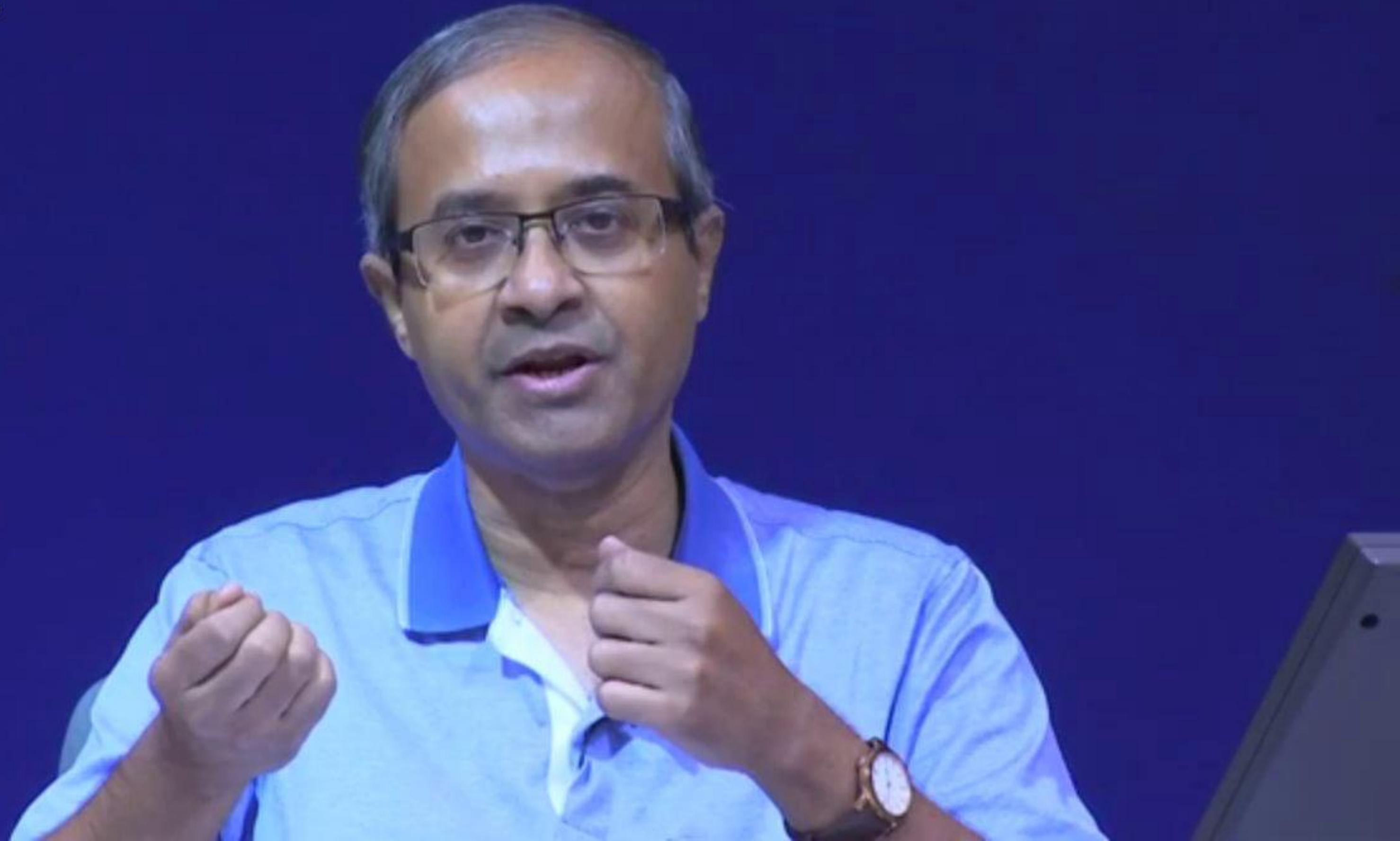
Hardware Modeling Using Verilog



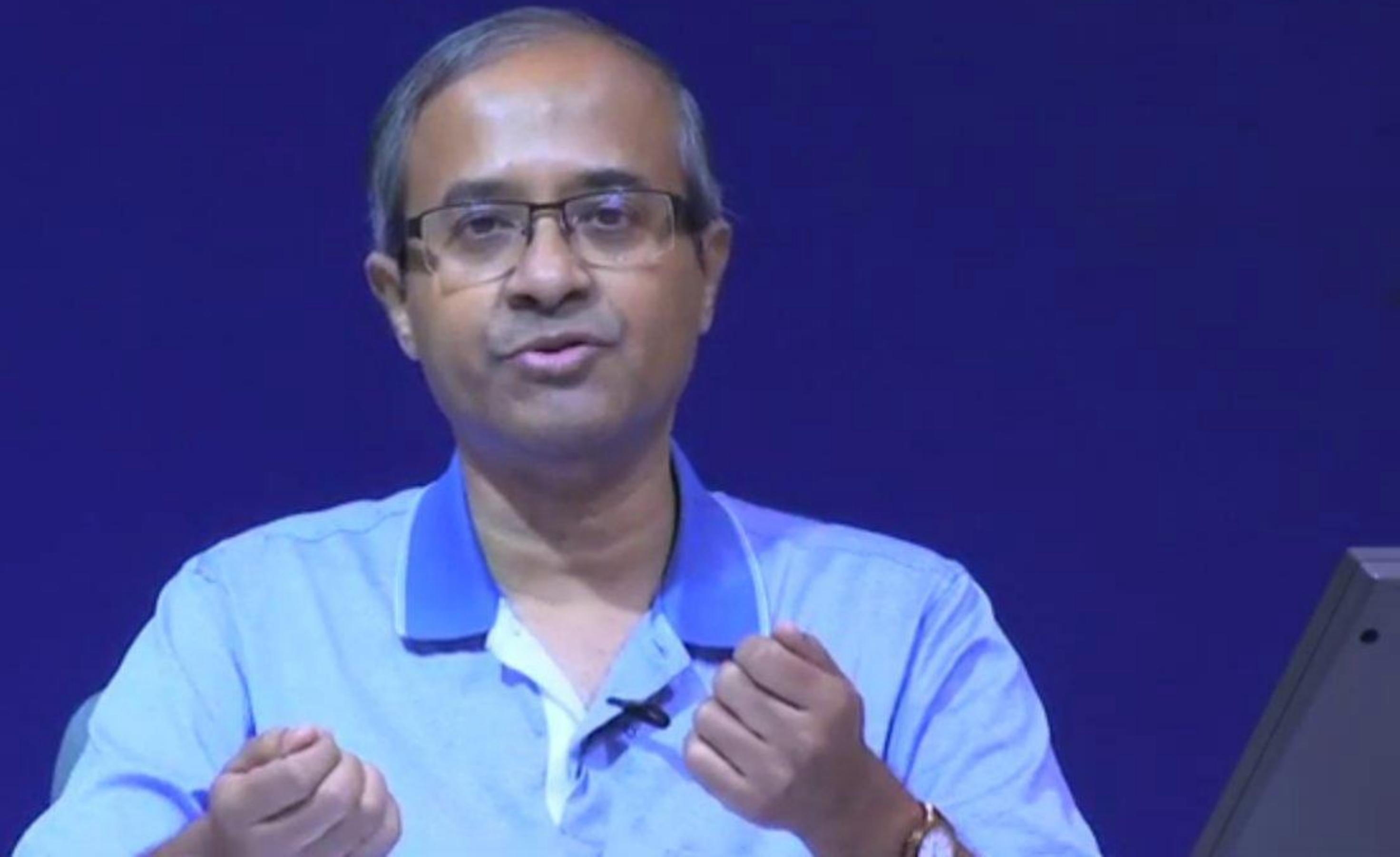
# XC4000X I/O Block Diagram



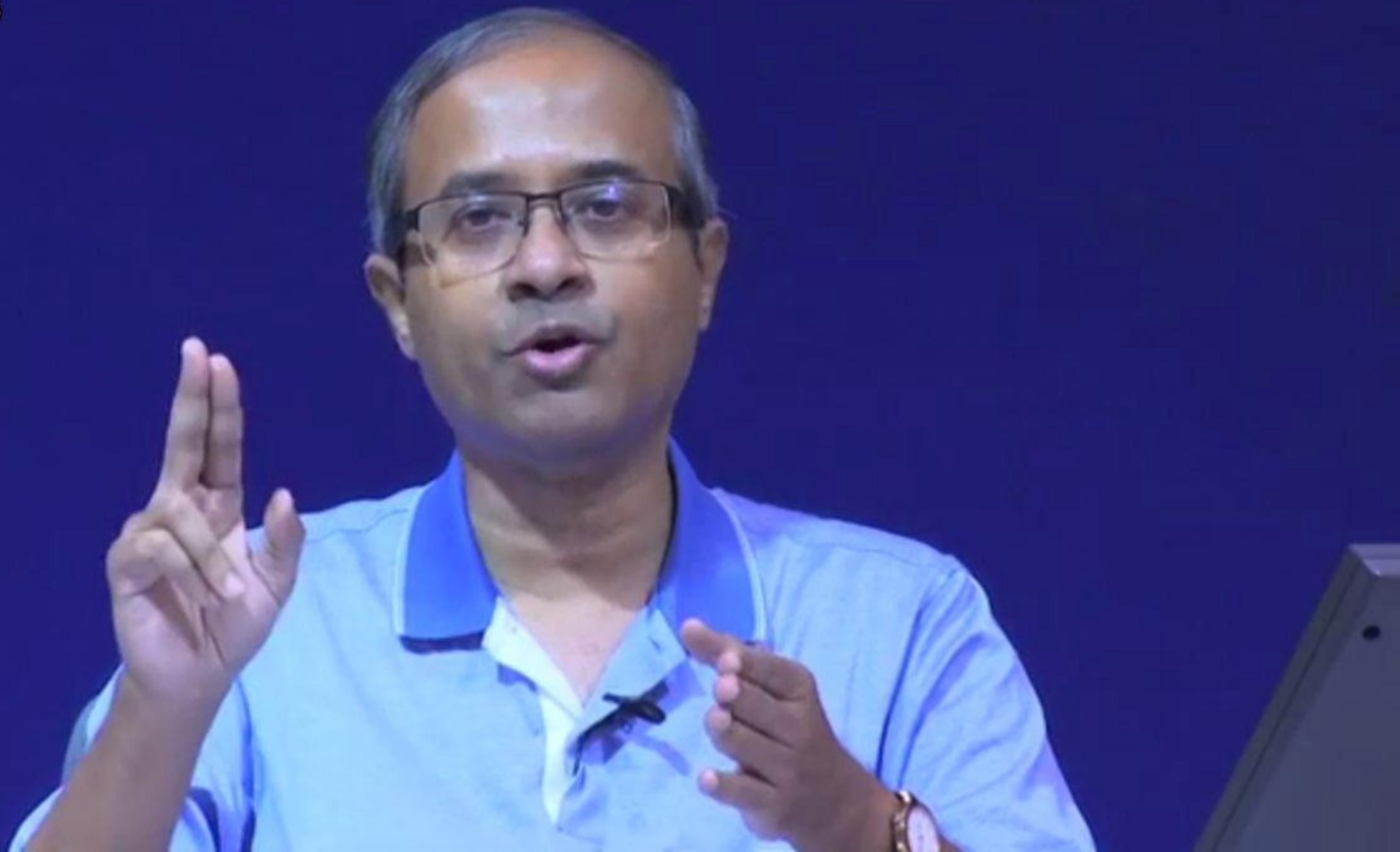
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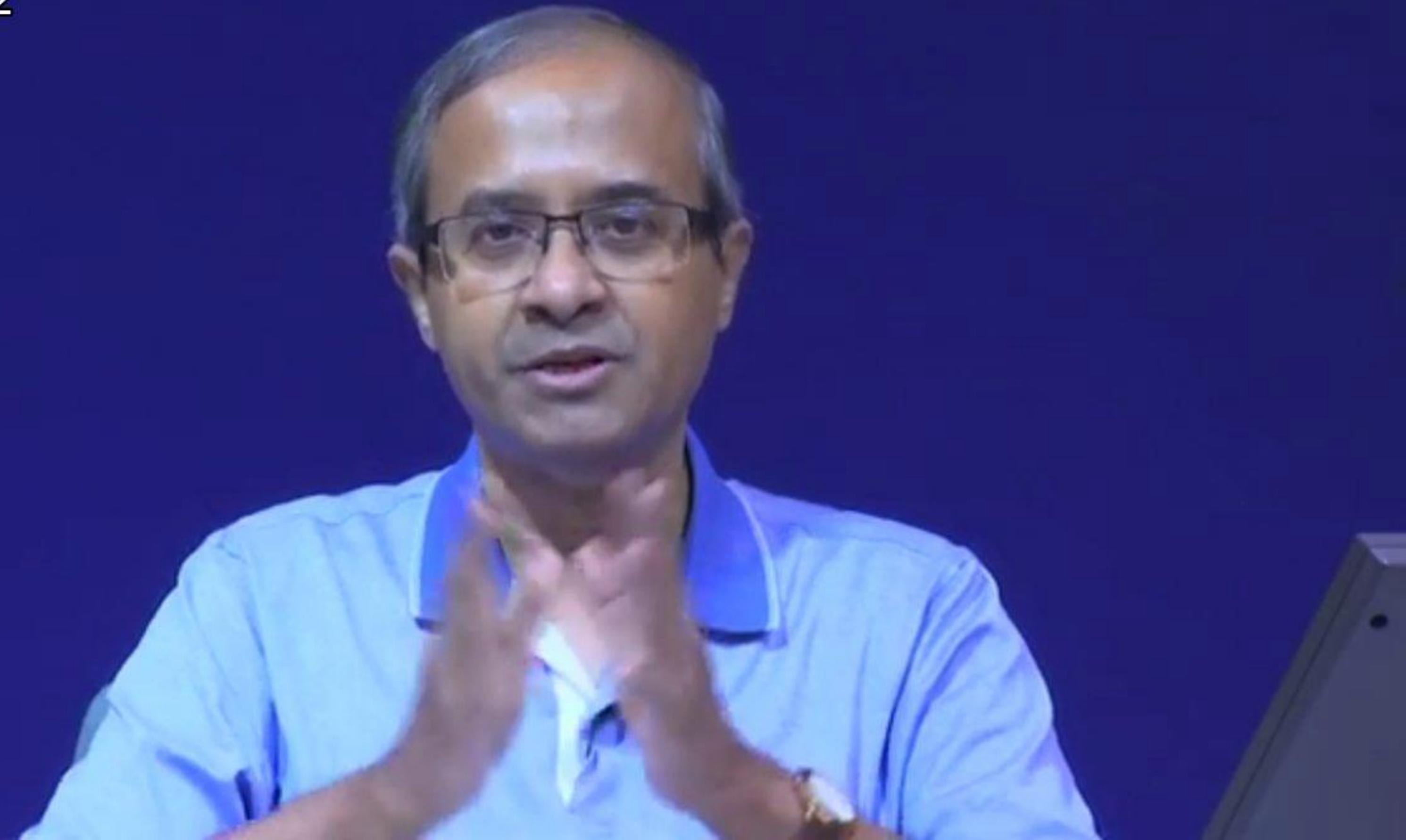
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00:17:58



00:18:02



00:18:10



00:18:12

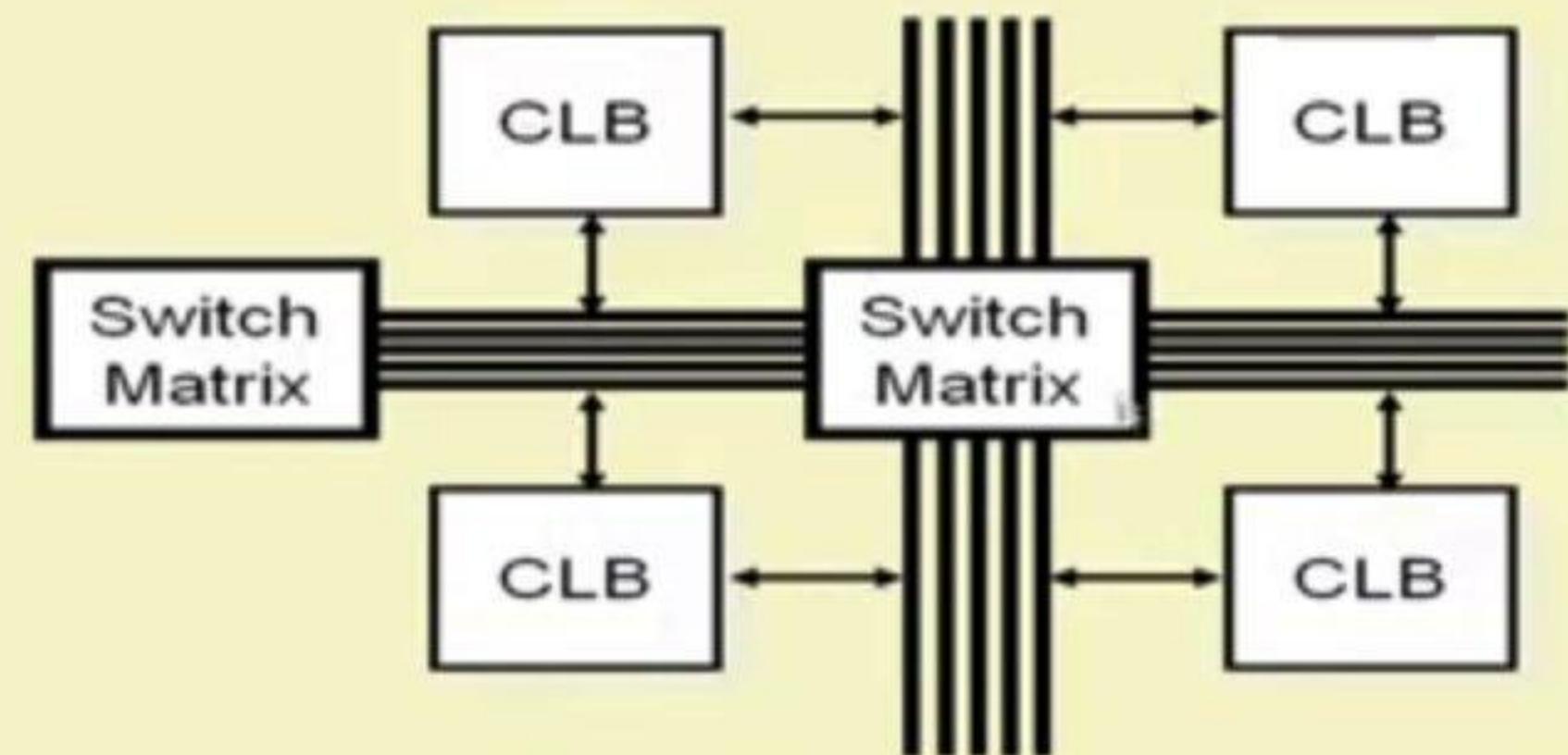


00:18:14



## Xilinx FPGA Routing

1. Fast Direct Interconnect – CLB to CLB
2. General Purpose Interconnect – Uses switch matrix



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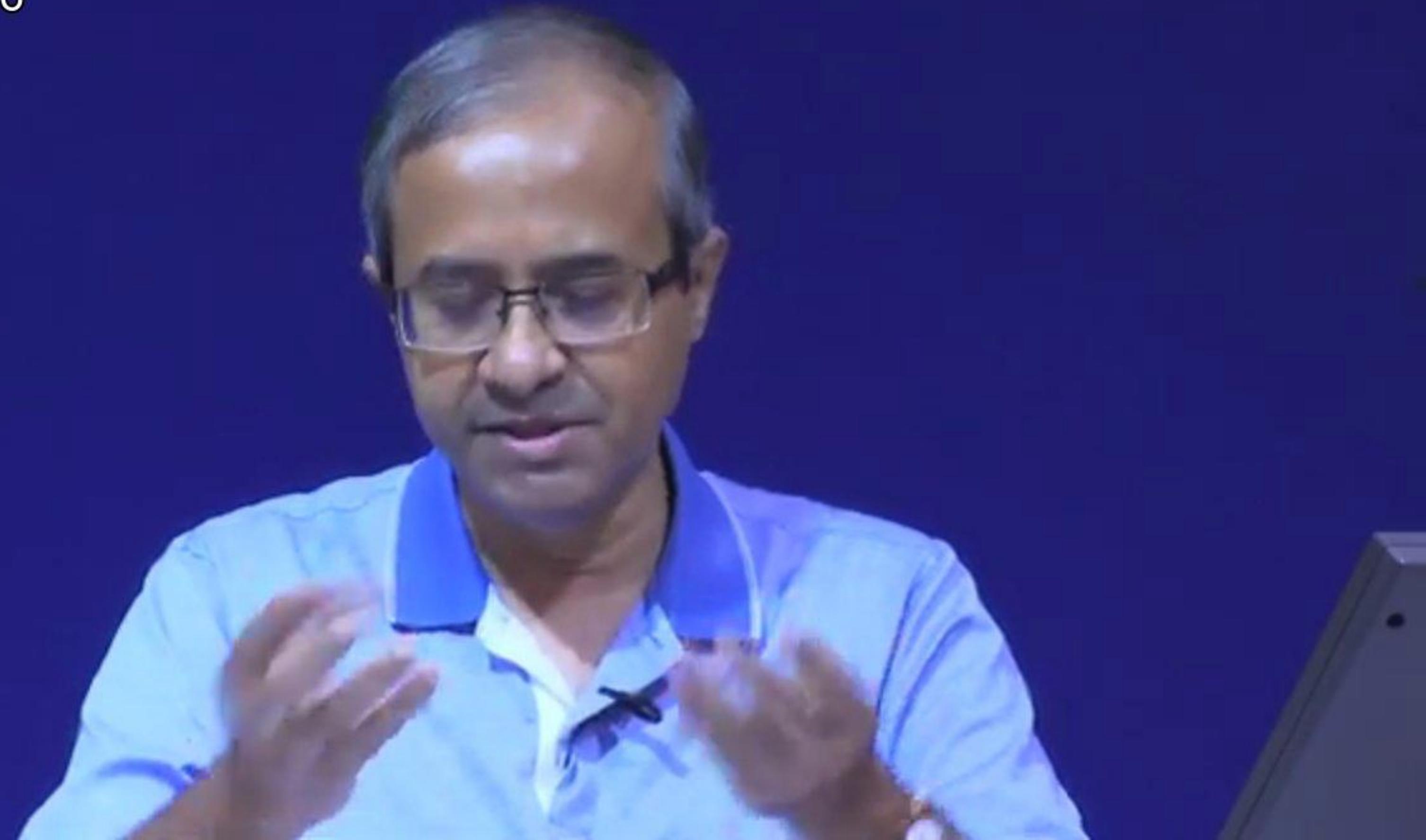
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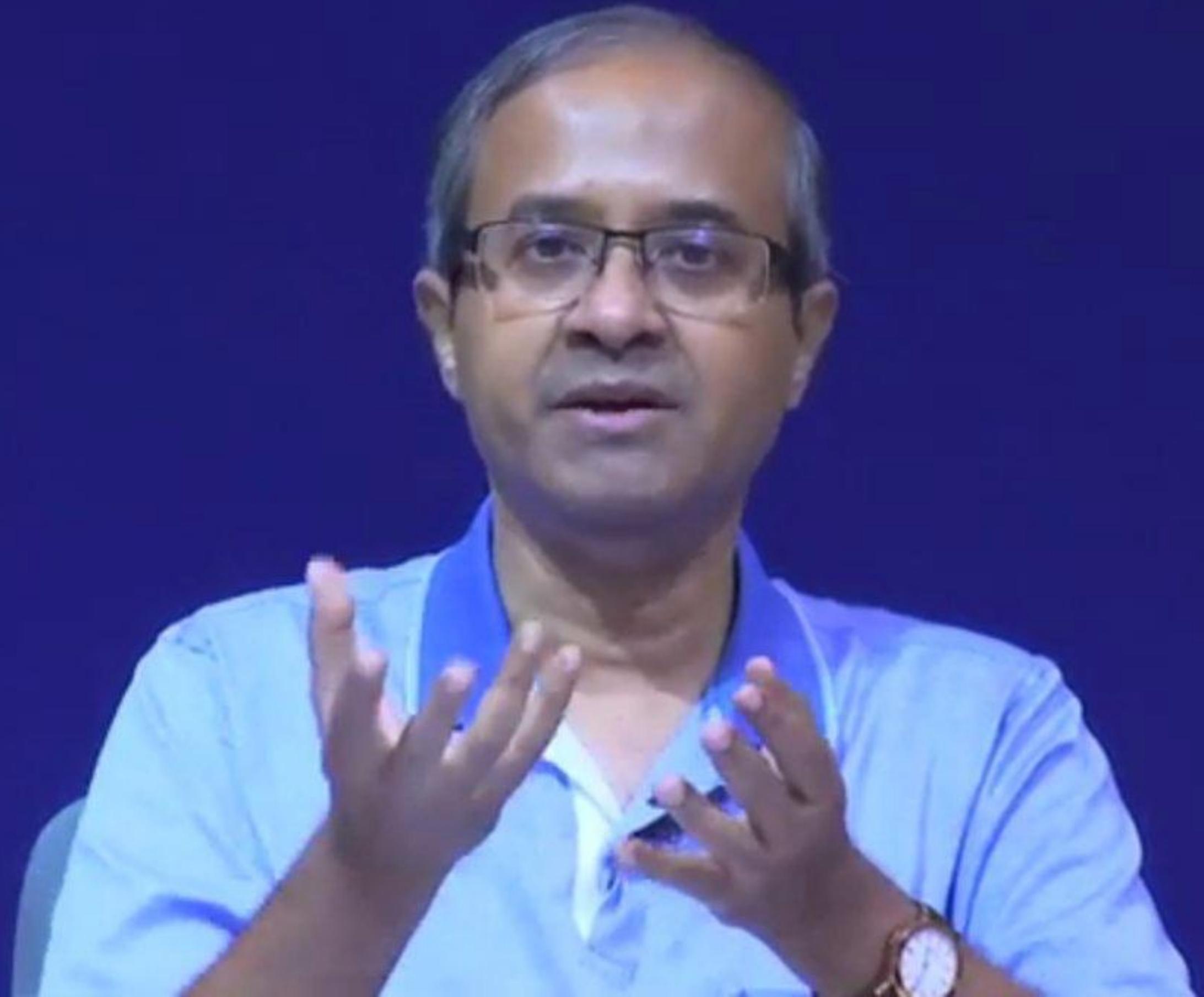
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00:19:16



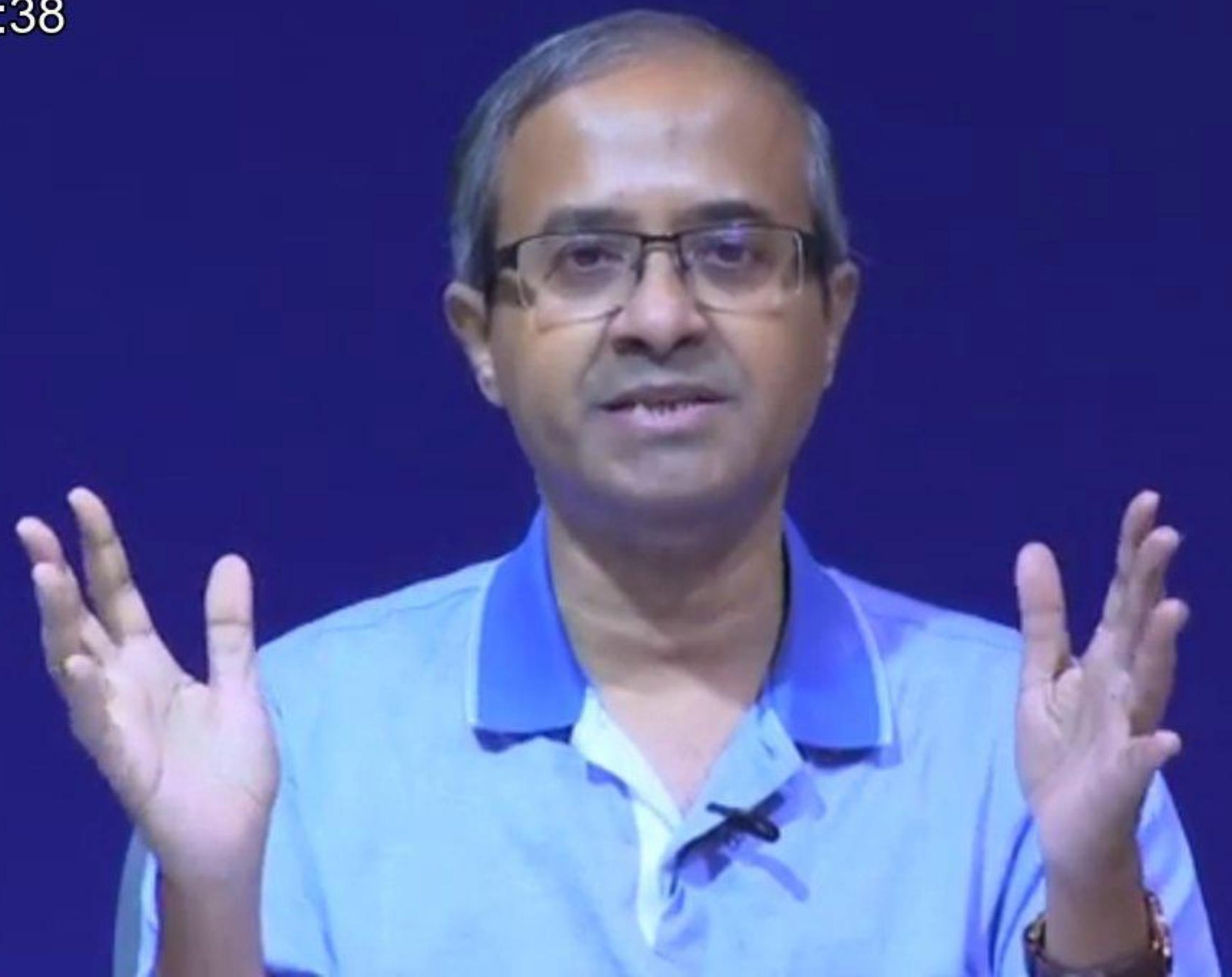
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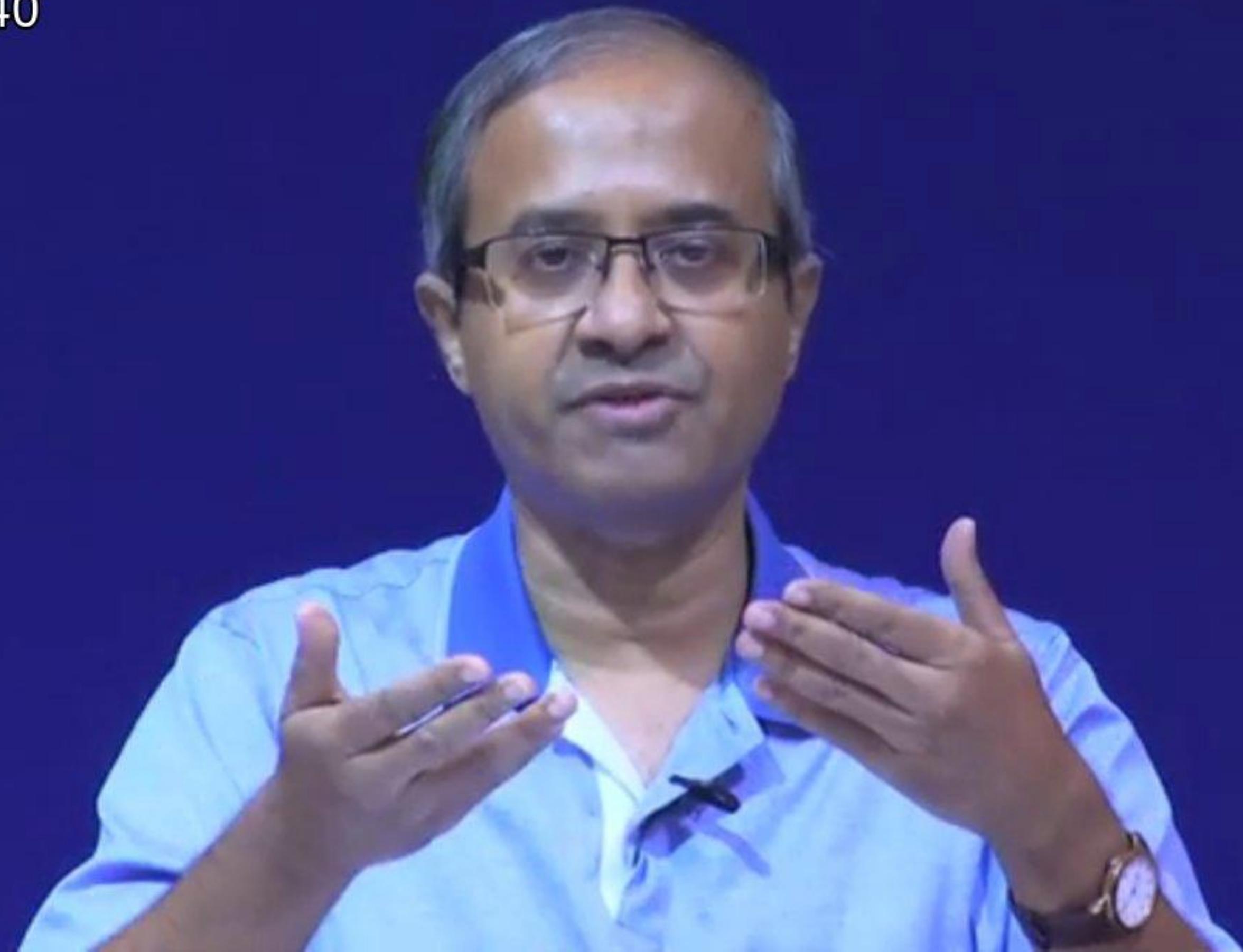
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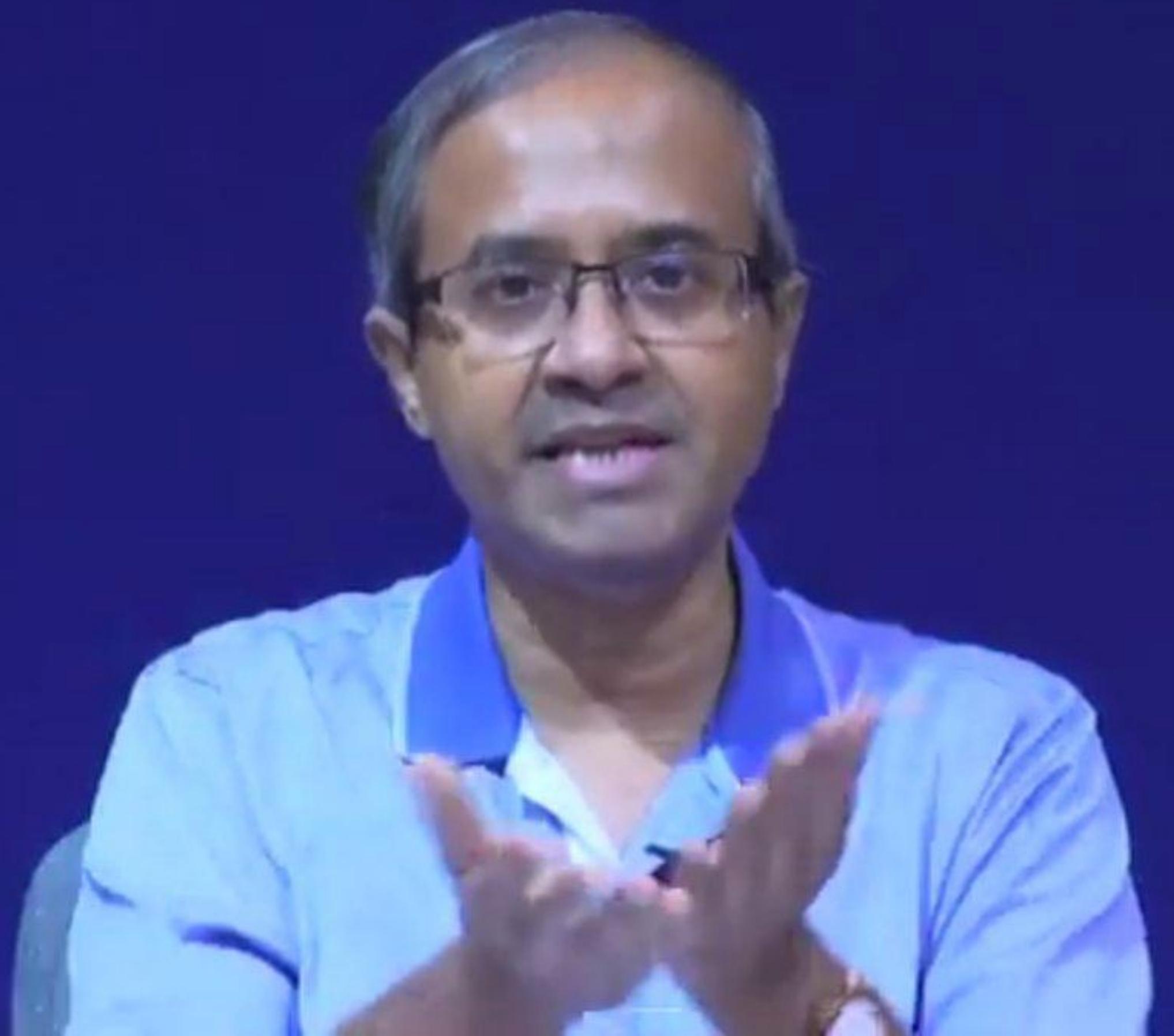
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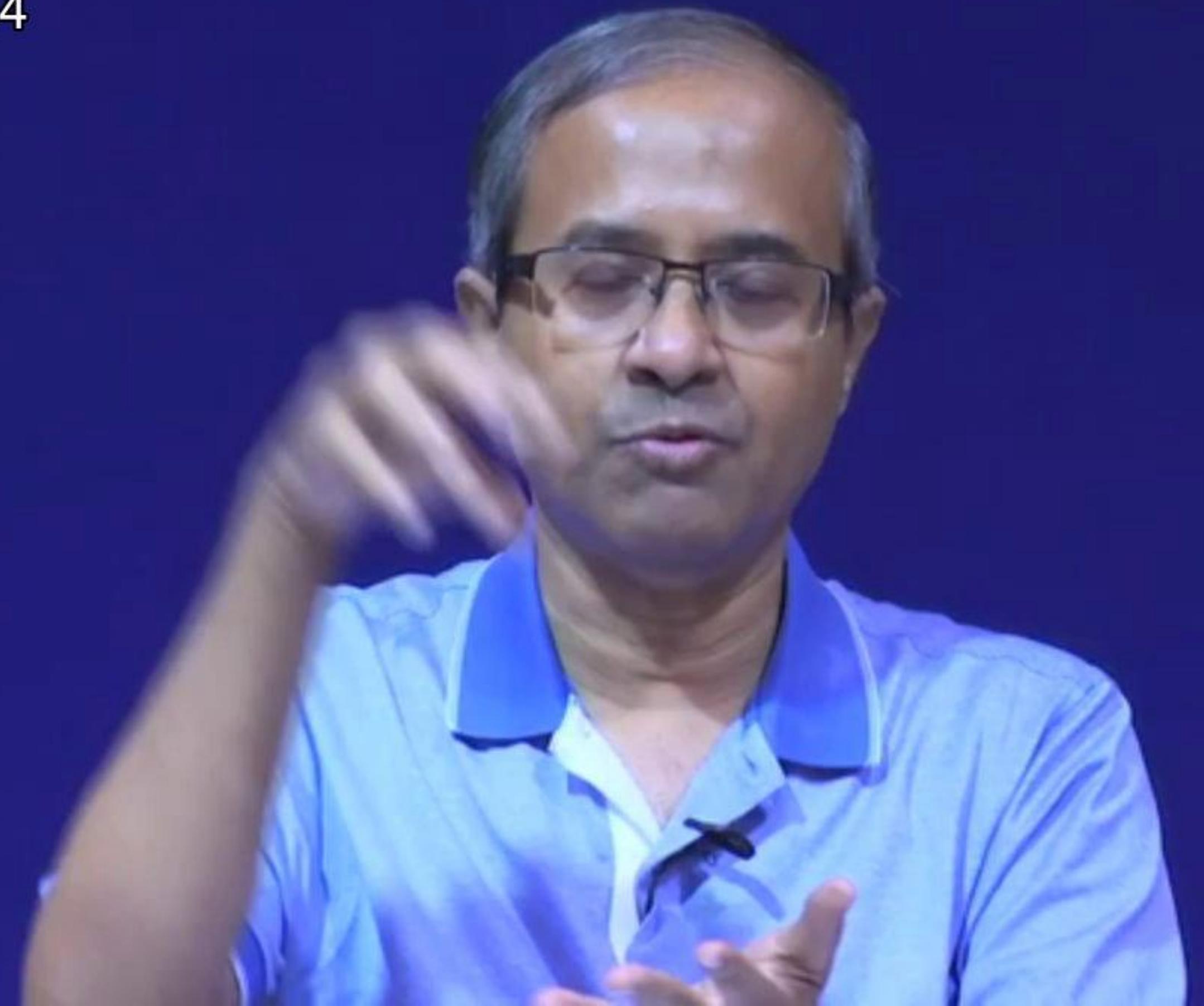
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00:19:42



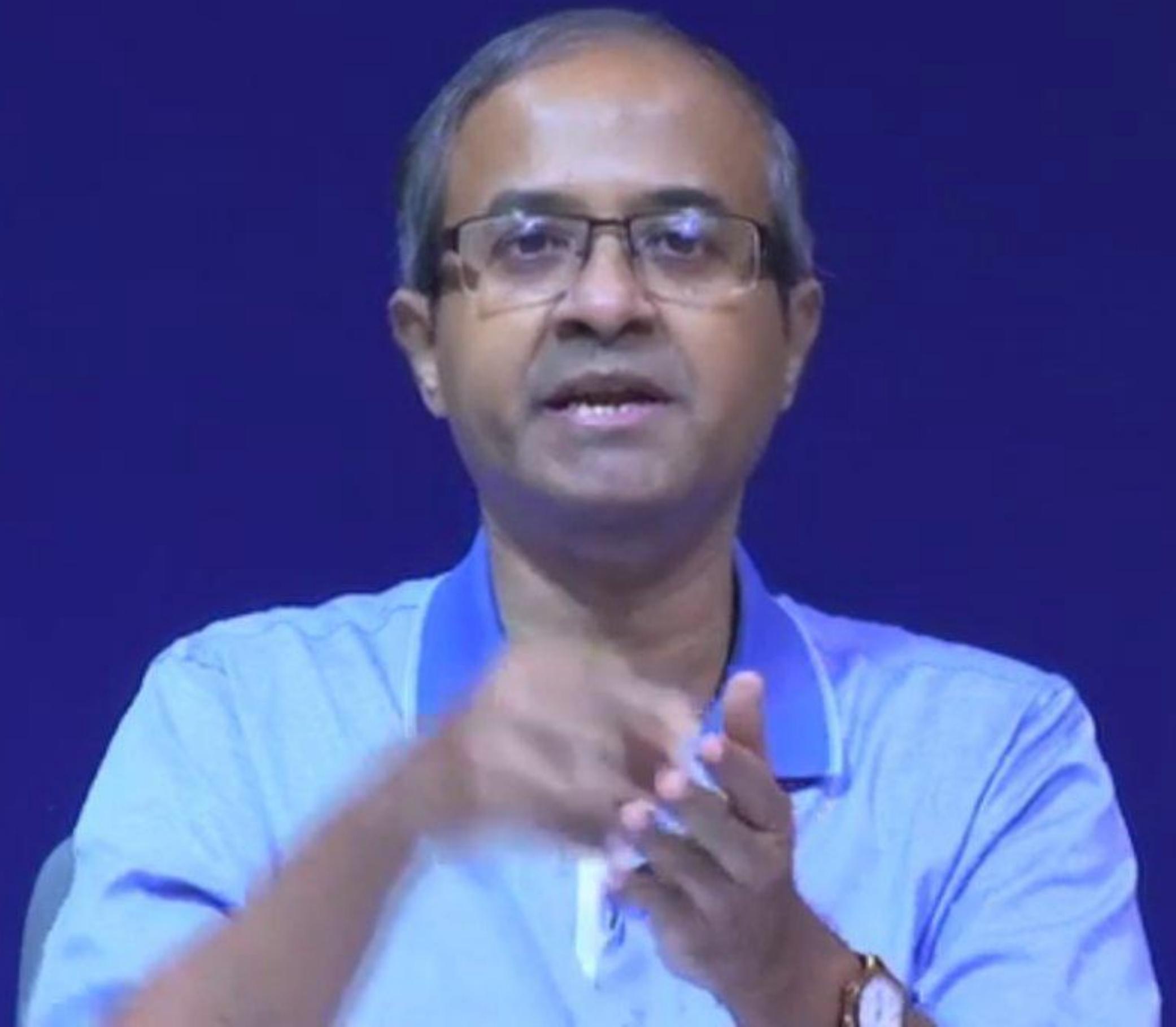
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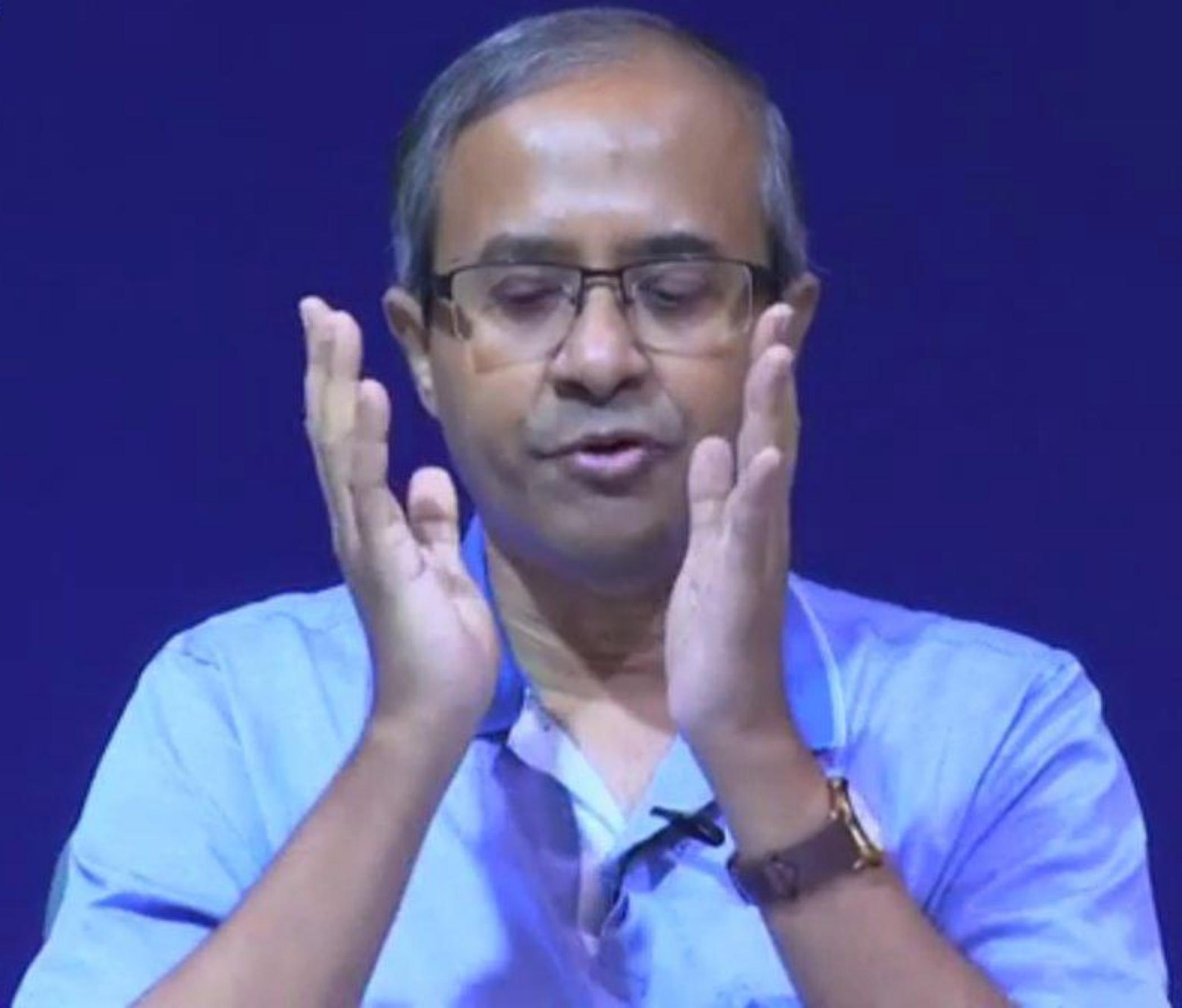
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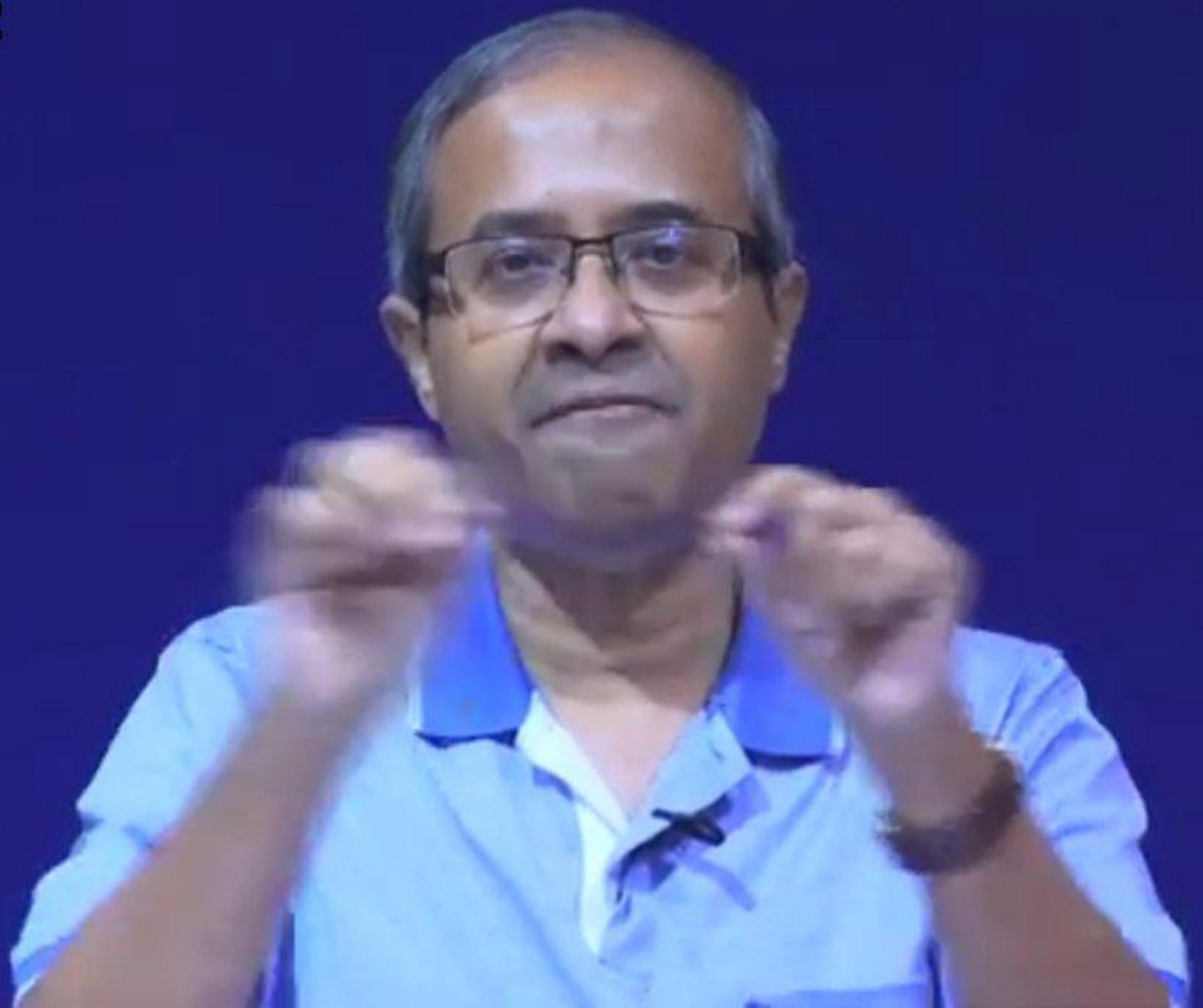
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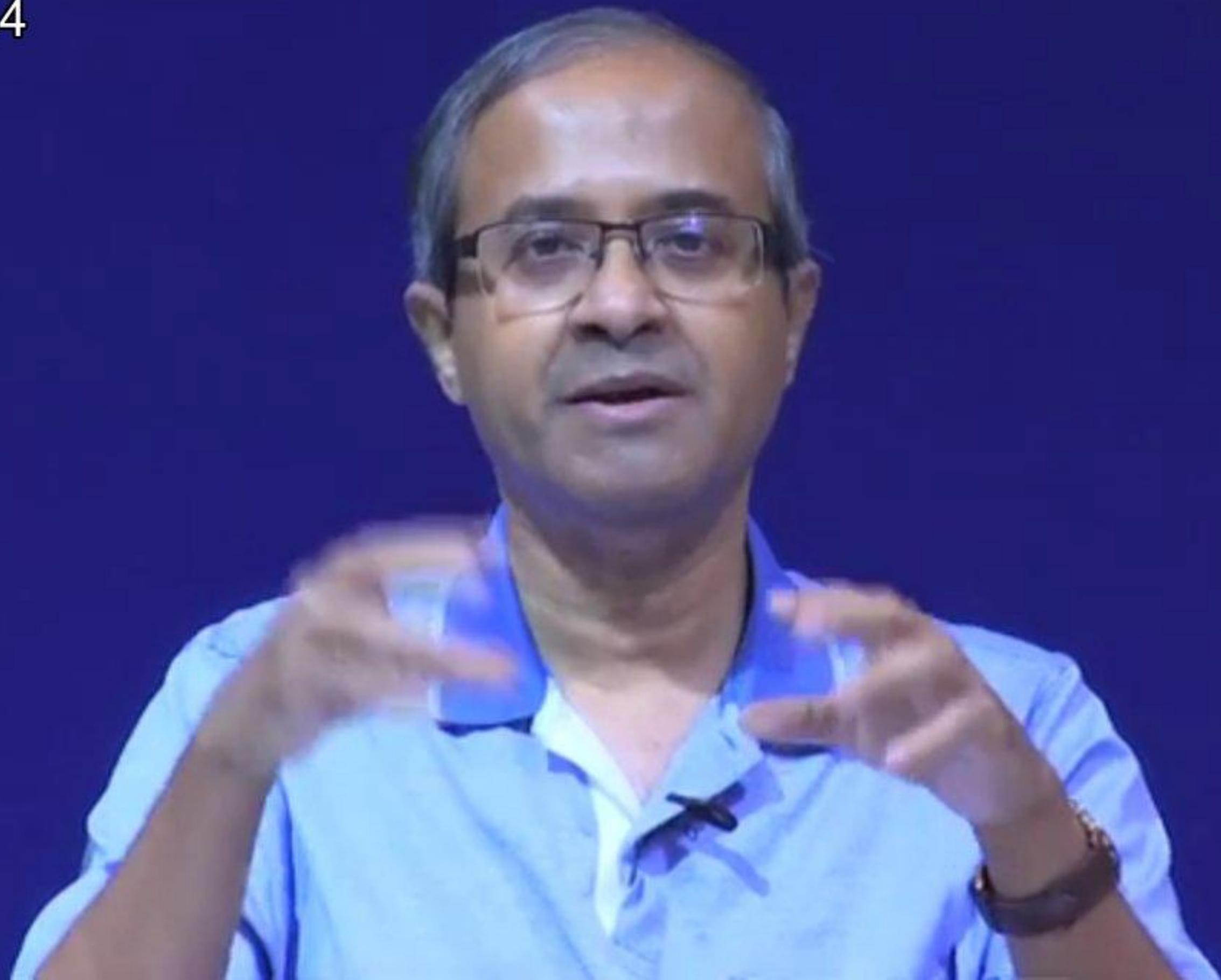
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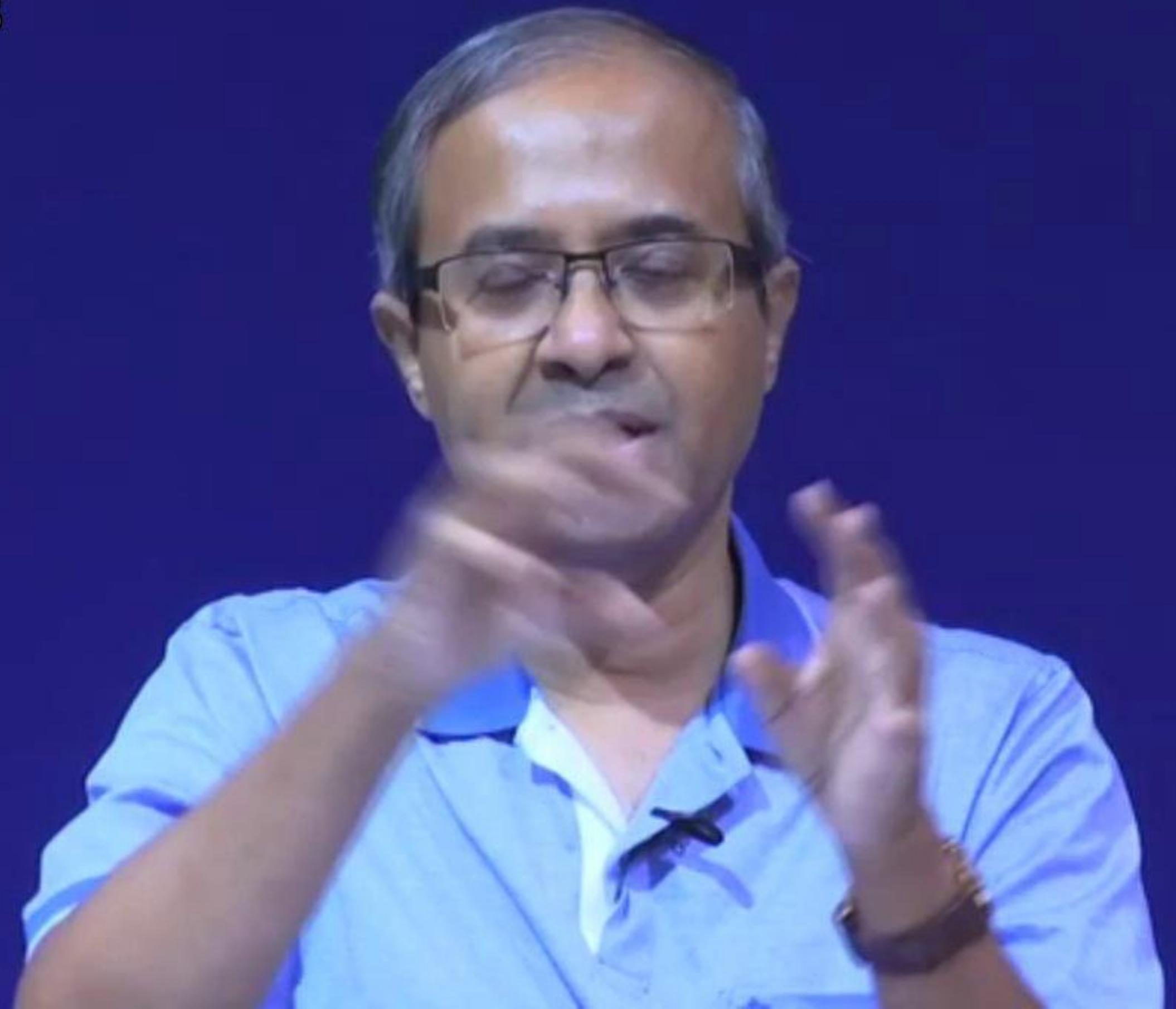
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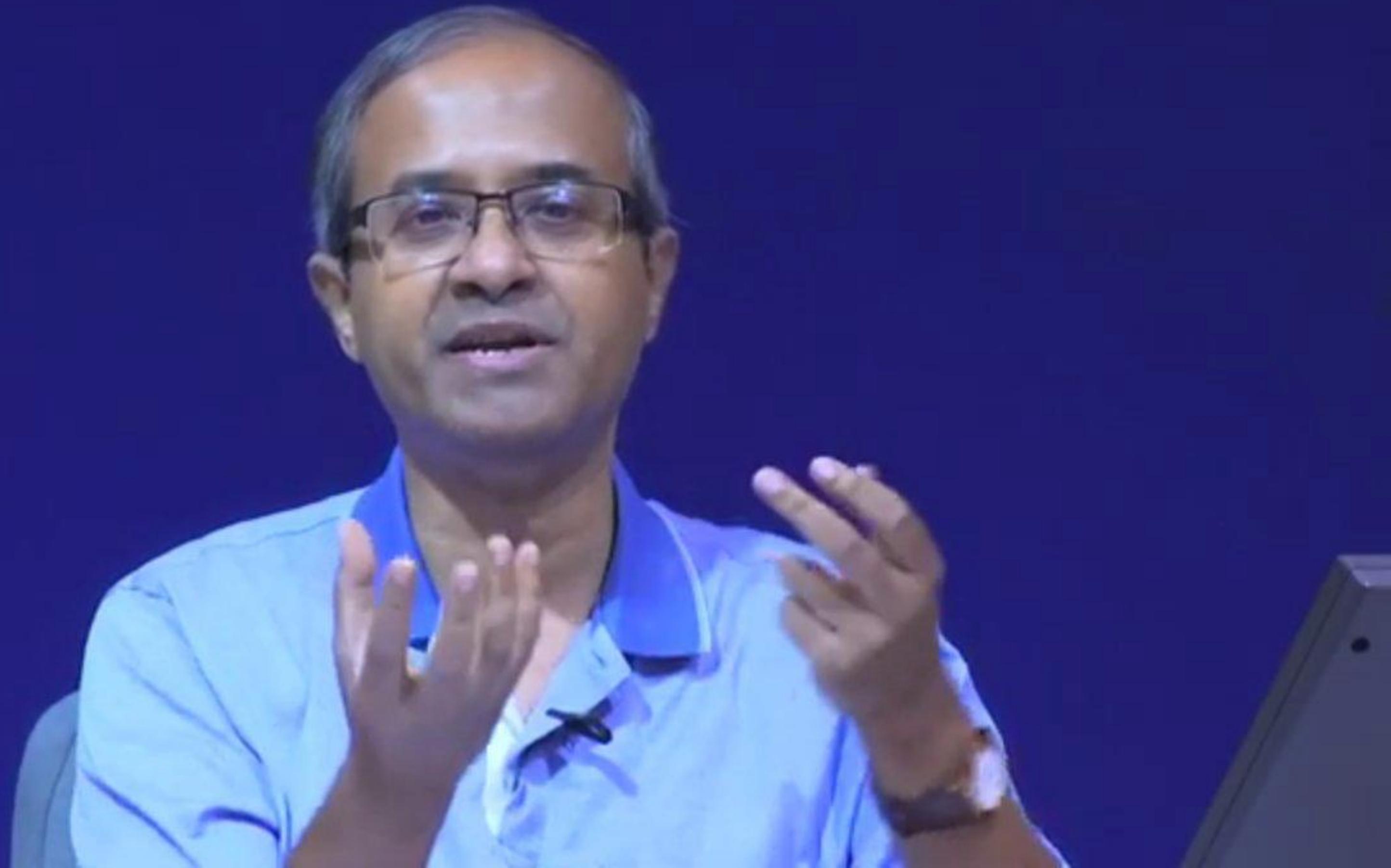
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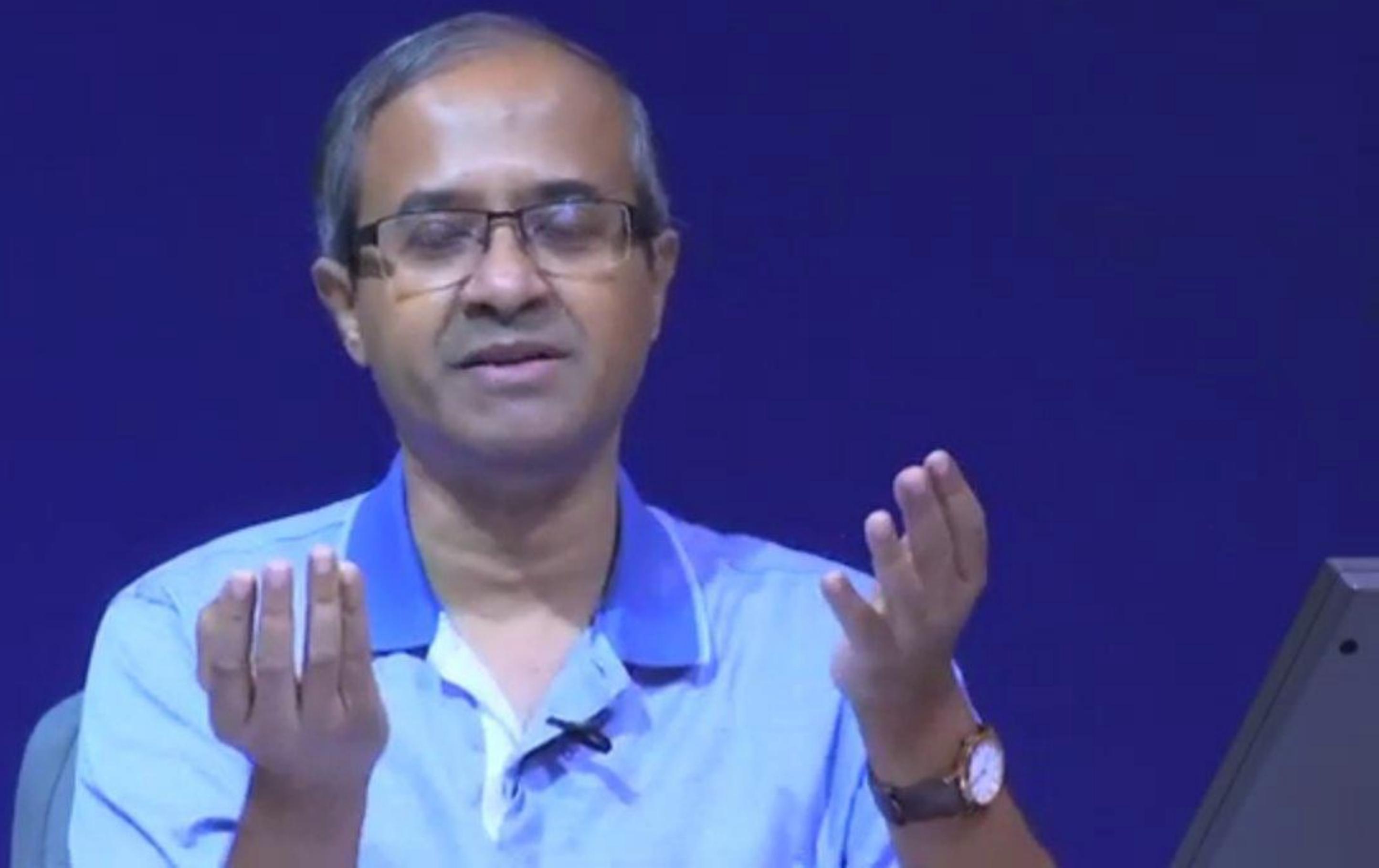
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00:20:56



00:20:58



00:21:00



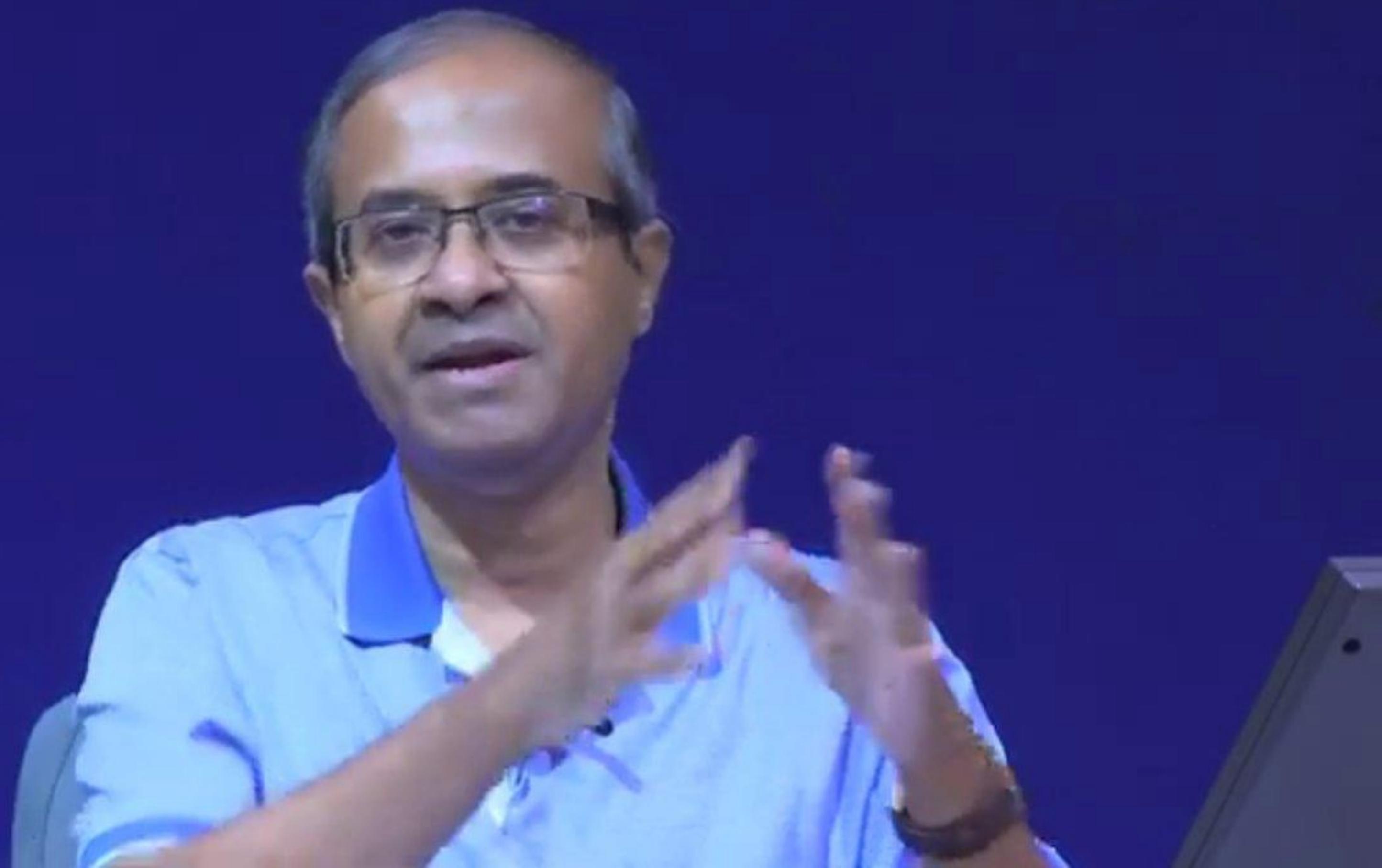
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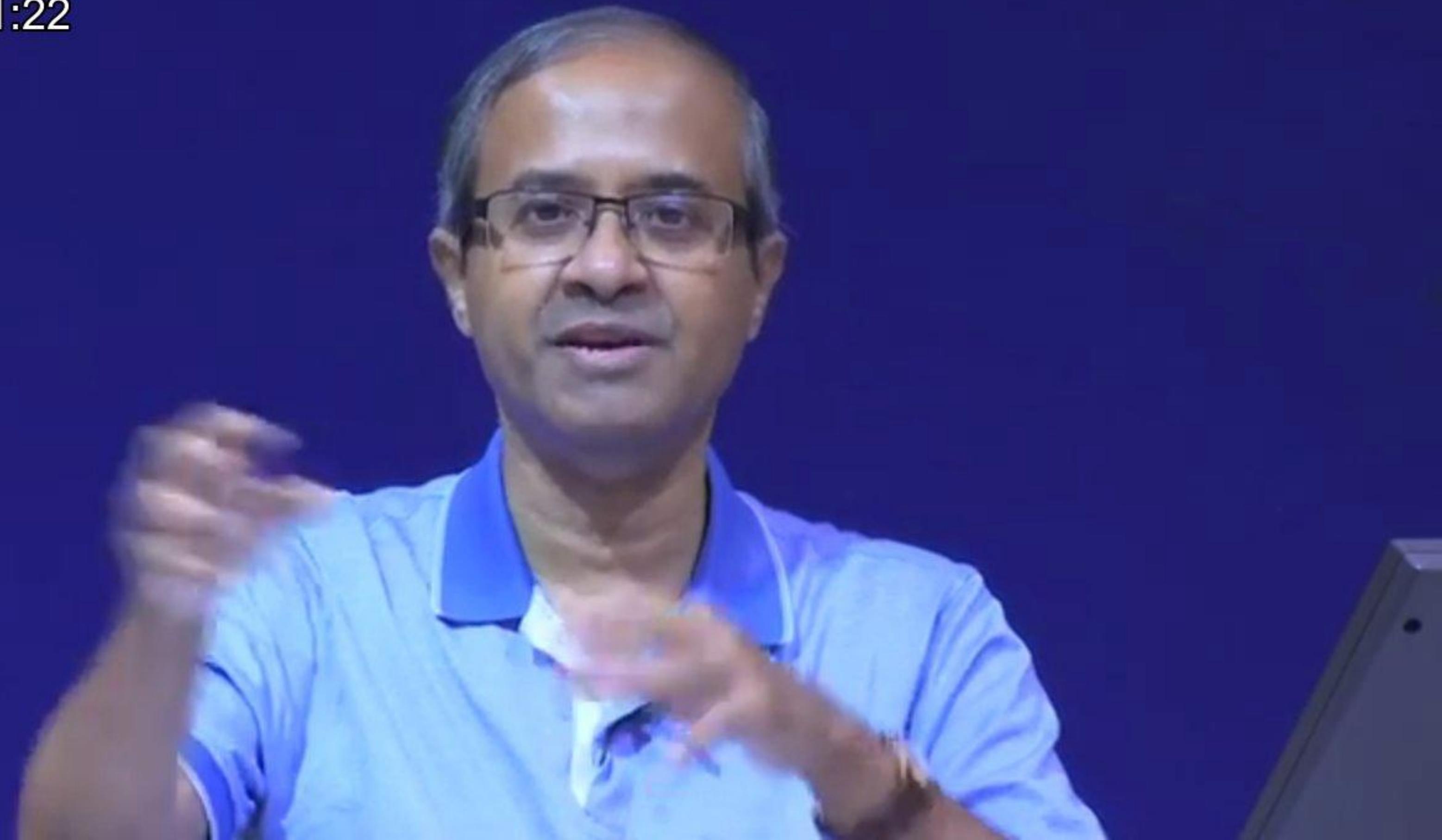
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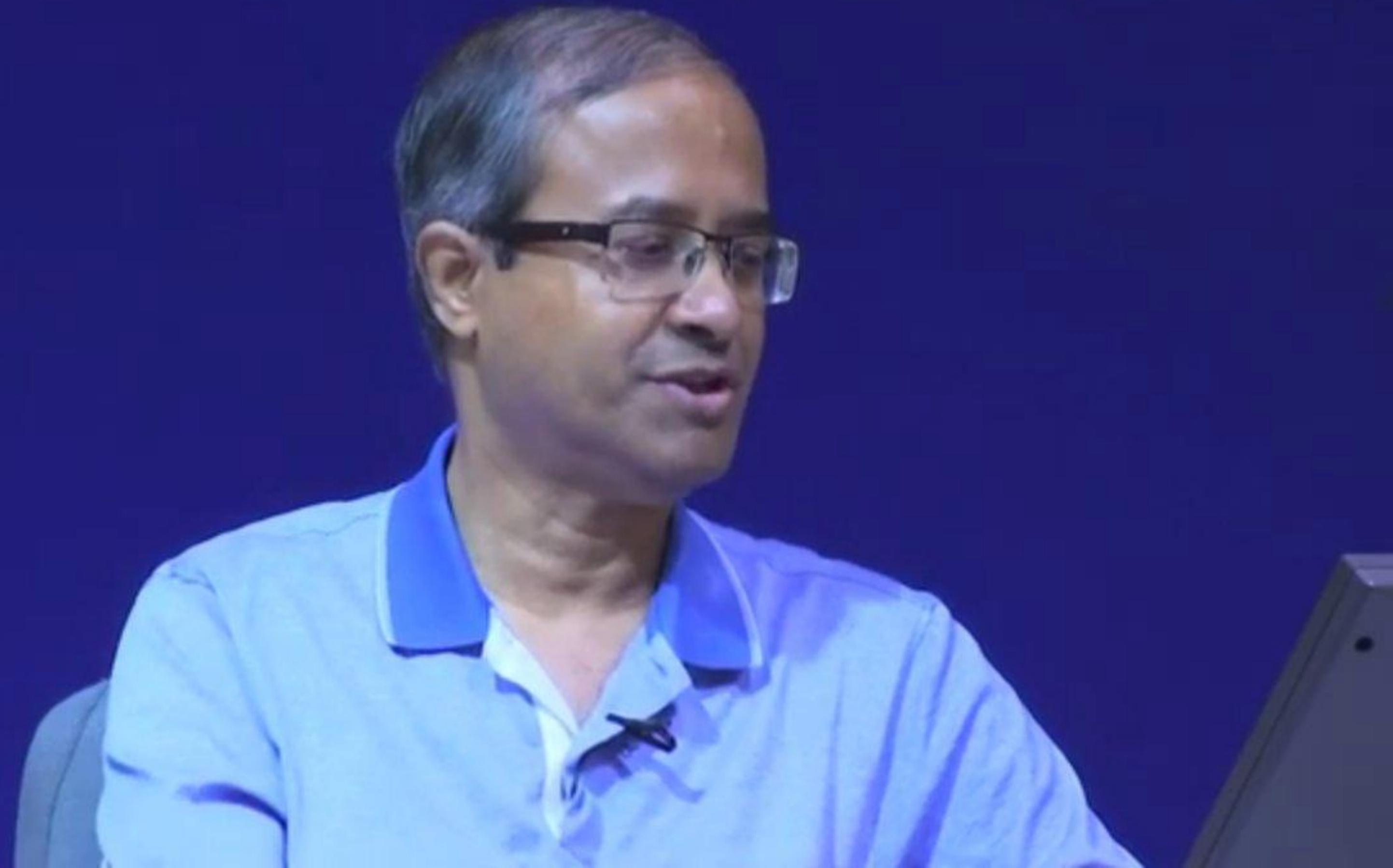
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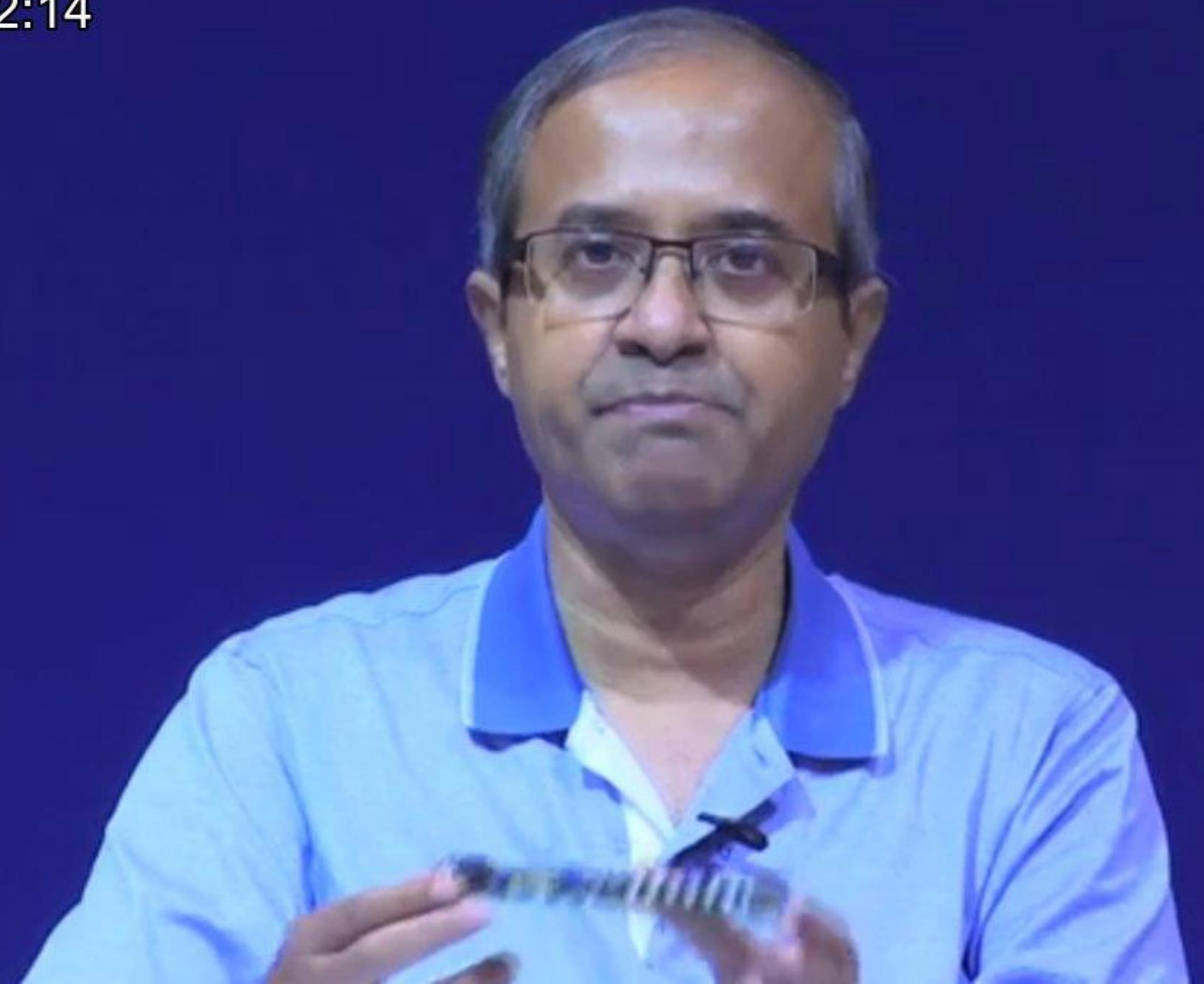
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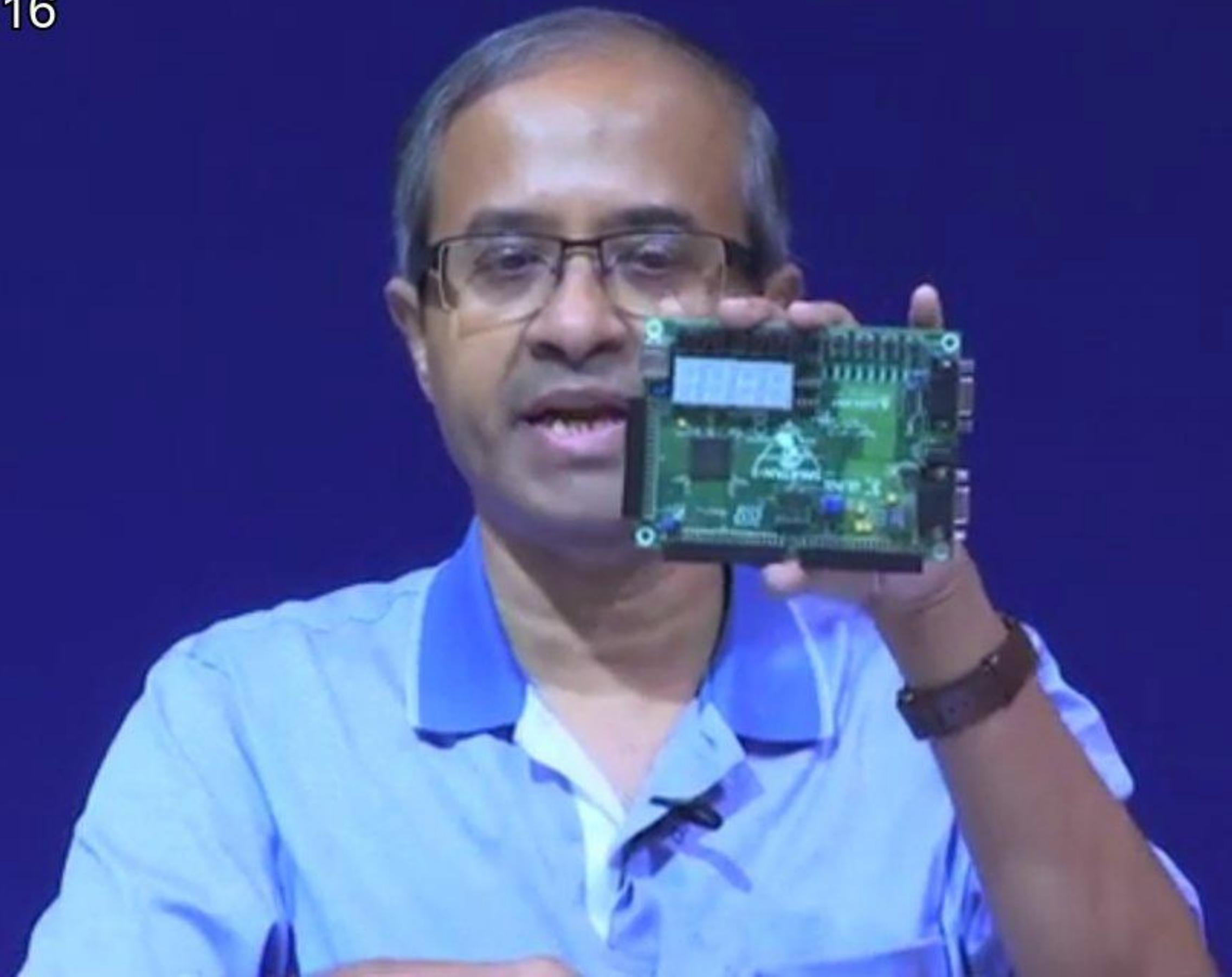
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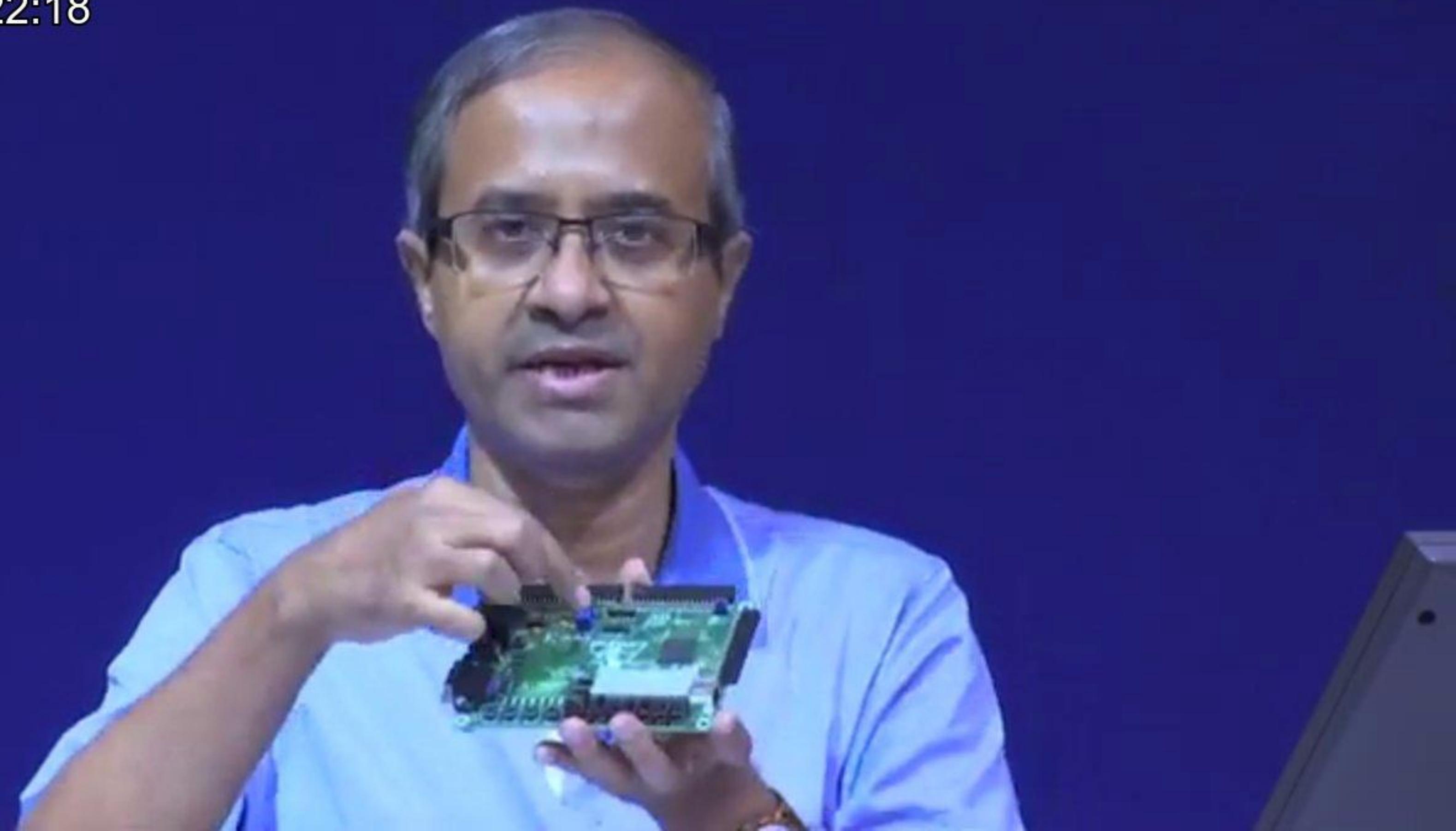
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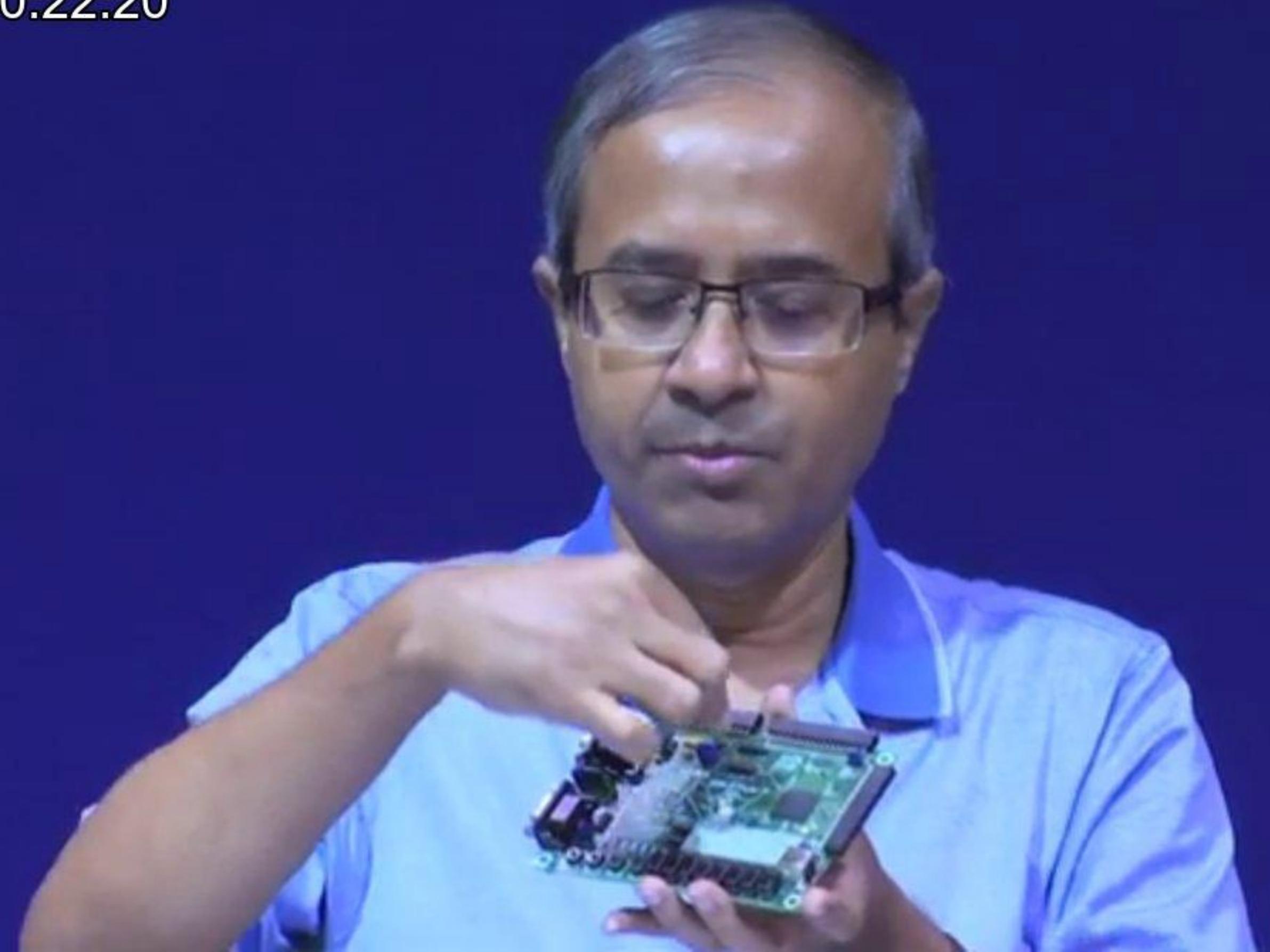
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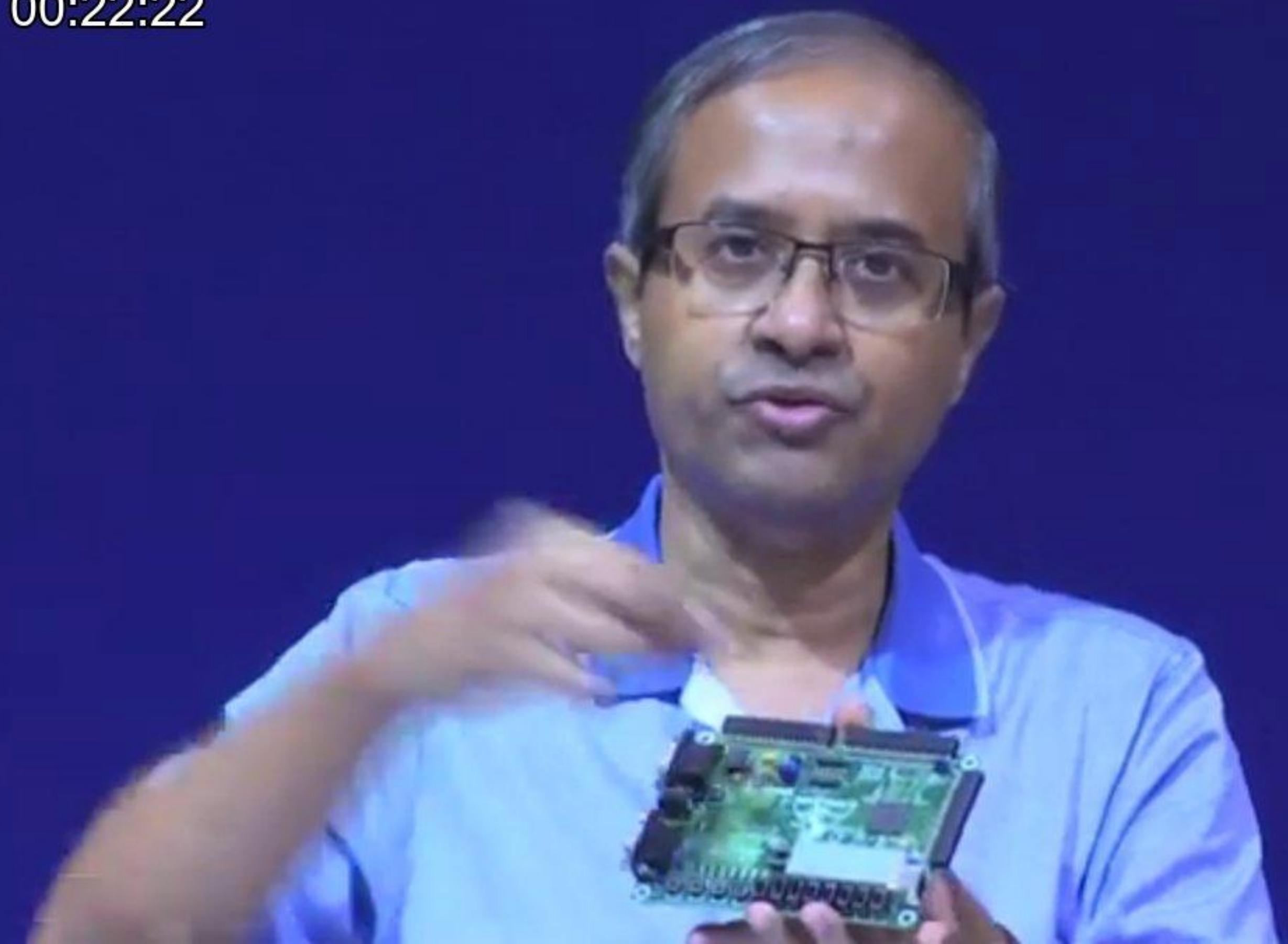
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00:22:20



00:22:22



00:22:40

## END OF LECTURE 04



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Hardware Modeling Using Verilog