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3.2

- Step 1:

+ The PC contains 300, the address of the first instruction. This value is loaded into the MAR

+ The value in location 300 (1940) is loaded into MBR and the PC is increased

- The value in the MBR is loaded into the IR

- Step 2:

+ The address portion of the IR (940) is loaded into the MAR

+ The value in location 940 is loaded into the MBR

+ The value in the MBR is loaded into the AC

- Step 3:

(- The value in location 307 is loaded into the MAR)

+ The PC contains 307, this value is loaded into the MAR

+ The value in location 301 is loaded into MBR and the PC is increased

+ The value in the MBR is loaded into the IR

- Step 4:

+ The address portion of the IR is loaded into the MAR

→ The value in location 941 is added to the value of AC and stored in the AC (AC2+AC3=AC)

+ The value in the MBR is loaded into the AC

- Step 5:

Một trang vở một trang tài

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+ The PC contains 302, the address of the third instruction, this value is then loaded to the MAR

+ The value in location 302 (2941) is loaded into the MBR and the PC is incremented

+ The value in the MBR is loaded into the IR

- Step 6

+ The address portion of the IR (941) is loaded into the MAR

+ The value in the IC (941) is loaded into the MBR, then loaded into the address 941

~~(7 bit)~~

3.3

a) First type is opcode $\Rightarrow 2^7 \cdot 2^9 = 2^{16}$ (bytes)

$\Rightarrow$ Maximum directly addressable memory capacity:

2^{16} bits = 16 Mbytes

b)

1) If the microprocessor bus has a 32-bit local data bus, the address can be transferred at the same time and decoded in memory. However, because there is a 16-bit local data bus, it needs (2+1) bus cycles to fetch 32-bit instruction

2) The 16-bit local address bus can't accept all of the memory so it needs to be transferred twice. There is a 16-bit local data bus so we need two cycles to fetch 32-bit instruction

Mọe trang vở mọe vương

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c)

- The program counter must be at least 26 bits
- The instruction register if contain only opcode then it has to be 6 bits long; if it contains the whole instruction, it has to be 32-bits long

3.5.

Clock cycle: $T = \frac{1}{f} = \frac{1}{8 \cdot 10^6} = 0.125 \cdot 10^{-6}$ (s) = 125 (ns)

Bus cycle: 4 · 125 = 500 (ns)

32-bit microprocessor access with a 16-bit external data bus

⇒ (to) 32 : 16 = 16 (bit) = 2 (byte) transfered per bus cycle

⇒ Transfer rate = 2 byte / 500 ns = $4 \cdot 10^6$ byte/s

Doubling the frequency may mean developing a new chip manufacturing technology, doubling the external data bus means wider on-chip data bus drivers / latches and modifications to the bus control logic. In the first case, the speed of the memory chips will also need to be doubled not to slow down the microprocessor, in the second case, the "word length" of the memory will have to be/still to be able to send / receive 32-bits quantities

3.14

a) Since there are four memory operations dealing with read and write (except add 1 to operand), 1 wait states was added