**Pledge Honor:**

**CS 488 Midterm Exam: 100 Points; Time 120 minutes Name:**

1. (5 Points) State whether you will get a memory alignment error for the following instructions and why? Assume x0 contains 0.
   a. sw x3, 194(x0)
   b. fld f2, 264(x0)

ANSWER:

**If the address is not aligned properly, the processor may not be able to access the data correctly and may raise a memory alignment error. However, since the starting address is 0, the address 264(x0) is aligned to the size of a double-precision floating-point value and thus this instruction will not cause a memory alignment error.**

2. (5 Points) Describe in 2-3 sentences what has limited the rate of growth of the processor's clock rate.

ANSWER:

**The law of diminishing returns governs the limits of progression in the growth of a processor's clock rate. While parallelism is a key part in speeding up a processor's clock rate, there is a finite value at which the clock rate can no longer be increased. The serial (unimprovable) components are the limit at which these clock rates are governed by, according to Amdahl's Law.**

3. (5 Points). What is the main reason the simple five-stage RISC-V architecture used WB split cycle?

ANSWER:

**RISC-V contains the Writeback (WB) split cycle stage which literally writes back the result to the destination register. This stage is mainly used to avoid data hazards in pipelining. The data hazards occur due to data dependencies among different instructions so the WB stage avoids these conflicts, which allows for a speedup in the execution of the instruction cycle using the pipelining process in RISC-V.**

4. (5 Points) What is the main reason the simple five-stage RISC-V architecture used separate memory for data (DM) and instruction (IM)?

ANSWER:

**It allows for a faster handling of instruction calls, and is important for preventing conflicts between data and instructions. If the two were not separated, conflicts may occur between the two during the execution process.**

5. (5 Points) Intel is spending $7 billion to complete its Fab 42 facility for 7 nm chip technology, which provides good dimensional scaling from its current 14nm. Based on what you learned in this course, what four major changes do you expect to see between 14nm and the new 7 nm?

ANSWER:

**Smaller sizes will result in a higher transistor density, which provides more speed overall. Another benefit of the smaller size will be the reduced power consumption and consequent reduction in generated heat. The decrease in power consumption will allow for more chips to be placed on a single die,which ties into the increase in functionality due to the transistor density previously mentioned. Lastly, the yield of the 7 nm process will be higher than that of the 14 due to the decrease in size. In terms of production, this means less defective chips on average.**

6. (15 Points) A model of Intel Red Dragon processor has a die size of 400 $mm^2$ and an estimated defect rate of 0.04 per $cm^2$. The process complexity factor is 13.5.

a. (8 Points) Assume the wafer yield is 100%, what is the die yield?

$$Die\ Yield = \frac{Wafer\ yield}{[1+Defects\ per\ unit\ area \bullet Die\ area]^N} = \frac{1}{[1+0.04+4]^{13.5}} = 0.1348$$

b. (7 Points). What is the cost of a chip if the cost of a wafer of diameter 300 mm is $7000?

$$Dies\ per\ wafer = \frac{\pi[\frac{Wafer\ diameter}{2}]^2}{Die\ area} - \frac{\pi(Wafer\ diameter)}{\sqrt{2 \bullet Die\ Area}} = \frac{\pi[\frac{300}{2}]^2}{400} - \frac{\pi(300)}{\sqrt{2 \bullet 400}} = 143.39$$

$$Cost\ of\ die = \frac{7000}{143.39 \bullet 0.1348} = \$362.15$$

ANSWER:

7. (15 Points). You are considering enhancing a processor by adding a GPU (Graphical Processing Unit) to run "View Me" programs faster. When computation is run in GPU, it is 6 times faster than the normal mode of execution.

a. (10 Points). What percentage of "View Me" should run in GPU to achieve an overall speedup of 4?

b. (5 Points). What percentage of the "View Me" execution time is in GPU when the overall speedup of 4 is achieved?

ANSWER:

**a. To achieve an overall speedup of 4, we can use the formula for speedup: Speedup = 1 / (1 - p + p/s) where p is the percentage of the program running on the GPU, and s is the speedup factor.Plugging in the**

**4 = 1 / (1 - p + p/6); p = 67.6%**

**Therefore, to achieve an overall speedup of 4, 67.6% of the "View Me" program should run on the GPU.**

**b. Solve for p when the overall speedup is 4 and the percentage of time running on GPU is unknown.**

**4 = 1 / (1 - q + q/6); q = 78.4%**

**Therefore, when the overall speedup is 4, approximately 78.4% of the "View Me" program's execution time is spent running on the GPU.**

8. (15 Points) Designers are considering two options for improving a system's performance. They know 20% of computation is graphic processing.

a. (7 Points) Option 1: Increase the main memory. This will improve 60% of the graphic processing by a factor of 4.

b. (8 Points) Option 2: Upgrade the GPU. This will improve the graphic processing by a factor of 2. Which option is better? Justify your answer.

ANSWER:

**a. For option 1, increasing the main memory improves 60% of the graphic processing by a factor of 4. This means that 60% of the computation can be sped up by a factor of 4, while the remaining 40% stays the same. Therefore, f = 0.4.**

**Using Amdahl's law, the overall speedup of option 1 can be calculated as:**

**Speedup = 1 / (1 - f + f/4) = 1 / (1 - 0.4 + 0.4/4) = 1.43**

**b. Using Amdahl's law, the overall speedup of option 2 can be calculated as:**

**Speedup = 1 / (1 - f + f/2) = 1 / (1 - 0 + 0/2) = 1**

**Comparing the two speedups, it is evident that option 2 has a higher overall speedup of 1, compared to option 1's overall speedup of 1.43.**

Therefore, upgrading the GPU (option 2) is the better choice for improving the system's performance.

9. (15 Points). Consider an architecture that executes an instruction in seven steps:

IF (INSTRUCTION FETCH)
ID (INSTRUCTION DECODE)
AG (OPERAND ADDRESS GENERATOR)
OL (OPERAND LOAD)
EX (EXECUTION)
OS (OPERAND STORE)
UP (UPDATE PC)

a. (5 Points) If each memory access (IF, OL, OS) takes 4 units of time to complete, while all other steps take 1 unit of time, what is the cycle time of this un-pipelined processor?

b. (5 Points) If we pipeline the processor in part "a" into a seven-stage pipeline, which adds an overhead of 2 units of time per latch, what would be the cycle time of this pipelined processor?

c. (5 Points) What is the speedup obtained by the pipeline?

ANSWER:

**The cycle time of the un-pipelined processor is equal to the sum of the time taken by each stage of the processor. Since all stages take 1 unit of time except for memory access stages (IF, OL, OS) which take 4 units of time each, the cycle time is:**

**Cycle time = 1 + 1 + 1 + 4 + 1 + 4 + 1 = 13 units of time.**

**Then pipeline the processor into a seven-stage pipeline with an overhead of 2 units of time per latch, the cycle time of the pipelined processor is:**

**Cycle time = Max(stage times) + overhead per latch= Max(1, 1, 1, 4, 1, 4, 1) + 2= 6 + 2 = 8 units of time.**

**The speedup obtained by the pipeline is equal to the ratio of the cycle time of the un-pipelined processor to the cycle time of the pipelined processor:**

**Speedup = Un-pipelined cycle time / Pipelined cycle time= 13 / 8= 1.625.**

**Therefore, the pipeline achieves a speedup of 1.625 times over the un-pipelined processor.**

10. (15 Points). Consider the following code segment:

```
        flw    f0, 0(x0)      ; load f0 from address 0+x0
Loop:   flw    f2, 0(x2)      ; load f2 from address 0+x2
        fmult  f2, f2, f0     ; f2 = f2 * f0
        addwi  x2, x2, 4      ; x2 = x2 + 4
        fsd    f2, -4(x2)     ; store x2 at address -4+x2
        subw   x4, x3, x2     ; x4 = x3 – x2
        bne    x4, x0, -24    ; branch to loop if x4!= 0 (i.e. set PC<- PC+offset)
```

Assume the initial value of x3 is x2 + 300.

a. (4 Points). What is the size of this code in IM and the size of its data in DM?

b. (8 Points) Show the timing diagram of this instruction sequence for the five stage RISC-V pipeline with full forwarding paths including register read and write in the same cycle, comparison performed in ID stage and PC updated in ID as well. Assume branch is handled by predicting it as taken. Table is provided.

c. (3 Points) How many cycles does this loop take to execute?

ANSWER:

a.

b.

| Instruction | CC 1 | CC 2 | CC 3 | CC 4 | CC 5 | CC 6 | CC 7 | CC 8 | CC 9 | CC 10 | CC 11 | CC 12 | CC 13 | CC 14 | CC 15 | CC 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| flw f0, 0(x0) | IF | ID | EX | M | WB | | | | | | | | | | | |
| Loop: flw f2, 0(x2) | | IF | ID | EX | M | WB | | | | | | | | | | |
| fmult f2, f2, f0 | | | IF | *S* | ID | EX | M | WB | | | | | | | | |
| addwi x2, x2, 4 | | | | | IF | ID | EX | M | WB | | | | | | | |
| fsd f2, -4(x2) | | | | | | IF | ID | EX | M | WB | | | | | | |
| subw x4, x3, x2 | | | | | | | IF | ID | EX | M | WB | | | | | |
| bne x4, x0, -24 | | | | | | | | IF | *S* | ID | EX | M | WB | | | |
| flw f2, 0(x2) | | | | | | | | | | IF | ID | EX | M | WB | | |

c.

13 clock cycles normally;