1.1)

[A] Yield = 1+((defects per area * die area)/N)^-N = 1+((0.04 * 2.00)/14)^-14 = 0.92332.
[B] A more complex design with a larger number of transistors may result in a higher defect rate, but this also depends on the manufacturing technology and process used to fabricate the device. The relationship between transistor count and defect rate is not straightforward, and there are other factors that can influence the overall reliability and performance of a device. It is possible that the age of BlueDragon is more than the age of Phoenix. The die age also matters a lot. As the die age increases the chance of defects in the die decreases.

1.2)

[A] To determine the profit per wafer for Phoenix chips, we need to find the number of defect-free chips that can be produced on a single wafer and then multiply that number by the profit per chip.The area of a wafer with a 450 mm diameter is (450mm/2)^2 * pi = 63,623.75 square millimeters.The number of defect-free chips that can be produced on a wafer is equal to the total wafer area divided by the area of a single chip, minus the area occupied by defects. Assuming that the area of a single chip is 1 square centimeter. Then the number of chips per wafer is 63623.75 mm^2 / (10^4 mm^2/cm^2) = 636.24 square cm.The number of defect-free chips on a wafer is then equal to 636.24 - (636.24 * 0.04) = 610.07 chips.The profit per wafer for Phoenix chips is then 610.07 * $30 per chip = $18,302.10.So, the manufacturer would make a profit of $18,302.10 on each wafer of Phoenix chips.
[B] Once again assuming that the area of a single chip is 1 square centimeter, then the number of chips per wafer is 63623.75 mm^2 / (10^4 mm^2/cm^2) = 636.24 square cm. The number of defect-free chips on a wafer is then equal to 636.24 - (636.24 * 0.03) = 622.48 chips. The profit per wafer for RedDragon chips is then 622.48 * $15 per chip = $9,337.20. So, the manufacturer would make a profit of $9,337.20 on each wafer of RedDragon chips.
[C] The facility can fabricate 70 wafers a month, so the total number of RedDragon chips that can be produced is 70 wafers * 622.48 chips/wafer = 43,574 chips. The facility can fabricate 70 wafers a month, so the total number of Phoenix chips that can be produced is 70 wafers * 610.07 chips/wafer = 42,707 chips. The demand for RedDragon chips is 50,000 chips per month, and the demand for Phoenix chips is 25,000 chips per month. Since the facility can produce 43,574 RedDragon chips per month, it should produce all 70 wafers as RedDragon chips to meet the demand. Since the facility can only produce 42,707 Phoenix chips per month, it should produce 70 wafers * 25,000 chips/42,707 chips = 41.5 wafers as Phoenix chips to meet the demand. So, the facility should make 70 wafers as RedDragon chips and 41 wafers as Phoenix chips.

1.4)

[A] When the quad-core operates for 1/8 of the time and is idle for the rest of the time, its dynamic energy is 0.5 W * (1/8) = 0.0625 W. This is 8 times less than the energy required when operating at full power, which is 0.5 W * 1 = 0.5 W. Similarly, the dynamic power when the core is running is 0.5 W, and the dynamic power when the core is idle is 0. This means that the average dynamic power over the entire time period is 0.5 W * (1/8) = 0.0625 W, which is 8 times less than the dynamic power when operating at full power, which is 0.5 W.

[B] When using frequency and voltage scaling, the power consumption is proportional to the frequency and voltage squared. So, if the frequency and voltage are reduced to 1/8, the power consumption would be reduced to 1/8^2 = 1/64 of the original power consumption. The dynamic energy consumption is equal to the power consumption multiplied by the time of operation. So, if the quad-core operates for 1/8 of the time, the dynamic energy consumption would be 0.5W * (1/8) = 0.0625 W. Therefore, compared to running at full power, the dynamic energy consumption would be reduced to 0.0625 / 2 = 0.03125 W and the dynamic power consumption would be reduced to 0.5 W * (1/64) = 0.0078125 W.
[C] In this case, the dynamic energy savings will be the same as in the frequency and voltage scaling scenario, because the voltage reduction will be limited to 50%. However, the dynamic power savings will be different because power is proportional to the square of voltage, so even a small reduction in voltage can have a significant impact on power. To calculate the dynamic power savings, we need to find the average voltage used while the core is running. Let's assume the frequency is reduced to 1/8 of the original frequency and that voltage is reduced to 50% of the original voltage, but no lower. Then, the average voltage used while the core is running would be (0.5 + 1)/2 = 0.75 volts.The dynamic power while the core is running would then be (0.75^2) * 0.5 = 0.28125 W. Comparing this to the dynamic power when the quad-core operates at full power (0.5 W), we can see that the dynamic power has been reduced by 0.5 - 0.28125 = 0.21875 W or 43.75%.

1.5)

[A] Amdahl's Law: 1/((0.8/4) + 0.2) = 2.5 frequency and voltage
[B] E = E_quad/E_single = [4(r/2.5)^2]/[4(r(0.16)^-1)^2] = 0.64 Joules
[C] Dynamic energy = (2 + 0.2(2))/4 = 2.4/4 = 0.6 dynamic energy

1.7)

[A] Moore's Law states that the number of transistors on a chip doubles approximately every two years. So, if in 2015 the number of transistors was X, then in 2025 the number of transistors would be X * 2^(10/2) = X * 2^5 = X * 32 times the number in 2015. Therefore, the number of transistors on a chip in 2025 should be 32 times the number in 2015.
[B] The increase in performance in the 1990s was roughly proportional to the increase in the number of transistors on a chip, as predicted by Moore's Law. If performance had continued to climb at the same rate, then in 2025 the performance of chips would have been 32 times that of the VAX-11/780, assuming the VAX-11/780 was used as a benchmark in the 1990s. It's important to note that the increase in performance has not always continued to climb at the same rate as the number of transistors. This is due to various factors, such as power consumption and heat dissipation, which limit the increase in performance as the number of transistors on a chip continues to grow. Additionally, the increase in performance has become more difficult to achieve as the size of transistors has approached physical limits.

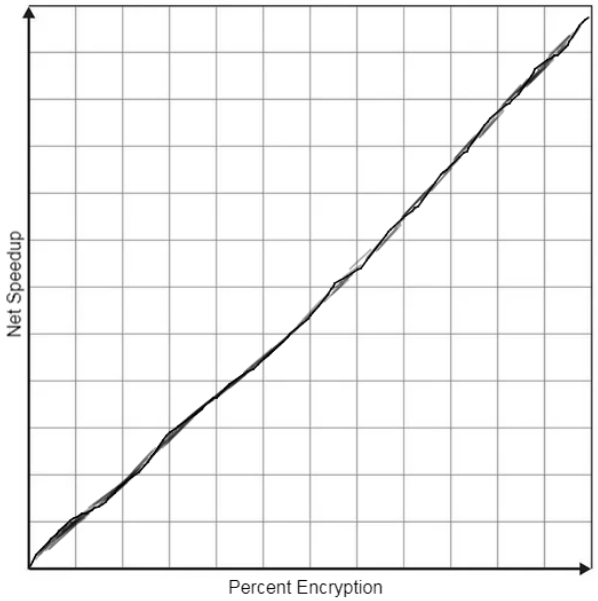
1.10)

[A] The mean time to failure (MTTF) is the average time a system operates without failure. It can be calculated as the reciprocal of the failure in time (FIT), which is the number of failures

per billion device-hours. So, for a single processor with a FIT of 100, the MTTF can be calculated as: MTTF = 1 / (FIT / 1,000,000,000) = 1 / (100 / 1,000,000,000) = 10,000,000 hours. Therefore, the MTTF for the system is 10 million hours. This indicates that, on average, the system can be expected to operate without failure for 10 million hours.
[B] If it takes one day to get the system running again, then the downtime is 24 hours. So, the availability can be calculated as: Availability = (Total time - Downtime) / Total time * 100%= (10 million hours - 24 hours) / 10 million hours * 100%= 999,999,976 hours / 10 million hours * 100%= 99.999996%. Therefore, the availability of the system is 99.999996%, which means it is operational and available to perform its intended function for 99.999996% of the time.

1.12)

[A]



[B] To calculate the percentage of encryption that would result in a net speedup of 2, we would need to solve for x in the following equation: Speedup = 20 * x / (100 - x) - 1 = 2 Here, x is the percentage of encryption operations, and (100 - x) is the percentage of normal operations. Solving for x, we get: x = (100 * Speedup + 100) / (Speedup + 21) = (100 * 2 + 100) / (2 + 21) = approximately 9.52%. So, a net speedup of 2 can be achieved with approximately 9.52% of encryption operations.
[C] If a net speedup of 2 is achieved, the percentage of time spent on encryption operations would be the percentage of encryption used to calculate the speedup/2, which is approximately 4.76%.