Take Home Assignment – due on 10-04-22 – CPE 487

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1. Convert the following numbers with the indicated bases to decimal:

   a) $(431)_5 = [4 \bullet 5^2] + [3 \bullet 5^1] + [1 \bullet 5^0] = \mathbf{116}$
   b) $(198)_{12} = [1 \bullet 12^2] + [9 \bullet 12^1] + [8 \bullet 12^0] = \mathbf{260}$
   c) $(445)_8 = [4 \bullet 8^2] + [4 \bullet 8^1] + [5 \bullet 8^0] = \mathbf{293}$
   d) $(345)_6 = [3 \bullet 6^2] + [4 \bullet 6^1] + [5 \bullet 6^0] = \mathbf{137}$

2. Add and multiply the following numbers without converting them to decimal:
   a) Binary numbers 1011 and 101.

   ```
     1011              1+1=10; carry the 1
      101
   +____
   10000
   ```

   b) Hexadecimal numbers 2E and 34.

   ```
     2E                [E+4] = 0x12 carry 1 from 0x12 leave the 2
     34                [2+3+1] = 0x6
   +__                 6 on the left, 2 on the right
     62
   ```

3. Decode the following ASCII code:

11000111 11101111 01101000 01101110 00100000 11000100 11101111 11100101
    ⇓   ⇓   ⇓   ⇓   ⇓   ⇓   ⇓   ⇓
    ?   ?   h   n   ?   ?   ?   ?

4. Complete the timing diagram of the following circuit by adding the timing trace for **f**:
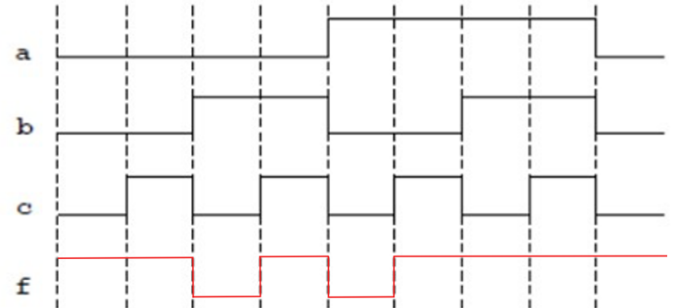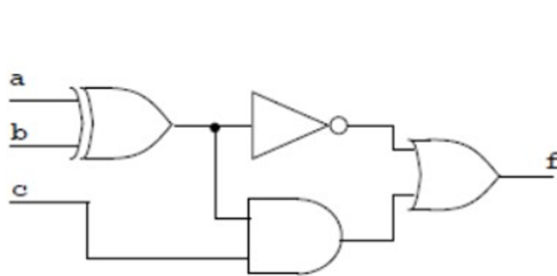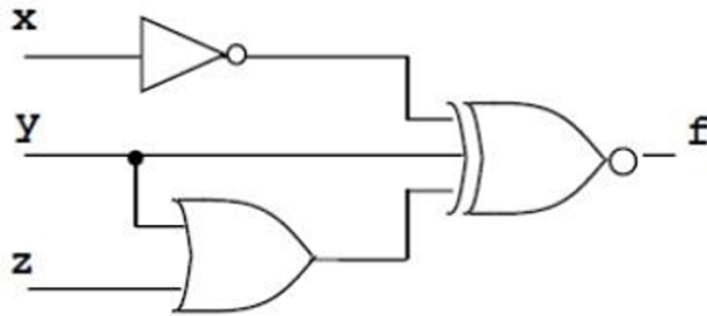

A eor B = Z

Z and C = X

X or -Z = F

Z | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0
C | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0
=====================================
X | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0
- Z | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1
=====================================
F | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1

5. Construct the truth table describing the output of the following circuit.

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Y or Z	-X	Y	F
0	1	0	0
1	1	0	1
1	1	1	0
1	1	1	0
0	0	0	1
1	0	0	0
1	0	1	1
1	0	1	1

6. The timing diagram below is correct for a 2-input (A & B) **NOR** gate.
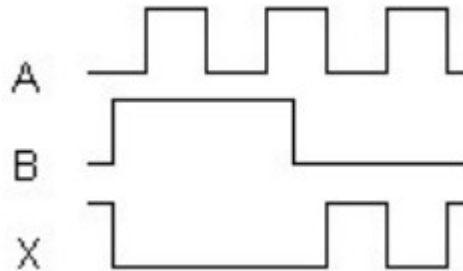
Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

7. Using VHDL signal assignment statements, write a description of the circuit (called and_or_gates) below
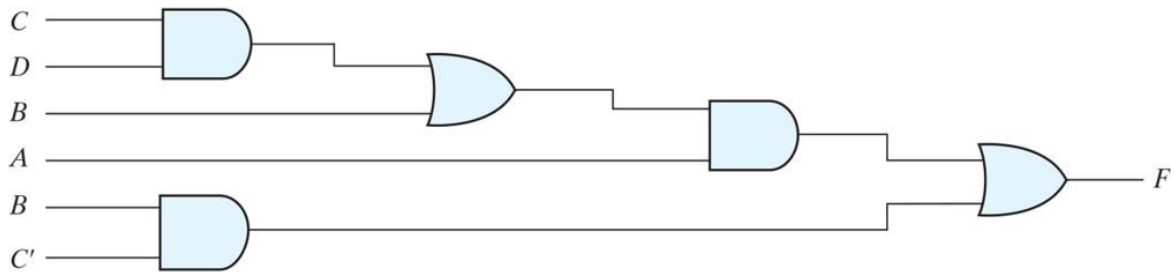
Note that C' is same as C

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity and_or_gates is
Port ( c : in STD_LOGIC;
d : in STD_LOGIC;
b : in STD_LOGIC;
a : in STD_LOGIC;
cprime: in STD_LOGIC;
end and_or_gates;

architecture SignalProcess of and_or_gates is

signal sig1,sig2,sig3,sig4: std_logic;

begin

sig1 <= ( c and d );
sig2 <= ( b and cprime );
sig3 <= ( sig1 or b );
sig4 <= ( a and sig3 );
F <= ( sig2 or sig4 );

end SignalProcess;
```