1.)

[A]

$Latency = 1\ cycle \quad Miss\ Rate = 0.03$

$Access\ Time = (1 - Miss\ Rate) \times (Hit\ Time) + (Miss\ Rate) \times (Miss\ Time)$

$= (0.97)(1) + 0.03(110) = 4.27\ cycles$

[B]

$Latency = 110\ cycles$

$Hit\ Rate = \frac{Cache\ Size}{Array\ Size} = \frac{64\ Kb}{1000\ Mb} = 0.000064$

$Access\ Time = 0.000064(1) + (0.999936)(110) = 109.993\ cycles$

2.)

Memory Access Excluded CPI = 1.35 Instructions = 20% load, 10% store, 70% access
L1 I-cache: 2% miss rate, 32 byte blocks, miss penalty 15 ns + 1 cycle
L2 D-cache: 5% miss rate, 16 byte blocks, miss penalty 15 ns + 1 cycle

[A]

$Access\ Time = 15\ ns$

$Miss\ Time\ [L1\ in\ L2] = 15 + 32(3.75)(\frac{1}{16}) = 2.5\ ns$

$Miss\ Time\ [Memory] = 60 + \frac{64}{16}(7.5) = 90\ ns$

$Avg.\ Memory\ Access\ Time = L2\ access\ time + memory\ access\ time + L2\ wb\ access\ time$

$= 0.02(22.5) + 0.02(0.2)(90) + 0.02(0.5)(90) = 0.99\ ns$

[B]

$Read\ Miss\ Time\ [L1\ in\ L2] = 15 + 3.75 = 18.75\ ns$

$Miss\ Time\ [L2\ in\ Memory] = 90\ ns$

$Avg.\ Memory\ Access\ Time\ [Read] = 0.02(18.75) + 0.02(0.2)(90) + 0.02(0.2)(0.5)(90)$

$= 0.92\ ns$

[C]

$Write\ Time\ [L1\ to\ L2] = 15 + 3.75 = 18.75\ ns$

$Miss\ Time\ [L2\ in\ Memory] = 90\ ns$

$Avg.\ Memory\ Access\ Time\ [Write] = 0.05(18.75) + 0.05(0.2)(90) + 0.05(0.2)(0.5)(90)$

$= 2.29\ ns$

3.)

[A]

4 entry cache $\rightarrow n\%4$

Instruction	Memory	Cache
Fld f0, 0(x0)	Load M[0]; *Miss*	4, 1, -, -, -, -, -, -
Fld f2, 0(x2)	Load M[16]; *Miss*	4, 1, 7, 9, -, -, -, -
Fsd f2, 0(x2)	Store M[16]; *Hit*	4, 1, 28, 9, -, -, -, -
Fld f2, 0(x2)	Load M[24]; *Hit*	4, 1, 28, 9, -, -, -, -
Fsd f2, 0(x2)	Store M[24]; *Hit*	4, 1, 28, 36, -, -, -, -
Fld f2, 0(x2)	Load M[32]; *Miss*	4, 1, 28, 36, 5, 3, -, -
Fsd f2, 0(x2)	Store M[32]; *Hit*	4, 1, 28, 36, 20, 3, -, -
Fld f2, 0(x2)	Load M[40]; *Hit*	4, 1, 28, 36, 20, 3, -, -
Fsd f2, 0(x2)	Store M[40]; *Hit*	4, 1, 28, 36, 20, 12, -, -
Fld f2, 0(x2)	Load M[48]; *Miss*	4, 1, 28, 36, 20, 12, 1, 2
Fsd f2, 0(x2)	Store M[48]; *Hit*	4, 1, 28, 36, 20, 12, 4, 2
Fld f2, 0(x2)	Load M[56]; *Hit*	4, 1, 28, 36, 20, 12, 4, 2
Fsd f2, 0(x2)	Store M[56]; *Hit*	4, 1, 28, 36, 20, 12, 4, 8
Fld f2, 0(x2)	Load M[64]; *Miss*	6, 8, 28, 36, 20, 12, 4, 8
Fsd f2, 0(x2)	Store M[64]; *Hit*	24, 8, 28, 36, 20, 12, 4, 8
Fld f2, 0(x2)	Load M[72]; *Hit*	24, 8, 28, 36, 20, 12, 4, 8
Fsd f2, 0(x2)	Store M[72]; *Hit*	24, 32, 28, 36, 20, 12, 4, 8
Fld f2, 0(x2)	Load M[80]; *Miss*	24, 32, 7, 3, 20, 12, 4, 8
Fsd f2, 0(x2)	Store M[80]; *Hit*	24, 32, 28, 3, 20, 12, 4, 8

[B]
2-way → $n\%2$

Instruction	Memory	Cache
Fld f0, 0(x0)	Load M[0]; *Miss*	4, 1, -, -, -, -, -, -
Fld f2, 0(x2)	Load M[16]; *Miss*	4, 1, -, -, 7, 9, -, -
Fsd f2, 0(x2)	Store M[16]; *Hit*	4, 1, -, -, 28, 9, -, -
Fld f2, 0(x2)	Load M[24]; *Hit*	4, 1, -, -, 28, 9, -, -
Fsd f2, 0(x2)	Store M[24]; *Hit*	4, 1, -, -, 28, 36, -, -
Fld f2, 0(x2)	Load M[32]; *Miss*	4, 1, 5, 3, 28, 36, -, -
Fsd f2, 0(x2)	Store M[32]; *Hit*	4, 1, 20, 3, 28, 36, -, -
Fld f2, 0(x2)	Load M[40]; *Hit*	4, 1, 20, 3, 28, 36, -, -
Fsd f2, 0(x2)	Store M[40]; *Hit*	4, 1, 20, 12, 28, 36, -, -
Fld f2, 0(x2)	Load M[48]; *Miss*	4, 1, 20, 12, 28, 36, 1, 2
Fsd f2, 0(x2)	Store M[48]; *Hit*	4, 1, 20, 12, 28, 36, 4, 2
Fld f2, 0(x2)	Load M[56]; *Hit*	4, 1, 20, 12, 28, 36, 4, 2
Fsd f2, 0(x2)	Store M[56]; *Hit*	4, 1, 20, 12, 28, 36, 4, 8
Fld f2, 0(x2)	Load M[64]; *Miss*	6, 8, 20, 12, 28, 36, 4, 8
Fsd f2, 0(x2)	Store M[64]; *Hit*	24, 8, 20, 12, 28, 36, 4, 8
Fld f2, 0(x2)	Load M[72]; *Hit*	24, 8, 20, 12, 28, 36, 4, 8
Fsd f2, 0(x2)	Store M[72]; *Hit*	24, 32, 20, 12, 28, 36, 4, 8
Fld f2, 0(x2)	Load M[80]; *Miss*	24, 32, 20, 12, 7, 3, 4, 8
Fsd f2, 0(x2)	Store M[80]; *Hit*	24, 32, 20, 12, 28, 3, 4, 8

4.)

$$AMAT = Hit\,Time + Miss\,Rate \times Miss\,Penalty$$
$$AMAT\,[Data] = 1 + 0.06 \times 16 = 1.96\,cycles$$
$$AMAT\,[Instruction] = 1 + 0.05 \times 16 = 1.8\,cycles$$
$$Avg.\ AMAT = \frac{1.96+1.8}{2} = 1.88\,cycles$$

5.)

[A]

Cache Block	Set	Memory Blocks residing in Cache Blocks
0	0	M0, M8, M16, M24
1	1	M1, M9, M17, M25
2	2	M2, M10, M18, M26
3	3	M3, M11, M19, M27
4	4	M4, M12, M20, M28
5	5	M5, M13, M21, M29
6	6	M6, M14, M22, M30
7	7	M7, M15, M23, M31

[B]

2-way $\rightarrow n\%2$

Cache Block	Set	Memory Blocks residing in Cache Blocks
0	0	M0, M2, M4,… M30
1	1	M1, M3, M5,… M31
2	0	M0, M2, M4,… M30
3	1	M1, M3, M5,… M31
4	0	M0, M2, M4,… M30
5	1	M1, M3, M5,… M31
6	0	M0, M2, M4,… M30
7	1	M1, M3, M5,… M31

6.)

$$Cache\ Miss\ CPI\ =\ 1\ +\ 0.2(0.02)\ \times\ 25\ cycles\ =\ 1.1\ cycles$$

$$Speedup\ =\ \frac{1.1}{1}\ =\ 1.1\ times\ faster$$

7.)

$$Critical\ Word\ First \rightarrow 10\ cycles$$
$$Without\ Critical\ Word\ =\ 10\ +\ (32\ -\ 1) \rightarrow 41\ cycles$$
$$Speedup\ = \frac{41}{10} = 4.1\ times\ faster$$