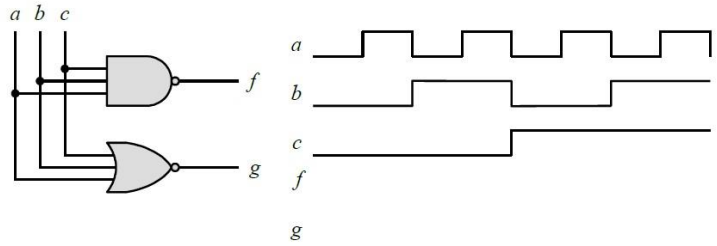
CPE 487 Midterm Exam (100 Points)

Due: October 18, 12:30pm

Signed *Alex Gaskins* Date *10/17/2022*

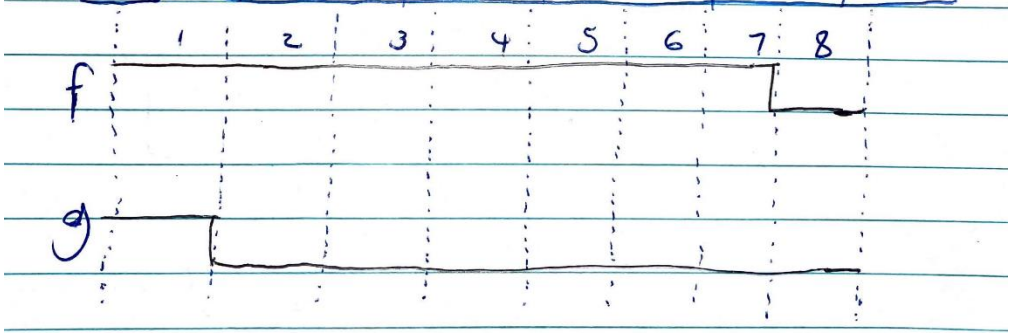
Part1: By hands only

1. Complete the timing diagram of the following circuit by adding the timing trace for **f** and **g**:

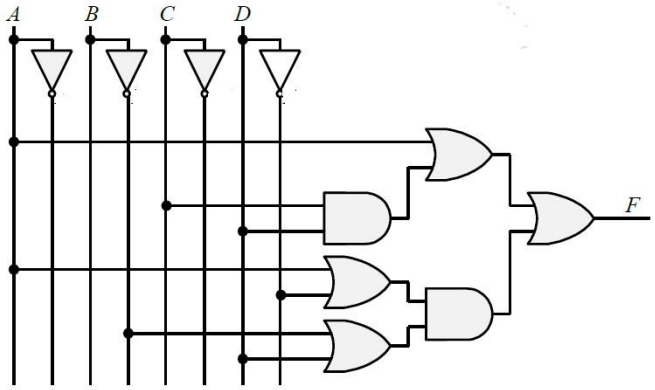


8 Intervals

	a	b	c	AND	f NAND	OR	g NOR
1	0	0	0	0	1	0	1
2	1	0	0	0	1	1	0
3	0	1	0	0	1	1	0
4	1	1	0	0	1	1	0
5	0	0	1	0	1	1	0
6	1	0	1	0	1	1	0
7	0	1	1	0	1	1	0
8	1	1	1	1	0	1	0



2. Write Boolean expression for the following circuits:

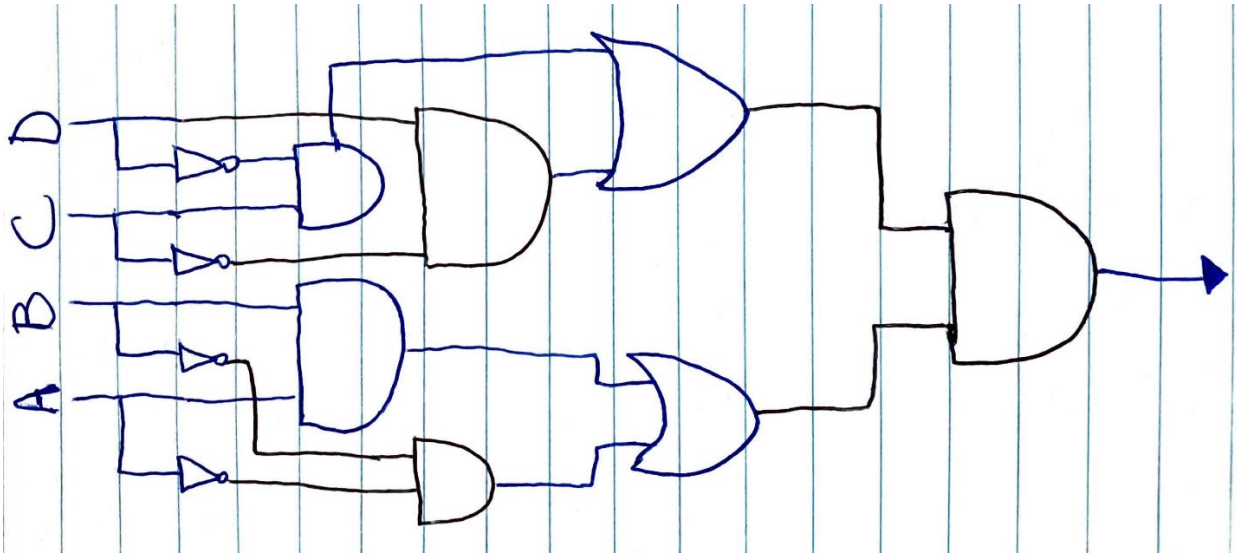


OR = + AND = ×

$F = [A + CD] + [A + D'] \times [B' + D]$

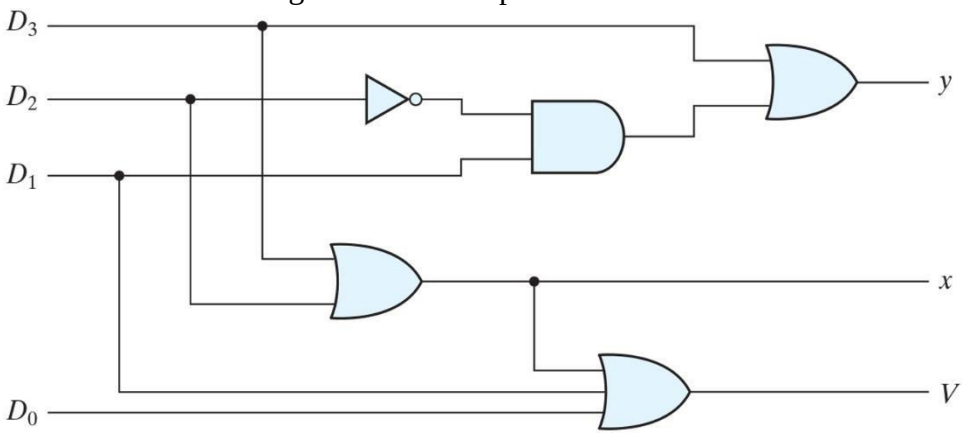
3. Draw the logic diagram corresponding to the following Boolean expression:

(AB + A'B')(CD' + C'D)



Part 2: Using Vivado

4. Use Vivado to write VHDL gate-level description encoder circuit shown below



Code:

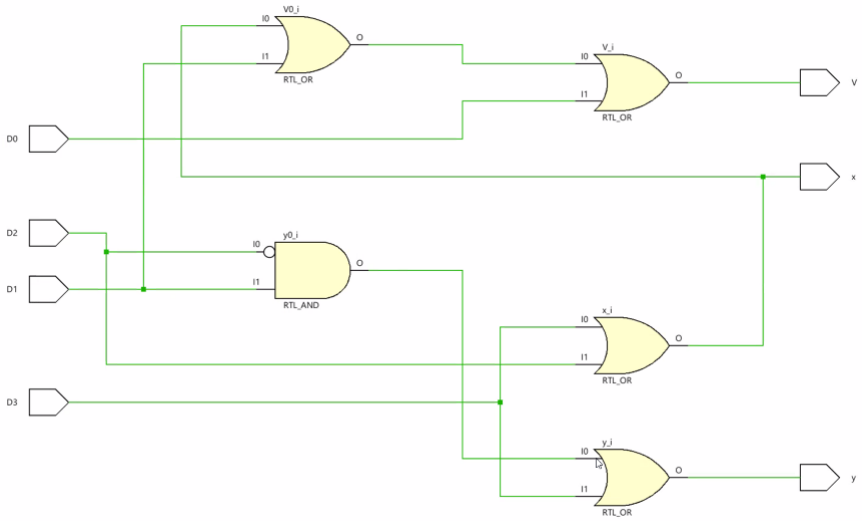
```
Library ieee;
use ieee.std_logic_1164.all;

entity encoder is
 port(D3,D2,D1,D0:in bit; y,x,v:out bit);
end encoder;

architecture logic of encoder is
begin
 y<= D3 or((not(D2) and D1);
 x<= D3 or D2;
 v<= D3 or D2 or D1 or D0;

end logic;
```

Schematic in Vivado:



5. Write behavioral (testbench) description of a four-input encoder circuit shown in #4, above.

Code:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY Testbench_encoder IS
END Testbench_encoder;

ARCHITECTURE behavior OF Testbench_encoder IS
COMPONENT MidTerm
        PORT(
                D3 : IN std_logic;
                D2 : IN std_logic;
                D1 : IN std_logic;
                D0 : IN std_logic;
                y : OUT std_logic;
                x : OUT std_logic;
                v : OUT std_logic );
END COMPONENT;

signal D3 : std_logic := '0';
signal D2 : std_logic := '0';
signal D1 : std_logic := '0';
signal D0 : std_logic := '0';
signal y : std_logic;
signal x : std_logic;
signal v : std_logic;

BEGIN
uut: MidTerm
PORT MAP ( D3 => D3, D2 => D2, D1 => D1, D0 => D0, y => y, x => x, v => v );
   process stim_proc: process begin
        wait for 100 ns;
        D3 <= '1'; D2 <= '0'; D1 <= '0'; D0 <= '1'; wait for 10 ns;
        D3 <= '1'; D2 <= '1'; D1 <= '1'; D0 <= '1'; wait for 10 ns;
        D3 <= '0'; D2 <= '1'; D1 <= '1'; D0 <= '0'; wait for 10 ns;
        D3 <= '1'; D2 <= '1'; D1 <= '0'; D0 <= '1'; wait for 10 ns;
        D3 <= '1'; D2 <= '0'; D1 <= '1'; D0 <= '1'; wait for 10 ns;
        D3 <= '0'; D2 <= '0'; D1 <= '0'; D0 <= '1'; wait for 10 ns;
        D3 <= '0'; D2 <= '0'; D1 <= '0'; D0 <= '0'; wait for 10 ns;
   end process;
END;
```

Output in Vivado: