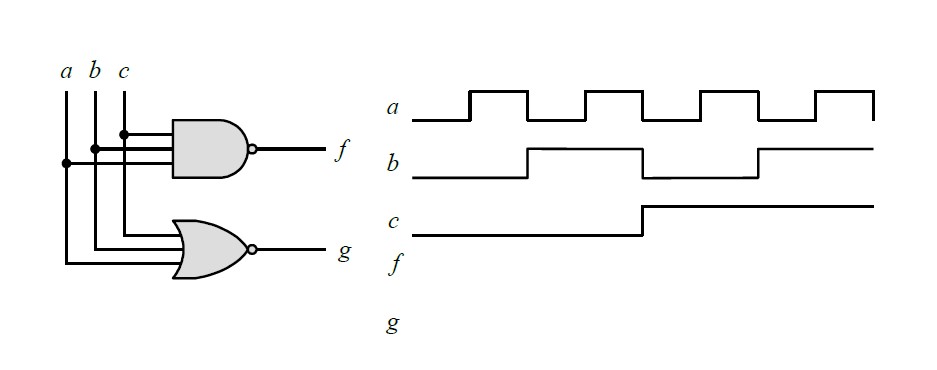
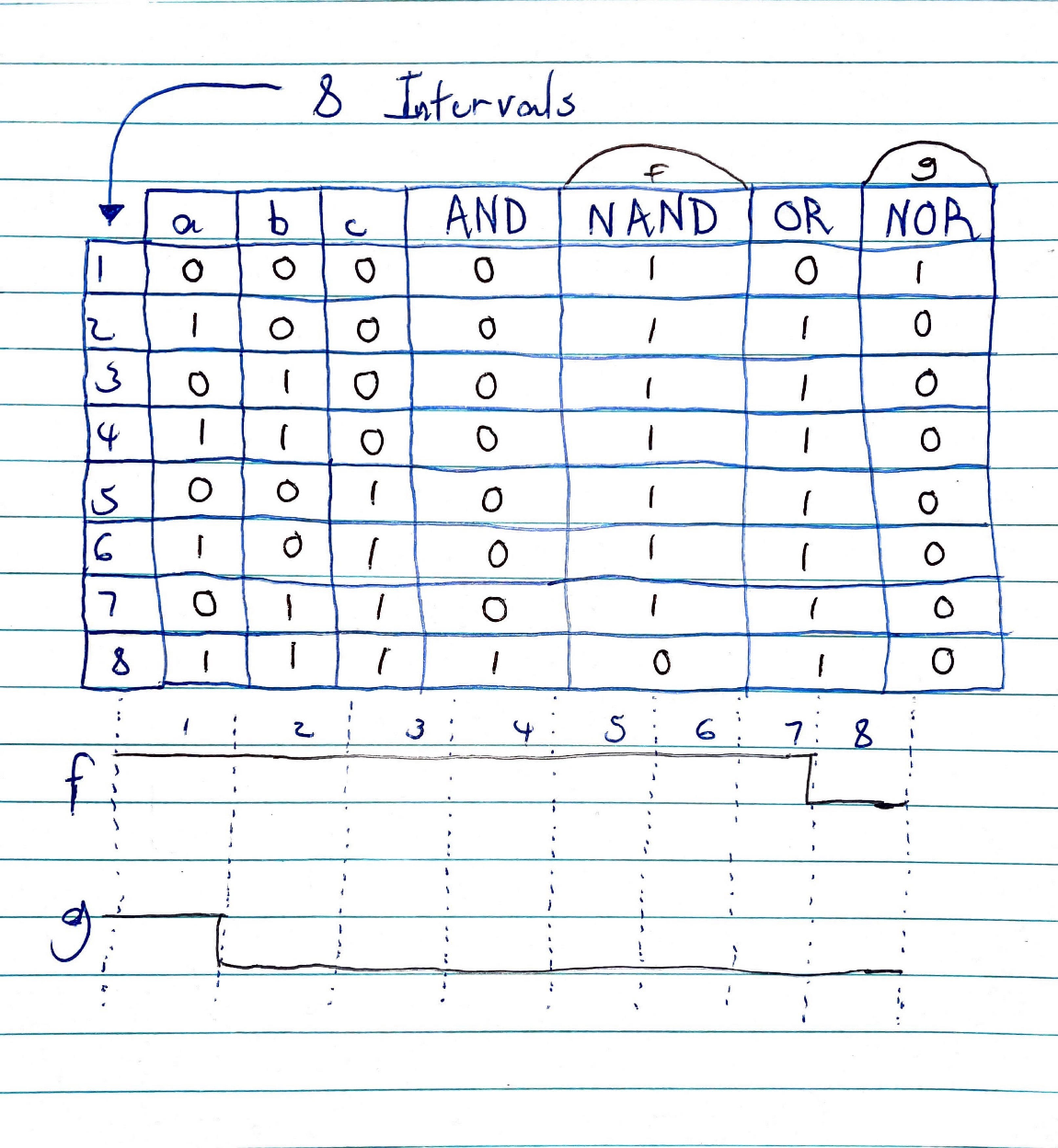
CPE 487 Midterm Exam (100 Points)

Due: October 18, 12:30pm

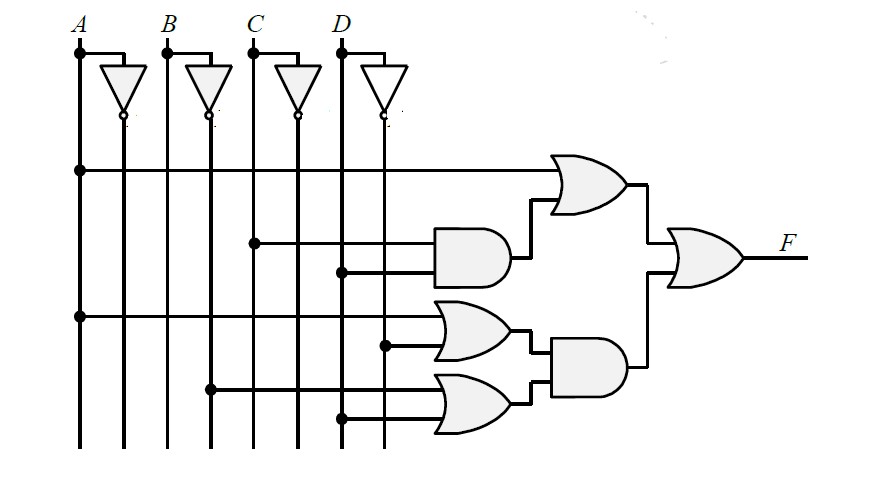
Signed **Alex Gaskins**  Date **10/17/2022**

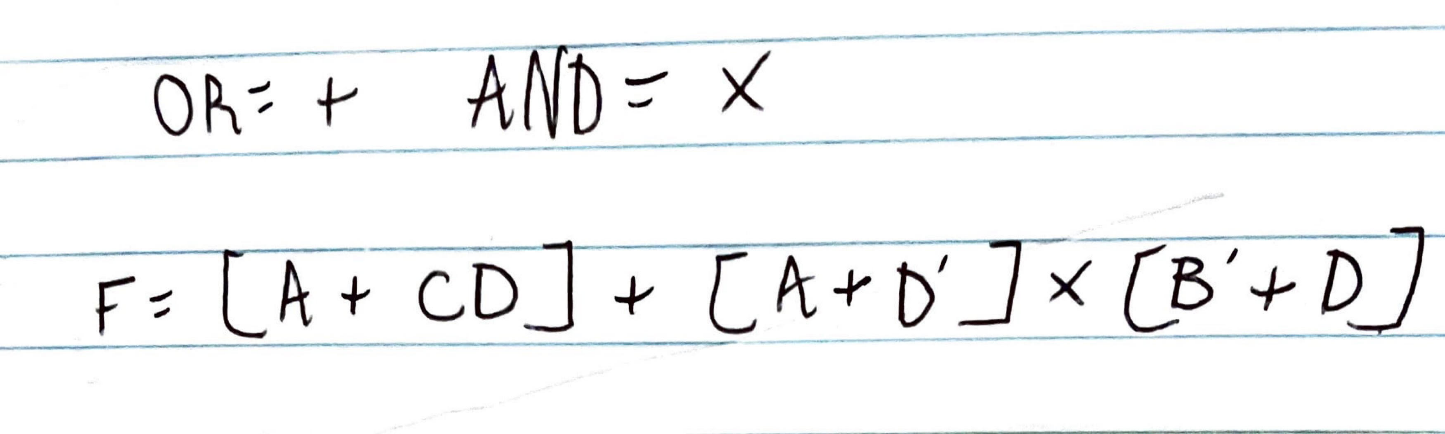
**Part1:** By hands only

1. Complete the timing diagram of the following circuit by adding the timing trace for **f** and **g**:



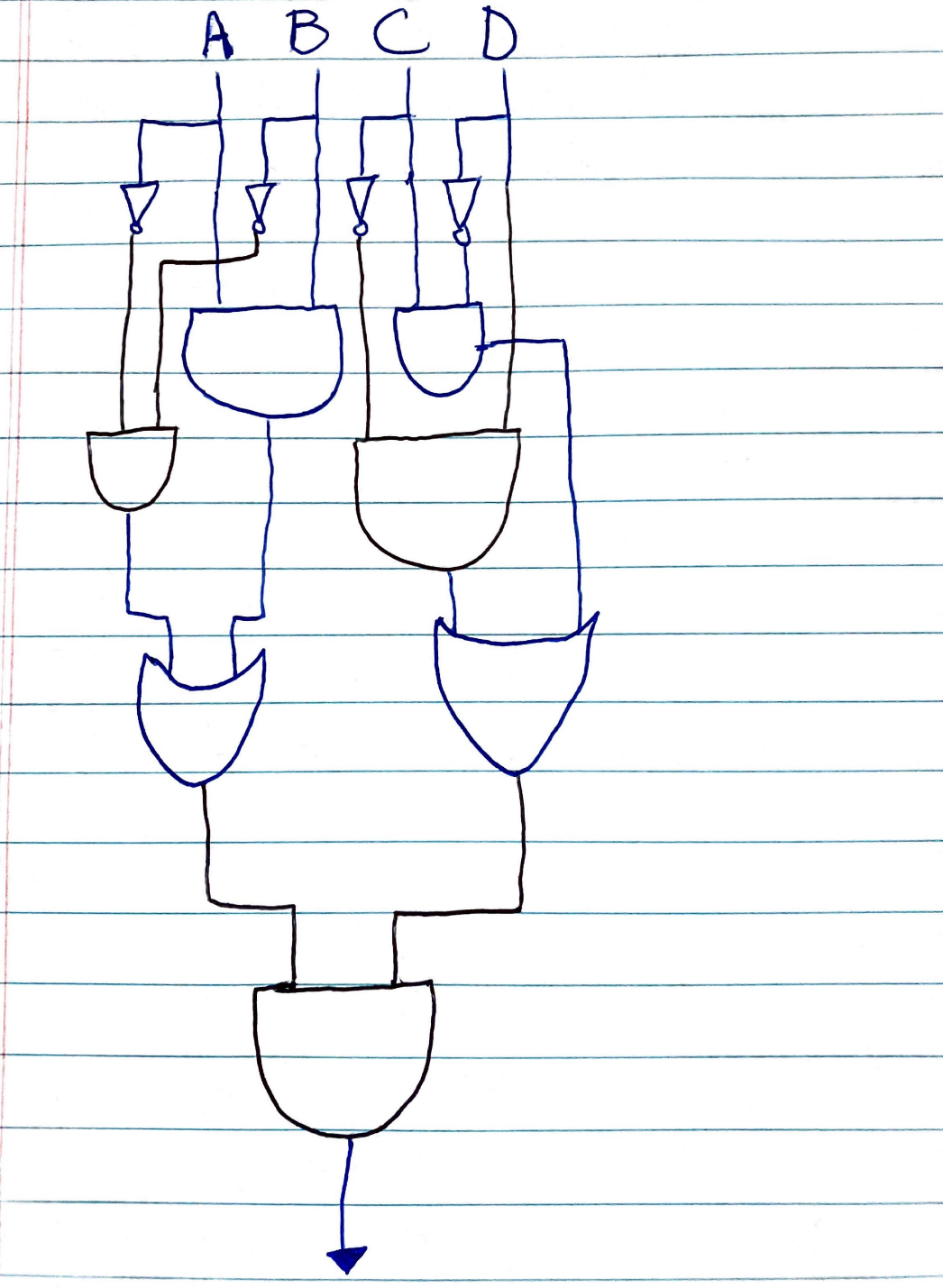
1. Write Boolean expression for the following circuits:





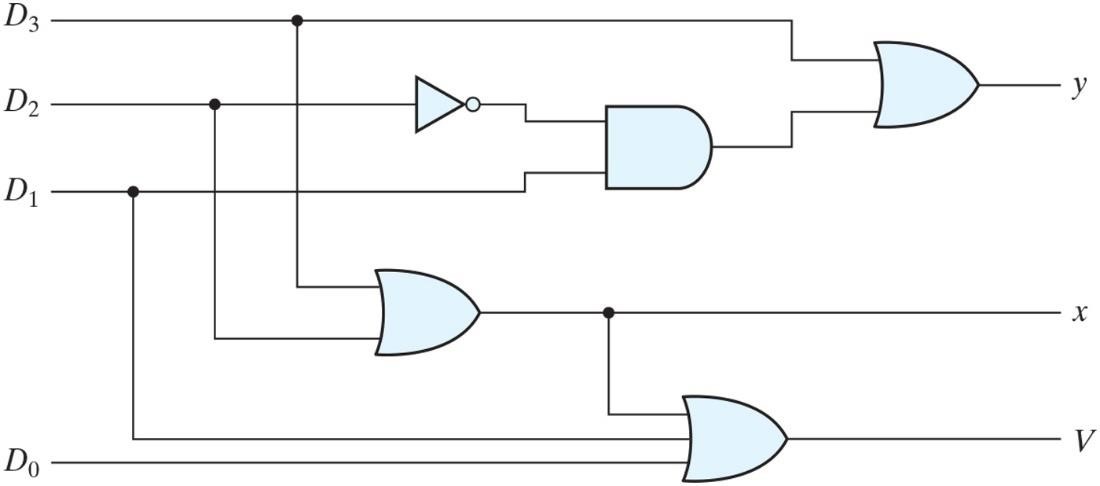
1. Draw the logic diagram corresponding to the following Boolean expression:

(AB + A’B’)(CD’ + C’D)



**Part 2:** Using Vivado

1. Use Vivado to write VHDL gate-level description encoder circuit shown below



**Code:**

Library ieee;

use ieee.std\_logic\_1164.all;

entity encoder is

port(D3,D2,D1,D0:in bit; y,x,v:out bit);

end encoder;

architecture logic of encoder is

begin

y<= D3 or((not(D2) and D1);  
x<= D3 or D2;

v<= D3 or D2 or D1 or D0;

end logic;

**Schematic in Vivado:** Diagram, schematic

Description automatically generated

1. Write behavioral (testbench) description of a four-input encoder circuit shown in #4, above.

**Code:**

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY Testbench\_encoder IS

END Testbench\_encoder;

ARCHITECTURE behavior OF Testbench\_encoder IS

COMPONENT MidTerm

PORT(

D3 : IN std\_logic;

D2 : IN std\_logic;

D1 : IN std\_logic;

D0 : IN std\_logic;

y : OUT std\_logic;

x : OUT std\_logic;

v : OUT std\_logic );

END COMPONENT;

signal D3 : std\_logic := '0';

signal D2 : std\_logic := '0';

signal D1 : std\_logic := '0';

signal D0 : std\_logic := '0';

signal y : std\_logic;

signal x : std\_logic;

signal v : std\_logic;

BEGIN

uut: MidTerm

PORT MAP ( D3 => D3, D2 => D2, D1 => D1, D0 => D0, y => y, x => x, v => v );

process stim\_proc: process begin

wait for 100 ns;

D3 <= '1'; D2 <= '0'; D1 <= '0'; D0 <= '1'; wait for 10 ns;

D3 <= '1'; D2 <= '1'; D1 <= '1'; D0 <= '1'; wait for 10 ns;

D3 <= '0'; D2 <= '1'; D1 <= '1'; D0 <= '0'; wait for 10 ns;

D3 <= '1'; D2 <= '1'; D1 <= '0'; D0 <= '1'; wait for 10 ns;

D3 <= '1'; D2 <= '0'; D1 <= '1'; D0 <= '1'; wait for 10 ns;

D3 <= '0'; D2 <= '0'; D1 <= '0'; D0 <= '1'; wait for 10 ns;

D3 <= '0'; D2 <= '0'; D1 <= '0'; D0 <= '0'; wait for 10 ns;

end process;

END; Top of Form

**Output in Vivado:**

Graphical user interface, application, PowerPoint

Description automatically generated