Roll No._____

Indian Institute of Information Technology Ranchi

Department of CSE

B. Tech End Semester Examination – Autumn Semester 2022-23

Semester: 5th	**Branch: CSE**
Course Code: CS 3007	**Course Name: Advanced Computer Architecture**
Duration: 3 hrs.	**QUESTION PAPER**
Instructions:	**Max Marks: 100**

(1) Answer all the questions. Number in [] indicates marks.
(2) Scientific calculator is allowed in the examination.
(3) Any missing data can be assumed suitably.

1	(a)	Define pipelining with example. Why pipelining is needed? Differentiate RISC and CISC architectures.	[2+2+6]
	(b)	**i).** Consider an unpipelined processor. Assume that it has 1-ns clock cycle and that it uses 4 cycles for ALU operations, 5 cycles for branches and 4 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose due to clock skew and setup, pipelining the processor adds 0.2 ns of overhead to the clock. Find out pipelined and non-pipelined execution time? Ignoring any latency impact, how much speedup in the instruction execution rate will we gain from a pipeline?	[3+3+4]
		Or	
		ii.) Consider an Intel P4 microprocessor with a 16 Kbyte unified L1 cache. The miss rate for this cache is 3% and the hit time is 2 CCs. The processor also has an 8 Mbyte, on-chip L2 cache. 95% of the time, data requests to the L2 cache are found. If data is not found in the L2 cache, a request is made to a 4 Gbyte main memory. The time to service a memory request is 100,000 CCs. On average, it takes 3.5 CCs to process a memory request. How often is data found in main memory?	[10]
2	(a)	With a neat diagram, explain the classic five stage pipeline for a RISC Processor.	[4+6]
	(b)	Point out the differences between data and task parallelism with example. Discuss Flynn's Classification of architecture?	[4+6]
3	(a)	Explain the implementation of basic pipeline for MIPS with a neat diagram Showing the data path. Give all the events with associated registers on every pipe stage of the MIPS pipeline.	[10]
	(b)	How does cache memory mapping work? Explain with a diagram of set associative cache memory mapping technique.	[10]
4	(a)	What is data dependence? Explain with an example & what are the hazards that can happen in pipeline system because of the data dependence?	[3+5]
	(b)	When we can implement loop unrolling method in order to exploit loop level parallelism? How does shared memory architecture and distributed memory architecture play a vital role in modern computing paradigm?	[6+6]
5	(a)	What do you mean by page replacement algorithm? How does it help in systems performance?	[2+4]
	(b)	Consider a main memory with five-page frames and the following sequence of page references: 3, 8, 2, 3, 9, 1, 6, 3, 8, 9, 3, 6, 2, 1, 3. Find out page fault ratios of FIFO, LRU and Optimal? which one of the following page replacement policies is better and why?	[6+6+2]

All The Best