Indian Institute of Information Technology Ranchi

Department of CSE

B. Tech Mid Semester Examination – Autumn Semester 2022-23

Semester: 5th	**Branch: CSE**
Course Code: CS 3007	**Course Name: Advanced Computer Architecture**

QUESTION PAPER

Duration: 2 hrs. **Max Marks: 60**

Instructions:
(1) Answer all the questions. Number in [] indicates marks.
(2) Scientific calculator is allowed in the examination.
(3) Any missing data can be assumed suitably.

1	**(a)**	A stream of numbers is used to perform the combined multiplication and addition operation, such as: for i = 1, 2, 3, ……., 7 Ai* Bi + Ci Can you draw the sub-operations performed in every segment of the pipeline as block diagram?	**[4]**
	(b)	Also compute the number cycle required for executing the above 1(a) instruction using time-space diagram.	**[4]**
	(c)	Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of 4. The same processor is upgraded to a pipelined processor with five stages but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume there are no stalls in the pipeline. The speed up achieved in this pipelined processor is-	**[4]**
	(d)	What is meant by Instruction Level Parallelism?	**[4]**
	(e)	Figure out the differences between RISC and CISC processor.	
2	**(a)**	Consider the following sequence of instructions in the program: 100: I1 101: I2 (JMP 250) 102: I3 . . 250: BI1 How this can be implemented by introducing delay slot until we get the target address.	**[5]**
	(b)	What is meant by dependence? List the type of dependence. How can data dependence be overcome?	**[2+1 +2]**
	(c)	We have 2 designs D1 and D2 for a synchronous pipeline processor. D1 has 5 stage pipeline with execution time of 3 ns, 2 ns, 4 ns, 2 ns and 3 ns. While the design D2 has 8 pipeline stages each with 2 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions?	**[5]**
	(d)	Draw a sample pipelined processor architecture and explain stagewise functionalities.	**[5]**
3	**(a)**	Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate- I. Pipeline cycle time	**[10]**

		II. Non-pipeline execution time III. Speed up ratio IV. Pipeline time for 1000 tasks V. Throughput	

	(b)	Add r1,r2,r3
		Sub r4,r1,r3
		And r6,r1,r7
		Or r8,r1,r9
		Xor r10,r1,r11
		On above example show RAW, WAW, WAR hazards.
			[10]

Roll No._____

End