

libcin

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# Contents

<b>1</b>	<b>FastCCD Communication Library (libcin)</b>	<b>1</b>
<b>2</b>	<b>Module Index</b>	<b>3</b>
2.1	Modules . . . . .	3
<b>3</b>	<b>Class Index</b>	<b>5</b>
3.1	Class List . . . . .	5
<b>4</b>	<b>File Index</b>	<b>7</b>
4.1	File List . . . . .	7
<b>5</b>	<b>Module Documentation</b>	<b>9</b>
5.1	Cin Control Initialization Routines . . . . .	9
5.1.1	Detailed Description . . . . .	9
5.1.2	Function Documentation . . . . .	9
5.1.2.1	cin_ctl_destroy() . . . . .	9
5.1.2.2	cin_ctl_init() . . . . .	10
5.1.2.3	cin_ctl_set_msg_callback() . . . . .	10
5.1.2.4	cin_data_send_magic() . . . . .	11
5.2	Cin Control Read/Rwrite Routines . . . . .	12
5.2.1	Detailed Description . . . . .	12
5.2.2	Function Documentation . . . . .	12
5.2.2.1	cin_ctl_read() . . . . .	12
5.2.2.2	cin_ctl_stream_write() . . . . .	12
5.2.2.3	cin_ctl_write() . . . . .	13

5.2.2.4	<a href="#">cin_ctl_write_with_readback()</a>	13
5.3	<a href="#">Cin Power Routines</a>	15
5.3.1	<a href="#">Detailed Description</a>	15
5.3.2	<a href="#">Function Documentation</a>	15
5.3.2.1	<a href="#">cin_ctl_fo_test_pattern()</a>	15
5.3.2.2	<a href="#">cin_ctl_fp_pwr()</a>	15
5.3.2.3	<a href="#">cin_ctl_pwr()</a>	15
5.4	<a href="#">CIN Firmware Upload Routines</a>	16
5.4.1	<a href="#">Detailed Description</a>	16
5.4.2	<a href="#">Function Documentation</a>	16
5.4.2.1	<a href="#">cin_ctl_load_config()</a>	16
5.4.2.2	<a href="#">cin_ctl_load_firmware()</a>	16
5.4.2.3	<a href="#">cin_ctl_load_firmware_data()</a>	17
5.4.2.4	<a href="#">cin_ctl_load_firmware_file()</a>	17
5.5	<a href="#">CIN FCLK Configuration Routines</a>	18
5.5.1	<a href="#">Detailed Description</a>	18
5.5.2	<a href="#">Function Documentation</a>	18
5.5.2.1	<a href="#">cin_ctl_get_fclk()</a>	18
5.5.2.2	<a href="#">cin_ctl_set_fclk()</a>	18
5.6	<a href="#">CIN Status Routines</a>	19
5.6.1	<a href="#">Detailed Description</a>	19
5.7	<a href="#">CIN Control Bias Routines</a>	20
5.7.1	<a href="#">Detailed Description</a>	20
5.8	<a href="#">CIN Control Timing Routines</a>	21
5.8.1	<a href="#">Detailed Description</a>	21
5.8.2	<a href="#">Function Documentation</a>	21
5.8.2.1	<a href="#">cin_config_get_timing_name()</a>	21
5.9	<a href="#">CIN Data Initialization Routines</a>	22
5.9.1	<a href="#">Detailed Description</a>	22
5.9.2	<a href="#">Function Documentation</a>	22
5.9.2.1	<a href="#">cin_data_destroy()</a>	22
5.9.2.2	<a href="#">cin_data_init()</a>	22
5.10	<a href="#">CIN Data Framestore Functions</a>	25
5.10.1	<a href="#">Detailed Description</a>	25
5.10.2	<a href="#">Function Documentation</a>	25
5.10.2.1	<a href="#">cin_data_framestore_disable()</a>	25
5.10.2.2	<a href="#">cin_data_framestore_skip()</a>	25
5.10.2.3	<a href="#">cin_data_framestore_trigger()</a>	26
5.10.2.4	<a href="#">cin_data_framestore_trigger_enable()</a>	26
5.10.2.5	<a href="#">cin_data_get_framestore_counter()</a>	26

<b>6 Class Documentation</b>	<b>29</b>
6.1 cin_config_timing Struct Reference	29
6.1.1 Member Data Documentation	29
6.1.1.1 cols	29
6.1.1.2 data	29
6.1.1.3 data_len	29
6.1.1.4 fclk_freq	30
6.1.1.5 framestore	30
6.1.1.6 name	30
6.1.1.7 overscan	30
6.1.1.8 rows	30
6.2 cin_ctl Struct Reference	30
6.2.1 Member Data Documentation	31
6.2.1.1 fclk_time_factor	31
6.3 cin_ctl_id Struct Reference	31
6.4 cin_ctl_listener Struct Reference	31
6.5 cin_ctl_pwr_mon_t Struct Reference	32
6.6 cin_ctl_pwr_val Struct Reference	32
6.7 cin_data Struct Reference	32
6.8 cin_data_callbacks Struct Reference	33
6.9 cin_data_descramble_map_t Struct Reference	33
6.10 cin_data_frame Struct Reference	34
6.11 cin_data_packet Struct Reference	34
6.12 cin_data_proc Struct Reference	34
6.13 cin_data_stats Struct Reference	35
6.14 cin_data_threads Struct Reference	35
6.15 cin_map_t Struct Reference	35
6.16 cin_port Struct Reference	36
6.17 fifo Struct Reference	36

<b>7 File Documentation</b>	<b>37</b>
7.1 src/cin.h File Reference	37
7.1.1 Detailed Description	42
7.1.2 LICENSE	43
7.1.3 DESCRIPTION	43
7.1.4 Macro Definition Documentation	43
7.1.4.1 CIN_CONFIG_MAX_TIMING_DATA	43
7.1.4.2 CIN_CONFIG_MAX_TIMING_MODES	43
7.1.4.3 CIN_CTL_BIAS_OFFSET	44
7.2 src/cin_register_map.h File Reference	44
7.2.1 Detailed Description	49
7.2.2 LICENSE	49
7.2.3 DESCRIPTION	49
7.2.4 TIMING	49
7.2.5 Macro Definition Documentation	49
7.2.5.1 CMD_DISABLE_CLKS	50
7.2.5.2 CMD_ENABLE_CLKS	50
7.2.5.3 CMD_FCLK_250	50
7.2.5.4 CMD_FCLK_COMMIT	50
7.2.5.5 CMD_MON_START	50
7.2.5.6 CMD_MON_STOP	50
7.2.5.7 CMD_PS_ENABLE	50
7.2.5.8 CMD_PS_POWERDOWN	50
7.2.5.9 CMD_READ_REG	51
7.2.5.10 CMD_RESET_FRAME_COUNT	51
7.2.5.11 CMD_SEND_FCRIC_CONFIG	51
7.2.5.12 CMD_SEND_SYNC_PULSE	51
7.2.5.13 CMD_SYNC_DETECTOR2READOUT	51
7.2.5.14 CMD_WR_CCD_BIAS_REG	51
7.2.5.15 CMD_WR_CCD_CLOCK_REG	51

7.2.5.16	REG_BIASCONFIGREGISTER0_REG . . . . .	51
7.2.5.17	REG_BIASREGISTERDATAOUT . . . . .	52
7.2.5.18	REG_CLOCK_EN_REG . . . . .	52
7.2.5.19	REG_CLOCKCONFIGREGISTER0_REG . . . . .	52
7.2.5.20	REG_COMMAND . . . . .	52
7.2.5.21	REG_DEBUGCOUNTER04_REG . . . . .	52
7.2.5.22	REG_DELAYTOSHUTTERLSB_REG . . . . .	52
7.2.5.23	REG_ETH_ENABLE . . . . .	52
7.2.5.24	REG_ETH_RESET . . . . .	53
7.2.5.25	REG_EXPOSURETIMELSB_REG . . . . .	53
7.2.5.26	REG_EXPOSURETIMEMSB_REG . . . . .	53
7.2.5.27	REG_FCLK_I2C_ADDRESS . . . . .	53
7.2.5.28	REG_FCLK_I2C_DATA_RD . . . . .	53
7.2.5.29	REG_FCLK_I2C_DATA_WR . . . . .	53
7.2.5.30	REG_FCLK_SET5 . . . . .	53
7.2.5.31	REG_FPGA_VERSION . . . . .	54
7.2.5.32	REG_FRM_10GbE_SEL . . . . .	54
7.2.5.33	REG_FRM_FPGA_VERSION . . . . .	54
7.2.5.34	REG_FRM_RESET . . . . .	54
7.2.5.35	REG_FRM_SANDBOX_REG0F . . . . .	54
7.2.5.36	REG_FRM_STREAM_TYPE . . . . .	54
7.2.5.37	REG_IMON_ADC0_CHF . . . . .	54
7.2.5.38	REG_MAC_CFG_VECTOR1 . . . . .	54
7.2.5.39	REG_MAC_CFG_VECTOR2 . . . . .	55
7.2.5.40	REG_MAC_STATS2_FAB2B1 . . . . .	55
7.2.5.41	REG_PHY1_MDIO_CMD . . . . .	55
7.2.5.42	REG_PS_ENABLE . . . . .	55
7.2.5.43	REG_PS_SYNC_DIV0 . . . . .	55
7.2.5.44	REG_PS_SYNC_DIV1 . . . . .	55
7.2.5.45	REG_PS_SYNC_DIV2 . . . . .	55
7.2.5.46	REG_PS_SYNC_DIV3 . . . . .	55
7.2.5.47	REG_PS_SYNC_DIV4 . . . . .	56
7.2.5.48	REG_SANDBOX_REG0F . . . . .	56
7.2.5.49	REG_SI570_REG3 . . . . .	56
7.2.5.50	REG_SRAM_COMMAND . . . . .	56
7.2.5.51	REG_SRAM_STATUS0 . . . . .	56
7.2.5.52	REG_STREAM_TYPE . . . . .	56
7.2.5.53	REG_TRIGGERMASK_REG . . . . .	56
7.2.5.54	REG_TRIGGERREPETITIONTIMELSB_REG . . . . .	56
7.2.5.55	REG_TRIGGERREPETITIONTIMEMSB_REG . . . . .	56





# Chapter 1

## FastCCD Communication Library (libcin)

### Introduction

This library, based in C is designed to control the FastCCD detector from Lawrence Berkeley National Laboratory. It controls both camera control functions and data acquisition (frame acquisition). It is separated into two distinct parts, the control part ,`cin_ctl`, and the data (image) part named `cin_data`. It was written in part for use with `areaDetector`.

### Prerequisites

The library relies on the following:

- `libconfig` (Used for nice config files)
- `libpthread` (Used for threading)
- `librt` (Used for time functions)

### Installation

Installation of the library is like most unix based source packages:

```
./make
./make doc
./make test
./make install
```

### TCP/IP Stack Tuning

In order for the CIN data to operate efficiently, the 10G interface on the host computer needs to be tuned. This needs to be done by adding the following to the file `/etc/sysctl.conf`.

```
# Increase the maximum buffer that user programs can request
# 2147483647 = 2048 Mb
net.core.rmem_max=2147483647
net.core.wmem_max=2147483647
# Set a default value 10 times bigger
net.core.rmem_default=1000000
net.core.wmem_default=1000000
# increase the length of the processor input queue
net.core.netdev_max_backlog = 250000
# recommended for hosts with jumbo frames enabled
net.ipv4.tcp_mtu_probing=1
```

These can be reread by the system without rebooting by entering the command:

```
$sudo sysctl --system
```

## Versioning

For the versions available, see the [tags on this repository](#).

## Authors

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See also the list of [contributors](#) who participated in this project.

## License

This project is licensed under the BSD License - see the [LICENSE](#) file for details

## Acknowledgments

A huge thanks to Peter Dennes, John Joseph and the detector team at LBNL and the team at Sydor Instruments.

## Chapter 2

# Module Index

### 2.1 Modules

Here is a list of all modules:

Cin Control Initialization Routines . . . . .	9
Cin Control Read/Rwrite Routines . . . . .	12
Cin Power Routines . . . . .	15
CIN Firmware Upload Routines . . . . .	16
CIN FCLK Configuration Routines . . . . .	18
CIN Status Routines . . . . .	19
CIN Control Bias Routines . . . . .	20
CIN Control Timing Routines . . . . .	21
CIN Data Initialization Routines . . . . .	22
CIN Data Framestore Functions . . . . .	25



## Chapter 3

# Class Index

### 3.1 Class List

Here are the classes, structs, unions and interfaces with brief descriptions:

<a href="#">cin_config_timing</a>	29
<a href="#">cin_ctl</a>	30
<a href="#">cin_ctl_id</a>	31
<a href="#">cin_ctl_listener</a>	31
<a href="#">cin_ctl_pwr_mon_t</a>	32
<a href="#">cin_ctl_pwr_val</a>	32
<a href="#">cin_data</a>	32
<a href="#">cin_data_callbacks</a>	33
<a href="#">cin_data_descramble_map_t</a>	33
<a href="#">cin_data_frame</a>	34
<a href="#">cin_data_packet</a>	34
<a href="#">cin_data_proc</a>	34
<a href="#">cin_data_stats</a>	35
<a href="#">cin_data_threads</a>	35
<a href="#">cin_map_t</a>	35
<a href="#">cin_port</a>	36
<a href="#">fifo</a>	36



## Chapter 4

# File Index

### 4.1 File List

Here is a list of all documented files with brief descriptions:

src/ <a href="#">cin.h</a> . . . . .	<a href="#">37</a>
src/ <a href="#">cin_register_map.h</a> . . . . .	<a href="#">44</a>
src/ <b>cinregisters.h</b> . . . . .	??
src/ <b>common.h</b> . . . . .	??
src/ <b>config.h</b> . . . . .	??
src/ <b>control.h</b> . . . . .	??
src/ <b>data.h</b> . . . . .	??
src/ <b>descramble.h</b> . . . . .	??
src/ <b>descramble_map.h</b> . . . . .	??
src/ <b>fifo.h</b> . . . . .	??
src/ <b>report.h</b> . . . . .	??





## Chapter 5

# Module Documentation

### 5.1 Cin Control Initialization Routines

#### Functions

- int [cin\\_ctl\\_init](#) ([cin\\_ctl\\_t](#) \*cin, char \*addr, uint16\_t port, uint16\_t sport, char \*bind\_addr, uint16\_t bind\_port, uint16\_t bind\_sport)
- int [cin\\_ctl\\_destroy](#) ([cin\\_ctl\\_t](#) \*cin)
- void [cin\\_ctl\\_set\\_msg\\_callback](#) ([cin\\_ctl\\_t](#) \*cin, cin\_ctl\_msg\_callback callback, void \*ptr)
- int [cin\\_data\\_send\\_magic](#) ([cin\\_data\\_t](#) \*cin)

#### 5.1.1 Detailed Description

#### 5.1.2 Function Documentation

##### 5.1.2.1 [cin\\_ctl\\_destroy\(\)](#)

```
int cin_ctl_destroy (
    cin\_ctl\_t * cin )
```

Destroy (close) the cin control library

Close connections, free memory and exit library

#### Parameters

<i>cin</i>	handle to cin library
------------	-----------------------

#### Returns

Returns 0 on success non-zero if error

### 5.1.2.2 cin\_ctl\_init()

```
int cin_ctl_init (
    cin_ctl_t * cin,
    char * addr,
    uint16_t port,
    uint16_t sport,
    char * bind_addr,
    uint16_t bind_port,
    uint16_t bind_sport )
```

Initialize the cin control library

Initialize the control structures and communications with the CIN via the control interface. This function opens the UDP ports and starts a listening thread to receive packets from the CIN.

#### Parameters

<i>cin</i>	handle to cin library
<i>addr</i>	ip address of CIN base address
<i>port</i>	UDP port of cin
<i>sport</i>	stream output UDP port of cin
<i>bind_addr</i>	ip address to bind to
<i>bind_port</i>	input udp port of cin
<i>bind_sport</i>	stream input udp port of cin

#### Returns

Returns 0 on success non-zero if error

### 5.1.2.3 cin\_ctl\_set\_msg\_callback()

```
void cin_ctl_set_msg_callback (
    cin_ctl_t * cin,
    cin_ctl_msg_callback callback,
    void * ptr )
```

Register a function to receive status messages

Close connections, free memory and exit library

#### Parameters

<i>cin</i>	handle to cin library
<i>callback</i>	function pointer to callback function
<i>ptr</i>	user pointer which is passed to callback routine

#### 5.1.2.4 cin\_data\_send\_magic()

```
int cin_data_send_magic (  
    cin_data_t * cin )
```

Send a magic packet to the CIN to initialize data

##### Parameters

<i>cin</i>	handle to cin library
------------	-----------------------

##### Returns

Returns 0 on success non-zero if error

## 5.2 Cin Control Read/Rwrite Routines

### Functions

- int [cin\\_ctl\\_read](#) ([cin\\_ctl\\_t](#) \*cin, uint16\_t reg, uint16\_t \*val, int wait)
- int [cin\\_ctl\\_write](#) ([cin\\_ctl\\_t](#) \*cin, uint16\_t reg, uint16\_t val, int wait)
- int [cin\\_ctl\\_stream\\_write](#) ([cin\\_ctl\\_t](#) \*cin, unsigned char \*val, int size)
- int [cin\\_ctl\\_write\\_with\\_readback](#) ([cin\\_ctl\\_t](#) \*cin, uint16\_t reg, uint16\_t val)

### 5.2.1 Detailed Description

### 5.2.2 Function Documentation

#### 5.2.2.1 cin\_ctl\_read()

```
int cin_ctl_read (
    cin\_ctl\_t * cin,
    uint16_t reg,
    uint16_t * val,
    int wait )
```

Read register from CIN

#### Parameters

<i>cin</i>	handle to cin library
<i>reg</i>	register to read
<i>val</i>	variable to read value of register to
<i>wait</i>	if non-zero, wait a predefined time before read command (for i2c)

#### Returns

Returns 0 on success non-zero if error

#### 5.2.2.2 cin\_ctl\_stream\_write()

```
int cin_ctl_stream_write (
    cin\_ctl\_t * cin,
    unsigned char * val,
    int size )
```

Write stream data to CIN

**Parameters**

<i>cin</i>	handle to cin library
<i>val</i>	array of values to write
<i>size</i>	size of array pointed to by val

Write stream data to cin in form of 16 bit array.

**Returns**

Returns 0 on success non-zero if error

**5.2.2.3 cin\_ctl\_write()**

```
int cin_ctl_write (
    cin_ctl_t * cin,
    uint16_t reg,
    uint16_t val,
    int wait )
```

Write register to CIN

**Parameters**

<i>cin</i>	handle to cin library
<i>reg</i>	register to write to
<i>val</i>	value to write to register
<i>wait</i>	if non-zero

Write register value to CIN. If wait is non-zero then wait a sleep time of i CIN\_CTL\_WRITE\_SLEEP before releasing the mutex to add flow control to the cin.

**Returns**

Returns 0 on success non-zero if error

**5.2.2.4 cin\_ctl\_write\_with\_readback()**

```
int cin_ctl_write_with_readback (
    cin_ctl_t * cin,
    uint16_t reg,
    uint16_t val )
```

Write register to CIN with readback verification

**Parameters**

<i>cin</i>	handle to cin library
<i>reg</i>	register to write to
<i>val</i>	value to write to register

Write register value to CIN. Follow write with read of register and compare value. CIN\_CTL\_WRITE\_SLEEP before releasing the mutex to add flow control to the cin.

**Returns**

Returns 0 on success non-zero if error

## 5.3 Cin Power Routines

### Functions

- int `cin_ctl_pwr` (`cin_ctl_t` \*cin, int pwr)
- int `cin_ctl_fp_pwr` (`cin_ctl_t` \*cin, int pwr)
- int `cin_ctl_fo_test_pattern` (`cin_ctl_t` \*cin, int on\_off)

#### 5.3.1 Detailed Description

These routine control power to the CIN for the Frame FPGA and the Front Panel

#### 5.3.2 Function Documentation

##### 5.3.2.1 `cin_ctl_fo_test_pattern()`

```
int cin_ctl_fo_test_pattern (
    cin_ctl_t * cin,
    int on_off )
```

Control Fiber Optic Interface Test Pattern

Turn on and off the fiber optic test pattern. The FO modules transmit a test pattern to indicate that communication with the data modules is correct. This routine turns on and off the modules. If on\_off is 0 then the FO test pattern is turned off, and if on\_off is 1 then the FO test pattern is turned on. Note: this routine manipulates the fCRIC mask, so you may need to reconfigure the fCRICs after using it.

cin handle to cin library on\_off test pattern status

CIN\_OK on success, CIN\_ERROR on an error

##### 5.3.2.2 `cin_ctl_fp_pwr()`

```
int cin_ctl_fp_pwr (
    cin_ctl_t * cin,
    int pwr )
```

Control CIN Front Panel Power

Turn on and off the CIN Front Panel power. The front panel power powers either the fiber optic modules or the LVDS lines to the camera. If pwr is 0 then turn off FP power and if pwr is 1 turn on the FP power.

cin handle to cin library pwr power status

CIN\_OK on success, CIN\_ERROR on an error

##### 5.3.2.3 `cin_ctl_pwr()`

```
int cin_ctl_pwr (
    cin_ctl_t * cin,
    int pwr )
```

Control CIN Frame FPGA Power

Turn on and off the frame FPGA power. If pwr is 0 then turn off power. If pwr is 1 turn on power.

cin handle to cin library pwr power status

CIN\_OK on success, CIN\_ERROR on an error

## 5.4 CIN Firmware Upload Routines

### Functions

- int [cin\\_ctl\\_load\\_firmware](#) ([cin\\_ctl\\_t](#) \*cin)
- int [cin\\_ctl\\_load\\_firmware\\_file](#) ([cin\\_ctl\\_t](#) \*cin, char \*filename)
- int [cin\\_ctl\\_load\\_firmware\\_data](#) ([cin\\_ctl\\_t](#) \*cin, unsigned char \*data, int data\_len)
- int [cin\\_ctl\\_load\\_config](#) ([cin\\_ctl\\_t](#) \*cin, const char \*filename)

### 5.4.1 Detailed Description

These routines control the upload of firmware to the frame FPGA in the CIN. The firmware can be uploaded using either a external file or an array of unsigned char (bytes). The function [cin\\_ctl\\_load\\_firmware\(\)](#) loads the pre-compiled firmware.

### 5.4.2 Function Documentation

#### 5.4.2.1 [cin\\_ctl\\_load\\_config\(\)](#)

```
int cin_ctl_load_config (  
    cin\_ctl\_t * cin,  
    const char * filename )
```

Load FPGA config file

Upload a FPGA config file to the CIN. This file is a simple file with each line containing a 4 digit hex value for the register location and a 4 digit hex value for the value to be written to the register.

cin handle to the cin library filename filename to load

CIN\_OK on success, CIN\_ERROR on an error

#### 5.4.2.2 [cin\\_ctl\\_load\\_firmware\(\)](#)

```
int cin_ctl_load_firmware (  
    cin\_ctl\_t * cin )
```

Load the pre-compiled frame FPGA firmware

cin handle to cin library

CIN\_OK on success, CIN\_ERROR on an error



#### 5.4.2.3 cin\_ctl\_load\_firmware\_data()

```
int cin_ctl_load_firmware_data (
    cin_ctl_t * cin,
    unsigned char * data,
    int data_len )
```

Load the frame FPGA firmware from char array

cin handle to cin library data array of binary FPGA firmware data\_len length of binary data

CIN\_OK on success, CIN\_ERROR on an error

#### 5.4.2.4 cin\_ctl\_load\_firmware\_file()

```
int cin_ctl_load_firmware_file (
    cin_ctl_t * cin,
    char * filename )
```

Load the frame FPGA firmware from file

cin handle to cin library filename file containing the binary FPGA firmware

CIN\_OK on success, CIN\_ERROR on an error

## 5.5 CIN FCLK Configuration Routines

### Functions

- int [cin\\_ctl\\_get\\_fclk](#) ([cin\\_ctl\\_t](#) \*cin, int \*clkfreq)
- int [cin\\_ctl\\_set\\_fclk](#) ([cin\\_ctl\\_t](#) \*cin, int clkfreq)

### 5.5.1 Detailed Description

These routines configure the Internal Frame FPGA Clock (FCLK) frequency.

### 5.5.2 Function Documentation

#### 5.5.2.1 cin\_ctl\_get\_fclk()

```
int cin_ctl_get_fclk (  
    cin\_ctl\_t * cin,  
    int * clkfreq )
```

Get the current frame FPGA clock frequency

cin handle to cin library clkfreq clock frequency

CIN\_OK on success, CIN\_ERROR on an error

#### 5.5.2.2 cin\_ctl\_set\_fclk()

```
int cin_ctl_set_fclk (  
    cin\_ctl\_t * cin,  
    int clkfreq )
```

Set the frame FPGA clock frequency

cin handle to cin library clkfreq clock frequency to set

CIN\_OK on success, CIN\_ERROR on an error

## 5.6 CIN Status Routines

### Functions

- int **cin\_ctl\_get\_cfg\_fpga\_status** ([cin\\_ctl\\_t](#) \*cin, uint16\_t \*\_val)
- int **cin\_ctl\_get\_id** ([cin\\_ctl\\_t](#) \*cin, [cin\\_ctl\\_id\\_t](#) \*\_val)
- int **cin\_ctl\_get\_dcm\_status** ([cin\\_ctl\\_t](#) \*cin, uint16\_t \*\_val)
- int **cin\_ctl\_get\_power\_status** ([cin\\_ctl\\_t](#) \*cin, int full, int \*pwr, [cin\\_ctl\\_pwr\\_mon\\_t](#) \*values)

### 5.6.1 Detailed Description

Status Routines

## 5.7 CIN Control Bias Routines

### Functions

- int **cin\_ctl\_set\_bias** ([cin\\_ctl\\_t](#) \*cin, int val)
- int **cin\_ctl\_get\_bias** ([cin\\_ctl\\_t](#) \*cin, int \*val)
- int **cin\_ctl\_set\_bias\_regs** ([cin\\_ctl\\_t](#) \*cin, uint16\_t \*vals, int verify)
- int **cin\_ctl\_get\_bias\_regs** ([cin\\_ctl\\_t](#) \*cin, uint16\_t \*vals)
- int **cin\_ctl\_set\_bias\_voltages** ([cin\\_ctl\\_t](#) \*cin, float \*voltage, int verify)
- int **cin\_ctl\_get\_bias\_voltages** ([cin\\_ctl\\_t](#) \*cin, float \*voltage, uint16\_t \*regs)

### 5.7.1 Detailed Description

Initialization group

## 5.8 CIN Control Timing Routines

### Functions

- int `cin_ctl_set_timing_regs` (`cin_ctl_t` \*cin, uint16\_t \*vals, int vals\_len)
- int `cin_ctl_get_timing_regs` (`cin_ctl_t` \*cin, uint16\_t \*vals, int vals\_len)
- int `cin_config_read_file` (`cin_ctl_t` \*cin, const char \*file)
- int `cin_config_get_timing_name` (`cin_ctl_t` \*cin, int num, char \*\*name)

### 5.8.1 Detailed Description

Timing setup group

### 5.8.2 Function Documentation

#### 5.8.2.1 `cin_config_get_timing_name()`

```
int cin_config_get_timing_name (  
    cin_ctl_t * cin,  
    int num,  
    char ** name )
```

Get the name of the timing config options

cin handle to cin library num number of timing option name char array of name

CIN\_OK on success, CIN\_ERROR on an error

## 5.9 CIN Data Initialization Routines

### Functions

- int `cin_data_init` (`cin_data_t` \*cin, char \*addr, uint16\_t port, char \*bind\_addr, uint16\_t bind\_port, int rcvbuf, int packet\_buffer\_len, int frame\_buffer\_len, cin\_data\_callback push\_callback, cin\_data\_callback pop\_callback, void \*usr\_ptr)
- void `cin_data_destroy` (`cin_data_t` \*cin)

### 5.9.1 Detailed Description

Initialization group

### 5.9.2 Function Documentation

#### 5.9.2.1 cin\_data\_destroy()

```
void cin_data_destroy (
    cin_data_t * cin )
```

Close the cin data library and cleanup

Stop all the processing threads and join them to the main thread. This function blocks until all threads have joined the main thread (program). This should be called to clean up the library before the program is exited

#### Parameters

<i>cin</i>	Handle to cin data library
------------	----------------------------

#### 5.9.2.2 cin\_data\_init()

```
int cin_data_init (
    cin_data_t * cin,
    char * addr,
    uint16_t port,
    char * bind_addr,
    uint16_t bind_port,
    int rcvbuf,
    int packet_buffer_len,
    int frame_buffer_len,
    cin_data_callback push_callback,
    cin_data_callback pop_callback,
    void * usr_ptr )
```

Initialize the cin data library

Initialize the data handling routines and start the threads for listening.

## Parameters

<i>cin</i>	Handle to cin data library
<i>addr</i>	IP-Address of cin (if NULL defaults to standard)
<i>port</i>	UDP Port of CIN
<i>bind_addr</i>	IP-Address to bind to (if NULL binds to 0.0.0.0)
<i>bind_port</i>	UDP Port of host
<i>rcvbuf</i>	TCP/IP Kernel receive buffer size
<i>packet_buffer_len</i>	Length of packet buffer fifo (in units number of packets)
<i>frame_buffer_len</i>	Length of frame (assembler) buffer fifo (in units of number of frames)
<i>push_callback</i>	This function is called when a data structure is needed
<i>pop_callback</i>	This function is called when an image has been processed
<i>usr_ptr</i>	Pointer passed to callback functions



## 5.10 CIN Data Framestore Functions

### Functions

- void `cin_data_framestore_trigger` (`cin_data_t` \*cin, int count)
- void `cin_data_framestore_skip` (`cin_data_t` \*cin, int count)
- int `cin_data_get_framestore_counter` (`cin_data_t` \*cin)
- void `cin_data_framestore_disable` (`cin_data_t` \*cin)
- void `cin_data_framestore_trigger_enable` (`cin_data_t` \*cin)

### 5.10.1 Detailed Description

Framestore Group

### 5.10.2 Function Documentation

#### 5.10.2.1 `cin_data_framestore_disable()`

```
void cin_data_framestore_disable (  
    cin_data_t * cin )
```

Disable the framestore modes

This function disables the framestore modes (software trigger and skip). If the camera is hardware triggering then the images will start to be processed.

#### Parameters

<code>cin</code>	Handle to the cin library
------------------	---------------------------

#### 5.10.2.2 `cin_data_framestore_skip()`

```
void cin_data_framestore_skip (  
    cin_data_t * cin,  
    int count )
```

Enable framestore skip mode

Enable the framestore skip mode. This function should be called before hardware triggering the camera. This causes the data processing to skip

## Parameters

<i>count</i>	frames from the first images to be read. This is usually done to stop the first few frames from being over exposed.
<i>cin</i>	handle to the <a href="#">cin_data</a> library

5.10.2.3 `cin_data_framestore_trigger()`

```
void cin_data_framestore_trigger (
    cin_data_t * cin,
    int count )
```

Send a framestore (software) trigger

Send a software trigger to the CIN by timestamping the request time and allow images to be processed when recieved after this time. The count option sets the number of frames to trigger. A value of -1 indicated that the trigger should not count images but run indefinitely after the trigger has occurred.

## Parameters

<i>cin</i>	handle to the <a href="#">cin_data</a> library
<i>count</i>	number of frames to trigger

5.10.2.4 `cin_data_framestore_trigger_enable()`

```
void cin_data_framestore_trigger_enable (
    cin_data_t * cin )
```

Enable the framestore trigger mode

This function enables the framestore trigger mode. It cases the images to not be processed pending a call to the function to (software) trigger the camera.

## Parameters

<i>cin</i>	Handle to the cin library
------------	---------------------------

5.10.2.5 `cin_data_get_framestore_counter()`

```
int cin_data_get_framestore_counter (
    cin_data_t * cin )
```

Get the value of the framestore counter

Return the number of frames in the framestore counter. In trigger mode, this returns the number of frames to go. In skip mode, this returns the number of frames that have to be skipped.

#### Parameters

<i>cin</i>	handle to the <a href="#">cin_data</a> library
------------	--

#### Returns

Number of frames to go in trigger



## Chapter 6

# Class Documentation

### 6.1 cin\_config\_timing Struct Reference

#### Public Attributes

- uint16\_t \* [data](#)
- int [data\\_len](#)
- char [name](#) [40]
- int [rows](#)
- int [cols](#)
- int [overscan](#)
- int [fclk\\_freq](#)
- int [framestore](#)

#### 6.1.1 Member Data Documentation

##### 6.1.1.1 cols

```
int cin_config_timing::cols
```

Cols for this timing setup

##### 6.1.1.2 data

```
uint16_t* cin_config_timing::data
```

Pointer to timing data

##### 6.1.1.3 data\_len

```
int cin_config_timing::data_len
```

timing data length

#### 6.1.1.4 fclk\_freq

```
int cin_config_timing::fclk_freq
```

FCLK Frequency to use

#### 6.1.1.5 framestore

```
int cin_config_timing::framestore
```

Flag (not zero means framestore

#### 6.1.1.6 name

```
char cin_config_timing::name[40]
```

String for config name

#### 6.1.1.7 overscan

```
int cin_config_timing::overscan
```

Number of overscan cols for this setup

#### 6.1.1.8 rows

```
int cin_config_timing::rows
```

Rows for this timing setup

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.2 cin\_ctl Struct Reference

### Public Attributes

- char \* **addr**
- char \* **bind\_addr**
- int **port**
- int **bind\_port**
- int **sport**
- int **bind\_sport**
- [cin\\_port\\_t](#) **ctl\_port**
- [cin\\_port\\_t](#) **stream\_port**
- [cin\\_config\\_timing\\_t](#) **timing** [[CIN\\_CONFIG\\_MAX\\_TIMING\\_MODES](#)]
- int **timing\_num**
- [cin\\_config\\_timing\\_t](#) \* **current\_timing**
- float **fclk\_time\_factor**
- [cin\\_ctl\\_listener\\_t](#) \* **listener**
- pthread\_mutex\_t **access**
- pthread\_mutexattr\_t **access\_attr**
- void(\* **msg\_callback**)(const char \*, int, void \*)
- void \* **msg\_callback\_ptr**

## 6.2.1 Member Data Documentation

### 6.2.1.1 fclk\_time\_factor

```
float cin_ctl::fclk_time_factor
```

In micro seconds

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.3 cin\_ctl\_id Struct Reference

### Public Attributes

- uint16\_t **base\_board\_id**
- uint16\_t **base\_serial\_no**
- uint16\_t **base\_fpga\_ver**
- uint16\_t **fabric\_board\_id**
- uint16\_t **fabric\_serial\_no**
- uint16\_t **fabric\_fpga\_ver**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.4 cin\_ctl\_listener Struct Reference

### Public Attributes

- struct [cin\\_port](#) \* **cp**
- [fifo](#) **ctl\_fifo**
- pthread\_t **thread\_id**
- pthread\_barrier\_t **barrier**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.5 cin\_ctl\_pwr\_mon\_t Struct Reference

### Public Attributes

- [cin\\_ctl\\_pwr\\_val\\_t](#) **bus\_12v0**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **mgmt\_3v3**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **mgmt\_2v5**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **mgmt\_1v2**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **enet\_1v0**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **s3e\_3v3**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **gen\_3v3**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **gen\_2v5**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **v6\_0v9**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **v6\_1v0**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **v6\_2v5**
- [cin\\_ctl\\_pwr\\_val\\_t](#) **fp**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.6 cin\_ctl\_pwr\_val Struct Reference

### Public Attributes

- double **i**
- double **v**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.7 cin\_data Struct Reference

### Public Attributes

- [fifo](#) \* **packet\_fifo**
- [fifo](#) \* **frame\_fifo**
- [cin\\_data\\_threads\\_t](#) **listen\_thread**
- [cin\\_data\\_threads\\_t](#) **assembler\_thread**
- [cin\\_data\\_threads\\_t](#) **descramble\_thread**
- [pthread\\_mutex\\_t](#) **descramble\_mutex**
- [pthread\\_mutex\\_t](#) **stats\_mutex**
- [pthread\\_mutex\\_t](#) **framestore\_mutex**
- [cin\\_data\\_callbacks\\_t](#) **callbacks**
- char \* **addr**
- char \* **bind\_addr**
- int **port**



- int **bind\_port**
- int **recv\_buf**
- [cin\\_port\\_t](#) **dp**
- struct timespec **framerate**
- unsigned long int **dropped\_packets**
- unsigned long int **malformed\_packets**
- uint16\_t **last\_frame**
- [cin\\_data\\_descramble\\_map\\_t](#) **map**
- int **framestore\_mode**
- struct timespec **framestore\_trigger**
- int **framestore\_counter**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.8 cin\_data\_callbacks Struct Reference

### Public Attributes

- void **push** ([cin\\_data\\_frame\\_t](#) \*, void \*usr\_ptr)
- void **pop** ([cin\\_data\\_frame\\_t](#) \*, void \*usr\_ptr)
- [cin\\_data\\_frame\\_t](#) \* **frame**
- void \* **usr\_ptr**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.9 cin\_data\_descramble\_map\_t Struct Reference

### Public Attributes

- uint32\_t \* **map**
- int **size\_x**
- int **size\_y**
- int **overscan**
- int **rows**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.10 cin\_data\_frame Struct Reference

### Public Attributes

- uint16\_t \* **data**
- uint16\_t **number**
- struct timespec **timestamp**
- int **size\_x**
- int **size\_y**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.11 cin\_data\_packet Struct Reference

### Public Attributes

- unsigned char \* **data**
- int **size**
- struct timespec **timestamp**

The documentation for this struct was generated from the following file:

- [src/data.h](#)

## 6.12 cin\_data\_proc Struct Reference

### Public Attributes

- void \*(\* **input\_get** )(void \*, int)
- void \*(\* **input\_put** )(void \*, int)
- void \* **input\_args**
- int **reader**
- void \*(\* **output\_put** )(void \*)
- void \*(\* **output\_get** )(void \*)
- void \* **output\_args**
- [cin\\_data\\_t](#) \* **parent**

The documentation for this struct was generated from the following file:

- [src/data.h](#)

## 6.13 cin\_data\_stats Struct Reference

### Public Attributes

- int **last\_frame**
- double **framerate**
- double **packet\_percent\_full**
- double **frame\_percent\_full**
- double **image\_percent\_full**
- long int **packet\_overruns**
- long int **frame\_overruns**
- long int **image\_overruns**
- long int **packet\_used**
- long int **frame\_used**
- long int **image\_used**
- long int **dropped\_packets**
- long int **mallformed\_packets**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.14 cin\_data\_threads Struct Reference

### Public Attributes

- pthread\_t **thread\_id**
- pthread\_barrier\_t **barrier**
- int **started**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.15 cin\_map\_t Struct Reference

### Public Attributes

- char \* **name**
- uint16\_t **reg**

The documentation for this struct was generated from the following file:

- [src/cinregisters.h](#)

## 6.16 cin\_port Struct Reference

### Public Attributes

- int **sockfd**
- struct timeval **tv**
- struct sockaddr\_in **sin\_srv**
- struct sockaddr\_in **sin\_cli**
- socklen\_t **slen**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

## 6.17 fifo Struct Reference

### Public Attributes

- void \* **data**
- void \* **head**
- void \* **tail**
- void \* **end**
- long int **size**
- int **elem\_size**
- int **full**
- long int **overruns**
- pthread\_mutex\_t **mutex**
- pthread\_cond\_t **signal**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

# Chapter 7

## File Documentation

### 7.1 src/cin.h File Reference

```
#include <stdint.h>
#include <stdio.h>
#include <sys/socket.h>
#include <netinet/in.h>
#include <netinet/ip.h>
#include <sys/time.h>
#include <pthread.h>
```

#### Classes

- struct [fifo](#)
- struct [cin\\_ctl\\_listener](#)
- struct [cin\\_port](#)
- struct [cin\\_config\\_timing](#)
- struct [cin\\_ctl](#)
- struct [cin\\_data\\_frame](#)
- struct [cin\\_data\\_stats](#)
- struct [cin\\_data\\_threads](#)
- struct [cin\\_data\\_callbacks](#)
- struct [cin\\_data\\_descramble\\_map\\_t](#)
- struct [cin\\_data](#)
- struct [cin\\_ctl\\_id](#)
- struct [cin\\_ctl\\_pwr\\_val](#)
- struct [cin\\_ctl\\_pwr\\_mon\\_t](#)

#### Macros

- #define **CIN\_OK** 0
- #define **CIN\_ERROR** -1
- #define **CIN\_CTL\_MSG\_OK** 0
- #define **CIN\_CTL\_MSG\_MINOR** 1
- #define **CIN\_CTL\_MSG\_MAJOR** 2

- #define CIN\_CTL\_IP "192.168.1.207"
- #define CIN\_CTL\_CIN\_PORT 49200
- #define CIN\_CTL\_BIND\_PORT 50200
- #define CIN\_CTL\_FRMW\_CIN\_PORT 49202
- #define CIN\_CTL\_FRMW\_BIND\_PORT 50202
- #define CIN\_CTL\_RCVBUF 10
- #define CIN\_CTL\_MAX\_READ\_TRIES 5
- #define CIN\_CTL\_MAX\_WRITE\_TRIES 5
- #define CIN\_CTL\_WRITE\_SLEEP 100
- #define CIN\_CTL\_READ\_SLEEP 100
- #define CIN\_CTL\_BIAS\_SLEEP 100000
- #define CIN\_CTL\_FO\_SLEEP 500000
- #define CIN\_CTL\_CONFIG\_SLEEP 100
- #define CIN\_CTL\_DCO\_SLEEP 1000000
- #define CIN\_CTL\_FCLK\_SLEEP 200000
- #define CIN\_CTL\_STREAM\_CHUNK 512
- #define CIN\_CTL\_STREAM\_SLEEP 5
- #define CIN\_CTL\_POWER\_ENABLE 0x001F
- #define CIN\_CTL\_POWER\_DISABLE 0x0000
- #define CIN\_CTL\_FP\_POWER\_ENABLE 0x0020
- #define CIN\_CTL\_DCM\_LOCKED 0x0001
- #define CIN\_CTL\_DCM\_PSDONE 0x0002
- #define CIN\_CTL\_DCM\_STATUS0 0x0004
- #define CIN\_CTL\_DCM\_STATUS1 0x0008
- #define CIN\_CTL\_DCM\_STATUS2 0x0010
- #define CIN\_CTL\_DCM\_TX1\_READY 0x0020
- #define CIN\_CTL\_DCM\_TX2\_READY 0x0040
- #define CIN\_CTL\_DCM\_ATCA\_ALARM 0x0080
- #define CIN\_CTL\_TRIG\_INTERNAL 0x0000
- #define CIN\_CTL\_TRIG\_EXTERNAL\_1 0x0001
- #define CIN\_CTL\_TRIG\_EXTERNAL\_2 0x0002
- #define CIN\_CTL\_TRIG\_EXTERNAL\_BOTH 0x0003
- #define CIN\_CTL\_FOCUS\_BIT 0x0002
- #define CIN\_CTL\_FCLK\_125 0x0000
- #define CIN\_CTL\_FCLK\_200 0x0001
- #define CIN\_CTL\_FCLK\_250 0x0002
- #define CIN\_CTL\_FCLK\_125\_C 0x0003
- #define CIN\_CTL\_FCLK\_200\_C 0x0004
- #define CIN\_CTL\_FCLK\_250\_C 0x0005
- #define CIN\_CTL\_FCLK\_156\_C 0x0006
- #define CIN\_CTL\_FPGA\_STS\_CFG 0x8000
- #define CIN\_CTL\_FPGA\_STS\_FP\_PWR 0x0008
- #define CIN\_CTL\_DCM\_STS\_ATCA 0x0080
- #define CIN\_CTL\_DCM\_STS\_LOCKED 0x0001
- #define CIN\_CTL\_DCM\_STS\_OVERRIDE 0x0800
- #define CIN\_CTL\_MUX1\_VCLK1 0x0001
- #define CIN\_CTL\_MUX1\_VCLK2 0x0002
- #define CIN\_CTL\_MUX1\_VCLK3 0x0003
- #define CIN\_CTL\_MUX1\_ATG 0x0004
- #define CIN\_CTL\_MUX1\_VFCLK1 0x0005
- #define CIN\_CTL\_MUX1\_VFCLK2 0x0006
- #define CIN\_CTL\_MUX1\_VFCLK3 0x0007
- #define CIN\_CTL\_MUX1\_HCLK1 0x0008
- #define CIN\_CTL\_MUX1\_HCLK2 0x0009
- #define CIN\_CTL\_MUX1\_OSW 0x000A

- #define **CIN\_CTL\_MUX1\_RST** 0x000B
- #define **CIN\_CTL\_MUX1\_CONVERT** 0x000C
- #define **CIN\_CTL\_MUX1\_SHUTTER** 0x000D
- #define **CIN\_CTL\_MUX1\_SWTRIGGER** 0x000E
- #define **CIN\_CTL\_MUX1\_TRIGMON** 0x000F
- #define **CIN\_CTL\_MUX1\_EXPOSE** 0x0000
- #define **CIN\_CTL\_MUX2\_VCLK1** 0x0010
- #define **CIN\_CTL\_MUX2\_VCLK2** 0x0020
- #define **CIN\_CTL\_MUX2\_VCLK3** 0x0030
- #define **CIN\_CTL\_MUX2\_ATG** 0x0040
- #define **CIN\_CTL\_MUX2\_VFCLK1** 0x0050
- #define **CIN\_CTL\_MUX2\_VFCLK2** 0x0060
- #define **CIN\_CTL\_MUX2\_VFCLK3** 0x0070
- #define **CIN\_CTL\_MUX2\_HCLK1** 0x0080
- #define **CIN\_CTL\_MUX2\_HCLK2** 0x0090
- #define **CIN\_CTL\_MUX2\_HCLK3** 0x00A0
- #define **CIN\_CTL\_MUX2\_OSW** 0x00B0
- #define **CIN\_CTL\_MUX2\_RST** 0x00C0
- #define **CIN\_CTL\_MUX2\_CONVERT** 0x00D0
- #define **CIN\_CTL\_MUX2\_SAVE** 0x00E0
- #define **CIN\_CTL\_MUX2\_HWTRIG** 0x00F0
- #define **CIN\_CTL\_MUX2\_EXPOSE** 0x0000
- #define **CIN\_CTL\_FO\_REG1** 0x821D
- #define **CIN\_CTL\_FO\_REG2** 0x821E
- #define **CIN\_CTL\_FO\_REG3** 0x821F
- #define **CIN\_DATA\_IP** "10.0.5.207"
- #define **CIN\_DATA\_BIND\_PORT** 49201
- #define **CIN\_DATA\_CIN\_PORT** 49203
- #define **CIN\_DATA\_FRAME\_BUFFER\_LEN** 1000
- #define **CIN\_DATA\_PACKET\_BUFFER\_LEN** 10000
- #define **CIN\_DATA\_MAX\_MTU** 9000
- #define **CIN\_DATA\_UDP\_HEADER** 8
- #define **CIN\_DATA\_MAGIC\_PACKET** UINT64\_C(0x0000F4F3F2F1F000)
- #define **CIN\_DATA\_MAGIC\_PACKET\_MASK** UINT64\_C(0x0000FFFFFFFFFFFF00)
- #define **CIN\_DATA\_TAIL\_MAGIC\_PACKET** UINT64\_C(0x010DF0ADDEF2F1F0)
- #define **CIN\_DATA\_TAIL\_MAGIC\_PACKET\_MASK** UINT64\_C(0xFFFFFFFFFFFFFFFF)
- #define **CIN\_DATA\_DROPPED\_PACKET\_VAL** 0x2000
- #define **CIN\_DATA\_DATA\_MASK** 0x1FFF
- #define **CIN\_DATA\_CTRL\_MASK** 0xE000
- #define **CIN\_DATA\_SIGN\_MASK** 0x1000
- #define **CIN\_DATA\_GAIN\_8** 0xC000
- #define **CIN\_DATA\_GAIN\_4** 0x4000
- #define **CIN\_DATA\_PACKET\_LEN** 8184
- #define **CIN\_DATA\_MAX\_PACKETS** 542
- #define **CIN\_DATA\_RCVBUF** (100\*1024\*1024)
- #define **CIN\_DATA\_MAX\_FRAME\_X** 1152
- #define **CIN\_DATA\_MAX\_FRAME\_Y** 2050
- #define **CIN\_DATA\_MAX\_STREAM** 2400000
- #define **CIN\_DATA\_CCD\_COLS** 96
- #define **CIN\_DATA\_CCD\_COLS\_PER\_CHAN** 10
- #define **CIN\_DATA\_PIPELINE\_FLUSH** 1344
- #define **CIN\_CTL\_NUM\_BIAS** 20
- #define **CIN\_CTL\_BIAS\_OFFSET** 0x0030
- #define **CIN\_CTL\_BIAS\_POSH** 0
- #define **CIN\_CTL\_BIAS\_NEGH** 1

- #define **CIN\_CTL\_BIAS\_POSRG** 2
- #define **CIN\_CTL\_BIAS\_NEGRG** 3
- #define **CIN\_CTL\_BIAS\_POSSW** 4
- #define **CIN\_CTL\_BIAS\_NEGSW** 5
- #define **CIN\_CTL\_BIAS\_POSV** 6
- #define **CIN\_CTL\_BIAS\_NEGV** 7
- #define **CIN\_CTL\_BIAS\_POSTG** 8
- #define **CIN\_CTL\_BIAS\_NEGTG** 9
- #define **CIN\_CTL\_BIAS\_POSVF** 10
- #define **CIN\_CTL\_BIAS\_NEGVF** 11
- #define **CIN\_CTL\_BIAS\_NEDGE** 12
- #define **CIN\_CTL\_BIAS\_OTG** 13
- #define **CIN\_CTL\_BIAS\_VDDR** 14
- #define **CIN\_CTL\_BIAS\_VDD\_OUT** 15
- #define **CIN\_CTL\_BIAS\_BUF\_BASE** 16
- #define **CIN\_CTL\_BIAS\_BUF\_DELTA** 17
- #define **CIN\_CTL\_BIAS\_SPARE1** 18
- #define **CIN\_CTL\_BIAS\_SPARE2** 19
- #define **DEBUG\_PRINT**(fmt, ...) if(\_debug\_print\_flag) { fprintf(stderr, "%s:%d:%s(): " fmt, \_\_FILE\_\_, \_\_LINE\_\_, \_\_func\_\_, \_\_VA\_ARGS\_\_); }
- #define **DEBUG\_COMMENT**(fmt) if(\_debug\_print\_flag) { fprintf(stderr, "%s:%d:%s(): " fmt, \_\_FILE\_\_, \_\_LINE\_\_, \_\_func\_\_); }
- #define **ERROR\_COMMENT**(fmt) if(\_error\_print\_flag) { fprintf(stderr, "%s:%d:%s(): " fmt, \_\_FILE\_\_, \_\_LINE\_\_, \_\_func\_\_); }
- #define **ERROR\_PRINT**(fmt, ...) if(\_error\_print\_flag) { fprintf(stderr, "%s:%d:%s(): " fmt, \_\_FILE\_\_, \_\_LINE\_\_, \_\_func\_\_, \_\_VA\_ARGS\_\_); }
- #define **CIN\_CONFIG\_MAX\_STRING** 40
- #define **CIN\_CONFIG\_MAX\_TIMING\_DATA** 880
- #define **CIN\_CONFIG\_MAX\_TIMING\_MODES** 20

## Typedefs

- typedef struct **cin\_ctl\_listener** **cin\_ctl\_listener\_t**
- typedef struct **cin\_port** **cin\_port\_t**
- typedef struct **cin\_config\_timing** **cin\_config\_timing\_t**
- typedef struct **cin\_ctl** **cin\_ctl\_t**
- typedef struct **cin\_data\_frame** **cin\_data\_frame\_t**
- typedef struct **cin\_data\_stats** **cin\_data\_stats\_t**
- typedef struct **cin\_data\_threads** **cin\_data\_threads\_t**
- typedef struct **cin\_data\_callbacks** **cin\_data\_callbacks\_t**
- typedef struct **cin\_data** **cin\_data\_t**
- typedef void(\* **cin\_data\_callback**) (**cin\_data\_frame\_t** \*, void \*usr\_ptr)
- typedef void(\* **cin\_ctl\_msg\_callback**) (const char \*, int, void \*)
- typedef struct **cin\_ctl\_id** **cin\_ctl\_id\_t**
- typedef struct **cin\_ctl\_pwr\_val** **cin\_ctl\_pwr\_val\_t**



## Functions

- void **cin\_set\_debug\_print** (int debug)
- void **cin\_set\_error\_print** (int error)
- void **cin\_report** (FILE \*fp, int details)
- int **cin\_ctl\_init** (cin\_ctl\_t \*cin, char \*addr, uint16\_t port, uint16\_t sport, char \*bind\_addr, uint16\_t bind\_port, uint16\_t bind\_sport)
- int **cin\_ctl\_destroy** (cin\_ctl\_t \*cin)
- void **cin\_ctl\_set\_msg\_callback** (cin\_ctl\_t \*cin, cin\_ctl\_msg\_callback callback, void \*ptr)
- int **cin\_data\_send\_magic** (cin\_data\_t \*cin)
- int **cin\_ctl\_read** (cin\_ctl\_t \*cin, uint16\_t reg, uint16\_t \*val, int wait)
- int **cin\_ctl\_write** (cin\_ctl\_t \*cin, uint16\_t reg, uint16\_t val, int wait)
- int **cin\_ctl\_stream\_write** (cin\_ctl\_t \*cin, unsigned char \*val, int size)
- int **cin\_ctl\_write\_with\_readback** (cin\_ctl\_t \*cin, uint16\_t reg, uint16\_t val)
- int **cin\_ctl\_pwr** (cin\_ctl\_t \*cin, int pwr)
- int **cin\_ctl\_fp\_pwr** (cin\_ctl\_t \*cin, int pwr)
- int **cin\_ctl\_fo\_test\_pattern** (cin\_ctl\_t \*cin, int on\_off)
- int **cin\_ctl\_load\_firmware** (cin\_ctl\_t \*cin)
- int **cin\_ctl\_load\_firmware\_file** (cin\_ctl\_t \*cin, char \*filename)
- int **cin\_ctl\_load\_firmware\_data** (cin\_ctl\_t \*cin, unsigned char \*data, int data\_len)
- int **cin\_ctl\_load\_config** (cin\_ctl\_t \*cin, const char \*filename)
- int **cin\_ctl\_get\_folk** (cin\_ctl\_t \*cin, int \*clkfreq)
- int **cin\_ctl\_set\_folk** (cin\_ctl\_t \*cin, int clkfreq)
- int **cin\_ctl\_get\_cfg\_fpga\_status** (cin\_ctl\_t \*cin, uint16\_t \*\_val)
- int **cin\_ctl\_get\_id** (cin\_ctl\_t \*cin, cin\_ctl\_id\_t \*\_val)
- int **cin\_ctl\_get\_dcm\_status** (cin\_ctl\_t \*cin, uint16\_t \*\_val)
- int **cin\_ctl\_get\_power\_status** (cin\_ctl\_t \*cin, int full, int \*pwr, cin\_ctl\_pwr\_mon\_t \*values)
- int **cin\_ctl\_set\_bias** (cin\_ctl\_t \*cin, int val)
- int **cin\_ctl\_get\_bias** (cin\_ctl\_t \*cin, int \*val)
- int **cin\_ctl\_set\_bias\_regs** (cin\_ctl\_t \*cin, uint16\_t \*vals, int verify)
- int **cin\_ctl\_get\_bias\_regs** (cin\_ctl\_t \*cin, uint16\_t \*vals)
- int **cin\_ctl\_set\_bias\_voltages** (cin\_ctl\_t \*cin, float \*voltage, int verify)
- int **cin\_ctl\_get\_bias\_voltages** (cin\_ctl\_t \*cin, float \*voltage, uint16\_t \*regs)
- int **cin\_ctl\_set\_timing\_regs** (cin\_ctl\_t \*cin, uint16\_t \*vals, int vals\_len)
- int **cin\_ctl\_get\_timing\_regs** (cin\_ctl\_t \*cin, uint16\_t \*vals, int vals\_len)
- int **cin\_ctl\_get\_camera\_pwr** (cin\_ctl\_t \*cin, int \*val)
- int **cin\_ctl\_set\_camera\_pwr** (cin\_ctl\_t \*cin, int val)
- int **cin\_ctl\_set\_clocks** (cin\_ctl\_t \*cin, int val)
- int **cin\_ctl\_get\_clocks** (cin\_ctl\_t \*cin, int \*val)
- int **cin\_ctl\_set\_trigger** (cin\_ctl\_t \*cin, int val)
- int **cin\_ctl\_get\_trigger** (cin\_ctl\_t \*cin, int \*val)
- int **cin\_ctl\_set\_focus** (cin\_ctl\_t \*cin, int val)
- int **cin\_ctl\_get\_focus** (cin\_ctl\_t \*cin, int \*val)
- int **cin\_ctl\_get\_triggering** (cin\_ctl\_t \*cin, int \*trigger)
- int **cin\_ctl\_int\_trigger\_start** (cin\_ctl\_t \*cin, int nimages)
- int **cin\_ctl\_int\_trigger\_stop** (cin\_ctl\_t \*cin)
- int **cin\_ctl\_ext\_trigger\_start** (cin\_ctl\_t \*cin, int trigger\_mode)
- int **cin\_ctl\_ext\_trigger\_stop** (cin\_ctl\_t \*cin)
- int **cin\_ctl\_set\_exposure\_time** (cin\_ctl\_t \*cin, float e\_time)
- int **cin\_ctl\_set\_trigger\_delay** (cin\_ctl\_t \*cin, float t\_time)
- int **cin\_ctl\_set\_cycle\_time** (cin\_ctl\_t \*cin, float ftime)
- int **cin\_ctl\_frame\_count\_reset** (cin\_ctl\_t \*cin)
- int **cin\_ctl\_set\_mux** (cin\_ctl\_t \*cin, int setting)
- int **cin\_ctl\_get\_mux** (cin\_ctl\_t \*cin, int \*setting)
- int **cin\_ctl\_set\_fcric\_clamp** (cin\_ctl\_t \*cin, int clamp)

- int **cin\_ctl\_set\_fcric\_gain** (cin\_ctl\_t \*cin, int gain)
- int **cin\_ctl\_set\_fcric\_regs** (cin\_ctl\_t \*cin, uint16\_t \*reg, int num\_reg)
- int **cin\_ctl\_set\_fcric** (cin\_ctl\_t \*cin)
- int **cin\_ctl\_set\_fabric\_address** (cin\_ctl\_t \*cin, char \*ip)
- int **cin\_ctl\_bias\_dump** (cin\_ctl\_t \*cin, FILE \*fp)
- int **cin\_ctl\_reg\_dump** (cin\_ctl\_t \*cin, FILE \*fp)
- int **cin\_config\_read\_file** (cin\_ctl\_t \*cin, const char \*file)
- int **cin\_config\_get\_timing\_name** (cin\_ctl\_t \*cin, int num, char \*\*name)
- int **cin\_data\_init** (cin\_data\_t \*cin, char \*addr, uint16\_t port, char \*bind\_addr, uint16\_t bind\_port, int rcvbuf, int packet\_buffer\_len, int frame\_buffer\_len, cin\_data\_callback push\_callback, cin\_data\_callback pop\_callback, void \*usr\_ptr)
- void **cin\_data\_destroy** (cin\_data\_t \*cin)
- void **cin\_data\_framestore\_trigger** (cin\_data\_t \*cin, int count)
- void **cin\_data\_framestore\_skip** (cin\_data\_t \*cin, int count)
- int **cin\_data\_get\_framestore\_counter** (cin\_data\_t \*cin)
- void **cin\_data\_framestore\_disable** (cin\_data\_t \*cin)
- void **cin\_data\_framestore\_trigger\_enable** (cin\_data\_t \*cin)
- struct cin\_data\_frame \* **cin\_data\_get\_next\_frame** (cin\_data\_t \*cin)
- void **cin\_data\_release\_frame** (cin\_data\_t \*cin, int free\_mem)
- struct cin\_data\_frame \* **cin\_data\_get\_buffered\_frame** (void)
- void **cin\_data\_release\_buffered\_frame** (void)
- void **cin\_data\_compute\_stats** (cin\_data\_t \*cin, cin\_data\_stats\_t \*stats)
- void **cin\_data\_show\_stats** (FILE \*fp, cin\_data\_stats\_t stats)
- void **cin\_data\_reset\_stats** (cin\_data\_t \*cin)
- int **cin\_data\_set\_descramble\_params** (cin\_data\_t \*cin, int rows, int overscan)
- void **cin\_data\_get\_descramble\_params** (cin\_data\_t \*cin, int \*rows, int \*overscan, int \*xsize, int \*ysize)
- int **cin\_com\_boot** (cin\_ctl\_t \*cin\_ctl, cin\_data\_t \*cin\_data, const char \*mode)
- int **cin\_ctl\_upload\_bias** (cin\_ctl\_t \*cin)

## Variables

- const char \* **cin\_build\_git\_time**
- const char \* **cin\_build\_git\_sha**
- const char \* **cin\_build\_version**
- int **\_debug\_print\_flag**
- int **\_error\_print\_flag**

### 7.1.1 Detailed Description

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## 7.1.2 LICENSE

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## 7.1.3 DESCRIPTION

Header file for CIN communications

## 7.1.4 Macro Definition Documentation

### 7.1.4.1 CIN\_CONFIG\_MAX\_TIMING\_DATA

```
#define CIN_CONFIG_MAX_TIMING_DATA 880
```

Max = 55 per state, 16 states

### 7.1.4.2 CIN\_CONFIG\_MAX\_TIMING\_MODES

```
#define CIN_CONFIG_MAX_TIMING_MODES 20
```

20 states max

### 7.1.4.3 CIN\_CTL\_BIAS\_OFFSET

```
#define CIN_CTL_BIAS_OFFSET 0x0030
```

Offset in address to read bias

## 7.2 src/cin\_register\_map.h File Reference

### Macros

- #define [REG\\_COMMAND](#) 0x0001
- #define [REG\\_READ\\_ADDRESS](#) 0x0002
- #define [REG\\_STREAM\\_TYPE](#) 0x0003
- #define [CMD\\_FCLK\\_125](#) 0xB000
- #define [CMD\\_FCLK\\_200](#) 0x7000
- #define [CMD\\_FCLK\\_250](#) 0x3000
- #define [REG\\_IF\\_MAC0](#) 0x0010
- #define [REG\\_IF\\_MAC1](#) 0x0011
- #define [REG\\_IF\\_MAC2](#) 0x0012
- #define [REG\\_IF\\_IP0](#) 0x0013
- #define [REG\\_IF\\_IP1](#) 0x0014
- #define [REG\\_IF\\_CMD\\_PORT\\_NUM](#) 0x001A
- #define [REG\\_IF\\_STREAM\\_IN\\_PORT\\_NUM](#) 0x001C
- #define [REG\\_IF\\_STREAM\\_OUT\\_PORT\\_NUM](#) 0x001D
- #define [REG\\_ETH\\_RESET](#) 0x0020
- #define [REG\\_ETH\\_ENABLE](#) 0x0021
- #define [REG\\_PHY1\\_MDIO\\_CMD](#) 0x0022
- #define [REG\\_PHY1\\_MDIO\\_CMD\\_DATA](#) 0x0023
- #define [REG\\_PHY1\\_MDIO\\_STATUS](#) 0x0024
- #define [REG\\_PHY1\\_MDIO\\_RD\\_ADDR](#) 0x0025
- #define [REG\\_PHY1\\_MDIO\\_RD\\_DATA](#) 0x0026
- #define [REG\\_MAC\\_CFG\\_VECTOR1](#) 0x0027
- #define [REG\\_PHY2\\_MDIO\\_CMD](#) 0x0028
- #define [REG\\_PHY2\\_MDIO\\_CMD\\_DATA](#) 0x0029
- #define [REG\\_PHY2\\_MDIO\\_STATUS](#) 0x002A
- #define [REG\\_PHY2\\_MDIO\\_RD\\_ADDR](#) 0x002B
- #define [REG\\_PHY2\\_MDIO\\_RD\\_DATA](#) 0x002C
- #define [REG\\_MAC\\_CFG\\_VECTOR2](#) 0x002D
- #define [CMD\\_PS\\_ENABLE](#) 0x0021
- #define [CMD\\_PS\\_POWERDOWN](#) 0x0022
- #define [REG\\_PS\\_ENABLE](#) 0x0030
- #define [REG\\_PS\\_SYNC\\_DIV0](#) 0x0031
- #define [REG\\_PS\\_SYNC\\_DIV1](#) 0x0032
- #define [REG\\_PS\\_SYNC\\_DIV2](#) 0x0033
- #define [REG\\_PS\\_SYNC\\_DIV3](#) 0x0034
- #define [REG\\_PS\\_SYNC\\_DIV4](#) 0x0035
- #define [CMD\\_PROGRAM\\_FRAME](#) 0x0041
- #define [REG\\_FRM\\_RESET](#) 0x0036
- #define [REG\\_FRM\\_10GbE\\_SEL](#) 0x0037;
- #define [CMD\\_ENABLE\\_CLKS](#) 0x0031
- #define [CMD\\_DISABLE\\_CLKS](#) 0x0032
- #define [REG\\_CLOCK\\_EN\\_REG](#) 0x0038

- #define **REG\_SI570\_REG0** 0x0039
- #define **REG\_SI570\_REG1** 0x003A
- #define **REG\_SI570\_REG2** 0x003B
- #define **REG\_SI570\_REG3** 0x003C
- #define **CMD\_MON\_STOP** 0x0011
- #define **CMD\_MON\_START** 0x0012
- #define **REG\_VMON\_ADC1\_CH1** 0x0040 /\* V12P\_BUS Voltage Monitor \*/
- #define **REG\_IMON\_ADC1\_CH0** 0x0041 /\* V12P\_BUS Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CH5** 0x0042 /\* V3P3\_MGMT Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CH5** 0x0043 /\* V3P3\_MGMT Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CH4** 0x0044 /\* V3P3\_S3E Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CH4** 0x0045 /\* V3P3\_S3E Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CH7** 0x0046 /\* V2P5\_MGMT Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CH7** 0x0047 /\* V2P5\_MGMT Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CH6** 0x0048 /\* V1P8\_MGMT Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CH6** 0x0049 /\* V1P8\_MGMT Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CH2** 0x004A /\* V1P2\_MGMT Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CH2** 0x004B /\* V1P2\_MGMT Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CH3** 0x004C /\* V1P0\_ENET Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CH3** 0x004D /\* V1P0\_ENET Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CH8** 0x004E /\* V3P3\_GEN Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CH8** 0x004F /\* V3P3\_GEN Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CH9** 0x0050 /\* V2P5\_GEN Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CH9** 0x0051 /\* V2P5\_GEN Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CHE** 0x0052 /\* V0P9\_V6 Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CHE** 0x0053 /\* V0P9\_V6 Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CHD** 0x0054 /\* V2P5\_V6 Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CHD** 0x0055 /\* V2P5\_V6 Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CHB** 0x0056 /\* V1P0\_V6 Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CHB** 0x0057 /\* V1P0\_V6 Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CHC** 0x0058 /\* V1P2\_V6 Voltage Monitor \*/
- #define **REG\_IMON\_ADC0\_CHC** 0x0059 /\* V1P2\_V6 Current Monitor \*/
- #define **REG\_VMON\_ADC0\_CHF** 0x005A /\* V5P0\_FP Voltage Monitor (1/2) \*/
- #define **REG\_IMON\_ADC0\_CHF** 0x005B /\* V5P0\_FP Current Monitor (1/2) \*/
- #define **REG\_DCM\_STATUS** 0x0080
- #define **REG\_FPGA\_STATUS** 0x0081
- #define **REG\_BOARD\_ID** 0x008D
- #define **REG\_HW\_SERIAL\_NUM** 0x008E
- #define **REG\_FPGA\_VERSION** 0x008F
- #define **REG\_SANDBOX\_REG00** 0x00F0
- #define **REG\_SANDBOX\_REG01** 0x00F1
- #define **REG\_SANDBOX\_REG02** 0x00F2
- #define **REG\_SANDBOX\_REG03** 0x00F3
- #define **REG\_SANDBOX\_REG04** 0x00F4
- #define **REG\_SANDBOX\_REG05** 0x00F5
- #define **REG\_SANDBOX\_REG06** 0x00F6
- #define **REG\_SANDBOX\_REG07** 0x00F7
- #define **REG\_SANDBOX\_REG08** 0x00F8
- #define **REG\_SANDBOX\_REG09** 0x00F9
- #define **REG\_SANDBOX\_REG0A** 0x00FA
- #define **REG\_SANDBOX\_REG0B** 0x00FB
- #define **REG\_SANDBOX\_REG0C** 0x00FC
- #define **REG\_SANDBOX\_REG0D** 0x00FD
- #define **REG\_SANDBOX\_REG0E** 0x00FE
- #define **REG\_SANDBOX\_REG0F** 0x00FF

- #define **REG\_FRM\_COMMAND** 0x8001
- #define **REG\_FRM\_READ\_ADDRESS** 0x8002
- #define **REG\_FRM\_STREAM\_TYPE** 0x8003
- #define **CMD\_SEND\_SYNC\_PULSE** 0x0100
- #define **CMD\_SYNC\_DETECTOR2READOUT** 0x0101
- #define **CMD\_WR\_CCD\_BIAS\_REG** 0x0102
- #define **CMD\_WR\_CCD\_CLOCK\_REG** 0x0103
- #define **CMD\_SEND\_FCRIC\_CONFIG** 0x0105
- #define **CMD\_RESET\_FRAME\_COUNT** 0x0106
- #define **REG\_IF\_MAC\_FAB1B0** 0x8010
- #define **REG\_IF\_MAC\_FAB1B1** 0x8011
- #define **REG\_IF\_MAC\_FAB1B2** 0x8012
- #define **REG\_IF\_IP\_FAB1B0** 0x8013
- #define **REG\_IF\_IP\_FAB1B1** 0x8014
- #define **REG\_IF\_CMD\_PORT\_NUM\_FAB1B** 0x8015
- #define **REG\_IF\_STREAM\_IN\_PORT\_NUM\_FAB1B** 0x8016
- #define **REG\_IF\_STREAM\_OUT\_PORT\_NUM\_FAB1B** 0x8017
- #define **REG\_XAUI\_FAB1B** 0x8018
- #define **REG\_MAC\_CONFIG\_VEC\_FAB1B0** 0x8019
- #define **REG\_MAC\_CONFIG\_VEC\_FAB1B1** 0x801A
- #define **REG\_MAC\_STATS1\_FAB1B0** 0x801B
- #define **REG\_MAC\_STATS1\_FAB1B1** 0x801C
- #define **REG\_MAC\_STATS2\_FAB1B0** 0x801D
- #define **REG\_MAC\_STATS2\_FAB1B1** 0x801E
- #define **REG\_IF\_MAC\_FAB2B0** 0x8020
- #define **REG\_IF\_MAC\_FAB2B1** 0x8021
- #define **REG\_IF\_MAC\_FAB2B2** 0x8022
- #define **REG\_IF\_IP\_FAB2B0** 0x8023
- #define **REG\_IF\_IP\_FAB2B1** 0x8024
- #define **REG\_IF\_CMD\_PORT\_NUM\_FAB2B** 0x8025
- #define **REG\_IF\_STREAM\_IN\_PORT\_NUM\_FAB2B** 0x8026
- #define **REG\_IF\_STREAM\_OUT\_PORT\_NUM\_FAB2B** 0x8027
- #define **REG\_XAUI\_FAB2B** 0x8028
- #define **REG\_MAC\_CONFIG\_VEC\_FAB2B0** 0x8029
- #define **REG\_MAC\_CONFIG\_VEC\_FAB2B1** 0x802A
- #define **REG\_MAC\_STATS1\_FAB2B0** 0x802B
- #define **REG\_MAC\_STATS1\_FAB2B1** 0x802C
- #define **REG\_MAC\_STATS2\_FAB2B0** 0x802D
- #define **REG\_MAC\_STATS2\_FAB2B1** 0x802E
- #define **REG\_SRAM\_COMMAND** 0x8030
- #define **REG\_SRAM\_START\_ADDR1** 0x8031
- #define **REG\_SRAM\_START\_ADDR0** 0x8032
- #define **REG\_SRAM\_STOP\_ADDR1** 0x8033
- #define **REG\_SRAM\_STOP\_ADDR0** 0x8034
- #define **REG\_SRAM\_FRAME\_DATA\_OUT1** 0x8035
- #define **REG\_SRAM\_FRAME\_DATA\_OUT0** 0x8036
- #define **REG\_SRAM\_FRAME\_DATA\_IN1** 0x8037
- #define **REG\_SRAM\_FRAME\_DATA\_IN0** 0x8038
- #define **REG\_SRAM\_FRAME\_DV** 0x8039
- #define **REG\_SRAM\_STATUS1** 0x803A
- #define **REG\_SRAM\_STATUS0** 0x803B
- #define **CMD\_FCLK\_COMMIT** 0x0012
- #define **REG\_FCLK\_I2C\_ADDRESS** 0x8040
- #define **REG\_FCLK\_I2C\_DATA\_WR** 0x8041
- #define **REG\_FCLK\_I2C\_DATA\_RD** 0x8042

- `#define REG_TRIGGERSELECT_REG 0x8050`
- `#define REG_TRIGGERMASK_REG 0x8051`
- `#define REG_CCDCLKSELECT_REG 0x8052`
- `#define REG_CDCLKDISABLE_REG 0x8053`
- `#define REG_FCLK_SET0 0xB007`
- `#define REG_FCLK_SET1 0xB008`
- `#define REG_FCLK_SET2 0xB009`
- `#define REG_FCLK_SET3 0xB00A`
- `#define REG_FCLK_SET4 0xB00B`
- `#define REG_FCLK_SET5 0xB00C`
- `#define REG_FRM_DCM_STATUS 0x8080`
- `#define REG_FRM_FPGA_STATUS 0x8081`
- `#define REG_FRM_BOARD_ID 0x808D`
- `#define REG_FRM_HW_SERIAL_NUM 0x808E`
- `#define REG_FRM_FPGA_VERSION 0x808F`
- `#define REG_FRM_SANDBOX_REG00 0x80F0`
- `#define REG_FRM_SANDBOX_REG01 0x80F1`
- `#define REG_FRM_SANDBOX_REG02 0x80F2`
- `#define REG_FRM_SANDBOX_REG03 0x80F3`
- `#define REG_FRM_SANDBOX_REG04 0x80F4`
- `#define REG_FRM_SANDBOX_REG05 0x80F5`
- `#define REG_FRM_SANDBOX_REG06 0x80F6`
- `#define REG_FRM_SANDBOX_REG07 0x80F7`
- `#define REG_FRM_SANDBOX_REG08 0x80F8`
- `#define REG_FRM_SANDBOX_REG09 0x80F9`
- `#define REG_FRM_SANDBOX_REG0A 0x80FA`
- `#define REG_FRM_SANDBOX_REG0B 0x80FB`
- `#define REG_FRM_SANDBOX_REG0C 0x80FC`
- `#define REG_FRM_SANDBOX_REG0D 0x80FD`
- `#define REG_FRM_SANDBOX_REG0E 0x80FE`
- `#define REG_FRM_SANDBOX_REG0F 0x80FF`
- `#define REG_DETECTOR_REVISION_REG 0x8100`
- `#define REG_DETECTOR_CONFIG_REG1 0x8101`
- `#define REG_DETECTOR_CONFIG_REG2 0x8102`
- `#define REG_DETECTOR_CONFIG_REG3 0x8103`
- `#define REG_DETECTOR_CONFIG_REG4 0x8104`
- `#define REG_DETECTOR_CONFIG_REG5 0x8105`
- `#define REG_DETECTOR_CONFIG_REG6 0x8106`
- `#define REG_DETECTOR_CONFIG_REG7 0x8107`
- `#define REG_DETECTOR_CONFIG_REG8 0x8108`
- `#define REG_IMG_PROC_REVISION_REG 0x8120`
- `#define REG_IMG_PROC_CONFIG_REG1 0x8121`
- `#define REG_IMG_PROC_CONFIG_REG2 0x8122`
- `#define REG_IMG_PROC_CONFIG_REG3 0x8123`
- `#define REG_IMG_PROC_CONFIG_REG4 0x8124`
- `#define REG_IMG_PROC_CONFIG_REG5 0x8125`
- `#define REG_IMG_PROC_CONFIG_REG6 0x8126`
- `#define REG_IMG_PROC_CONFIG_REG7 0x8127`
- `#define REG_IMG_PROC_CONFIG_REG8 0x8128`
- `#define REG_BIASANDCLOCKREGISTERADDRESS 0x8200`
- `#define REG_BIASANDCLOCKREGISTERDATA 0x8201`
- `#define REG_CLOCKREGISTERDATAOUT 0x8202`
- `#define REG_BIASREGISTERDATAOUT 0x8203`
- `#define REG_BIASCONFIGREGISTER0_REG 0x8204`
- `#define REG_CLOCKCONFIGREGISTER0_REG 0x8205`

- #define **REG\_BIASPARAM\_READ\_START** 0x3000
- #define **REG\_EXPOSURETIMEMSB\_REG** 0x8206
- #define **REG\_EXPOSURETIMELSB\_REG** 0x8207
- #define **REG\_ALTEXPOSURETIMEMSB\_REG** 0x8306
- #define **REG\_ALTEXPOSURETIMELSB\_REG** 0x8307
- #define **REG\_TRIGGERREPETITIONTIMEMSB\_REG** 0x8208
- #define **REG\_TRIGGERREPETITIONTIMELSB\_REG** 0x8209
- #define **REG\_DELAYTOEXPOSUREMSB\_REG** 0x820A
- #define **REG\_DELAYTOEXPOSURELSB\_REG** 0x820B
- #define **REG\_NUMBEROFEXPOSURE\_REG** 0x820C
- #define **REG\_SHUTTERTIMEMSB\_REG** 0x820D
- #define **REG\_SHUTTERTIMELSB\_REG** 0x820E
- #define **REG\_DELAYTOSHUTTERMSB\_REG** 0x820F
- #define **REG\_DELAYTOSHUTTERLSB\_REG** 0x8210
- #define **REG\_FCRIC\_MASK\_REG1** 0x8211
- #define **REG\_FCRIC\_MASK\_REG2** 0x8212
- #define **REG\_FCRIC\_MASK\_REG3** 0x8213
- #define **REG\_LVDS\_OVERFLOW\_ERROR\_REG1** 0x8214
- #define **REG\_LVDS\_OVERFLOW\_ERROR\_REG2** 0x8215
- #define **REG\_LVDS\_OVERFLOW\_ERROR\_REG3** 0x8216
- #define **REG\_LVDS\_PARITY\_ERROR\_REG1** 0x8217
- #define **REG\_LVDS\_PARITY\_ERROR\_REG2** 0x8218
- #define **REG\_LVDS\_PARITY\_ERROR\_REG3** 0x8219
- #define **REG\_LVDS\_STOP\_BIT\_ERROR\_REG1** 0x821A
- #define **REG\_LVDS\_STOP\_BIT\_ERROR\_REG2** 0x821B
- #define **REG\_LVDS\_STOP\_BIT\_ERROR\_REG3** 0x821C
- #define **REG\_FCRIC\_WRITE0\_REG** 0x821D
- #define **REG\_FCRIC\_WRITE1\_REG** 0x821E
- #define **REG\_FCRIC\_WRITE2\_REG** 0x821F
- #define **REG\_FCRIC\_READ0\_REG** 0x8220
- #define **REG\_FCRIC\_READ1\_REG** 0x8221
- #define **REG\_FCRIC\_READ2\_REG** 0x8222
- #define **REG\_DEBUGVIDEO0\_REG** 0x8223
- #define **REG\_DEBUGVIDEO1\_REG** 0x8224
- #define **REG\_DEBUGVIDEO2\_REG** 0x8225
- #define **REG\_DEBUGVIDEO3\_REG** 0x8226
- #define **REG\_DEBUGVIDEO4\_REG** 0x8227
- #define **REG\_DEBUGVIDEO5\_REG** 0x8228
- #define **REG\_DEBUGVIDEO6\_REG** 0x8229
- #define **REG\_DEBUGVIDEO7\_REG** 0x822A
- #define **REG\_DEBUGVIDEO8\_REG** 0x822B
- #define **REG\_DEBUGVIDEO9\_REG** 0x822C
- #define **REG\_DEBUGVIDEO10\_REG** 0x822D
- #define **REG\_DEBUGVIDEO11\_REG** 0x822E
- #define **REG\_DEBUGCOUNTER00\_REG** 0x822F
- #define **REG\_DEBUGCOUNTER01\_REG** 0x8230
- #define **REG\_DEBUGCOUNTER02\_REG** 0x8231
- #define **REG\_DEBUGCOUNTER03\_REG** 0x8232
- #define **REG\_DEBUGCOUNTER04\_REG** 0x8233
- #define **CMD\_READ\_REG** 0x0001



### 7.2.1 Detailed Description

&lt;

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### 7.2.3 DESCRIPTION

Control and Frame FPGA Register Map

### 7.2.4 TIMING

The exposure time is set through the REG\_EXPOSURETIMEMSB\_REG and REG\_EXPOSURETIMELSB\_REG registers. Their value in wall time depends on the fclk frequency. At 200 MHz fclk a register value of 0x00000001 corresponds to 20 us. At 125 MHz, a value of 0x00000001 corresponds to 32 us.

### 7.2.5 Macro Definition Documentation

#### 7.2.5.1 CMD\_DISABLE\_CLKS

```
#define CMD_DISABLE_CLKS 0x0032
```

Disable Frame FPGA clock crystals

#### 7.2.5.2 CMD\_ENABLE\_CLKS

```
#define CMD_ENABLE_CLKS 0x0031
```

Enable selected Frame FPGA clock crystals

#### 7.2.5.3 CMD\_FCLK\_250

```
#define CMD_FCLK_250 0x3000
```

Ethernet Interface

#### 7.2.5.4 CMD\_FCLK\_COMMIT

```
#define CMD_FCLK_COMMIT 0x0012
```

Start I2C Write/Read

#### 7.2.5.5 CMD\_MON\_START

```
#define CMD_MON_START 0x0012
```

Start voltage and current monitor

#### 7.2.5.6 CMD\_MON\_STOP

```
#define CMD_MON_STOP 0x0011
```

Stop voltage and current monitor

#### 7.2.5.7 CMD\_PS\_ENABLE

```
#define CMD_PS_ENABLE 0x0021
```

Enable Selected Power Modules

#### 7.2.5.8 CMD\_PS\_POWERDOWN

```
#define CMD_PS_POWERDOWN 0x0022
```

Start power down sequence

#### 7.2.5.9 CMD\_READ\_REG

```
#define CMD_READ_REG 0x0001
```

Read Register CIN\_REGISTER\_MAP\_H

#### 7.2.5.10 CMD\_RESET\_FRAME\_COUNT

```
#define CMD_RESET_FRAME_COUNT 0x0106
```

RESET STATISTICS/DEBUG COUNTERS Ethernet Interface

#### 7.2.5.11 CMD\_SEND\_FCRIC\_CONFIG

```
#define CMD_SEND_FCRIC_CONFIG 0x0105
```

SEND CONFIG DATA TO FRIC

#### 7.2.5.12 CMD\_SEND\_SYNC\_PULSE

```
#define CMD_SEND_SYNC_PULSE 0x0100
```

ISSUES A SYNC PULSE

#### 7.2.5.13 CMD\_SYNC\_DETECTOR2READOUT

```
#define CMD_SYNC_DETECTOR2READOUT 0x0101
```

COMMAND TO SYNC DETECTOR AND READOUT (SEE IMAGE PROCESSING)

#### 7.2.5.14 CMD\_WR\_CCD\_BIAS\_REG

```
#define CMD_WR_CCD_BIAS_REG 0x0102
```

WRITE CCD BIAS REGISTERS

#### 7.2.5.15 CMD\_WR\_CCD\_CLOCK\_REG

```
#define CMD_WR_CCD_CLOCK_REG 0x0103
```

WRITE CCD CLOCK REGISTER

#### 7.2.5.16 REG\_BIASCONFIGREGISTER0\_REG

```
#define REG_BIASCONFIGREGISTER0_REG 0x8204
```

Clock Static Registers

**7.2.5.17 REG\_BIASREGISTERDATAOUT**

```
#define REG_BIASREGISTERDATAOUT 0x8203
```

Bias Static Registers

**7.2.5.18 REG\_CLOCK\_EN\_REG**

```
#define REG_CLOCK_EN_REG 0x0038
```

Clock Enable Register Programmable Si570 Clock Registers

**7.2.5.19 REG\_CLOCKCONFIGREGISTER0\_REG**

```
#define REG_CLOCKCONFIGREGISTER0_REG 0x8205
```

Bias Voltage

**7.2.5.20 REG\_COMMAND**

```
#define REG_COMMAND 0x0001
```

<Command Registers

**7.2.5.21 REG\_DEBUGCOUNTER04\_REG**

```
#define REG_DEBUGCOUNTER04_REG 0x8233
```

```
=====
```

**CIN Commands**

Common Commands

**7.2.5.22 REG\_DELAYTOSHUTTERLSB\_REG**

```
#define REG_DELAYTOSHUTTERLSB_REG 0x8210
```

Digitizer Registers

**7.2.5.23 REG\_ETH\_ENABLE**

```
#define REG_ETH_ENABLE 0x0021
```

Enable Eth Hardware 1=Rx, 2=Tx, 3=Both

#### 7.2.5.24 REG\_ETH\_RESET

```
#define REG_ETH_RESET 0x0020
```

Reset Eth Hardware 1=Rx, 2=Tx, 3=Both

#### 7.2.5.25 REG\_EXPOSURETIMELSB\_REG

```
#define REG_EXPOSURETIMELSB_REG 0x8207
```

Exposure time LSB

#### 7.2.5.26 REG\_EXPOSURETIMESB\_REG

```
#define REG_EXPOSURETIMESB_REG 0x8206
```

Exposure time MSB

#### 7.2.5.27 REG\_FCLK\_I2C\_ADDRESS

```
#define REG_FCLK_I2C_ADDRESS 0x8040
```

[ Slave Address(7), RD/WRn(1), Reg Address(8) ] Slave address Hx58 -> HxB when shifted up by 1

#### 7.2.5.28 REG\_FCLK\_I2C\_DATA\_RD

```
#define REG_FCLK_I2C_DATA_RD 0x8042
```

[ Read Failed (1), Write Failed(1), Toggle bit(1), 0(5), Read Data (8) ]

#### 7.2.5.29 REG\_FCLK\_I2C\_DATA\_WR

```
#define REG_FCLK_I2C_DATA_WR 0x8041
```

[ Clock Select(2), Clock Enable (1), 0(5), Write Data (8) ] Clock Select: (00): 250 MHz (01): 200 MHz (10): FPGA FCRIC Clk (11): Si570 Programmable

#### 7.2.5.30 REG\_FCLK\_SET5

```
#define REG_FCLK_SET5 0xB00C
```

FRM Status

#### 7.2.5.31 REG\_FPGA\_VERSION

```
#define REG_FPGA_VERSION 0x008F
```

Sandbox Registers

#### 7.2.5.32 REG\_FRM\_10GbE\_SEL

```
#define REG_FRM_10GbE_SEL 0x0037;
```

10GbE Link Select Clock Enables

#### 7.2.5.33 REG\_FRM\_FPGA\_VERSION

```
#define REG_FRM_FPGA_VERSION 0x808F
```

Sandbox Registers

#### 7.2.5.34 REG\_FRM\_RESET

```
#define REG_FRM_RESET 0x0036
```

Frame Reset

#### 7.2.5.35 REG\_FRM\_SANDBOX\_REG0F

```
#define REG_FRM_SANDBOX_REG0F 0x80FF
```

Image Processing Registers

#### 7.2.5.36 REG\_FRM\_STREAM\_TYPE

```
#define REG_FRM_STREAM_TYPE 0x8003
```

List of Commands

#### 7.2.5.37 REG\_IMON\_ADC0\_CHF

```
#define REG_IMON_ADC0_CHF 0x005B /* V5P0_FP Current Monitor (1/2) */
```

Status Registers

#### 7.2.5.38 REG\_MAC\_CFG\_VECTOR1

```
#define REG_MAC_CFG_VECTOR1 0x0027
```

Ethernet Hardware Conf

#### 7.2.5.39 REG\_MAC\_CFG\_VECTOR2

```
#define REG_MAC_CFG_VECTOR2 0x002D
```

Ethernet Hardware Conf Power Supply Control

#### 7.2.5.40 REG\_MAC\_STATS2\_FAB2B1

```
#define REG_MAC_STATS2_FAB2B1 0x802E
```

SRAM Test Interface

#### 7.2.5.41 REG\_PHY1\_MDIO\_CMD

```
#define REG_PHY1_MDIO_CMD 0x0022
```

Start(1), RnW(1), WDRd(1), PHY Addr(5), REG Addr(5)

#### 7.2.5.42 REG\_PS\_ENABLE

```
#define REG_PS_ENABLE 0x0030
```

Power Supply Enable:

#### 7.2.5.43 REG\_PS\_SYNC\_DIV0

```
#define REG_PS_SYNC_DIV0 0x0031
```

2.5V Gen

#### 7.2.5.44 REG\_PS\_SYNC\_DIV1

```
#define REG_PS_SYNC_DIV1 0x0032
```

3.3V Gen

#### 7.2.5.45 REG\_PS\_SYNC\_DIV2

```
#define REG_PS_SYNC_DIV2 0x0033
```

2.5V Frame

#### 7.2.5.46 REG\_PS\_SYNC\_DIV3

```
#define REG_PS_SYNC_DIV3 0x0034
```

0.9V Frame

**7.2.5.47 REG\_PS\_SYNC\_DIV4**

```
#define REG_PS_SYNC_DIV4 0x0035
```

5.0V FP Frame FPGA Control

**7.2.5.48 REG\_SANDBOX\_REG0F**

```
#define REG_SANDBOX_REG0F 0x00FF
```

-----< Frame FPGA Registers > Command Registers

**7.2.5.49 REG\_SI570\_REG3**

```
#define REG_SI570_REG3 0x003C
```

Power Monitor Registers

**7.2.5.50 REG\_SRAM\_COMMAND**

```
#define REG_SRAM_COMMAND 0x8030
```

1 bit [0] >> Read NOT Write 2 bits [3:2] >> Modes: – Single RW 0x00 – Burst RW 0x01 – Test/Diagnostic 10 – Sleep 11 1 bit [4] >> start/stop

**7.2.5.51 REG\_SRAM\_STATUS0**

```
#define REG_SRAM_STATUS0 0x803B
```

Programmable Clock

**7.2.5.52 REG\_STREAM\_TYPE**

```
#define REG_STREAM_TYPE 0x0003
```

FCLK Values

**7.2.5.53 REG\_TRIGGERMASK\_REG**

```
#define REG_TRIGGERMASK_REG 0x8051
```

[00]==SW Trigger, [01]==FP TrigIn2, [10]==FP TrigIn1, [11]==FP TrigIn1OR2

**7.2.5.54 REG\_TRIGGERREPETITIONTIMELSB\_REG**

```
#define REG_TRIGGERREPETITIONTIMELSB_REG 0x8209
```

Trigger Cycle Time LSB

**7.2.5.55 REG\_TRIGGERREPETITIONTIMESB\_REG**

```
#define REG_TRIGGERREPETITIONTIMESB_REG 0x8208
```

Trigger Cycle Time MSB



# Index

- CIN Control Bias Routines, [20](#)
- CIN Control Timing Routines, [21](#)
  - [cin\\_config\\_get\\_timing\\_name](#), [21](#)
- CIN Data Framestore Functions, [25](#)
  - [cin\\_data\\_framestore\\_disable](#), [25](#)
  - [cin\\_data\\_framestore\\_skip](#), [25](#)
  - [cin\\_data\\_framestore\\_trigger](#), [26](#)
  - [cin\\_data\\_framestore\\_trigger\\_enable](#), [26](#)
  - [cin\\_data\\_get\\_framestore\\_counter](#), [26](#)
- CIN Data Initialization Routines, [22](#)
  - [cin\\_data\\_destroy](#), [22](#)
  - [cin\\_data\\_init](#), [22](#)
- CIN FCLK Configuration Routines, [18](#)
  - [cin\\_ctl\\_get\\_fclk](#), [18](#)
  - [cin\\_ctl\\_set\\_fclk](#), [18](#)
- CIN Firmware Upload Routines, [16](#)
  - [cin\\_ctl\\_load\\_config](#), [16](#)
  - [cin\\_ctl\\_load\\_firmware](#), [16](#)
  - [cin\\_ctl\\_load\\_firmware\\_data](#), [16](#)
  - [cin\\_ctl\\_load\\_firmware\\_file](#), [17](#)
- CIN Status Routines, [19](#)
- CIN\_CONFIG\_MAX\_TIMING\_DATA
  - [cin.h](#), [43](#)
- CIN\_CONFIG\_MAX\_TIMING\_MODES
  - [cin.h](#), [43](#)
- CIN\_CTL\_BIAS\_OFFSET
  - [cin.h](#), [43](#)
- CMD\_DISABLE\_CLKS
  - [cin\\_register\\_map.h](#), [49](#)
- CMD\_ENABLE\_CLKS
  - [cin\\_register\\_map.h](#), [50](#)
- CMD\_FCLK\_250
  - [cin\\_register\\_map.h](#), [50](#)
- CMD\_FCLK\_COMMIT
  - [cin\\_register\\_map.h](#), [50](#)
- CMD\_MON\_START
  - [cin\\_register\\_map.h](#), [50](#)
- CMD\_MON\_STOP
  - [cin\\_register\\_map.h](#), [50](#)
- CMD\_PS\_ENABLE
  - [cin\\_register\\_map.h](#), [50](#)
- CMD\_PS\_POWERDOWN
  - [cin\\_register\\_map.h](#), [50](#)
- CMD\_READ\_REG
  - [cin\\_register\\_map.h](#), [50](#)
- CMD\_RESET\_FRAME\_COUNT
  - [cin\\_register\\_map.h](#), [51](#)
- CMD\_SEND\_FCRIC\_CONFIG
  - [cin\\_register\\_map.h](#), [51](#)
- CMD\_SEND\_SYNC\_PULSE
  - [cin\\_register\\_map.h](#), [51](#)
- CMD\_SYNC\_DETECTOR2READOUT
  - [cin\\_register\\_map.h](#), [51](#)
- CMD\_WR\_CCD\_BIAS\_REG
  - [cin\\_register\\_map.h](#), [51](#)
- CMD\_WR\_CCD\_CLOCK\_REG
  - [cin\\_register\\_map.h](#), [51](#)
- Cin Control Initialization Routines, [9](#)
  - [cin\\_ctl\\_destroy](#), [9](#)
  - [cin\\_ctl\\_init](#), [10](#)
  - [cin\\_ctl\\_set\\_msg\\_callback](#), [10](#)
  - [cin\\_data\\_send\\_magic](#), [11](#)
- Cin Control Read/Rwrite Routines, [12](#)
  - [cin\\_ctl\\_read](#), [12](#)
  - [cin\\_ctl\\_stream\\_write](#), [12](#)
  - [cin\\_ctl\\_write](#), [13](#)
  - [cin\\_ctl\\_write\\_with\\_readback](#), [13](#)
- Cin Power Routines, [15](#)
  - [cin\\_ctl\\_fo\\_test\\_pattern](#), [15](#)
  - [cin\\_ctl\\_fp\\_pwr](#), [15](#)
  - [cin\\_ctl\\_pwr](#), [15](#)
- [cin.h](#)
  - [CIN\\_CONFIG\\_MAX\\_TIMING\\_DATA](#), [43](#)
  - [CIN\\_CONFIG\\_MAX\\_TIMING\\_MODES](#), [43](#)
  - [CIN\\_CTL\\_BIAS\\_OFFSET](#), [43](#)
- [cin\\_config\\_get\\_timing\\_name](#)
  - CIN Control Timing Routines, [21](#)
- [cin\\_config\\_timing](#), [29](#)
  - [cols](#), [29](#)
  - [data](#), [29](#)
  - [data\\_len](#), [29](#)
  - [fclk\\_freq](#), [29](#)
  - [framestore](#), [30](#)
  - [name](#), [30](#)
  - [overscan](#), [30](#)
  - [rows](#), [30](#)
- [cin\\_ctl](#), [30](#)
  - [fclk\\_time\\_factor](#), [31](#)
- [cin\\_ctl\\_destroy](#)
  - Cin Control Initialization Routines, [9](#)
- [cin\\_ctl\\_fo\\_test\\_pattern](#)
  - Cin Power Routines, [15](#)
- [cin\\_ctl\\_fp\\_pwr](#)
  - Cin Power Routines, [15](#)
- [cin\\_ctl\\_get\\_fclk](#)
  - CIN FCLK Configuration Routines, [18](#)
- [cin\\_ctl\\_id](#), [31](#)
- [cin\\_ctl\\_init](#)

- Cin Control Initialization Routines, 10
- cin\_ctl\_listener, 31
- cin\_ctl\_load\_config
  - CIN Firmware Upload Routines, 16
- cin\_ctl\_load\_firmware
  - CIN Firmware Upload Routines, 16
- cin\_ctl\_load\_firmware\_data
  - CIN Firmware Upload Routines, 16
- cin\_ctl\_load\_firmware\_file
  - CIN Firmware Upload Routines, 17
- cin\_ctl\_pwr
  - Cin Power Routines, 15
- cin\_ctl\_pwr\_mon\_t, 32
- cin\_ctl\_pwr\_val, 32
- cin\_ctl\_read
  - Cin Control Read/Rwrite Routines, 12
- cin\_ctl\_set\_fclk
  - CIN FCLK Configuration Routines, 18
- cin\_ctl\_set\_msg\_callback
  - Cin Control Initialization Routines, 10
- cin\_ctl\_stream\_write
  - Cin Control Read/Rwrite Routines, 12
- cin\_ctl\_write
  - Cin Control Read/Rwrite Routines, 13
- cin\_ctl\_write\_with\_readback
  - Cin Control Read/Rwrite Routines, 13
- cin\_data, 32
- cin\_data\_callbacks, 33
- cin\_data\_descramble\_map\_t, 33
- cin\_data\_destroy
  - CIN Data Initialization Routines, 22
- cin\_data\_frame, 34
- cin\_data\_framestore\_disable
  - CIN Data Framestore Functions, 25
- cin\_data\_framestore\_skip
  - CIN Data Framestore Functions, 25
- cin\_data\_framestore\_trigger
  - CIN Data Framestore Functions, 26
- cin\_data\_framestore\_trigger\_enable
  - CIN Data Framestore Functions, 26
- cin\_data\_get\_framestore\_counter
  - CIN Data Framestore Functions, 26
- cin\_data\_init
  - CIN Data Initialization Routines, 22
- cin\_data\_packet, 34
- cin\_data\_proc, 34
- cin\_data\_send\_magic
  - Cin Control Initialization Routines, 11
- cin\_data\_stats, 35
- cin\_data\_threads, 35
- cin\_map\_t, 35
- cin\_port, 36
- cin\_register\_map.h
  - CMD\_DISABLE\_CLKS, 49
  - CMD\_ENABLE\_CLKS, 50
  - CMD\_FCLK\_250, 50
  - CMD\_FCLK\_COMMIT, 50
  - CMD\_MON\_START, 50
  - CMD\_MON\_STOP, 50
  - CMD\_PS\_ENABLE, 50
  - CMD\_PS\_POWERDOWN, 50
  - CMD\_READ\_REG, 50
  - CMD\_RESET\_FRAME\_COUNT, 51
  - CMD\_SEND\_FCRIC\_CONFIG, 51
  - CMD\_SEND\_SYNC\_PULSE, 51
  - CMD\_SYNC\_DETECTOR2READOUT, 51
  - CMD\_WR\_CCD\_BIAS\_REG, 51
  - CMD\_WR\_CCD\_CLOCK\_REG, 51
  - REG\_BIASCONFIGREGISTER0\_REG, 51
  - REG\_BIASREGISTERDATAOUT, 51
  - REG\_CLOCK\_EN\_REG, 52
  - REG\_CLOCKCONFIGREGISTER0\_REG, 52
  - REG\_COMMAND, 52
  - REG\_DEBUGCOUNTER04\_REG, 52
  - REG\_DELAYTOSHUTTERLSB\_REG, 52
  - REG\_ETH\_ENABLE, 52
  - REG\_ETH\_RESET, 52
  - REG\_EXPOSURETIMELSB\_REG, 53
  - REG\_EXPOSURETIMEMSB\_REG, 53
  - REG\_FCLK\_I2C\_ADDRESS, 53
  - REG\_FCLK\_I2C\_DATA\_RD, 53
  - REG\_FCLK\_I2C\_DATA\_WR, 53
  - REG\_FCLK\_SET5, 53
  - REG\_FPGA\_VERSION, 53
  - REG\_FRM\_10GbE\_SEL, 54
  - REG\_FRM\_FPGA\_VERSION, 54
  - REG\_FRM\_RESET, 54
  - REG\_FRM\_SANDBOX\_REG0F, 54
  - REG\_FRM\_STREAM\_TYPE, 54
  - REG\_IMON\_ADC0\_CHF, 54
  - REG\_MAC\_CFG\_VECTOR1, 54
  - REG\_MAC\_CFG\_VECTOR2, 54
  - REG\_MAC\_STATS2\_FAB2B1, 55
  - REG\_PHY1\_MDIO\_CMD, 55
  - REG\_PS\_ENABLE, 55
  - REG\_PS\_SYNC\_DIV0, 55
  - REG\_PS\_SYNC\_DIV1, 55
  - REG\_PS\_SYNC\_DIV2, 55
  - REG\_PS\_SYNC\_DIV3, 55
  - REG\_PS\_SYNC\_DIV4, 55
  - REG\_SANDBOX\_REG0F, 56
  - REG\_SI570\_REG3, 56
  - REG\_SRAM\_COMMAND, 56
  - REG\_SRAM\_STATUS0, 56
  - REG\_STREAM\_TYPE, 56
  - REG\_TRIGGERMASK\_REG, 56
  - REG\_TRIGGERREPETITIONTIMELSB\_REG, 56
  - REG\_TRIGGERREPETITIONTIMEMSB\_REG, 56
- cols
  - cin\_config\_timing, 29
- data
  - cin\_config\_timing, 29
- data\_len
  - cin\_config\_timing, 29
- fclk\_freq

- cin\_config\_timing, [29](#)
- fclk\_time\_factor
  - cin\_ctl, [31](#)
- fifo, [36](#)
- framestore
  - cin\_config\_timing, [30](#)
- name
  - cin\_config\_timing, [30](#)
- overscan
  - cin\_config\_timing, [30](#)
- REG\_BIASCONFIGREGISTER0\_REG
  - cin\_register\_map.h, [51](#)
- REG\_BIASREGISTERDATAOUT
  - cin\_register\_map.h, [51](#)
- REG\_CLOCK\_EN\_REG
  - cin\_register\_map.h, [52](#)
- REG\_CLOCKCONFIGREGISTER0\_REG
  - cin\_register\_map.h, [52](#)
- REG\_COMMAND
  - cin\_register\_map.h, [52](#)
- REG\_DEBUGCOUNTER04\_REG
  - cin\_register\_map.h, [52](#)
- REG\_DELAYTOSHUTTERLSB\_REG
  - cin\_register\_map.h, [52](#)
- REG\_ETH\_ENABLE
  - cin\_register\_map.h, [52](#)
- REG\_ETH\_RESET
  - cin\_register\_map.h, [52](#)
- REG\_EXPOSURETIMELSB\_REG
  - cin\_register\_map.h, [53](#)
- REG\_EXPOSURETIMEMSB\_REG
  - cin\_register\_map.h, [53](#)
- REG\_FCLK\_I2C\_ADDRESS
  - cin\_register\_map.h, [53](#)
- REG\_FCLK\_I2C\_DATA\_RD
  - cin\_register\_map.h, [53](#)
- REG\_FCLK\_I2C\_DATA\_WR
  - cin\_register\_map.h, [53](#)
- REG\_FCLK\_SET5
  - cin\_register\_map.h, [53](#)
- REG\_FPGA\_VERSION
  - cin\_register\_map.h, [53](#)
- REG\_FRM\_10GbE\_SEL
  - cin\_register\_map.h, [54](#)
- REG\_FRM\_FPGA\_VERSION
  - cin\_register\_map.h, [54](#)
- REG\_FRM\_RESET
  - cin\_register\_map.h, [54](#)
- REG\_FRM\_SANDBOX\_REG0F
  - cin\_register\_map.h, [54](#)
- REG\_FRM\_STREAM\_TYPE
  - cin\_register\_map.h, [54](#)
- REG\_IMON\_ADC0\_CHF
  - cin\_register\_map.h, [54](#)
- REG\_MAC\_CFG\_VECTOR1
  - cin\_register\_map.h, [54](#)
- REG\_MAC\_CFG\_VECTOR2
  - cin\_register\_map.h, [54](#)
- REG\_MAC\_STATS2\_FAB2B1
  - cin\_register\_map.h, [55](#)
- REG\_PHY1\_MDIO\_CMD
  - cin\_register\_map.h, [55](#)
- REG\_PS\_ENABLE
  - cin\_register\_map.h, [55](#)
- REG\_PS\_SYNC\_DIV0
  - cin\_register\_map.h, [55](#)
- REG\_PS\_SYNC\_DIV1
  - cin\_register\_map.h, [55](#)
- REG\_PS\_SYNC\_DIV2
  - cin\_register\_map.h, [55](#)
- REG\_PS\_SYNC\_DIV3
  - cin\_register\_map.h, [55](#)
- REG\_PS\_SYNC\_DIV4
  - cin\_register\_map.h, [55](#)
- REG\_SANDBOX\_REG0F
  - cin\_register\_map.h, [56](#)
- REG\_SI570\_REG3
  - cin\_register\_map.h, [56](#)
- REG\_SRAM\_COMMAND
  - cin\_register\_map.h, [56](#)
- REG\_SRAM\_STATUS0
  - cin\_register\_map.h, [56](#)
- REG\_STREAM\_TYPE
  - cin\_register\_map.h, [56](#)
- REG\_TRIGGERMASK\_REG
  - cin\_register\_map.h, [56](#)
- REG\_TRIGGERREPETITIONIMELSB\_REG
  - cin\_register\_map.h, [56](#)
- REG\_TRIGGERREPETITIONIMEMSB\_REG
  - cin\_register\_map.h, [56](#)
- rows
  - cin\_config\_timing, [30](#)
- src/cin.h, [37](#)
- src/cin\_register\_map.h, [44](#)