

libcin

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Contents

1	FastCCD Communication Library (libcin)	1
2	Module Index	3
2.1	Modules	3
3	Class Index	5
3.1	Class List	5
4	File Index	7
4.1	File List	7
5	Module Documentation	9
5.1	Cin Control Initialization Routines	9
5.1.1	Detailed Description	9
5.1.2	Function Documentation	9
5.1.2.1	cin_ctl_destroy()	9
5.1.2.2	cin_ctl_init()	10
5.1.2.3	cin_data_send_magic()	10
5.2	Cin Control Read/Rwrite Routines	12
5.2.1	Detailed Description	12
5.2.2	Function Documentation	12
5.2.2.1	cin_ctl_read()	12
5.2.2.2	cin_ctl_stream_write()	12
5.2.2.3	cin_ctl_write()	13
5.2.2.4	cin_ctl_write_with_readback()	13

5.3	CIN Firmware Upload Routines	15
5.3.1	Detailed Description	15
5.4	CIN FCLK Configuration Routines	16
5.4.1	Detailed Description	16
5.5	CIN Status Routines	17
5.5.1	Detailed Description	17
5.6	CIN Control Bias Routines	18
5.6.1	Detailed Description	18
5.7	CIN COnTrol Timing Routines	19
5.7.1	Detailed Description	19
5.8	CIN Data Initialization Routines	20
5.8.1	Detailed Description	20
5.8.2	Function Documentation	20
5.8.2.1	cin_data_destroy()	20
5.8.2.2	cin_data_init()	20
5.9	CIN Data Framestore Functions	23
5.9.1	Detailed Description	23
5.9.2	Function Documentation	23
5.9.2.1	cin_data_framestore_disable()	23
5.9.2.2	cin_data_framestore_skip()	23
5.9.2.3	cin_data_framestore_trigger()	24
5.9.2.4	cin_data_framestore_trigger_enable()	24
5.9.2.5	cin_data_get_framestore_counter()	24

6 Class Documentation	27
6.1 cin_config_timing Struct Reference	27
6.1.1 Member Data Documentation	27
6.1.1.1 cols	27
6.1.1.2 data	27
6.1.1.3 data_len	27
6.1.1.4 fclk_freq	28
6.1.1.5 framestore	28
6.1.1.6 name	28
6.1.1.7 overscan	28
6.1.1.8 rows	28
6.2 cin_ctl Struct Reference	28
6.2.1 Member Data Documentation	29
6.2.1.1 fclk_time_factor	29
6.3 cin_ctl_id Struct Reference	29
6.4 cin_ctl_listener Struct Reference	29
6.5 cin_ctl_pwr_mon_t Struct Reference	30
6.6 cin_ctl_pwr_val Struct Reference	30
6.7 cin_data Struct Reference	30
6.8 cin_data_callbacks Struct Reference	31
6.9 cin_data_descramble_map_t Struct Reference	31
6.10 cin_data_frame Struct Reference	32
6.11 cin_data_packet Struct Reference	32
6.12 cin_data_proc Struct Reference	32
6.13 cin_data_stats Struct Reference	33
6.14 cin_data_threads Struct Reference	33
6.15 cin_map_t Struct Reference	33
6.16 cin_port Struct Reference	34
6.17 fifo Struct Reference	34

7 File Documentation	35
7.1 src/cin.h File Reference	35
7.1.1 Detailed Description	40
7.1.2 LICENSE	40
7.1.3 DESCRIPTION	41
7.1.4 Macro Definition Documentation	41
7.1.4.1 CIN_CONFIG_MAX_TIMING_DATA	41
7.1.4.2 CIN_CONFIG_MAX_TIMING_MODES	41
7.1.4.3 CIN_CTL_BIAS_OFFSET	41
7.2 src/cin_register_map.h File Reference	41
7.2.1 Detailed Description	46
7.2.2 LICENSE	46
7.2.3 DESCRIPTION	47
7.2.4 TIMING	47
7.2.5 Macro Definition Documentation	47
7.2.5.1 CMD_DISABLE_CLKS	47
7.2.5.2 CMD_ENABLE_CLKS	47
7.2.5.3 CMD_FCLK_250	47
7.2.5.4 CMD_FCLK_COMMIT	47
7.2.5.5 CMD_MON_START	47
7.2.5.6 CMD_MON_STOP	48
7.2.5.7 CMD_PS_ENABLE	48
7.2.5.8 CMD_PS_POWERDOWN	48
7.2.5.9 CMD_READ_REG	48
7.2.5.10 CMD_RESET_FRAME_COUNT	48
7.2.5.11 CMD_SEND_FCRIC_CONFIG	48
7.2.5.12 CMD_SEND_SYNC_PULSE	48
7.2.5.13 CMD_SYNC_DETECTOR2READOUT	48
7.2.5.14 CMD_WR_CCD_BIAS_REG	49
7.2.5.15 CMD_WR_CCD_CLOCK_REG	49

7.2.5.16	REG_BIASCONFIGREGISTER0_REG	49
7.2.5.17	REG_BIASREGISTERDATAOUT	49
7.2.5.18	REG_CLOCK_EN_REG	49
7.2.5.19	REG_CLOCKCONFIGREGISTER0_REG	49
7.2.5.20	REG_COMMAND	49
7.2.5.21	REG_DEBUGCOUNTER04_REG	49
7.2.5.22	REG_DELAYTOSHUTTERLSB_REG	50
7.2.5.23	REG_ETH_ENABLE	50
7.2.5.24	REG_ETH_RESET	50
7.2.5.25	REG_EXPOSURETIMELSB_REG	50
7.2.5.26	REG_EXPOSURETIMEMSB_REG	50
7.2.5.27	REG_FCLK_I2C_ADDRESS	50
7.2.5.28	REG_FCLK_I2C_DATA_RD	50
7.2.5.29	REG_FCLK_I2C_DATA_WR	51
7.2.5.30	REG_FCLK_SET5	51
7.2.5.31	REG_FPGA_VERSION	51
7.2.5.32	REG_FRM_10GbE_SEL	51
7.2.5.33	REG_FRM_FPGA_VERSION	51
7.2.5.34	REG_FRM_RESET	51
7.2.5.35	REG_FRM_SANDBOX_REG0F	51
7.2.5.36	REG_FRM_STREAM_TYPE	52
7.2.5.37	REG_IMON_ADC0_CHF	52
7.2.5.38	REG_MAC_CFG_VECTOR1	52
7.2.5.39	REG_MAC_CFG_VECTOR2	52
7.2.5.40	REG_MAC_STATS2_FAB2B1	52
7.2.5.41	REG_PHY1_MDIO_CMD	52
7.2.5.42	REG_PS_ENABLE	52
7.2.5.43	REG_PS_SYNC_DIV0	52
7.2.5.44	REG_PS_SYNC_DIV1	53
7.2.5.45	REG_PS_SYNC_DIV2	53
7.2.5.46	REG_PS_SYNC_DIV3	53
7.2.5.47	REG_PS_SYNC_DIV4	53
7.2.5.48	REG_SANDBOX_REG0F	53
7.2.5.49	REG_SI570_REG3	53
7.2.5.50	REG_SRAM_COMMAND	53
7.2.5.51	REG_SRAM_STATUS0	54
7.2.5.52	REG_STREAM_TYPE	54
7.2.5.53	REG_TRIGGERMASK_REG	54
7.2.5.54	REG_TRIGGERREPETITIONTIMELSB_REG	54
7.2.5.55	REG_TRIGGERREPETITIONTIMEMSB_REG	54

Chapter 1

FastCCD Communication Library (libcin)

Introduction

This library, based in C is designed to control the FastCCD detector from Lawrence Berkeley National Laboratory. It controls both camera control functions and data acquisition (frame acquisition). It is separated into two distinct parts, the control part ,[cin_ctl](#), and the data (image) part named [cin_data](#). It was written in part for use with areaDetector.

Prerequisites

The library relies on the following:

- `libbsd` (Used for string manipulation)
- `libconfig` (Used for nice config files)
- `libpthread` (Used for threading)
- `librt` (Used for time functions)

Installation

Installation of the library is like most unix based source packages:

```
./make
./make doc
./make test
./make install
```

TCP/IP Stack Tuning

In order for the CIN data to operate efficiently, the 10G interface on the host computer needs to be tuned. This needs to be done by adding the following to the file `/etc/sysctl.conf`.

```
# Increase the maximum buffer that user programs can request
# 2147483647 = 2048 Mb
net.core.rmem_max=2147483647
net.core.wmem_max=2147483647
# Set a default value 10 times bigger
net.core.rmem_default=1000000
net.core.wmem_default=1000000
# increase the length of the processor input queue
net.core.netdev_max_backlog = 250000
# recommended for hosts with jumbo frames enabled
net.ipv4.tcp_mt看u_probing=1
```

These can be reread by the system without rebooting by entering the command:

```
$sudo sysctl --system
```

Versioning

For the versions available, see the [tags on this repository](#).

Authors

- **Stuart B. Wilkins** - [stuwilkins](#)

See also the list of [contributors](#) who participated in this project.

License

This project is licensed under the BSD License - see the [LICENSE](#) file for details

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A huge thanks to Peter Dennes, John Joseph and the detector team at LBNL and the team at Sydor Instruments.

Chapter 2

Module Index

2.1 Modules

Here is a list of all modules:

Cin Control Initialization Routines	9
Cin Control Read/Rwrite Routines	12
CIN Firmware Upload Routines	15
CIN FCLK Configuration Routines	16
CIN Status Routines	17
CIN Control Bias Routines	18
CIN Control Timing Routines	19
CIN Data Initialization Routines	20
CIN Data Framestore Functions	23

Chapter 3

Class Index

3.1 Class List

Here are the classes, structs, unions and interfaces with brief descriptions:

cin_config_timing	27
cin_ctl	28
cin_ctl_id	29
cin_ctl_listener	29
cin_ctl_pwr_mon_t	30
cin_ctl_pwr_val	30
cin_data	30
cin_data_callbacks	31
cin_data_descramble_map_t	31
cin_data_frame	32
cin_data_packet	32
cin_data_proc	32
cin_data_stats	33
cin_data_threads	33
cin_map_t	33
cin_port	34
fifo	34

Chapter 4

File Index

4.1 File List

Here is a list of all documented files with brief descriptions:

src/ cin.h	35
src/ cin_register_map.h	41
src/ cinregisters.h	??
src/ common.h	??
src/ config.h	??
src/ control.h	??
src/ data.h	??
src/ descramble.h	??
src/ descramble_map.h	??
src/ fifo.h	??
src/ report.h	??

Chapter 5

Module Documentation

5.1 Cin Control Initialization Routines

Functions

- int `cin_ctl_init` (`cin_ctl_t` *cin, char *addr, uint16_t port, uint16_t sport, char *bind_addr, uint16_t bind_port, uint16_t bind_sport)
- int `cin_ctl_destroy` (`cin_ctl_t` *cin)
- void `cin_ctl_message` (`cin_ctl_t` *cin, char *message, int severity)
- void `cin_ctl_set_msg_callback` (`cin_ctl_t` *cin, void *msg_callback, void *ptr)
- int `cin_data_send_magic` (`cin_data_t` *cin)

5.1.1 Detailed Description

5.1.2 Function Documentation

5.1.2.1 `cin_ctl_destroy()`

```
int cin_ctl_destroy (  
    cin_ctl_t * cin )
```

Destroy (close) the cin control library

Close connections, free memory and exit library

Parameters

<code>cin</code>	handle to cin library
------------------	-----------------------

Returns

Returns 0 on success non-zero if error

5.1.2.2 cin_ctl_init()

```
int cin_ctl_init (
    cin_ctl_t * cin,
    char * addr,
    uint16_t port,
    uint16_t sport,
    char * bind_addr,
    uint16_t bind_port,
    uint16_t bind_sport )
```

Initialize the cin control library

Initialize the control structures and communications with the CIN via the control interface. This function opens the UDP ports and starts a listening thread to receive packets from the CIN.

Parameters

<i>cin</i>	handle to cin library
<i>addr</i>	ip address of CIN base address
<i>port</i>	UDP port of cin
<i>sport</i>	stream output UDP port of cin
<i>bind_addr</i>	ip address to bind to
<i>bind_port</i>	input udp port of cin
<i>bind_sport</i>	stream input udp port of cin

Returns

Returns 0 on success non-zero if error

5.1.2.3 cin_data_send_magic()

```
int cin_data_send_magic (
    cin_data_t * cin )
```

Send a magic packet to the CIN to initialize data

Parameters

<i>cin</i>	handle to cin library
------------	-----------------------

Returns

Returns 0 on success non-zero if error

5.2 Cin Control Read/Rwrite Routines

Functions

- int `cin_ctl_read` (`cin_ctl_t` *cin, uint16_t reg, uint16_t *val, int wait)
- int `cin_ctl_write` (`cin_ctl_t` *cin, uint16_t reg, uint16_t val, int wait)
- int `cin_ctl_stream_write` (`cin_ctl_t` *cin, unsigned char *val, int size)
- int `cin_ctl_write_with_readback` (`cin_ctl_t` *cin, uint16_t reg, uint16_t val)
- int `cin_ctl_pwr` (`cin_ctl_t` *cin, int pwr)
- int `cin_ctl_fp_pwr` (`cin_ctl_t` *cin, int pwr)
- int `cin_ctl_fo_test_pattern` (`cin_ctl_t` *cin, int on_off)

5.2.1 Detailed Description

5.2.2 Function Documentation

5.2.2.1 cin_ctl_read()

```
int cin_ctl_read (
    cin_ctl_t * cin,
    uint16_t reg,
    uint16_t * val,
    int wait )
```

Read register from CIN

Parameters

<i>cin</i>	handle to cin library
<i>reg</i>	register to read
<i>val</i>	variable to read value of register to
<i>wait</i>	if non-zero, wait a predefined time before read command (for i2c)

Returns

Returns 0 on success non-zero if error

5.2.2.2 cin_ctl_stream_write()

```
int cin_ctl_stream_write (
    cin_ctl_t * cin,
    unsigned char * val,
    int size )
```

Write stream data to CIN

Parameters

<i>cin</i>	handle to cin library
<i>val</i>	array of values to write
<i>size</i>	size of array pointed to by val

Write stream data to cin in form of 16 bit array.

Returns

Returns 0 on success non-zero if error

5.2.2.3 cin_ctl_write()

```
int cin_ctl_write (
    cin_ctl_t * cin,
    uint16_t reg,
    uint16_t val,
    int wait )
```

Write register to CIN

Parameters

<i>cin</i>	handle to cin library
<i>reg</i>	register to write to
<i>val</i>	value to write to register
<i>wait</i>	if non-zero

Write register value to CIN. If wait is non-zero then wait a sleep time of i CIN_CTL_WRITE_SLEEP before releasing the mutex to add flow control to the cin.

Returns

Returns 0 on success non-zero if error

5.2.2.4 cin_ctl_write_with_readback()

```
int cin_ctl_write_with_readback (
    cin_ctl_t * cin,
    uint16_t reg,
    uint16_t val )
```

Write register to CIN with readback verification

Parameters

<i>cin</i>	handle to cin library
<i>reg</i>	register to write to
<i>val</i>	value to write to register

Write register value to CIN. Follow write with read of register and compare value. CIN_CTL_WRITE_SLEEP before releasing the mutex to add flow control to the cin.

Returns

Returns 0 on success non-zero if error

5.3 CIN Firmware Upload Routines

Functions

- int **cin_ctl_load_config** ([cin_ctl_t](#) *cin, char *filename)
- int **cin_ctl_load_firmware** ([cin_ctl_t](#) *cin)
- int **cin_ctl_load_firmware_file** ([cin_ctl_t](#) *cin, char *filename)
- int **cin_ctl_load_firmware_data** ([cin_ctl_t](#) *cin, unsigned char *data, int data_len)

5.3.1 Detailed Description

Firmware upload routines

5.4 CIN FCLK Configuration Routines

Functions

- int **cin_ctl_get_fclk** ([cin_ctl_t](#) *cin, int *clkfreq)
- int **cin_ctl_set_fclk** ([cin_ctl_t](#) *cin, int clkfreq)

5.4.1 Detailed Description

FCLK (Internal FPGA Clock) Routines

5.5 CIN Status Routines

Functions

- int **cin_ctl_get_cfg_fpga_status** ([cin_ctl_t](#) *cin, uint16_t *_val)
- int **cin_ctl_get_id** ([cin_ctl_t](#) *cin, [cin_ctl_id_t](#) *_val)
- int **cin_ctl_get_dcm_status** ([cin_ctl_t](#) *cin, uint16_t *_val)
- int **cin_ctl_get_power_status** ([cin_ctl_t](#) *cin, int full, int *pwr, [cin_ctl_pwr_mon_t](#) *values)

5.5.1 Detailed Description

Status Routines

5.6 CIN Control Bias Routines

Functions

- int **cin_ctl_set_bias** ([cin_ctl_t](#) *cin, int val)
- int **cin_ctl_get_bias** ([cin_ctl_t](#) *cin, int *val)
- int **cin_ctl_set_bias_regs** ([cin_ctl_t](#) *cin, uint16_t *vals, int verify)
- int **cin_ctl_get_bias_regs** ([cin_ctl_t](#) *cin, uint16_t *vals)
- int **cin_ctl_set_bias_voltages** ([cin_ctl_t](#) *cin, float *voltage, int verify)
- int **cin_ctl_get_bias_voltages** ([cin_ctl_t](#) *cin, float *voltage, uint16_t *regs)

5.6.1 Detailed Description

Initialization group

5.7 CIN Control Timing Routines

Functions

- int **cin_ctl_set_timing_regs** ([cin_ctl_t](#) *cin, uint16_t *vals, int vals_len)
- int **cin_ctl_get_timing_regs** ([cin_ctl_t](#) *cin, uint16_t *vals, int vals_len)

5.7.1 Detailed Description

Timing setup group

5.8 CIN Data Initialization Routines

Functions

- int `cin_data_init` (`cin_data_t` *cin, char *addr, uint16_t port, char *bind_addr, uint16_t bind_port, int rcvbuf, int packet_buffer_len, int frame_buffer_len, cin_data_callback push_callback, cin_data_callback pop_callback, void *usr_ptr)
- void `cin_data_destroy` (`cin_data_t` *cin)

5.8.1 Detailed Description

Initialization group

5.8.2 Function Documentation

5.8.2.1 `cin_data_destroy()`

```
void cin_data_destroy (
    cin_data_t * cin )
```

Close the cin data library and cleanup

Stop all the processing threads and join them to the main thread. This function blocks until all threads have joined the main thread (program). This should be called to clean up the library before the program is exited

Parameters

<i>cin</i>	Handle to cin data library
------------	----------------------------

5.8.2.2 `cin_data_init()`

```
int cin_data_init (
    cin_data_t * cin,
    char * addr,
    uint16_t port,
    char * bind_addr,
    uint16_t bind_port,
    int rcvbuf,
    int packet_buffer_len,
    int frame_buffer_len,
    cin_data_callback push_callback,
    cin_data_callback pop_callback,
    void * usr_ptr )
```

Initialize the cin data library

Initialize the data handling routines and start the threads for listening.

Parameters

<i>cin</i>	Handle to cin data library
<i>addr</i>	IP-Address of cin (if NULL defaults to standard)
<i>port</i>	UDP Port of CIN
<i>bind_addr</i>	IP-Address to bind to (if NULL binds to 0.0.0.0)
<i>bind_port</i>	UDP Port of host
<i>rcvbuf</i>	TCP/IP Kernel receive buffer size
<i>packet_buffer_len</i>	Length of packet buffer fifo (in units number of packets)
<i>frame_buffer_len</i>	Length of frame (assembler) buffer fifo (in units of number of frames)
<i>push_callback</i>	This function is called when a data structure is needed
<i>pop_callback</i>	This function is called when an image has been processed
<i>usr_ptr</i>	Pointer passed to callback functions

5.9 CIN Data Framestore Functions

Functions

- void `cin_data_framestore_trigger` (`cin_data_t` *cin, int count)
- void `cin_data_framestore_skip` (`cin_data_t` *cin, int count)
- int `cin_data_get_framestore_counter` (`cin_data_t` *cin)
- void `cin_data_framestore_disable` (`cin_data_t` *cin)
- void `cin_data_framestore_trigger_enable` (`cin_data_t` *cin)

5.9.1 Detailed Description

Framestore Group

5.9.2 Function Documentation

5.9.2.1 `cin_data_framestore_disable()`

```
void cin_data_framestore_disable (  
    cin_data_t * cin )
```

Disable the framestore modes

This function disables the framestore modes (software trigger and skip). If the camera is hardware triggering then the images will start to be processed.

Parameters

<code>cin</code>	Handle to the cin library
------------------	---------------------------

5.9.2.2 `cin_data_framestore_skip()`

```
void cin_data_framestore_skip (  
    cin_data_t * cin,  
    int count )
```

Enable framestore skip mode

Enable the framestore skip mode. This function should be called before hardware triggering the camera. This causes the data processing to skip

Parameters

<i>count</i>	frames from the first images to be read. This is usually done to stop the first few frames from being over exposed.
<i>cin</i>	handle to the cin_data library

5.9.2.3 `cin_data_framestore_trigger()`

```
void cin_data_framestore_trigger (
    cin_data_t * cin,
    int count )
```

Send a framestore (software) trigger

Send a software trigger to the CIN by timestamping the request time and allow images to be processed when recieved after this time. The count option sets the number of frames to trigger. A value of -1 indicated that the trigger should not count images but run indefinitely after the trigger has occurred.

Parameters

<i>cin</i>	handle to the cin_data library
<i>count</i>	number of frames to trigger

5.9.2.4 `cin_data_framestore_trigger_enable()`

```
void cin_data_framestore_trigger_enable (
    cin_data_t * cin )
```

Enable the framestore trigger mode

This function enables the framestore trigger mode. It cases the images to not be processed pending a call to the function to (software) trigger the camera.

Parameters

<i>cin</i>	Handle to the cin library
------------	---------------------------

5.9.2.5 `cin_data_get_framestore_counter()`

```
int cin_data_get_framestore_counter (
    cin_data_t * cin )
```


Get the value of the framestore counter

Return the number of frames in the framestore counter. In trigger mode, this returns the number of frames to go. In skip mode, this returns the number of frames that have to be skipped.

Parameters

<i>cin</i>	handle to the cin_data library
------------	--

Returns

Number of frames to go in trigger

Chapter 6

Class Documentation

6.1 cin_config_timing Struct Reference

Public Attributes

- uint16_t * [data](#)
- int [data_len](#)
- char [name](#) [40]
- int [rows](#)
- int [cols](#)
- int [overscan](#)
- int [fclk_freq](#)
- int [framestore](#)

6.1.1 Member Data Documentation

6.1.1.1 cols

```
int cin_config_timing::cols
```

Cols for this timing setup

6.1.1.2 data

```
uint16_t* cin_config_timing::data
```

Pointer to timing data

6.1.1.3 data_len

```
int cin_config_timing::data_len
```

timing data length

6.1.1.4 fclk_freq

```
int cin_config_timing::fclk_freq
```

FCLK Frequency to use

6.1.1.5 framestore

```
int cin_config_timing::framestore
```

Flag (not zero means framestore

6.1.1.6 name

```
char cin_config_timing::name[40]
```

String for config name

6.1.1.7 overscan

```
int cin_config_timing::overscan
```

Number of overscan cols for this setup

6.1.1.8 rows

```
int cin_config_timing::rows
```

Rows for this timing setup

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

6.2 cin_ctl Struct Reference

Public Attributes

- char * **addr**
- char * **bind_addr**
- int **port**
- int **bind_port**
- int **sport**
- int **bind_sport**
- [cin_port_t](#) **ctl_port**
- [cin_port_t](#) **stream_port**
- [cin_config_timing_t](#) **timing** [[CIN_CONFIG_MAX_TIMING_MODES](#)]
- int **timing_num**
- [cin_config_timing_t](#) * **current_timing**
- float **fclk_time_factor**
- [cin_ctl_listener_t](#) * **listener**
- pthread_mutex_t **access**
- pthread_mutexattr_t **access_attr**
- void(* **msg_callback**)(char *, int, void *)
- void * **msg_callback_ptr**

6.2.1 Member Data Documentation

6.2.1.1 fclk_time_factor

```
float cin_ctl::fclk_time_factor
```

In micro seconds

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

6.3 cin_ctl_id Struct Reference

Public Attributes

- uint16_t **base_board_id**
- uint16_t **base_serial_no**
- uint16_t **base_fpga_ver**
- uint16_t **fabric_board_id**
- uint16_t **fabric_serial_no**
- uint16_t **fabric_fpga_ver**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

6.4 cin_ctl_listener Struct Reference

Public Attributes

- struct [cin_port](#) * **cp**
- [fifo](#) **ctl_fifo**
- pthread_t **thread_id**
- pthread_barrier_t **barrier**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

6.5 cin_ctl_pwr_mon_t Struct Reference

Public Attributes

- [cin_ctl_pwr_val_t](#) **bus_12v0**
- [cin_ctl_pwr_val_t](#) **mgmt_3v3**
- [cin_ctl_pwr_val_t](#) **mgmt_2v5**
- [cin_ctl_pwr_val_t](#) **mgmt_1v2**
- [cin_ctl_pwr_val_t](#) **enet_1v0**
- [cin_ctl_pwr_val_t](#) **s3e_3v3**
- [cin_ctl_pwr_val_t](#) **gen_3v3**
- [cin_ctl_pwr_val_t](#) **gen_2v5**
- [cin_ctl_pwr_val_t](#) **v6_0v9**
- [cin_ctl_pwr_val_t](#) **v6_1v0**
- [cin_ctl_pwr_val_t](#) **v6_2v5**
- [cin_ctl_pwr_val_t](#) **fp**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

6.6 cin_ctl_pwr_val Struct Reference

Public Attributes

- double **i**
- double **v**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

6.7 cin_data Struct Reference

Public Attributes

- [fifo](#) * **packet_fifo**
- [fifo](#) * **frame_fifo**
- [cin_data_threads_t](#) **listen_thread**
- [cin_data_threads_t](#) **assembler_thread**
- [cin_data_threads_t](#) **descramble_thread**
- [pthread_mutex_t](#) **descramble_mutex**
- [pthread_mutex_t](#) **stats_mutex**
- [pthread_mutex_t](#) **framestore_mutex**
- [cin_data_callbacks_t](#) **callbacks**
- char * **addr**
- char * **bind_addr**
- int **port**

- int **bind_port**
- int **recv_buf**
- [cin_port_t](#) **dp**
- struct timespec **framerate**
- unsigned long int **dropped_packets**
- unsigned long int **malformed_packets**
- uint16_t **last_frame**
- [cin_data_descramble_map_t](#) **map**
- int **framestore_mode**
- struct timespec **framestore_trigger**
- int **framestore_counter**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

6.8 cin_data_callbacks Struct Reference

Public Attributes

- void **push** ([cin_data_frame_t](#) *, void *usr_ptr)
- void **pop** ([cin_data_frame_t](#) *, void *usr_ptr)
- [cin_data_frame_t](#) * **frame**
- void * **usr_ptr**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

6.9 cin_data_descramble_map_t Struct Reference

Public Attributes

- uint32_t * **map**
- int **size_x**
- int **size_y**
- int **overscan**
- int **rows**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

6.10 cin_data_frame Struct Reference

Public Attributes

- uint16_t * **data**
- uint16_t **number**
- struct timespec **timestamp**
- int **size_x**
- int **size_y**

The documentation for this struct was generated from the following file:

- [src/cin.h](#)

6.11 cin_data_packet Struct Reference

Public Attributes

- unsigned char * **data**
- int **size**
- struct timespec **timestamp**

The documentation for this struct was generated from the following file:

- [src/data.h](#)

6.12 cin_data_proc Struct Reference

Public Attributes

- void *(* **input_get**)(void *, int)
- void *(* **input_put**)(void *, int)
- void * **input_args**
- int **reader**
- void *(* **output_put**)(void *)
- void *(* **output_get**)(void *)
- void * **output_args**
- [cin_data_t](#) * **parent**

The documentation for this struct was generated from the following file:

- [src/data.h](#)

6.13 cin_data_stats Struct Reference

Public Attributes

- int **last_frame**
- double **framerate**
- double **packet_percent_full**
- double **frame_percent_full**
- double **image_percent_full**
- long int **packet_overruns**
- long int **frame_overruns**
- long int **image_overruns**
- long int **packet_used**
- long int **frame_used**
- long int **image_used**
- long int **dropped_packets**
- long int **malformed_packets**

The documentation for this struct was generated from the following file:

- src/[cin.h](#)

6.14 cin_data_threads Struct Reference

Public Attributes

- pthread_t **thread_id**
- int **started**

The documentation for this struct was generated from the following file:

- src/[cin.h](#)

6.15 cin_map_t Struct Reference

Public Attributes

- char * **name**
- uint16_t **reg**

The documentation for this struct was generated from the following file:

- src/cinregisters.h

6.16 cin_port Struct Reference

Public Attributes

- int **sockfd**
- struct timeval **tv**
- struct sockaddr_in **sin_srv**
- struct sockaddr_in **sin_cli**
- socklen_t **slen**

The documentation for this struct was generated from the following file:

- src/[cin.h](#)

6.17 fifo Struct Reference

Public Attributes

- void * **data**
- void * **head**
- void * **tail**
- void * **end**
- long int **size**
- int **elem_size**
- int **full**
- long int **overruns**
- pthread_mutex_t **mutex**
- pthread_cond_t **signal**

The documentation for this struct was generated from the following file:

- src/[cin.h](#)

Chapter 7

File Documentation

7.1 src/cin.h File Reference

```
#include <stdint.h>
#include <stdio.h>
#include <sys/socket.h>
#include <netinet/in.h>
#include <netinet/ip.h>
#include <sys/time.h>
#include <pthread.h>
```

Classes

- struct [fifo](#)
- struct [cin_ctl_listener](#)
- struct [cin_port](#)
- struct [cin_config_timing](#)
- struct [cin_ctl](#)
- struct [cin_data_frame](#)
- struct [cin_data_stats](#)
- struct [cin_data_threads](#)
- struct [cin_data_callbacks](#)
- struct [cin_data_descramble_map_t](#)
- struct [cin_data](#)
- struct [cin_ctl_id](#)
- struct [cin_ctl_pwr_val](#)
- struct [cin_ctl_pwr_mon_t](#)

Macros

- #define **CIN_OK** 0
- #define **CIN_ERROR** -1
- #define **CIN_CTL_MSG_OK** 0
- #define **CIN_CTL_MSG_MINOR** 1
- #define **CIN_CTL_MSG_MAJOR** 2

- #define CIN_CTL_IP "192.168.1.207"
- #define CIN_CTL_CIN_PORT 49200
- #define CIN_CTL_BIND_PORT 50200
- #define CIN_CTL_FRMW_CIN_PORT 49202
- #define CIN_CTL_FRMW_BIND_PORT 50202
- #define CIN_CTL_RCVBUF 10
- #define CIN_CTL_MAX_READ_TRIES 5
- #define CIN_CTL_MAX_WRITE_TRIES 5
- #define CIN_CTL_WRITE_SLEEP 100
- #define CIN_CTL_READ_SLEEP 100
- #define CIN_CTL_BIAS_SLEEP 100000
- #define CIN_CTL_FO_SLEEP 500000
- #define CIN_CTL_CONFIG_SLEEP 100
- #define CIN_CTL_DCO_SLEEP 1000000
- #define CIN_CTL_FCLK_SLEEP 200000
- #define CIN_CTL_STREAM_CHUNK 512
- #define CIN_CTL_STREAM_SLEEP 5
- #define CIN_CTL_POWER_ENABLE 0x001F
- #define CIN_CTL_POWER_DISABLE 0x0000
- #define CIN_CTL_FP_POWER_ENABLE 0x0020
- #define CIN_CTL_DCM_LOCKED 0x0001
- #define CIN_CTL_DCM_PSDONE 0x0002
- #define CIN_CTL_DCM_STATUS0 0x0004
- #define CIN_CTL_DCM_STATUS1 0x0008
- #define CIN_CTL_DCM_STATUS2 0x0010
- #define CIN_CTL_DCM_TX1_READY 0x0020
- #define CIN_CTL_DCM_TX2_READY 0x0040
- #define CIN_CTL_DCM_ATCA_ALARM 0x0080
- #define CIN_CTL_TRIG_INTERNAL 0x0000
- #define CIN_CTL_TRIG_EXTERNAL_1 0x0001
- #define CIN_CTL_TRIG_EXTERNAL_2 0x0002
- #define CIN_CTL_TRIG_EXTERNAL_BOTH 0x0003
- #define CIN_CTL_FOCUS_BIT 0x0002
- #define CIN_CTL_FCLK_125 0x0000
- #define CIN_CTL_FCLK_200 0x0001
- #define CIN_CTL_FCLK_250 0x0002
- #define CIN_CTL_FCLK_125_C 0x0003
- #define CIN_CTL_FCLK_200_C 0x0004
- #define CIN_CTL_FCLK_250_C 0x0005
- #define CIN_CTL_FCLK_156_C 0x0006
- #define CIN_CTL_FPGA_STS_CFG 0x8000
- #define CIN_CTL_FPGA_STS_FP_PWR 0x0008
- #define CIN_CTL_DCM_STS_ATCA 0x0080
- #define CIN_CTL_DCM_STS_LOCKED 0x0001
- #define CIN_CTL_DCM_STS_OVERRIDE 0x0800
- #define CIN_CTL_MUX1_VCLK1 0x0001
- #define CIN_CTL_MUX1_VCLK2 0x0002
- #define CIN_CTL_MUX1_VCLK3 0x0003
- #define CIN_CTL_MUX1_ATG 0x0004
- #define CIN_CTL_MUX1_VFCLK1 0x0005
- #define CIN_CTL_MUX1_VFCLK2 0x0006
- #define CIN_CTL_MUX1_VFCLK3 0x0007
- #define CIN_CTL_MUX1_HCLK1 0x0008
- #define CIN_CTL_MUX1_HCLK2 0x0009
- #define CIN_CTL_MUX1_OSW 0x000A

- #define **CIN_CTL_MUX1_RST** 0x000B
- #define **CIN_CTL_MUX1_CONVERT** 0x000C
- #define **CIN_CTL_MUX1_SHUTTER** 0x000D
- #define **CIN_CTL_MUX1_SWTRIGGER** 0x000E
- #define **CIN_CTL_MUX1_TRIGMON** 0x000F
- #define **CIN_CTL_MUX1_EXPOSE** 0x0000
- #define **CIN_CTL_MUX2_VCLK1** 0x0010
- #define **CIN_CTL_MUX2_VCLK2** 0x0020
- #define **CIN_CTL_MUX2_VCLK3** 0x0030
- #define **CIN_CTL_MUX2_ATG** 0x0040
- #define **CIN_CTL_MUX2_VFCLK1** 0x0050
- #define **CIN_CTL_MUX2_VFCLK2** 0x0060
- #define **CIN_CTL_MUX2_VFCLK3** 0x0070
- #define **CIN_CTL_MUX2_HCLK1** 0x0080
- #define **CIN_CTL_MUX2_HCLK2** 0x0090
- #define **CIN_CTL_MUX2_HCLK3** 0x00A0
- #define **CIN_CTL_MUX2_OSW** 0x00B0
- #define **CIN_CTL_MUX2_RST** 0x00C0
- #define **CIN_CTL_MUX2_CONVERT** 0x00D0
- #define **CIN_CTL_MUX2_SAVE** 0x00E0
- #define **CIN_CTL_MUX2_HWTRIG** 0x00F0
- #define **CIN_CTL_MUX2_EXPOSE** 0x0000
- #define **CIN_CTL_FO_REG1** 0x821D
- #define **CIN_CTL_FO_REG2** 0x821E
- #define **CIN_CTL_FO_REG3** 0x821F
- #define **CIN_DATA_IP** "10.0.5.207"
- #define **CIN_DATA_BIND_PORT** 49201
- #define **CIN_DATA_CIN_PORT** 49203
- #define **CIN_DATA_MAX_MTU** 9000
- #define **CIN_DATA_UDP_HEADER** 8
- #define **CIN_DATA_MAGIC_PACKET** UINT64_C(0x0000F4F3F2F1F000)
- #define **CIN_DATA_MAGIC_PACKET_MASK** UINT64_C(0x0000FFFFFFFFFFFFF00)
- #define **CIN_DATA_TAIL_MAGIC_PACKET** UINT64_C(0x010DF0ADDEF2F1F0)
- #define **CIN_DATA_TAIL_MAGIC_PACKET_MASK** UINT64_C(0xFFFFFFFFFFFFFFFFF)
- #define **CIN_DATA_DROPPED_PACKET_VAL** 0x2000
- #define **CIN_DATA_DATA_MASK** 0x1FFF
- #define **CIN_DATA_CTRL_MASK** 0xE000
- #define **CIN_DATA_SIGN_MASK** 0x1000
- #define **CIN_DATA_GAIN_8** 0xC000
- #define **CIN_DATA_GAIN_4** 0x4000
- #define **CIN_DATA_PACKET_LEN** 8184
- #define **CIN_DATA_MAX_PACKETS** 542
- #define **CIN_DATA_RCVBUF** (100*1024*1024)
- #define **CIN_DATA_MAX_FRAME_X** 1152
- #define **CIN_DATA_MAX_FRAME_Y** 2050
- #define **CIN_DATA_MAX_STREAM** 2400000
- #define **CIN_DATA_CCD_COLS** 96
- #define **CIN_DATA_CCD_COLS_PER_CHAN** 10
- #define **CIN_DATA_PIPELINE_FLUSH** 1344
- #define **CIN_CTL_NUM_BIAS** 20
- #define **CIN_CTL_BIAS_OFFSET** 0x0030
- #define **CIN_CTL_BIAS_POSH** 0
- #define **CIN_CTL_BIAS_NEGH** 1
- #define **CIN_CTL_BIAS_POSRG** 2
- #define **CIN_CTL_BIAS_NEGRG** 3

- `#define CIN_CTL_BIAS_POSSW 4`
- `#define CIN_CTL_BIAS_NEGSW 5`
- `#define CIN_CTL_BIAS_POSV 6`
- `#define CIN_CTL_BIAS_NEGV 7`
- `#define CIN_CTL_BIAS_POSTG 8`
- `#define CIN_CTL_BIAS_NEGTG 9`
- `#define CIN_CTL_BIAS_POSVF 10`
- `#define CIN_CTL_BIAS_NEGVF 11`
- `#define CIN_CTL_BIAS_NEDGE 12`
- `#define CIN_CTL_BIAS_OTG 13`
- `#define CIN_CTL_BIAS_VDDR 14`
- `#define CIN_CTL_BIAS_VDD_OUT 15`
- `#define CIN_CTL_BIAS_BUF_BASE 16`
- `#define CIN_CTL_BIAS_BUF_DELTA 17`
- `#define CIN_CTL_BIAS_SPARE1 18`
- `#define CIN_CTL_BIAS_SPARE2 19`
- `#define DEBUG_PRINT(fmt, ...) if(_debug_print_flag) { fprintf(stderr, "%s:%d:%s(): " fmt, __FILE__, __LINE__, __func__, __VA_ARGS__); }`
- `#define DEBUG_COMMENT(fmt) if(_debug_print_flag) { fprintf(stderr, "%s:%d:%s(): " fmt, __FILE__, __LINE__, __func__); }`
- `#define ERROR_COMMENT(fmt) if(_error_print_flag) { fprintf(stderr, "%s:%d:%s(): " fmt, __FILE__, __LINE__, __func__); }`
- `#define ERROR_PRINT(fmt, ...) if(_error_print_flag) { fprintf(stderr, "%s:%d:%s(): " fmt, __FILE__, __LINE__, __func__, __VA_ARGS__); }`
- `#define CIN_CONFIG_MAX_STRING 40`
- `#define CIN_CONFIG_MAX_TIMING_DATA 880`
- `#define CIN_CONFIG_MAX_TIMING_MODES 20`

Typedefs

- `typedef struct cin_ctl_listener cin_ctl_listener_t`
- `typedef struct cin_port cin_port_t`
- `typedef struct cin_config_timing cin_config_timing_t`
- `typedef struct cin_ctl cin_ctl_t`
- `typedef struct cin_data_frame cin_data_frame_t`
- `typedef struct cin_data_stats cin_data_stats_t`
- `typedef struct cin_data_threads cin_data_threads_t`
- `typedef struct cin_data_callbacks cin_data_callbacks_t`
- `typedef struct cin_data cin_data_t`
- `typedef void(* cin_data_callback) (cin_data_frame_t *, void *usr_ptr)`
- `typedef struct cin_ctl_id cin_ctl_id_t`
- `typedef struct cin_ctl_pwr_val cin_ctl_pwr_val_t`

Functions

- `void cin_set_debug_print (int debug)`
- `void cin_set_error_print (int error)`
- `void cin_report (FILE *fp, int details)`
- `int cin_ctl_init (cin_ctl_t *cin, char *addr, uint16_t port, uint16_t sport, char *bind_addr, uint16_t bind_port, uint16_t bind_sport)`
- `int cin_ctl_destroy (cin_ctl_t *cin)`
- `void cin_ctl_message (cin_ctl_t *cin, char *message, int severity)`
- `void cin_ctl_set_msg_callback (cin_ctl_t *cin, void *msg_callback, void *ptr)`

- int [cin_data_send_magic](#) (cin_data_t *cin)
- int [cin_ctl_read](#) (cin_ctl_t *cin, uint16_t reg, uint16_t *val, int wait)
- int [cin_ctl_write](#) (cin_ctl_t *cin, uint16_t reg, uint16_t val, int wait)
- int [cin_ctl_stream_write](#) (cin_ctl_t *cin, unsigned char *val, int size)
- int [cin_ctl_write_with_readback](#) (cin_ctl_t *cin, uint16_t reg, uint16_t val)
- int [cin_ctl_pwr](#) (cin_ctl_t *cin, int pwr)
- int [cin_ctl_fp_pwr](#) (cin_ctl_t *cin, int pwr)
- int [cin_ctl_fo_test_pattern](#) (cin_ctl_t *cin, int on_off)
- int [cin_ctl_load_config](#) (cin_ctl_t *cin, char *filename)
- int [cin_ctl_load_firmware](#) (cin_ctl_t *cin)
- int [cin_ctl_load_firmware_file](#) (cin_ctl_t *cin, char *filename)
- int [cin_ctl_load_firmware_data](#) (cin_ctl_t *cin, unsigned char *data, int data_len)
- int [cin_ctl_get_fclk](#) (cin_ctl_t *cin, int *clkfreq)
- int [cin_ctl_set_fclk](#) (cin_ctl_t *cin, int clkfreq)
- int [cin_ctl_get_cfg_fpga_status](#) (cin_ctl_t *cin, uint16_t * _val)
- int [cin_ctl_get_id](#) (cin_ctl_t *cin, cin_ctl_id_t * _val)
- int [cin_ctl_get_dcm_status](#) (cin_ctl_t *cin, uint16_t * _val)
- int [cin_ctl_get_power_status](#) (cin_ctl_t *cin, int full, int *pwr, cin_ctl_pwr_mon_t *values)
- int [cin_ctl_set_bias](#) (cin_ctl_t *cin, int val)
- int [cin_ctl_get_bias](#) (cin_ctl_t *cin, int *val)
- int [cin_ctl_set_bias_regs](#) (cin_ctl_t *cin, uint16_t *vals, int verify)
- int [cin_ctl_get_bias_regs](#) (cin_ctl_t *cin, uint16_t *vals)
- int [cin_ctl_set_bias_voltages](#) (cin_ctl_t *cin, float *voltage, int verify)
- int [cin_ctl_get_bias_voltages](#) (cin_ctl_t *cin, float *voltage, uint16_t *regs)
- int [cin_ctl_set_timing_regs](#) (cin_ctl_t *cin, uint16_t *vals, int vals_len)
- int [cin_ctl_get_timing_regs](#) (cin_ctl_t *cin, uint16_t *vals, int vals_len)
- int [cin_ctl_get_camera_pwr](#) (cin_ctl_t *cin, int *val)
- int [cin_ctl_set_camera_pwr](#) (cin_ctl_t *cin, int val)
- int [cin_ctl_set_clocks](#) (cin_ctl_t *cin, int val)
- int [cin_ctl_get_clocks](#) (cin_ctl_t *cin, int *val)
- int [cin_ctl_set_trigger](#) (cin_ctl_t *cin, int val)
- int [cin_ctl_get_trigger](#) (cin_ctl_t *cin, int *val)
- int [cin_ctl_set_focus](#) (cin_ctl_t *cin, int val)
- int [cin_ctl_get_focus](#) (cin_ctl_t *cin, int *val)
- int [cin_ctl_get_triggering](#) (cin_ctl_t *cin, int *trigger)
- int [cin_ctl_int_trigger_start](#) (cin_ctl_t *cin, int nimages)
- int [cin_ctl_int_trigger_stop](#) (cin_ctl_t *cin)
- int [cin_ctl_ext_trigger_start](#) (cin_ctl_t *cin, int trigger_mode)
- int [cin_ctl_ext_trigger_stop](#) (cin_ctl_t *cin)
- int [cin_ctl_set_exposure_time](#) (cin_ctl_t *cin, float e_time)
- int [cin_ctl_set_trigger_delay](#) (cin_ctl_t *cin, float t_time)
- int [cin_ctl_set_cycle_time](#) (cin_ctl_t *cin, float ftime)
- int [cin_ctl_frame_count_reset](#) (cin_ctl_t *cin)
- int [cin_ctl_set_mux](#) (cin_ctl_t *cin, int setting)
- int [cin_ctl_get_mux](#) (cin_ctl_t *cin, int *setting)
- int [cin_ctl_set_fcric_clamp](#) (cin_ctl_t *cin, int clamp)
- int [cin_ctl_set_fcric_gain](#) (cin_ctl_t *cin, int gain)
- int [cin_ctl_set_fcric_regs](#) (cin_ctl_t *cin, uint16_t *reg, int num_reg)
- int [cin_ctl_set_fcric](#) (cin_ctl_t *cin)
- int [cin_ctl_set_fabric_address](#) (cin_ctl_t *cin, char *ip)
- int [cin_ctl_bias_dump](#) (cin_ctl_t *cin, FILE *fp)
- int [cin_ctl_reg_dump](#) (cin_ctl_t *cin, FILE *fp)
- int [cin_config_read_file](#) (cin_ctl_t *cin, const char *file)

- int `cin_data_init` (`cin_data_t` *cin, char *addr, uint16_t port, char *bind_addr, uint16_t bind_port, int rcvbuf, int packet_buffer_len, int frame_buffer_len, cin_data_callback push_callback, cin_data_callback pop_callback, void *usr_ptr)
- void `cin_data_destroy` (`cin_data_t` *cin)
- void `cin_data_framestore_trigger` (`cin_data_t` *cin, int count)
- void `cin_data_framestore_skip` (`cin_data_t` *cin, int count)
- int `cin_data_get_framestore_counter` (`cin_data_t` *cin)
- void `cin_data_framestore_disable` (`cin_data_t` *cin)
- void `cin_data_framestore_trigger_enable` (`cin_data_t` *cin)
- struct `cin_data_frame` * `cin_data_get_next_frame` (`cin_data_t` *cin)
- void `cin_data_release_frame` (`cin_data_t` *cin, int free_mem)
- struct `cin_data_frame` * `cin_data_get_buffered_frame` (void)
- void `cin_data_release_buffered_frame` (void)
- void `cin_data_compute_stats` (`cin_data_t` *cin, `cin_data_stats_t` *stats)
- void `cin_data_show_stats` (FILE *fp, `cin_data_stats_t` stats)
- void `cin_data_reset_stats` (`cin_data_t` *cin)
- int `cin_data_set_descramble_params` (`cin_data_t` *cin, int rows, int overscan)
- void `cin_data_get_descramble_params` (`cin_data_t` *cin, int *rows, int *overscan, int *xsize, int *ysize)
- int `cin_com_boot` (`cin_ctl_t` *cin_ctl, `cin_data_t` *cin_data, char *mode)
- int `cin_ctl_upload_bias` (`cin_ctl_t` *cin)

Variables

- const char * `cin_build_git_time`
- const char * `cin_build_git_sha`
- const char * `cin_build_version`
- int `_debug_print_flag`
- int `_error_print_flag`

7.1.1 Detailed Description

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7.1.2 LICENSE

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7.1.3 DESCRIPTION

header file for CIN communications

7.1.4 Macro Definition Documentation

7.1.4.1 CIN_CONFIG_MAX_TIMING_DATA

```
#define CIN_CONFIG_MAX_TIMING_DATA 880
```

Max = 55 per state, 16 states

7.1.4.2 CIN_CONFIG_MAX_TIMING_MODES

```
#define CIN_CONFIG_MAX_TIMING_MODES 20
```

20 states max

7.1.4.3 CIN_CTL_BIAS_OFFSET

```
#define CIN_CTL_BIAS_OFFSET 0x0030
```

Offset in address to read bias

7.2 src/cin_register_map.h File Reference

Macros

- #define [REG_COMMAND](#) 0x0001
- #define **REG_READ_ADDRESS** 0x0002
- #define [REG_STREAM_TYPE](#) 0x0003
- #define **CMD_FCLK_125** 0xB000
- #define **CMD_FCLK_200** 0x7000
- #define [CMD_FCLK_250](#) 0x3000
- #define **REG_IF_MAC0** 0x0010
- #define **REG_IF_MAC1** 0x0011
- #define **REG_IF_MAC2** 0x0012
- #define **REG_IF_IP0** 0x0013
- #define **REG_IF_IP1** 0x0014
- #define **REG_IF_CMD_PORT_NUM** 0x001A
- #define **REG_IF_STREAM_IN_PORT_NUM** 0x001C
- #define **REG_IF_STREAM_OUT_PORT_NUM** 0x001D
- #define [REG_ETH_RESET](#) 0x0020
- #define [REG_ETH_ENABLE](#) 0x0021
- #define [REG_PHY1_MDIO_CMD](#) 0x0022

- #define **REG_PHY1_MDIO_CMD_DATA** 0x0023
- #define **REG_PHY1_MDIO_STATUS** 0x0024
- #define **REG_PHY1_MDIO_RD_ADDR** 0x0025
- #define **REG_PHY1_MDIO_RD_DATA** 0x0026
- #define **REG_MAC_CFG_VECTOR1** 0x0027
- #define **REG_PHY2_MDIO_CMD** 0x0028
- #define **REG_PHY2_MDIO_CMD_DATA** 0x0029
- #define **REG_PHY2_MDIO_STATUS** 0x002A
- #define **REG_PHY2_MDIO_RD_ADDR** 0x002B
- #define **REG_PHY2_MDIO_RD_DATA** 0x002C
- #define **REG_MAC_CFG_VECTOR2** 0x002D
- #define **CMD_PS_ENABLE** 0x0021
- #define **CMD_PS_POWERDOWN** 0x0022
- #define **REG_PS_ENABLE** 0x0030
- #define **REG_PS_SYNC_DIV0** 0x0031
- #define **REG_PS_SYNC_DIV1** 0x0032
- #define **REG_PS_SYNC_DIV2** 0x0033
- #define **REG_PS_SYNC_DIV3** 0x0034
- #define **REG_PS_SYNC_DIV4** 0x0035
- #define **CMD_PROGRAM_FRAME** 0x0041
- #define **REG_FRM_RESET** 0x0036
- #define **REG_FRM_10GbE_SEL** 0x0037;
- #define **CMD_ENABLE_CLKS** 0x0031
- #define **CMD_DISABLE_CLKS** 0x0032
- #define **REG_CLOCK_EN_REG** 0x0038
- #define **REG_SI570_REG0** 0x0039
- #define **REG_SI570_REG1** 0x003A
- #define **REG_SI570_REG2** 0x003B
- #define **REG_SI570_REG3** 0x003C
- #define **CMD_MON_STOP** 0x0011
- #define **CMD_MON_START** 0x0012
- #define **REG_VMON_ADC1_CH1** 0x0040 /* V12P_BUS Voltage Monitor */
- #define **REG_IMON_ADC1_CH0** 0x0041 /* V12P_BUS Current Monitor */
- #define **REG_VMON_ADC0_CH5** 0x0042 /* V3P3_MGMT Voltage Monitor */
- #define **REG_IMON_ADC0_CH5** 0x0043 /* V3P3_MGMT Current Monitor */
- #define **REG_VMON_ADC0_CH4** 0x0044 /* V3P3_S3E Voltage Monitor */
- #define **REG_IMON_ADC0_CH4** 0x0045 /* V3P3_S3E Current Monitor */
- #define **REG_VMON_ADC0_CH7** 0x0046 /* V2P5_MGMT Voltage Monitor */
- #define **REG_IMON_ADC0_CH7** 0x0047 /* V2P5_MGMT Current Monitor */
- #define **REG_VMON_ADC0_CH6** 0x0048 /* V1P8_MGMT Voltage Monitor */
- #define **REG_IMON_ADC0_CH6** 0x0049 /* V1P8_MGMT Current Monitor */
- #define **REG_VMON_ADC0_CH2** 0x004A /* V1P2_MGMT Voltage Monitor */
- #define **REG_IMON_ADC0_CH2** 0x004B /* V1P2_MGMT Current Monitor */
- #define **REG_VMON_ADC0_CH3** 0x004C /* V1P0_ENET Voltage Monitor */
- #define **REG_IMON_ADC0_CH3** 0x004D /* V1P0_ENET Current Monitor */
- #define **REG_VMON_ADC0_CH8** 0x004E /* V3P3_GEN Voltage Monitor */
- #define **REG_IMON_ADC0_CH8** 0x004F /* V3P3_GEN Current Monitor */
- #define **REG_VMON_ADC0_CH9** 0x0050 /* V2P5_GEN Voltage Monitor */
- #define **REG_IMON_ADC0_CH9** 0x0051 /* V2P5_GEN Current Monitor */
- #define **REG_VMON_ADC0_CHE** 0x0052 /* V0P9_V6 Voltage Monitor */
- #define **REG_IMON_ADC0_CHE** 0x0053 /* V0P9_V6 Current Monitor */
- #define **REG_VMON_ADC0_CHD** 0x0054 /* V2P5_V6 Voltage Monitor */
- #define **REG_IMON_ADC0_CHD** 0x0055 /* V2P5_V6 Current Monitor */
- #define **REG_VMON_ADC0_CHB** 0x0056 /* V1P0_V6 Voltage Monitor */
- #define **REG_IMON_ADC0_CHB** 0x0057 /* V1P0_V6 Current Monitor */

- #define **REG_VMON_ADC0_CHC** 0x0058 /* V1P2_V6 Voltage Monitor */
- #define **REG_IMON_ADC0_CHC** 0x0059 /* V1P2_V6 Current Monitor */
- #define **REG_VMON_ADC0_CHF** 0x005A /* V5P0_FP Voltage Monitor (1/2) */
- #define **REG_IMON_ADC0_CHF** 0x005B /* V5P0_FP Current Monitor (1/2) */
- #define **REG_DCM_STATUS** 0x0080
- #define **REG_FPGA_STATUS** 0x0081
- #define **REG_BOARD_ID** 0x008D
- #define **REG_HW_SERIAL_NUM** 0x008E
- #define **REG_FPGA_VERSION** 0x008F
- #define **REG_SANDBOX_REG00** 0x00F0
- #define **REG_SANDBOX_REG01** 0x00F1
- #define **REG_SANDBOX_REG02** 0x00F2
- #define **REG_SANDBOX_REG03** 0x00F3
- #define **REG_SANDBOX_REG04** 0x00F4
- #define **REG_SANDBOX_REG05** 0x00F5
- #define **REG_SANDBOX_REG06** 0x00F6
- #define **REG_SANDBOX_REG07** 0x00F7
- #define **REG_SANDBOX_REG08** 0x00F8
- #define **REG_SANDBOX_REG09** 0x00F9
- #define **REG_SANDBOX_REG0A** 0x00FA
- #define **REG_SANDBOX_REG0B** 0x00FB
- #define **REG_SANDBOX_REG0C** 0x00FC
- #define **REG_SANDBOX_REG0D** 0x00FD
- #define **REG_SANDBOX_REG0E** 0x00FE
- #define **REG_SANDBOX_REG0F** 0x00FF
- #define **REG_FRM_COMMAND** 0x8001
- #define **REG_FRM_READ_ADDRESS** 0x8002
- #define **REG_FRM_STREAM_TYPE** 0x8003
- #define **CMD_SEND_SYNC_PULSE** 0x0100
- #define **CMD_SYNC_DETECTOR2READOUT** 0x0101
- #define **CMD_WR_CCD_BIAS_REG** 0x0102
- #define **CMD_WR_CCD_CLOCK_REG** 0x0103
- #define **CMD_SEND_FCRIC_CONFIG** 0x0105
- #define **CMD_RESET_FRAME_COUNT** 0x0106
- #define **REG_IF_MAC_FAB1B0** 0x8010
- #define **REG_IF_MAC_FAB1B1** 0x8011
- #define **REG_IF_MAC_FAB1B2** 0x8012
- #define **REG_IF_IP_FAB1B0** 0x8013
- #define **REG_IF_IP_FAB1B1** 0x8014
- #define **REG_IF_CMD_PORT_NUM_FAB1B** 0x8015
- #define **REG_IF_STREAM_IN_PORT_NUM_FAB1B** 0x8016
- #define **REG_IF_STREAM_OUT_PORT_NUM_FAB1B** 0x8017
- #define **REG_XAUI_FAB1B** 0x8018
- #define **REG_MAC_CONFIG_VEC_FAB1B0** 0x8019
- #define **REG_MAC_CONFIG_VEC_FAB1B1** 0x801A
- #define **REG_MAC_STATS1_FAB1B0** 0x801B
- #define **REG_MAC_STATS1_FAB1B1** 0x801C
- #define **REG_MAC_STATS2_FAB1B0** 0x801D
- #define **REG_MAC_STATS2_FAB1B1** 0x801E
- #define **REG_IF_MAC_FAB2B0** 0x8020
- #define **REG_IF_MAC_FAB2B1** 0x8021
- #define **REG_IF_MAC_FAB2B2** 0x8022
- #define **REG_IF_IP_FAB2B0** 0x8023
- #define **REG_IF_IP_FAB2B1** 0x8024
- #define **REG_IF_CMD_PORT_NUM_FAB2B** 0x8025

- #define REG_IF_STREAM_IN_PORT_NUM_FAB2B 0x8026
- #define REG_IF_STREAM_OUT_PORT_NUM_FAB2B 0x8027
- #define REG_XAUI_FAB2B 0x8028
- #define REG_MAC_CONFIG_VEC_FAB2B0 0x8029
- #define REG_MAC_CONFIG_VEC_FAB2B1 0x802A
- #define REG_MAC_STATS1_FAB2B0 0x802B
- #define REG_MAC_STATS1_FAB2B1 0x802C
- #define REG_MAC_STATS2_FAB2B0 0x802D
- #define REG_MAC_STATS2_FAB2B1 0x802E
- #define REG_SRAM_COMMAND 0x8030
- #define REG_SRAM_START_ADDR1 0x8031
- #define REG_SRAM_START_ADDR0 0x8032
- #define REG_SRAM_STOP_ADDR1 0x8033
- #define REG_SRAM_STOP_ADDR0 0x8034
- #define REG_SRAM_FRAME_DATA_OUT1 0x8035
- #define REG_SRAM_FRAME_DATA_OUT0 0x8036
- #define REG_SRAM_FRAME_DATA_IN1 0x8037
- #define REG_SRAM_FRAME_DATA_IN0 0x8038
- #define REG_SRAM_FRAME_DV 0x8039
- #define REG_SRAM_STATUS1 0x803A
- #define REG_SRAM_STATUS0 0x803B
- #define CMD_FCLK_COMMIT 0x0012
- #define REG_FCLK_I2C_ADDRESS 0x8040
- #define REG_FCLK_I2C_DATA_WR 0x8041
- #define REG_FCLK_I2C_DATA_RD 0x8042
- #define REG_TRIGGERSELECT_REG 0x8050
- #define REG_TRIGGERMASK_REG 0x8051
- #define REG_CCDCLKSELECT_REG 0x8052
- #define REG_CDCLKDISABLE_REG 0x8053
- #define REG_FCLK_SET0 0xB007
- #define REG_FCLK_SET1 0xB008
- #define REG_FCLK_SET2 0xB009
- #define REG_FCLK_SET3 0xB00A
- #define REG_FCLK_SET4 0xB00B
- #define REG_FCLK_SET5 0xB00C
- #define REG_FRM_DCM_STATUS 0x8080
- #define REG_FRM_FPGA_STATUS 0x8081
- #define REG_FRM_BOARD_ID 0x808D
- #define REG_FRM_HW_SERIAL_NUM 0x808E
- #define REG_FRM_FPGA_VERSION 0x808F
- #define REG_FRM_SANDBOX_REG00 0x80F0
- #define REG_FRM_SANDBOX_REG01 0x80F1
- #define REG_FRM_SANDBOX_REG02 0x80F2
- #define REG_FRM_SANDBOX_REG03 0x80F3
- #define REG_FRM_SANDBOX_REG04 0x80F4
- #define REG_FRM_SANDBOX_REG05 0x80F5
- #define REG_FRM_SANDBOX_REG06 0x80F6
- #define REG_FRM_SANDBOX_REG07 0x80F7
- #define REG_FRM_SANDBOX_REG08 0x80F8
- #define REG_FRM_SANDBOX_REG09 0x80F9
- #define REG_FRM_SANDBOX_REG0A 0x80FA
- #define REG_FRM_SANDBOX_REG0B 0x80FB
- #define REG_FRM_SANDBOX_REG0C 0x80FC
- #define REG_FRM_SANDBOX_REG0D 0x80FD
- #define REG_FRM_SANDBOX_REG0E 0x80FE

- `#define REG_FRM_SANDBOX_REG0F 0x80FF`
- `#define REG_DETECTOR_REVISION_REG 0x8100`
- `#define REG_DETECTOR_CONFIG_REG1 0x8101`
- `#define REG_DETECTOR_CONFIG_REG2 0x8102`
- `#define REG_DETECTOR_CONFIG_REG3 0x8103`
- `#define REG_DETECTOR_CONFIG_REG4 0x8104`
- `#define REG_DETECTOR_CONFIG_REG5 0x8105`
- `#define REG_DETECTOR_CONFIG_REG6 0x8106`
- `#define REG_DETECTOR_CONFIG_REG7 0x8107`
- `#define REG_DETECTOR_CONFIG_REG8 0x8108`
- `#define REG_IMG_PROC_REVISION_REG 0x8120`
- `#define REG_IMG_PROC_CONFIG_REG1 0x8121`
- `#define REG_IMG_PROC_CONFIG_REG2 0x8122`
- `#define REG_IMG_PROC_CONFIG_REG3 0x8123`
- `#define REG_IMG_PROC_CONFIG_REG4 0x8124`
- `#define REG_IMG_PROC_CONFIG_REG5 0x8125`
- `#define REG_IMG_PROC_CONFIG_REG6 0x8126`
- `#define REG_IMG_PROC_CONFIG_REG7 0x8127`
- `#define REG_IMG_PROC_CONFIG_REG8 0x8128`
- `#define REG_BIASANDCLOCKREGISTERADDRESS 0x8200`
- `#define REG_BIASANDCLOCKREGISTERDATA 0x8201`
- `#define REG_CLOCKREGISTERDATAOUT 0x8202`
- `#define REG_BIASREGISTERDATAOUT 0x8203`
- `#define REG_BIASCONFIGREGISTER0_REG 0x8204`
- `#define REG_CLOCKCONFIGREGISTER0_REG 0x8205`
- `#define REG_BIASPARAM_READ_START 0x3000`
- `#define REG_EXPOSURETIMEMSB_REG 0x8206`
- `#define REG_EXPOSURETIMELSB_REG 0x8207`
- `#define REG_ALTEXPOSURETIMEMSB_REG 0x8306`
- `#define REG_ALTEXPOSURETIMELSB_REG 0x8307`
- `#define REG_TRIGGERREPETITIONTIMEMSB_REG 0x8208`
- `#define REG_TRIGGERREPETITIONTIMELSB_REG 0x8209`
- `#define REG_DELAYTOEXPOSUREMSB_REG 0x820A`
- `#define REG_DELAYTOEXPOSURELSB_REG 0x820B`
- `#define REG_NUMBEROFEXPOSURE_REG 0x820C`
- `#define REG_SHUTTERTIMEMSB_REG 0x820D`
- `#define REG_SHUTTERTIMELSB_REG 0x820E`
- `#define REG_DELAYTOSHUTTERMSB_REG 0x820F`
- `#define REG_DELAYTOSHUTTERLSB_REG 0x8210`
- `#define REG_FCRIC_MASK_REG1 0x8211`
- `#define REG_FCRIC_MASK_REG2 0x8212`
- `#define REG_FCRIC_MASK_REG3 0x8213`
- `#define REG_LVDS_OVERFLOW_ERROR_REG1 0x8214`
- `#define REG_LVDS_OVERFLOW_ERROR_REG2 0x8215`
- `#define REG_LVDS_OVERFLOW_ERROR_REG3 0x8216`
- `#define REG_LVDS_PARITY_ERROR_REG1 0x8217`
- `#define REG_LVDS_PARITY_ERROR_REG2 0x8218`
- `#define REG_LVDS_PARITY_ERROR_REG3 0x8219`
- `#define REG_LVDS_STOP_BIT_ERROR_REG1 0x821A`
- `#define REG_LVDS_STOP_BIT_ERROR_REG2 0x821B`
- `#define REG_LVDS_STOP_BIT_ERROR_REG3 0x821C`
- `#define REG_FCRIC_WRITE0_REG 0x821D`
- `#define REG_FCRIC_WRITE1_REG 0x821E`
- `#define REG_FCRIC_WRITE2_REG 0x821F`
- `#define REG_FCRIC_READ0_REG 0x8220`

- #define **REG_FCRIC_READ1_REG** 0x8221
- #define **REG_FCRIC_READ2_REG** 0x8222
- #define **REG_DEBUGVIDEO0_REG** 0x8223
- #define **REG_DEBUGVIDEO1_REG** 0x8224
- #define **REG_DEBUGVIDEO2_REG** 0x8225
- #define **REG_DEBUGVIDEO3_REG** 0x8226
- #define **REG_DEBUGVIDEO4_REG** 0x8227
- #define **REG_DEBUGVIDEO5_REG** 0x8228
- #define **REG_DEBUGVIDEO6_REG** 0x8229
- #define **REG_DEBUGVIDEO7_REG** 0x822A
- #define **REG_DEBUGVIDEO8_REG** 0x822B
- #define **REG_DEBUGVIDEO9_REG** 0x822C
- #define **REG_DEBUGVIDEO10_REG** 0x822D
- #define **REG_DEBUGVIDEO11_REG** 0x822E
- #define **REG_DEBUGCOUNTER00_REG** 0x822F
- #define **REG_DEBUGCOUNTER01_REG** 0x8230
- #define **REG_DEBUGCOUNTER02_REG** 0x8231
- #define **REG_DEBUGCOUNTER03_REG** 0x8232
- #define **REG_DEBUGCOUNTER04_REG** 0x8233
- #define **CMD_READ_REG** 0x0001

7.2.1 Detailed Description

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7.2.2 LICENSE

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7.2.3 DESCRIPTION

Control and Frame FPGA Register Map

7.2.4 TIMING

The exposure time is set through the REG_EXPOSURETIMEMSB_REG and REG_EXPOSURETIMELSB_REG registers. Their value in wall time depends on the fclk frequency. At 200 MHz fclk a register value of 0x00000001 corresponds to 20 us. At 125 MHz, a value of 0x00000001 corresponds to 32 us.

7.2.5 Macro Definition Documentation

7.2.5.1 CMD_DISABLE_CLKS

```
#define CMD_DISABLE_CLKS 0x0032
```

Disable Frame FPGA clock crystals

7.2.5.2 CMD_ENABLE_CLKS

```
#define CMD_ENABLE_CLKS 0x0031
```

Enable selected Frame FPGA clock crystals

7.2.5.3 CMD_FCLK_250

```
#define CMD_FCLK_250 0x3000
```

Ethernet Interface

7.2.5.4 CMD_FCLK_COMMIT

```
#define CMD_FCLK_COMMIT 0x0012
```

Start I2C Write/Read

7.2.5.5 CMD_MON_START

```
#define CMD_MON_START 0x0012
```

Start voltage and current monitor

7.2.5.6 CMD_MON_STOP

```
#define CMD_MON_STOP 0x0011
```

Stop voltage and current monitor

7.2.5.7 CMD_PS_ENABLE

```
#define CMD_PS_ENABLE 0x0021
```

Enable Selected Power Modules

7.2.5.8 CMD_PS_POWERDOWN

```
#define CMD_PS_POWERDOWN 0x0022
```

Start power down sequence

7.2.5.9 CMD_READ_REG

```
#define CMD_READ_REG 0x0001
```

Read Register CIN_REGISTER_MAP_H

7.2.5.10 CMD_RESET_FRAME_COUNT

```
#define CMD_RESET_FRAME_COUNT 0x0106
```

RESET STATISTICS/DEBUG COUNTERS Ethernet Interface

7.2.5.11 CMD_SEND_FCRIC_CONFIG

```
#define CMD_SEND_FCRIC_CONFIG 0x0105
```

SEND CONFIG DATA TO FRIC

7.2.5.12 CMD_SEND_SYNC_PULSE

```
#define CMD_SEND_SYNC_PULSE 0x0100
```

ISSUES A SYNC PULSE

7.2.5.13 CMD_SYNC_DETECTOR2READOUT

```
#define CMD_SYNC_DETECTOR2READOUT 0x0101
```

COMMAND TO SYNC DETECTOR AND READOUT (SEE IMAGE PROCESSING)

7.2.5.14 CMD_WR_CCD_BIAS_REG

```
#define CMD_WR_CCD_BIAS_REG 0x0102
```

WRITE CCD BIAS REGISTERS

7.2.5.15 CMD_WR_CCD_CLOCK_REG

```
#define CMD_WR_CCD_CLOCK_REG 0x0103
```

WRITE CCD CLOCK REGISTER

7.2.5.16 REG_BIASCONFIGREGISTER0_REG

```
#define REG_BIASCONFIGREGISTER0_REG 0x8204
```

Clock Static Registers

7.2.5.17 REG_BIASREGISTERDATAOUT

```
#define REG_BIASREGISTERDATAOUT 0x8203
```

Bias Static Registers

7.2.5.18 REG_CLOCK_EN_REG

```
#define REG_CLOCK_EN_REG 0x0038
```

Clock Enable Register Programmable Si570 Clock Registers

7.2.5.19 REG_CLOCKCONFIGREGISTER0_REG

```
#define REG_CLOCKCONFIGREGISTER0_REG 0x8205
```

Bias Voltage

7.2.5.20 REG_COMMAND

```
#define REG_COMMAND 0x0001
```

<Command Registers

7.2.5.21 REG_DEBUGCOUNTER04_REG

```
#define REG_DEBUGCOUNTER04_REG 0x8233
```

=====

CIN Commands

Common Commands

7.2.5.22 REG_DELAYTOSHUTTERLSB_REG

```
#define REG_DELAYTOSHUTTERLSB_REG 0x8210
```

Digitizer Registers

7.2.5.23 REG_ETH_ENABLE

```
#define REG_ETH_ENABLE 0x0021
```

Enable Eth Hardware 1=Rx, 2=Tx, 3=Both

7.2.5.24 REG_ETH_RESET

```
#define REG_ETH_RESET 0x0020
```

Reset Eth Hardware 1=Rx, 2=Tx, 3=Both

7.2.5.25 REG_EXPOSURETIMELSB_REG

```
#define REG_EXPOSURETIMELSB_REG 0x8207
```

Exposure time LSB

7.2.5.26 REG_EXPOSURETIMEMSB_REG

```
#define REG_EXPOSURETIMEMSB_REG 0x8206
```

Exposure time MSB

7.2.5.27 REG_FCLK_I2C_ADDRESS

```
#define REG_FCLK_I2C_ADDRESS 0x8040
```

[Slave Address(7), RD/WRn(1), Reg Address(8)] Slave address Hx58 -> HxB when shifted up by 1

7.2.5.28 REG_FCLK_I2C_DATA_RD

```
#define REG_FCLK_I2C_DATA_RD 0x8042
```

[Read Failed (1), Write Failed(1), Toggle bit(1), 0(5), Read Data (8)]

7.2.5.29 REG_FCLK_I2C_DATA_WR

```
#define REG_FCLK_I2C_DATA_WR 0x8041
```

[Clock Select(2), Clock Enable (1), 0(5), Write Data (8)] Clock Select: (00): 250 MHz (01): 200 MHz (10): FPGA FCRIC Clk (11): Si570 Programmable

7.2.5.30 REG_FCLK_SET5

```
#define REG_FCLK_SET5 0xB00C
```

FRM Status

7.2.5.31 REG_FPGA_VERSION

```
#define REG_FPGA_VERSION 0x008F
```

Sandbox Registers

7.2.5.32 REG_FRM_10GbE_SEL

```
#define REG_FRM_10GbE_SEL 0x0037;
```

10GbE Link Select Clock Enables

7.2.5.33 REG_FRM_FPGA_VERSION

```
#define REG_FRM_FPGA_VERSION 0x808F
```

Sandbox Registers

7.2.5.34 REG_FRM_RESET

```
#define REG_FRM_RESET 0x0036
```

Frame Reset

7.2.5.35 REG_FRM_SANDBOX_REG0F

```
#define REG_FRM_SANDBOX_REG0F 0x80FF
```

Image Processing Registers

7.2.5.36 REG_FRM_STREAM_TYPE

```
#define REG_FRM_STREAM_TYPE 0x8003
```

List of Commands

7.2.5.37 REG_IMON_ADC0_CHF

```
#define REG_IMON_ADC0_CHF 0x005B /* V5P0_FP Current Monitor (1/2) */
```

Status Registers

7.2.5.38 REG_MAC_CFG_VECTOR1

```
#define REG_MAC_CFG_VECTOR1 0x0027
```

Ethernet Hardware Conf

7.2.5.39 REG_MAC_CFG_VECTOR2

```
#define REG_MAC_CFG_VECTOR2 0x002D
```

Ethernet Hardware Conf Power Supply Control

7.2.5.40 REG_MAC_STATS2_FAB2B1

```
#define REG_MAC_STATS2_FAB2B1 0x802E
```

SRAM Test Interface

7.2.5.41 REG_PHY1_MDIO_CMD

```
#define REG_PHY1_MDIO_CMD 0x0022
```

Start(1), RnW(1), WDRd(1), PHY Addr(5), REG Addr(5)

7.2.5.42 REG_PS_ENABLE

```
#define REG_PS_ENABLE 0x0030
```

Power Supply Enable:

7.2.5.43 REG_PS_SYNC_DIV0

```
#define REG_PS_SYNC_DIV0 0x0031
```

2.5V Gen

7.2.5.44 REG_PS_SYNC_DIV1

```
#define REG_PS_SYNC_DIV1 0x0032
```

3.3V Gen

7.2.5.45 REG_PS_SYNC_DIV2

```
#define REG_PS_SYNC_DIV2 0x0033
```

2.5V Frame

7.2.5.46 REG_PS_SYNC_DIV3

```
#define REG_PS_SYNC_DIV3 0x0034
```

0.9V Frame

7.2.5.47 REG_PS_SYNC_DIV4

```
#define REG_PS_SYNC_DIV4 0x0035
```

5.0V FP Frame FPGA Control

7.2.5.48 REG_SANDBOX_REG0F

```
#define REG_SANDBOX_REG0F 0x00FF
```

-----< Frame FPGA Registers > Command Registers

7.2.5.49 REG_SI570_REG3

```
#define REG_SI570_REG3 0x003C
```

Power Monitor Registers

7.2.5.50 REG_SRAM_COMMAND

```
#define REG_SRAM_COMMAND 0x8030
```

1 bit [0] >> Read NOT Write 2 bits [3:2] >> Modes: – Single RW 0x00 – Burst RW 0x01 – Test/Diagnostic 10 – Sleep 11 1 bit [4] >> start/stop

7.2.5.51 REG_SRAM_STATUS0

```
#define REG_SRAM_STATUS0 0x803B
```

Programmable Clock

7.2.5.52 REG_STREAM_TYPE

```
#define REG_STREAM_TYPE 0x0003
```

FCLK Values

7.2.5.53 REG_TRIGGERMASK_REG

```
#define REG_TRIGGERMASK_REG 0x8051
```

[00]==SW Trigger, [01]==FP TrigIn2, [10]==FP TrigIn1, [11]==FP TrigIn1OR2

7.2.5.54 REG_TRIGGERREPETITIONTIMELSB_REG

```
#define REG_TRIGGERREPETITIONTIMELSB_REG 0x8209
```

Trigger Cycle Time LSB

7.2.5.55 REG_TRIGGERREPETITIONTIMESB_REG

```
#define REG_TRIGGERREPETITIONTIMESB_REG 0x8208
```

Trigger Cycle Time MSB

Index

- CIN COntrol Timing Routines, [19](#)
- CIN Control Bias Routines, [18](#)
- CIN Data Framestore Functions, [23](#)
 - [cin_data_framestore_disable](#), [23](#)
 - [cin_data_framestore_skip](#), [23](#)
 - [cin_data_framestore_trigger](#), [24](#)
 - [cin_data_framestore_trigger_enable](#), [24](#)
 - [cin_data_get_framestore_counter](#), [24](#)
- CIN Data Initialization Routines, [20](#)
 - [cin_data_destroy](#), [20](#)
 - [cin_data_init](#), [20](#)
- CIN FCLK Configuration Routines, [16](#)
- CIN Firmware Upload Routines, [15](#)
- CIN Status Routines, [17](#)
- CIN_CONFIG_MAX_TIMING_DATA
 - [cin.h](#), [41](#)
- CIN_CONFIG_MAX_TIMING_MODES
 - [cin.h](#), [41](#)
- CIN_CTL_BIAS_OFFSET
 - [cin.h](#), [41](#)
- CMD_DISABLE_CLKS
 - [cin_register_map.h](#), [47](#)
- CMD_ENABLE_CLKS
 - [cin_register_map.h](#), [47](#)
- CMD_FCLK_250
 - [cin_register_map.h](#), [47](#)
- CMD_FCLK_COMMIT
 - [cin_register_map.h](#), [47](#)
- CMD_MON_START
 - [cin_register_map.h](#), [47](#)
- CMD_MON_STOP
 - [cin_register_map.h](#), [47](#)
- CMD_PS_ENABLE
 - [cin_register_map.h](#), [48](#)
- CMD_PS_POWERDOWN
 - [cin_register_map.h](#), [48](#)
- CMD_READ_REG
 - [cin_register_map.h](#), [48](#)
- CMD_RESET_FRAME_COUNT
 - [cin_register_map.h](#), [48](#)
- CMD_SEND_FCRIC_CONFIG
 - [cin_register_map.h](#), [48](#)
- CMD_SEND_SYNC_PULSE
 - [cin_register_map.h](#), [48](#)
- CMD_SYNC_DETECTOR2READOUT
 - [cin_register_map.h](#), [48](#)
- CMD_WR_CCD_BIAS_REG
 - [cin_register_map.h](#), [48](#)
- CMD_WR_CCD_CLOCK_REG
 - [cin_register_map.h](#), [49](#)
- Cin Control Initialization Routines, [9](#)
 - [cin_ctl_destroy](#), [9](#)
 - [cin_ctl_init](#), [10](#)
 - [cin_data_send_magic](#), [10](#)
- Cin Control Read/Rwrite Routines, [12](#)
 - [cin_ctl_read](#), [12](#)
 - [cin_ctl_stream_write](#), [12](#)
 - [cin_ctl_write](#), [13](#)
 - [cin_ctl_write_with_readback](#), [13](#)
- [cin.h](#)
 - [CIN_CONFIG_MAX_TIMING_DATA](#), [41](#)
 - [CIN_CONFIG_MAX_TIMING_MODES](#), [41](#)
 - [CIN_CTL_BIAS_OFFSET](#), [41](#)
- [cin_config_timing](#), [27](#)
 - [cols](#), [27](#)
 - [data](#), [27](#)
 - [data_len](#), [27](#)
 - [fclk_freq](#), [27](#)
 - [framestore](#), [28](#)
 - [name](#), [28](#)
 - [overscan](#), [28](#)
 - [rows](#), [28](#)
- [cin_ctl](#), [28](#)
 - [fclk_time_factor](#), [29](#)
- [cin_ctl_destroy](#)
 - Cin Control Initialization Routines, [9](#)
- [cin_ctl_id](#), [29](#)
- [cin_ctl_init](#)
 - Cin Control Initialization Routines, [10](#)
- [cin_ctl_listener](#), [29](#)
- [cin_ctl_pwr_mon_t](#), [30](#)
- [cin_ctl_pwr_val](#), [30](#)
- [cin_ctl_read](#)
 - Cin Control Read/Rwrite Routines, [12](#)
- [cin_ctl_stream_write](#)
 - Cin Control Read/Rwrite Routines, [12](#)
- [cin_ctl_write](#)
 - Cin Control Read/Rwrite Routines, [13](#)
- [cin_ctl_write_with_readback](#)
 - Cin Control Read/Rwrite Routines, [13](#)
- [cin_data](#), [30](#)
- [cin_data_callbacks](#), [31](#)
- [cin_data_descramble_map_t](#), [31](#)
- [cin_data_destroy](#)
 - CIN Data Initialization Routines, [20](#)
- [cin_data_frame](#), [32](#)
- [cin_data_framestore_disable](#)
 - CIN Data Framestore Functions, [23](#)

- cin_data_framestore_skip
 - CIN Data Framestore Functions, [23](#)
- cin_data_framestore_trigger
 - CIN Data Framestore Functions, [24](#)
- cin_data_framestore_trigger_enable
 - CIN Data Framestore Functions, [24](#)
- cin_data_get_framestore_counter
 - CIN Data Framestore Functions, [24](#)
- cin_data_init
 - CIN Data Initialization Routines, [20](#)
- cin_data_packet, [32](#)
- cin_data_proc, [32](#)
- cin_data_send_magic
 - Cin Control Initialization Routines, [10](#)
- cin_data_stats, [33](#)
- cin_data_threads, [33](#)
- cin_map_t, [33](#)
- cin_port, [34](#)
- cin_register_map.h
 - CMD_DISABLE_CLKS, [47](#)
 - CMD_ENABLE_CLKS, [47](#)
 - CMD_FCLK_250, [47](#)
 - CMD_FCLK_COMMIT, [47](#)
 - CMD_MON_START, [47](#)
 - CMD_MON_STOP, [47](#)
 - CMD_PS_ENABLE, [48](#)
 - CMD_PS_POWERDOWN, [48](#)
 - CMD_READ_REG, [48](#)
 - CMD_RESET_FRAME_COUNT, [48](#)
 - CMD_SEND_FCRIC_CONFIG, [48](#)
 - CMD_SEND_SYNC_PULSE, [48](#)
 - CMD_SYNC_DETECTOR2READOUT, [48](#)
 - CMD_WR_CCD_BIAS_REG, [48](#)
 - CMD_WR_CCD_CLOCK_REG, [49](#)
 - REG_BIASCONFIGREGISTER0_REG, [49](#)
 - REG_BIASREGISTERDATAOUT, [49](#)
 - REG_CLOCK_EN_REG, [49](#)
 - REG_CLOCKCONFIGREGISTER0_REG, [49](#)
 - REG_COMMAND, [49](#)
 - REG_DEBUGCOUNTER04_REG, [49](#)
 - REG_DELAYTOSHUTTERLSB_REG, [50](#)
 - REG_ETH_ENABLE, [50](#)
 - REG_ETH_RESET, [50](#)
 - REG_EXPOSURETIMELSB_REG, [50](#)
 - REG_EXPOSURETIMEMSB_REG, [50](#)
 - REG_FCLK_I2C_ADDRESS, [50](#)
 - REG_FCLK_I2C_DATA_RD, [50](#)
 - REG_FCLK_I2C_DATA_WR, [50](#)
 - REG_FCLK_SET5, [51](#)
 - REG_FPGA_VERSION, [51](#)
 - REG_FRM_10GbE_SEL, [51](#)
 - REG_FRM_FPGA_VERSION, [51](#)
 - REG_FRM_RESET, [51](#)
 - REG_FRM_SANDBOX_REG0F, [51](#)
 - REG_FRM_STREAM_TYPE, [51](#)
 - REG_IMON_ADC0_CHF, [52](#)
 - REG_MAC_CFG_VECTOR1, [52](#)
 - REG_MAC_CFG_VECTOR2, [52](#)
 - REG_MAC_STATS2_FAB2B1, [52](#)
 - REG_PHY1_MDIO_CMD, [52](#)
 - REG_PS_ENABLE, [52](#)
 - REG_PS_SYNC_DIV0, [52](#)
 - REG_PS_SYNC_DIV1, [52](#)
 - REG_PS_SYNC_DIV2, [53](#)
 - REG_PS_SYNC_DIV3, [53](#)
 - REG_PS_SYNC_DIV4, [53](#)
 - REG_SANDBOX_REG0F, [53](#)
 - REG_SI570_REG3, [53](#)
 - REG_SRAM_COMMAND, [53](#)
 - REG_SRAM_STATUS0, [53](#)
 - REG_STREAM_TYPE, [54](#)
 - REG_TRIGGERMASK_REG, [54](#)
 - REG_TRIGGERREPETITIONTIMELSB_REG, [54](#)
 - REG_TRIGGERREPETITIONTIMEMSB_REG, [54](#)
- cols
 - cin_config_timing, [27](#)
- data
 - cin_config_timing, [27](#)
- data_len
 - cin_config_timing, [27](#)
- fclk_freq
 - cin_config_timing, [27](#)
- fclk_time_factor
 - cin_ctl, [29](#)
- fifo, [34](#)
- framestore
 - cin_config_timing, [28](#)
- name
 - cin_config_timing, [28](#)
- overscan
 - cin_config_timing, [28](#)
- REG_BIASCONFIGREGISTER0_REG
 - cin_register_map.h, [49](#)
- REG_BIASREGISTERDATAOUT
 - cin_register_map.h, [49](#)
- REG_CLOCK_EN_REG
 - cin_register_map.h, [49](#)
- REG_CLOCKCONFIGREGISTER0_REG
 - cin_register_map.h, [49](#)
- REG_COMMAND
 - cin_register_map.h, [49](#)
- REG_DEBUGCOUNTER04_REG
 - cin_register_map.h, [49](#)
- REG_DELAYTOSHUTTERLSB_REG
 - cin_register_map.h, [50](#)
- REG_ETH_ENABLE
 - cin_register_map.h, [50](#)
- REG_ETH_RESET
 - cin_register_map.h, [50](#)
- REG_EXPOSURETIMELSB_REG
 - cin_register_map.h, [50](#)
- REG_EXPOSURETIMEMSB_REG

cin_register_map.h, [50](#)
REG_FCLK_I2C_ADDRESS
 cin_register_map.h, [50](#)
REG_FCLK_I2C_DATA_RD
 cin_register_map.h, [50](#)
REG_FCLK_I2C_DATA_WR
 cin_register_map.h, [50](#)
REG_FCLK_SET5
 cin_register_map.h, [51](#)
REG_FPGA_VERSION
 cin_register_map.h, [51](#)
REG_FRM_10GbE_SEL
 cin_register_map.h, [51](#)
REG_FRM_FPGA_VERSION
 cin_register_map.h, [51](#)
REG_FRM_RESET
 cin_register_map.h, [51](#)
REG_FRM_SANDBOX_REG0F
 cin_register_map.h, [51](#)
REG_FRM_STREAM_TYPE
 cin_register_map.h, [51](#)
REG_IMON_ADC0_CHF
 cin_register_map.h, [52](#)
REG_MAC_CFG_VECTOR1
 cin_register_map.h, [52](#)
REG_MAC_CFG_VECTOR2
 cin_register_map.h, [52](#)
REG_MAC_STATS2_FAB2B1
 cin_register_map.h, [52](#)
REG_PHY1_MDIO_CMD
 cin_register_map.h, [52](#)
REG_PS_ENABLE
 cin_register_map.h, [52](#)
REG_PS_SYNC_DIV0
 cin_register_map.h, [52](#)
REG_PS_SYNC_DIV1
 cin_register_map.h, [52](#)
REG_PS_SYNC_DIV2
 cin_register_map.h, [53](#)
REG_PS_SYNC_DIV3
 cin_register_map.h, [53](#)
REG_PS_SYNC_DIV4
 cin_register_map.h, [53](#)
REG_SANDBOX_REG0F
 cin_register_map.h, [53](#)
REG_SI570_REG3
 cin_register_map.h, [53](#)
REG_SRAM_COMMAND
 cin_register_map.h, [53](#)
REG_SRAM_STATUS0
 cin_register_map.h, [53](#)
REG_STREAM_TYPE
 cin_register_map.h, [54](#)
REG_TRIGGERMASK_REG
 cin_register_map.h, [54](#)
REG_TRIGGERREPETITIONTIMELSB_REG
 cin_register_map.h, [54](#)
REG_TRIGGERREPETITIONTIMEMSB_REG
 cin_register_map.h, [54](#)
rows
 cin_config_timing, [28](#)

src/cin.h, [35](#)
src/cin_register_map.h, [41](#)