Numerical Characterization of the Stress Induced Voiding Inside Via of Various Cu/Low k Interconnects

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Abstract

Modeling methodologies including a dynamic stress evolution are proposed in this work to characterize the relative stress-induced voiding (SIV) probability inside via of various Cu/Low k interconnects. Seven patterns being representative of versatile IC design units are selected. It is demonstrated that our modeling approach can serve as a good method identifying the most troublesome layout units to inside-via SIV, and the results aligned well with the experimental data. From our studies, two kinds of layout styles when designed together are found detrimental: (1) the layout units with via(s) subjected to significant upper-metal edge confinement and (2) the one with via close to big vacancy sources.

Keywords: Stress-induced voiding, SIV

Introduction

The reliability concerns associated with the stress induced voiding (SIV) phenomena are becoming important engineering tasks as the interconnect dimension shrinks and the material system advances to Cu/Low k. In general, there are two kinds of voiding sites (1): one is commonly found upon via bottom and another is inside the linking vias. To set-up robust circuit design rules avoiding SIV occurrence, numerical simulation using the finite element method serves as an effective and economic tool for the extraction of SIV circuit pattern dependency and the invention of SIV resistant layout designs in addition to the costly experimental approach. A numerical index including vacancy evolution had been proposed (2) to assess the former via-bottom voiding behavior of various interconnects. This article will present the modeling results of the latter SIV mode, namely the voiding inside the linking vias [Fig. 1] of Cu/Low k interconnects. Various simple geometries that can be treated as the fundamental building blocks of the diverse circuit designs are studied [Fig. 2]. The vacancy clustering and the void nucleation tendency inside via of various Cu/Low k interconnects will be discussed. Moreover, the relative failure probability due to stress-induced voiding inside the linking vias is also presented.

Experimental

Two levels of Cu/Low k interconnects plus one top metal layer and one passivation layer were fabricated. Single damascene wafer processing was applied to the bottom metal layer and dual-damascene techniques to the upper metal layers and the linking vias. After the multi-level processes and the passivation, the processed wafers were subjected to an unbiased thermal-stressing environment for a continuous time period. The testing circuit resistance was measured and recorded before and after the thermal stressing. The resistance shift of all samples was then analyzed to obtain their statistic significance.

Numerical Simulations

Test structures

A few of the most representative geometries that can be treated as the fundamental building blocks of the diverse circuit designs were selected and numerically simulated to characterize their SIV performance. Schematics of these unit patterns are illustrated in Fig. 2(A) ~ Fig. 2(G). One quarter or one-half of the symmetrical 3D-modeling domains were constructed for each of the studied unit pattern geometry. The finite element simulations were carried out using the commercial package ANSYS to obtain their stress profiles for further analysis. The initial stress free temperature and the final thermal stressing temperature were specified at 275℃ and 175℃, respectively.

Modeling Methodology

It is important to elucidate the mechanism of SIV phenomena inside vias in order to model it correctly. In addition to the significance of the thermo mechanical via pulling stress (σ_z), experimental work had been carried out to assess the applicability of diffusion mechanism which asserts the saturated vacancies are driven by the stress gradient($\Delta\sigma_h$) and migrate towards the low stress regions just like those causing via-bottom voiding, yet through diffusion pathways with much higher activation energy. Our silicon data [Fig.3] show the test circuit failure rate is stressing temperature dependent, which implies (3) the vacancy diffusion mechanism can't be ignored modeling SIV inside vias.

1. Vacancy clustering tendency on regions atop via – Modeling efforts are made to characterize the evolved vacancy clustering intensity on top of the linking via for the interested geometries as they affect the following void nucleation inside the via. The numerical index (2) previously proposed, being influenced by the local geometry-dependent stress field and the via-site-dependent vacancy source (upper metal area), is adopted to emulate the vacancy concentration evolution towards a predefined control volume atop via. [Fig. 4] In addition, since a relaxed stress field resulted from the vacancy migration alleviates the vacancy migrating intensity and their clustering tendency, the physics of stress evolution is also considered to avoid the over-estimated and/or even erroneous tendency prediction.

2. Relative void nucleation tendency inside the vias – SIV phenomena usually begin with the micro-void nucleation, which then creates a zone with local minimum stress soliciting the vacancies. To characterize the relative nucleation tendency among the modeled geometries, an index I_{VN} is defined (Eqn. (1)) and the geometry of Fig. 2(A) is adopted as a reference. It is noted that, in Eqn (1), R_{SV} stands for the SIV probability of the creep model (3), C_v is the clustered vacancy concentration, Ω the atomic volume, k the Boltzmann's constant, T_s the thermal stressing temperature and $\Delta\sigma_h$ the hydrostatic stress gradient. The superscript "ref " stands for those physical properties of the benchmark geometry.

$$I_{VN} = \frac{R_{SV}}{R_{SV}^{ref}} = \frac{C_V}{C_V^{ref}} \left[\frac{\Delta\sigma_h}{\Delta\sigma_h^{ref}} \right]^n \exp\left[\frac{\Omega}{kT_s} \left(\sigma_Z - \sigma_Z^{ref} \right) \right] \qquad (1)$$

3. Relative failure probability – In order to extract the pattern dependent vulnerability to SIV inside vias an empirical relation is proposed. (Eqn (2)) It correlates their relative failure probability with the dominant thermo mechanical pulling stress component (σ_z) inside via, the

voiding nucleation tendency (I_{vn}) and the effective modulus B of via (4). It is noted that the effective modulus of vias is about the same for the same material system regardless of their locations. Therefore, another index I_{FP} is introduced as shown in Eqn (3) to assess the relative vulnerability of various patterns to the stress induced voiding inside via.

$$TTF_{SIV} \approx \frac{B}{\sigma_z R_{SV}} \quad (2)$$

$$I_{FP} = \frac{TTF_{SIV}}{TTF_{SIV}^{ref}} \approx \frac{\sigma_z^{ref} R_{SV}^{ref}}{\sigma_z R_{SV}} \quad (3)$$

Results and Discussion

Figure 5A shows the index reflecting the vacancy evolution of various interested geometries with and without the stress relaxation. (2) The evolution of vacancy also induces the stress relaxation (5), thus the stress profile evolves so is the vacancy migration intensity. Figure 5B illustrates the stress contours before and after the stress evolution. Figure 6 shows the hydrostatic stress profiles of the interested via area of various geometries where the via locations and the corresponding stress environments vary. Figure 7 shows the dominant stress component inside via (σ_z) of various patterns. It is interesting to note that due to Poisson effects the trench metal (atop the via) would relax the thermal stresses yet the regions near the confined metal edge are less likely to deform, thus resulting in higher thermal mismatch stress. Therefore, as more edge confinement near the metal area atop the interested via, higher stress component will be resulted. For example, A > C > B and E > D. Figure 8 indicates the assessments of the relative void nucleation tendency among these structures considering both the stress component and the hydrostatic stresses. Patterns E and F, are both in a group showing the highest potential to suffer from the void nucleation inside the vias. Figure 9 shows the relative failure probability due to SIV inside vias where pattern E and F are in the high-risk group and pattern F is shown to be the most vulnerable layout design unit to SIV inside vias. It is noted that some similarities are identified for these two structures. For both patterns, large vacancy source (metal area) atop the via are found and the edge confinement effect is also significant so as to yield higher thermal stresses distribution (higher vacancy driving force and the via pulling stress) in the regions near via. Whereas only one of these two conditions is found for the rest of patterns. Figure 10 illustrates the silicon data of one of our earlier version Cu/Low k process flows, in which the testing circuits possess various Fig. 2F like unit patterns. It is found that the geometrical dimension affects the results significantly and the various resulting stress fields are crucial. For example, as the dimension B and W become shorter (closer to the large vacancy source and stronger edge confinement) the higher the failure rates. Figure 11 illustrates the similar results where there are two linking vias and this design trick improves the SIV probability inside vias. Although inside-via SIV phenomena had been nicely resolved with our later process optimization, high-risk layouts should still be smartly avoided to guarantee a robust product reliability.

Conclusions

Numerical methodologies including a dynamic stress evolution are presented in this work to characterize the vacancy clustering and the relative void nucleation tendency inside vias of various unit patterns commonly seen in versatile IC layouts. They are both associated with another numerical index aiming at predicting the relative failure probability due to inside-via SIV. It is found that the most detrimental unit designs as far as the inside-via-SIV is concerned are those having both the large vacancy source (metal area) and significant edge confinement effect atop the via. In addition, design of dual vias improves the vulnerability of SIV inside the linking vias.

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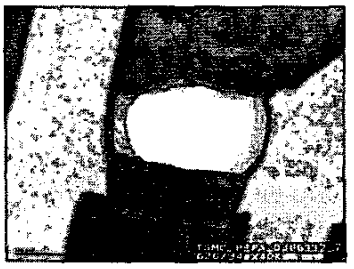

Fig. 1 TEM picture of a typical vacancy accumulation site inside the via

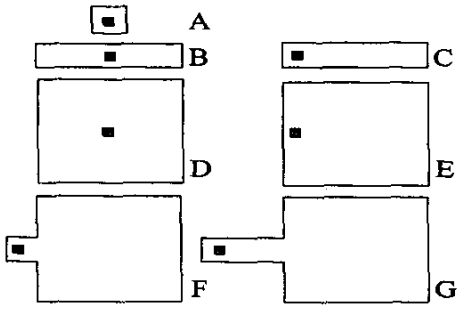

Fig. 2 Studied pattern units. (A) V1 lies below the center of a (1 x 1) M2 (B) V1 lies below the center of a (1 x 20) M2 (C) V1 lies below the edge of a (1 x 20) M2 (D) V1 lies below the center of a (20 x20) M2 (E) V1 lies below the edge of a (20 x 20) M2 (F) V1 lies below the edge of a (1 x 1) M2 that extended from a (20 x 20) M2 (G) V1 lies below the edge of a (1 x 20) M2 that extended from a (20 x 20) M2. All V1s link to a (1 x 1) M1. Unit: um

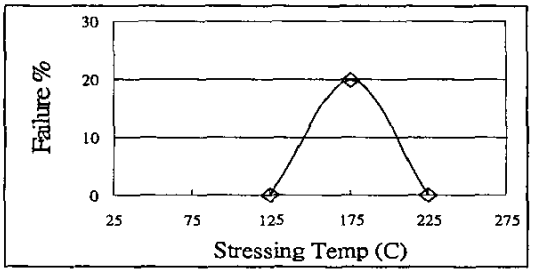

Fig. 3 Failure percentage of the patterns having Fig. 2(F) like unit patterns with M2 atop a single linking via using 65-nm processing technology, after 168 hours of thermal stressing; Rc shift over 20% is considered failure

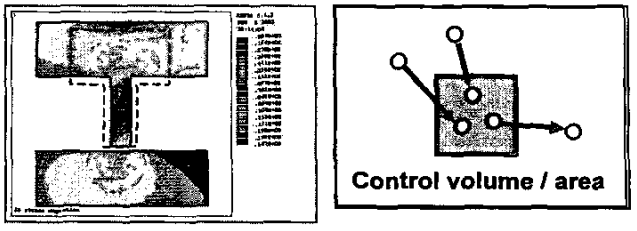

Fig. 4 The control volume atop/of via of each modeled geometry inside which the vacancy concentration evolution is monitored

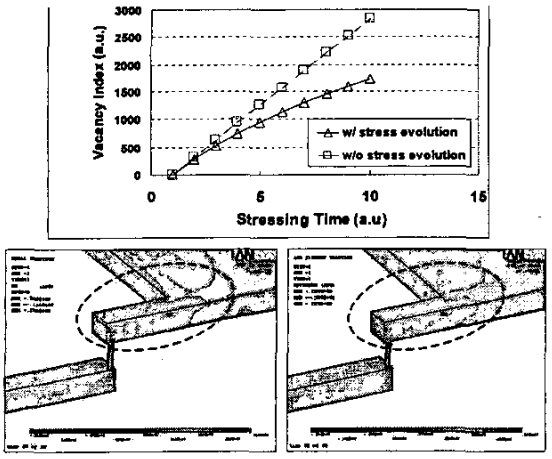

Fig. 5 A: Index reflecting the vacancy concentration evolution within the control volume atop interested via (or the vacancy clustering tendency), B: The exemplary evolved stress contours; left: without stress evolution, right: with stress evolution

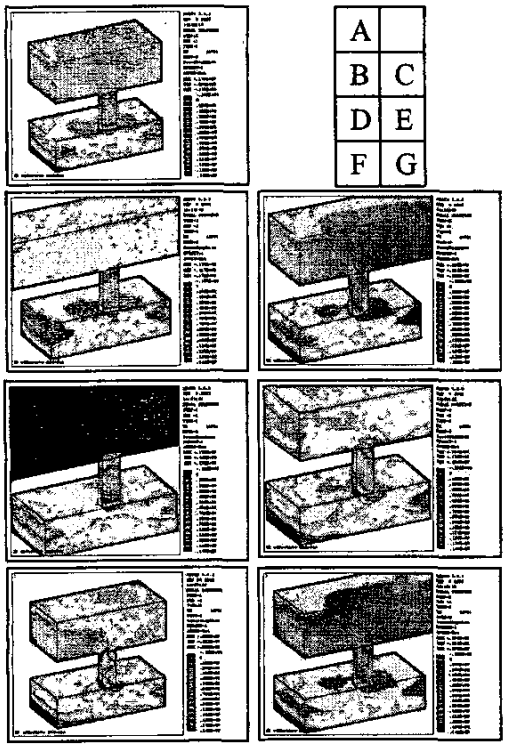

Fig. 6 Hydrostatic stress profile of the various modeled geometries

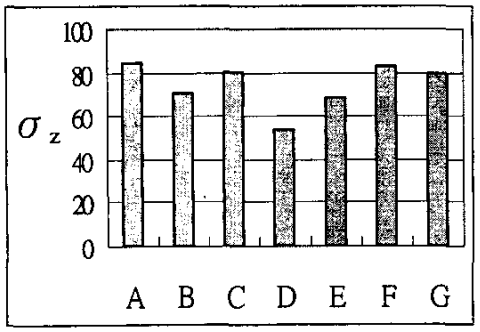

Fig. 7 Thermo mechanical via pulling stress (MPa) of various geometries

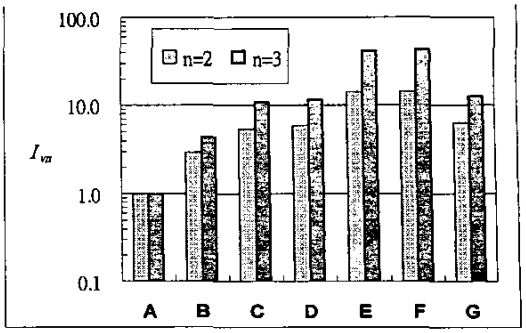

Fig. 8 Index I_{VN} reflecting the relative void nucleation tendency inside vias of various modeled pattern geometries

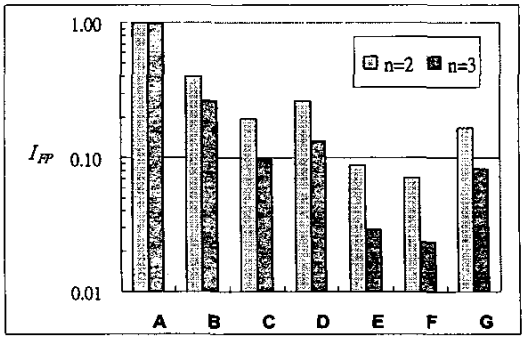

Fig. 9 Index I_{FP} reflecting the relative failure probability due to SIV inside vias of various modeled pattern geometries

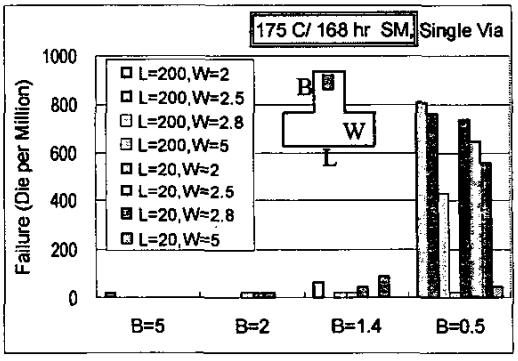

Fig. 10 Failure rate of the test circuits having Fig. 2(F) like unit patterns with one linking via after 168 hours of thermal stressing; Rc shift over 100% is considered failure

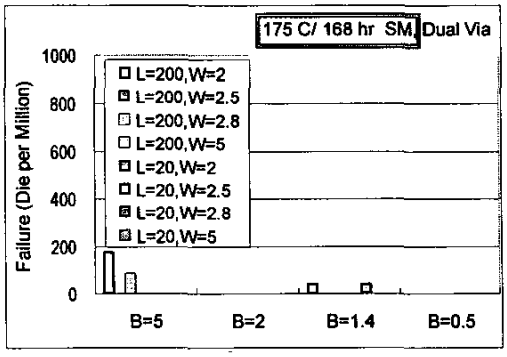

Fig. 11 Failure rate of the test circuits having Fig. 2(F) like unit patterns with two linking via after 168 hours of thermal stressing; Rc shift over 100% is considered failure