A High Order Multi-Bit ΣΔ Modulator for Multi-Standard Wireless Receiver

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Abstract—**The next generation of cellular systems will be increasingly similar to a data communication system. Not only will it transfer voice and multimedia data, it will also be integrated with WLAN to access Internet whenever possible. Thus these cellular systems need highly integrated multi-standard receivers. The design of the A/D converter in such receivers is a big challenge. A reconfigurable ΣΔ modulator which is suitable for GSM/WCDMA/WLAN standards, is introduced in this paper. According to the different signal bandwidth and Dynamic Range (DR) specifications, this ΣΔ modulator is reconfigured to achieve the required dynamic range with less power consumption. The prototype is implemented in TSMC 0.18μm CMOS process with 1.8V power supply.**

I. Introduction

Cellular systems are now moving from 2G to 3G. While a 2G cellular system focuses on voice transmission, 3G brings high-speed data transmission which enables wideband multimedia applications. 4G mobile systems will be further integrated with Wireless Local Area Networks (WLAN). A user will employ the WLAN mode whenever the mobile terminal is within range of a WLAN access point [1]. WLAN-enabled cell phones are expected to contain multimode cellular capability. A suggestion is to encompass GSM and WCDMA operation, in addition to WLAN [2]. WCDMA will take care of wide-area medium-speed data connections, while GSM will provide speech and lower-rate data in remote areas. The addition of WLAN compatibility will add high-speed data connections to the mix.

Fig. 1 depicts the multi-standard receiver architecture proposed by the Analog VLSI Lab. of the Ohio State University. A switch selects between the three receive modes and the transmit mode. A low-IF (100 kHz) architecture has been used for GSM to reduce the DC offset problem and relax the image rejection requirement while a zero-IF architecture has been used for the other two standards. Three RF filters have been used to select appropriate signal bands. Due to the proximity of WCDMA and WLAN bands, LNA and mixer have been shared between them but a second LNA and mixer is necessary for GSM operation. However, when one set of LNA and mixer is operational, the other set is powered down to reduce power consumption. Baseband components in the I and Q paths include a DC-notch filter, poly-phase filter, VGA and ADC and these are shared among the three standards. The receiver was designed using MS Excel® and a transient analysis of the receiver was performed using Simulink® to gain a better insight into the design trade-offs.

To cover multiple cellular and WLAN standards is a challenge, since the bandwidth and resolution requirements are widely spread in those standards. The ADC in the receiver path is a bottleneck in such a system. Table I summarizes the channel bandwidth and dynamic range requirements of the baseband

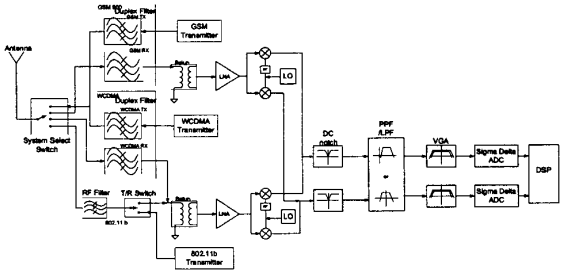

Fig. 1. Triple standard receiver architecture

TABLE I
ADC DR REQUIREMENTS OBTAINED FROM THE MULTI-STANDARD RECEIVER MODEL SIMULATIONS

Wireless Standards	Frequency (MHz)	Channel Bandwidth	Dynamic Range
GSM	890-915 (Tx) 935-960 (Rx)	200 kHz	80 dB
WCDMA	1850-1910 (Tx) 1920-1980 (Rx)	5 MHz	60 dB
WLAN	2401-2473	20 MHz	50 dB

ADC for the three standards, obtained from the Simulink® model of the receiver. ΣΔ ADC is an attractive choice for a multi-standard solution, since data rate is naturally traded for resolution in such an ADC.

This paper describes a switched-capacitor (SC) ΣΔ modulator operating from 1.8V supply and implemented in TSMC 0.18μm CMOS technology. It achieves SNDR of 83 dB for GSM mode, 73 dB for WCDMA and 58 dB for WLAN. It can also be used for some other standards (e.g. Bluetooth) without any modification.

The paper is organized as follows. The architecture of this multi-standard ΣΔ modulator is first explained followed by a description of the important building blocks. The simulation results and discussion are then provided and the important results are summarized in the conclusion section.

II. ΣΔ Modulator Architecture

Theoretical DR of a ΣΔ modulator is the maximum signal to quantization noise ratio (i.e. peak SNR_Q). As shown in (1), there is a trade-off between the order L, the oversampling ratio M and the number of bits B in the quantizer. For signals of very wide bandwidth, such as in WLAN receiver, oversampling ratio might only be 4 or 5 because the achievable clock frequency is constrained by the process technology. As a result, higher order and/or multi-bit quantizer have to be employed to get the

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TABLE II
COMPARISON OF ΣΔ MODULATOR ARCHITECTURES

Wireless Standards	Order L	OSR M	F_{clk} (MHz)	bits B	SNR_Q (dB)
GSM	2	64	25.6	1	79
	2	**128**	**51.2**	**1**	**94**
	3	64	25.6	1	107
WCDMA	3	16	80	2	74
	4	**20**	**100**	**1**	**88**
	5	16	80	1	95
WLAN	4	5	100	4	58
	5	4	80	4	52
	5	**5**	**100**	**3**	**56**

required resolution. For the lower data rate application, such as GSM receiver, M can be easily made more than 100 due to much smaller signal bandwidth. Thus 2^{nd} order and single bit quantizer is usually enough for this kind of application.

$$Peak\ SNR_Q = \frac{3}{2} \cdot \frac{2L+1}{\pi^{2L}} \cdot M^{2L+1} \cdot (2^B - 1)^2 \quad (1)$$

Table II compares peak SNR_Q of the three standards for different values of L, M and B. Due to stability issues of high order single loop ΣΔ modulators and loading effects and nonlinearity problems of multi-bit quantizers, a MASH topology with smaller number of bits in the quantizer is preferred. Thus the configuration of the ΣΔ modulator, which is in bold in Table II, is found to be the most suitable.

Due to scaling effects and non-linearities of the building blocks, around 10 dB drop from the theoretical DR is expected upon implementation. As the theoretical DR (shown in Table II) is more than 10 dB higher than the specifications for GSM and WCDMA, this drop causes no problem in these two modes. However, it could be of concern in WLAN application. In order to further increase SNR_Q for WLAN mode, the quantization noise power in the signal bandwidth has to be reduced. This can be done by adjusting the zeros of Noise Transfer Function (NTF). Usually all zeros of NTF are placed at DC. If some of these zeros are placed inside the signal bandwidth but at higher frequencies from DC, it will help to minimize the quantization noise power in the useful bandwidth [3][4].

Taking into account the above considerations, a cascade 2-1-1-1 structure with multi-bit quantizer is proposed. The topology of this multi-standard ΣΔ modulator is shown in Fig. 2. The first stage is a second order, single bit ΣΔ modulator. Since the GSM mode needs only 2^{nd} order and single bit ΣΔ modulator, only the first stage is powered on to do the A/D conversion. All the other stages are turned off to save power. Latter stages are all first order ΣΔ modulators for easier configuration as third, fourth or fifth order ΣΔ modulators. For a medium-speed data transmission, like for a Bluetooth signal which has 1 MHz channel bandwidth, 3^{rd} order ΣΔ ADC is enough. For a higher speed data transmission, such as in WCDMA, the first 3 stages (i.e. 4^{th} order) are employed to get more than 60 dB SNDR. As discussed above, in WLAN mode, careful placement of the zeros of NTF so as to further suppress the quantization noise power is a must. This is realized by adding a feedback path from the last stage to the third stage as shown in Fig. 2. In addition, a 9 level quantizer is used in the last stage and a 3 level (1.5 bits) quantizer is employed in the second last

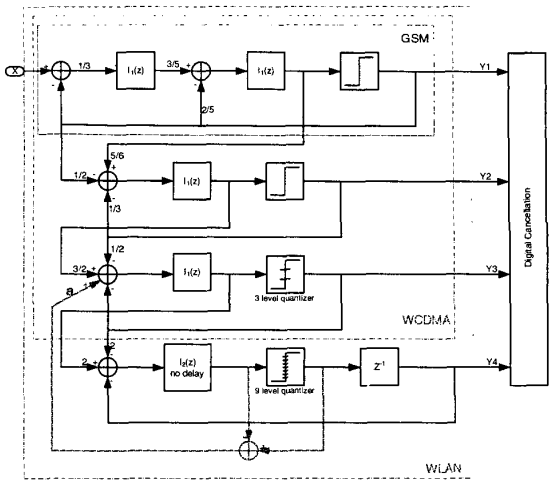

Fig. 2. Triple standard receiver architecture

stage to make sure the total quantization noise power is small enough.

Transfer functions for the last 2 stages are as follows

$$Y_3(z) = z^{-1}X_3(z) + (1-z^{-1})Q_3(z) + az^{-1}Q_4(z) \quad (2)$$
$$Y_4(z) = -2z^{-1} \cdot Q_3(z) + z^{-1}(1-z^{-1}) \cdot Q_4(z) \quad (3)$$

where Q_3 and Q_4 are the quantization errors of the 3^{rd} stage and 4^{th} stage respectively, X_3 is the input to the 3rd stage, 'a' is the feedback factor from the last stage to the 2^{nd} last stage. Thus NTF of the last two stages is

$$z^{-1}[1 - 2(1-a)z^{-1} + z^{-2}] \quad (4)$$

Combined with the first 2 stages, the total NTF of the system is

$$z^{-1}[1 - 2(1-a)z^{-1} + z^{-2}](1-z^{-1})^3 \quad (5)$$

Feedback factor 'a' is used to adjust the zeros in this NTF. Minimization of the noise power inside the signal bandwidth becomes an optimization problem formulated as follows

$$min\ G = \int_0^{\frac{\pi}{M}} \left|(1-e^{-j\Omega})^3 \cdot [1-2(1-a)e^{-j\Omega} + e^{-j2\Omega}]\right|^2 d\Omega \quad (6)$$

The optimal value of 'a' is then determined by

$$1-a = \frac{\frac{-15\pi}{8M} + \frac{13}{4}sin\left(\frac{\pi}{M}\right) - sin\left(\frac{2\pi}{M}\right) + \frac{1}{4}sin\left(\frac{3\pi}{M}\right) - \frac{1}{32}sin\left(\frac{4\pi}{M}\right)}{\frac{5\pi}{2M} - \frac{15}{4}sin\left(\frac{\pi}{M}\right) + \frac{3}{4}sin\left(\frac{2\pi}{M}\right) - \frac{1}{12}sin\left(\frac{3\pi}{M}\right)} \quad (7)$$

Table III shows the optimal feedback ratio 'a' for different M. Basically a notch is placed at around $0.88f_B$ (where f_B is the signal bandwidth, i.e. half of the channel bandwidth). However, when M increases, the feedback strength needs to be much smaller which makes the zero spread strategy not practical for medium and high oversampling ratios. For example, when M=8, 'a' needs to be 0.05925. 'a' is realized in SC modulator by the capacitor ratio. This ratio of nearly 1/20 implies a big capacitor spread and large layout area. So in this system the feedback from the last stage to the third stage is only used when oversampling ratio is as low as 5, which is the case of the WLAN mode. In WLAN mode, oversampling ratio of 5

TABLE III
OPTIMAL 'a' FOR DIFFERENT OVERSAMPLING RATIOS

M	Optimal 'a'
4	0.2286
5	**0.1488**
8	0.05925
16	0.01495

is employed in this system and the optimal ratio of 0.1488 is rounded to 1/6 for circuit implementation.

A programmable decimation filter is used to filter the out-of-channel noise and downsample the output to Nyquist rate. Filtering is accomplished in multiple stages. First stage is a Comb filter which is reconfigured for these three standards. In GSM mode, the comb filter is set to be third order and decimation is chosen to be 32; in WCDMA mode, the comb filter is reconfigured to be the fifth order and decimated by 5; in WLAN mode, the order and the decimation are 6 and 5 respectively. Two halfband filter stages, each decimating by 2 are used for GSM and WCDMA modes. An FIR filter is used as the last stage in all standards to further suppress the quantization noise and the blockers.

A Simulink® behavioral model of the modulator which includes OTA non-idealities (finite DC gain, finite gain-bandwidth, finite slew rate and output swing), comparator non-idealites (offset and hysterisis), DAC non-linearity and coefficient mismatch was simulated to obtain the specifications of the building-blocks. Based on the specifications obtained from this model, the peak SNR is 88 dB for GSM mode (M=128, L=2, B=1), 80 dB for WCDMA mode (M=20, L=4, B=1.5) and 60.8 dB for WLAN mode (M=5, L=5, B=3).

III. Circuit Implementation

The multi-standard SC $\Sigma\Delta$ modulator is prototyped in TSMC $0.18\mu m$, 1.8V CMOS technology and has been submitted for fabrication. The designs of important building blocks are discussed in this section.

A. Design of the OTA

Behavioral simulations indicate that at least 60 dB DC gain, more than 360 MHz gain-bandwidth and 200 V/μs slew rate is necessary in order to not degrade DR in WLAN mode. Thus gain boosting strategy is used to boost the DC gain without sacrificing the excellent frequency performance of the folded cascode topology. Fig. 3 shows the schematic of the folded cascode fully differential OTA with SC common mode feedback. Performance of the designed OTA is summarized in Table IV. Scaling down the biasing currents of the second, third, and fourth OTA is possible and will lower the power consumption. However, due to time constraint, scaling is not performed in this prototype.

B. Design of Comparators and the Quantizer

Owing to the noise-shaping nature of $\Sigma\Delta$ modulators, the comparator specifications are much more relaxed for high oversampling ratios, and for comparators in the latter stages. Thus in GSM and WCDMA modes, comparators with 5 mV-10 mV offset and 10 mV-20 mV hysteresis are found to be adequate. However in WLAN mode, a more accurate comparator is needed for the first stage since its non-idealities are only shaped by 2^{nd} order and not suppressed enough by the low oversampling ratio of 5. Behavioral simulations show that for the peak SNR to drop by less than 1 dB, the comparator should have an offset and hysteresis of less than 2 mV and 5 mV respectively. Hence two types of comparators are used in this system. A multi-stage comparator [6] as shown in Fig. 4 is used in the first stage; regenerative comparators [7] as shown in Fig. 5 are used in the subsequent stages and flash ADC. Fig. 6 shows the 9 level quantizer that's used in the last stage for WLAN mode. The $2V_{pp}$ maximum output swing of OTAs limits the input range of this 9 level quantizer and thus bounds its nominal quantization step size to 125 mV. The regenerative comparator provides enough resolution and consumes lower power than the multi-stage comparator when used in the flash ADC of this 9 level quantizer. R-ladder based DAC is used in this $\Sigma\Delta$ modulator for its simplicity. The INL error due to 2% resistor mismatch is less than 5 mV. Because this INL error undergoes a 4^{th} order noise shaping, the 2% resistor mismatch leads to less than 2 dB loss in SNR. Thus no additional Dynamic Element Matching (DEM) circuit is used to reduce the DAC nonlinearity error.

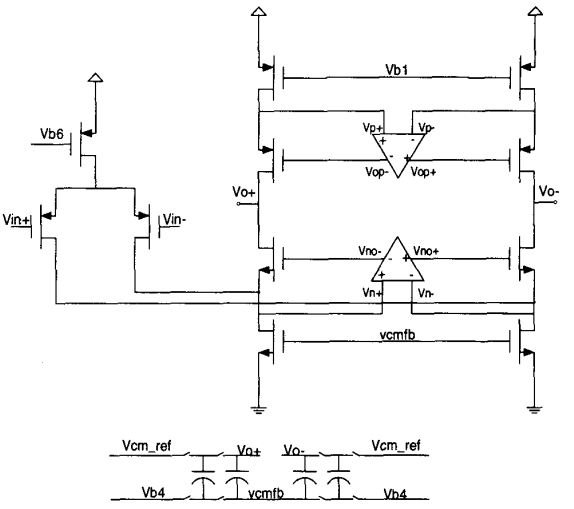

Fig. 3. Gain boosted OTA topology

TABLE IV
OTA PERFORMANCE

GB_OTA $C_L = 3pF$	DC Gain = 72 dB, Output swing = ± 1 V, Gain-bandwidth = 435 MHz, Phase Margin = 76° , Slew rate = 220 V/μs, CMRR = 101.5 dB @DC, 84.6 dB@1 MHz, PSRR = 102 dB @DC, 85. 6 dB @1 MHz, Power = 7.22 mW (excluding biasing).

IV. Simulation Results

This $\Sigma\Delta$ modulator is implemented in TSMC $0.18\mu m$ CMOS technology and operates from 1.8V supply voltage. The whole circuit is simulated using CADENCE-SPECTRE®. The simulated SNR versus input level is plotted in Fig. 7. Since

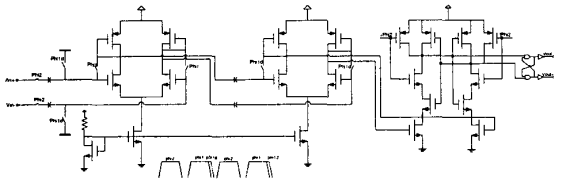

Fig. 4. Multi-stage comparator

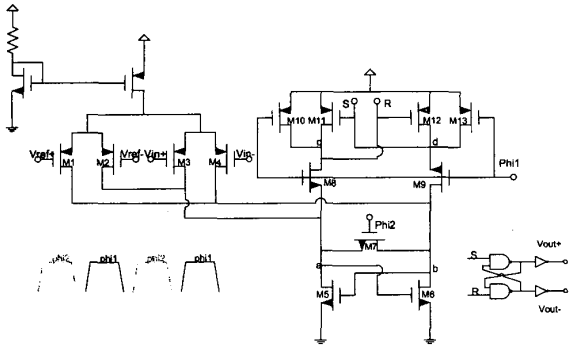

Fig. 5. Regenerative comparator

SPECTRE transient analysis does not include noise information, dominant noise - kT/C noise is hand calculated using (7), where N_i is the kT/C noise of the i^{th} stage, M is the oversampling ratio, A_i is the gain between the modulator input and the ith integrator input. Considering the kT/C noise, the SNDR from SPECTRE simulation is 85 dB, 74 dB and 58 dB for GSM, WCDMA and WLAN respectively. Table V summarizes the simulated performance of this $\Sigma\Delta$ modulator.

$$N_{kT/C} = \frac{N_1}{M} + \frac{\pi^2}{3A_2^2M^3}N_2 + \frac{\pi^4}{5A_3^2M^5}N_3 + \frac{\pi^6}{7A_4^2M^7}N_4 + \frac{\pi^8}{9A_5^2M^9}N_5 \quad (8)$$

MASH $\Sigma\Delta$ modulators are sensitive to coefficient mismatches. These coefficients are implemented in the switched-capacitor $\Sigma\Delta$ modulator by capacitor ratios. This necessitates the Monte-Carlo analysis for the capacitor mismatch. With a capacitor mismatch of 0.1%, Monte-Carlo simulation reveals a variation of peak SNR by 1dB, 0.73dB and 2.1dB for GSM, WCDMA and WLAN modes respectively.

TABLE V
SUMMARY OF PERFORMANCE OF THE MULTI-STANDARD $\Sigma\Delta$ MODULATOR

	Spectre® SNDR	$SNR_{kT/C}$	Total SNDR
GSM: 200kS/s, OSR=128, Order=2, bits=1, C_{S1}=0.5pF	85 dB	88 dB	83dB
WCDMA: 5MS/s, OSR=20, Order=4, 3-level feedback, C_{S1}=0.3pF	74 dB	79 dB	73dB
WLAN: 20MS/s, OSR=5, Order=5, 9-level feedback, C_{S1}=0.2pF	58 dB	69dB	58dB

V. CONCLUSION

A GSM/WCDMA/WLAN multi-standard $\Sigma\Delta$ modulator is proposed in this paper. Its SC implementation in a 1.8V TSMC 0.18-μm CMOS process uses gain-boosting strategy for OTA, offset cancellation strategy in comparator and multi-bit feedback. The prototype achieves an SNDR of 83 dB for GSM mode, 73 dB for WCDMA mode and 58 dB for WLAN.

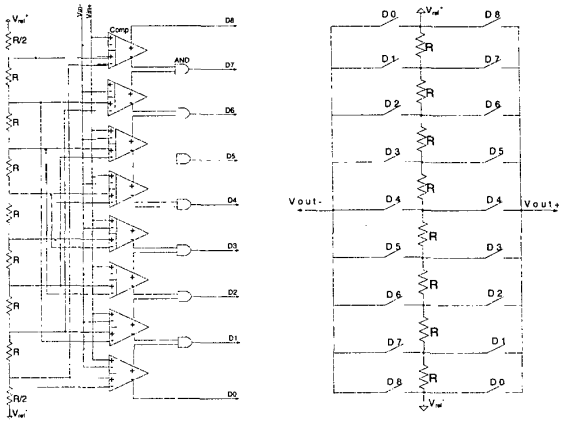

Fig. 6. Schematic of 9 level quantizer

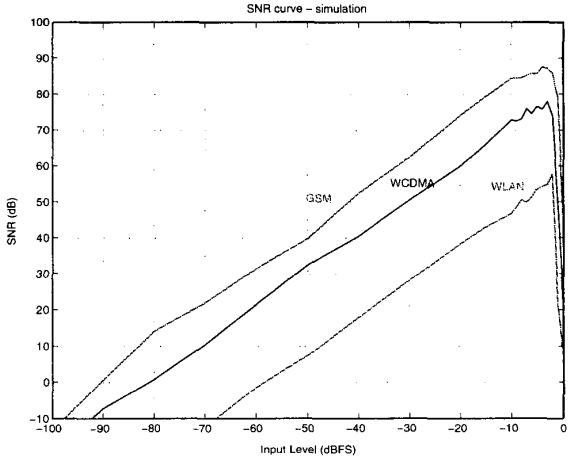

Fig. 7. SNR Vs. Input level obtained from Circuit-level simulations

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