A High Resolution, Extended Temperature Sigma Delta ADC in 3.3V 0.5μm SOS-CMOS

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Abstract—A ΣΔ modulator designed specifically for extended temperature applications is reported. The design is fabricated in a 3.3-V 0.5μm SOS-CMOS process and incorporates a 2-2 cascade architecture allowing operation as either a 2nd- or 4th-order modulator. Experimental data for both modulator configurations are presented including dynamic range (or effective resolution), signal-to-noise ratio and total harmonic distortion over a temperature range of 25°C to 225°C. The design obtains an effective resolution of ~16 bits at 25°C and ~12 bits at 225°C, both at a digital output rate of 2KS/s. Specific design details associated with high temperature operation are discussed including architectural issues, device sizing, and modulator noise. In addition, a digital decimation filter designed for use with the modulator and implemented in both software and in a field programmable gate array is summarized. This paper reports the first 4th-order ΣΔ modulator fabricated in an SOI/SOS process and demonstrates the feasibility of high resolution data conversion at elevated temperatures.

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1. INTRODUCTION

Recent advances in integrated circuit fabrication technologies and in temperature-tolerant circuit architectures have enabled true precision measurements in extreme environments. In particular, engine exhaust monitoring (both internal combustion and jet engine), seismic exploration/well management, and satellite/space flight have emerged as three of the most temperature demanding monitoring applications currently facing industry [1-3].

One of the most common functional modules in any sensor interface is the analog-to-digital converter (ADC). Of the many different circuit topologies employed for analog-to-digital conversion, only sigma delta (ΣΔ) based methods have shown significant promise for precision high temperature operation. ΣΔ methods incorporate oversampling and noise shaping and consequently provide improved resolution over Nyquist-rate conversion methods by trading component accuracy for time. This inherent property of oversampled converters makes them ideal for high-temperature applications since component errors and drifts associated with elevated temperature are well tolerated compared to other analog-to-digital conversion (ADC) techniques.

Several papers have been published on ΣΔ modulators implemented in Silicon-On-Sapphire (SOS) or Silicon-On-Insulator (SOI) for high-temperature or radiation environments [4-6]. Though significant, these reported designs implement 2nd-order noise shaping and produce at best 13 bits of resolution. This research addresses the need to extent the obtainable resolution of ΣΔ ADCs fabricated in SOI/SOS for high-temperature applications and reports the first 4th-order modulator architecture fabricated in SOS/SOI.

2. MODULATOR ARCHITECTURE

The modulator reported was designed with special consideration for high-temperature operation [3]. Though cascade topologies do present some disadvantages when compared to single-loop structures, namely reduced input dynamic range and matching errors, the topology composed of two 2nd-order loops is inherently stable. In addition, single-loop modulator architectures allow for more straight-forward implementation of the digital decimation filters, but

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require proper initialization, monitoring and compensation to ensure robust stability. For these reasons, a 2-2c cascaded architecture was selected. The classical integrator gain was implemented since it has been shown to be less sensitive to matching errors as compared to alternative gain selections that minimize the required integrator output swing. The 2-2c modulator architecture is shown in Figure 1.

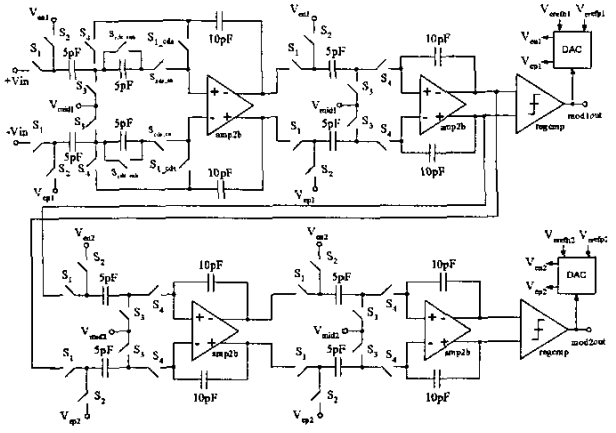


Figure 1 – 2-2c cascade modulator architecture with 1st-stage correlated double sampler

3. INTEGRATOR AMPLIFIER

The integrator amplifier is the most critical functional block of the modulator as it determines the integrator performance and dominates the input-referred electronic noise of the modulator. A fully differential architecture was implemented for rejection of common-mode noise and offsets. Preliminary simulations and SOS MOSFET device measurements indicate that either a multi-stage topology or cascoded topology is required to obtain open loop dc gains on the order of 2000. Multi-stage topologies require more than one common-mode feedback loop (CMFB) and are typically more difficult to compensate than single-stage structures [6]. Conversely, a folded cascode topology produces high loop gain, requires a single CMFB loop, and is more easily compensated. Disadvantages of this architecture include increased input-referred noise and limited output swing due to the cascode devices. However, the stability advantages of the folded cascode over multi-stage topologies make it more desirable for wide temperature application.

A schematic of the fully-differential folded cascode amplifier is shown in Figure 2. Continuous-time CMFB was incorporated to allow use in both sampled- and continuous-time applications. The output of the amplifier is buffered using source followers made of intrinsic devices (~zero threshold voltage) and the common-mode voltage determined using a resistance divider. The CMFB loop compares this voltage to a CMFB reference and controls the load devices M9 & M10 to maintain the output at the desired common-mode level. A modified wide-swing cascode biasing is used throughout to provide maximized output swing and precise bias setting [7,8]. The bias circuit for the amplifier is shown in Figure 2 and incorporates feedback loops formed by MB8/MB9 and MB17/MB18 to ensure the cascode devices M10, M12, M14, and M20 remain in saturation over a wide range of temperatures.

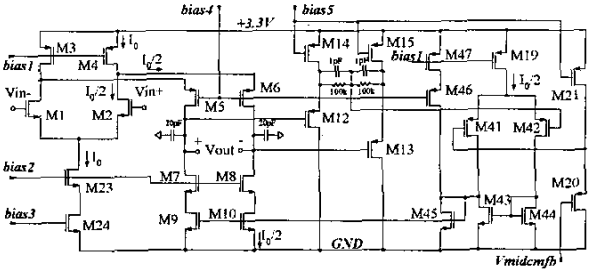


Figure 2 – Folded cascade opamp with common-mode feedback

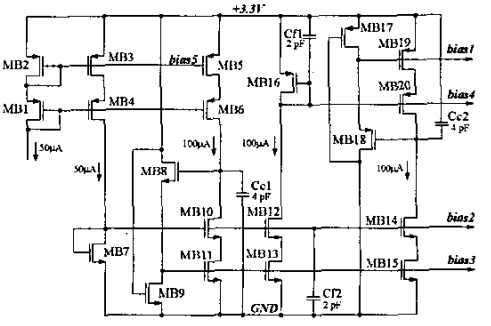


Figure 3 – Opamp bias circuitry incorporating low-voltage cascodes

4. DIGITAL DECIMATION FILTER

The decimation filter designed for use with the ΣΔ modulator is shown in Figure 4. The filter implements a novel architecture allowing use with both single loop architectures and cascaded architectures. The decimation ratio is 256, and the maximum resolution is 24 bits. As Figure 4 shows, the decimation filter is made of two FIR filters, the noise-cancellation filter, and a sinc filter with the decimator. The FIR filter is designed as a one-bit-input FIR filter using adders only, allowing operation at the oversampling frequency. The primary purpose of the FIR filter is to correct the droop caused by the 4th-order sinc filter as well as to add to the total filter out-of-band attenuation. The goal in this design was to have the pass-band ripple less than 0.02 dB, while maintaining sufficient stop-band attenuation to suppress the out-of-band quantization noise of a high-resolution modulator.

The FIR filters from Figure 4 have an order of 4096 and are composed of 64 non-zero taps padded with 64 zero-taps.

The non-zero tap values were determined using the Remez exchange algorithm in Matlab. 64 zero-taps were inserted between the filter taps to generate a comb-like filter whose structure is shown in Figure 5. Each shift register is one bit wide allowing multiplier-free implementation. The filter taps are 12-bit precision and produce a 15-bit wide data path at the output of the filter. The magnitude response of the filter was simulated using Matlab and is shown in Figure 6.

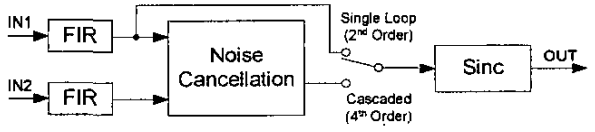


Figure 4 – Decimation filter architecture

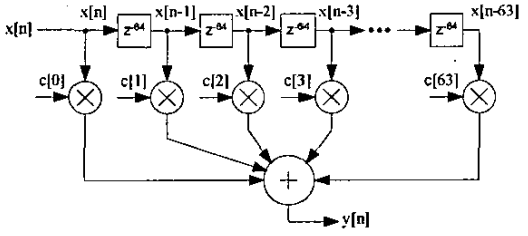


Figure 5 – FIR filter structure

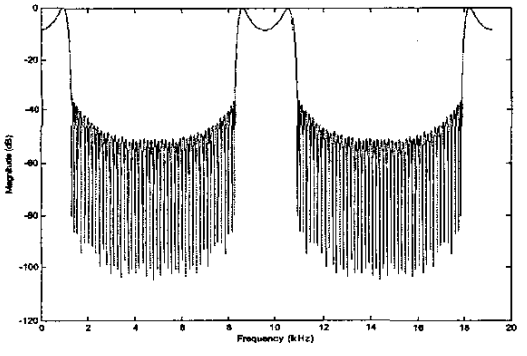


Figure 6 – Magnitude response of the FIR filter (f_s = 614.4 kHz)

The noise cancellation filter of Figure 4 is required when the filter is used with cascaded ΣΔ modulators composed of 2 single-bit loops [7]. Most commonly, this filter is placed before the decimation filter which consequently requires multi-bit multiplication in the decimation filter. The topology presented in this work partitions the filter, placing the noise cancellation function following the FIR function. This topological improvement reduces the overall filter implementation complexity and allows higher signal bandwidths. The noise cancellation filter block diagram is shown in Figure 7. The inputs are 15-bits wide and the filter produces a 21-bit result.

The sinc filter of Figure 4 is a 4th-order sinc filter followed by decimation. The most effective implementation of the filter is an integrator-decimator-differentiator structure as shown in Figure 8. The decimation factor M is 256, and it is equal to the oversampling ratio of the modulator.

As elaborated in [8], to avoid overflow the datapath size in the sinc structure needs to be

$$b > \log_2\left[\left(M^k + 1\right)\right] + c > 53 \qquad (1)$$

where b is the number of bits in the datapath, $M=256$ is the decimation ratio, $k=4$ is the sinc order, and $c=21$ is the number of bits input to the sinc filter from the noise cancellation filter. A number of the least significant bits from (1) can be dropped depending on the modulator's practical dynamic range.

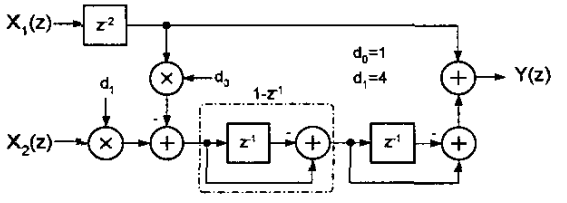


Figure 7 – Noise-cancellation filter

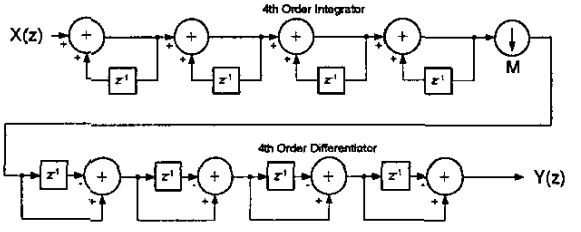


Figure 8 – 4th-order sinc filter with a by-M decimator

Figure 9 shows the total impulse response of the filter without decimation. The filter exhibits an increase of 20dB/octave in stop-band attenuation making it most effective at rejecting the quantization noise furthest away from the baseband where the most of the noise power is located. Lower attenuation at frequencies closer to the baseband is sufficient since the quantization noise power at these frequencies is very low. Note that the nulls of the sinc function have been placed to maximize attenuation of the baseband images of the FIR filter.

As shown in Figure 10, the simulated total pass-band ripple for the decimation filter is less than 0.015 dB which is much better than the pass-band ripple in most commercial, low-temperature ADCs. Figure 11 shows the simulated 3dB-bandwidth of the filter which is approximately 1 kHz for the decimated sampling frequency of 2.4 kHz.

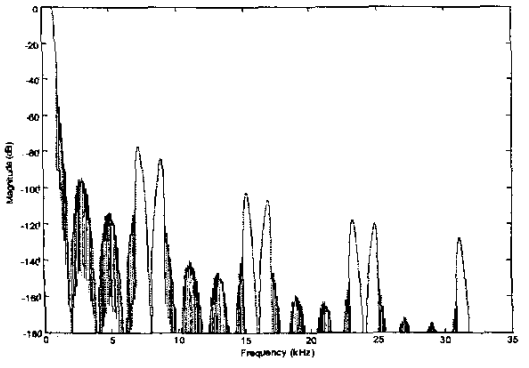


Figure 9 – Magnitude response of the decimation filter (f_s = 614.4 kHz)

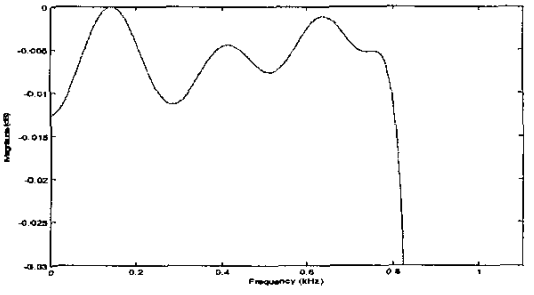


Figure 10 – Simulated pass-band ripple of the decimation filter

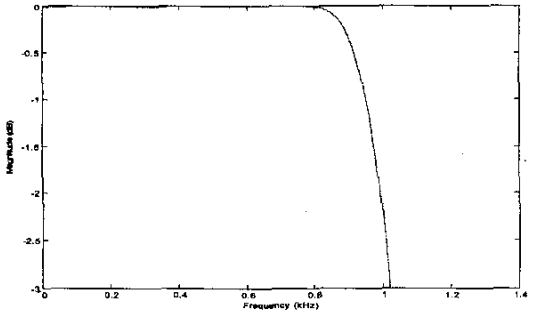


Figure 11 – Simulated 3-dB filter response

The decimation filter was first implemented in a Xilinx XC4062XLA-09-HQ240 FPGA as an intermediate step in an effort to design a high-resolution, high-temperature ΣΔ A/D converter ASIC [9]. The shift register from Figure 5 was designed as a 4096-bit long, one-bit wide FIFO using FPGAs distributed RAM controlled by an address counter. Since the impulse response of the FIR filter is symmetric, the one-bit multiplication with the 12-bit filter taps was implemented as a multiplexer.

Besides the decimation filter core, a number of additional blocks were implemented to allow filter configuring and self testing. Interfacing to the filter is accomplished using an SPI port that allows access to a number of configuration and status registers. The entire FPGA implementation required 2,727 flip-flops, 2,485 4-input lookup tables, and 637 3-input lookup tables which represented 80% of the FPGA resources. Testing of the FPGA code was performed using a generic board containing two XC4062XLA FPGAs and interface circuitry to communicate with a PC running a LabVIEW GUI. The filter can operate using input data from either an external modulator or a pre-stored modulator file. The output of the filter is stored to the PCs hard drive, analyzed, and displayed using the LabVIEW GUI.

Figure 12 shows the simulated output of the decimation filter with an input data stream acquired from an Analog Devices AD1555 modulator (full-scale input signal, f = *240 Hz*). Figure 13 shows the output of the FPGA-implemented decimation filter under the same test conditions. As demonstrated in Figures 12 and 13, excellent agreement between the simulated and experimental results was observed. Furthermore, the calculated SNRs in both cases were identical.

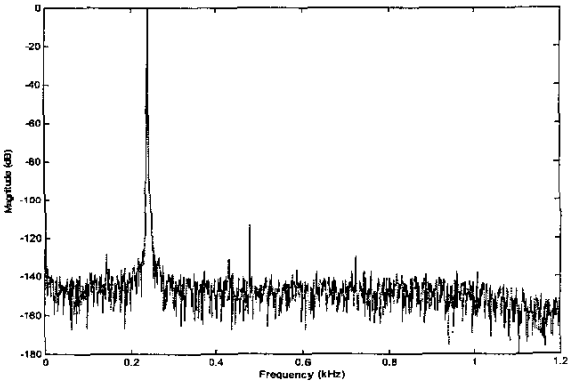


Figure 12 – Simulated decimation filter output using AD1555 modulator (0-dB, 240-Hz input)

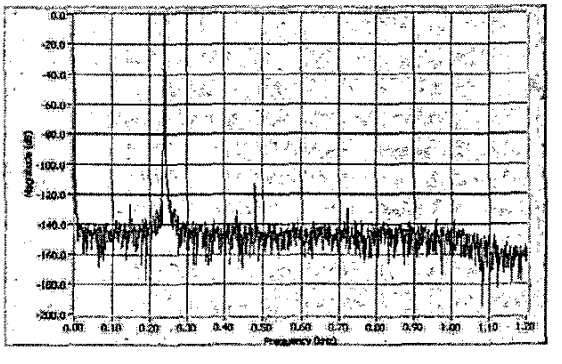


Figure 13 – Experimental decimation filter output using AD1555 modulator (0-dB, 240-Hz input)

Figures 14 and 15 show simulated and experimental results for the decimation filter where the input data stream was generated using a custom-designed, high-temperature ASIC modulator [3]. Again, excellent agreement in filter performance was observed.

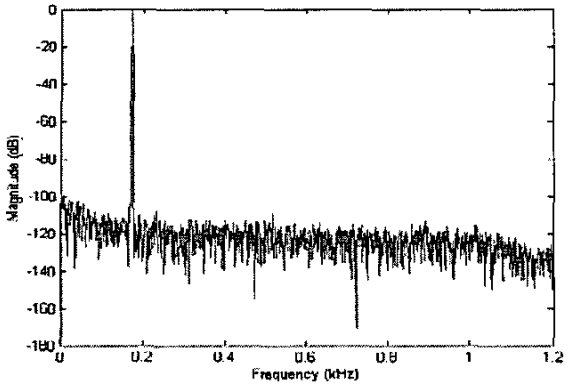


Figure 14 – Simulated decimation filter output using custom-designed modulator (-6-dB, 180-Hz input)

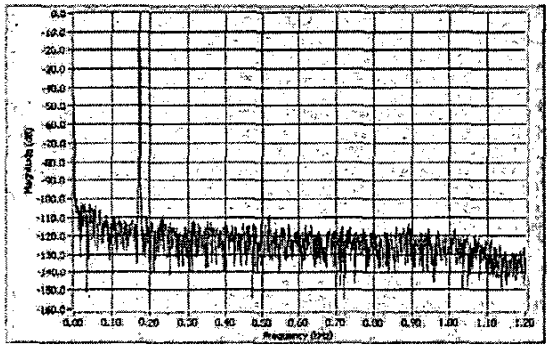


Figure 15 – Experimental decimation filter output using custom-designed modulator (-6-dB, 180-Hz input)

5. Experimental Results

The modulator and digital filter designs were fabricated as separate integrated circuits in a 0.5μm SOS-CMOS process available through MOSIS. Photographs of these two custom chips are shown in Figures 16 and 17. The modulator ASIC incorporates the circuits of Figure 1 plus clock generation circuitry and buffer amplifiers to enable off-chip monitoring of each integrator output. The digital filter ASIC was designed using a mixture of standard cell and custom layout techniques. To minimize silicon implementation area, the FIR shift registers were implemented as custom-designed SRAM cells controlled by a set of counters. The noise cancellation and sinc filter chip layouts were also custom designed to reduce the chip area. Only the SPI circuitry was synthesized directly from VHDL using standard cells. Testing of the digital filter ASIC produced the same results over the temperature range of 25°C to 225°C as the FPGA implementation at room temperature. The remaining part of this section will focus entirely on the ΣΔ modulator test results.

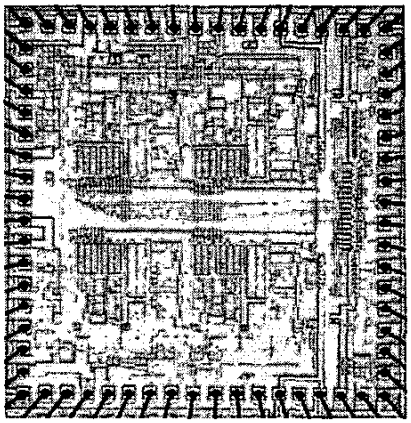


Figure 16 – Photograph of the 2nd- and 4th-order ΣΔ modulator fabricated in 0.5μm SOS-CMOS

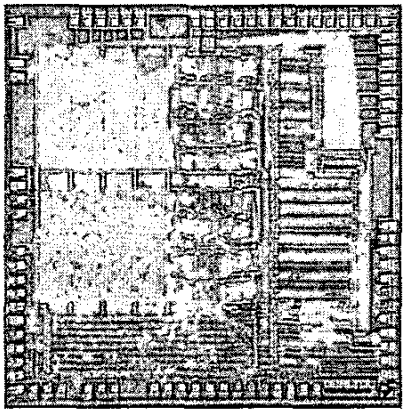


Figure 17 – Photograph of the digital decimation filter fabricated in 0.5μm SOS-CMOS

Figure 18 shows the measured open loop response of the integrator amplifier as a function of temperature from 25°C to 200°C with 20pF load capacitance. Table 1 summarizes the preliminary results of the testing. These results indicate very little degradation of the amplifier open loop gain with increasing temperature. Maintaining high loop gain is important at all temperatures to prevent excessive noise contribution from secondary integrators in the modulator loop.

A multitude of tests were performed on the modulator as a function of temperature and input amplitude using a custom-designed test setup. The chips were tested from 25°C to 225°C with a low-noise input sine wave of 36.6Hz and

144Hz. The measured output spectrum of the modulator is presented in Figures 19-22. Figures 19 & 20 show the room temperature output spectra as a function of input amplitude for the modulator configured as 2nd and 4th order, with CDS disabled, and with CDS enabled. Each FFT is calculated from ~1M points and the spectra shown represent an average of 8 runs. Figures 21 and 22 show the output spectra as a function of temperature for a fixed input signal amplitude of -3dB. Note the increase in the noise floor with increasing temperature.

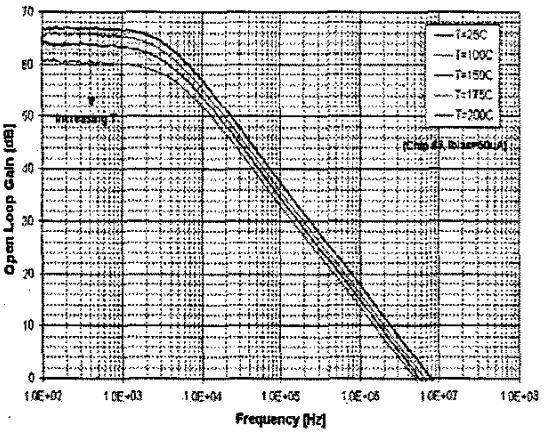
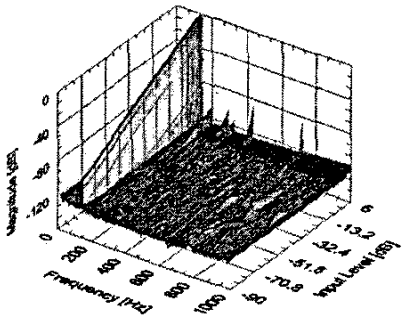


Figure 18 – Measured DC open loop gain vs. T

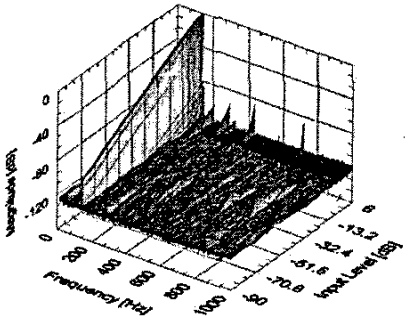
Table 1 - Opamp measured performance summary

Parameter	T=25°C	T=150°C	T=200°C
A_{ol} [V/V]	2298	1611	1117
GBW	7.85MHz	5.60 MHz	4.99 MHz

At each temperature the SNR and THD were calculated as a function of input amplitude and are presented in Figures 23 and 24, respectively. Test results indicate decreased peak SNR with temperature as expected. However, this is the result of increased electronic noise [10] and not quantization noise shaping as demonstrated by both the measured dc gain of the integrator amplifier and observed slope of the shaped quantization noise at high temperature. In addition, the THD calculations indicate increased distortion with both increased input signal level and temperature, as expected. The measured dynamic range (DR) of the modulator as a function of temperature is shown in Figure 25, for both 2nd and 4th order modulators with the CDS enabled and disabled. A summary of test data for the modulators over a range of temperatures is shown in Table 2.

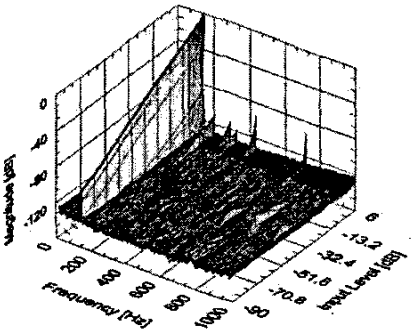


(a)

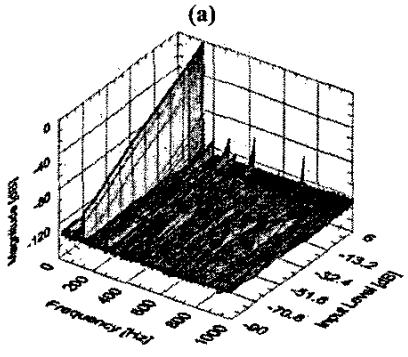


(b)

Figure 19 – Measured 2nd-order modulator output spectrum at room temperature (a) CDS off and (b) CDS on (f_{in} = 144Hz)



(a)



(b)

Figure 20 – Measured 4th-order modulator output spectrum at room temperature (a) CDS off and (b) CDS on (f_{in} = 144Hz)

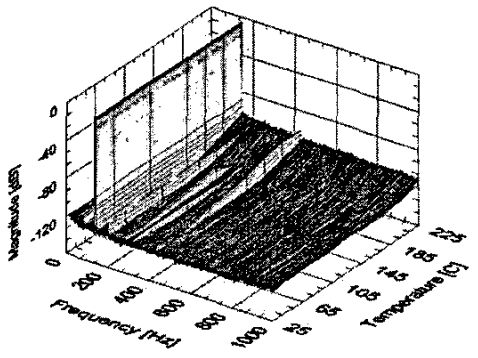


Figure 21 – Measured 4th-order modulator output spectrum vs. T (CDS off, -3dB input, f_{in} = 144Hz)

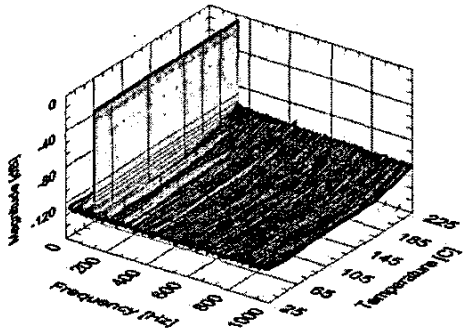


Figure 22 – Measured 4th-order modulator output spectrum vs. T (CDS on, -3dB input, f_{in} = 144Hz)

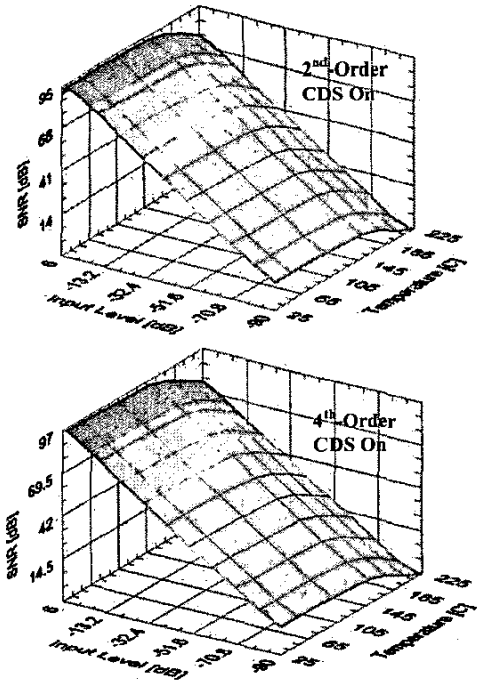
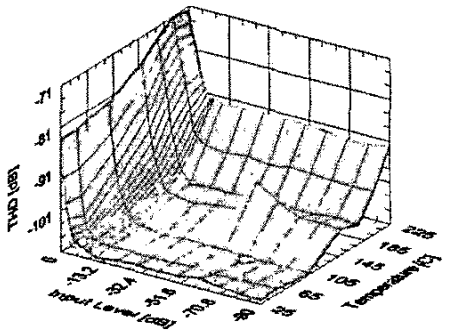
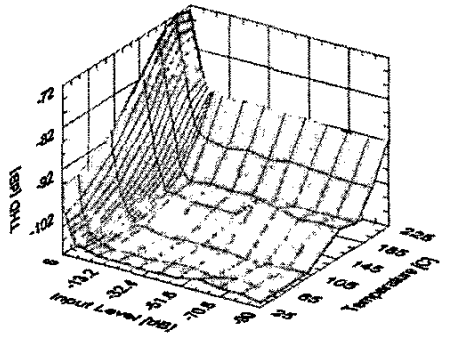


Figure 23 – Measured SNR as a function of T and modulator input level (f_{in} = 144Hz)



(a)



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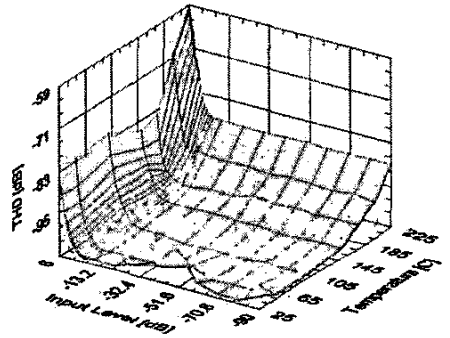
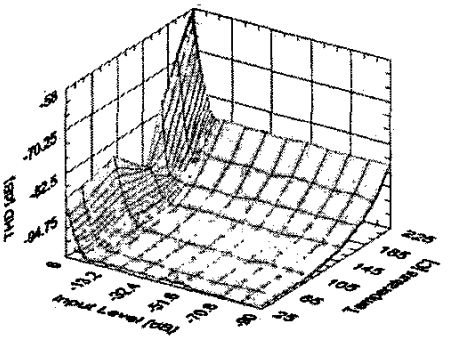


(c)



(d)

Figure 24 – Measured THD as a function of temperature and modulator input level (a) CDS off, 2nd-order, (b) CDS off 4th-order, (c) CDS on, 2nd-order, (d) CDS on, 4th-order, (all cases f_{in} = 144Hz)

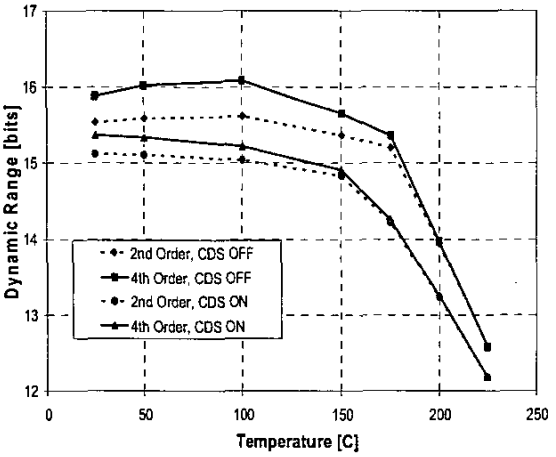


Figure 25 – Measured 4th-order modulator output spectrum vs. T (CDS on, -3dB input, f_{in} = 144Hz)

Table 2 – Measured modulator performance (DOR=2KSPS, 36.6Hz input, CDS off)

Parameter	T=25°C (2^{nd} / 4^{th})	T=150°C (2^{nd} / 4^{th})	T=200°C (2^{nd} / 4^{th})	T=225°C (2^{nd} / 4^{th})
SNR [dB]	95.4/97.4	94.3/96.0	85.8/85.9	77.6/77.6
Res. [bits]	15.5/15.9	15.4/15.7	14.0/14.0	12.6/12.6
SNR [dB]	93.9/94.8	92.9/93.3	81.8/81.8	72.6/72.6

Overall testing indicates that low-frequency noise reduction is accomplished using CDS but this techniques provides limited benefit in this case due to the increase of the white noise associated with this operation. In addition, the low frequency reduction due to CDS appears to increasingly fail for temperatures above 175°C as noticed by the 1/f noise creep in the output spectrum. The reason for this phenomenon is not obvious and will require further investigation. However, the use of CDS will provide significant improvement in dynamic range over a system without CDS for smaller signal bandwidths than shown in this paper.

6. Conclusions

This work represents the first presentation of both 2^{nd}- and 4^{th}-order ΣΔ modulators in SOI/SOS and demonstrates the feasibility of high-resolution data conversion in SOS using ΣΔ techniques at elevated temperatures. SNR, THD, and DR data were presented over a temperature range of 25°C to 225°C. Over the entire temperature range, the measured modulator performance indicates that the design is input-noise limited and improved performance can be obtained with better noise management. The use of CDS in this design provided no improvement in performance with a digital output rate of 2k samples/second. However, significant improvement in performance over systems without CDS can be obtained up to ~175°C if lower DORs are used. The high flicker noise contribution of the MOS devices in SOS processes certainly imposes dynamic range limitations if design and implementation techniques are not incorporated for additional suppression of 1/f noise.

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Nance Ericson is a member of the Monolithic Systems Development Group in the Engineering Science and Technology Division at the Oak Ridge National Laboratory. He also serves as an Adjunct Assistant Professor of Electrical Engineering at the University of Tennessee, Knoxville. He received the B.Sc. degree from Christian Brothers University, Memphis, TN in 1987, the M.S. degree from the University of Tennessee, Knoxville in 1993, and the Ph.D. from the University of Tennessee, Knoxville in 2002, all in electrical engineering. Presently, he is involved in a variety of research projects with focus on the design of mixed-signal CMOS integrated circuits and integrated sensors for harsh environment and biomedical applications. His research interests include physiological/biological sensing, nanostructures, high-resolution data converters in SOS-CMOS, and high-temperature integrated circuits. He has authored or coauthored over 60 technical publications. He holds seven patents in the area of high-temperature measurement, integrated photo-spectrometers, and implantable sensing methods.

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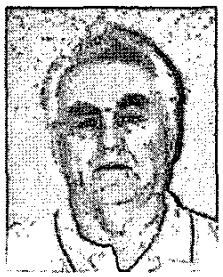

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