A Monolithic RF Microsystem in SOI CMOS for Low-Power Operation in Radiation-Intense Environments[1]

Erik A. McShane and Krishna Shenai
Dept. of EECS (M/C 154)
University of Illinois at Chicago
851 South Morgan Street
Chicago, IL 60607
312-996-2633
{mcshane,shenai}@eecs.uic.edu

Brent Blaes
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
Pasadena, CA 91109
818-354-9013
Brent.R.Blaes@jpl.nasa.gov

Abstract—A monolithic radio-frequency (RF) microsystem has been designed and fabricated in an advanced 0.25-micron SOI CMOS technology. The architecture is comprised of a compact digital core for local program execution and command handling; a 400-MHz RF transceiver for wireless program download and data transfer; and analog baseband circuitry which doubles as an embedded testability network. The IC is intended to support nanosatellite avionics and wireless remote sensing. The motivation of the work was to develop a team design methodology for producing integrated circuit (IC) intellectual property (IP) in the context of a specific application. Another intention is to investigate the suitability of an ultra-low-power digital technology for mixed-signal/RF circuit design. The design was a collaborative effort between UIC and JPL that demonstrates the potential for technology transfer between universities and federal laboratories.

TABLE OF CONTENTS

1. INTRODUCTION

The emerging class of nanosatellites and miniature spacecraft is motivating a transition in avionics systems toward monolithic integration. This trend has been evident in consumer electronics for years since it delivers improved system density, reduced system mass, and equal or better performance. A similar evolution in aerospace applications, however, has lagged behind primarily because of additional constraints on reliability, fault tolerance or redundancy, cost, and specific functional requirements.

Submicron VLSI technology, particularly CMOS, has now matured to the degree that it can satisfactorily implement a broad range of digital, analog, RF, and sensor electronics in a monolithic integrated circuit (IC). These technologies, considering their thin gates oxides (under 100 Å) and small channel areas, can also offer radiation hardness to better than 100 Krad, even without special process modifications. A single IC or a small chipset thus can deliver the performance comparable to a multi-board system without compromising on functionality. Since CMOS is also a relatively low-cost technology, hardware reliability can be provided at the IC level by piggy-backing redundant units for hot-swap recovery.

Exploiting monolithic integration, though, requires that two challenges be met. First is modeling and preventing undesirable electro-thermal interference between nominally isolated subsystems on the IC. This is a problem common to all monolithic systems. It can be addressed now only by combining engineering foresight with efficient custom models; no comprehensive software tool exists to perform complete verification. Second is the development of hard- and soft-core IP that offers both high performance and multiple reuse. This issue pertains to defining sufficiently broad performance characteristics and then defining how technology details influence them.

For the work described in this paper, we decided to develop a monolithic RF microsystem with sufficient complexity to explore these issues, but with enough simplicity to clearly evaluate experimentally each independent subsystem. We have developed an architecture that consists of digital, analog, power, and RF subsystems for applications in microsatellite avionics and wireless remote sensing.

The architecture consists of a digital processor core, an RF transceiver, an I/O (input/output) interface linking the processor to communications, and two on-chip DC-DC voltage converters for integrated power management. These subsystems are linked by a testability network which can be used to fully isolate the subsystem for test or to join them for functional operation.

The paper is organized as follows. First an overview of the entire architecture is presented. Next each of the major subsystems is discussed in detail: digital, analog, RF, and testability. Finally conclusions and future work are offered and described.

[1] 0-7803-5846-5/00/$10.00 © 2000 IEEE

2. Architecture Overview

The architecture is comprised of digital, analog, power, and RF subsystems. A block diagram is shown in Fig. 1. Program code is downloaded via the RF link (the antenna is labeled ANT) or by using a parallel bus interface (marked IBUS and OBUS for input and output bus, respectively). The control program, which runs in a continuous loop, can be used to monitor an external component via the parallel bus and transfer data to the RF transceiver for uplink. This IC demonstrates the integration potential of a technology optimized for low-power digital circuits that also has inherent radiation-hard properties. It is part of an ongoing effort to integrate analog, RF, and digital circuits into a single low-voltage digital technology for microavionics.

The digital core consists of an 8-bit 33-MHz microcontroller (the RISC CPU) and a 256-byte SRAM (static RAM) for local program storage. A reduced instruction set (16 instructions) performs ALU (arithmetic/logic unit) operations and data transfers between memory and the RF transceiver I/O controller. The I/O control is interrupt-driven, and a single shared register is used for data transfer.

In the start-up condition, the IC enters a spin-wait state that is maintained until a data transfer is initiated from the I/O interface. Using a microcoded ROM (read-only memory) boot program, data is sequentially stored in the SRAM until a termination code is received. At that time, control is transferred from the boot ROM to the stored program. The stored program executes in a continuous loop unless the IC reset pin is stimulated, which causes it to flush the stored program and return to the spin-wait state.

The RF communications is provided by a 400-MHz zero-IF (zero intermediate frequency) transceiver. Data transmission consists of an 8-bit binary word with a hold time of 500 microseconds, resulting in a data rate of approximately 2 KByte/sec. The baseband signal is generated by the summation of eight unique ASK (amplitude shift keyed)-modulated sine waves. The sinusoids are uniformly distributed on a logarithmic scale in a 100-kHz bandwidth. A data byte provides the ASK modulation signal.

The complex baseband is then frequency multiplied by a 400-MHz carrier to produce the RF signal. Baseband signal recovery is achieved with eight parallel envelope detectors, each tuned to the frequency of a specific baseband sinusoid. Transmissions are initiated and terminated with unique 8-bit patterns. The I/O controller defaults to a standby receive mode in which the downconverted data is compared with the initiate key. The transmitter is activated only by a request from the loop program executed in the digital logic.

The two on-chip voltage converters (labeled as PMAD) are a demonstration of a boost converter with integrated feedback control and startup circuitry [1]. The converters are intended to provide a rapid response to dynamic load conditions for minimal ripple in the internal supply voltage. Independent converters are present for the analog/RF and digital subsystems to minimize the coupling of digital switching transients onto analog supply lines. Each shares a 2-V battery (BATT) as an input and has an IC output (either DCD or DCA) to an external filter capacitor. The filter outputs are returned to the IC using the inputs VDDD and VDDA for digital and analog voltage supply, respectively.

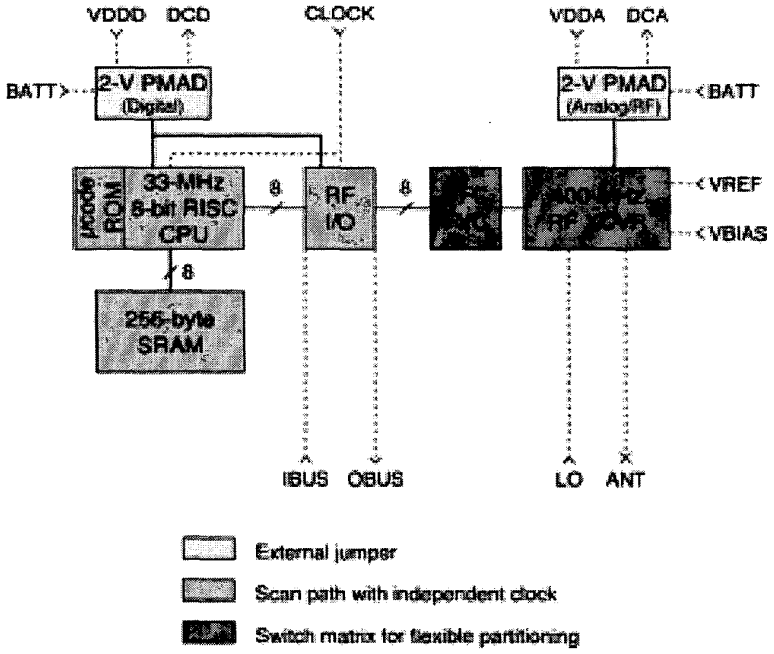
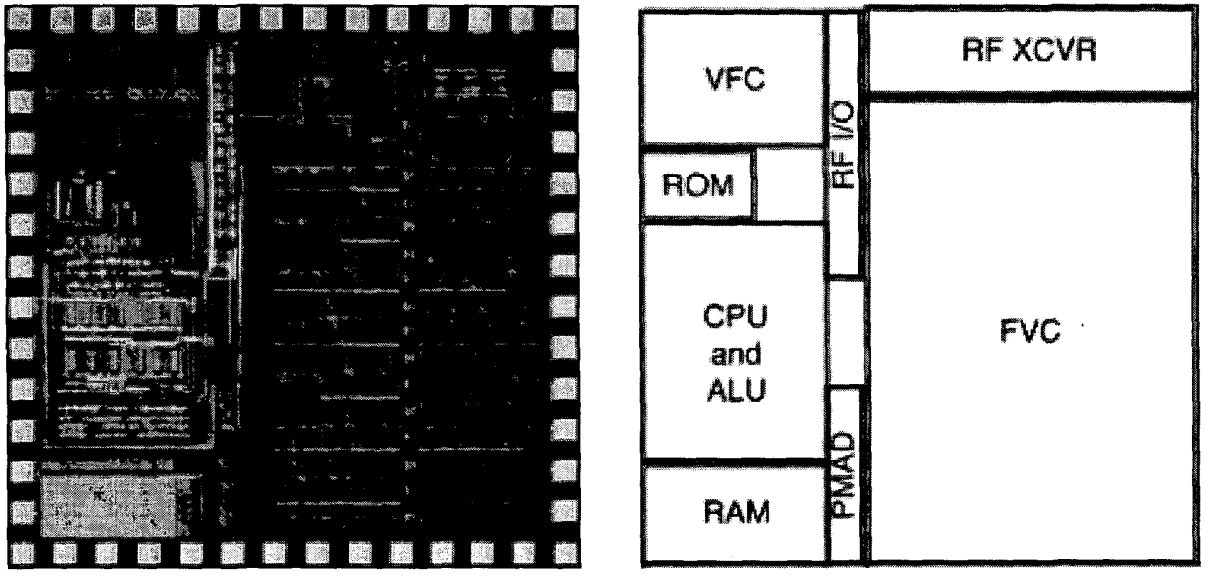


Figure 1 Block diagram of the RF microsystem.



(a) (b)

Figure 2 Illustrations of the (a) die layout and (b) floorplan mapping.

The embedded testability network can be used to segregate the individual subsystems for isolated functional testing. This is accomplished in several levels. First, the external filter capacitor of the voltage converters can be used to measure regulation. Second, all the digital logic includes a scan path which provides full controllability and observability of all internal storage nodes and combinational logic. Third, a switch matrix can partition the analog baseband electronics. The gross test partitioning is indicated in Fig. 1 by various shadings.

The IC was fabricated using the MIT/Lincoln Laboratory 2-V 0.25-micron SOI CMOS technology. The die layout and floorplan are shown in Fig. 2. It occupies a 2.2 mm x 2.2 mm footprint, of which the RF and analog baseband processing circuits consume approximately 80%. The die is currently undergoing testing at the Jet Propulsion Laboratory through collaboration with the JPL Systems on a Chip Group.

Following this overview of the architecture, its subsystems are described in more detail.

3. Digital Subsystem

The digital architecture implements an 8-bit 33-MHz RISC CPU with microprogrammed control and a small, fast local memory. The eight-bit signal width of the RF section was used to fix the datapath and internal bus widths at 8 bits. To keep memory addressing simple and fast, an eight-bit address is used to directly access memory, yielding a total address space of 256 bytes. The memory is thus similar to a direct-mapped cache [2]. All instructions are of a fixed, one-byte size to match the bus width. A fixed instruction size was chosen to reduce the complexity of instruction decode and issue. A second consideration is that the limited capacity of the on-chip memory is not suitable for the extensive computations or processing which are served by a richer instruction set. Figure 3 shows the block diagram of the digital subsystem.

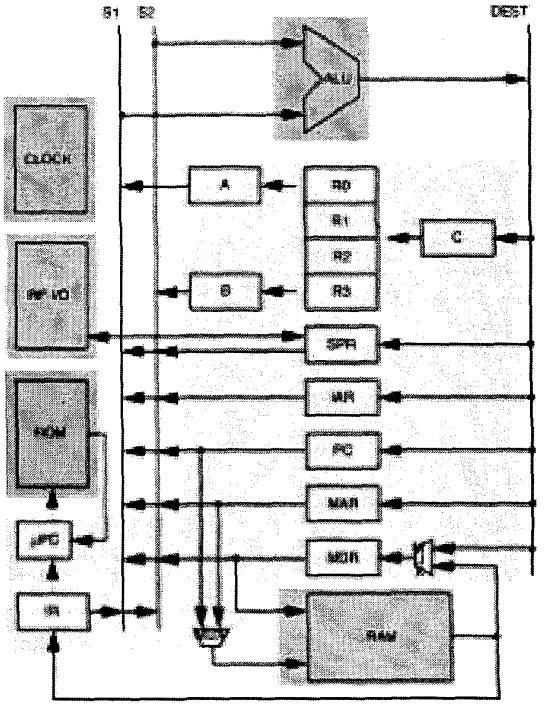


Figure 3 Block diagram of the digital subsystem.

Of the eight available instruction bits, four are reserved for the opcode yielding a total of 16 instructions. The remaining four bits are used to specify either source and destination registers or as an immediate value for data load or jump offset. Figure 4 lists the instruction set and addressing modes. All arithmetic operations are signed and no floating-point instructions are available.

A 32-bit by 23-bit ROM acts as the microprogram storage. Bit storage is provided by a single pass transistor tied to either the power or ground rail. This circuit topology was designed with consideration of the layout design rules to ensure an optimized physical implementation. No instruction buffering or prefetching is employed since the ROM can deliver a row access within the 3 ns window allocated for instruction fetch and setup. This speed is due in part to its small size but also to the staggering of the address decode and data fetch operations.

Program and data storage is provided by a 256-byte SRAM. Although the capacity is small, it provides enough storage to fully exercise the instruction set and run limited programs. A larger storage capacity was impractical just to validate the prototype since SRAM macros are standard components of ASIC libraries. The SRAM itself did not constitute an IP of interest within the system. Besides area and feasibility constraints, a 256-byte memory is the maximum addressabke space obtained by eight bits without resorting to a segmented or offset addressing technique.

	4	2	2
R-Type	opcode	rs	rd

ADD	R1, R2	R1 <- R1 + R2
SUB	R1, R2	R1 <- R1 - R2
AND	R1, R2	R1 <- R1 ^ R2
XOR	R1, R2	R1 <- R1 ⊕ R2
SLL	R1, R2	R1 <- R1 << R2
SLT	R1, R2	R1 <- ? (R1 < R2)
SEQ	R1, R2	R1 <- ? (R1 == R2)
MOVI2S	SPR, R1	SPR <- R1
MOVS2I	R1, SPR	R1 <- SPR
LB	R1, R2	R1 <- M[R2]
SB	R1, R2	M[R2] <- R1
JALR	R1	R3 <- PC + 1; PC <- R1

	4	4
I-Type	opcode	immediate

LI	#15	R0 <- 15
BEQZ	name	? (R0 == 0) PC <- PC + name
TRAP	name	IAR <- PC; PC <- name
RFE		PC <- IAR

Figure 4 Instruction set architecture.

An arithmetic-logical unit (ALU) implements the data manipulation instructions. To minimize system complexity the ALU is involved in every instruction execution, either to perform a data operation or to redirect data among bus lines or between registers. The basis of the ALU chain is a ripple-carry adder. Although ripple-carry is not suitable for high-performance and does not scale well to larger operands, it met our timing goals. The simplicity of the cell design was also amenable to a compact physical design.

To control interaction of the analog and digital sections of the IC, an I/O state machine arbitrates communications using the system bus and provides all necessary timing. Transmission and reception occur in a series of phases. Figure 5 shows the state machine for the RF I/O.

A received data signal is always preceded by a key, assumed to be the digital signal 11110000, which is held for four consecutive sample periods. A transmitted data signal is preceded by a complementary key. A key is used to isolate a valid transmission from spontaneous RF noise signals.

In the (default) receive mode, the RF I/O monitors the data lines to determine if a key has been received. If a key is seen, then a trigger is sent to latch the data which has been converted by the baseband signal processing. Data is captured in the special purpose register (labeled as SPR in Fig. 3). Latching after the trigger ensures that the input data has stabilized and the no following data transmission has distorted the current input. Once data has been latched, an interrupt is sent to the CPU.

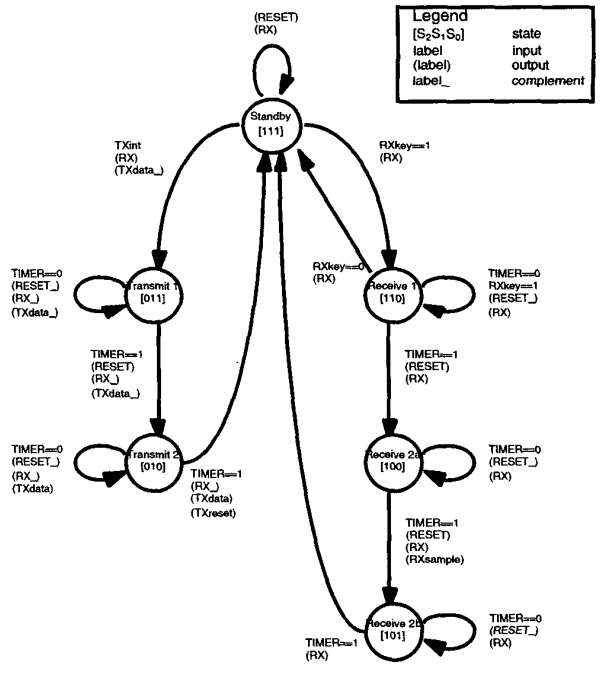


Figure 5 State machine of the RF I/O controller.

This design abstraction is ideal for two applications: embedded control in which the CPU is a slave to an external process and remote sensing in which the CPU operates autonomously except for interruptions to deliver status reports.

On a data transmission the sequence operates in reverse. The I/O control applies the data byte to gate the appropriate baseband signals. After the transmit circuits have stabilized, the I/O transmits a key, followed by the data byte.

4. Analog Subsystem

The analog subsystem is comprised of the baseband signal processing circuits and the monolithic voltage converters.

The baseband signal has a single channel of 100 kHz bandwidth which delivers an 8-bit digital code using amplitude-shift keying (ASK) modulation. The eight discrete tones are spaced equidistant on a logarithmic scale as shown in Fig. 6. Each tone has a maximum strength of 0.55 V, and a level of 0.11 V is the threshold for detection in the receive path.

The RF signal is processed by two complementary circuits. On the receive path the analog-digital translation is performed by a frequency-voltage conversion (FVC) unit. Similarly, on the transmit path, a voltage-frequency converter (VFC) is used to transform a digital byte of data to its frequency representation.

The choice of ASK modulation simplifies the FVC design. Instead of sampling a multi-level input, an envelope detector can be used to determine the presence or absence of a sinusoidal signal. In this IC, a dual-envelope detector has been designed to decrease the settling time by detecting positive and negative swings of the input sinusoid. Figure 7 shows the schematic of a dual-envelope detector. The FVC is implemented as eight separate paths each tuned to a specific data-tone frequency. Within a path the baseband signal is first filtered through a narrow bandpass filter to remove adjacent tones.

The VFC works in reverse, by summing eight transmit paths, each tuned to a specific frequency. Analog ring oscillators generate the signals, and the digital data to be transmitted is used to select the data using complementary transmission gates.

The on-chip power management unit, shown in Fig. 8, performs two essential functions. First, it regulates the external supply voltage to minimize ripple or distortion. Since this IC is intended for low-power embedded or remote applications, external power would typically be supplied by batteries or solar cells. Power regulation offsets the voltage droop which is characteristic of battery power.

A second function is noise isolation. Since separate supplies are provided for the analog/RF and digital sections, the noise introduced on the supply line by rapid digital switching does not perturb analog biasing. Likewise, regulation can be individually optimized in each subsystem.

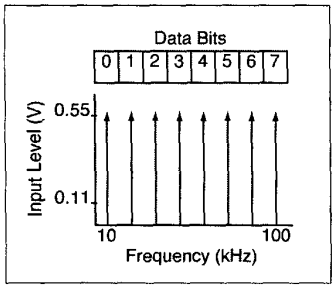


Figure 6 Frequency distribution of the baseband signal.

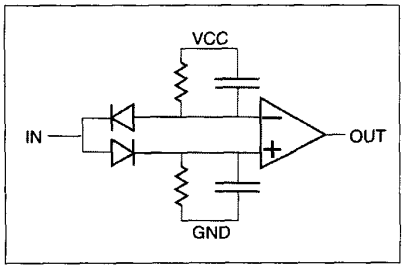


Figure 7 Dual envelope detector used in the FVC.

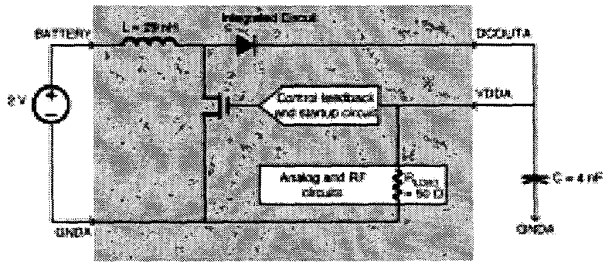


Figure 8 Circuit schematic of the DC-DC voltage converter [1].

5. RF SUBSYSTEM

The RF subsystem is comprised of a 400 MHz zero-IF transceiver which translates a 100 kHz bandwidth baseband signal using a 400.1 MHz local oscillator signal. A monodyne architecture was selected to minimize the component count by eliminating the additional filtering and mixing necessary for a heterodyne architecture. Also, since the carrier frequency is 400 MHz and the digital processing occurs at 33 MHz, a frequency translation to an intermediate frequency is unnecessary. The signal has a single channel of 100 kHz bandwidth which delivers an 8-bit digital code using amplitude-shift keying (ASK) modulation. A block diagram is shown in Fig. 9.

The mixers are a double-balanced design to cancel out common-mode DC biasing signals and offset the non-linear dependence of the MOSFET gain on the drain bias. A single-to-differential converter generates two out-of-phase signals. The local oscillator signal is fed through a similar converter. Figure 10 shows the schematic of the downmixer. This topology is very amenable to monolithic integration with digital logic for baseband processing.

Figure 11 is the frequency harmonics after down mixing a 50 kHz signal, showing acceptable distortion levels. Distortion in the mixer output is not viewed as critical to our application since the ASK modulation is insensitive to minor phase distortion, and the signal detection circuits require only threshold detection and not absolute values.

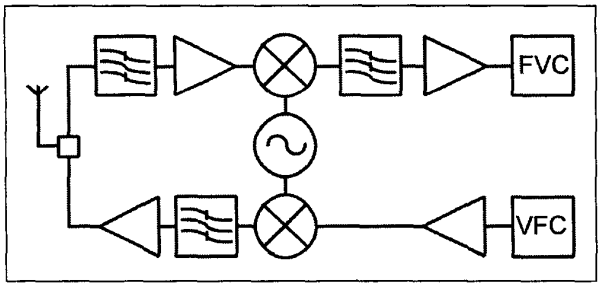


Figure 9 RF transceiver block diagram.

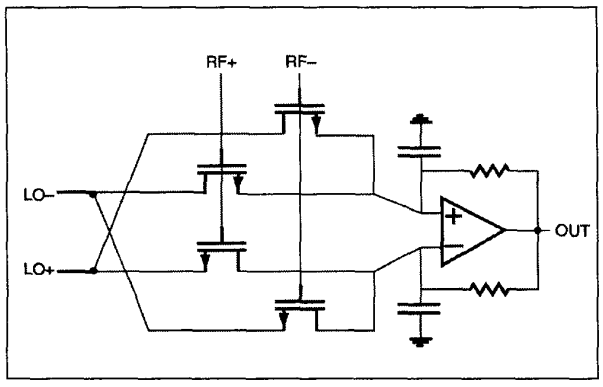


Figure 10 Down-mixer circuit schematic.

Filters are required both in the transceiver signal paths and in the baseband signal processing. The low-pass filter is a simple three-stage Friend circuit and is not discussed further. The bandpass filter design was more challenging because of the low gain provided by the operational amplifiers at frequencies above the carrier frequency. Conventional analysis assuming ideal opamp characteristics did not match with simulated results and steep rolloff could be obtained only at the expense of severe attenuation in the passband. Additional stages to restore signal levels tended to further limit the frequency response.

The final bandpass filter design was tuned through extensive simulation to match the channel center frequency and provide maximum attenuation of outside frequencies. Figure 12 shows the final bandpass filter characteristics. As indicated, the center frequency nearly matches the desired 400 MHz, but the 3 dB bandwidth far exceeds the nominal 100 kHz. Submicron CMOS filters have shown better response [3-5].

In an ideal receiver, each path will experience either the total absence of a signal, or the presence of a single frequency. Distortion in the downmixer introduces some adjacent-channel interference, but the data tone spacing is sufficiently wide that the bandpass filter of a single path in the FVC can reject adjacent tones.

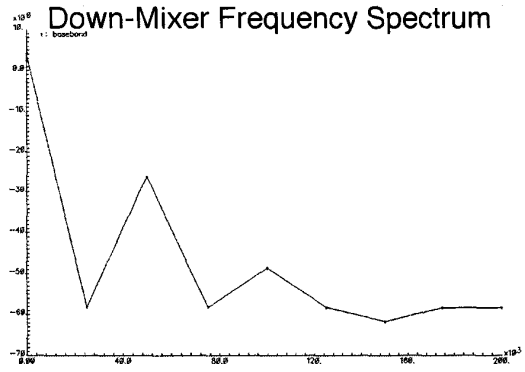


Figure 11 Harmonics of the downmixed signal.

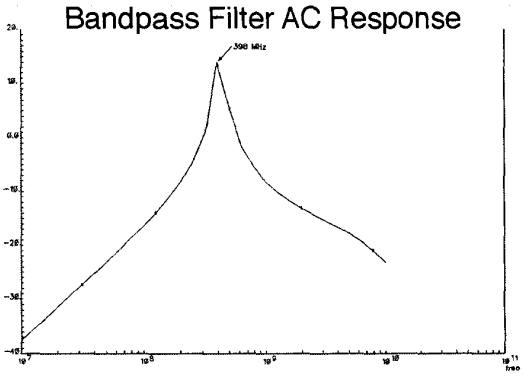


Figure 12 Bandpass filter characteristics.

6. TESTABILITY

A major challenge in verification of mixed-signal VLSICs is real-time testing of analog and digital subsystems. Digital switch-level logic is amenable to exhaustive testing through standard scan techniques, but this approach is insufficient for dynamic analog circuits [6,7]. Also, scan techniques may fail to identify dynamic timing hazards which appear only during continuous operation. Although analog testing buses have been developed, they do not readily permit access to individual subsystems or do not sufficiently integrate surrounding digital logic [8].

Testability of the entire IC is provided in three different formats. First the feedback path of the DC-DC converters is accessible through the external jumper. Second the entire digital subsystem is visible using a scan path network. Finally, a switch matrix is embedded which allows highly flexible transitions between fully functional and test modes.

Core digital functional testability is provided by a 152-bit FIFO (first-in first-out) serial scan path (from pins SCANIN to SCANOUT) controlled by an enable pin and a clock (using pins SCANEN and SCANCLK) joining all internal data registers, address registers, and state-machine variables, including all interrupt flags.

The complete controllability and observability of the scan path guarantees full static testability of the sequential logic. Only partial test of state machines (SMs) is possible since not all SM inputs are available to the scan path; however, since the internal state variables are visible, the state activity can be monitored and adjusted during dynamic testing. By decoupling the scan clock and operating clock, scan data can be inserted and reviewed at any time during continuous operation.

The mixed-signal testability architecture consists of a switch matrix embedded within the functional VLSI architecture (see Fig. 13). The multi-purpose internal buses serve dual roles for testability and continuous circuit operation. Partitioning of the systems for test is defined by external control of IC pins (viz. pins TESTC1, TESTC2, TESTC3, and TESTM) which configure the internal switch matrix. Table I lists the possible test configurations and pin settings. In the various dynamic test modes, the transceiver can be tapped at several locations: (in the receiver) before and after the down-mixer and prior to baseband signal recovery, and (in the transmitter) after baseband signal generation and after the up-mixer. Pins TESTC1, TESTC2, and TESTC3 can be ganged together or applied individually.

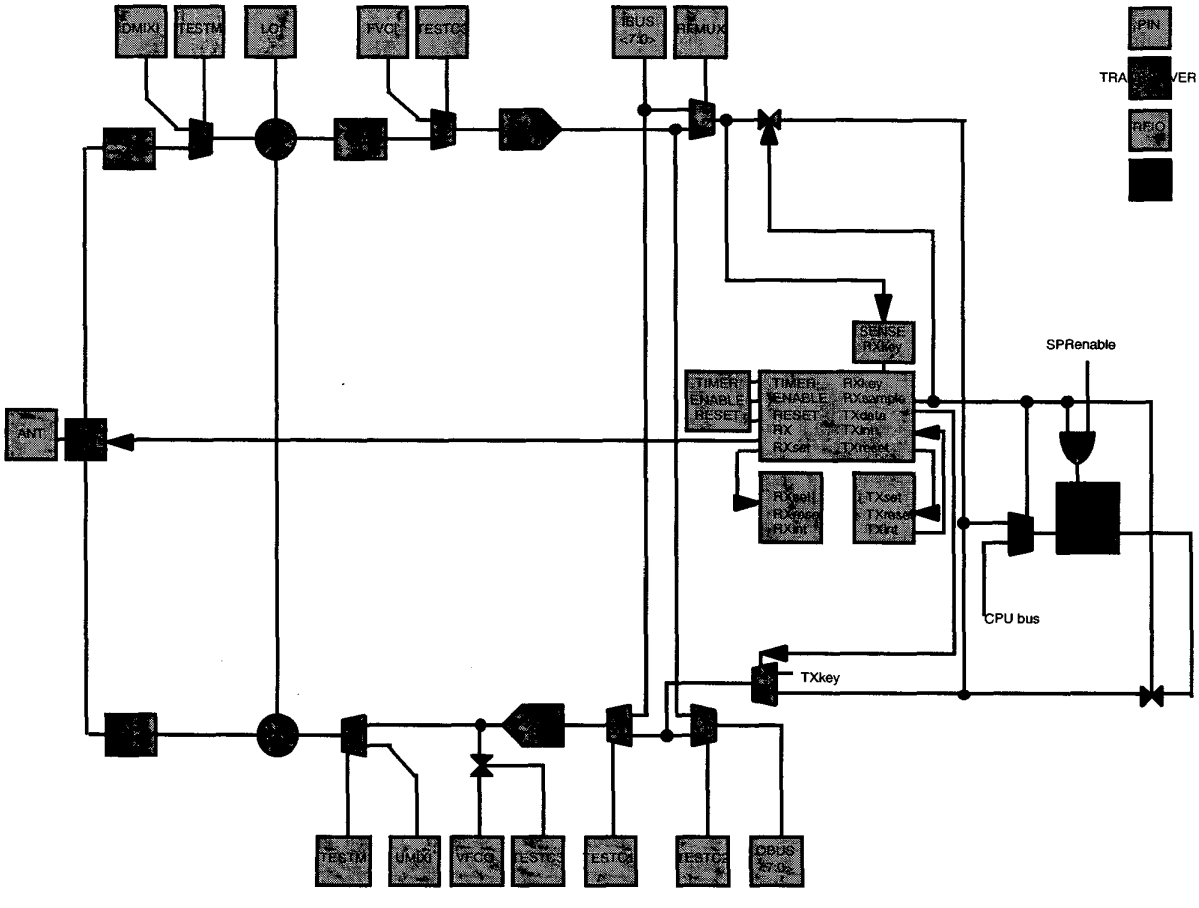


Figure 13 Testability block diagram.

Table I RF/analog test pin settings and configurations.

Function #	RFMUX	TESTC(1-3)	TESTM	Operation
1	don't care	0	0	• Normal system operation
2	don't care	0	1	• Test DMIX: apply input to DMIXI with no output detection • Test UMIX: apply input to UMIXI and detect output at antenna (Note: must also set antenna direction to output by scan path.)
3	don't care	1	0	• Test FVC: apply input to FVCI and detect output at OBUS<7:0> • Test VFC: apply input to IBUS<7:0> and detect output at VFCO
4	don't care	1	1	• Test UMIX: apply input to UMIXI and detect output at antenna (Note: must also set antenna direction to output by scan path.) • Test FVC: apply input to FVCI and detect output at OBUS<7:0> • Test VFC: apply input to IBUS<7:0> and detect output at VFCO

In mixed dynamic and static test, real-time execution can be halted to view or edit internal elements of the scan path; following the scan operations real-time execution is resumed. This technique of breakpointing can verify that internal states have responded correctly to dynamic events. Logic states can also be preset statically through the scan path to artificially induce desired responses upon return to continuous test. Mixed-mode testing can be used to verify operation of interrupt handling between the CPU and the memory or RF/I/O subsystems.

A multi-purpose internal bus can either perform according to its functional specification or provide a stimulus/response path to IC pins. Reuse of internal buses reduces layout dimensions by eliminating dedicated test routing, and it allows measurement of bus characteristics by injecting signals or monitoring bus outputs. For RF test, RFMUX can be set high or low. In standard (test) mode data "received" by RF I/O is provided by the FVC (external bus). Data sent for RF transmission is always mirrored to a second external bus. External buses can be used for test or sent to an external bus controller (e.g. I2C) for wired communication.

7. Conclusions

The RF microsystem has been implemented on the 0.25-micron SOI CMOS process of MIT/Lincoln Laboratory and is currently undergoing testing. Intended primarily for ultra-low-power digital logic, employing supply voltages of less than 2 V, the MIT/LL FDSOI process is not well characterized for analog and high-frequency (RF) performance. This architecture will help identify signal integrity troubles. Table II gives some IC details.

A full-CMOS implementation of this architecture has been designed. Although individual circuits could benefit from specialized processes, CMOS is the most cost-effective fabrication technology for monolithic systems due to its predominance in digital applications and emerging systems-on-a-chip architectures, of which this chip is an example. Since the selected foundry process is intended for digital applications, some modified structures were designed, including diode-connected MOSFETs for biasing and spiral inductors for mixing and power conversion.

Table II IC specifications.

0.25 μm SOI CMOS, mesa-isolated process
1-layer polysilicon, 3-layer metal
IC dimensions: 2.2 mm x 2.2 mm
IC transistor count: ~18,000

Passive structures are realized in several ways. For capacitors, the intrinsic gate capacitance of a MOSFET structure is employed. The only limitation is the area necessary to produce large-valued capacitances, as seen in the large areas of the power supplies. Resistors were a similar challenge. Unlike precision RF or analog processes which rely on discrete components or laser-trimmed elements, our implementation called for monolithic solutions requiring no additional processing steps or special handling. Several implementations resulted, including polysilicon resistors, switched capacitors, and diffused resistors.

The low-voltage technology also demonstrated that future monolithic systems may have to compromise low-power digital operation to maintain a suitable dynamic range for analog circuits, if a conventional process flow is followed. Alternatively, using split die in which separate regions are uniquely optimized for analog or digital characteristics, performance can be enhanced at the expense of process complexity.

The collaborative design effort between UIC and JPL is encouraging in that universities can contribute intellectually to aerospace applications which will maintain NASA's mandate of low-cost space missions. Conversely, through this type of interaction, NASA and its centers will capture the attention of university researchers and graduate students to build interest in aerospace careers and technologies.

Acknowledgments

This work was in part performed at the Center for Integrated Space Microsystems, Jet Propulsion Laboratory, California Institute of Technology. This was sponsored by the National Aeronautics and Space Administration.

REFERENCES

[1] M. Trivedi and K. Shenai, "A Monolithic DC to DC Converter," U.S. Patent #5,959,439, Sep. 1999.

[2] M. Motomura, T. Inoue, H. Yamada, and A. Konagaya, "Cache-Processor Coupling: A Fast and Wide On-Chip Data Cache Design," *IEEE J. Solid-State Circuits*, vol. 30, no. 4, pp. 375-381, April 1995.

[3] C.-Y. Wu and S.-Y. Hsiao, "The Design of a 3-V 900-MHz CMOS Bandpass Amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 159-167, February 1997.

[4] D. Shen, C.-M. Hwang, B. Lusignan, and B. Wooley, "A 900-MHz RF Front-End with Integrated Discrete-Time Filtering," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1945-1953, December 1996.

[5] E. Abou-Allam, E. I. El-Masry, and T. Manku, "CMOS Front-End Amplifier with On-Chip Tuning," in *IEEE Int'l. Symp. on Circuits and Systems*, pp. 148-151, 1996.

[6] J. Verfaillie, "A General-Purpose Design-for-Test Methodology at the Analog-Digital Boundary of Mixed-Signal VLSI," *J. Electronic Testing: Theory and Applications*, vol. 9, no. 1-2, pp. 109-115, 1996.

[7] J. M. Dasilva *et al*, "Mixed Current/Voltage Observation Towards Effective Testing of Analog and Mixed-Signal Circuits," *J. Electronic Testing: Theory and Applications*, vol. 9, no. 1-2, pp. 75-88, 1996.

[8] A. Cron, "A D-and-T Special Report—P1149.4 Mixed-Signal Test Bus," *IEEE Design and Test of Computers*, vol. 13, no. 3, pp. 98-101, 1996.

Erik A. McShane is a PhD student at the University of Illinois at Chicago. His dissertation research is on low-power mixed-signal circuits and embedded memory design. He has been employed at the Jet Propulsion Laboratory for two summers as an engineering intern to perform microavionics development at the JPL Center for Integrated Space Microsystems (CISM). He has published over 10 papers in this field and has seven patents pending office action. He is a UIC University Fellow. He received his BSCompE from the University of Illinois at Urbana-Champaign.

Krishna Shenai is a Professor of EECS at the University of Illinois at Chicago. He is the Director of the Microsystems Research Center and the Power Electronics Research Laboratory. His current interests are in low-power monolithic systems development and nanosatellite technology. He has over 10 years of industry experience in research and development capacities at such companies as Intel, COMSAT, and GE Corporate R&D. He has authored over 100 journal papers and has 10 awarded patents. He is a Senior Member of IEEE and recipient of the UIC University Scholar Award. He received his PhD in EE from Stanford University.

Brent Blaes received the B.S. and M.E. degrees in Electrical Engineering from California State Polytechnic University, Pomona, in 1977 and 1979 respectively. He has been with JPL since 1977 where his work involved the design, test and characterization of high-reliability integrated circuits and test chips. He has worked extensively in the development of test circuits, sensors and measurements techniques for measuring and characterizing total dose and SEU effects of CMOS circuits. He has also been involved in the design of custom CMOS chips and support circuitry for a number flight experiments (CRRES, MSX, STRV, RRELAX-Clementine, MAPEX-, MOX-Mars Lander). He was the chief designer of the Radiation and Reliability Assurance Experiment which has flown on the Clementine-I spacecraft and the cognizant engineer and designer of the Free Flying Magnetometer (FFM) data system. He has five patents, four involving radiation detectors and characterization techniques and one on a technique for measuring on-chip delays of integrated circuit devices.