COB and COC for Low Cost and High Density Package

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1. INTRODUCTION

Today, portable electronic devices have many more functions than the same type of non portable products had a few years ago. As the similitude rules are no longer valid when designers are faced with miniaturization, it is necessary to find and develop new approaches for the packaging and the interconnections of the integrated circuits. By using a well mastered Chip-On-Board (COB) technology (Fig. 1) in association with a very accurate die attach process, it is possible to offer an inexpensive Chip-On-Chip (COC) solution to the engineers who need a 3-D assembly for a higher level of miniaturization.

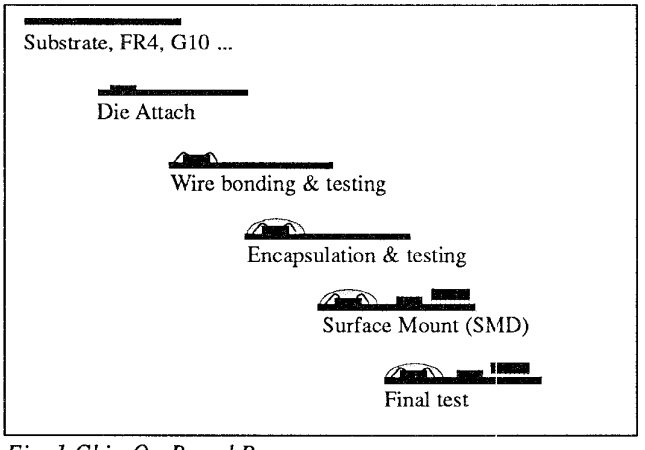

Fig. 1 Chip-On-Board Process

2. THE COC CONCEPT

The main idea is to use the 3-D configuration when the available surface is not sufficient to accommodate all the necessary components. In the COB technology, the dies are directly bonded to a Printed Circuit Board (PCB), electrically connected with bonding wires and then over-coated with a glob-op epoxy. This technology exists since at least 20 years, but can be used for assembling large ICs with high reliability only since a few years.

The COC represents one more step into the COB process and it consists of assembling two ICs, one upon the other, using the COB technology. In order to obtain the requested high yield and high reliability, this step of the process must be controlled carefully. The deposition of the glue for the attachment of the top die as well as its placement must be perfectly controlled to ensure its flatness and to guaranty that no particle of silicon or other foreign matter between the two ICs will damage the bottom IC. A clean room environment is necessary for these operations. Finally, the glob top protective resin is applied taking into account the various levels of ICs and bonding in such a way to keep its volume as small as possible.

This concept can be applied whenever two ICs of different dimensions (surfaces in a ratio of approximately 1:2) have their connections in common or close to one another in the set-up diagram. During the assembling, connections between both ICs and the PCB are also possible.

3. THE STRESS FACTOR

The bottom IC passivation specifications are very critical and must be properly defined i.e. type, thickness and hardness. The choice of the insulating glue or die attach glue for the top IC is also very important, i.e. viscosity, coefficient of expansion (TCE) and curing temperature. During the assembly process, the different components (ICs, PCB, glob top resin, die attach glues, etc.) will go through several curing cycles. In such a structure, we have to consider at least four important mechanical stresses : polymerization stress during the glob top coating, thermomechanical stress during the cooling after polymerization, thermomechanical stress during the curing of the top die attachment and thermomechanical stress during Surface Mounted Device (SMD) soldering. In order to guaranty a high reliability, we must know the exact distribution and magnitude of stress during these assembly steps to ensure that the mechanical strengths of epoxy, silicon and bonding wires are not exceeded. Even more critical, could be the effects of the stress generated by the attachment of the top IC on the bottom one, i.e. the possible shift of the frequency of an oscillator.

3.1 Simulation and stress analysis

In order to define the best possible conditions for the COC assembly, we are working with a stress analysis method that we developed to do the same work for the COB assembly. (1) The basic conditions we observe for the COB are identical for the COC (Fig. 2) and we find that the polymerization stress can be as high as 25% of the final stress after cooling. But, we also show that the polymerization stress in the resin increases with the square of the resin thickness and the COC configuration needs a larger amount of resin than just one die for the COB assembly. The use of the program ANSYS (2) which is based on the Finite Element Method (FEM) allows us to calculate thermomechanical stresses in a COB structure. As with our other works, we already have a good idea of the thermome-

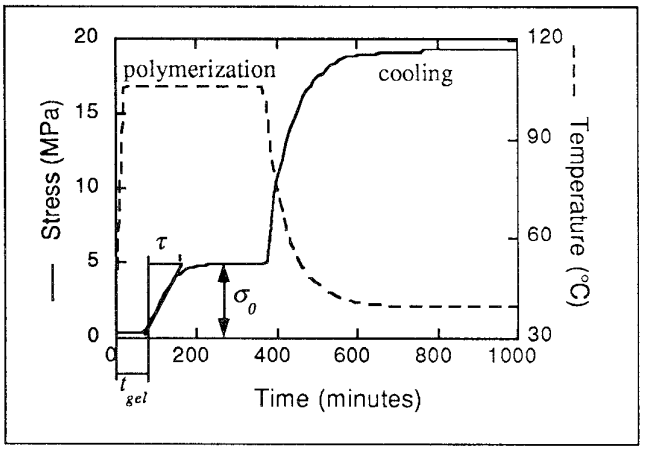

Fig. 2 Temperature and normal stress during polymerization

chanical stresses in a COB structure, we are more interested by the kind of stress the top die could create into the bottom die, without and with the glob top resin (Fig. 3). As we did several simulations, we are taking into account the following variables, i.e. :

1. Thickness of the attachment glue between the two ICs
2. Type of the attachment glue between the two ICs
3. Type of the glob top epoxy
4. Variation of the temperature.

From our simulations, we are getting graphics and values of the stress into different axes in MPa. Our previous works (1) show a very good correlation between simulation and practical experiences, so we are conducting only a limited number of practical experiences. We are simulating the stress values, compression and traction, into the PCB, the bottom die, the attachment glue of the top die and the glob top resin. Our previous studies of the COB are showing that the stress values above 50 MPa are dangerous for the integrity of the packaging.

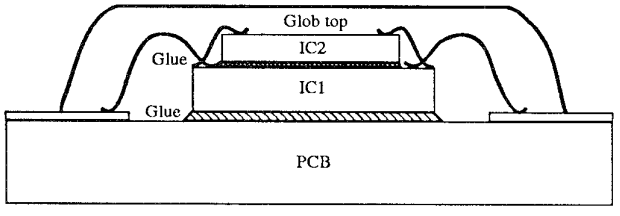

Fig. 3 Exemple of COC structure

3.2 The main results

For the simulation presented below we are working with the following variables, i.e. :

. Type of attachment glue : H70S (TCE 70 ppm)
H70E (TCE 20 ppm)

. Thickness of attachment glue: 50 µm (10^{-6}m)
100 µm
200 µm

. Variation of temperature : 60°C
100°C
200°C

We are getting the main results on two different forms, i.e. : one is an array of the main values (Fig. 4) and the second one is a graphic (Fig. 5). From all these arrays and graphics we are able to obtain the main indications for the first approach of the COC.

		SX	SY	SZ	SIGE
PCB	max	21.89	28.05	44.127	41.58
	min	-4.97	-8.94	-12.179	0.71
IC	max	47.39	55.53*	28.68	131.37
	min	-78.66	-115.725*	-12.33	13.8
Glue	max	71.96	71.66	5.59	101.75
	min	55.92	55.108	-15.23	65.148

* on the same IC

Fig. 4 Distribution of the max and min constrains (MPa)

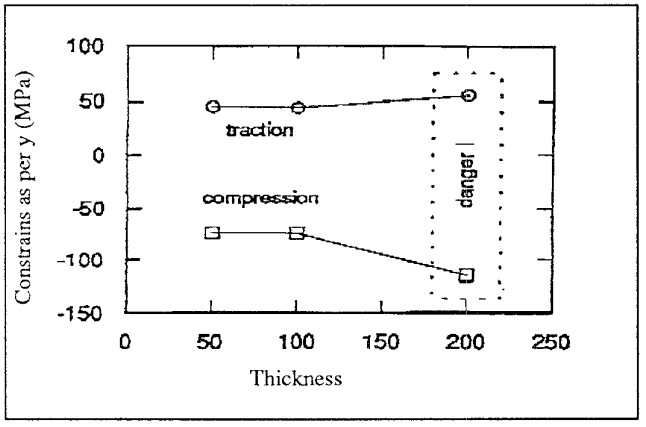

Fig. 5 Constrains as per y axys on the bottom die

Regarding the thickness of the attachment glue, the minimum stress is obtain with 100 µm, as the traction and the compression stress are increasing with the thickness of the glue. This result is more distinct with the H70S, even without variation of the temperature. With a thickness of 200 µm, the Xs in the bottom die could be as high as 159 MPa with a major risk to strongly put the integrity of this die in danger. As we also could imagine, the stress is increasing with the temperature and is creating very dangerous levels of stress in all components, as soon as the temperature is above 150°C. This phenomena is more dangerous with the glue H70S (TCE 70 ppm) than with the H70E (20ppm). During the COC process, we could easily maintain the temperature below 150°C, but it is not possible if we also have to assemble SMD components on the same module. In this case and in order to avoid inducing too much stress into the die, it will be better to assemble the SMD components before the COC.

To complete the first analysis, we also made a few simulations

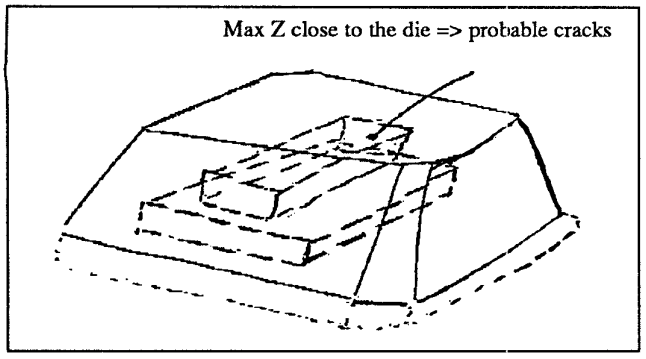

Fig. 6 The COC with the glob top resin

to compute the level of stress caused by the glob top resin (Fig. 6). For the simulation, we are using the H70E (TCE 20 ppm) glue, the EO1016 epoxy resin (TCE 46 ppm at 20°C and 140 ppm at 140°C) and the temperature ranges from 140°C to 20°C (120°C)) the main results are showing a very high level of Sy inside the die and also a very high Sz inside the resin, close to the top die. Based on our experience with COB, we could stay that the above stress inside the die will threaten its integrity and the one inside the glob top will create cracks and strongly decrease the efficiency of the protection.

4. CONCLUSION

The COC is a very attractive packaging technology that could be used when a very high silicon density is necessary and the third dimension (Z axes) is offering some room (fig. 7). However, to guaranty the integrity and the reliability of this kind of package, the choice of the main variables is very important, i.e. the type of attachment glue, its thickness and the glob top resin. However, these variables must be defined for each new configuration, our experiences showing that, i.e., the glue with lower TCE is not always giving the best results. For this reason, we are recommending to simulate each new configuration to obtain an acceptable yield during the manufacturing of the modules using the COC package. Also, there are at least two important parameters that we didn't include into our analysis : the passivation of the surface of the bottom die and the viscosity of the glue. Today, as we are working very carefully and with a slower speed than with the COB, we are already getting good results with the COC as we assemble several tens of thousand packages of this type each month. As we are conducting more stress simulations and practical analyses, we are continually improving the yield of the COC package and we are confident that we will able to reach the typical 98% yield of the COB package.

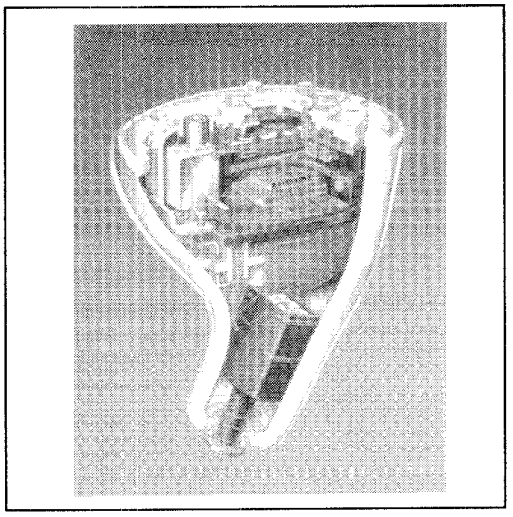

Fig. 7 Medical application of the COC package (Source Phonak CH-Stäfa)

References :

1) Stress analysis and reliability of Chip-On-Board encapsulation technology, P. Sarbach, L. Guerin, A. Weber, Ph. Clot 1993 IEEE IEMT Symposium.

2) ANSYS User's Manual, Swanson Analysis Systems Inc., Houston Pa. (1989).