COMPACT CSC ACQUISITION SYSTEM: VXI D-size Modules with a DSP Interface

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Abstract

A complete electronics system has been developed, from the preamplifiers up to the readout and control interface, for the cathode strip chambers of the BBS spectrometer. The system is based on application specifics D-size VXI modules. The size of electronics has been reduced by the use of small surface mounted daughter boards. Flat topped-pulse is produced with a new time-variant filter. In all modules, ADCs 16-bit and FIFO memory are followed by a Digital Signal Processor, which performs data filtering and cathode induced charge interpolation. Good analog noise performance is obtained in multi-processor environment.

I. INTRODUCTION

For the light-ion detection system of the Big-Bite Spectrometer [8] at KVI, Groningen, The Netherlands, we have designed the front-end electronics, trigger and data acquisition system. The basic requirement to the system is localization and identification of particles from 200MeV protons up to 30MeV/nucleon ^{20}Ne. The detector consists of two position sensitive Cathode Strip Chambers (CSC), each has 2 localization layers U-V inclined 45° (active surface 97x25cm^2, anode plane made of gold-plated tungsten wires 12μ in diameter and distant 1.6mm, cathode plane made of Au-plated 6.4 mm strips, anode-cathode gap 6mm) and a set of two scintillator layers used for triggering and particle identification.

The cathode strip chamber provides high precision position measurement and performance stability achieved by the geometrical position of the strips. However, it demands large number of channels for charge measurement of each strip. The intrinsic spatial resolution of a CSC depends on the physical processes in the gas, but it can be limited by the electronic noise in the charge measurement. The position error due to electronic noise is given by:

$$\sigma_e = K \cdot w \frac{\sigma_q}{Q_t} \qquad (1)$$

where w is the strip width, σ_q is the rms error in the charge measurement per strip, Q_t is the total charge, and K is the constant (between 2 and 3 [9]) which depends on centroid-finding algorithm. The expression (1) determines the choice and the quality of the applied electronics.

This paper presents the design of a compact, high-performance CSC readout system based on custom built VXI modules. To accelerate the data flux, a digital signal processor (DSP) is included on each module.

II. OVERVIEW OF THE READOUT SYSTEM

The system's overview is presented in Fig. 1. Cathode charge and anode voltage preamplifiers are placed on the printed circuit board of the detector. A VXI rack, distant 4m, contains 6 custom modules: four 64-ch Cathode modules, Photomultiplier & 1st level trigger, and Anode & Master trigger. Slot 0 and VIC are commercial embedded VXI and VME modules.

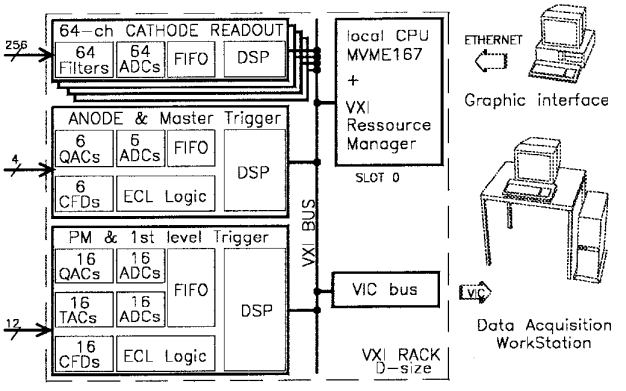

Fig. 1 Block diagram of the compact CSC acquisition system based on custom VXI D-size modules.

III. CATHODE READOUT

A. Position finding method

The cathode strip chamber is a multiwire proportional chamber with segmented cathode readout. The position is determined by interpolating the induced charge on the cathode strips. The readout of every second strip reduces the number of channels by factor of two (see Fig. 2). Capacitive charge division from intermediate cathode strips to adjacent readout strips improves position resolution and differential nonlinearity [1].

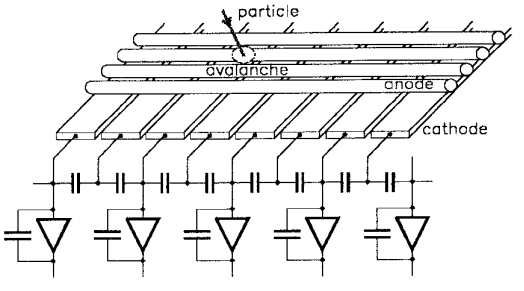

Fig. 2 Cathode Strip Chamber with capacitive charge division.

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B. Charge Preamplifiers

High gain and low noise charge-sensitive preamplifiers, on a surface-mounted daughter boards (27x18mm), are fixed on the printed circuit board of the detector. The gain of 2V/pC or 0.5V/pC can be selected by the VXI remote control. The equivalent noise charge is 340 electrons rms + 8 electrons per pF of input capacitance.

C. 64-channel VXI module

A custom VXI module (Fig. 3) accepts signals from all preamplifiers of one cathode layer. It contains 64 shaping amplifiers followed by 64 Analogue to Digital Converters (ADC), a serial to parallel converter, a FIFO derandomising buffer and a 32-bit DSP.

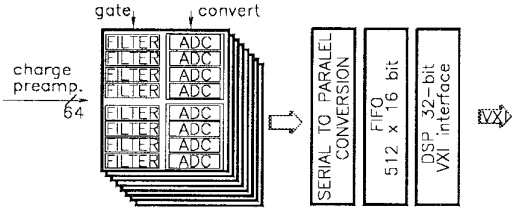

Fig. 3 Block diagram of the Cathode 64 channel VXI module.

A flat topped-pulse is produced by a new shaping amplifier which operates as a time-variant filter (see Fig. 4). To match the timing of the trigger, the input signal passes through a delay line of 250ns. The filter consists of Salen-Key active integrators with shaping time of 300 ns. The precision at high count rate is improved by Tail Cancellation Restorer (TCR) which is followed by a fast Track/Hold circuit.

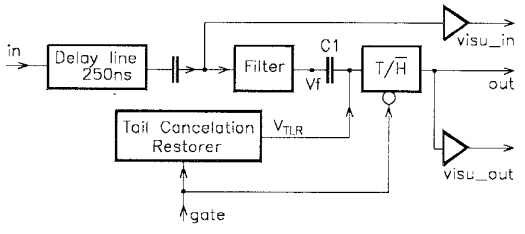

Fig. 4 Block diagram of the new shaping amplifier.

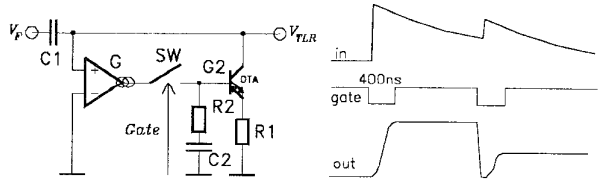

Fig. 5 Circuit diagram of the Tail Cancellation Restorer (TCR) and waveshapes corresponding to Fig. 4.

The Tail Cancellation Restorer (Fig. 5) is a gated base-line restorer of second degree, it restores not only the level but also the slope of the input signal (the input level is held in C1 and the input slope is held in C2). It makes possible to measure a pulse which is on the tail of another one. No pole/zero cancellation stage is necessary. The reason why this restorer has not been put before in practical use is that injected charge in C2 by the transition of the gate causes strong level shifts. For this critical design point we have used a new switch with charge injection of only 40 fC (Burr Brown SHC615).

The TCR response should be without ringing for optimal performance. Assuming switch SW closed and $G2 \cdot R1 >> 1$, the transfer function of the TCR circuit is given by

$$\frac{V_{TLR}}{V_F} = \frac{s^2}{s^2 + \frac{G \cdot R2}{R1 \cdot C1} \cdot s + \frac{G}{R1 \cdot C1 \cdot C2}} = \frac{s^2}{(s-\alpha_1)\cdot(s-\alpha_2)} \qquad (2)$$

where

$$\alpha_{1,2} = \frac{-G \cdot R2}{2 \cdot R1 \cdot C1} \pm \frac{\sqrt{G} \cdot \sqrt{G \cdot R2^2 \cdot C2 - 4 \cdot R1 \cdot C1}}{2 \cdot R1 \cdot C1 \cdot \sqrt{C2}} \quad . \qquad (3)$$

The time response to an exponential input of type

$$V_F = \frac{1}{s - 1/\tau_i}, \qquad (4)$$

plotted in the figure 6, shows that a pulse can be cancelled in 2 µs up to 0.01%.

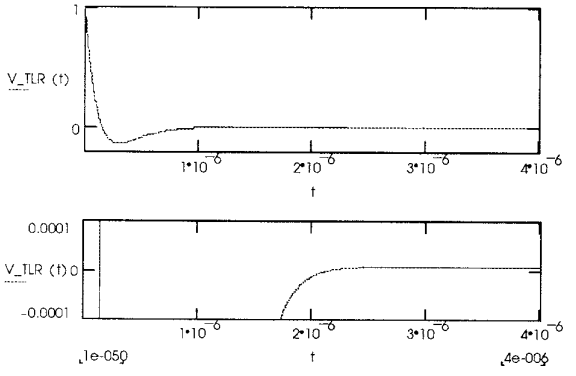

Fig. 6. Plot of the TCR response (C1,C2=1.5 nF, R1=500 Ω, R2=200 Ω, G =50 mA/V, τ_i=50µs).Time scale from 0 to 4µs. Zoom ±0.01 %.

This analyses is valid for small signals, without saturation of current sources. Large signals can be examined by SPICE simulation. As others types of restorers, the TCR can be optimized for low noise or for high-count rate. The oscillogram of the cathode processing channel is shown in Fig. 7.

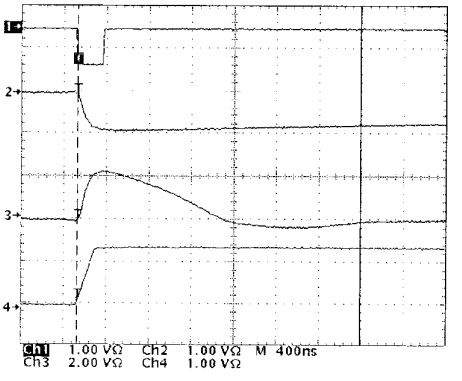

Fig. 7 Oscillogram of the signals: gate (1), output of the delay-line (2), TCR output (3), track & hold output (4), for large input signal.

The linear part can accept more than 10^5 gates/s. The track/hold circuit serves as analog memory stage and permits to convert only those events which are validated later by other external detectors.

The equivalent input noise charge of the complete linear chain, from charge preamplifier to ADC, is 650 electrons rms (with 10 pF at the preamplifier input), which corresponds to 0.2 mV rms at the ADC input (full range 2.5V). That allows the large dynamic range required to detect in the same experiment particles which deposed charge ratio is 40 to 1. The photograph of the shaping amplifier is shown in Fig. 8.

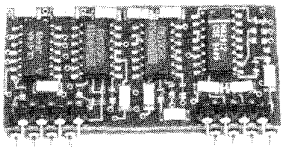

Fig.8 Photograph of the shaping amplifier daughter board (37x19mm).

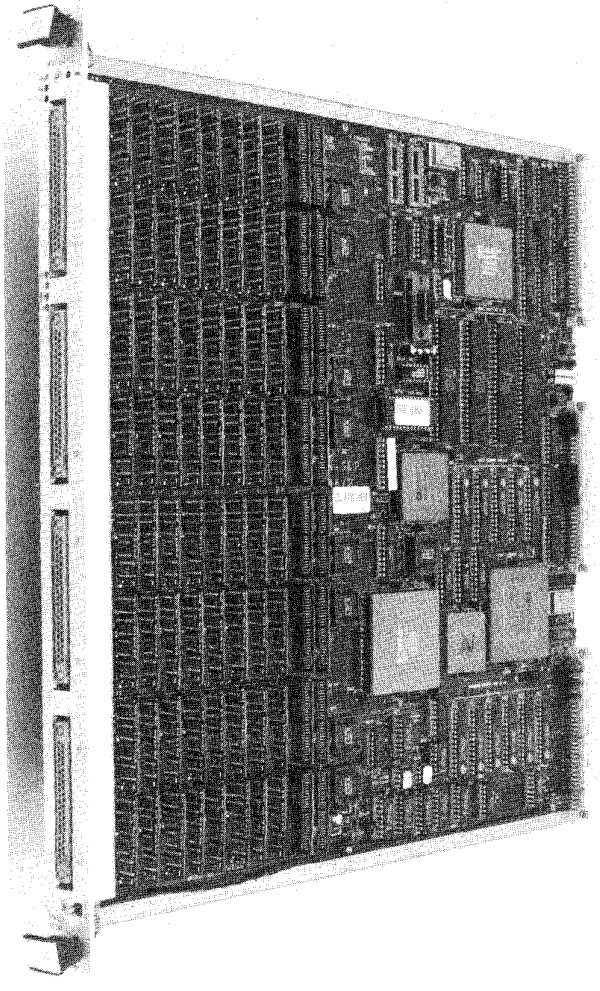

Fig. 9 Photograph of the Cathode VXI module which contains 64 shaping amplifiers, 64 ADCs, FIFO and a DSP interface.

The ADC is 18-bit PCM1750 serial output (16 bits of information are used). A special surface mounted daughter board (37x19mm), containing 4 ADCs, has been built. The conversion to parallel format is accomplished using a programmable logic cell array (XC4010) which deserialises all 64 channels of one module and generates the conversion sequence signals.

FIFO (First In First Out) derandomising buffer is provided in order to avoid excessive acquisition deadtime. In FIFO mode, the dead time is 10μs and corresponds to 5μs of ADC conversion plus 5μs of serial to parallel conversion.

The particle position in each CSC layer is calculated by an incorporated DSP using the center-of-gravity algorithm [6]. The execution time is 20 μs for pedestal subtraction, gain correction, maximum finding and center-of-gravity calculation on 5 strips. The event rate is so limited to around 3 x 10^4 convert/s.

Special care has been taken to the layout of the printed circuit board because of coexistence of high speed DSP system in the same card with high resolution converters. The photograph of the VXI module is shown in Fig. 9.

IV. ANODE READOUT

Fast shaping of the anode signal (50 ns) is done by a surface mounted voltage-sensitive preamplifier, which is placed on the printed circuit board of the detector. The same circuit provides the test injection input not only to itself, but also to all cathode preamplifiers by injected charge through the anode - cathode capacity.

The Anode & Master trigger module provides gating and timing of all VXI modules of the local system and communicates the triggering information. Two configuration modes are possible: independent and subsystem mode. In the independent mode the module is the Master of the system. In the subsystem mode, the module is a slave to an external trigger, for example EDEN [2], and waits for an external validation to start the AD conversion and for an external Reset to start a new event.

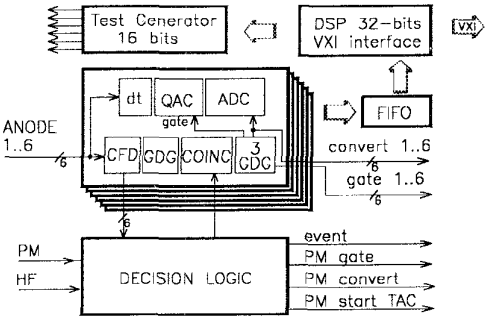

Fig. 10 Anode readout & 2nd level trigger VXI module.

The simplified block diagram of the VXI module is shown at Fig. 10. The output of each anode preamplifier is connected to a Constant Fraction Discriminator (CFD). The event is triggered by the coincidence of the PM signal and of all enabled anode inputs. In that moment the module generates the

"gate" signal to shape and hold all cathode charges, and produces a "event" signal to external trigger. The common TDC start is also provided for the PM VXI module. The dead time of this first level is 600 ns plus the time necessary for the external detector response. After the reception of the external validation, the module generates ADC "convert" signal.

Once the data have been stored in the FIFO, which is around 10 μs from the start of the event, all analog inputs can accept a new event. The DSP processing time depends on implemented algorithms of all modules. Each DSP can assert "reject event", in the first few μs, if it founds some of previously programmed rejection conditions. Otherwise, the cards are asserting "codage" on the VXI back plane. At the end of "codage", in independent mode, the module generates VME readout interrupt request (IRQ). The results are then ready in the double port memory of each module.

Charge to Amplitude Converters (QAC) followed by ADCs are incorporated to control the anode charges. The timings of all Gate and Delay Generators (GDG), the thresholds and the delays of the CFDs are controlled by software. Test signal, injected to the anode plane, permits the calibration of the cathode readout. The trigger, the amplitude, and the path of the precision pulser (16 bits, 6 outputs) are controlled by the DSP program.

V. PHOTOMULTIPLIER READOUT

Two scintillator layers are used for triggering and particle identification by time of flight and dE/dx measurements. The first layer consists of 4 and the second of 2 plastic scintillators. The light from each scintillator is send to 2 photomultiplier tubes (PMT) via a light guide.

Signals from each PMT are send to the custom VXI module. This module contains CFDs with Mean Timer, ADCs and TDCs. Inputs of ADCs and TDCs are delayed 250 ns, the time to match the "gate PM" and "start TAC" trigger signals. Fast ECL decision logic circuit generates a "PM" signal if one of authorized configurations has been detected.

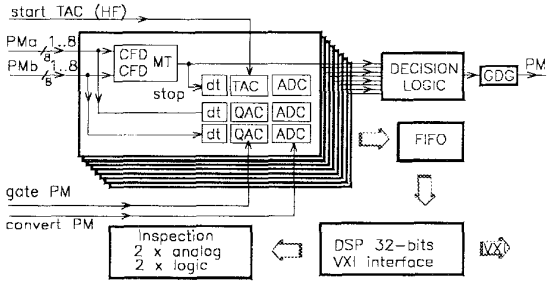

Fig. 11 Block diagram of the PhotoMultiplier readout & 1st level trigger VXI module.

The block diagram of the VXI module is shown in Fig. 11. All functions are realized as small daughter boards, except the Time to Amplitude Converter (TAC) which is a commercially available ASIC [10]. The CFD thresholds, delays, the width and the delay of the GAG and the configuration status of the decision logic are controlled by the software.

VI. DIGITAL SIGNAL PROCESSING

Digital Signal Processor (DSP) is processor optimized to execute fast multiply-accumulate instructions. For this project we have chosen the ADSP 21020. In 30 ns clock cycle it can execute 3 operations and perform 2 data access in 32-bit floating point.

The DSP of each module (Fig. 12) disposes of 64 Kwords of program and data memory. At power-up it is booted by associated 16-bit DSP (ADSP2111) which provides also the RS-232 interface (without the VXI environment a single card can be down-loaded and run by a PC), additional memory and further possibility to hold the event number in the case of FIFO pipeline mode of other sub-detectors. Card control registers, 8 x 16 bit = 128 decoded levels, connected to the DSP data bus, are realized in programmable logic cell array (XC4005H). A double access port memory of 1K x 32bit (IDT7130) connects local DSP data bus to VXI A24D32 bus. A protocol of the use of the double access port memory has been defined. This protocol covers the DSP reset, program down-loading, set up, controls and data acquisition. The DSP program of each module is assembled at PC and down-loaded via ethernet to the VXI rack.

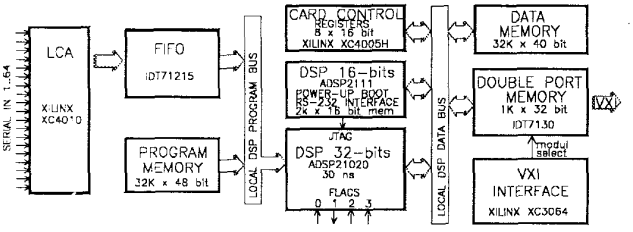

Fig. 12 Block diagram of the DSP configuration of each VXI card.

The DSP flags 3..0 are used to control the data acquisition. FIFO at the DSP input can derandomise up to 8 complete events. The FIFO full "FF" control signal is send to the master logic to extend the busy time. The FIFO empty flag "EF", connected to DSP Flag_in0, is used to start the DSP processing. If the DSP decides to reject the data, it asserts the "Flag_out1", which is connected to the master logic by the VXI STARY line. When the master logic decides to reject the event, it asserts TTLTRG5 "reject event" which is connected to Flag_in2 of each DSP. The double access port memory left flag "LF", connected to DSP Flag_in3, is used to indicate to the DSP the end of the VXI readout.

Acting as local control point for acquisition activity, the DSP of each card performs the following major functions:

(1) processes and filters the input data,
(2) detects some possible cases of event rejection, for example double - hit, saturation, zero event, out of window, etc..,
(3) communicates output data and status information to the VXI and executes the remote control,
(4) keeps track of the number of events, make local real-time control histograms, execute program controlled diagnostic sequences.

All DSPs of all cards process the data of the same event in parallel. The peak processing power contained in six ADSP 21020 is 1000 MFLOPS.

DSP controls, via card control registers, all VXI diagnostic and testing facilities [4,5]: ability to multiplex a lot of the internal signals, both analogue and digital, onto backplane inspection lines, where they can be examined at the front panel of the VXI slot 0. All internal voltages can be measured by a special line of the slot 0. Each card's internal temperature can be monitored for security control and real time gain compensation.

VII. DATA ACQUISITION HARDWARE

The VXI crate (Fig. 13) is controlled by MVME167 which is incorporated inside of the modular VXI Resource Manager (STRUCK STR8032, at slot 0), and run under the VxWorks operating system. The readout electronics is under the general control of workstation for setting up and local acquisition, with Ethernet as the control bus. PC provides the graphic interface (LabView) for diagnostic facilities. The crate is linked to the external readout system via the VICbus card which allows fast memory-mapped access.

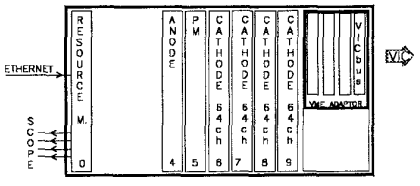

Fig. 13 VXI (D - size) crate.

VIII. RESULTS AND DISCUSSION

Tests during the 1995 with the chamber ¼ prototype [3] and with electronics previously described have approved good position resolution. The Fig. 14 shows X-ray absorption localisation for ^{55}Fe isotope source with a narrow collimator. It is difficult to estimate the contribution of the source to the total resolution of 120 μ.

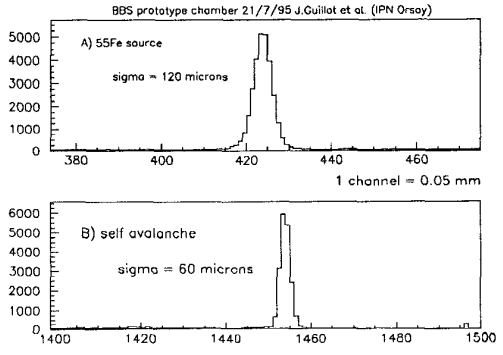

Fig. 14 X-ray absorption (up) and a self-avalanche (down) peak.

During the same measurement (1 count/second) a self avalanche peak has been observed. It has the same cathode charge distribution as the real one. The position resolution of 60μ is close to the intrinsic resolution of a CSC [7]. It indicates the negligible electronic noise contribution in spite of the cathode read-out pitch of 12.8 mm and multiprocessor environment.

IX. CONCLUSION

We have built a compact Cathode Strip Chamber data acquisition system based on custom VXI modules. All necessary electronics for 256 channel readout has been built in only a half of a D-size VXI rack. The rapid increase in microprocessor performance in the last few years permits now to insert a DSP at every VXI module to accelerate and to reduce the data flux. The complete set of modules will work with the BBS spectrometer at the end of 1995.

ACKNOWLEDGEMENTS

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