Development of a Low Cost, Fault Tolerant, and Highly Reliable Command and Data Handling Computer (Pulse™)

Michel Elias
Honeywell Commercial Systems Operation
13350 US 19 North
Clearwater, FL 33764-7290
mhelias@space.honeywell.com

Abstract-Traditionally, command and data handling computers have been designed to manage the different and many remote interface units within the satellite "bus" platform. In this distributed architecture, the command and data handling requires low throughput processors (1-4 Mips) to pass data to other units or for download to ground stations for further processing.

The advent of very large radiation hardened ASICs has enabled the application of powerful processing of the RHPPc (based on the Motorola licensed PowerPC 603e) with a simplified IEEE-1394 backplane bus to provide a highly reliable and cost competitive centralized command and data handling sub-system as shown in Figure 1 below. This robust architecture is tailorable and easily modified to meet the varying needs of the satellite and space transportation applications.

By using a commercially compliant processor (RHPPc is fully compliant with the instruction set of PowerPc 603e processor), software and its tools, which are one of the most complex, high risk, and expensive undertaking of the system architecture for a satellite bus controller, become a low risk design issue and much more cost effective. An extensive array of Commercial Off The Shelf (COTS) software tools is currently available for thePower PC processor family, rendering the software development environment associated with the Pulse™ to be a relatively low impact on the overall program thus, reducing the overall program recurring and non-recurring cost. The Pulse™ supports most of the COTS operating systems with the current Board Support Package (both basic and custom) being designed to be VxWorks compliant.

TABLE OF CONTENTS

1. INTRODUCTION

The Pulse™ command and data handling computer deploys very large radiation hardened ASIC technology needed for both GEO and LEO orbits with highly integrated components which support medium to high volume production for large constellations. The architecture incorporates industry standard interfaces including MIL-STD-1553B/1773 and IEEE-1394 (Firewire), *Super* EDAC algorithms that allow the use of soft DRAM (lower cost) without incurring the penalties associated with the high SEU rates, and a distributed power supply architecture.

The development of the Pulse™ is targeted toward the needs of the space community where radiation hardness, high reliability and fault tolerance, and low cost are required.

Figure 2 shows the block diagram of the dual redundant Pulse™ architecture. Figure 3 shows a triple redundant Pulse™ with three Single Board Computers (SBC) and five redundant Input/Output (I/O) modules.

2. ARCHITECTURE FEATURES

The Pulse™ architecture is based on a fault tolerant, highly redundant, highly reliable, yet low cost and low power topology. The architecture is designed to support up to four single board computers operating in parallel. A combination of software and hardware priority determination scheme is used to allocate which of the SBCs is in charge and which is a backup. Fault management and containment is handled autonomously by the SBC's while still providing full control for ground reconfiguration. The Pulse™ is architected to be modular by design and function. This is accomplished by a distributed power architecture, card edge I/O and SBC connectors, multi-drop backplane IEEE-1394 bus and a modularized I/O suite.

The Pulse™ architecture centers around Honeywell's radiation hardened Power PC 603e microprocessor. In addition, two support ASICs, the ECHO and HYDRA, have been designed to provide the necessary interfaces required for processor and I/O support. The ECHO ASIC, shown in

Figure 5, resides on each of the SBCs while the HYDRA ASIC, shown in Figure 8, resides on each of the I/O modules. The HYDRA ASIC provides the common I/O interface to the backplane as well as a 320C50 based embedded DSP used for I/O control within the Pulse™.

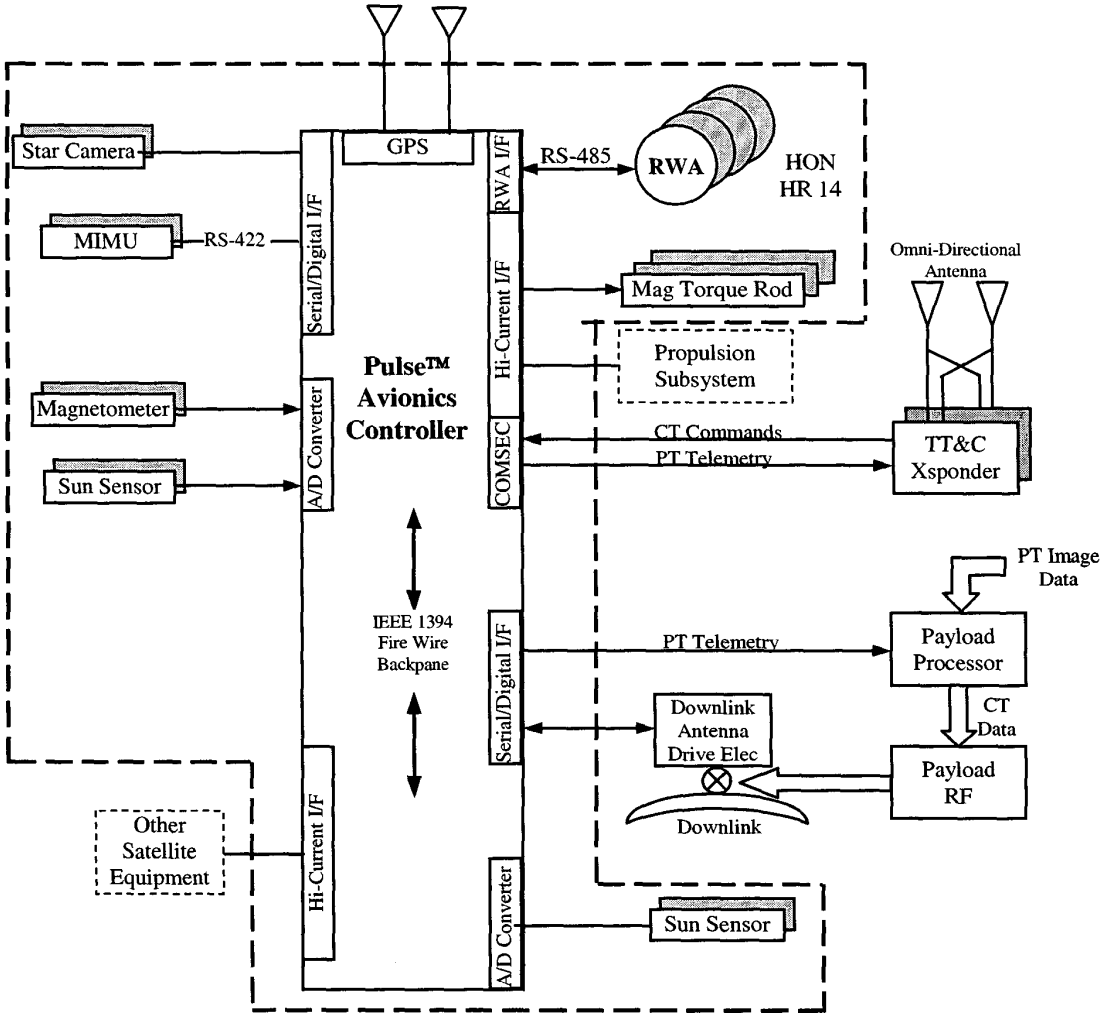

Figure 1 – Generic Satellite Bus System Architecture

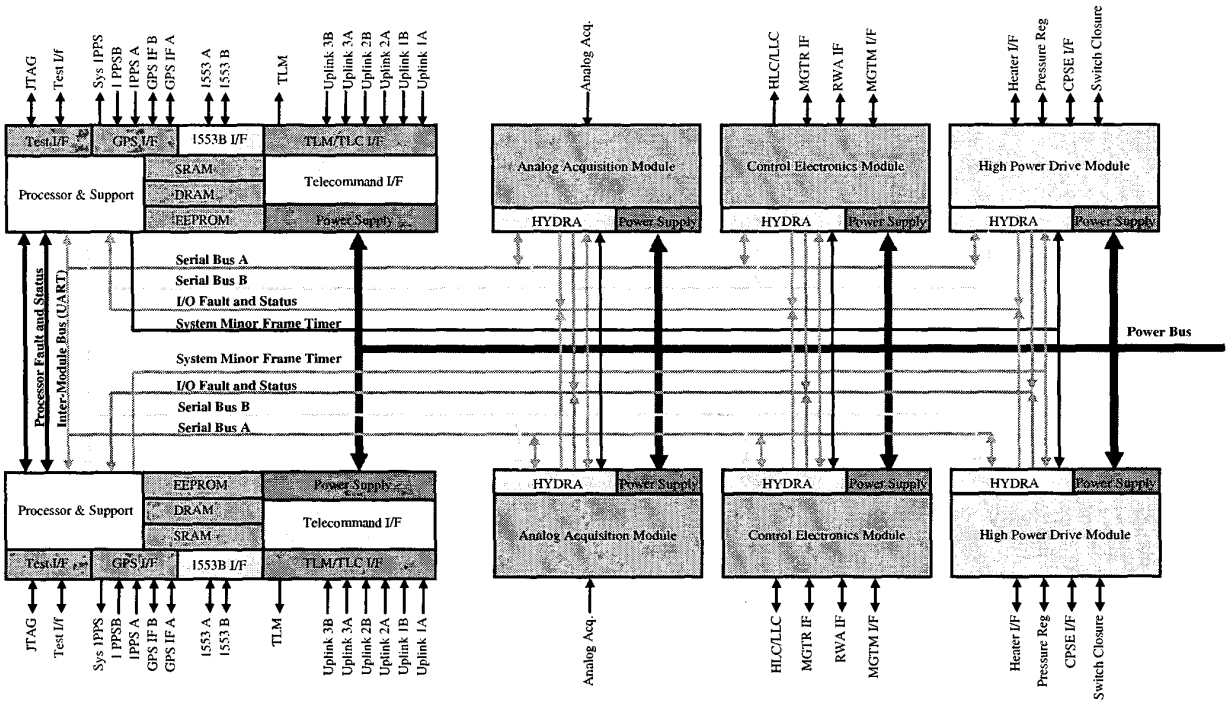

Figure 2 – Dual Redundant Pulse Block Diagram

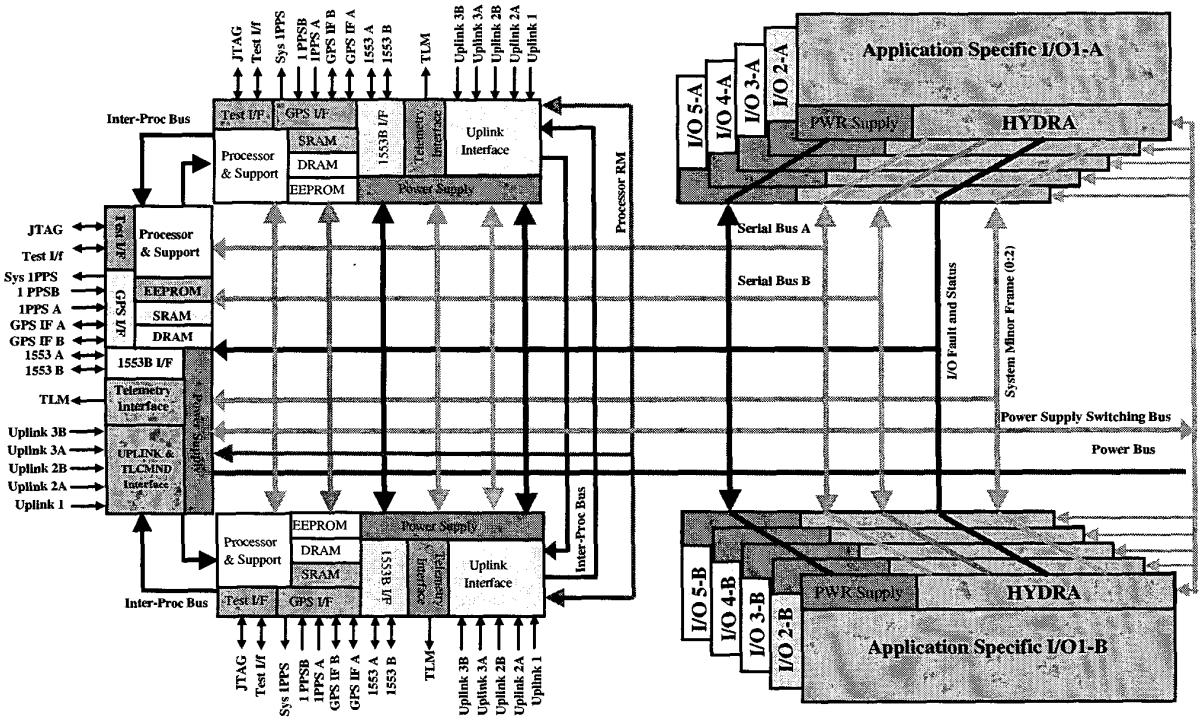

Figure 3 – Triple Redundant (SBC) Pulse Block Diagram

Inter-module communications within the Pulse™ is performed via the IEEE-1394 (Firewire) bus operating at speeds from 25 Mbps up to 100 Mbps based on the data bandwidth requirements of the specific application. The IEEE-1394 interface is fully compliant with the IEEE standard for a High Performance Serial Bus identified as IEEE-1394-1995. The Firewire interface has been implemented within both the ECHO and HYDRA ASICs in compliance with the Link layer, Transaction layer, and Backplane Physical layer. This backplane implementation provides excellent redundancy and fault management necessary for command and data handling units.

This versatile architecture is readily tailorable to meet the many different needs of both the low and high volume constellations and space transportation through cost and schedule effective missionization.

3. System Design Features

The Pulse™ incorporates all features that are commonly desired in command and data handling computers. In addition, many of the I/O functions that are traditionally located in Remote I/O Units (RIU), have been localized within the Pulse™ thus reducing overall power, and cost, while improving the reliability and thermal characteristics of the satellite. Based on the satellite configuration, overall weight may be reduced. Additionally, the architecture supports the ability to redistribute the I/O modules as Remote Interface Units while maintaining the same interfaces (IEEE-1394) among the processing function and I/O functions.

System design features include the following:

- Radiation Hardened RHPPc built at Honeywell's Solid State Electronic Center (SSEC) using the latest 0.35 µm SIO V technology.
- High throughput to power ratio; the RHPPc provides an 81Mips/W compared to a 25Mips/W for the RAD750
- Scalable throughput from 35 Mips (Dhrystone) up to 210 Mips, allowing the user to reconfigure the processor throughput based on the mission phase, thus reducing power consumption and improving thermal and reliability performance.
- Throughput margin provided within the C&DH computer allows for integration of many satellite bus functions that traditionally required multiple processing units.
- Integrated T&C within the SBC board. This feature eliminates the need for separate modules dedicated to the telemetry and commanding functions
- Modular design allows for minimal non-recurring costs to make changes in the product requirements. Due to the Pulse's simplified backplane architecture, its distributed power architecture, and the use of a memory mapped serial bus (IEEE-1394A) rather than the traditional parallel buses, expanding or shrinking the chassis involves low risk mechanical design and timing analysis tasks.
- Distributed power supply architecture allows for tailored and very efficient power supply topology thus reducing overall power dissipation and most of all, providing the design with the ability to accommodate any I/O type without the need to redesign power supplies or overdesign a centralized supply to handle the different redundancy configurations that may be required during the life of the mission
- Fault tolerant Architecture. All module interfaces are cold separable allowing the Pulse™ to be fully cross-strapped thus providing a system with no single point failure, no mission degradation due to two dissimilar failures and de-orbit capability following two similar failures. With proper distribution of I/O functions, the Pulse™ is two fault tolerant.
- The standard mechanical form factor of 6U-220 is easily adaptable to 6U-180 or 6U-160 based on program needs.
- Smart I/O control via the HYDRA ASIC allows for very adaptable mission configurations during flight.
- Each module within the Pulse™ is a standalone unit allowing for improved testing procedures and reduced testing time.
- 28V-100V power input, with minimal convertor redesign of the primary stage
- Designed to meet the stringent MIL-STD-461D EMI/EMC requirements

4. Single Board Computer (SBC)

The heart of the Pulse™ is its SBC. The SBC is designed around Honeywell's radiation hardened RHPPc processor and its companion support ASIC the ECHO. Figure 4 shows the block diagram of the SBC. Figure 5 shows the block diagram of the ECHO ASIC residing on the SBC.

Reducing the overall recurring cost of the C&DH systems has been one of the main drivers behind the architecture baselined for the SBC. Many functions that traditionally required whole modules have been integrated into the SBC resulting in extensive reduction in weight, size, power, and recurring cost, while significantly improving the overall reliability, SEU, and probability of mission success. Because of the technology used, temperature per unit are has either been reduced or kept at status quo.

The SBC provides a versatile memory architecture that interfaces with SRAM, DRAM, EEPROM, and PROM. Robust Error Correction and Detection (EDAC) algorithms are embedded within the ECHO ASIC. Those EDAC algorithms include both the standard EDAC that provide single error correction double error detection (SECDED)

across both 32 bit and 64 bit wide memories, as well as a super EDAC algorithm that performs correction across 5-bit nibbles and allows the loss of one whole memory device without affecting the processor performance.

The SBC provides the following features:

- Twelve independently configurable memory banks providing the capability to support up to 2 Gbytes of addressable memory
- Separate power for command functions allowing the SBC to be mostly powered off (including the RHPPc) while keeping the uplink interfaces fully functional
- Hardwired telecommand processing without processor intervention
- Three fully compliant CCSDS uplink interfaces, two of which are cross-strapped
- Fully compliant CCSDS type 2 and 3, grade 1 and 2 downlink interface
- MIL-STD-1553B interface
- Up to 64 low level open collector telecommands
- Two GPS 1PPs interfaces
- Two Watchdog timers
- One Shutdown timer
- Two general purpose timers
- One Mission timer
- System time generation of both minor and major frame timing sequences
- Fault detection and redundancy management

The current SBC design provides one bank each of SRAM (2 Mbytes), DRAM (64 Mbytes), EEPROM 92 Mbytes), and two banks of PROM (64 Kbytes).

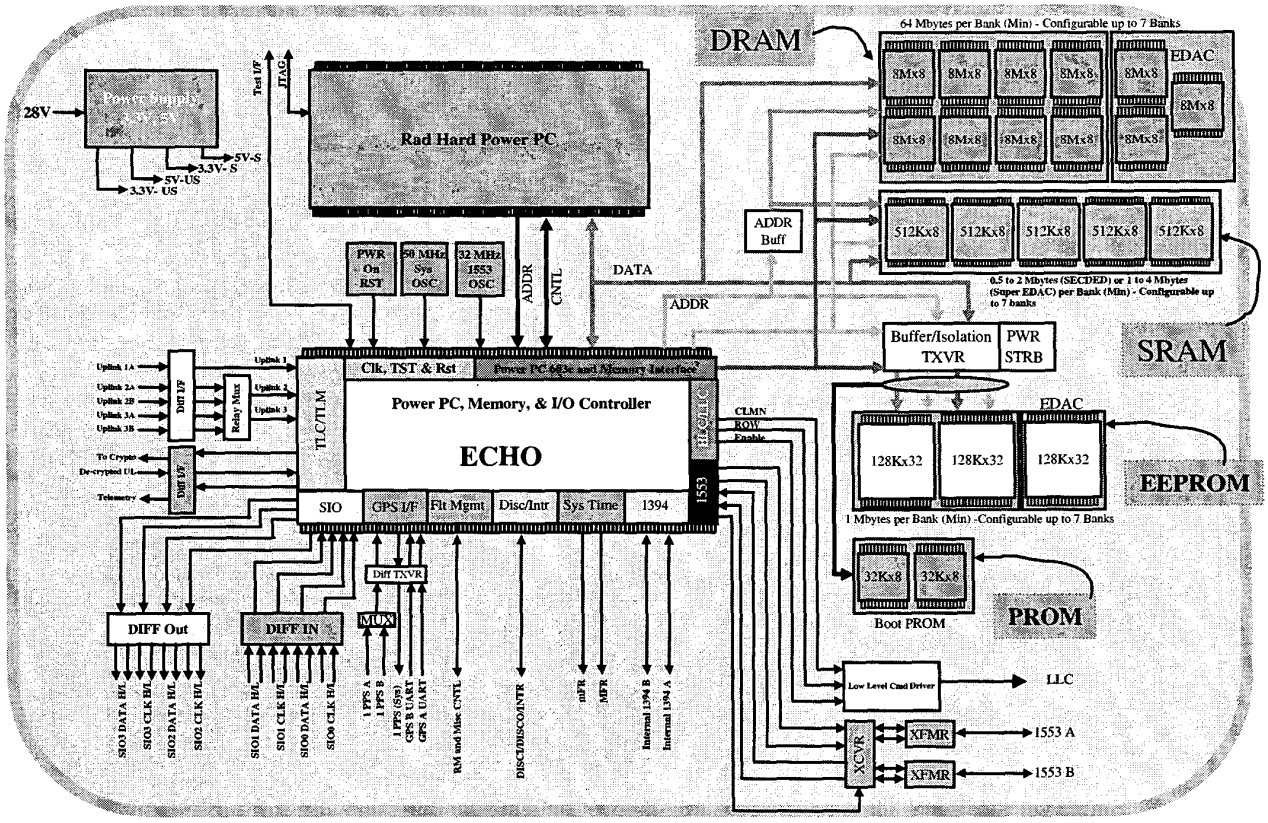

Figure 4 – Single Board Computer Block Diagram

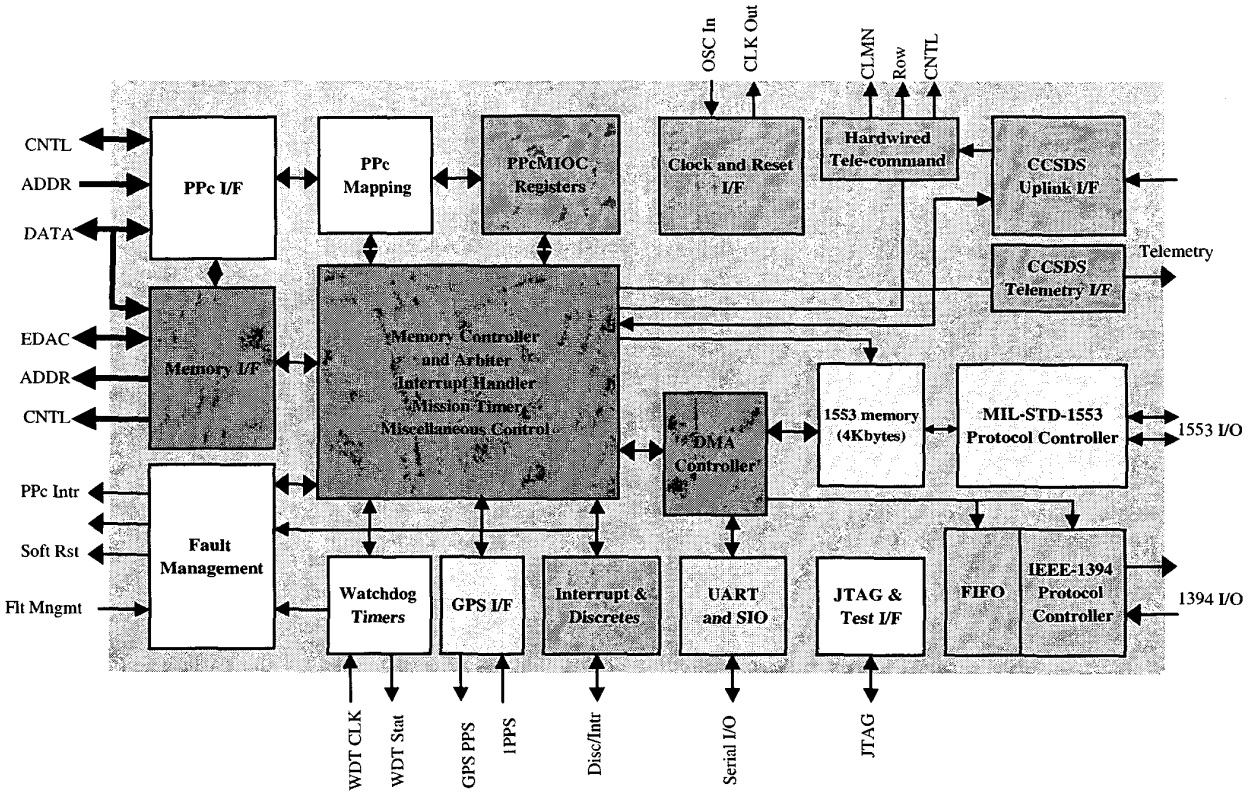

Figure 5 – ECHO ASIC Block Diagram

5. STANDARDIZED INTERFACES

The Pulse™ provides several industry standard interfaces that are used to provide uplink and downlink communication channels. Those interfaces, which are resident on the SBC, and embedded within the radiation hardened ECHO ASIC are as follows:

- Three uplink interfaces that are programmable to be either fully compliant to the CCSDS recommendations or be strictly a word by word software controlled interfaces. Two of the interfaces are fully cross-strapped. The third is typically used as an umbilical interface for ground testing. The uplink interfaces support data rates of up to 1 Mbps
  - When configured for CCSDS compliance (Power Up initial state), the ECHO ASIC within the SBC performs all the necessary data validation checks up to the segmentation layer of the protocol. Data stored in memory will form the packetaization layer as described by the recommendation. This approach alleviates the processor from performing the data integrity checks and the ECHO ensures that data stored into the memory for processor manipulation is free of errors.
  - When configured for non-CCSDS mode, the uplink channels provide the user the capability to send a contiguous serial data stream with a programmable synchronization pattern of 32-bit data word.
  - The uplink interfaces provide a processor independent reconfiguration command channel via a dedicated hardwired telecommand interface that allows ground communication and reconfiguration of the Pulse™ without processor intervention. Up to 64 fully programmable hardwired telecommand are provided
- One CCSDS compliant downlink channel that meets grades 2 and 3, levels 1 and 2 of the CCSDS recommendations. This channel is capable of transmitting data at a rate of up to 1.4 Mbps
- Four fully synchronous, programmable, full duplex serial interfaces with up to 10 Mbps data rates
- Three 8250 compliant UARTs
- Optional external IEEE-1394 multi-drop interface

6. INPUT/OUTPUT MODULES

One of the major advantages of the Pulse™ is its modularized I/O suite. Honeywell has developed an ASIC, code named HYDRA, that is used as both an I/O controller and the interface to the Pulse's backplane. Figure 6 shows the block diagram of the generic I/O module. Figure 7 shows the I/O core block, and Figure 8 shows the HYDRA architecture. Each I/O module is fully cross-strapped with the processors within the system. The HYDRA ASIC embeds a 320C50 DSP as the controller micro-sequencer, IEEE-1394 interface, MIL-STD-1553B interface, timers, programmable discretes, reaction wheel interface, as well as a versatile memory interface with single error correction and double bit detection EDAC algorithm. The HYDRA ASIC is built on SSEC SOI V technology providing the space community with the first 320C50 DSP based radiation hardened micro-controller.

By utilizing the HYDRA ASIC on each of the I/O modules, a common interface is now provided between the processors and all the I/O modules effectively providing the SBCs with an extension of its own memory map. This approach allows the application S/W to be easily modified for the different I/O modules with minimal impact to the qualification and validation of the software suite.

By embedding a 320C50 DSP within the HYDRA, the I/O modules can be considered as stand alone units.

As part of the early development effort, Honeywell has designed and in the process of testing most of the I/O functional blocks. Those I/O functional blocks include:

- High Level pulse commands (0-28 V)
- Low Level pulse commands (0-5 V open collector)
- High and Low level analog in
- Passive analog in - thermistor I/F ; compatible with GSFC S-311-P-18 characteristics used, tailorable to others
- 3 axis magnetometer in - compatible with Billingsley Magnetics TFM100S; high level analog equivalent circuits
- 2-axis coarse sun sensor in - compatible with Adcole Model # 44930 (low level analog I/F)
- Torque rod drive - compatible with Ithaco TR140CFR; easily adaptable to other requirements
- Solar array drive - stepper motor I/F ; compatible with Honeywell PEPE-008 as guide
- Reaction wheel assemblies - compatible with Honeywell's HR14X analog I/F but can be easily modified to be compatible with others
- Reaction wheel assemblies - multi-drop serial I/F compliant to HR14X(digital I/F)
- Bi-level discrete inputs/outputs

Once a program specific I/O interface is defined, modification of the above interface for both electrical and quantity requirements is quite simple thus reducing the overall NRE while still providing the user an early software development unit.

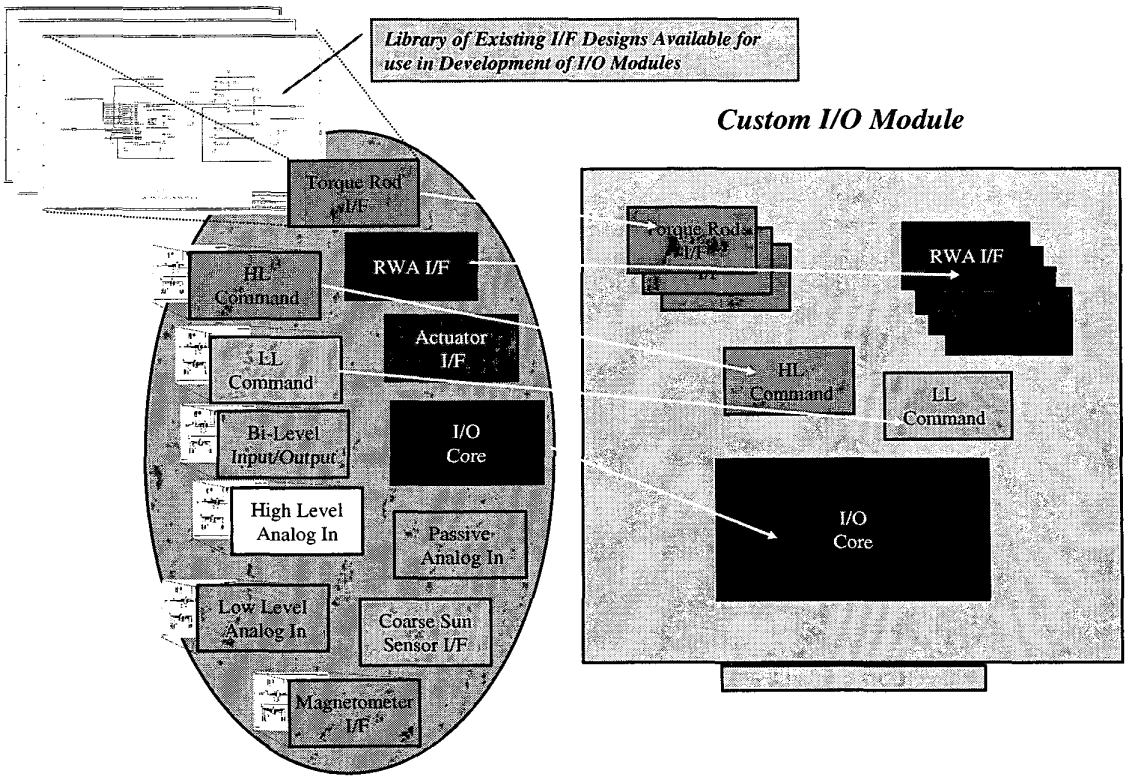

Figure 6 – Generic I/O Module Block Diagram

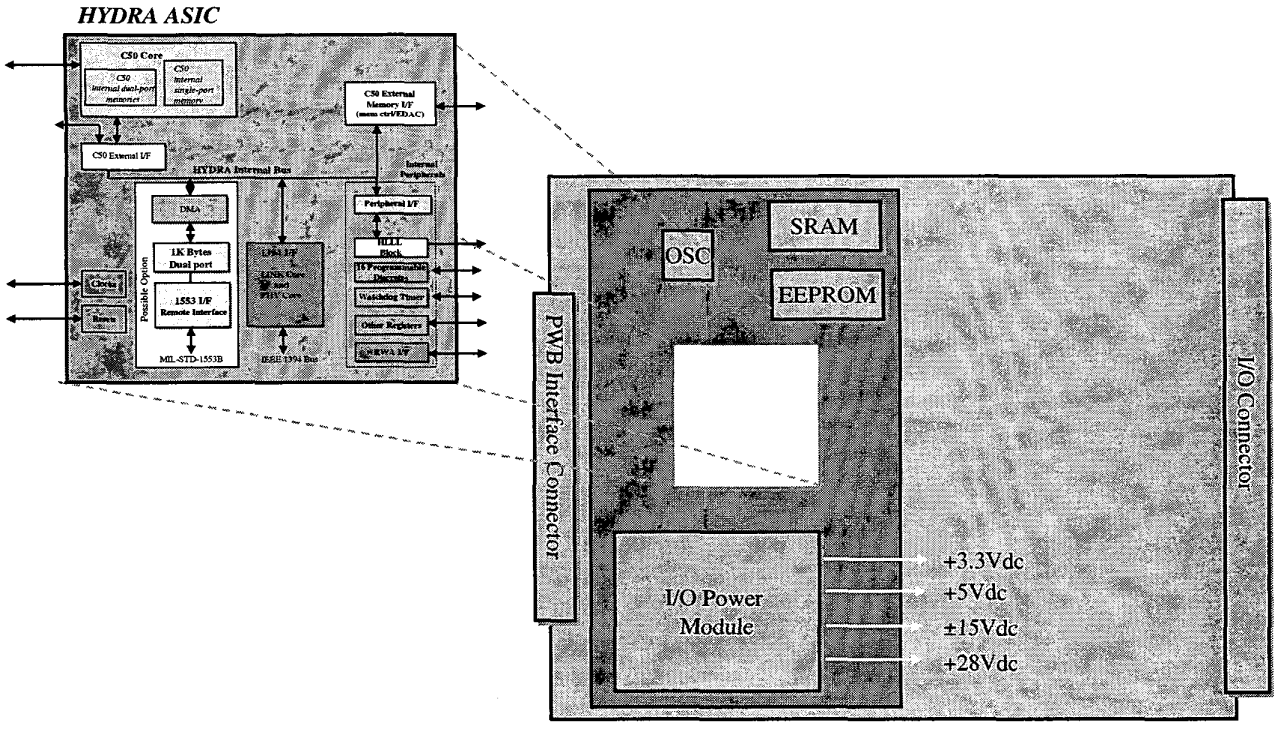

Figure 7 – I/O Core Block Diagram

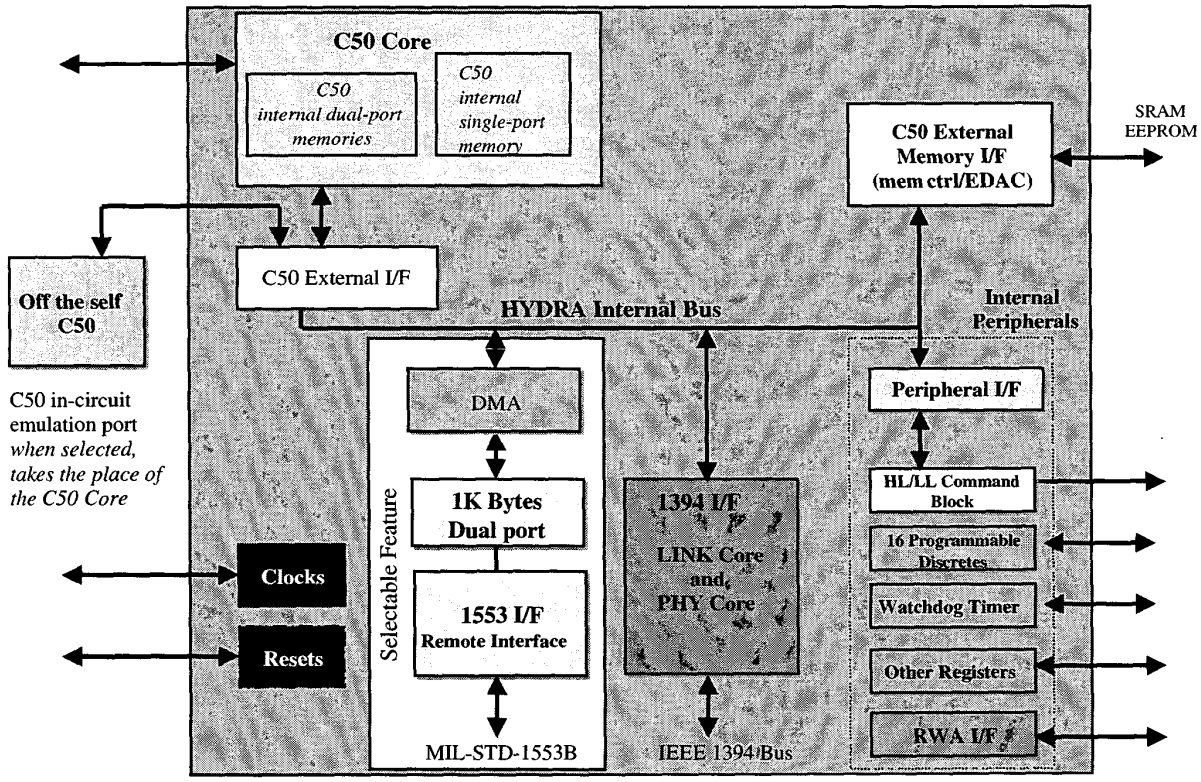

Figure 8 – HYDRA ASIC Block Diagram

7. MECHANICAL FEATURES

Mechanically, the Pulse™ is designed to fit the 6U-220 form factor. As shown in Figures 9 and 10, the current configuration of the Pulse, consists of 3 redundant SBCs and 5 redundant I/O modules, for a total of 13 slot chassis, weighs approximately 55 lbs., measures 18.8 (L)x11.75 (W)x10.7 (H), and occupies a volume of 2366 in^3. The I/O modules provide up to 2000 signal I/O through the top connector interface.

The mechanical design of the Pulse™ was baselined to allow modifications in the card size to be easily accomplished. The Pulse™ mechanical design supports configuration of 6U-180 and 6U-160 form factors, and from 4 up to 16 modules. The Master Interconnect Board (MIB) is extremely simplified with the implementation of the IEEE-1394 multi-drop backplane interface allowing modification of the MIB to be accomplished with minimal design impacts.

8. ENVIRONMENTS

The Pulse™ is designed to meet the environmental requirements of low earth orbits. With part substitution for different radiation ennvironments, GEO and/or MEO orbits are easily accommodated.

Preliminary estimates for the Pulse™ reliability is around 0.995 for 10 years with a 30°C baseplate temperature. The Pulse™ provides SEU resistance of 4E-05 upsets/Pulse/day in a 10% Adams WC, geosynchronous orbit.

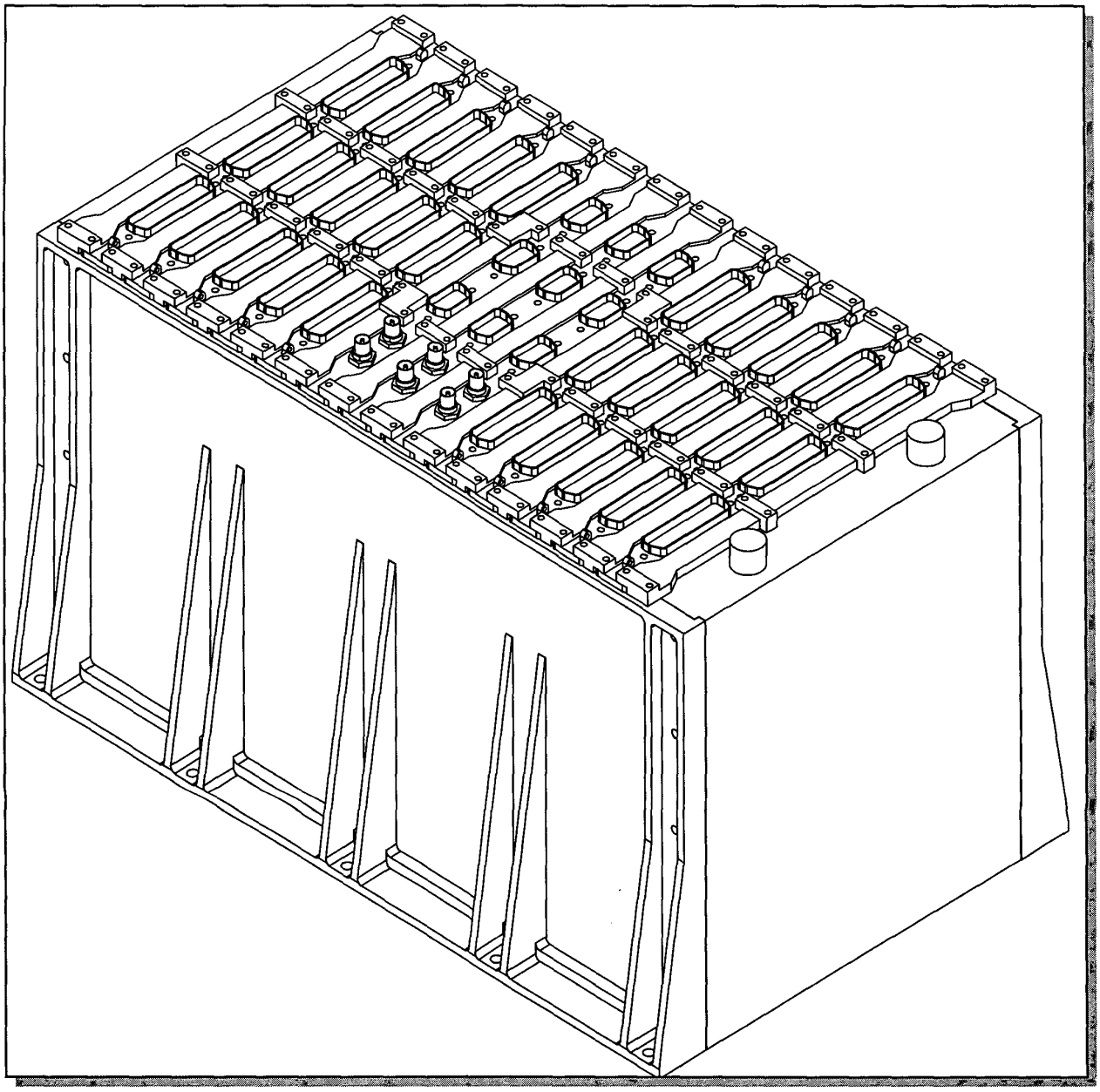

Figure 9 – Pulse Isometric View

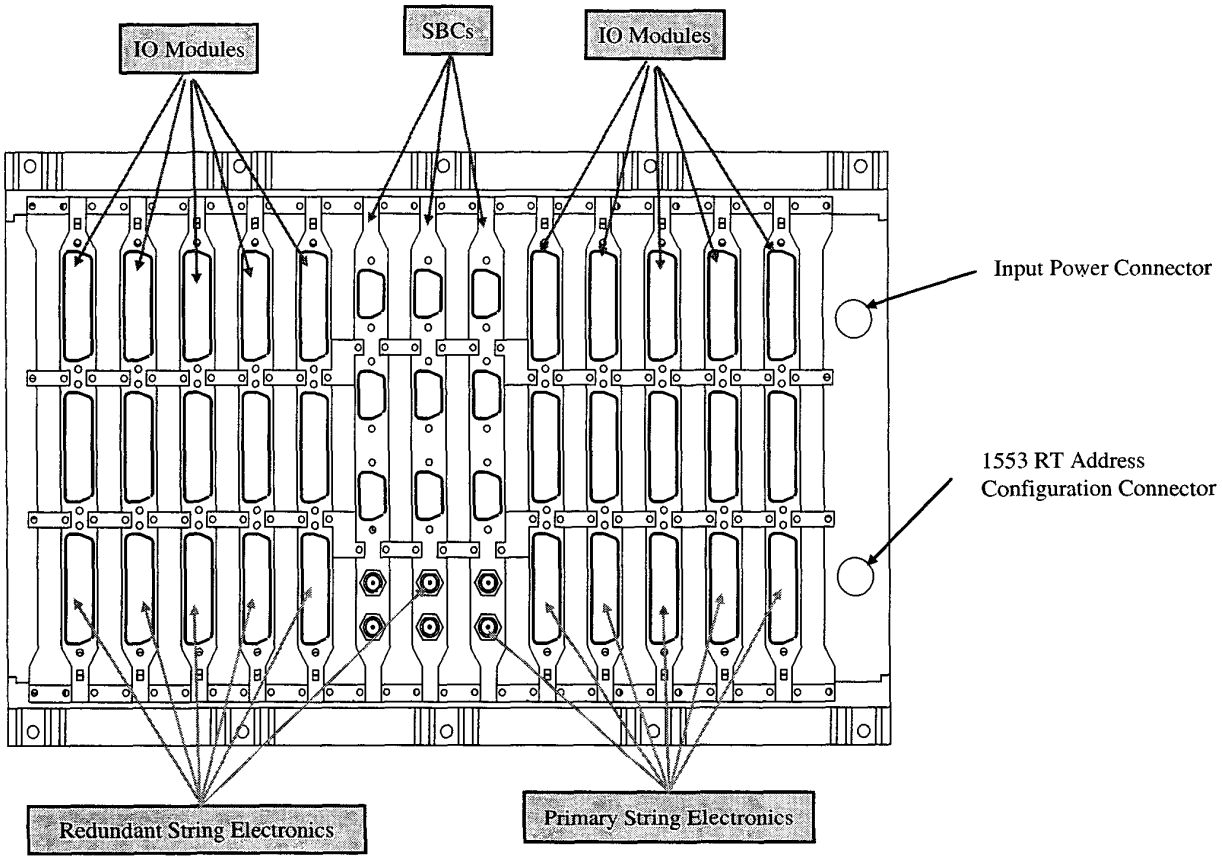

Figure 10 – Pulse Top View

9. CONCLUSION

The Pulse™ design draws on considerable flight heritage and the latest radiation hardened ASIC technologies. Conservative system engineering methods carefully implement fault tolerance and redundancy management to meet the needs of most applications. The highly integrated design assures high reliability for mission success at a very competitive cost.

The Pulse™ architecture and feature set provides the user with a scalable architecture that can be readily modified to meet the varying needs of different satellite applications, while maintaining a standard COTS software environment and hardware platform.