A Multichip Module, the Basic Building Block for Large Area Pixel Detectors

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Abstract

In order to build large array pixel detectors for future experiments in High Energy Physics e.g. for experiments at the Large Hadron Collider (LHC) at CERN, one needs to construct easy to handle and manufacturable modules which can be used to put together to big detector systems. Diode- (pixel-) arrays can be fabricated in wafer size dimensions (currently about 8 cm in length); read out chips have dimensions of about 1 cm^2. A natural (but not trivial) thing would be to use the silicon diode array as the basic building block for a detector system. Several read out chips have to be bonded onto this module. For easy module interconnections the data lines, control lines, and power distributions have to be connected to the periphery of the module. To avoid complicated wiring, all lines should be integrated onto the detector substrate. Such a module could be made using multichip module (MCM) technology. Some electrical considerations of such a module and possible realizations are discussed.

Multichip module as basic building block

The type of technology proposed here is called MCM-D where the interconnections are formed by depositing dielectric materials and conductors onto a base substrate which in our case is high-resistivity, active, fully depleted silicon. The production technology closely follows semiconductor techniques. The most commonly used conductor materials are aluminium, copper, or gold. Dielectric materials might be silica, polyimide, or benzocyclobutene with a thickness of 5 to 25 μm. Photolithography, sputtering, wet and dry etching are used to create the interconnections. A first try towards a multichip module for a pixel detector has been carried out for the planned very forward detector for DELPHI-Experiment [1] at CERN. Ref. [2] describes in some detail mechanical, thermal, and electrical considerations. MCM packaging technology is decribed in [3]. This note only deals with some electrical aspects for the chip-to-periphery interconnections.

Electrical considerations

In the LHC environment [4] we have to deal with "medium" frequencies. Even for clock rates below 100 MHz one has to take care that line capacitances and line resitances do not cause RC-line charging which may slow down signal speeds quite considerably. In the 100 to 500 MHz domain the interconnections must be controlled-impedance transmission lines and should be terminated. In all cases decoupling capacitors must be on the substrate and as close as possible to the active elements. The line cross sections have to be large to decrease dc and ac resistive losses. The power and ground plane positioning in the layer stack becomes important.

Thin film interconnection lines, such as used in IC-technology, give unacceptable performances even at medium frequencies. These lines show RC-charging delays which increase with the square of their length. For example a thin IC-line of 20 cm length gives a charging delay of more then 100 nsec compared to about 1 nsec for a pure TEM wave. The way out of this problem is to use thick film LC-transmission lines. A structure which is favourable for our application is a stripline configuration where the x- and y-signal lines are imbedded into a dielectric material with two metal planes on top and bottom (ground and power plate in Fig. 1) closing the structure. Such a "homogeneous" structure, as shown in Fig. 1, has lowest possible cross talk between two parallel lines, when width, thickness, and line spacing are fixed. This effect can be easily understood: The presence of the two metal planes provides conductor surfaces that attract electric field lines which would normally terminate on another signal line. The magnetic field lines are similarly confined by the reduced space around the signal conductor. Careful simulations and comparisons with experiment have been described in Ref. [5]. The calculations described below have been compared with these simulations.

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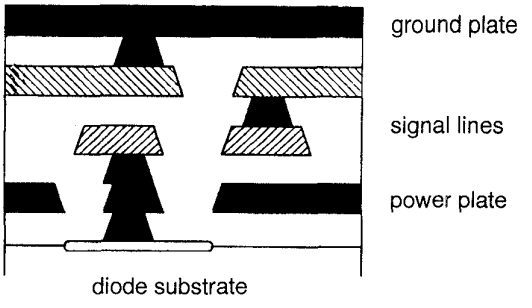

Fig. 1: Schematic MCM interconnection structure

The two low impedance low resistivity metal planes, enclosing the signal lines, can be used for power and ground distributions to the read out chips.

A criterion for the thickness of the signal lines to achieve LC-transmission line behaviour can be evaluated from the attenuation of the signal amplitude when transversing a line of length l. In case of a microstrip line model a simple measure is given by calculating the product of the line thickness t and the dielectric height h (distance from the metal plate). LC-behaviour is obtained [5] if

$$th \gg \rho c l \varepsilon_0 \sqrt{\varepsilon_r}$$

where ρ is the metal resistivity, ε_r is the relative dielectric constant, ε_0 the dielectric constant of the vacuum and c the vacuum light velocity. For a line of length l = 15 cm and a low stress polyimide dielectric with ε_r= 2.8 one observes LC-behaviour for

$$t\,h \gg 18\ \mu m^2$$

for an aluminium line (ρ = 2.8 $\mu\Omega$cm) and

$$t\,h \gg 11\ \mu m^2$$ for a copper line (ρ = 1.7 $\mu\Omega$ cm).

To analyse a periodic array of interconnect lines with distributional characteristics, an analytical program [6] has been written. The structure of the analysed microstrip lines is shown in Fig. 2.

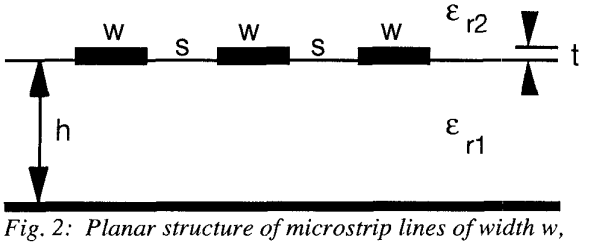

Fig. 2: Planar structure of microstrip lines of width w, line spacing s, thickness t, and a distance h from the ground plate.

In its most elementary form such a structure consists of two adjacent lines which can support two different modes of propagation with different characteristic impedances and phase velocities. If the lines are symmetric, as shown in Fig. 3, the modes reduce to even and odd modes corresponding to an even and odd symmetry about a plane which can be placed as a magnetic or electric wall.

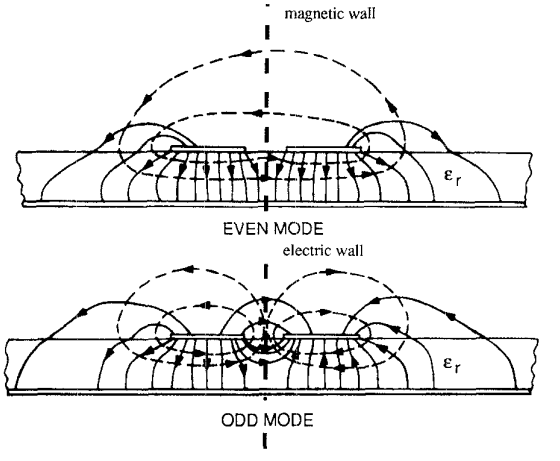

Fig. 3: Even and odd mode field configurations in coupled microstrip lines

For the analysis such a coupled transmission line model has been used to compute line capacitances, line inductances, characteristic impedances and the line resistance. The inter-line voltage coupling is estimated. The analytical formulae used are taken from Ref. [7] and [8]. The capacitance model for determining even and odd mode capacitances is shown in Fig. 4.

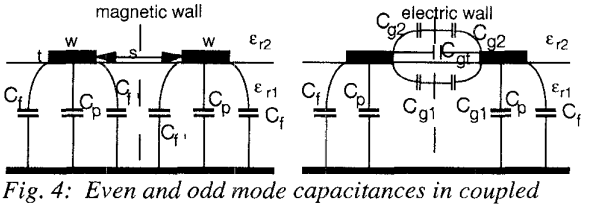

Fig. 4: Even and odd mode capacitances in coupled microstrip lines

From Fig. 4 we get for the even mode capacitance per unit length

$$C_e = C_p + C_f + C_f$$

and for the odd mode capacitance per unit length

$$C_o = C_p + C_f + C_{g1} + C_{g2} + C_{gt}\ .$$

$C_{g1,2}$ are "measured" against the virtual electric wall; C_{gt} is the capacitance between the two lines. The even and odd mode capacitances determine the self capacitance and mutual capacitance per unit lengths between the two lines:

$$C_s = (C_o + C_e)/2$$

$C_m = (C_o - C_e)/2$.

If we assume a non-magnetic dielectric medium ($\mu = \mu_o$), the self and mutual inductances can be computed

$$L_s = \mu_o\varepsilon_o\,(1/C_e^{air} + 1/C_o^{air})/2$$

$$L_m = \mu_o\varepsilon_o\,(1/C_e^{air} - 1/C_o^{air})/2$$

with $C_{e,o}^{air}$ being the even, odd capacitances without a dielectric medium.

To extend the microstrip line model to the stripline model configuration discussed in the beginning, the same microstrip model was applied again now taking the dielectric thickness equal to 2h which is the distance to the second metal plate. Again even and odd mode capacitances and inductances were computed. The simplified capacitance model is illustrated in Fig. 5.

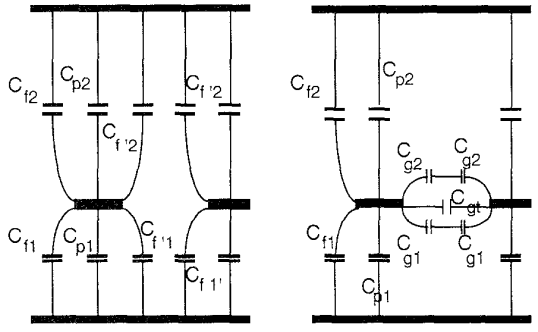

Fig. 5: Even and odd mode capacitances in a coupled stripline configuration

In this case we get for the stripline configuration:

$$C_e = C_{f1} + C_{f2} + C_{p1} + C_{p2} + C_{f1} + C_{f2}$$

$$C_o = C_{f1} + C_{f2} + C_{p1} + C_{p2} + C_{g1} + C_{g2} + C_{gt}\ .$$

The computation of self and mutual capacitances and inductances is done the same way as described before. (For the second signal plane the geometrical situation is reverse: The distance to the upper metal plane is h and to the lower metal plane 2h. The even and odd mode capacitances stay the same as for the lower signal plane discussed before).

For aluminium lines of width w = 20 μm, thickness t = 6 μm, with a spacing s = 20 μm, a polyimide dielectric with $\varepsilon_r = 2.8$ and thickness h = 12 μm, we get for the stripline configuration a typical capacitance of 1.6 pF/cm with a time of flight of about 60 psec/cm. The characteristic impedance is $Z_0 \cong 40\,\Omega$ and the voltage coupling to the next neighboured line is less then -20 dB. For a 10 cm long line the signal damping is about 25 %.

For good overall performance the line driver output resistance should be less than 40 Ω. The receiver resistance might be greater then 1 kΩ, the input capacitance should not be much greater then the line capacitance.

Possible realisation

Fig. 6 a) shows the sketch of a possible pixel module for LHC applications [4]. The proposed four-metal structure would add ~60 μm to the thickness of the silicon substrate which currently is 300 μm thick.

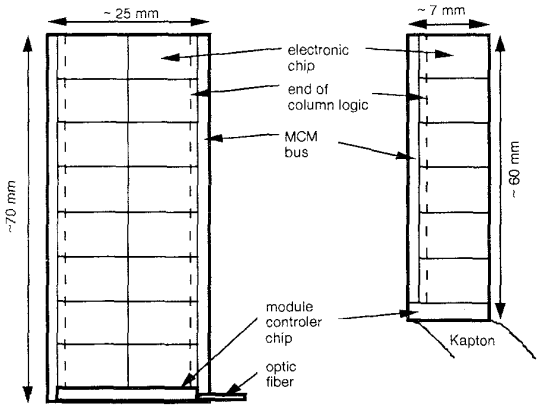

Fig.6: Sketch of pixel modules: (a) as currently discussed in the ATLAS collaboration; (b) proposed prototype compatible with a "ladder" for the Omega experiment.

Considering the proposed ATLAS scheme (Fig. 6a), an additional problem appears. In this scheme 16 read out chips have to be bump bonded to the detector substrate. If the yield of good chips is 93 %, the MCM-yield is only 31 %, not taking into account possible problems during chip mounting. This means that one has to perform very careful full functional tests (and possibly even some burn-in) before mounting the chips to the detectors. The MCM-yield increases to 85 % if the single die yield after tests is 99 %. This problem is known as the "Known-good Die" problem (KGD). The IC-manufacturer Intel just started this KGD business [9]. The Intel initiative could probably result in the globalization of the MCM technology. We have to observe carefully what is going on in this field in the near future.

To reduce the KGD problem and to start with a simpler module we propose to build a MCM prototype (Fig. 6b) compatible with a "ladder" for the Omega experiment [10]. In this case six read out chips are mounted on the detector array. The end of column logic at the periphery of each chip is connected to the MCM bus consisting of two signal planes between two metal planes for power and ground distributions to the chips. At the module's periphery the bus is connected to a

controller chip, currently under production in Genova [11]. For the new developed OMEGA3/LHC1 read out chip [12] connections to and from the end of column logic are foreseen which can be either bump bonded to the MCM bus or wire bonded to a ceramic substrate as done before.

Fig. 7 shows a part of a preliminary layout of the most critical region of the MCM, the feed through connections from the detector elements to a read out chip. This layout is consistent with the design rules of GEC-Marconi [13]. This preliminary study shows that it is possible, even with design rules from 1993, to build a MCM with about 2000 I/O's per cm^2 from the active Si-substrate through the deposited MCM-D layers.

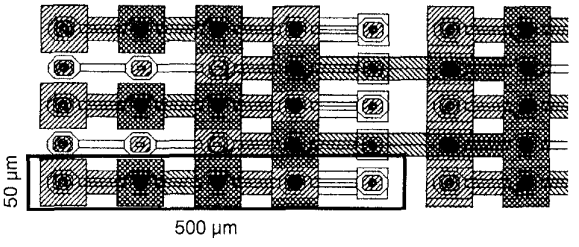

Fig. 7: Part of a preliminary layout of some staggered feed through connections from pixel diodes to a read out chip (shown are five neighbour cells of 50 µm times 500 µm)

Conclusions

This study demonstrates that a multichip module is potentially an appropriate building block for large area pixel detectors. Four metal planes separated by polyimide dielectric layers allow for fast signal transmission and low cross talk between adjacent signal lines if driving and termination requirements can be met. The two metal layers above and below the signal lines offer the possibility of low resistivity power distribution because of their large widths. The proposed metal structure results in controlled-impedance transmission signal lines. A preliminary layout demonstrates that the needed very high I/O low pitch feed through is achievable with present available MCM-D technology.

After this feasibility study a first module prototype should be built in the near future.

References

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