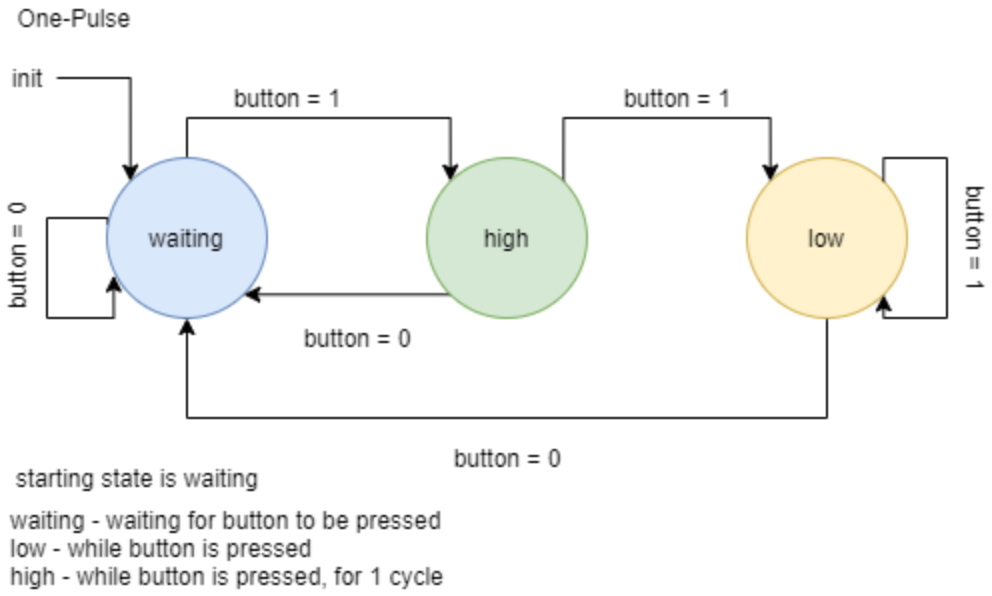
Lab 3 Discussion

If you have a de-bounced button (that is, one that only goes high when you push it and immediately goes back low when you let go) as an input to a 100MHz FSM, you would have to hold down the button for about 10ns to have it only advance one state in the FSM. This is obviously impractical. Draw a bubble diagram for a "one-pulse" FSM that outputs a 1-cycle pulse every time the button is pressed, regardless of how long it is held down. Keep in mind there is no other state or memory in the universe other than which bubble the FSM is currently on. If you are confused about what is a pure FSM and what is not, ask your TA for help.



Assume some stray radiation hits the state bits of a one-hot encoded FSM and one of those bits is flipped such that either two state bits are high or zero state bits are high. What will happen to the design if it was written as a Verilog case statement with no default entry? What if there was a default entry?

> If there is no default entry, it will infer a latch and the output will be undefined. In Verilog, it will exit that case statement and as a result, the erroneous state will stay broken forever (registers are not updated).
> If there is a default entry, the stray case would fall into the default case and the default entry would be the output.