a. The critical path of your design – Report the slack, source, and destination of the critical path. Look at the list of locations the signal visits under 'Maximum Data Path'. Do you recognize from where in your logic this path comes from?
   <u>Critical Path:</u>
   Slack = 5.363ns
   Source: bicycle_fsm/beat/value_ref/q_reg[4]/C
   Destination: bicycle_fsm/beat/value_reg/q_reg[21]/D
   It seems as if this logic path comes from constantly consulting the *beat32 module*

b. Those resource usage statistics we collected in labs 1 and 2. Double click "Design Summary/Reports" and select "Summary" at the top of the reports list.
   i. What fraction of the FPGA's slice LUTs did your implementation consume?
      0.86%
   ii. How many slices are occupied?
      54 slices
   iii. How many slice registers did your implementation consume? These registers are configured as flip-flops, which you instantiated using the dff module.
      143 slice registers

c. Open the FPGA layout.
   - **Marked flipflop from master_FSM is in pink on bottom right**