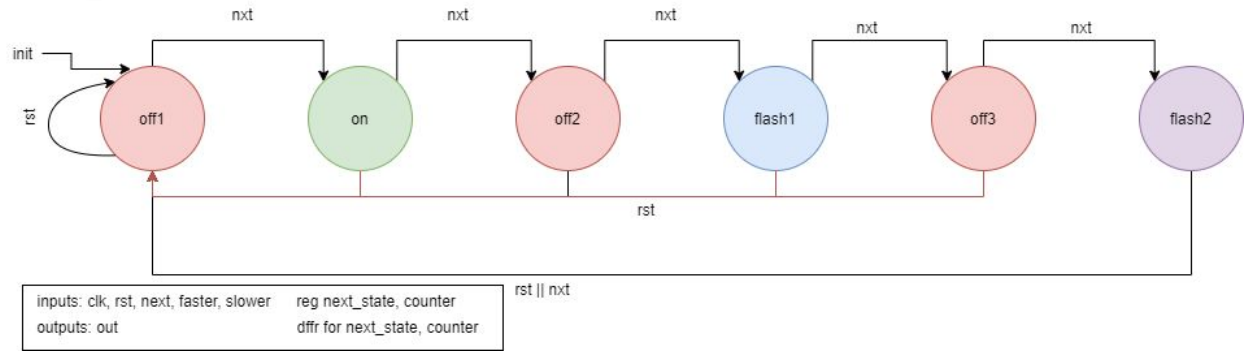
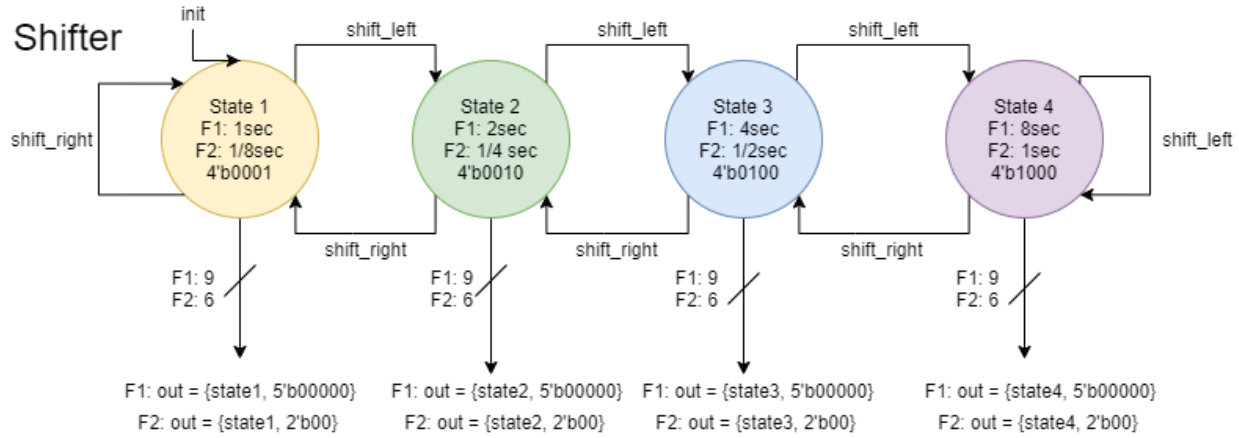
Finite State Machines

Master_FSM



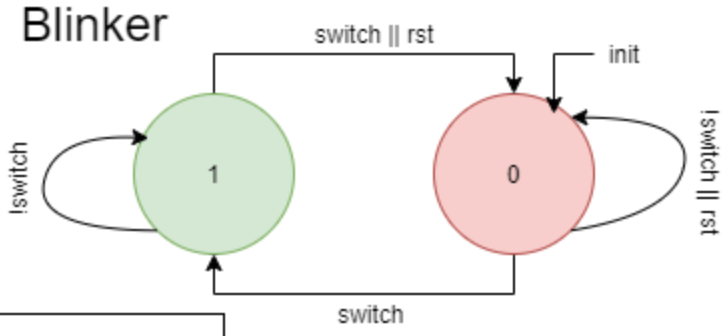
inputs: clk, rst, next, faster, slower
outputs: out
reg next_state, counter
dffr for next_state, counter

Shifter



inputs: shift_left, shift_right
output: out
reg: next_state

Blinker



input: clk, switch, rst
output: out

Block Diagrams

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