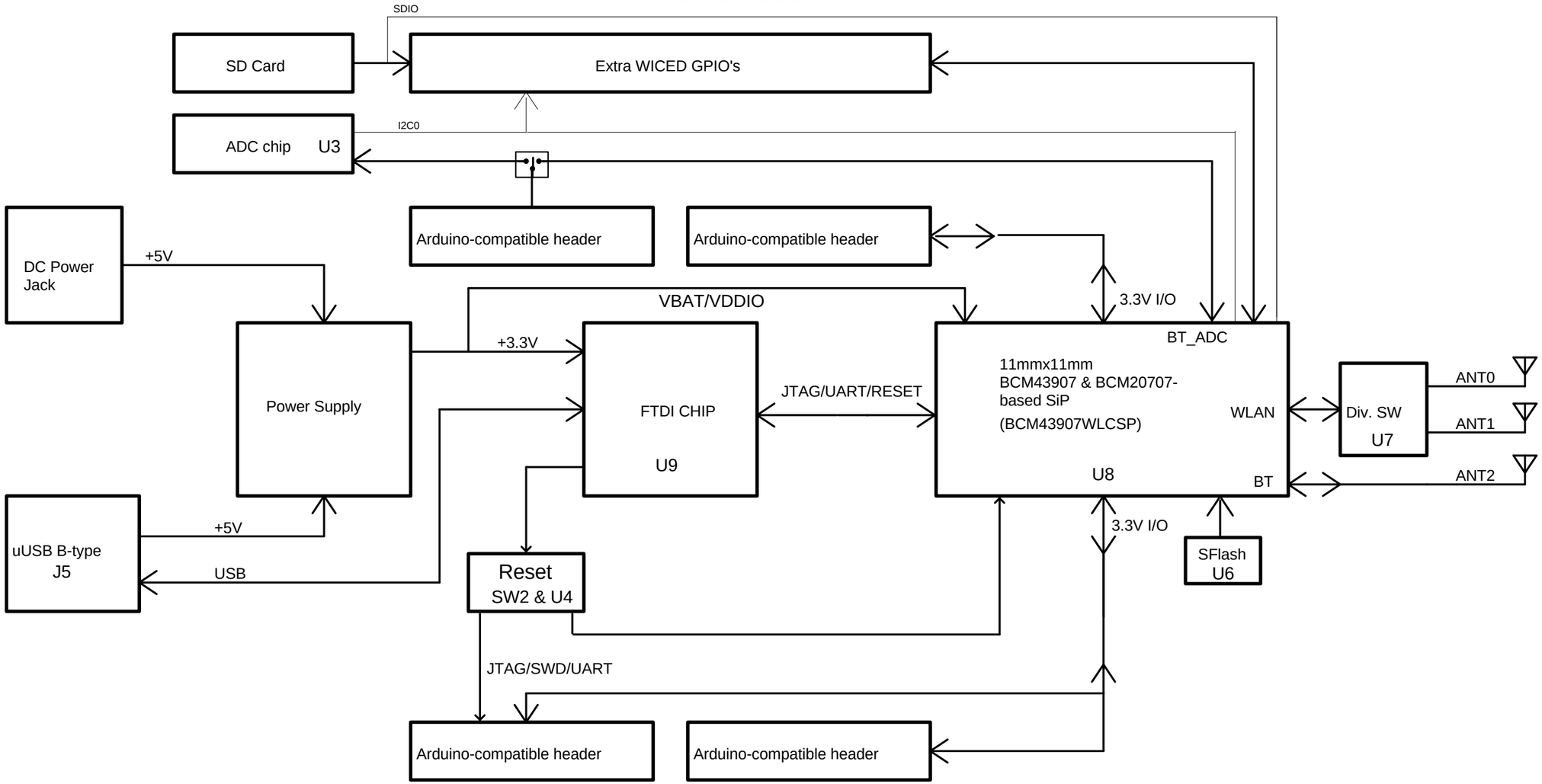
BCM943907AEVAL2F



*** INDEX ***

SHEET 1: SYSTEM BLOCK DIAGRAM
SHEET 2: REVISION HISTORY
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SHEET 6: BCM43907 (WLAN) and BCM20707 (BT) SiP (11mm x 11mm)
SHEET 7: BOOTSTRAPS AND SFLASH
SHEET 8: RF FRONT-END (ANTs)
SHEET 9: DELAY, AUTH IC, SD
SHEET 10: ARDUINO AND WICED HEADERS

SYSTEM BLOCK DIAGRAM

Approvals		Broadcom			
		Company Confidential			
Designer	Date	SIZE: B	TITLE: BCM943907AEVAL2F_1		
Reviewer	Date				
Reviewer	Date	Designer: GURMAIL KANDOLA		Drawing Number: 824-129830-0010	Version: 02
Reviewer	Date	DATE: 15/10/2015:15:20 Oct 15, 2015		SHEET 1 OF 1	

REVISION HISOTRY

REV	DATE	NOTES
P101	9/2/ 2015	Engineering release for procurement.
P102	10/15/ 2015	1. Merged BT_VBAT and BT_VDDIO into a new net BT_3V3. Removed R25. 2. Switched Ant0, Ant1 RF and control signals at U7 to remove RF trace cross over seen in layout. 3. Replaced ANT2 with single-band ant 4. Changed footprint for U6 and U9 . Added L12, 14. Removed Strapping GPIO_9_USB* 5. Since BT RF trace from U8 to J3 was long, added another pi matching network.

REVISION HISOTRY

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SIZE	TITLE	
B		BCM943907AEVAL2F_1 2
DATE	15/10/2015:15:27	SHEET OF 1

BCM43907WLCSP SiP Pin Name	WICED header net name
PWM_4	PWM_4
PWM_5	PWM_5
I2S0_MCK	I2S0_MCK
I2S0_SD_OUT	I2S0_SD_OUT
I2S0_SCK_BLCK	I2S0_SCK_BLCK
I2S0_WS_LRCLK	I2S0_WS_LRCLK
NC	NC
GND	GND
SPI_1_CLK	SPI_1_CLK
I2S1_SD_OUT	I2S1_SD_OUT
SPI_1_MISO	SPI_1_MISO
SPI_0_CLK	SPI_0_CLK
SPI_1_MOSI	SPI_1_MOSI
SPI_0_MOSI	SPI_0_MOSI
SPI_1_CS	SPI_1_CS
SPI_0_CS	SPI_0_CS
SPI_0_MISO	SPI_0_MISO
UART0_RXD_BT_JTAG_TDO	UART0_RXD_BT_JTAG_TDO
GND	GND
UART0_TXD_BT_JTAG_TDI	UART0_TXD_BT_JTAG_TDI
USB2_HOST_DEV_SEL	USB2_HOST_DEV_SEL
UART0_CTS_BT_JTAG_CLK	UART0_CTS_BT_JTAG_CLK
I2C_0_SCL	I2C_0_SCL
UART0_RTS_BT_JTAG_TMS	UART0_RTS_BT_JTAG_TMS
I2C_0_SDA	I2C_0_SDA
I2S1_MCK	I2S1_MCK
I2S1_WS_LRCLK	I2S1_WS_LRCLK
GND	GND
I2S1_SCK_BCLK	I2S1_SCK_BCLK
SDIO_DATA_1	SDIO_DATA_1
SDIO_DATA_0	SDIO_DATA_0
SDIO_CLK	SDIO_CLK
SDIO_CMD	SDIO_CMD
SDIO_DATA_3	SDIO_DATA_3
SDIO_DATA_2	SDIO_DATA_2
RF_SW_CTRL_6_UART1_RXD	RF_SW_CTRL_6_UART1_RXD
UART1_TXD	RF_SW_CTRL_7_UART1_TXD
RF_SW_CTRL_8_BT_GPIO_7	RF_SW_CTRL_8_BT_GPIO_7
RF_SW_CTRL_9_BT_GPIO_6H	RF_SW_CTRL_9_BT_GPIO_6
HIB_WAKE	HIB_WAKE
HIB_LPO_SEL	HIB_LPO_SEL
HIB_REG_ON_IN	HIB_REG_ON_IN
USB2_DN	USB2_DN
USB2_DP	USB2_DP
BT_DEV_WAKE	BT_DEV_WAKE
BT_HOST_WAKE	BT_HOST_WAKE
BT_GPIO_2_BT_JTAG_TRST	BT_GPIO_2_BT_JTAG_TRST

BCM43907WLCSP SiP Pin Name	BCM43907WLCSP SiP Pin Function	SiP bootstrap option	Arduino header net name	Arduino functions
GPIO_0	UART0_RX		GPIO_0	UART_RX
GPIO_1_GSPI_MODE	UART0_TX	GSPI MODE	GPIO_1_GSPI_MODE	UART_TX
GPIO_13_SDIO_MODE	GPIO_13	SDIO MODE	GPIO_13_SDIO_MODE	GPIO
GPIO_7_WCPU_BOOT_MODE	PWM1	WLAN BOOT	GPIO_7_WCPU_BOOT_MODE	PWM
GPIO_14	GPIO_14		GPIO_14	GPIO
GPIO_16	PWM0		GPIO_16	PWM
GPIO_15	PWM1		GPIO_15	PWM
I2S0_SD_IN	GPIO_26		I2S0_SD_IN	GPIO
BT_ADC_0	ADC		ARD_AD0	AD0
BT_ADC_1	ADC		ARD_AD1	AD1
BT_ADC_2	ADC		ARD_AD2	AD2
BT_ADC_3	ADC		ARD_AD3	AD3
I2C_1_SDA	I2C_SDA		ARD_AD4_SDA	AD4, SDA
I2C_1_SCL	I2C_SCL		ARD_AD5_SCL	AD5, SCL
I2S1_SD_IN	GPIO_29		I2S1_SD_IN	GPIO
GPIO_12	PWM2		GPIO_12	PWM
GPIO_11_ACPU_BOOT_MODE	SPI1_CS, PWM5	APPS BOOT	GPIO_11_ACPU_BOOT_MODE	PWM, SPI_CS
GPIO_10	SPI1_MOSI, PWM4		GPIO_10	PWM, SPI_MOSI
GPIO_8_TAP_SEL	SPI1_MISO, PWM2		GPIO_8_TAP_SEL	SPI_MISO
GPIO_9_USB_HSIC_SEL	SPI1_CLK, PWM3		GPIO_9_USB_HSIC_SEL	SPI_SCK
GND	GND		GND	GND
N/A (supplied off eval board)	N/A (supplied off eval board)		ARD_AREF	POWER
I2C_1_SDA	I2C_SDA		ARD_AD4_SDA	AD4, SDA
I2C_1_SCL	I2C_SCL		ARD_AD5_SCL	AD5, SCL
NC	NC		ARD_NC	NC
N/A (supplied off eval board)	N/A (supplied off eval board)		N/A	POWER
RESET_L	RESET		RESET_N	RESET
N/A (supplied off eval board)	N/A (supplied off eval board)		+3V3	POWER
N/A (supplied off eval board)	N/A (supplied off eval board)		N/A	POWER
GND	GND		GND	GND
GND	GND		GND	GND
N/A (supplied off eval board)	N/A (supplied off eval board)		VIN_EXT	POWER

BCM43907WLCSP SiP Pin Name	On Board Debug Interface
GPIO2_JTAG_TCK	GPIO2_JTAG_TCK
GPIO3_JTAG_TMS	GPIO3_JTAG_TMS
GPIO4_JTAG_TDI	GPIO4_JTAG_TDI
GPIO5_JTAG_TDO	GPIO5_JTAG_TDO
GPIO6_JTAG_TRST_L	GPIO6_JTAG_TRST_L
RF_SW_CTRL_7_UART1_TX	RF_SW_CTRL_7_UART1_TXD
RF_SW_CTRL_6_UART1_RX	RF_SW_CTRL_6_UART1_RXD

WICED / ARDUINO HEADER PAIRS

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SIZE	TITLE	
B	BCM943907AEVAL2F_1	
DATE 05/10/2015:17:59		SHEET 3 OF 1

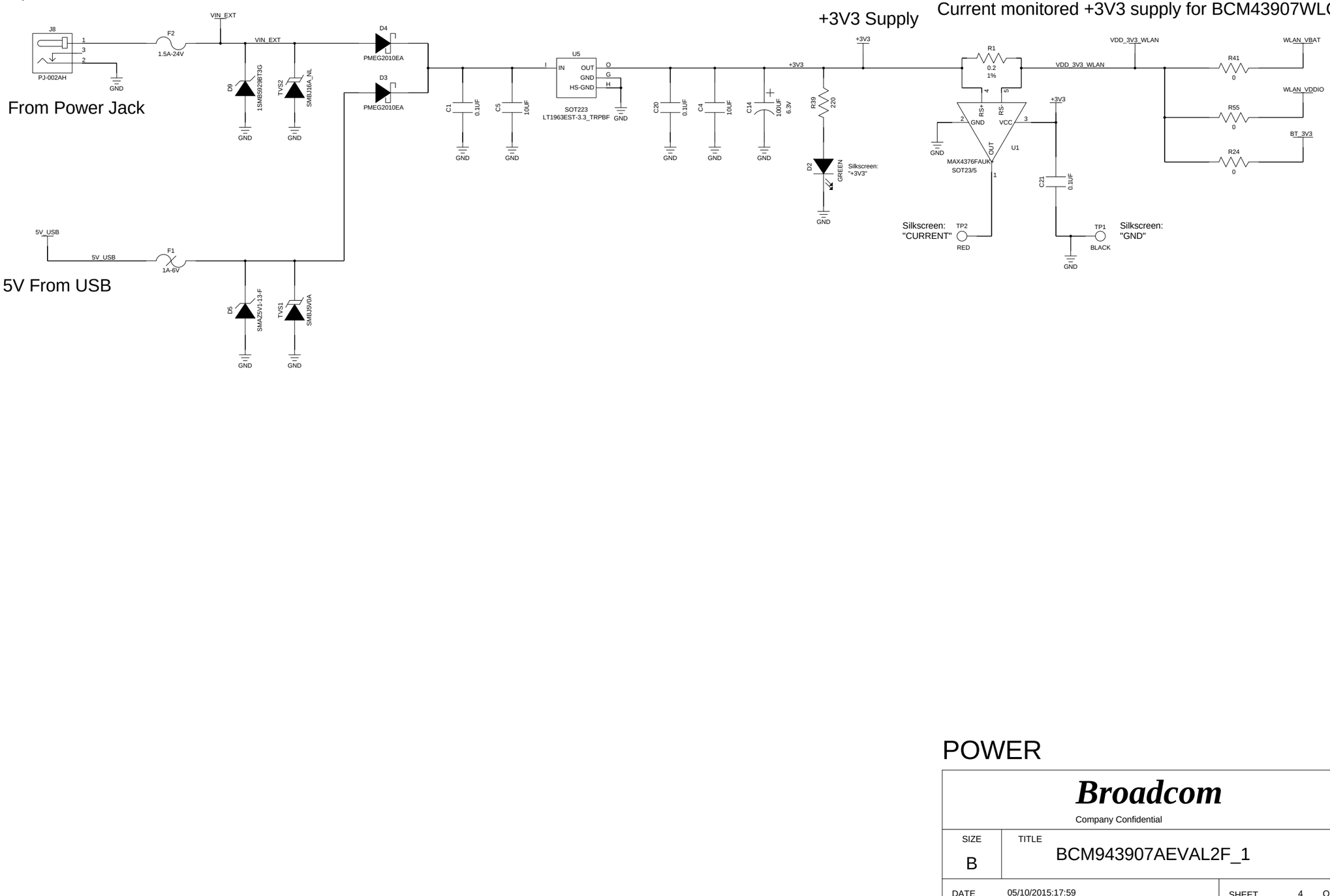
2.1mm DC Jack (centre pin positive)
Typ.= 5Vdc
(Min.= 4.5Vdc)
(Max.= 15Vdc)

From Power Jack

5V From USB

+3V3 Supply

Current monitored +3V3 supply for BCM43907WLCSP SiP



POWER

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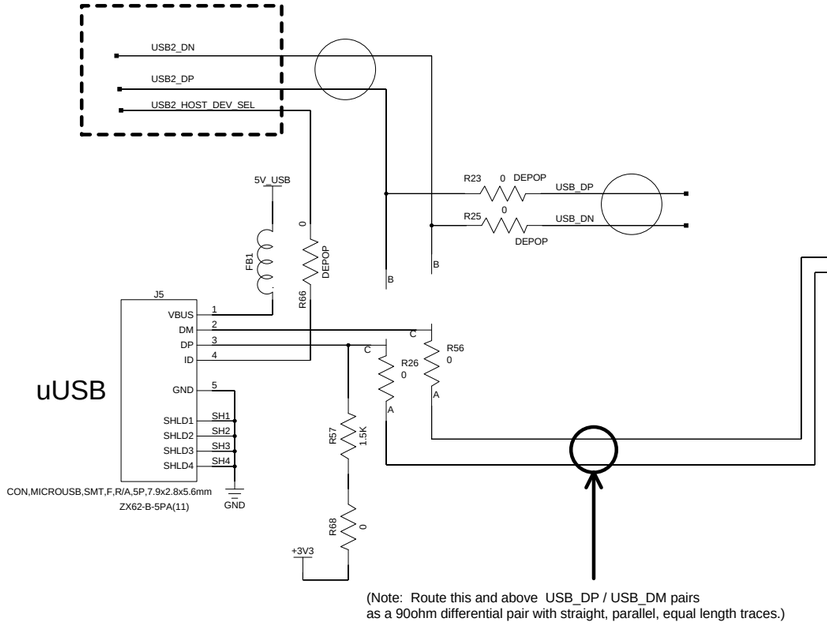
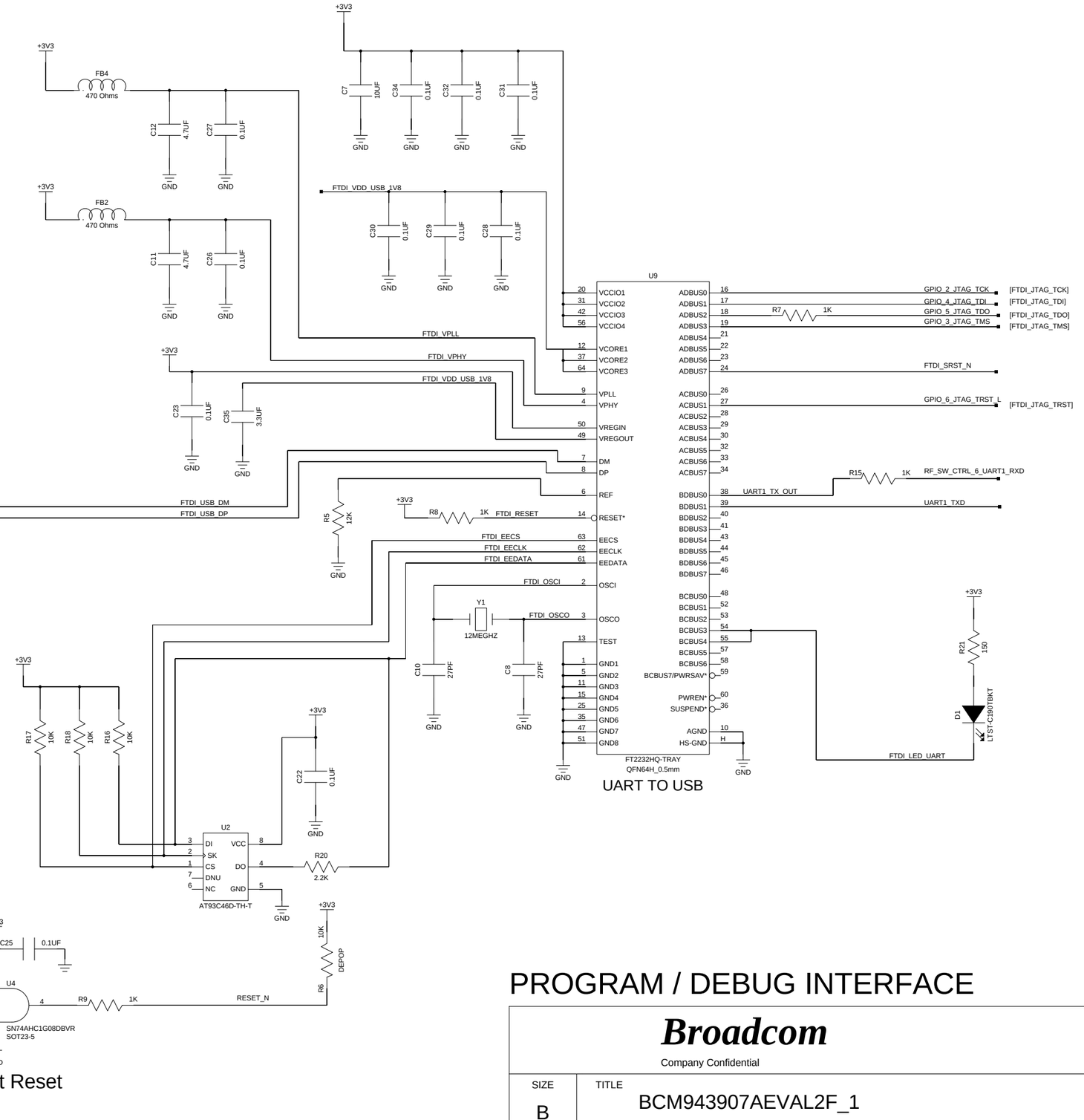
SIZE	TITLE	
B	BCM943907AEVAL2F_1	
DATE 05/10/2015:17:59		SHEET 4 OF 1

WICED py provision

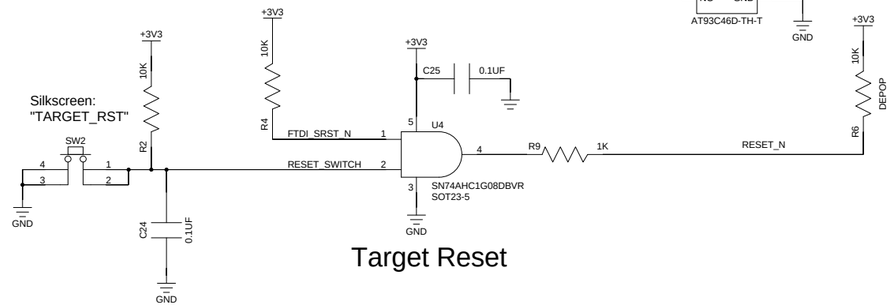


uUSB

(Note: Route this and above USB_DP / USB_DM pairs
as a 90ohm differential pair with straight, parallel, equal length traces.)



UART TO USB



Target Reset

PROGRAM / DEBUG INTERFACE

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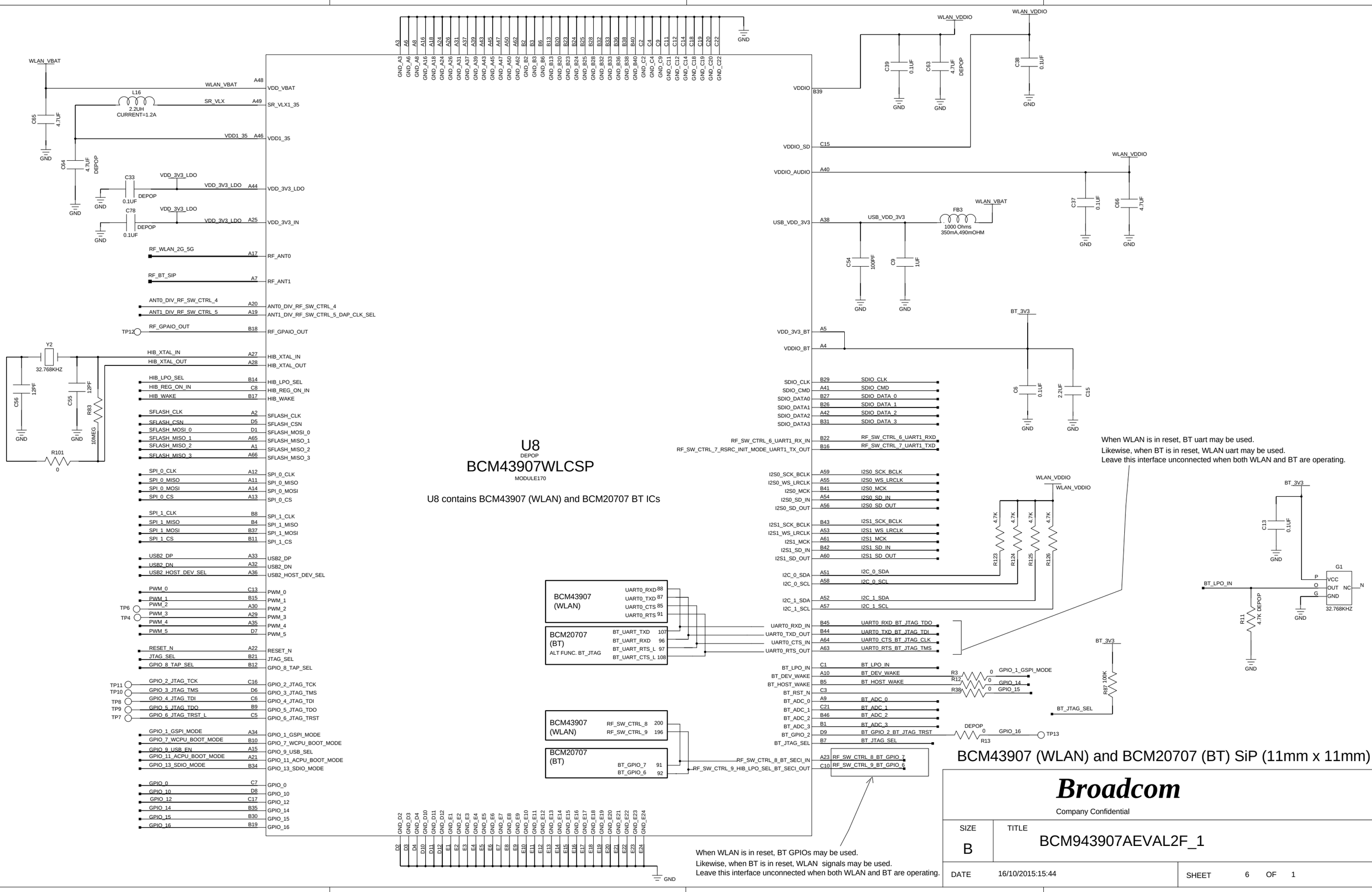
SIZE	TITLE
B	BCM943907AEVAL2F_1
DATE 07/10/2015:17:50	SHEET 5 OF 1



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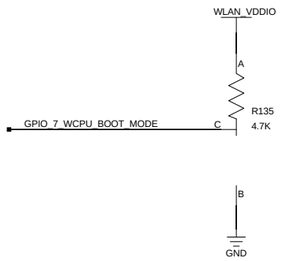
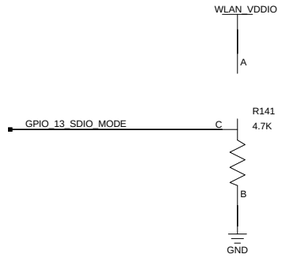
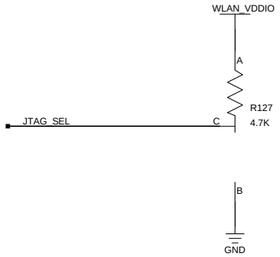
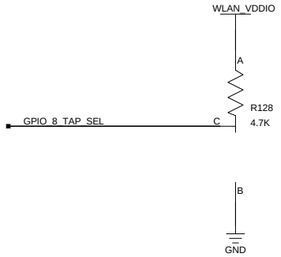
SIZE	TITLE
B	BCM943907AEVAL2F_1
DATE 16/10/2015:15:44	SHEET 6 OF 1

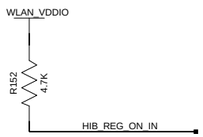


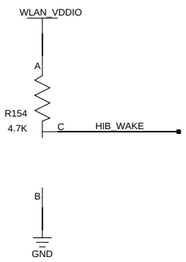


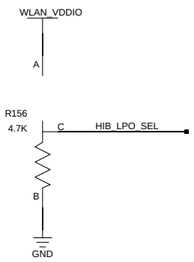
Pin	Strap Function	Strap Pull	
		Chip Default	Board Default
GPIO_1_GSPI_MODE	gSPI Mode	0	0
GPIO_7_WCPU_BOOT_MODE	WCPU Boot Mode : 0 = TCROM Boot 1 = TCMSRAM Boot	0	1 R135 = 4.7K to WLAN_VDDIO
GPIO_11_ACPU_BOOT_MODE	ACPU Boot Mode : 0 = SOCROM Boot 1 = SOCSRAM Boot	0	0
GPIO_13_SDIO_MODE	SDIO Mode : 0 = SDIO Device 1 = SDIO Host	0	0 R141= 4.7K to GND
			1
ANT1_RF_SW_CTRL_5	Host DAP Clock Sel	0	0
RF_SW_CTRL_7_UART1_TDX	Host RSRC Init	0	0
RF_SW_CTRL_9_BT_GPIO_6	LPO Sel : 0 = LPO from HIB	0	0

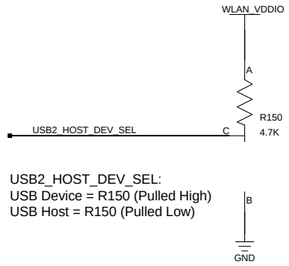




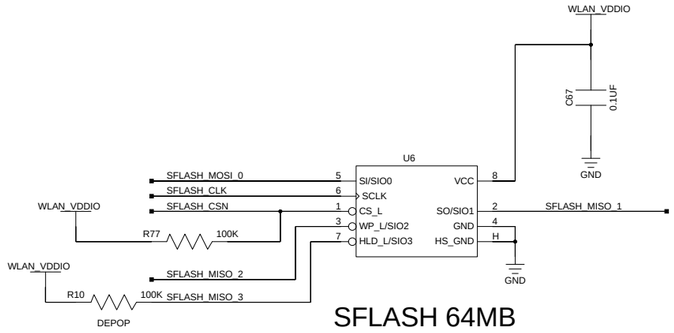








USB2_HOST_DEV_SEL:
USB Device = R150 (Pulled High)
USB Host = R150 (Pulled Low)



SFLASH 64MB

BOOTSTRAPS AND SFLASH

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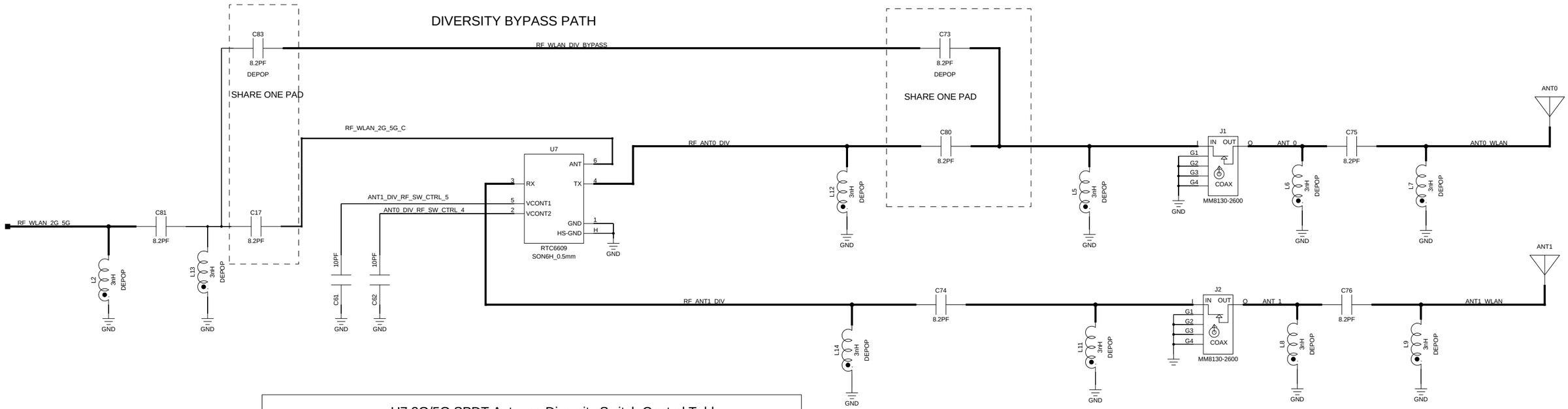
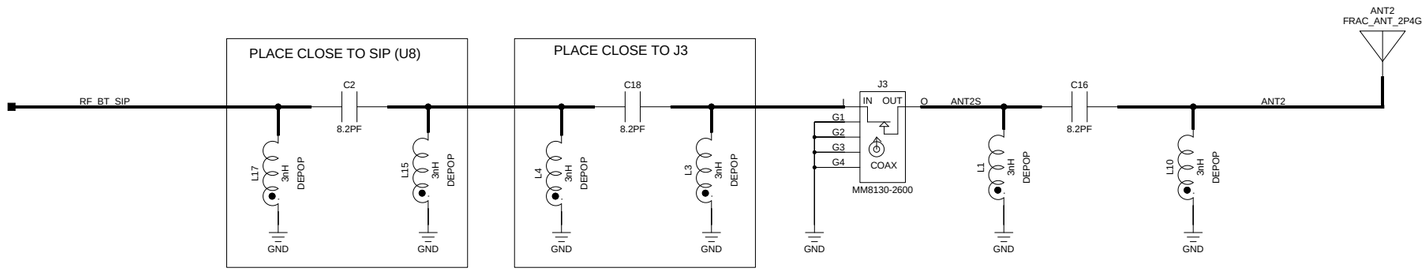
SIZE	TITLE	
B	BCM943907AEVAL2F_1	
DATE 06/10/2015:12:58		SHEET 7 OF 1



U7 2G/5G SPDT Antenna Diversity Switch Control Table		
MODE OF OPERATION Ant Diversity	ANT0_DIV_RF_SW_CTRL_4 SPDT (U7 Pin 6)	ANT1_DIV_RF_SW_CTRL_5 SPDT (U7 Pin 4)
RF_WLAN_2G_5G to Ant0	1	0
RF_WLAN_2G_5G to Ant1	0	1

ALL OTHER STATES UNDEFINED



RF FRONT-END (ANTs)

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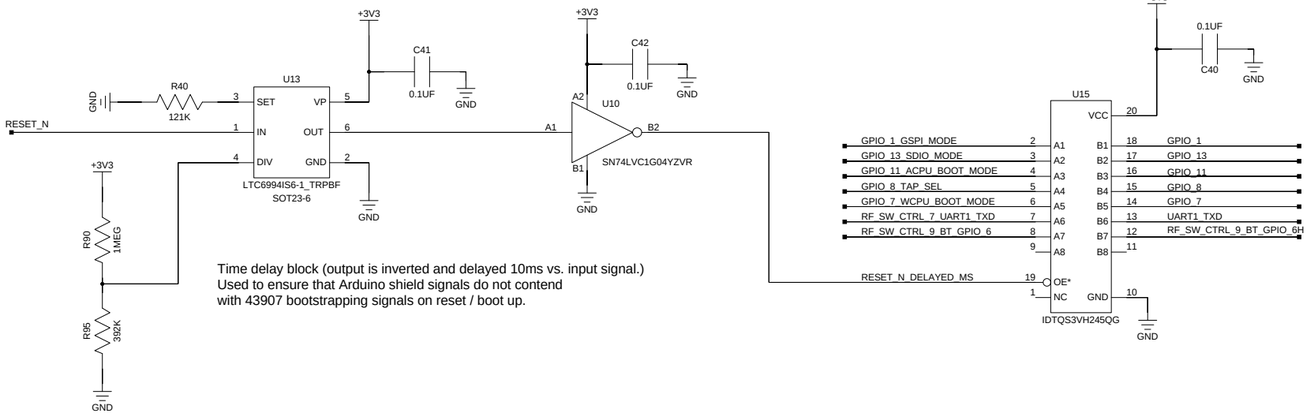
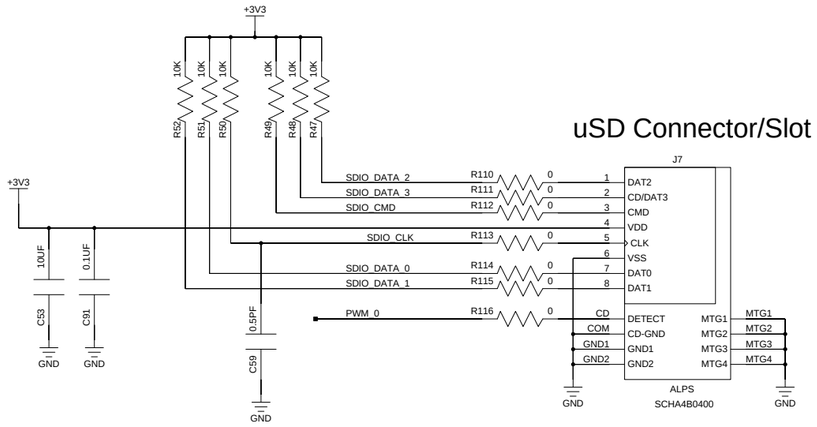
SIZE	TITLE
B	BCM943907AEVAL2F_1
DATE 15/10/2015:15:28	SHEET 8 OF 1

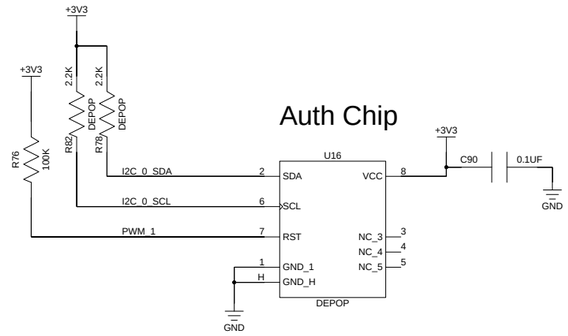
Reset Delay



uSD Connector/Slot



Auth Chip



DELAY, AUTH IC, SD

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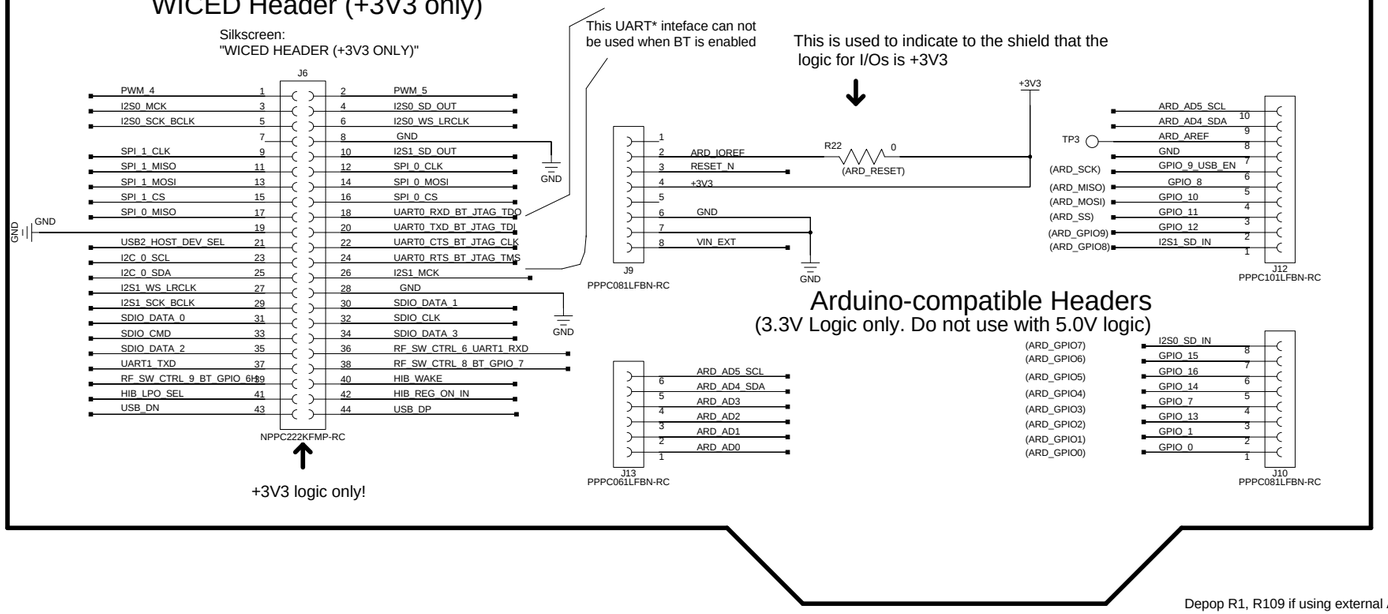
SIZE	TITLE	
B	BCM943907AEVAL2F_1	
DATE 05/10/2015:17:59		SHEET 9 OF 1

WICED Header (+3V3 only)

Silkscreen:
"WICED HEADER (+3V3 ONLY)"

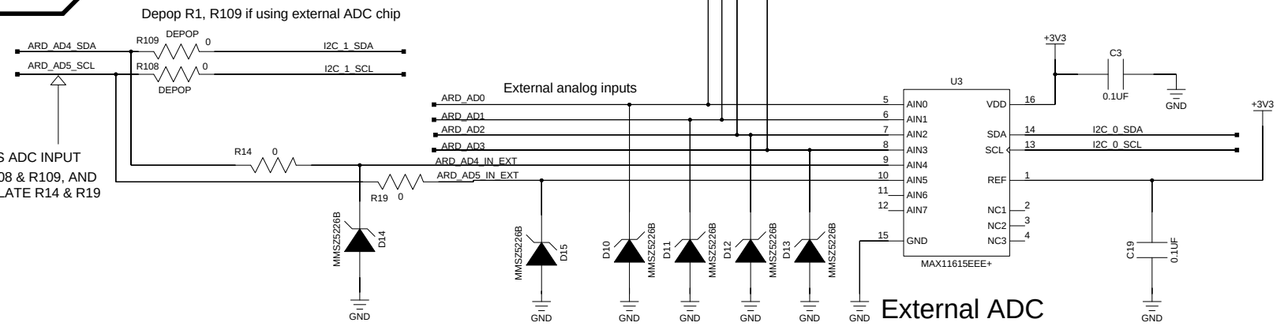


Arduino-compatible Headers

(3.3V Logic only. Do not use with 5.0V logic)

+3V3 logic only!

Depop R1, R109 if using external ADC chip



Place acrylic feet at the corners (or as close to) of the board on the bottom layer.
Make sure they to not overlap the edge of the board.

F3
NON PCB MOUNT PART
RUBBER,FEET,9.5X3.8mm,ACRYLIC TRANSPARENT
SJ5306

F4
NON PCB MOUNT PART
RUBBER,FEET,9.5X3.8mm,ACRYLIC TRANSPARENT
SJ5306

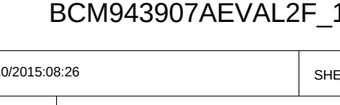
F5
NON PCB MOUNT PART
RUBBER,FEET,9.5X3.8mm,ACRYLIC TRANSPARENT
SJ5306

F6
NON PCB MOUNT PART
RUBBER,FEET,9.5X3.8mm,ACRYLIC TRANSPARENT
SJ5306

ZJ1
NON PCB MOUNT PART
CBL,USB-A/MICROUSB-B,M/M,2ft,4/5P DATA CABLE,BROADPEBBLE
99-110080-0001

When using BT_ADC by populating these resistors,
depop external ADC chip U3 first.

BT_ADC supports maximum sample speed of 96ksps
For U3, it is 94.6ksps.



Populate R14, R19 AND
depop R109, R108 if using external ADC chip

DOC1
DOCUMENT
SCHEMATIC DIAGRAM
824-129830-0010

PCB1
PRINTED CIRCUIT BOARD
200-129830-0010

XX1
NON PCB MOUNT PART
SHIELD
210-129830-0001
DEPOP

ARDUINO AND WICED HEADERS

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SIZE	TITLE
B	BCM943907AEVAL2F_1
DATE 07/10/2015:08:26	SHEET 10 OF 1