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Rev01 Initial Release Schematic - 03/06/2015

43907 Updates - 03/17/2015

- Added Separate Module Pin VDD_3V3_IN_2 for VDDIO_RF and OTP_VDD_3V3 Supplies of 43907

43907 Updates - 03/20/2015

- Added 100K Pull Up Resistor on SFLASH_N and 10K Pull Up resistor on RESET_N

43907 Updates - 04/03/2015

- Added C5 (01005 Case Size Cap) and FB3 (0201 Case Size Ferrite Beads at Pin 200 of U1 (43907 Chip)

- Added C6, L4 and L3 place holders for additional matching on RF Signal

43907 Updates - 04/13/2015

- C5 Replaced With 0.033uF GRM022R60J333ME15 Part

- FB3 Replaced with BLM03HG102SN1B Part

- Added FB7 Ferrite Bead BLM03HG102SN1B on U1 Pin 305 and 307, VDDIO_RMII Supply

- Updated RF_SW_CTRL_8 and RF_SW_CTRL_9 net names to show UART2 in them

43907 Updates - 05/22/2015

- C5 capacitor changed to No Load (Depop)

- FB3 Replaced with 0 Ohms Resistor Part

- Changed XTAL Load Caps C23 and C24 to 33pF GRM0225C1C330JD05D Part

- Updated FL1 Diplexer to TDK : DPX205850DT-9043B2BR

- Updated the 2G RF Matching : L1 = 3.6nH Murata LQP03TN3N6B02D, C15 = NoLoad (Depop)

DOCUMENT

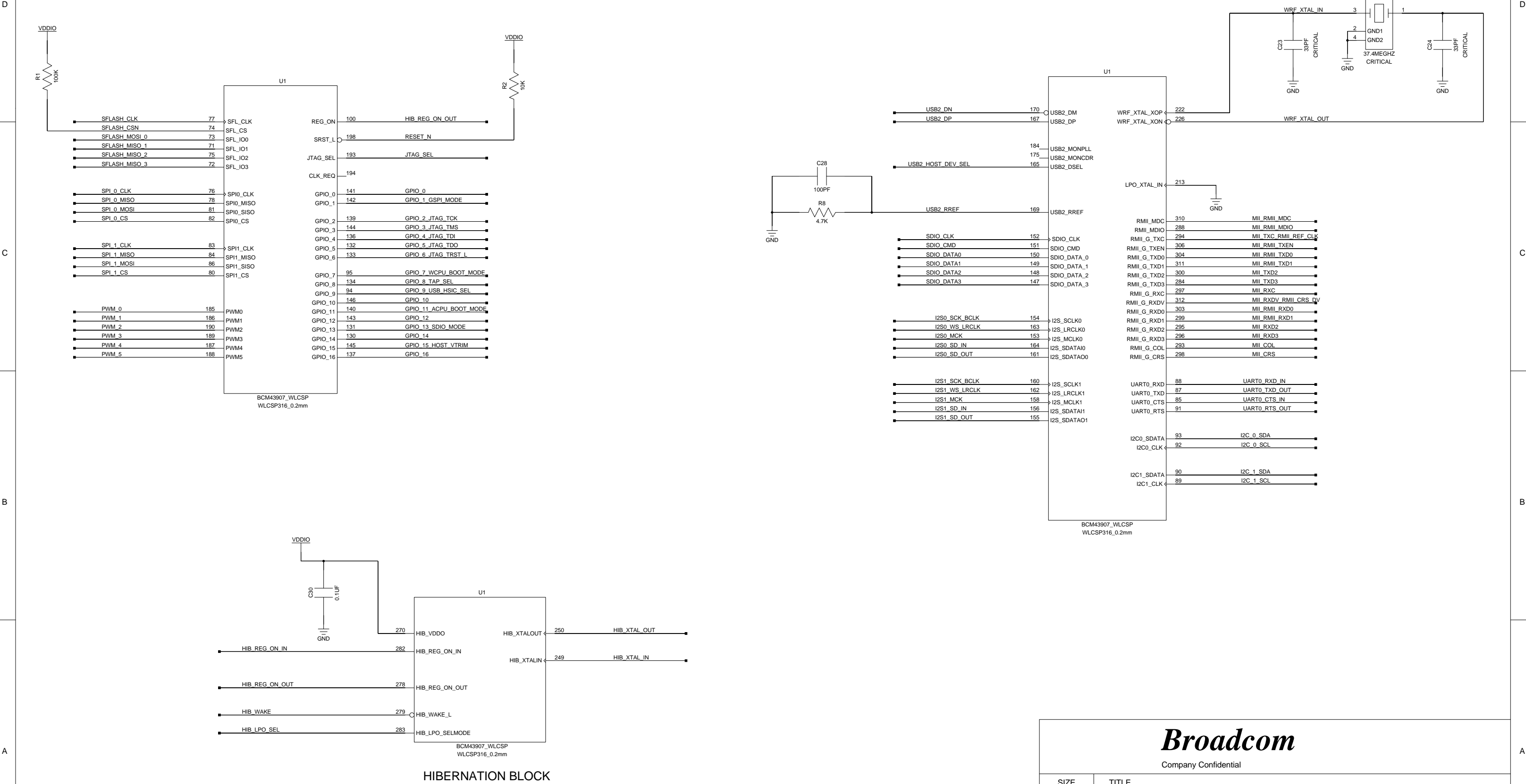
SCHEMATIC DIAGRAM

824-129085-0010

PRINTED CIRCUIT BOARD

200-129085-0010

Approvals		<div><div><div><div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div></div></div></div><div><div><div><div></div><div></div><div><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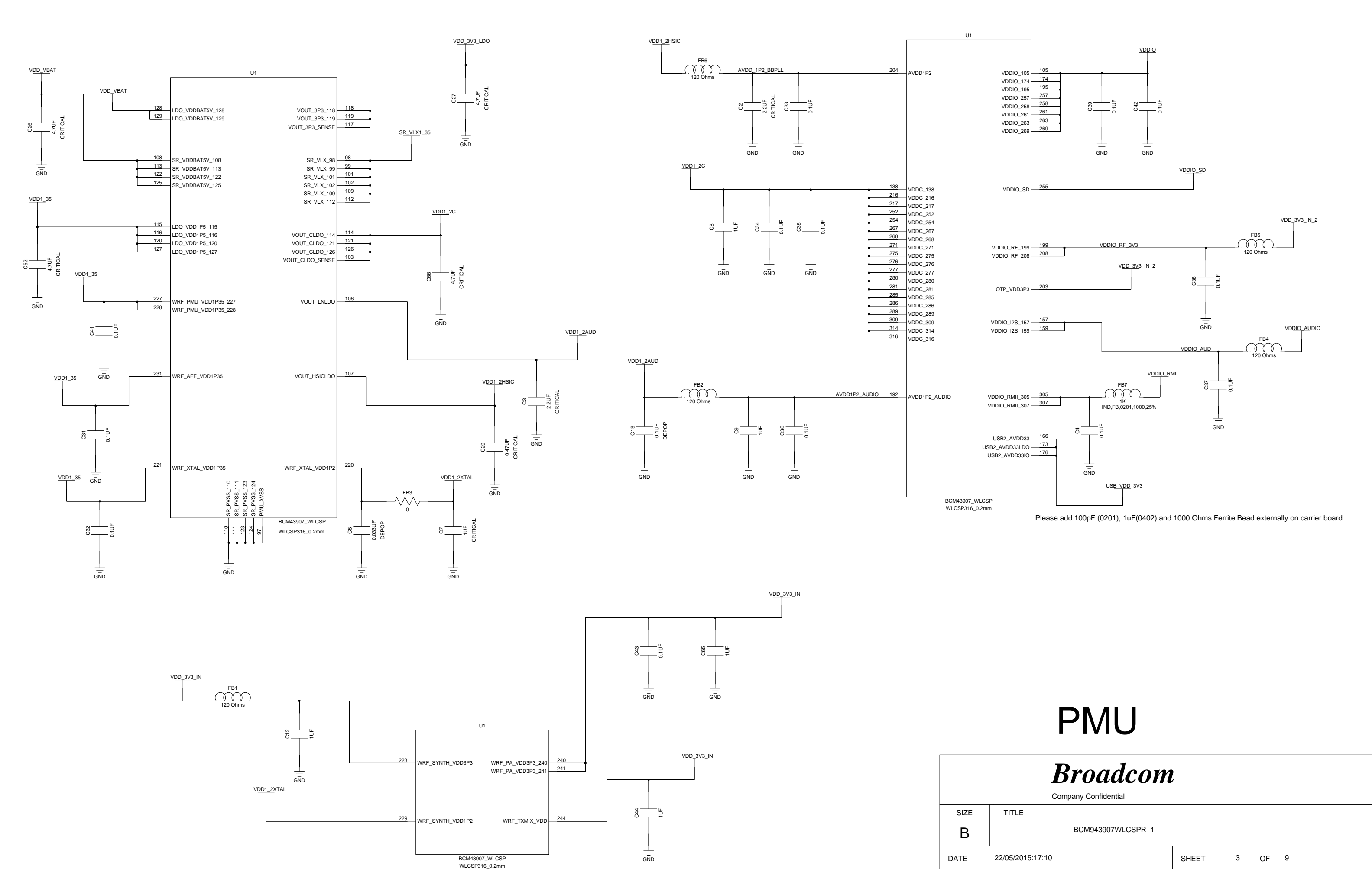
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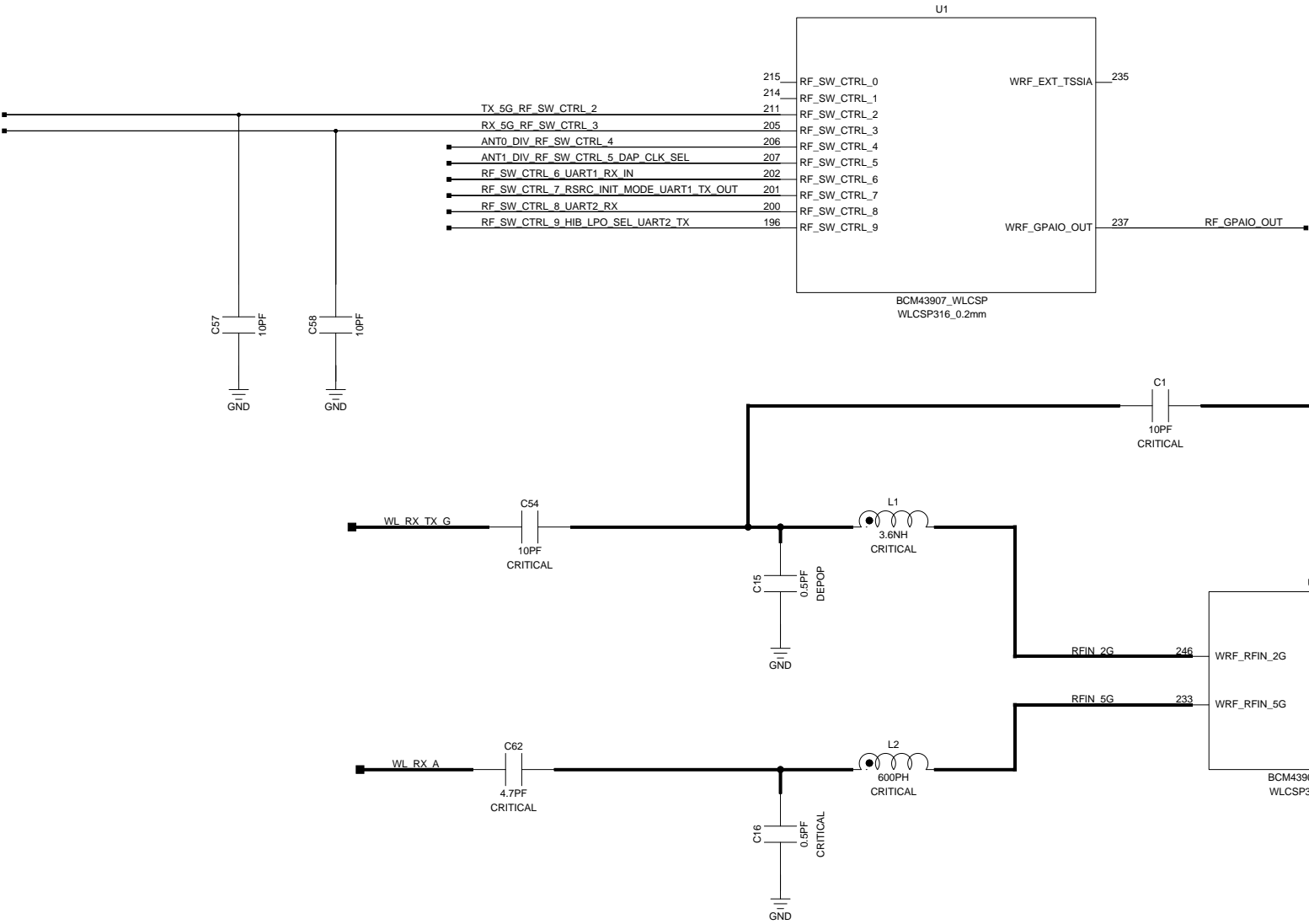
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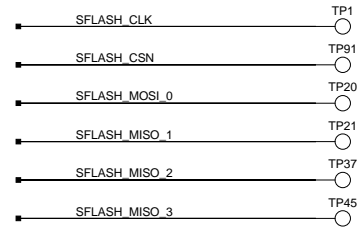
Broadcom

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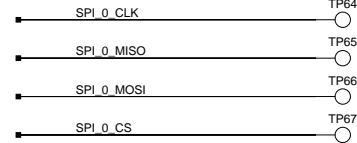
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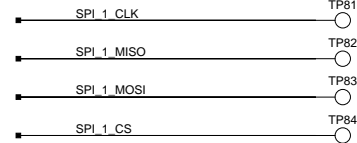
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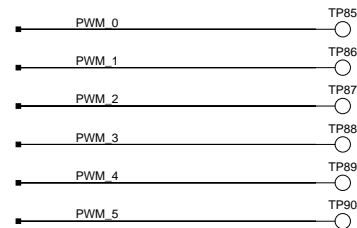
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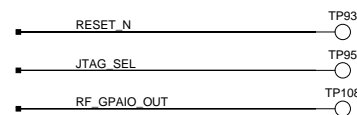
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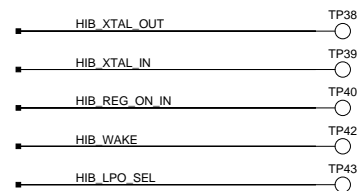
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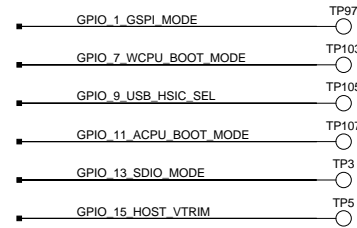
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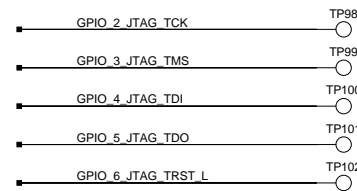
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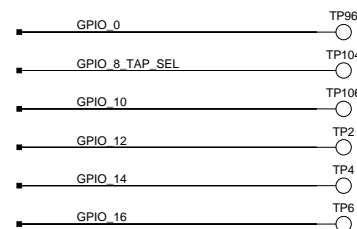
Straps on GPIO's



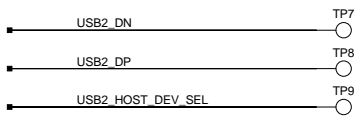
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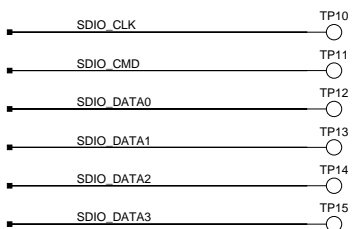
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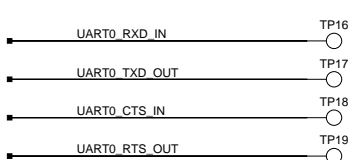
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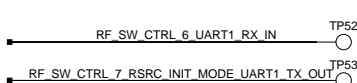
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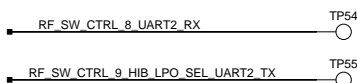
FAST UART



SLOW UART1



SLOW UART2

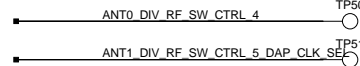


Strapping Options

Pin	Strap Function	Internal Strap Pull Chip Default
GPIO_1	gSPI Mode	0
GPIO_7	WCPU Boot Mode : 0 = TCROM Boot 1 = TCMSRAM Boot	0
GPIO_9	USB/HSIC Sel : 0 = HSIC PHY 1 = USB PHY	0
GPIO_11	ACPU Boot Mode : 0 = SOCROM Boot 1 = SOCSRAM Boot	0
GPIO_13	SDIO Mode : 0 = SDIO Device 1 = SDIO Host	0
GPIO_15	Host Vtrim Enable 0 = Host Vtrim Disable 1 = Host Vtrim Enable	0
RF_SW_CTRL_5	Host DAP Clock Sel	0
RF_SW_CTRL_7	Host RSRC Init	0
RF_SW_CTRL_9	LPO Sel : 0 = LPO from HIB 1 = Internal 32KHz LPO	0

Note : GPIO_15 is a Strap for A0 IC Only and not for B0

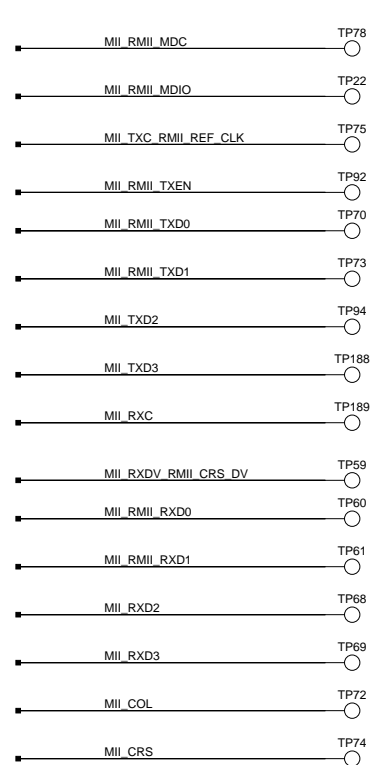
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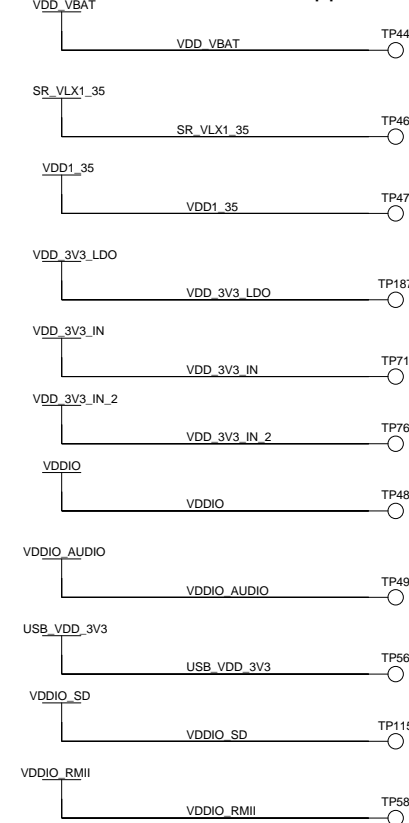
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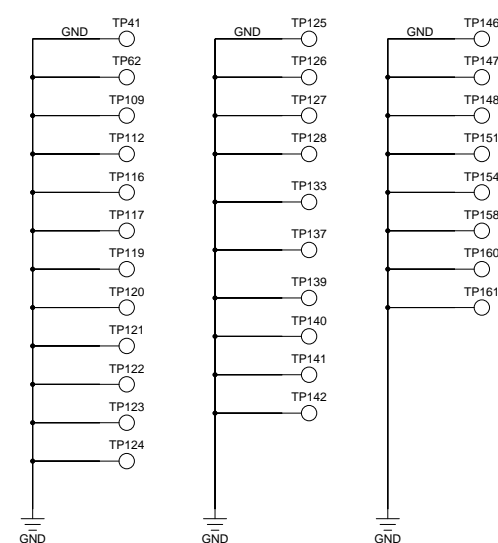
MII/RMII



BCM43907 Supplies



GND



Module Pins

PMU Section Recommendation By Broadcom Corporation PMU Team

1. External 43909 CBUCK Inductor For Any inductor any other than LQM2MPN2R2MG0, please review the new inductor with PMU team.

2. BCM43907 PMU Caps :

- a. VBAT Cap : Nominal value 4.7uF. 0402 inch, 10V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 1.645uF at 4.8V.

ii.Effective capacitance should NOT drop below 1.88uF at 4.2V

iii.Effective capacitance should NOT drop below 2.2uF at 3.6V

iv.Recommended cap: Murata GRM155R61A475M or any cap matching or better than above DC bias profile

v.This 4.7uF can be shared with SR_VDDBAT5V & LDO_VDDBAT5V pins but the cap must be closer to SR_VDDBAT5V.
- b. CBUCK CapNominal value 4.7uF. 0402 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 3.622uF at 1.35V.

ii.Recommended cap: Murata GRM155R60J475ME87 or any cap matching or better than above DC bias profile

iii.I noted you used GRM155R61A475MEAA 10V cap; this is fine but it's an overkill & more expensive than 6.3V cap.
- c. LDO3P3 CapNominal value 4.7uF. 0402 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 1.773uF at 3.3V.

ii.Recommended cap: Murata GRM155R60J475ME87 or any cap matching or better than above DC bias profile
- d. CLDO Cap : Nominal value 4.7uF. 0402 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 3.91uF at 1.2V.

ii.Recommended cap: Murata GRM155R60J475ME87 or any cap matching or better than above DC bias profile
- d. LNLDO Cap :Nominal value 2.2uF. 0402 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 1.87uF at 1.2V.

ii.Recommended cap: Murata GRM155R60J225ME15 or any cap matching or better than above DC bias profile

iii.If you want to use 2 pcs of 0201 inch size 1uF, the total effective capacitance at 1.2V DC bias must meet 1.87uF typical.
- e. HSICLDO CapNominal value 0.47uF. 0201 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 0.376uF at 1.2V.

ii.Recommended cap: Murata GRM033R60J474ME90 or any cap matching or better than above DC bias profile

PMU Section Recommendation By Broadcom Corporation PMU Team cntd...

4. Module Layout : We consider module layout the same as FCFBGA package substrate routing.

PMU team needs to review the module pins relating to VBAT, SR_VLX, VSS which can impact CBUCK chip reliability.

Module Layout Routing Guidelines

Please ensure module designer extracts all these parasitic inductances & resistances for our review. The following needs to be achieved :

a. SR_VDDBAT5V pin to VBAT cap :

- i. Top-layer routing, length < 42mils (1.066mm), width > 10mils (0.254mm)
- ii. Routing ESR < 5mOhms, ESL < 400pH at 4MHz - 200MHz

b. CBUCK output cap to LDO_VDD1p5 pin:

- i. 2nd layer routing, length < 42mils(1.066mm), width>10mils(0.254mm)
- ii. Routing ESR<10mOhms.

c. SR_VLX pin to inductor:

- i. Routing length < 80mils(2.032mm), 10mils(0.254mm)<width<30mils(0.762mm)

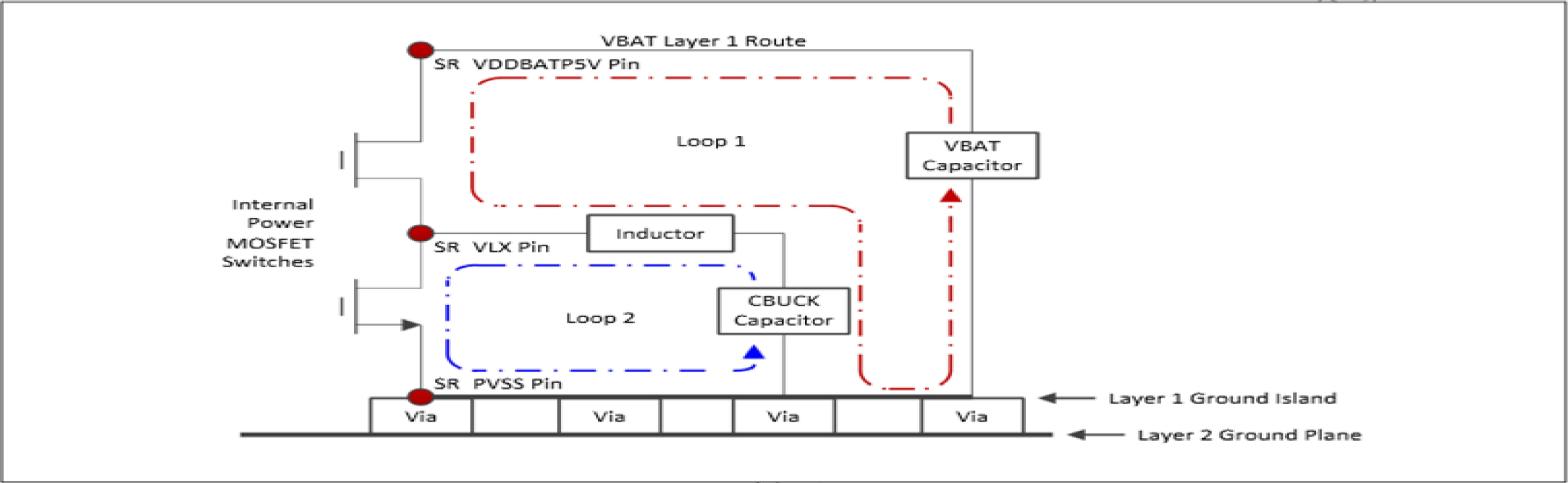
d. Top-Layer GND island connecting SR_PVSS pin, CBUCK cap gnd, VBAT cap gnd:

- i. Routing ESR<5mOhms, ESL<300pH at 4MHz - 200MHz

PMU Notes from Broadcom Corporation PMU Team

Potential CBUCK Noise if Routing Not Optimized

Figure 17: EMI Loops in Buck Switching Regulator



Picture Above Shows Two Loops through MOSFETs of CBUCK

- 1)Each loop starts from a cap and ends at its ground terminal.
- 2)The area within each loop is proportional to the EMI. Routing of sensitive signals through the areas
- 3)bounded by these two loops should be strictly avoided.
- 4)Top-layer routings are used to conduct switching currents to avoid micro-via inductances.
- 5)VBAT, CBUCK cap sits on a top-layer gnd island connecting to SR_PVSS pin directly.
- 6)Micro-vias are still used to connect this top-layer gnd island to 2nd-layer GND Plane and this only carries DC currents.
- 7)The 2nd Layer GND Plane also acts as a shield over the 2 EMI loops to prevent noise radiation to other layers.