

GPIO FUNCTIONALITY FROM BCM43907 PERSPECTIVE			
Actual PAD Names on BCM43907 WLCSP PKG	GPIO Definition on BCM43907 GCI Bus ---2nd # is----	Input or Output from BCM43907	Description of Functionality
GPIO_0	GPIO_0 1	Input	AUDIO_MULTI_SW
GPIO_1	GPIO_1 1	Output	43907 Wakes up BT IC (BT_DEV_WAKE)
GPIO_2	GPIO_2 1*	NC - JTAG	Not Used ----- JTAG_TCK - 4 Debug
GPIO_3	GPIO_3 1*	NC - JTAG	Not Used ----- JTAG_TMS - 4 Debug
GPIO_4	GPIO_4 1*	NC - JTAG	Not Used ----- JTAG_TDI - 4 Debug
GPIO_5	GPIO_5 1*	NC - JTAG	Not Used ----- JTAG_TDO - 4 Debug
GPIO_6	GPIO_6 1*	NC - JTAG	Not Used ----- JTAG_TRST_L - 4 Debug
GPIO_7	GPIO_7 1	Input	AUDIO_FWD_SW
GPIO_8	GPIO_8 1	Input	TAP_SEL
GPIO_9	GPIO_9 1	Input	AUDIO_VOL_UP_SW
GPIO_10	GPIO_10 1	Input	AUTH IC RESET
GPIO_11	GPIO_11 1	NC	Not Used
GPIO_12	GPIO_12 1	Input	CODEC PDN
GPIO_13	GPIO_13 1	Input	AUDIO_VOL_DOWN_SW
GPIO_14	GPIO_14 1	Input	BT IC Wakes up 43907 (BT_HOST_WAKE)
GPIO_15	GPIO_15 1	Input	43907 Reset to BT IC (LOW = RESET BT 707)
GPIO_16	GPIO_16 1	Output	Battery Charger Interrupt
PWM_0	GPIO_18 3	Input	Enable +3.3V SW Regulator PSM mode ( Power Save Mode )
PWM_1	GPIO_19 3	Output	Enable +2.0V SW Regulator
PWM_2	GPIO_20 3	Output	Enable +1.8V LDO
PWM_3	GPIO_21 3	Input	Enable Green LED
PWM_4	GPIO_22 3	Input	Enable Red LED
PWM_5	GPIO_23 3	Input	AUDIO_BCK_SW
SPI_0_CLK	GPIO_25 3	Input	Audio Interrupt
SPI_0_MISO	GPIO_24 3	Input	AUDIO_PLAY_PAUSE_SW
SPI_0_MOSI	GPIO_26 3	IN / OUT	TEST POINT
SPI_0_CS	GPIO_27 3	IN / OUT	TEST POINT
I2C0_SDATA	GPIO_28 3	IN / OUT	I2C0
I2C0_CLK	GPIO_29 3	IN / OUT	I2C0

DOCUMENT

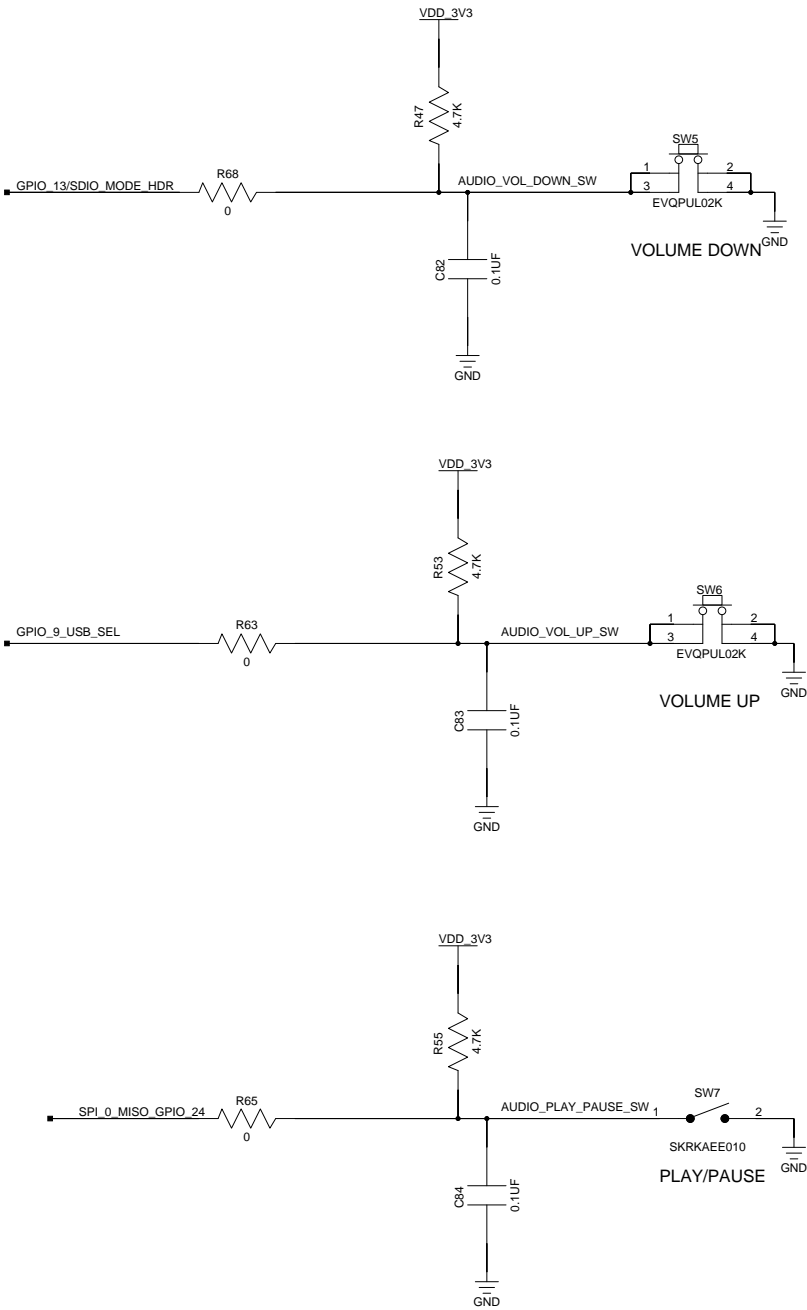
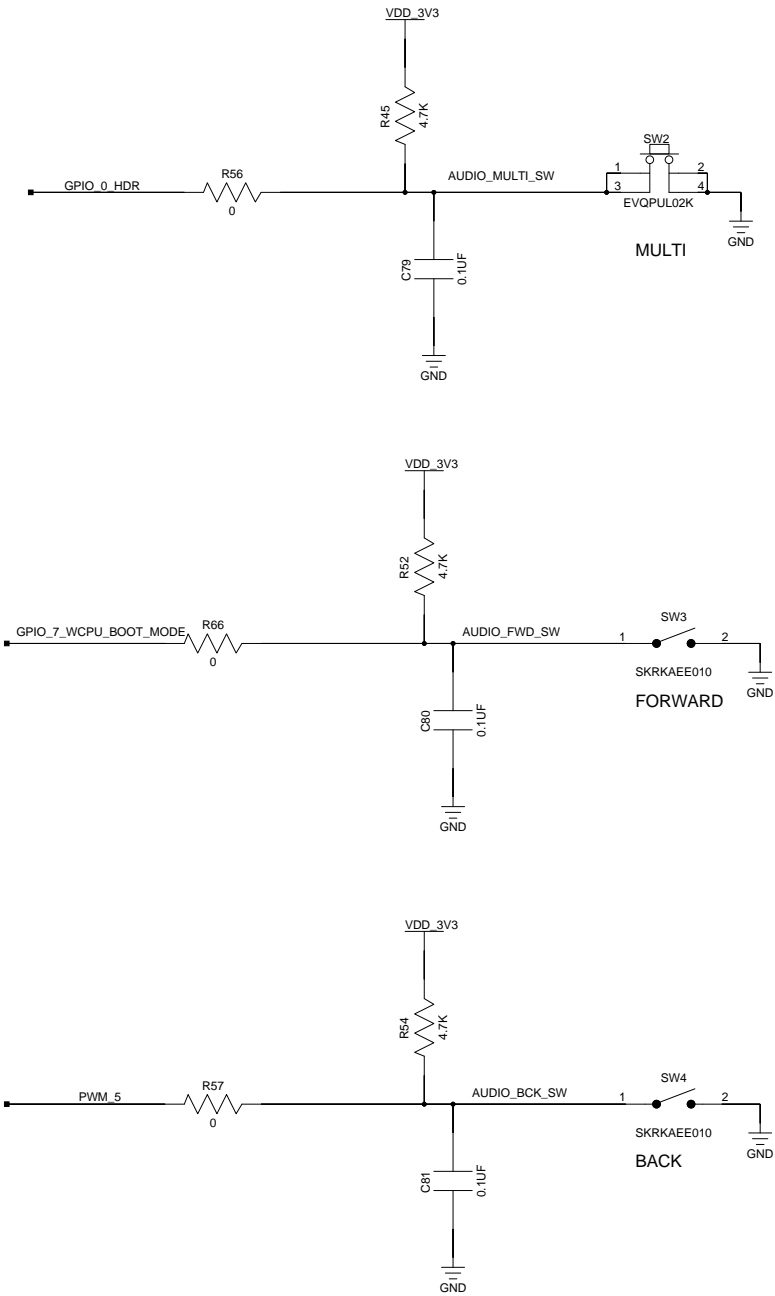
SCHEMATIC DIAGRAM  
824-130092-0010

PRINTED CIRCUIT BOARD

200-130092-0010

Approvals		<div><div>Broadcom</div><div>Company Confidential</div></div>			
Designer	Date				
Reviewer	Date	SIZE B	TITLE BCM943907WAE2_1		
Reviewer	Date	Designer MILIU		Drawing Number 824-130092-0010	Version 01
Reviewer	Date	DATE13/11/2015:10:31			SHEET1 OF 7

AUDIO SWITCHES ARRAY



## D



## A



## 1



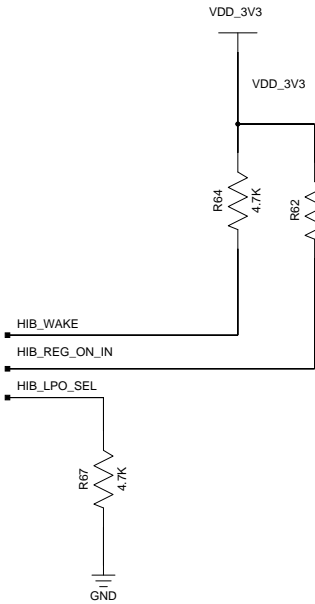
# Power Supplies



SIZE <b>B</b>	TITLE BCM943907WAE2_1		
DATE	13/11/2015:10:05	SHEET	3 OF 7

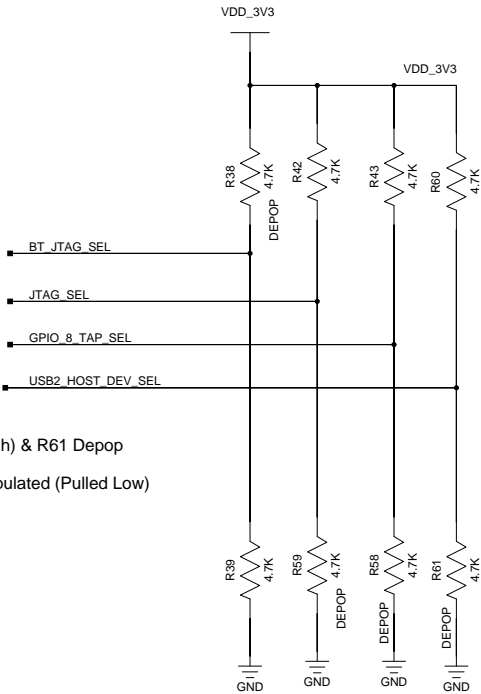
Pin	Strap Function	Strap Pull	
		Chip Default	Board Default
GPIO_1	gSPI Mode	0	
GPIO_7	WCPU Boot Mode : 0 = TCROM Boot 1 = TCMSRAM Boot	0	1 REFER TO AUDIO SWITCHES ARRAY
GPIO_9	USB/HSIC Sel : 0 = HSIC PHY 1 = USB PHY	0	1 REFER TO AUDIO SWITCHES ARRAY
GPIO_11	ACPU Boot Mode : 0 = SOCROM Boot 1 = SOCSRAM Boot	0	
GPIO_13	SDIO Mode : 0 = SDIO Device 1 = SDIO Host	0	
RF_SW_CTRL_5	Host DAP Clock Sel	0	
RF_SW_CTRL_7	Host RSRC Init	0	

HIBERNATION STRAPPING

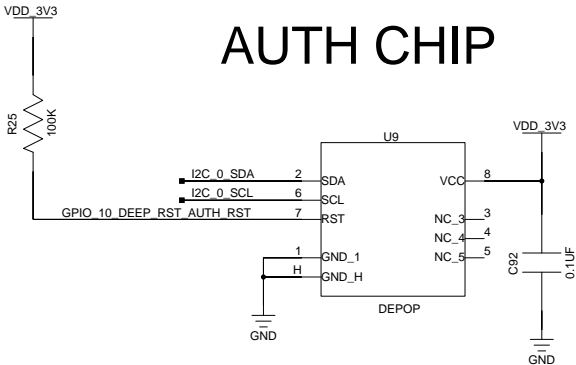


USB2\_HOST\_DEV\_SEL

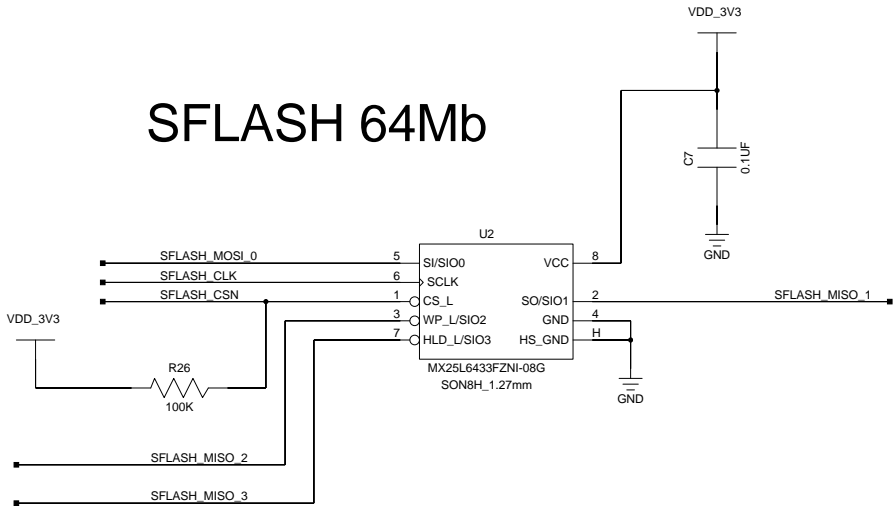
USB Device : R60 Populated (Pulled High) & R61 Depop  
USB Host : R60 Depopped & R61 Populated (Pulled Low)



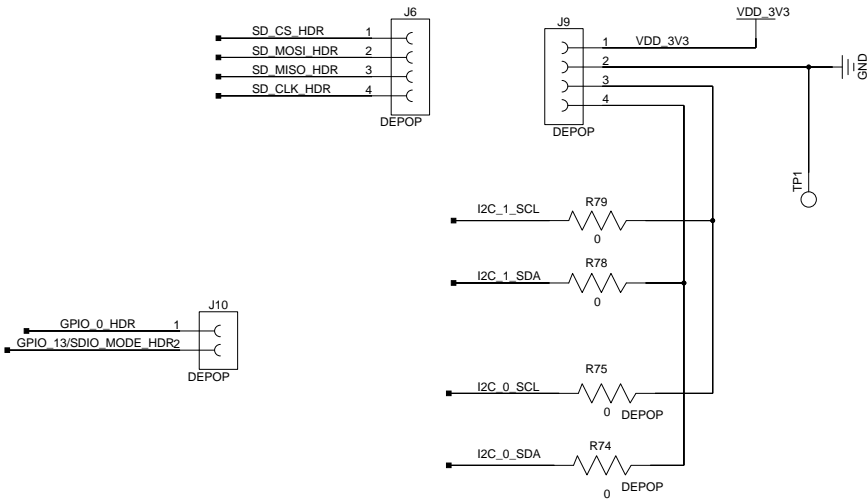
AUTH CHIP



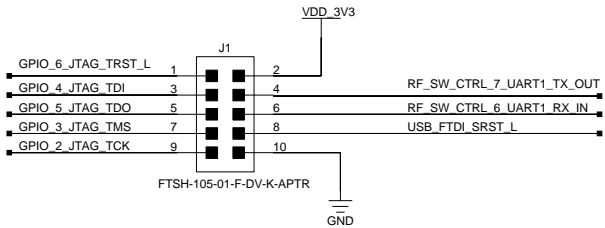
SFLASH 64Mb



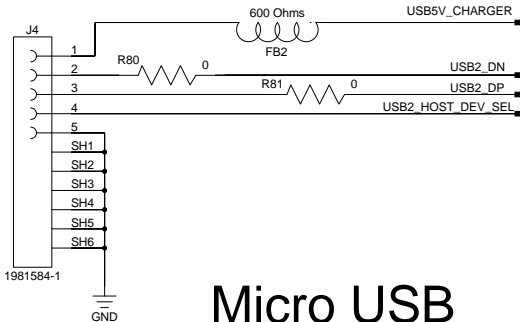
Display 2.54mm Header



JTAG/UART1 Micro Header



Micro USB



Straps + SFLASH + MISC

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SIZE B	TITLE BCM943907WAE2_1		
DATE	02/12/2015:14:03	SHEET	4 OF 7

D

General Vp decoupling

C

B

A

4

3

2

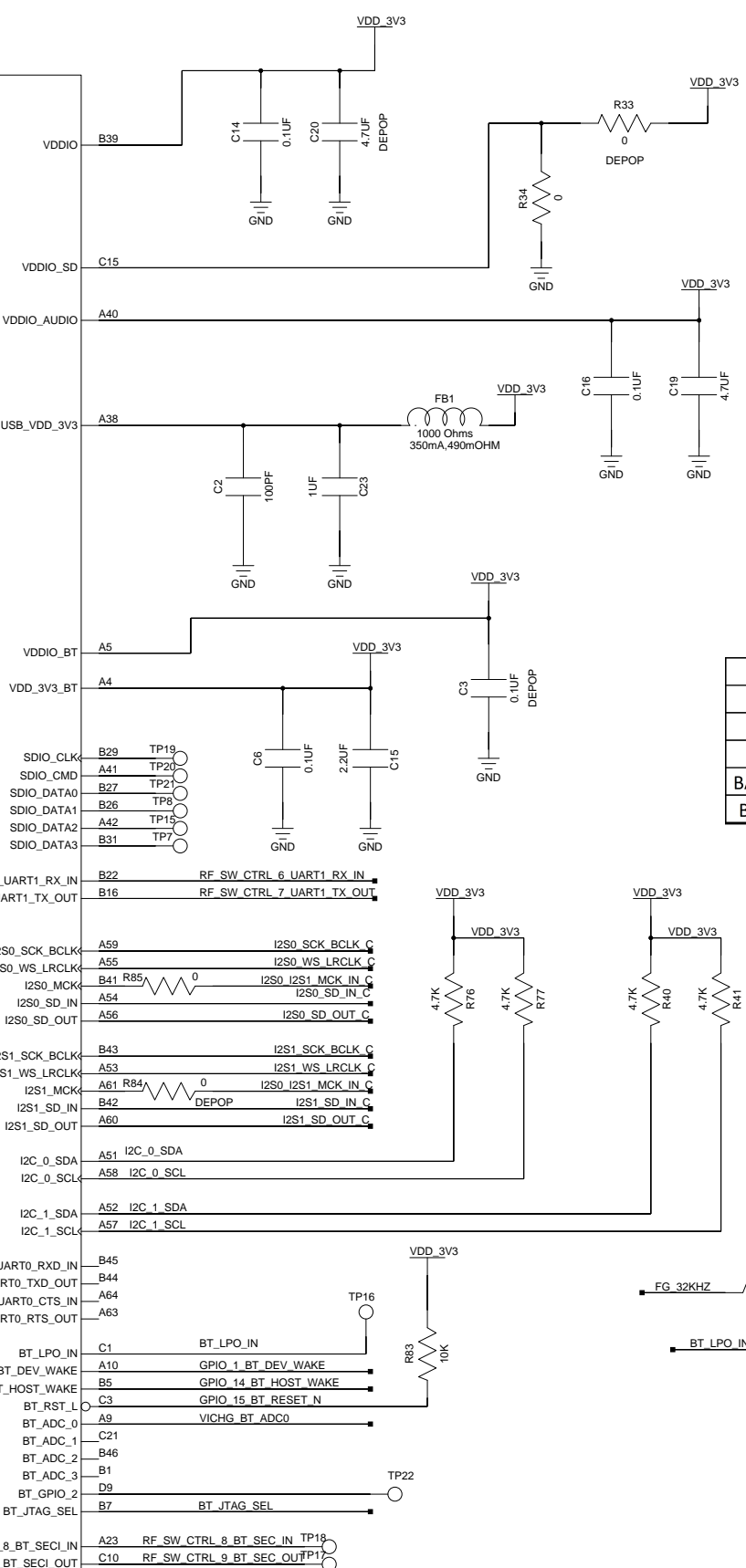
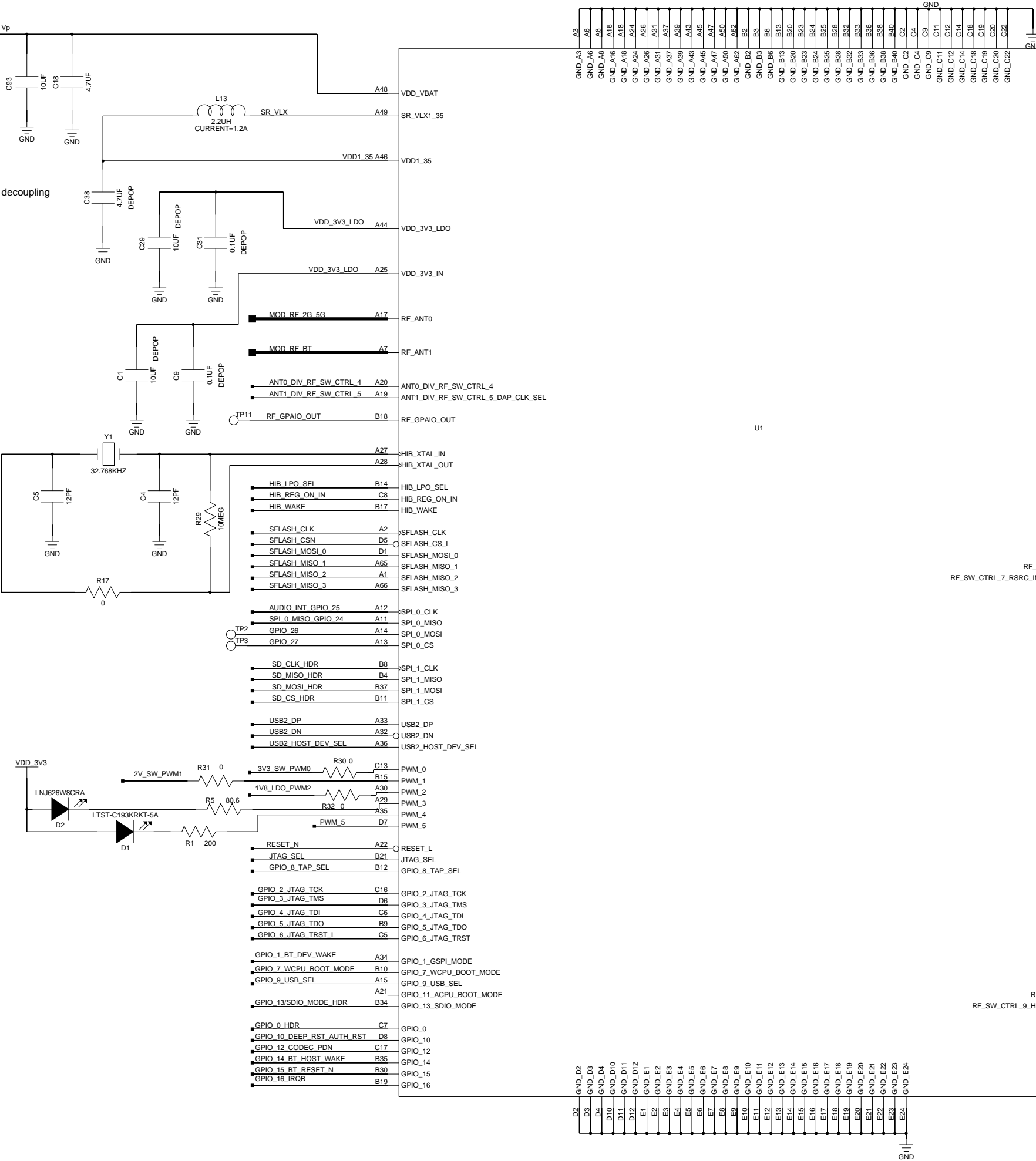
1

D

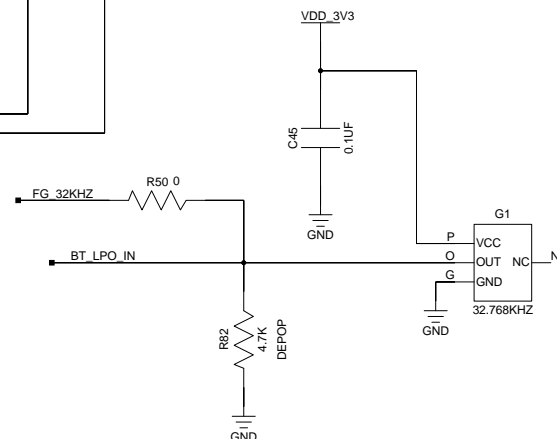
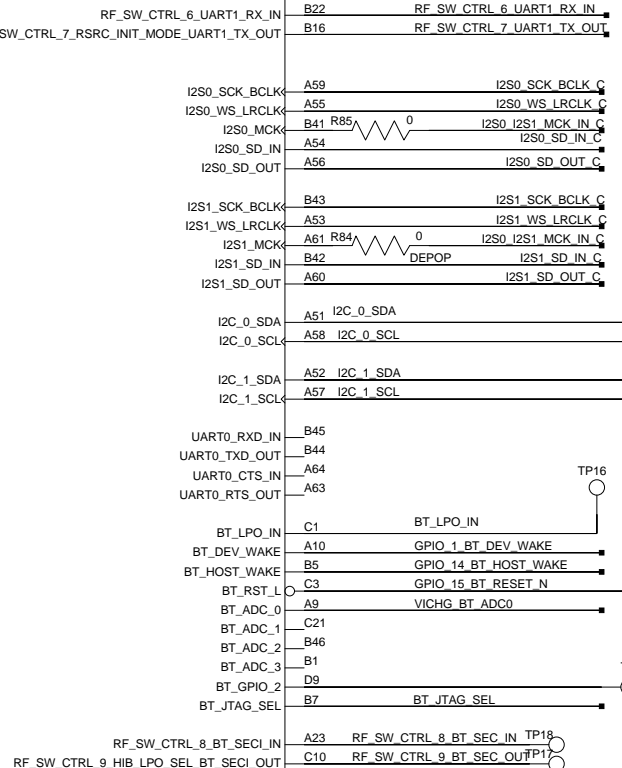
C

B

A



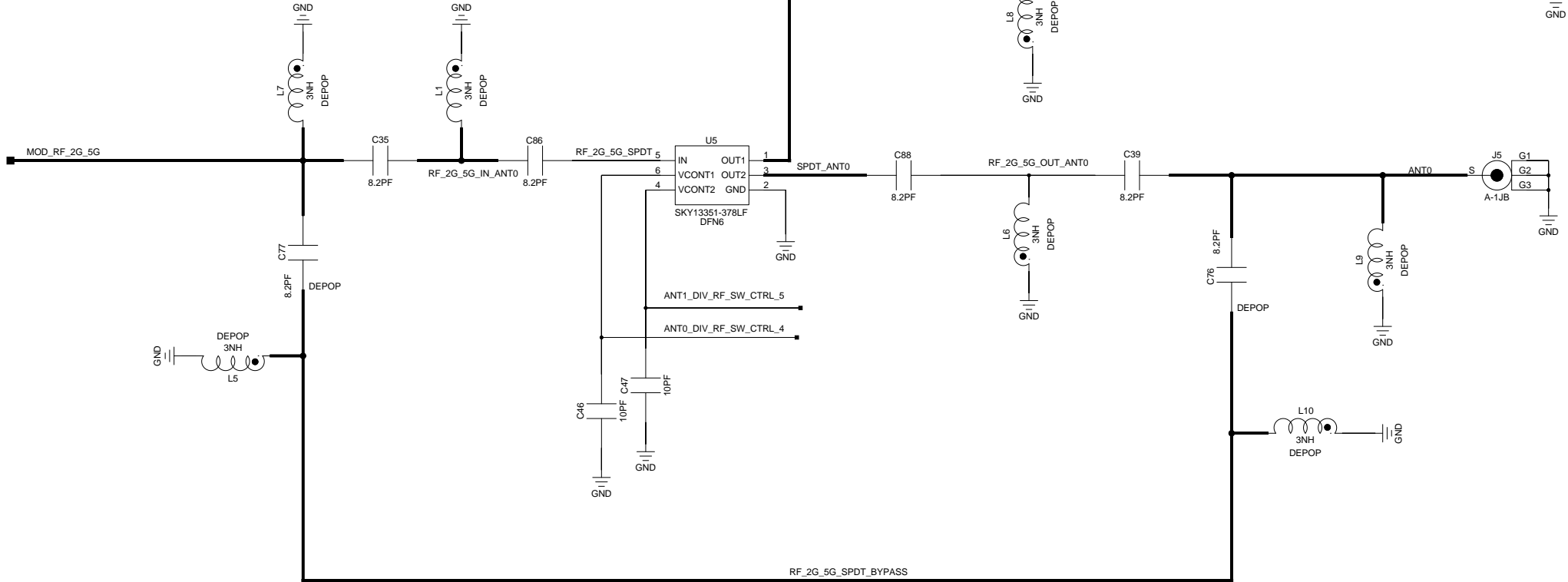
I2C_0 BUS	
DEVICE	I2C ADDRESS
AUDIO CODEC ( U6 )	0X12
AUTH CHIP ( U9 )	0X10
BATTERY CHARGER ( U8 )	0X6A
BATTERY GAUGE ( U11 )	0X6C



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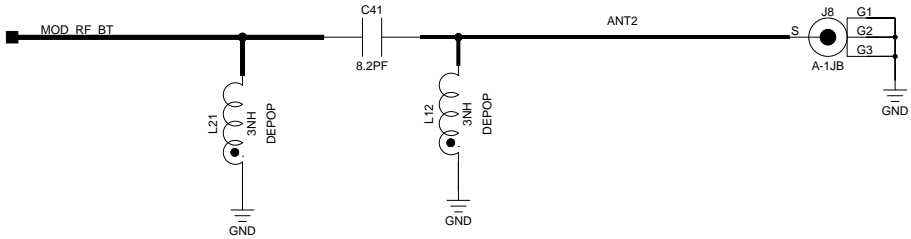
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SIZE	TITLE	DATE	02/12/2015:14:05	SHEET	5	OF	7
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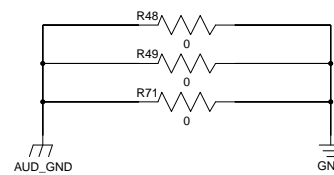
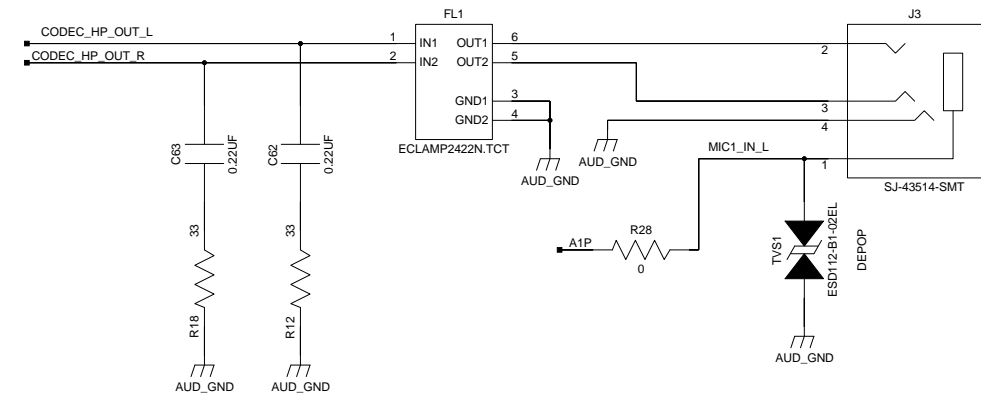
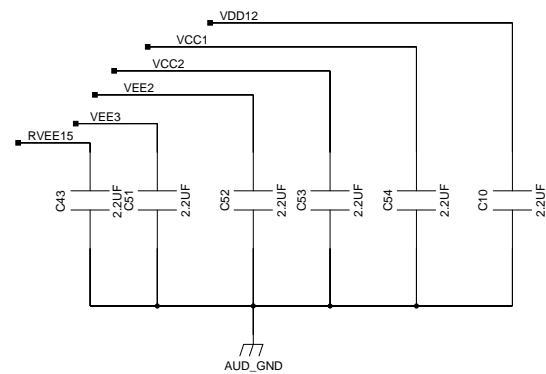
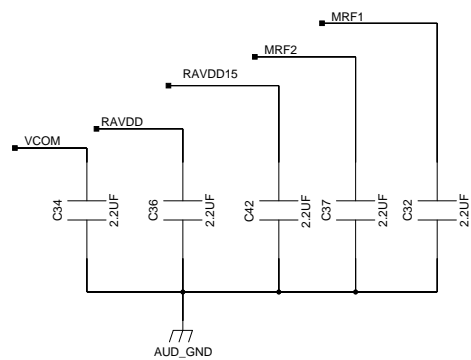
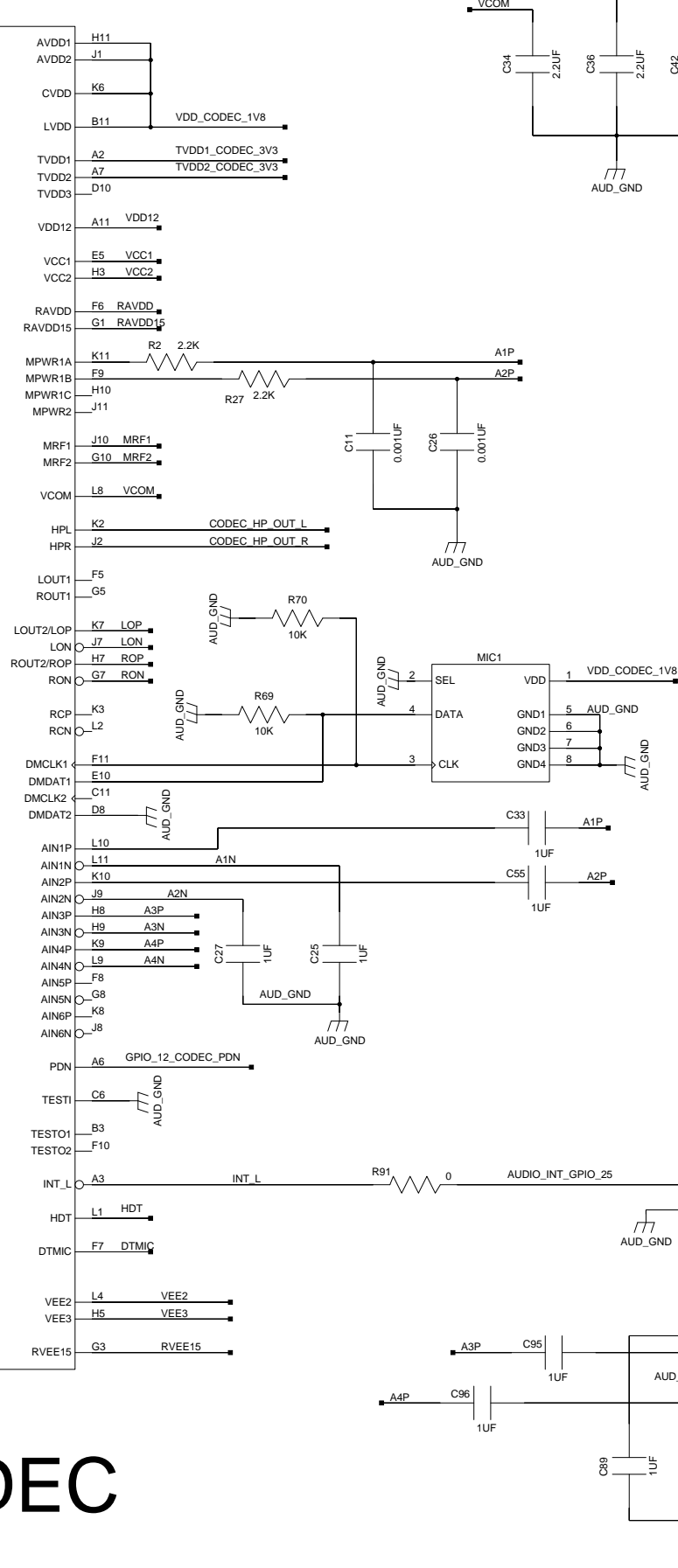
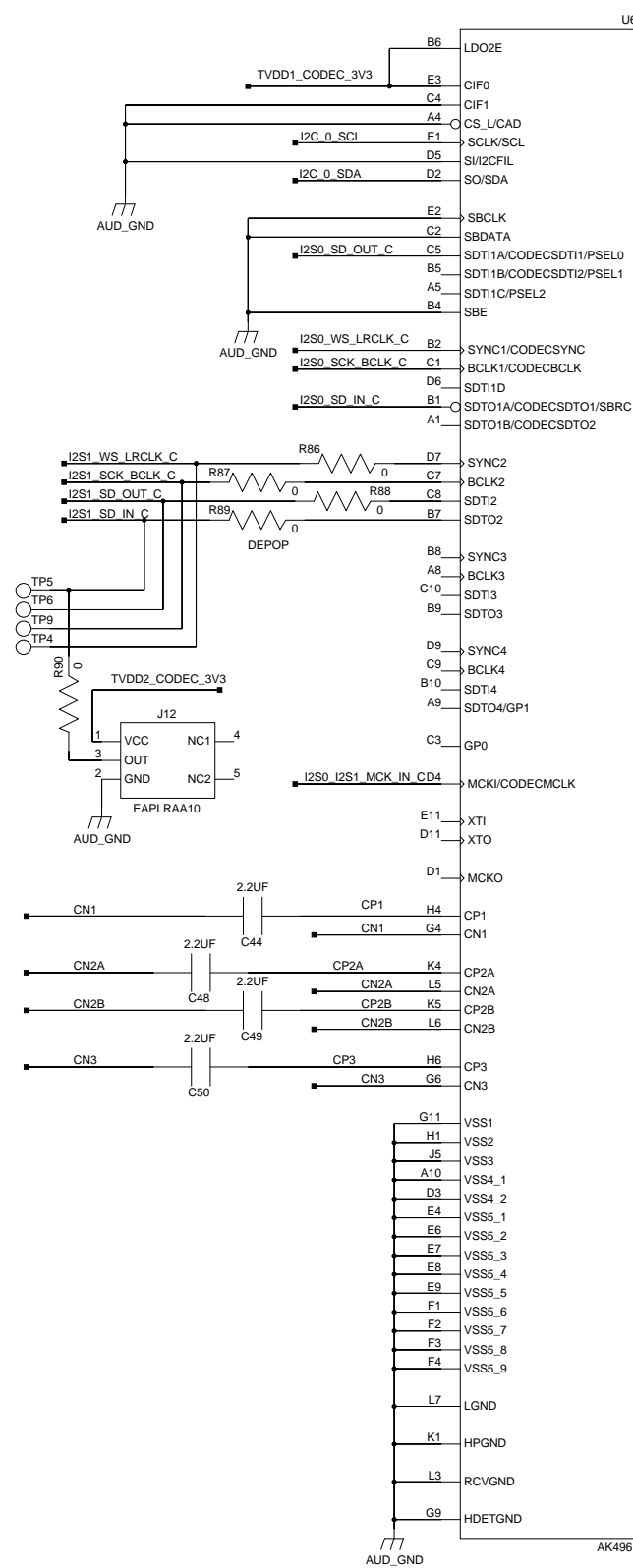


U5 2G/5G SPDT Antenna Diversity Switch Control Table		
MODE OF OPERATION Ant Diversity	ANT0_DIV_RF_SW_CTRL_4 SPDT (U5 VCONT1)	ANT1_DIV_RF_SW_CTRL_5 DPDT (U5 VCONT2)
RF_2G_5G to Ant0	1	0
RF_2G_5G to Ant1	0	1

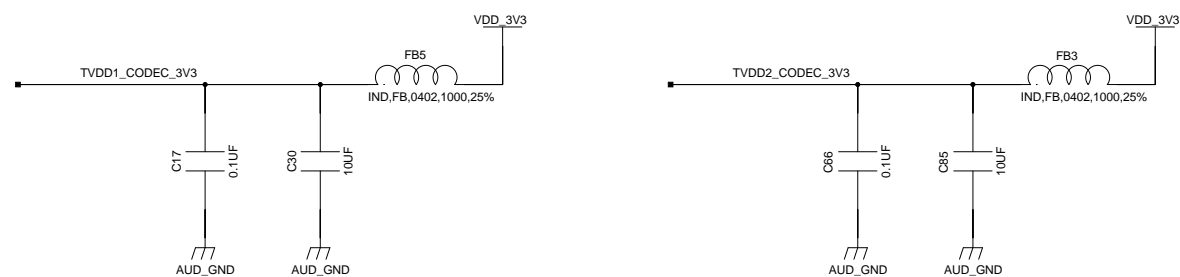
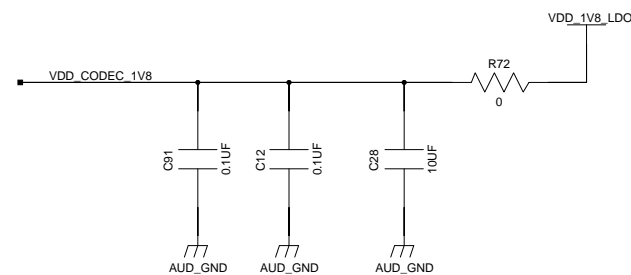
ALL OTHER STATES UNDEFINED



# ANTENNA DIVERSITY



Audio Section has a separate Audio GND to isolate from noise of other sections.  
It connects to common GND (GND) with a 0 Ohms Resistors



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DATE 04/12/2015:15:13	SHEET 7	OF 7	