Rev01 Initial Release Schematic - 11/03/2014

Rev02 Second Release Schematic - 11/14/2014

Updates :

Updates - 11/05/2014

- Updated FL1 to 0603 - Murata LFB182G45CL3D178

BT Section Updates - 11/06/2014

- Updated Y2 20MHz XTAL to 1.6x1.2mm - TXC - 8Q20070002

BT Section U3 Updates - 11/12/2014

- Added note that BT LPO_IN can be fed from GPIO_12, 13, 14 or 15 of BCM43909 or external 32KHz Clock
- Added R3 10K (depopped) on BT_XTAL_STRAP_1 (To provide option for 40MHz XTAL if needed)
- Depopped R4 since BT has dedicated XTAL
- BT_OTP_VDD3P3V (U3 Pin 104) & BT_USB_VDDO (U3 Pin41) – Tied together and now connect to VDD_3V3_BT
- Removed 0 Ohm resistor (R1) on BT_VCOVDD1P2 (U3 Pin48)
- Renamed R6 resistor to R1
- Removed the C4 cap (2.2uF) on supply feeding PAD_I_VBAT(U3 Pin1) & PAD_I_VIN_LDO2P5 (U3 Pin4) and added note to include this cap externally on carrier board
- Removed BT_GPIO3 & BT_GPIO_5 going to Module pins, they are NC
- C25 and C21 changed to 10pF Cap

43907 Section U1 Updates 11/12/2014

- Removed C22 (100pF) & C11 (1uF) and FB3 on USB Supply pins (U1 Pins 166, 173, 176) – Added note to have these components externally on carrier board
- Replaced C3 with 1uF 0201 cap and add additional 1uF (GRM033R60G105MEA2D) cap on VOUT_LNLDO supply (U1, Pin 106)
- Replaced C2 and C33 with 1uF 0201 cap (GRM033R60G105MEA2D) cap on AVDD1P2 supply (U1, Pin 204)

BT Section U3 Updates - 11/13/2014

- BT(U3) Pin1, Pin4 supply changed back to BT_3V3_VDD, removed the extra module pin for BT_VDD
- C5 cap on PAD_O_VDD2P5 (U3 Pin3) changed to 2.2uF, 0402 size (GRM155R60J225M), removed the additional 1uF cap (C4) on the line

43907 Section U1 Updates 11/13/2014

- Added another module pin VDD_3V3_IN, to feed the WLAN Radio (WRF_SYNTH_VDD3P3, WRF_PA_VDD3P3, WRF_TXMIX_VDD) , VDDIO_RF & OTP_VDD3P3, on the carrier board this pin can be connected to VOUT_3P3 through VDD_3V3_LDO module pin or disconnected using resistor
- Replaced C3 cap on VOUT_LNLDO(U1 Pin 106) with 2.2uF 0402 cap (GRM155R60J225M)
- RF_Inductors : Replaced L1 with 3.3nH 0201 (LQP03TN3N3B02D), and L2 with 0.6nH 0201 (LQP03TN0N6B02D) Inductor
- U2 5G T/R Switch replaced with Skyworks SKY13351-378LF part 1mmx1mm

43907 Section U1 Updates 11/14/2014

- C12 and C65 changed to 1uF 6.3V Rated Caps (GRM033R60J105MEA2D) on U1 (Pin223) and U1 (Pin240,241) WLAN Radio Supplies
- Removed C18 and C19 0.001uF caps on U1 VDDC Rail
- Added 10pF(C4) DC Block Cap on RF Signal to Ant1 Path
- C52 PMU Cap on SR_VDDBAT5V (U1, Pins 108, 113,122,125) changed to 6.3V Rated Part (GRM155R60J475ME87D) as per PMU Team recommendation
- C29 PMU Cap on VOUT_HSICLDO (U1, Pin107) changed to 6.3V Rated Part (GRM033R60J474ME90D) as per PMU Team recommendation
- C27 PMU Cap on VOUT_3P3,VOUT_3P3_SENSE (U1, Pins 118,119,117) changed to 6.3V Rated Part (GRM155R60J475ME87D) as per PMU Team recommendation
- Marked U1, PMU Caps, XTAL, XTAL Caps, RF Components Critical
- Changed net name of RF 2G signals going to FL1 to RF_2G_FL_A1
- Changed net name of RF 2G signals going to FL2 to RF_2G_FL_A0

BT Section U1 Updates 11/18/2014

- C50 cap BT 20703 Chip (U4) Pin 13 removed
- R7 replaced with 3.3 Ohms 01005 Resistor

Rev03 Third Release Schematic - 12/19/2014

Updates 11/21/2014

- FL2 changed to mirrored diplexer Murata - LFD182G45MJ5R653

43907 Section U1 Updates 12/02/2014

- C44 changed to 1uF 0201 cap (GRM033R60J105MEA2D)

RF Section Updates 12/08/2014

- Added C11 and C18 10pF caps and option for WL 2G to bypass Diplexer and go to Module Ant Pin

BT Section U3 Updates 12/09/2014

- Remove BT GPIO_2 signal going to Module Pin
- Bring Out 5 Additional BT Signals to Module Pins (4 for BT ADC and 1 for BT JTAG_SEL)

BT Section U3 Updates 12/12/2014

- Remove BT GPIO_4 signal going to Module Pin
- Remove BT SFLASH Signals going to Module Pins

43907 Section U1 Updates 12/15/2014

- C2 changed to 2.2uF 0402 cap (GRM155R60J225ME15D)
- C33 changed to 0.1uF 01005 Cap

43907 Section U1 Updates 12/17/2014

- Added additional 0.1uF cap before FB2 (Depopped by default)
- Changed FL2 to 0805 Diplexer

43907 Updates 12/17/2014

- Removed C11 and C18 caps and Dixplexer Bypass Option
- Removed R10
- Removed extra GND TP's

RF Section Updates 12/18/2014

- Removed R11, C68 & C67

BT U3 Updates 01/15/2015

- Updated BT Symbol to BCM20707 Part

BT U3 Updates 01/30/2015

- BT GPIO_2 signal brought out to Module Pin TP162

BT U3 Updates 02/02/2015

- BT XTAL (Y2) Changed to 40MHz 8Q40070003 Part
- R3 Popoulated and R2 Depopopped to enable BT 40MHz XTAL Mode

43907 U1 Updates 02/05/2015

- VDDIO_SD (U1 Pin255) separated from VDDIO and brought out to TP115
- Swapped the locations of C65 and C44 Caps on Module to match schematic
- Updated the netname of VDDIO_RF supply to VDDIO_RF_3V3

RF Front End Updates 03/03/2015

- FL2 Diplexer Updated to Cyntec TDP-2012-205-VAS
- FL1 BPF Updated to Murata LFB182G45CGXR030

RF Front End Updates 03/18/2015

- FL2 Diplexer Updated to TDK DPX205850DT-9048A2BR

RF Front End Updates - Set WLAN to Ant0, BT to Ant1 05/04/2015

- Depop C59, C46, C54, C21
- Populate C60, C45, C61, C25
- Depop U4 - 2.4G DPDT Switch
- Change FL2 to TDK DPX205850DT-9043B1BR (2.4G LPF /5G BPF) Part

BCM43907 XTAL Section Updates- 05/22/2015

- C23 and C24 changed to 33pF GRM0225C1C330JD05D Parts

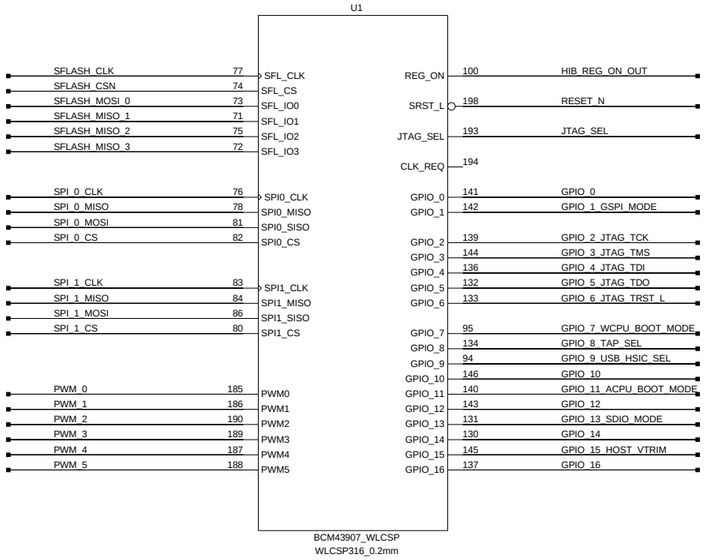
RF Front End Updates - 05/22/2015

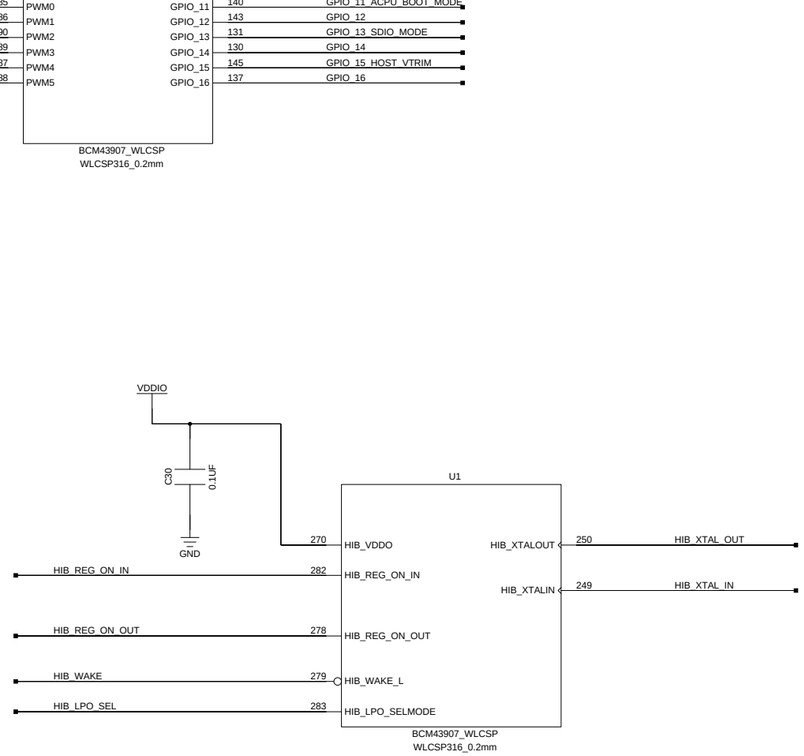
- Change FL2 to TDK DPX205850DT-9043B2BR (2.4G LPF /5G BPF) Part
- C15 matching cap changed to NoLoad (Depop)
- L1 changed to 3.6nH Murata (LQP03TN3N6B02D) Part

DOCUMENT
SCHEMATIC DIAGRAM 824-127858-0020

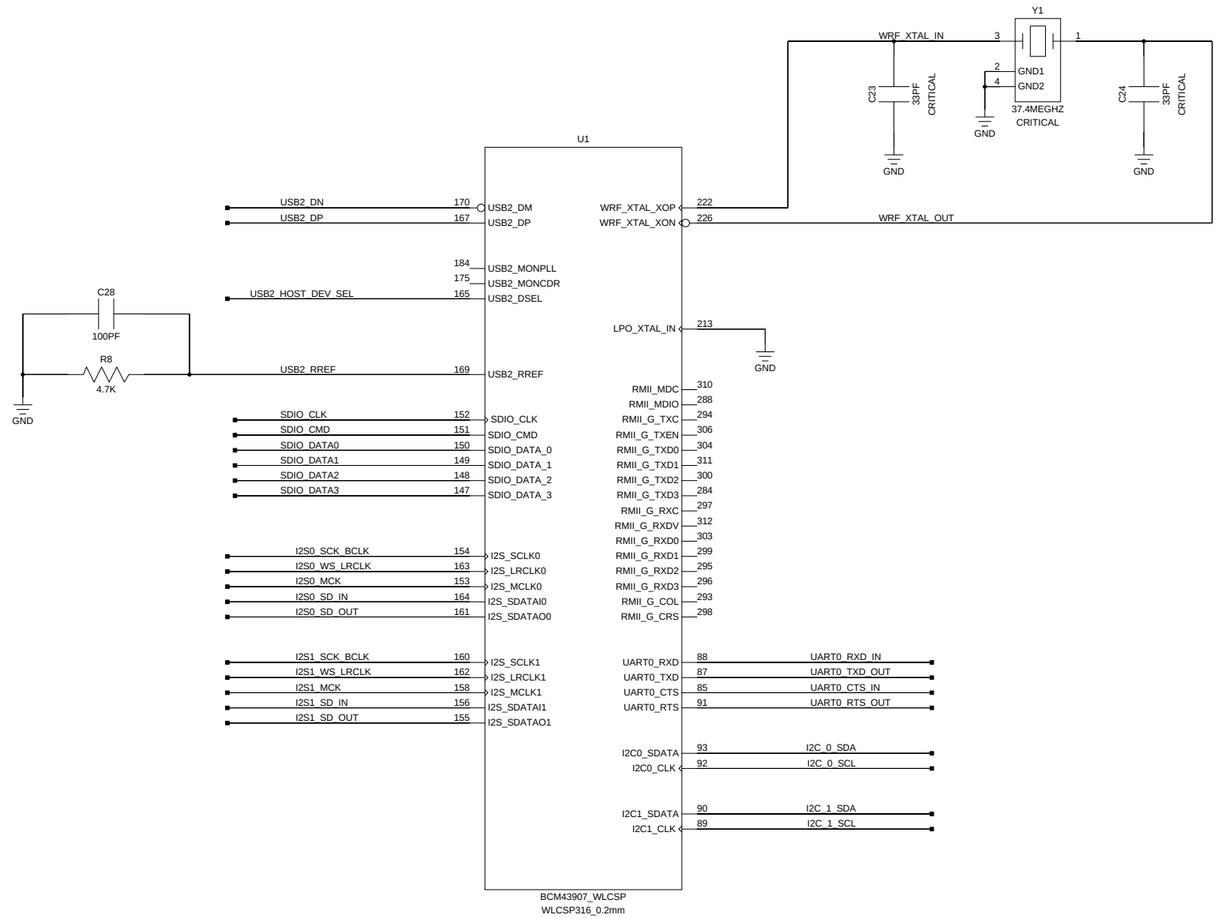
PRINTED CIRCUIT BOARD
200-127858-0010

Approvals		Broadcom Company Confidential		
Designer	Date			
Reviewer	Date	SIZE B	TITLE BCM943907WLCSP_1	
Reviewer	Date	Designer VIJAY DESAI	Drawing Number 824-127858-0010	Version 09
Reviewer	Date	DATE 22/05/2015:16:46	SHEET 1 OF 11	





HIBERNATION BLOCK



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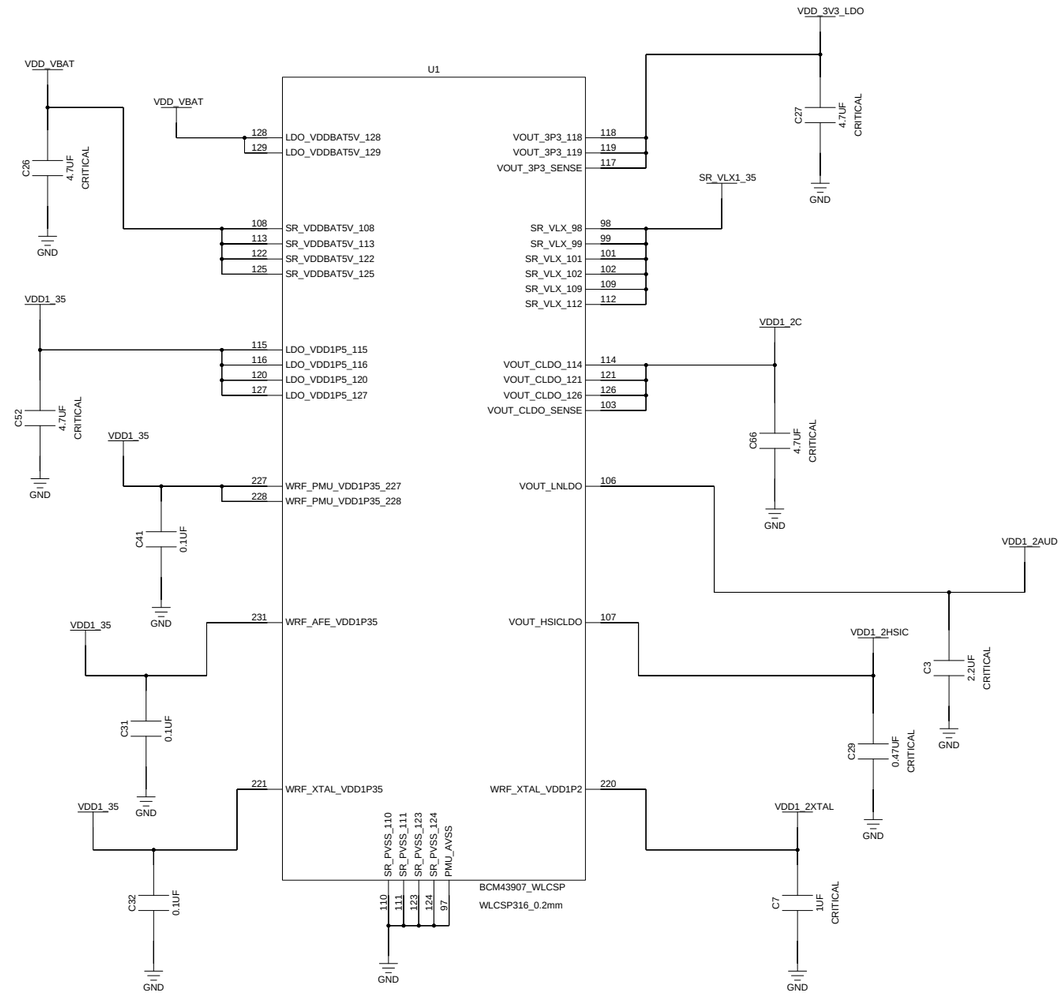
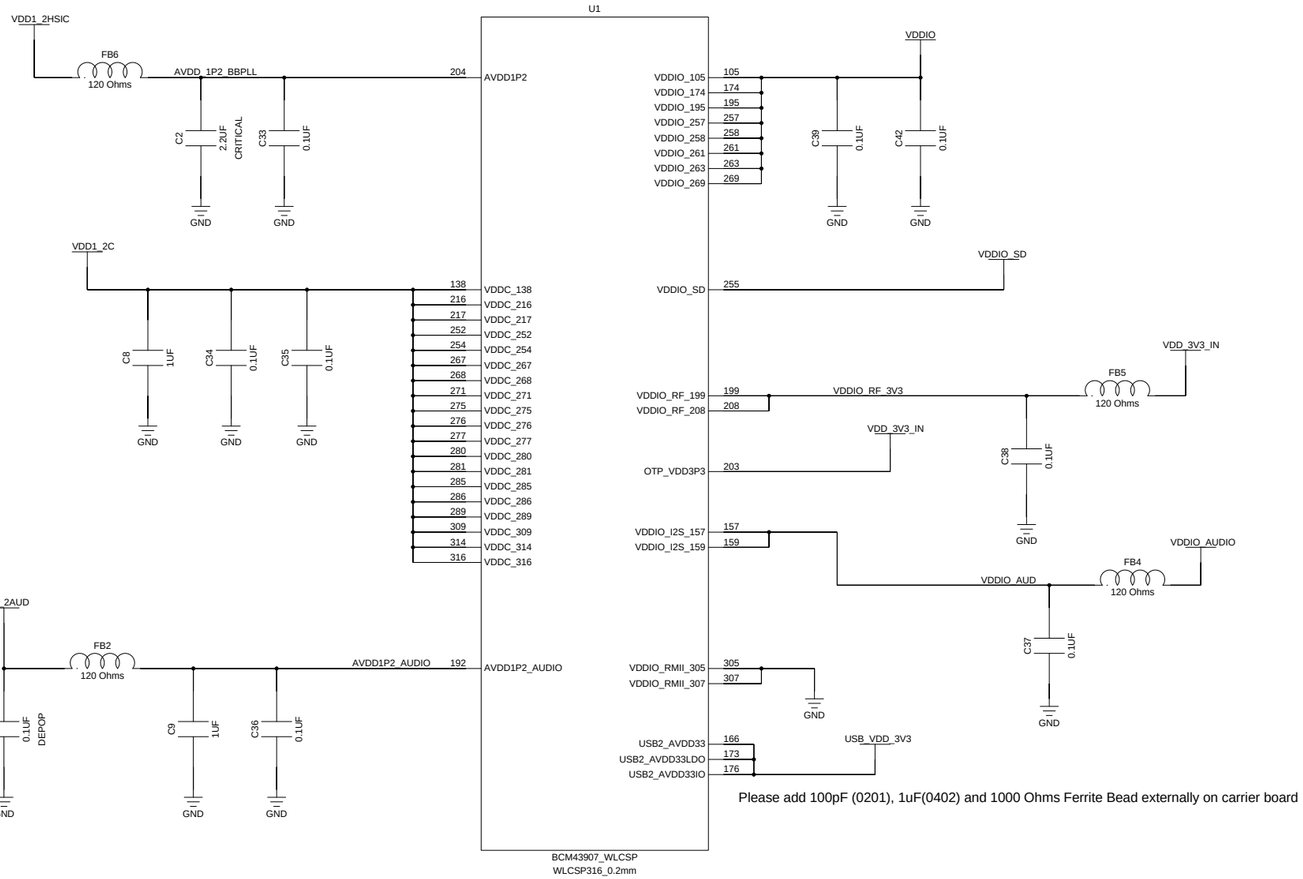
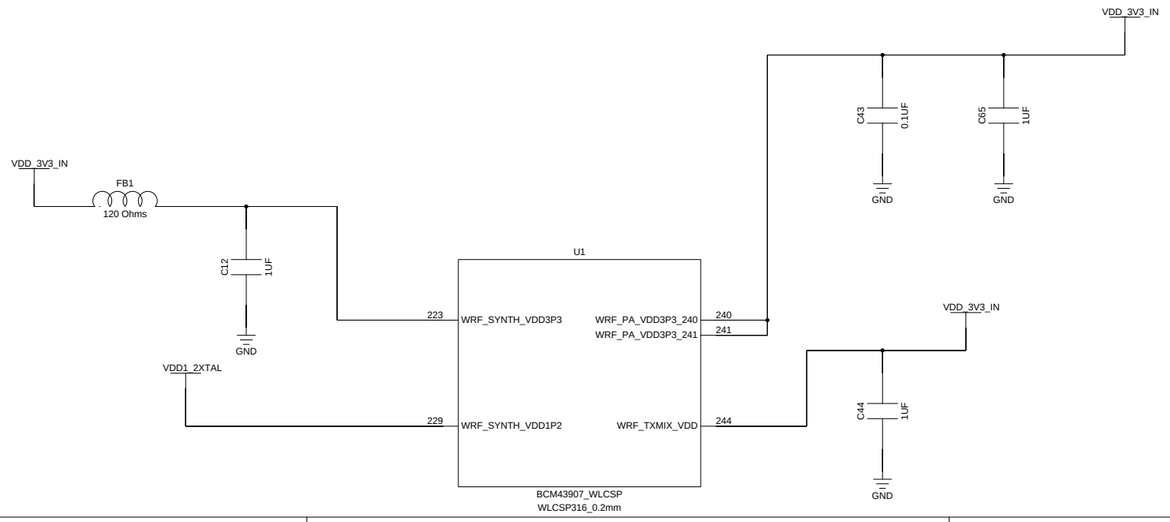
SIZE	TITLE	
B	BCM943907WLCSP_1	
DATE 22/05/2015:16:48		SHEET 2 OF 11





Please add 100pF (0201), 1uF(0402) and 1000 Ohms Ferrite Bead externally on carrier board



PMU

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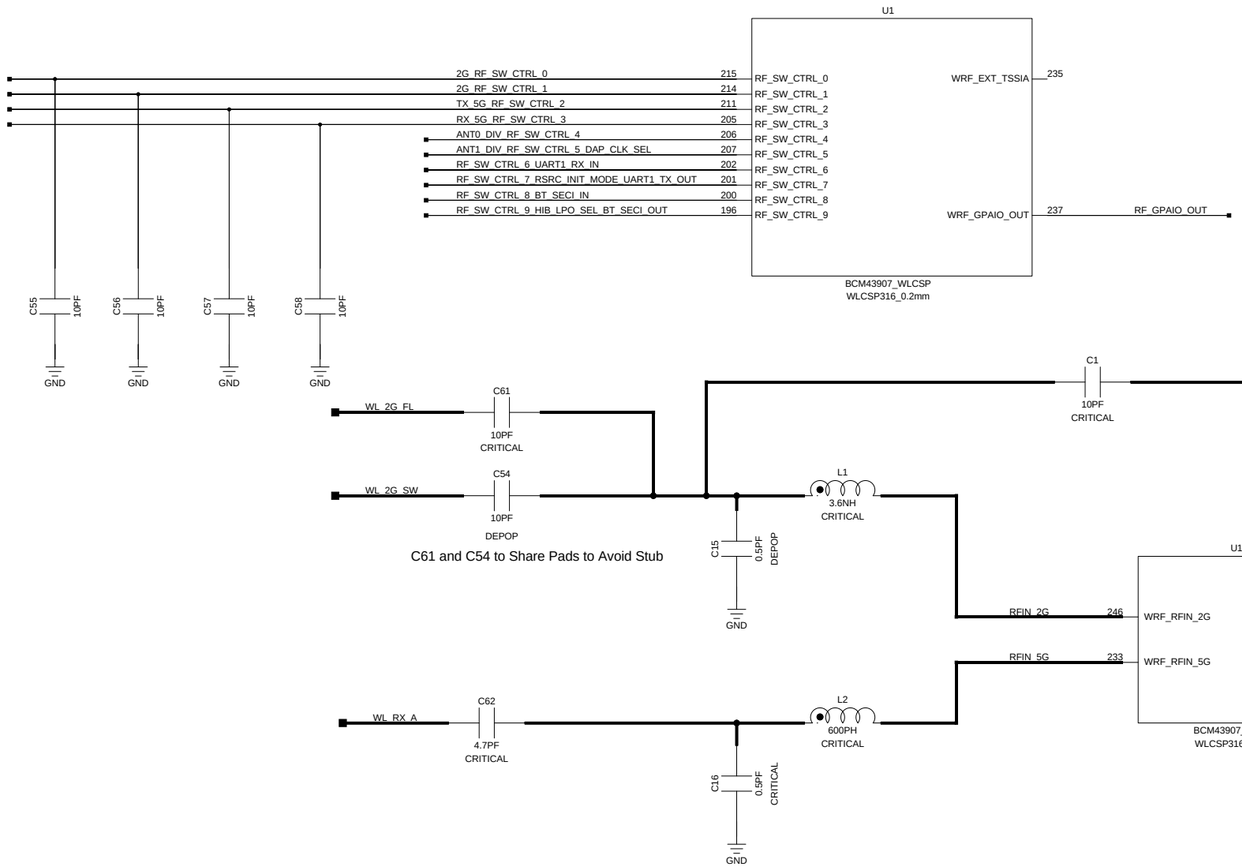
SIZE	TITLE		
B	BCM943907WLCSP_1		
DATE 05/02/2015:11:41		SHEET 3	OF 11



WLAN RF

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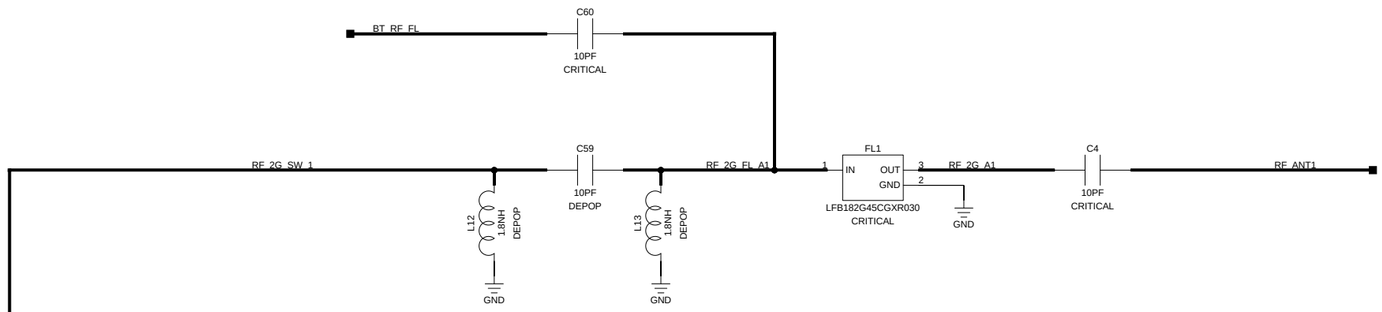
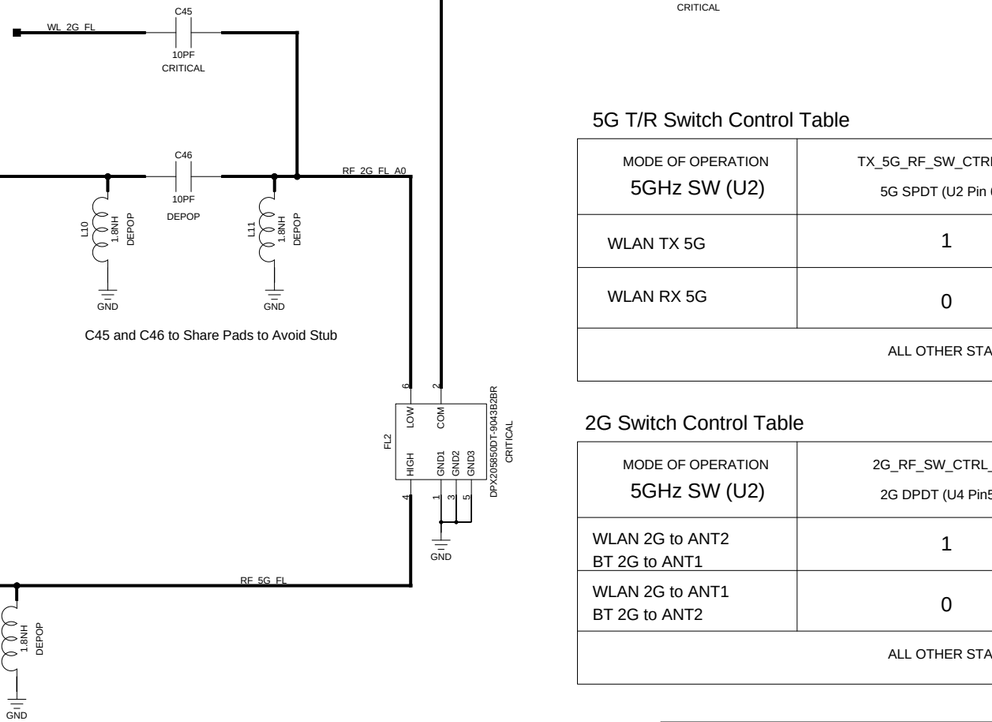
SIZE	TITLE	
B	BCM943907WLCSP_1	
DATE 22/05/2015:16:48		SHEET 4 OF 11



C60 and C59 to Share Pads to Avoid Stub



WLAN/BT Diversity Switch

5G T/R Switch

C45 and C46 to Share Pads to Avoid Stub

5G T/R Switch Control Table

MODE OF OPERATION 5GHz SW (U2)	TX_5G_RF_SW_CTRL_2 5G SPDT (U2 Pin 6)	RX_5G_RF_SW_CTRL_3 5G SPDT (U2 Pin 4)
WLAN TX 5G	1	0
WLAN RX 5G	0	1
ALL OTHER STATES UNDEFINED		

2G Switch Control Table

MODE OF OPERATION 5GHz SW (U2)	2G_RF_SW_CTRL_0 2G DPDT (U4 Pin5)	2G_RF_SW_CTRL_1 2G DPDT (U4 Pin 2)
WLAN 2G to ANT2 BT 2G to ANT1	1	0
WLAN 2G to ANT1 BT 2G to ANT2	0	1
ALL OTHER STATES UNDEFINED		

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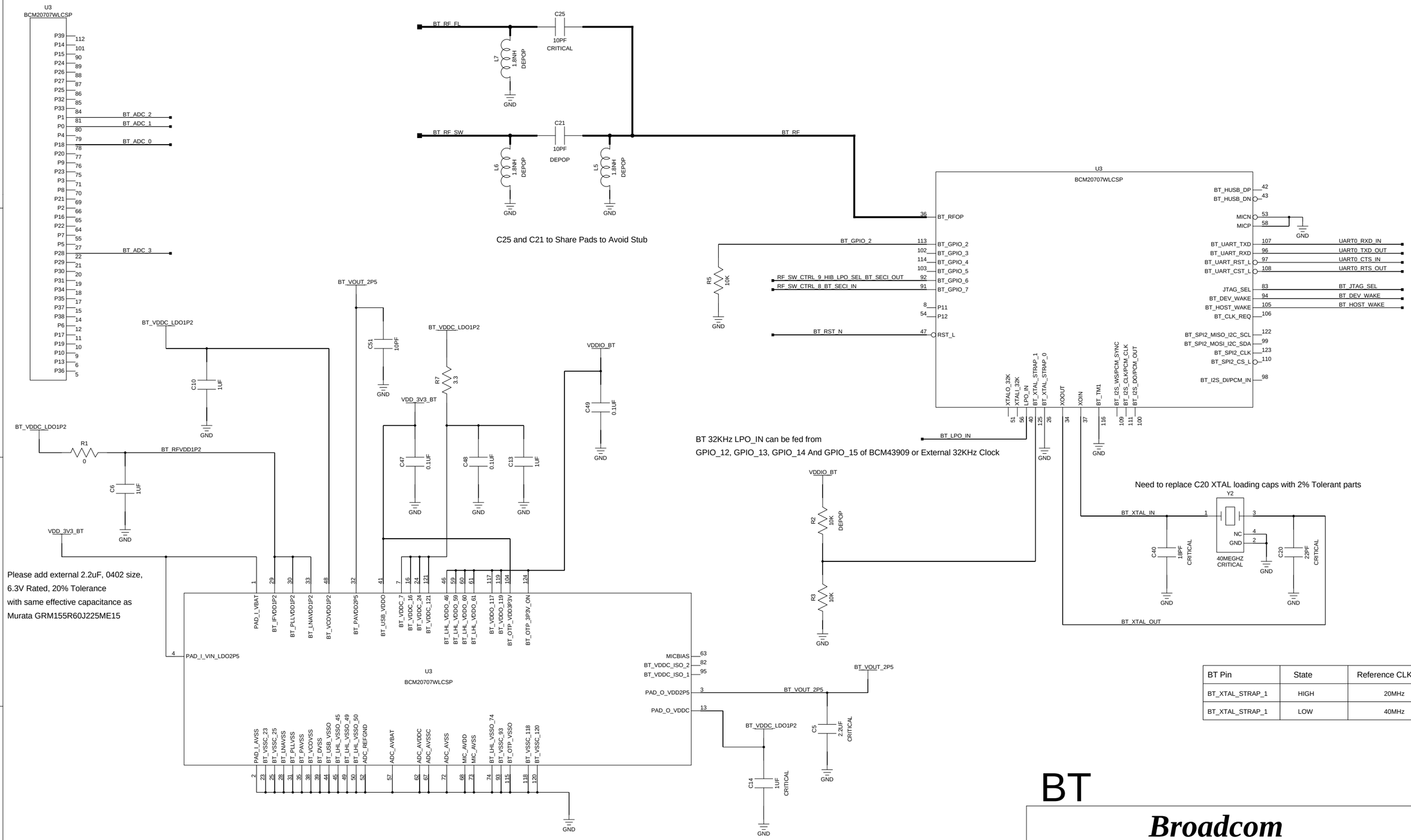
SIZE	TITLE	
B	BCM943907WLCSP_1	
DATE 22/05/2015:16:48		SHEET 5 OF 11



BT Pin	State	Reference CLK Frequency
BT_XTAL_STRAP_1	HIGH	20MHz
BT_XTAL_STRAP_1	LOW	40MHz

BT

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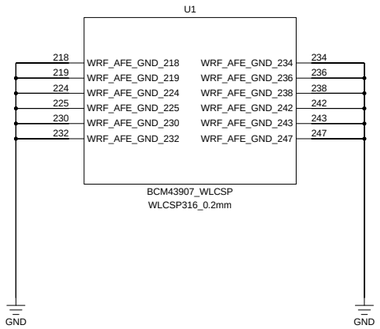
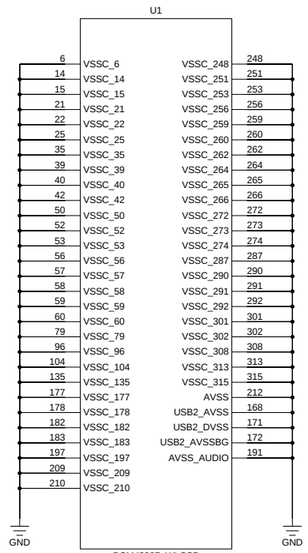
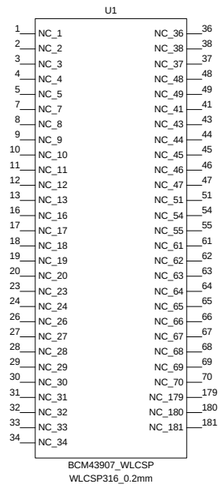
SIZE	TITLE	
B	BCM943907WLCSP_1	
DATE 04/05/2015:11:54		SHEET 6 OF 11





GND Pins



NC Pins

GND + NC's

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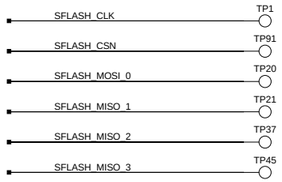
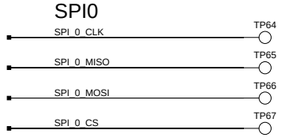
SIZE	TITLE	
B	BCM943907WLCSP_1	
DATE 15/12/2014:12:08		SHEET 7 OF 11

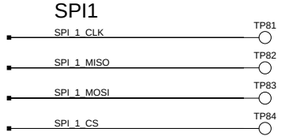
Quad-SPI SFLASH



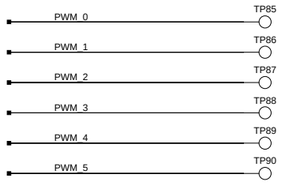
SPI0



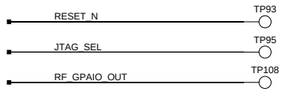
SPI1



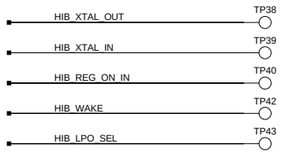
PWM



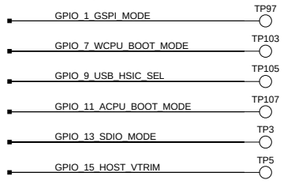
MISC



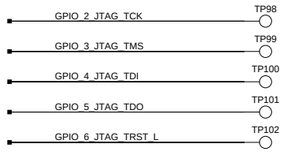
HIB Block



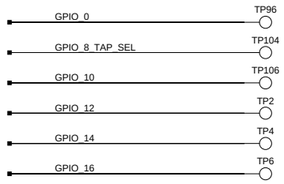
Straps on GPIO's



JTAG

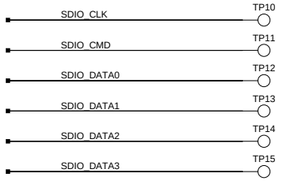


GPIO's

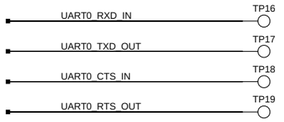


USB

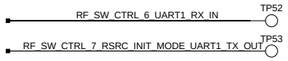
SDIO



FAST UART



SLOW UART

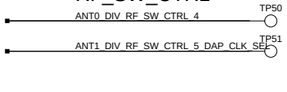


SECI (For BT CO-EX)

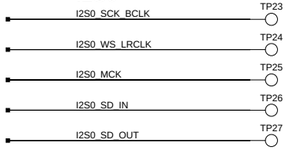
Strapping Options

Pin	Strap Function	Internal Strap Pull
		Chip Default
GPIO_1	gSPI Mode	0
GPIO_7	WCPU Boot Mode : 0 = TCROM Boot 1 = TCMSRAM Boot	0
GPIO_9	USB/HSIC Sel : 0 = HSIC PHY 1 = USB PHY	0
GPIO_11	ACPU Boot Mode : 0 = SOCROM Boot 1 = SOCSRAM Boot	0
GPIO_13	SDIO Mode : 0 = SDIO Device 1 = SDIO Host	0
GPIO_15	Host Vtrim Enable 0 = Host Vtrm Disable 1 = Host Vtrim Enable	0
RF_SW_CTRL_5	Host DAP Clock Sel	0
RF_SW_CTRL_7	Host RSRC Init	0
RF_SW_CTRL_9	LPO Sel : 0 = LPO from HIB 1 = Internal 32KHz LPO	0

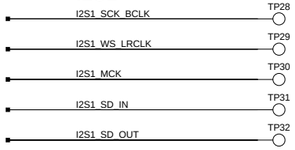
RF_SW_CTRL



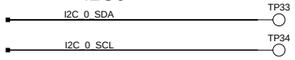
I2S0



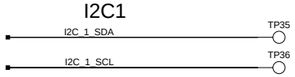
I2S1



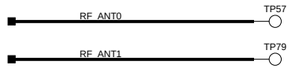
I2C0



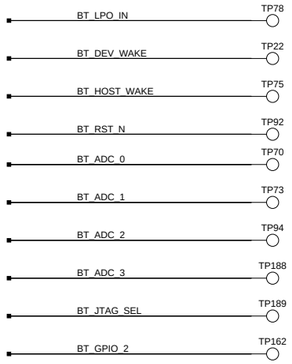
I2C1



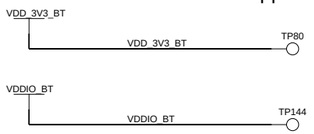
RF



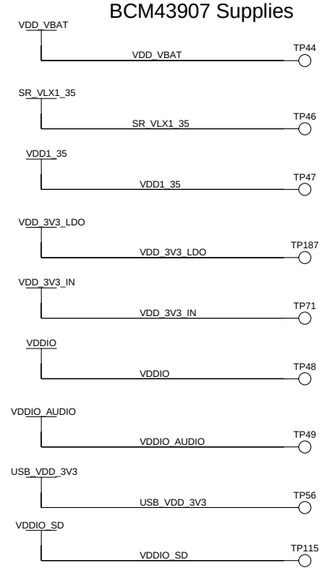
BT



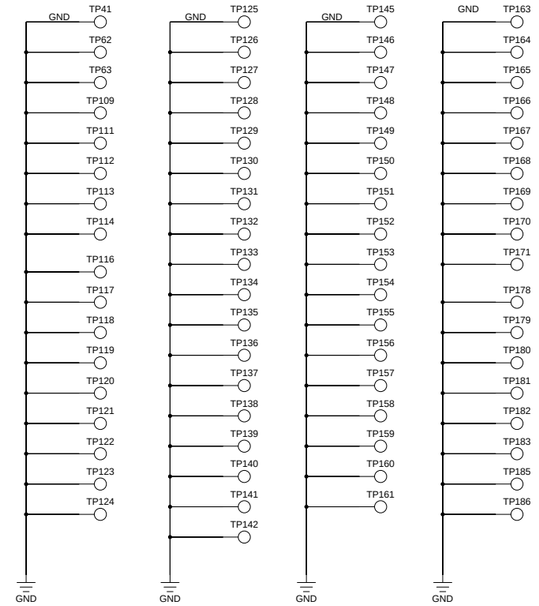
BT BCM20707 Supplies



BCM43907 Supplies



GND



Module Pins

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SIZE	TITLE	
B	BCM43907WLCSP_1	
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PMU Section Recommendation By Broadcom Corporation PMU Team

1. External 43909 CBUCK Inductor Any inductor any other than LQM2MPN2R2MG0, please review the new inductor with PMU team.
2. BCM43907 PMU Caps :

a. VBAT Cap : Nominal value 4.7uF. 0402 inch, 10V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 1.645uF at 4.8V.

ii.Effective capacitance should NOT drop below 1.88uF at 4.2V

iii.Effective capacitance should NOT drop below 2.2uF at 3.6V

iv.Recommended cap: Murata GRM155R61A475M or any cap matching or better than above DC bias profile

v.This 4.7uF can be shared with SR_VDDBAT5V & LDO_VDDBAT5V pins but the cap must be closer to SR_VDDBAT5V.

b. CBUCK Cap: Nominal value 4.7uF. 0402 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 3.622uF at 1.35V.

ii.Recommended cap: Murata GRM155R60J475ME87 or any cap matching or better than above DC bias profile

iii.I noted you used GRM155R61A475MEAA 10V cap; this is fine but it's an overkill & more expensive than 6.3V cap.

c. LDO3P3 Cap: Nominal value 4.7uF. 0402 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 1.773uF at 3.3V.

ii.Recommended cap: Murata GRM155R60J475ME87 or any cap matching or better than above DC bias profile

d. CLDO Cap : Nominal value 4.7uF. 0402 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 3.91uF at 1.2V.

ii.Recommended cap: Murata GRM155R60J475ME87 or any cap matching or better than above DC bias profile

d. LNLDO Cap :Nominal value 2.2uF. 0402 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 1.87uF at 1.2V.

ii.Recommended cap: Murata GRM155R60J225ME15 or any cap matching or better than above DC bias profile

iii.If you want to use 2 pcs of 0201 inch size 1uF, the total effective capacitance at 1.2V DC bias must meet 1.87uF typical.

e. HSICLDO Cap: Nominal value 0.47uF. 0201 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 0.376uF at 1.2V.

ii.Recommended cap: Murata GRM033R60J474ME90 or any cap matching or better than above DC bias profile

2. BCM20703 BT PMU Caps :

a. BT 2.5V LDO Out Cap: Nominal value 2.3uF. 0402 inch, 6.3V, 20%, X5R, ceramic surface-mount

i.Effective capacitance should NOT drop below 1.056uF at 2.5V.

ii.Recommended cap: Murata GRM155R60J225ME15D or any cap matching or better than above DC bias profile

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PMU Section Recommendation By Broadcom Corporation PMU Team cntd...

4. Module Layout : We consider module layout the same as FCFBGA package substrate routing.

PMU team needs to review the module pins relating to VBAT, SR_VLX, VSS which can impact CBUCK chip reliability.

Module Layout Routing Guidelines

Please ensure module designer extracts all these parasitic inductances & resistances for our review. The following needs to be achieved :

a. SR_VDDBAT5V pin to VBAT cap :

i.Top-layer routing, length < 42mils (1.066mm), width >10mils (0.254mm)

ii.Routing ESR<5mOhms, ESL<400pH at 4MHz - 200MHz

b. CBUCK output cap to LDO_VDD1p5 pin:

i. 2nd layer routing, length < 42mils(1.066mm), width>10mils(0.254mm)

ii. Routing ESR<10mOhms.

c. SR_VLX pin to inductor:

i. Routing length < 80mils(2.032mm), 10mils(0.254mm)<width<30mils(0.762mm)

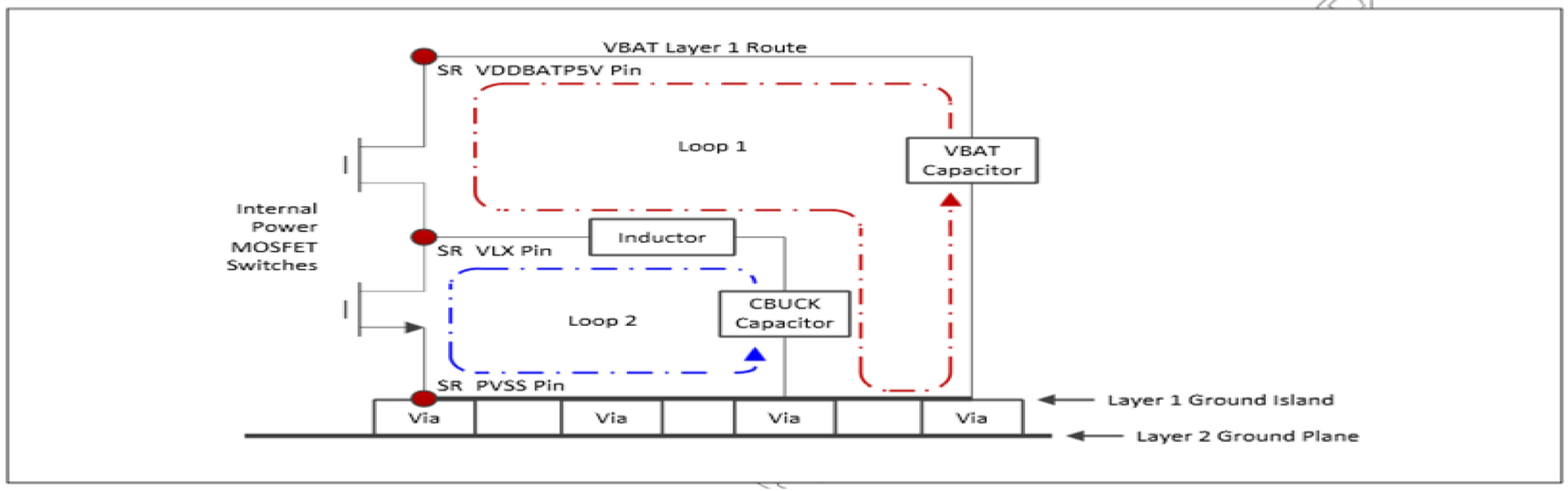
d. Top-Layer GND island connecting SR_PVSS pin, CBUCK cap gnd, VBAT cap gnd:

i. Routing ESR<5mOhms, ESL<300pH at 4MHz - 200MHz

PMU Notes from Broadcom Corporation PMU Team

Potential CBUCK Noise if Routing Not Optimized

Figure 17: EMI Loops in Buck Switching Regulator



Picture Above Shows Two Loops through MOSFETs of CBUCK

1)Each loop starts from a cap and ends at its ground terminal.

2)The area within each loop is proportional to the EMI. Routing of sensitive signals through the areas

3)bounded by these two loops should be strictly avoided.

4)Top-layer routings are used to conduct switching currents to avoid micro-via inductances.

5)VBAT, CBUCK cap sits on a top-layer gnd island connecting to SR_PVSS pin directly.

6)Micro-vias are still used to connect this top-layer gnd island to 2nd-layer GND Plane and this only carries DC currents.

7)The 2nd Layer GND Plane also acts as a shield over the 2 EMI loops to prevent noise radiation to other layers.

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