Design Rules Verification Report

Filename : C:\Users\kevin.cotton\OneDrive - Cégep Limoilou_Cours-TGE\243-436-Dev-Prod4-Certifications\Projet de fin de session\243-436-PCB-SuiveurDeLigne-7capteurs\243-4xx-Suiveur-IR-7.PcbDoc

Warnings 0
Rule Violations 0
Waived Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Un-Connected Pin Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.15mm) (Max=5mm) (Preferred=0.2mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.3mm) (Max=5mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.075mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	0

Waived Violations	
Un-Connected Pin Constraint ((All))	1
Total	1

Un-Connected Pin Constraint ((All))
Un-Connected Pin Constraint: Pad U8-13(38.765mm,17.145mm) on Bottom Layer Waived by Kevin Cotton at 2026-02-13 18:13:14no ERC check on