

Design Rules Verification Report

Filename : C:\Users\kevin.cotton\OneDrive - Cégep Limoilou\Cours-TGE\243-436 - Developp

Warnings 0

Rule Violations 0

Warnings	
Total	0
Rule Violations	
Clearance Constraint (Gap=0.15mm) (All),(All)	0
Clearance Constraint (Gap=0.25mm) (Inpoly),(All)	0
Clearance Constraint (Gap=0.125mm) (InDifferentialPair('CAN') or InDifferentialPair('USB_D')),All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.125mm) (Max=5mm) (Preferred=0.15mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.25mm) (Conductor Width=0.5mm) (Air Gap=0.25mm)	0
Hole Size Constraint (Min=0.2mm) (Max=5.5mm) (All)	0
Hole To Hole Clearance (Gap=0.3mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.099mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	0