Design Rules Verification Report

Filename : D:\Google Drive\kco_SailN2k\PCB_NMEA2kSimpleIndicatorDST\DST800_NMEA2

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.203mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.15mm) (Max=5mm) (Preferred=0.2mm) (All)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Prefered=0.254mm)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Prefered=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.5mm) (Conductor Width=0.3mm) (Air Gap=0.25mm)	0
Hole Size Constraint (Min=0.45mm) (Max=5mm) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Room DST800_NMEA2k-CAN_Indicator (Bounding Region = (25.4mm, 25.4mm, 70.485mm, 81.153mm)	0
Component Clearance Constraint (Horizontal Gap = 0mm, Vertical Gap = 0mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Silk primitive without silk layer	0
Silk primitive without silk layer	0
Total	0