CS 516000 FPGA Architecture & CAD

Final Project (Due: Jan. 10, 2023)

This design project is completely open in terms of how you solve the problem. (You may propose your own approach or follow previously proposed approaches in the literature.)
You may work individually or in a team of two persons, you will receive an additional bonus if you finish this project on your own.

Given a circuit netlist (V, E) where V represents the set of circuit nodes and E represents the set of nets (each net is a directed hyperedge), and a system graph (V',E') where V' represents the set of FPGAs and E' represents the set of connection channels connecting specific pairs of FPGAs. Each net has a unique source plus one or more sinks. We want to assign the circuit nodes to the given FPGAs to minimize the sum of external degrees of all FPGAs subject to the following constraints. (The external degree of a FPGA F_i is defined as the number of hyperedges incident with F_i but not fully inside F_i.)

1. Fixed node constraints: There are some circuit nodes which are already assigned to specific FPGAs and cannot be moved to other FPGAs.
2. Partition size constraints: The total number of circuit nodes assigned to each FPGA must not exceed the capacity of a FPGA (we assume all FPGAs have the same capacity).
3. Topology constraints: If node u is the source node of a net and node v is a sink node of the same net, then nodes u and v are either assigned to the same FPGA (i.e., FPGA(u) = FPGA(v)) or assigned to two neighboring FPGAs (i.e., (FPGA(u), FPGA(v)) $\in$ E').

Input Format

There are mainly four parts in the input file.
The first part is a single line listing the total number of FPGAs, total number of FPGA connection channels, capacity per FPGA, total number of nodes, total number of nets, and total number of fixed nodes.
Format:
< Total number of FPGAs> <Total number of FPGA connection channels> <Capacity per FPGA> <Total number of nodes><Total number of nets> <Total number of fixed nodes>
A sample of the first part is given below.

```
4 3 3 8 5 2
```

Note that the FPGA indices are from 0 to < Total number of FPGAs>-1. The node indices are from 0 to <Total number of nodes>-1.

Each line of the second part lists the two FPGAs connected by each FPGA connection channel. The number of lines in the second part is equal to the total number of FPGA connection channels.
Format:<FPGA id> <FPGA id>
A sample of the second part is given below.

```
0 3
1 3
2 3
```

The third part provides the information of the nets. The information of each net is given by a separate line where the first label is the id of its source node and the remaining labels are the ids of its sink nodes. The number of lines for the third part is equal to the total number of nets.
Format:<source node id> <sink node id><sink node id>…
A sample of the third part is given below.

```
0 1 2
1 2 6
2 3 5
3 4
6 7
```

The final part is the fixed node description. The information of each fixed node is given by a separate line where the first label is the id of the fixed node and the second label is the id of the FPGA it is assigned to.
Format:<fixed node id><FPGA id>
A sample input of the final part is given below.

```
2 3
4 0
```

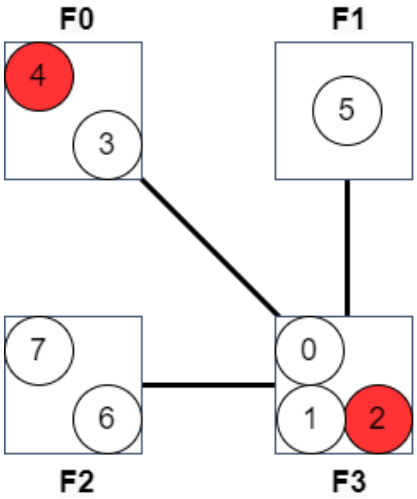
Output Format

Output the partitioning result in the order of the node id. For each line, the first label is the id of node and the second label is the id of FPGA which it is assigned to.
Format: <node id><FPGA id>

A sample output is given below.

```
0 3
1 3
2 3
3 0
4 0
5 1
6 2
7 2
```

The figure below shows a feasible partitioning solution for the sample input above. The red nodes are fixed to the FPGAs they belong to. In this case, there are two hyperedges ((1, 2, 6) and (2, 3, 5)) incident with F_3 but not fully inside F_3. So, the external degree of F_3 is 2. The sum of external degrees of all FPGAs is 5.



Project Submission

The source codes should be uploaded to eeclass. Please include a Makefile for compiling your codes. In addition, upload a report describing the details of your approach. If it is a team work, each member has to explain what he has done and the percentage of his contribution.

Name the executable file "topart" and make sure your program can be executed by running the command:

$./topart <**input file path**> <**output file path**>

like the one below

```
./topart ./input/testcase1.txt ./output/output1.txt
```

Makefile requirement

All codes should be compiled by running the command:

$make

You have to delete the executable file by running the command:

$make clean

Environment and Execution

(1) Language: C/C++

(2) Platform: Linux

Evaluation

- For each benchmark, if your result violates any fixed node constraint or partition size constraint, the quality score on that benchmark will be 0. For each violation of the topology constraints, we will add two to the sum of external degrees as a penalty.
- If your program takes more than 10 minutes to generate a result, it fails on that benchmark.
- Any plagiarism will result in a 0 grade for the project.

Grading

- 20%: The completeness of your program and report
- 80%: The solution quality (hidden testcases included)
  - The quality score is based on the sum of external degrees of your solution compared to other students when your solution is valid. Here is the equation for score calculation:

$$100 - 30 \times \min\{\ 1, \left(\frac{\text{Your sum of external degrees}}{\text{The smallest sum of external degrees}} - 1\right)\ \}$$

Reference

"TopoPart: a Multi-level Topology-Driven Partitioning Framework for Multi-FPGA Systems", in *Proc. of 2021 International Conference on Computer-Aided Design*.