Qsys - CE3910_03_14_2016.qsys (D:\altera\CE3910_system_vga\CE3910_03_14_2016.qsys)

File Edit System View Tools Help

Component Library

Project
- New Component...
- i2c_master
- myNewPWMv2
- MyIPs
- myIPs
- System

Library
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New... Edit... Add...

System Contents | Address Map | Clock Settings | Project Settings | Instance Parameters | System Inspector | HDL Example | Generation

	cpu.data_master	cpu.instruction_master	video_pixel_buffer_dma_0.avalon_pixel_dma_master
cpu.jtag_debug_module	0x0080_2800 - 0x0080_2fff	0x0080_2800 - 0x0080_2fff	
sysid_qsys_0.control_slave	0x0080_3008 - 0x0080_300f		
sdram.s1	0x0000_0000 - 0x007f_ffff	0x0000_0000 - 0x007f_ffff	
onchip_memory2_0.s1	0x0080_0000 - 0x0080_1fff	0x0080_0000 - 0x0080_1fff	0x0080_0000 - 0x0080_1fff
jtag_uart_0.avalon_jtag_slave	0x0080_3000 - 0x0080_3007		
video_pixel_buffer_dma_0.avalon_cont...	0x0080_3010 - 0x0080_301f		
pixel_port.s1	0x0080_2010 - 0x0080_201f		
Cam_control.s1	0x0080_2000 - 0x0080_200f		
oc_i2c_master_top_0.avalon_slave_0	0x0080_2020 - 0x0080_2027		
myNewPWMv2_0.avalon_slave_0	0x0080_2028 - 0x0080_202f		
Altera_UP_SD_Card_Avalon_Interface...	0x0080_2400 - 0x0080_27ff		
timer_0.s1	0x0080_2040 - 0x0080_205f		
timer_1.s1	0x0080_2060 - 0x0080_207f		
LEDS.s1	0x0080_2030 - 0x0080_203f		
pushbuttons.s1	0x0080_20d0 - 0x0080_20df		
LCDData.s1	0x0080_20a0 - 0x0080_20bf		
LCDControl.s1	0x0080_2080 - 0x0080_209f		
MyUART_0.mms1	0x0080_20c0 - 0x0080_20c3		

Messages

Description	Path
9 Info Messages	
System ID is not assigned automatically. Edit the System ID parameter to provide a unique ID	System.sysid_qsys_0
Time stamp will be automatically updated when this component is generated.	System.sysid_qsys_0
RGB Resampling: 8 (bits) x 4 (planes) -> 10 (bits) x 3 (planes)	System.video_rgb_resampler_0

0 Errors, 0 Warnings

4:04 PM
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