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High Performance 128-Channel Acquisition System for Electrophysiological Signals

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ABSTRACT The increased popularity of investigations and exploits in the fields of neurological rehabilitation, human emotion recognition, and other relevant brain-computer interfaces demand the need for flexible electrophysiology data acquisition systems. Such systems often require to be multi-modal and multi-channel capable of acquiring and processing several different types of physiological signals simultaneously in real-time. Developments of modular and scalable electrophysiological data acquisition systems for experimental research enhance understanding and progress in the field. To contribute to such an endeavor, we present an open-source hardware project called High-Channel Count Electrophysiology or HiCCE, targeting to produce an easily-adaptable, cost-effective, and affordable electrophysiological acquisition system as an alternative solution for mostly available commercial tools and the current state of the art in the field. In this paper, we describe the design and validation of the entire chain of the HiCCE-128 electrophysiological data acquisition system. The system comprises of 128 independent channels capable of acquiring signal at 31.25 kHz, with 16 effective bits per channel with a measured noise level of about 3 μV. The reliability and feasibility of the implemented system have been confirmed through a series of tests and real-world applications. The modular design methodology based on the FPGA Mezzanine Card (FMC) standard allows the connection of the HiCCE-128 board to programmable system-on-chip carrier devices through the high-speed FMC link. The implemented architecture enables end users to add various high-response electrophysiological signal processing techniques in the field programmable gate arrays (FPGA) part of the system on chip (SoC) device on each channel in parallel according to application specification.

INDEX TERMS Data acquisition, electrophysiology, field programmable gate arrays (FPGA), multi-channel, open source hardware, system on chip (SoC).

I. INTRODUCTION

Since the last decade, research and analysis on the physiological signals from the human body have gained huge attention. The research covers different aspects of biosignals and has successfully applied to different kind of application that can control different kinds of devices and machines, improve communication between human and machines and has helped in rehabilitation. The group of biosignals measurements and processing from the human body comprises signals known as electroencephalography (EEG), electrocardiography (ECG), electromyography (EMG), electrogastrography (EGG), electrooculography (EOG) and skin conductance response (SCR) [1]–[5]. EEG is a physiological signal that reads scalp electrical activity generated by the brain. Typically, metal electrodes will be used to collect the electrical activity of the brain from the scalp surface. The variation of the surface potential from the scalp reflects the functional activities of the brain.

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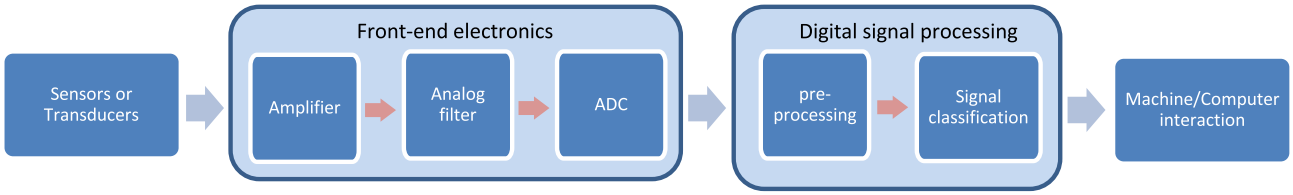

FIGURE 1. Typical physiological data acquisition system structure.

The EEG reading is a non-invasive reading that can be applied to human subjects for various types of applications.

The increasing need for devices in the field of neurorehabilitation, human emotion recognition, and other relevant brain computer interfaces (BCI) has sparked new interest in electroencephalography data acquisition system development. Brain computer interface is a system that acquires signals from the neural activity of the brain with the goal to establish a communication channel between the brain and computer. Such a system has many great potentials for example in bioengineering applications, human emotion monitoring, neuroscience and human-machine interaction.

Fig. 1 shows the typical structure of an electrophysiological data acquisition system. The physiological signal acquisition consists of sensors or transducers and front-end components to collect, amplify, filter, and convert analog signals to digital data. The collected data will be pre-processed to remove noise or unnecessary information. The cleaned signals will be classified according to the given criteria based on the intended application. Once the signals have been classified and processed, they will be used by different devices for a specific application.

Neurological disease or injury (stroke, spinal cord injury), monitoring cognitive engagement, identifying emotion related behaviours and other EEG based applications have increased research interest in brain computer interface. Using EEG data in such neurorehabilitation can help and support daily activities and improve the patients' quality of life considerably. In such a situation, the capability of the rehabilitation system is a relevant factor and has attracted serious consideration [6].

With the advance of computing processing technology, the trend of device development has moved towards multi-modal and multi-channel acquisition system capable of acquiring and processing several physiological signals simultaneously. In some applications, the adaptation of a real-time system that analyses different kinds of physiological signals is very important and crucial. For example, data collected from the human body, for instance, EEG and EMG simultaneously in real-time have a wide range of practical purposes in stroke rehabilitation and therapy. Often, these electrophysiological systems require to generate the output or decision within a certain limit of time thus, the systems must have real-time capabilities. For example, in human falling prediction and prevention applications [7], the system needs to process data coming from different types of electrophysiological channels and make the corrective action within 300 ms in order to avoid falls.

To date, several professional and high-quality EEG acquisition devices are available from multiple vendors. However, these thousand dollars devices are targeted at medical institutions and not meant for the general public and entry-level use, which hinders wide adaptation in BCI or other physiological application research [8]. Table 1 shows a comparison among several commercial EEG data acquisition system.

Though the systems shown in Table 1 are commonly used for medical applications, due to the proprietary close system architecture, they are not reconfigurable to customize the system according to the user application requirements. Moreover, these systems are only scalable up to the number of channels offered by the manufacturer hence may limit the spatial accuracy. High channel count can improve classification accuracy through spatial based artefacts attenuation. On top of that, some of the above systems require a stationary personal computer (PC) for data processing, thus limiting mobility and adaptability for online processing or wireless data transfer due to the closed firmwares. A highly versatile device can be achieved through a complete system that locally collects and processes electrophysiological data in the device of the embedded system.

We present an open source hardware project called High-Channel Count Electrophysiology or HiCCE, aiming to design and validate instrumentation in this space at a cost effective and affordable as currently feasible given the current state of the art. We hope that the capability to acquire and locally process multiple channels of different types of electrophysiological signals simultaneously along with its high response will allow and stimulate high-quality electrophysiological experimental research. The project is being developed in the framework of an open-collaborative project, released under the European Council for Nuclear Research (CERN) Open Hardware license. The source files including schematics, PCB design files, SoC firmware, and software files are located at the project repository https://ohwr.org/project/hicce-fmc-128/wikis/home. In this paper, we describe the general HiCCE architecture with its second designed 128-channel data acquisition board, the HiCCE-128v2.0, capable of acquiring at 31.25 kHz, 16 effective bits per channel with a measured noise level of about 3 μV. The design exploits modern electronic devices and techniques including Reconfigurable Virtual Instrumentation (RVI) based on programmable logic devices [17]–[20].

TABLE 1. Commercial data acquisition systems.

System	Max. Sampling Rate (SPS)	No. of Channels	Digital Output Resolution	Input Range (mV)	Noise Level (RMS)	Processor	Connectivity	CMRR	Price (€)
g.tec Nautilus [9]	500	64	24-bits	±187.5	<0.6 μV @ 1-30 Hz	TI DSP	Wireless 2.4 GHz/ USB 2.0	>90 dB	>4.5 k
g.tec HIamp [10]	38.4 k	256	24-bits	±340	<0.5 μV @ 1-30 Hz	TI DSP	USB 2.0	>90 dB	>31 k
TMSi Mobita [11]	2000	32	24-bits	±200	<0.4 μV @ 0.1-10 Hz	N/A	Wi-Fi IEEE 802.11 b/g	>100 dB	N/A
TMSi Refa [12]	2048	136	24-bits	±150	<1 μV @ 128 Hz	N/A	USB 2.0	>90 dB	N/A
Emotiv [13] EPOC Flex	128	32	14-bits	±4.12	N/A	N/A	Wireless proprietary 2.4 GHz	N/A	>2 k
BioSemi [14] ActiveTwo AD-box	16 k	256	24-bits	±262	<2 μV @ 16 kHz	N/A	USB 2.0	>90 dB	>40 k
ANT Neuro [15] eego mylab	16 k	256	24-bits	±50	<1 μV @ Lowest Freq.	N/A	USB 2.0	>100 dB	>25 k
Brain Products [16] actiCHamp	25 k	168	24-bits	±400	<2 μV @ 0-35 Hz	N/A	USB 2.0	>100dB	>25 k

The next sections of this paper are structured as follows. Section II provides an overview of state-of-the-art designs and related works in the field. The system architecture and related materials including the HiCCE-128v2.0 board, the SoC design strategy, and other associated modular designs are described in detail in Section III. Section IV describes the system evaluation and validation methods through several real-world experiments and tests with the obtained results. We compare our system with other existing hardware designs and discuss possible improvements for the system in Section V. Finally, in Section VI the conclusions are presented.

II. RELATED WORKS

Several research works have been devoted in the development of EEG data acquisition system. Majority of the development focus on the low-cost data acquisition system based on micro-electronic devices. Pinho *et al.* [21] developed a wireless and wearable EEG acquisition system for ambulatory monitoring. The proposed embedded system consists of 32 active dry electrodes and a front-end system of 24-bit, 1 kSPS (kilo samples per second) sampling frequency analog to digital converter per channel. The system includes a real-time EEG signal processing on 1 GHz ARM CPU. Wi-Fi connectivity is available to send the data to the PC for offline analysis and processing. The system has no scalability option and hence is limited to 32 channels only. The use of processor in the acquisition board presented in Pinho *et al.* [21] for signal processing means that the system has no capability to process multi-modal signals in parallel.

Feng *et al.* [22] proposed a system called EEGu2 as a portable embedded system for brain computer interface, which is based on BeagleBone Black (BBB). The system consists of a custom design cape, an acquisition board for 16 channels, 24-bit, 1 kSPS sampling frequency data acquisition system. While the individual acquisition board only consumes 101.2 mW power, the processor (BBB) power consumption is larger than the acquisition board, which is 1850 mW. Similar to Pinho *et al.* [21], this approach has no possibility to process multi-modal signals. Increasing the number of acquisition boards and processors for multi-modal signal processing will significantly increase the cost and power consumption.

Vo *et al.* [23] proposed a low cost 8-channel EEG acquisition system. The system relies on an ARM STM32F4 processor to process the live stream of EEG data. The communication to the PC is done through a Bluetooth module. Although some of the processing can be done by the embedded ARM processor, the BCI implementation requires a PC for numerical processing. The low number of channels means that the system is limited in terms of spatial resolution and may affect the signal classification accuracy.

Wild *et al.* [24] proposed a low-cost EEG acquisition system that sent the data to the PC for processing through Bluetooth communication. The system is a 4 channel in-ear EEG recording device that will collect and amplify the signals before sending to the PC for processing. Nathan *et al.* [25] developed a 16 channel with Bluetooth enabled for EEG data acquisition and processing. The collected data will be sent to the PC for analysis and processing. Both systems require

PC for signal processing hence limiting the mobility aspect of the system. The small number of channels limit the spatial resolution for better accuracy.

Most of the systems reviewed earlier in the Section II lack the ability to process multiple data online from multiple sensor channels simultaneously since all these systems were based on sequential execution devices such as single-core microprocessors or microcontrollers. A system with the ability of acquiring signals from multi physiological sensors and multi-channels requires a system having high-end capabilities. Such a system should be able to be interfaced with a large number of sensors/channels and must be able to perform complex processing on the data. Field Programmable Gate Array (FPGA) can help in to reduce the complexity and cost of the design process for a high channel count data acquisition system. Most conventional processors have limited computing resources such as arithmetic-logic unit (ALU), CPU, etc. These processors perform their operations sequentially because they can only operate one set of data in one time. On the other hand, FPGA can have multiple ALU blocks and several other components that can be interconnected to perform their intended operations simultaneously in parallel manner. Several physiological sensors can be connected to the analog front-end and then to the FPGA for parallel processing.

The advance development of system on chip (SoC) that combines microprocessor and FPGA on a single device has attracted a number of data acquisition system development that capitalized the benefit of both worlds for real-time online processing. References [7], [26]–[29] proposed an FPGA based system for a complete real-time system that can eliminate the use of bulky personal computer for signal processing. However, these systems often rely on a small number of electrodes that are only sufficient for simple applications. For real-time complex applications that highly depends on the capability to remove artefacts, the ability of the system to process high-dimensional data is very important. In this regard, the use of high number of channels is beneficial for high accuracy classification and prediction through spatial-based artefacts attenuation [30].

III. SYSTEM ARCHITECTURE

A. HiCCE ARCHITECTURE

When analog front-end circuits for electrophysiology are designed, three factors are mainly considered,

- Target application
- Number of channels required
- Sensitivity

Obviously, the latter two are correlated with the target application. Most common electrophysiology applications use ECG, EEG, or EMG systems. Each of these applications has different characteristics in frequency bandwidth, electrical dynamic range, etc. Table 2 summarizes some of these features. In terms of number of channels, Electrocorticography (ECoG) experiments often acquire data from high-density electrode arrays with high spatial resolution.

TABLE 2. Common electrophysiology signals and properties [40]–[43].

Biopotential	Frequency range (Hz)	Amplitude range (mV)	No. of channels
Electrocardiogram (ECG)	0.05 – 150 (diagnostic) 0.5 – 40 (monitoring)	0.1 – 5	12 (in hospital) 3 (in field)
Electroencephalogram (EEG)	0.1 – 100	0.025 – 0.1	21 (10 – 20 system) 345 (10 – 5 system)
Electrocorticography (ECoG)	0.1 – 500	0.1 – 0.5	>500
Electromyography (EMG)	25 – 5000	0.1 – 100	<15

ECoG signals are much stronger than EEG signals since electrodes are placed directly on the surface of the cerebral cortex. For EEG signal acquisition, the 10-20 system is widely used in clinical tests while the 10-5 system or 5 % system was proposed by Oostenveld and Praamstra [31] for high spatial resolution research studies. For some applications such as rehabilitation, it is required to deviate from traditional systems and acquire ECG, EEG and EMG simultaneously and synchronously [32]–[34]. Considering this information, all the application-specific electronics of the high channel count electrophysiology (HiCCE) board was developed. The acquisition chain of the HiCCE consists of four 32 channel analog multiplexers produced by Intan Technologies [35] and four analog to digital converters (ADCs) [36] as shown in Fig. 2, in total 128 channels can be used to acquire biosignals with a rate of 31.25 kSPS. There have been several comparison studies done [37]–[39] and the Intan analog multiplexer shows an advantage over others in terms of the number of channels, power per channel, and sampling rates. On the other hand, HiCCE is a cost-effective system that can be used in variety of electrophysiological experiments.

This paper presents the second revised version of the HiCCE board, the HiCCE-128v2.0. This HiCCE is a simplified version of the first prototype [20] in which digital potentiometers were removed and fixed the bandwidth to 1.0 Hz – 20 kHz.

This hardware module designed such a way that it is reliable for a long period of time with low noise operations. Outputs of the ADCs are driven by serial peripheral interface (SPI) physically connected to low-voltage differential signaling (LVDS) pairs in a Low-Pin-Count FPGA mezzanine card (FMC) connector, and physical size and shape of the printed circuit board (PCB) layout was adopted according to the FMC standard open ANSI/VITA 57.1-2008 [44], which leverages to use with any commercial standard FMC Carrier. Another reason for choosing FMC open standard is to have a reliable electrical connection between the HiCCE-128v2.0 board and the Carrier. The main focus in designing the PCB was avoiding interference of various noise sources such as the coupling of digital signal noise into analog signals and ambient noise to the signal paths. By reducing inductance and capacitance, and maintaining constant impedance on signal

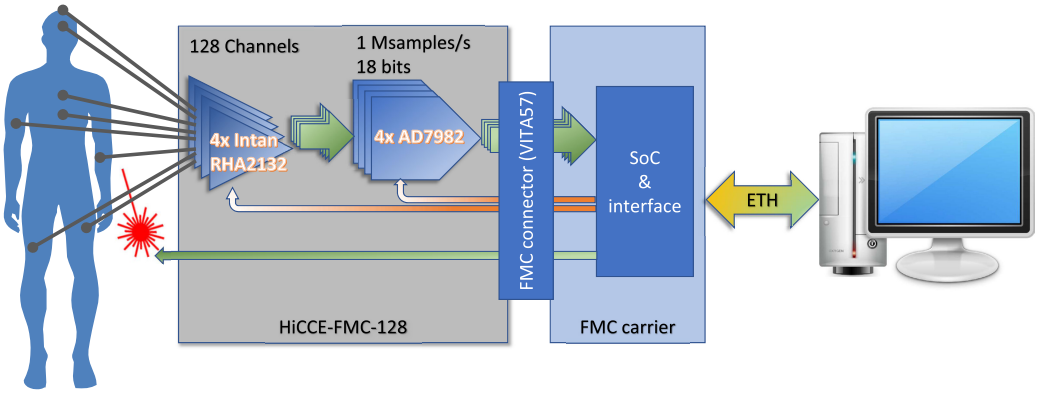

FIGURE 2. General schematic of the HiCCE architecture.

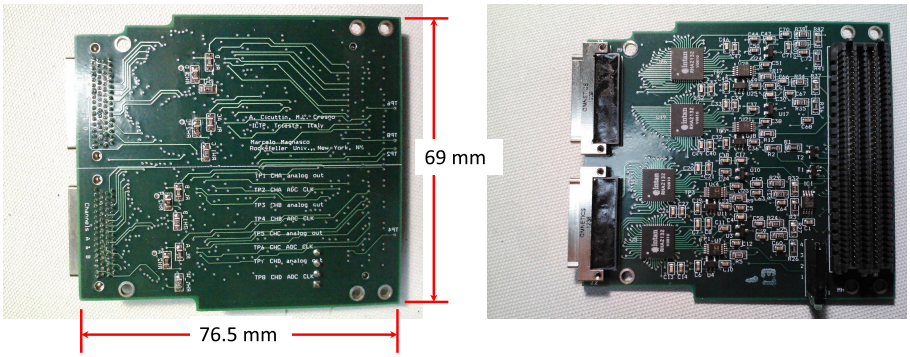

FIGURE 3. HiCCE-128v2.0 FMC board.

traces in the given standard FMC board size, we designed a 10-layers PCB shown in Fig. 3.

As shown in the Table 2, most of the electrophysiological signals are slow oscillatory and frequency of interest is less than 5 kHz. Thus, the sampling rate of the HiCCE is sufficient for digitizing these kinds of signals. The main focus of developing the HiCCE board is to process 128 independent channels parallel with the highest noise rejection. Low power consumption of the HiCCE opens up the possibility to use with portable electrophysiological acquisition systems.

There are several reliable commercial electrophysiology systems available, which are expensive and often unaffordable for individual use and research development. Moreover, most of these systems come with the whole unit including the proprietary acquisition systems and interfaces, which cannot be easily altered to the specification needed by the end user. Instead of proprietary interfaces, two 65 pin Omnetics connectors with gold-plated contacts have been used to collect electrophysiological signals. Thus, any kind of electrodes can be easily adapted to the system.

B. MODULAR FPGA ARCHITECTURE

Typically, front-end electronics of electrophysiology are controlled using microprocessors or microcontrollers. Since these controllers have fix hardware in the silicon, it is easy to programme them and example codes in several programming languages are available freely on the web. The sequential processing nature makes them inefficient in performance in many applications [45]. Moreover, the lack of computation capabilities limits feature extraction and compressions in microcontroller/ microprocessors. In modern experimental research on electrophysiology, it is very important to be able to record many channels, with the highest resolutions on both amplitude and time for a long period of time, where data acquisition systems with DSP-cores are renowned for. However, the modern hybrid programmable system on chip composed with FPGA and multi core processor nowadays offers high data rate acquisition, real time processing and transmission.

However, the associated complex internal structures of these SoC devices require significant designing and programming skills to successfully develop a working system and exploit its capacities. In order to simplify the complex real-time implementation, we efficiently split the design among the three main subsystems: FPGA, microprocessor (uP) and PC as shown in Fig. 4. External hardware controllers facilitate communication between FPGA and the application specific hardware, which is directly connected to the FPGA. All the time critical processing such as filtering and feature extractions are encapsulated in the Core FPGA Design.

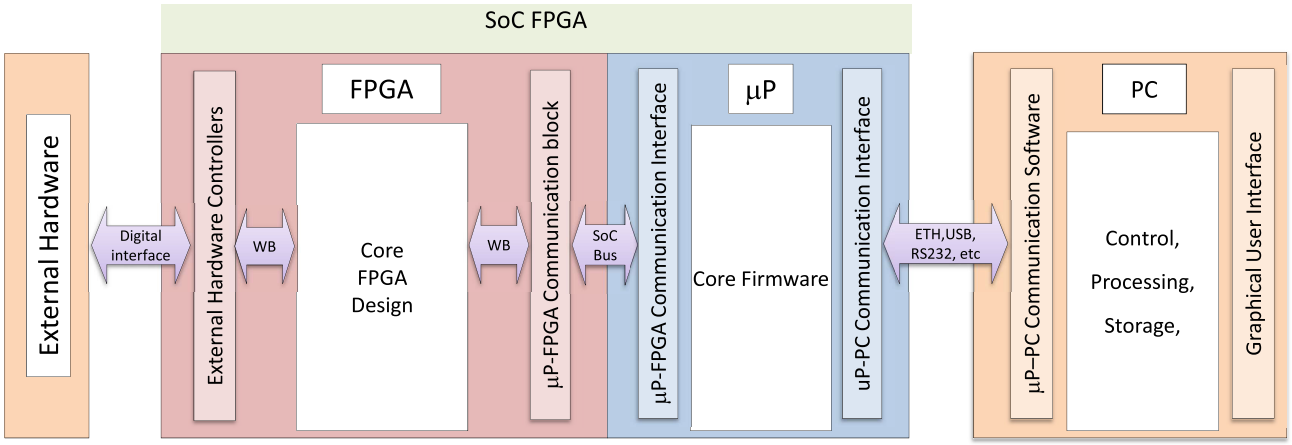

FIGURE 4. SoC FPGA based modular architecture for the HiCCE128 system.

Depending on FPGA vendor, interconnect between FPGA and microprocessor may have a different bus architecture such as the Advanced eXtensible Interface (AXI), or Avalon. We introduced the uP-FPGA communication block as a custom IP (ComBlock) [46] for the designing tool, where all the complexities of the SoC bus are effectively abstracted and hidden inside the IP. In this way, complex SoC designs can be easily ported to different vendors and families. In the FPGA, each block communicates each other with a simple standardized interface such as Wishbone standard bus interface.

Similarly, in uP, uP-FPGA communication interface and uP-PC communication interface are software routines that handled the relevant interfaces on FPGA and PC sides, while none time critical or microsecond accurate processors can be embedded in the Core Firmware. The PC resident software facilitates mainly data processing, storing and controlling the whole system by issuing commands through the graphical user interface (GUI).

In this work, we implemented the system in Xilinx's Zynq-7020, which consists of a dual core ARM Cortex-A9 processor tidily coupled with Artix-7 FPGA fabric based ZedBoard SoC board manufactured by Avnet [47]. The standard Ethernet communication with TCP/IP protocol was used to exchange data, commands and error messages between uP and software APIs in the PC.

C. ELECTRODES SYSTEM

Every electrophysiology system is composed of an electrode system, in which the type of electrodes can be varied depending on the target application. The electrode system must be able to pick up small localized electric potentials generated by the body. Since ECG and EMG signals produced by respectively cardiac activities of the heart and the electrically or neurologically activated muscle cells are in the range of millivolts, simple surface electrodes made out of conductive pads attached to the skin can be used to collect the signals. Typically, disposable adhesive Ag/AgCl electrodes use for such experiments.

EEG signals are much weaker than the others but have the same order of the noise. Typically, in EEG experiments, electrode cap or headset are used with the acquisition system. The official standard EEG electrode system is the international 10-20 system, where the cap has 21 electrodes distributed according to the standard [48]. However, the advancement of multi-channel electrophysiology systems, allows researchers to increase the spatial resolution of the EEG system. Although, caps with 10-20 standard can be easily found and available commercially, caps with higher density electrode arrays up to 500 electrodes can only be found in some manufactures with custom specifications. There are two main types of EEG caps: dry electrode and wet electrode caps. The dry electrode caps are easy to use, but signal sensitivity is low. On the other hand, wet electrode caps improve the sensitivity by applying conductive gel between electrode and scalp. However, it is difficult to clean and maintain the cap. Moreover, most subjects do not like to apply the gel to the scalp.

In this study, we used Ag/AgCl wet electrode caps, shown in Fig. 5 adjusted with the international 10-20 standard in order to obtain data with the highest EEG signal strength and adhesive electrodes for ECG and EMG signals.

D. PC CONTROL AND GRAPHICAL USER INTERFACE

Although the entire acquisition system is designed as an FPGA centric, some parameters of the FPGA side can be reconfigured from the host PC via a general purpose GUI developed based on National Instruments LabVIEW software. With compatible to the uP-PC communication interface settings, TCP/IP Ethernet protocol has been integrated into the GUI. The GUI communicates with the uP-PC communication interface of the SoC device through the uP-PC communication software API on the PC side. The core firmware built in the uP that handles configuration and readout routines according to the user requests coming from the GUI.

The GUI, in its current version (Fig. 6), is divided into two tabs:

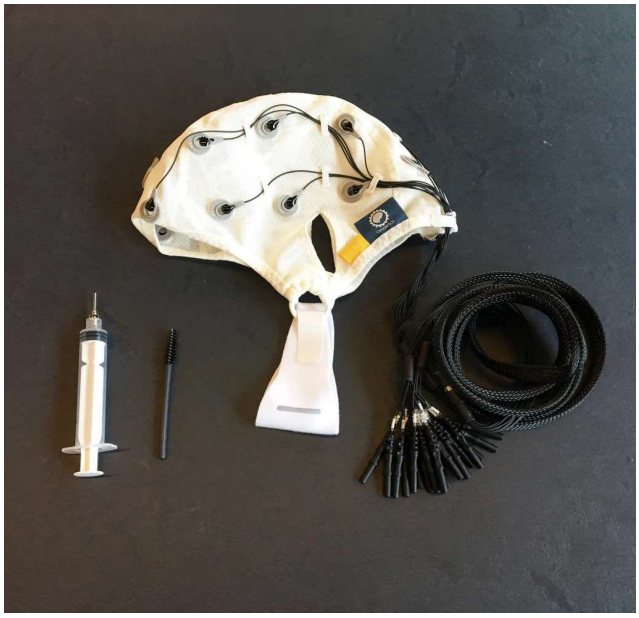

FIGURE 5. Ag/AgCl wet electrode cap with 10-20 standard.

- HiCCE-32 with Filter tab: can continually visualize up to 32 channels attached to each Intan chip as raw or filtered data. It is also facilitated to set the configuration parameters of the HiCCE such as selecting the mode, Intan block, filter bandwidth, and channels. Users can apply a standard infinite impulse response (IIR) Butterworth filter to the signals by specifying the filter characteristics in the "Filter specifications" section of the GUI.
- HiCCE-128 (Raw) tab: this tab displays all 128 channels continually without any calculations. When the number of channels is more than 32, it is difficult to visualize all the channels stacked in the same graph.

Moreover, all the data from the HiCCE-128 system can be stored in the PC for further analysis in both tabs. The standard graph palette of the software enables to zoom in/out and inspect sections of the signals.

IV. SYSTEM PERFORMANCE

This section describes the evaluation of the HiCCE-128v2.0 board and the acquisition system through simple experiments and measurements to validate the reliability of the system for electrophysiology researches. The sampling rate of the HiCCE-128v2.0 was set to 15 kSPS with the sequential channel selection mode for all the tests.

A. INPUT REFERRED NOISE

Input referred noise (IRN) represents the effect of all noise sources in the circuit, which include the noise introduced by the internal circuitry of the analog multiplexer and the ADC as well as the PCB. The IRN value provides an idea about the quality of the analog front-end electronics circuit. The measurements for the IRN have been performed with all input channels along with the reference input grounded.

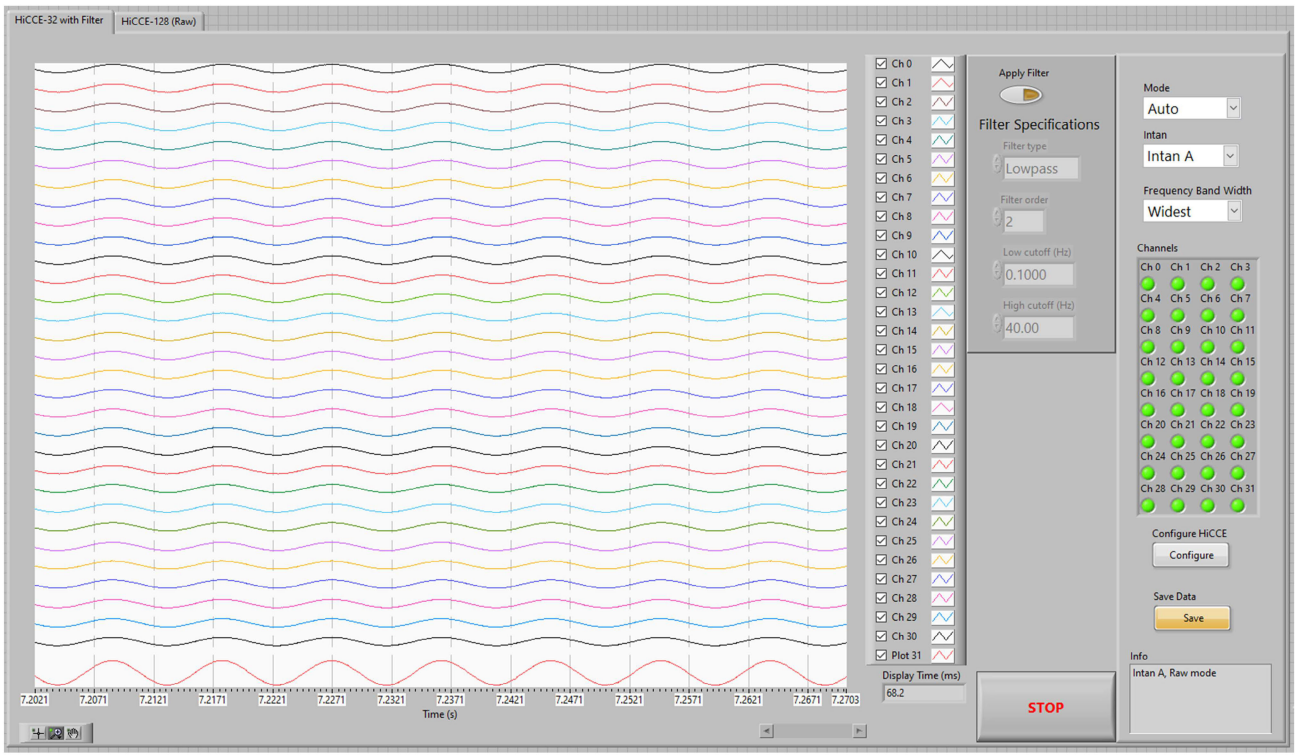

FIGURE 6. HiCCE-32 with Filter tab of the GUI.

The root mean square (RMS) of input referred noise was calculated for every channel, which are shown in Fig. 7. The measured IRN is less than 5 μV for all channels and the average value is about 3 μV. These values are in close agreement with the reported intrinsic noise of the Intan front-end chip that is about 2 μV rms. Although this value is larger than some of the commercial systems listed in the Table 1, a correct (or an accurate) comparison of noise figures must be done by considering the noise spectral density, a characteristic that is not generally specified in commercial instrumentation. Moreover, most of those values reported in the limited band of sampling frequencies except BioSemi ActiveTwo AD-box that is the most expensive system in the Table 1.

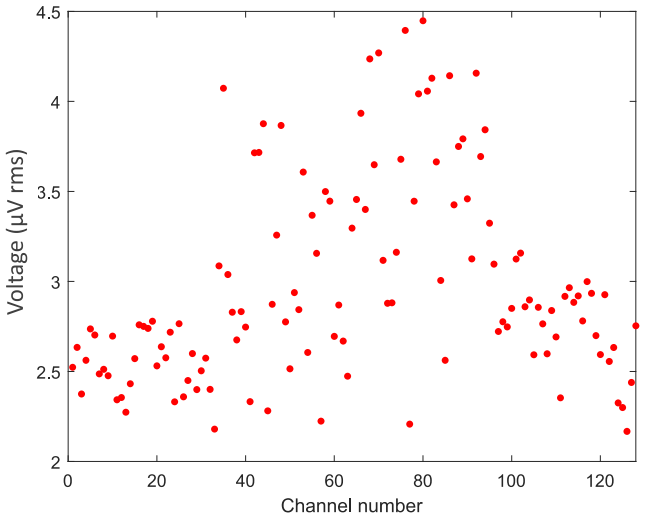

FIGURE 7. Input referred noise for every channel.

In the Fig. 7, it can be observed that IRN values from channel number 33 to 96, which corresponding to electrodes attached to the two Intan chips located closer to the edges of the PCB are much higher than on the others. The reason for this excess is probably due to the exposure to pick up interferences from the lateral edges of the board, while the Intan chips located in the middle of the PCB are naturally shielded being far from the edges. However, measured IRN on all channels is in the acceptable range.

B. COMMON MODE REJECTION RATIO

Common mode rejection ratio (CMRR) is a quantitative measure of the ability of the first stage differential or instrumentation amplifier to efficiently eliminate the common mode signal which simultaneously presents on both inputs at in-phase [49]. The measurements for the CMRR have been recorded by connecting all the channels along with reference to an external signal generator produced a fixed 1 kHz sine signal as shown in Fig. 8.

The CMRR can be estimated in decibels using the differential mode gain (A_{dm}) and the common-mode gain (A_{cm}) with the equation (1). It has been observed that the common mode

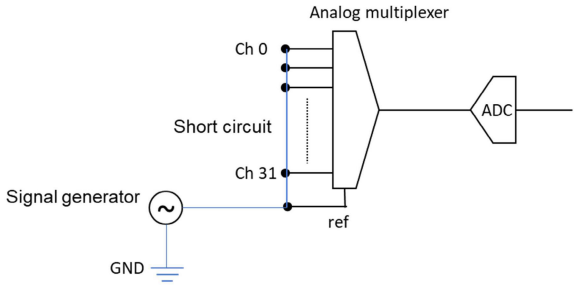

FIGURE 8. Circuit setup to measure Common Mode Rejection Ratio (CMRR).

rejection ratio of the HiCCE-128 system is about 81 dB.

$$CMRR = 20\log_{10}\frac{Adm}{Acm}. \quad (1)$$

The measured CMRR is also very similar to the value presented in the Intan front-end chip that is about 82 dB. These values are slightly lower than the CMRR values of the commercial data acquisition systems stated in the Table 1. Having a good CMRR guarantees accurate recordings of weak electrophysiological signals while rejecting common-mode signals. Typically, the CMRR value of front-end amplifiers greater than 70 dB is sufficient for suppressing common-mode interference in most electrophysiological recordings [50], while applying proper electric grounding and wiring schemes.

C. ELECTRICAL CHARACTERISTICS

During the IRN test, it has been observed that each channel has different baselines around 1.2376 V and spread in the range of approximately 20 mV, which is 100 μV referred to the analog input voltages since the gain of the front-end chip is 200. Fig. 9 shows the measured baselines of the 128 channels. According to the datasheet of the front-end chip, an on-chip voltage reference generates a DC voltage of approximately 1.235 V at the analog multiplexer output.

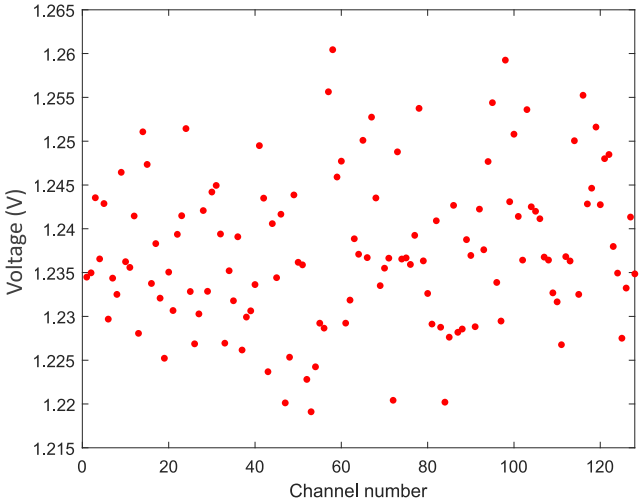

FIGURE 9. Analog output DC offset values of all 128 channels.

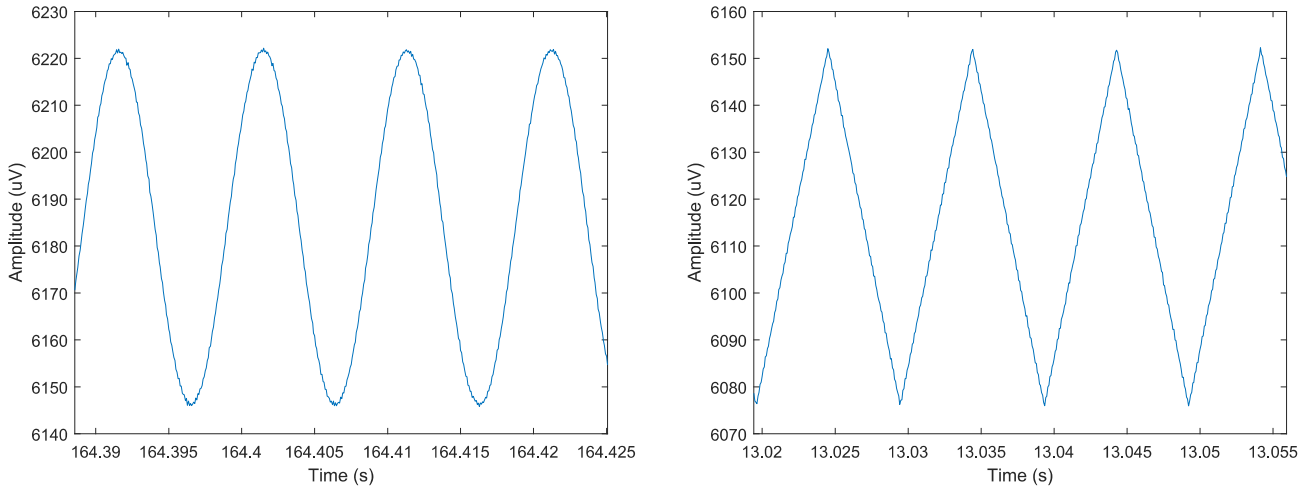

FIGURE 10. Typical response to sine and symmetric triangular signals of 76 μV amplitude and 100 Hz frequency.

Therefore, it can be stated that measured pedestal values are in close agreement with the reported value of the datasheet.

Before experimenting with the real subjects, the system was extensively tested with stimuli. The signals were generated by applying signal generator output to a simple resistor divider circuit or resistive voltage divider consisting of two resistors of 2 Ω and 26.2 kΩ. Thus, the total noise in the captured signal is the summation of the intrinsic noise of the HiCCE-128v2.0 board and the associated noise contribution from the stimulator circuit. Fig. 10 shows representative traces of captured sine and symmetric triangular signals correspond to signal generator output with a frequency of 100 Hz and peak to peak amplitude of 1 V. Therefore, the input signal to each channel is then 76.33 μV due to the resistive attenuation of the voltage divider circuit. According to the figure, it is being shown the ability to extract the signal from such a noisy environment. With these results, it can be concluded that the HiCCE-128 acquisition system was working properly.

These quantitative analyses show that the system is capable of acquiring electrophysiology signals with good noise suppression.

D. POWER USAGE

Current described acquisition system needs a wired communication link with the host PC. The system can be easily adapted for portable applications by replacing the wired Ethernet link with low-cost Bluetooth or Wi-Fi. For such a wireless electrophysiological system, the low power usage is the most important requirement which allows to record signals for a longer uninterrupted period of time.

On this matter, several low power FPGAs are commercially available [45] and numerous researches [51]–[54] showed that carefully tailored FPGA design can optimize the power consumption.

In this section, power usage of the system is investigated to identify the power drain parts and suitability for portable electrophysiological applications.

Xilinx provides tools and guidelines to estimate the power usage of the FPGA at different stages of the design cycle: pre-design, pre-implementation, post-synthesis, post-placement, and post-routing [55]. Among them, the most accurate power analysis and estimation give at post-route since it incorporates the resources from the implemented design. Thus, a vectorless power evaluation at post-route was performed in the Vivado tool with settings specified in Table 3. The On-Chip power summary that was generated is presented in Table 4. According to this table, the tool predicted 1.521 W power usage and processor dynamic power utilized 91% of the total calculated power, whereas the DDR3 memory interface consumed 72% of it. However, the HiCCE-128v2.0 FMC board is not considered for the power calculation by the software tool since the power model for the board is not integrated. Incorporating the power information on component datasheets [35], [36], [56], [57] of the HiCCE board, the power consumption of the board can be loosely calculated

TABLE 3. Parameters for post-route power estimation.

Settings	Values
Family	Zynq-7000
Device	XC7Z020
Package	CLG484
Speed Grade	-1
Temp Grade	Commercial
Process	Maximum
Ambient Temp	30.0 °C
Airflow	250 LFM
Heat Sink	Low Profile
Board Selection	Medium (10"x10")
No. of Board Layers	8 to 11

TABLE 4. On-Chip power estimation summary.

Resource		Power		
		(W)	(W)	(%)
FPGA Dynamic	CLOCK	0.013	0.036	2
	LOGIC	0.004		
	BRAM	0.014		
	DSP	0.000		
	PLL	0.000		
	MMCM	0.000		
	Other	0.000		
	IO	0.004		
FPGA Static		0.041	0.041	3
Processor Dynamic	LOGIC	0.348	1.390	91
	DDR	1.004		
	IO	0.038		
Processor Static		0.055	0.055	4
Total On-Chip Power			1.521	100

and that needs to be added to the overall power utilization. The maximum power usage of the HiCCE-128v2.0 is less than 1 mW/channel where the Intan analog front-end chips and ADCs consumed approximately 95 % of the total power consumption. Moreover, the wired Ethernet link consumes 350.4 mW from off-chip power rails [47] and 3 mW from on-chip power connections that included in the power calculation of the Processor Dynamic in the Table 4.

Normally, the actual power consumption of the board is higher than the estimated values due to uncertainties related to the device power models and various other reasons. Zedboard has a 10 mΩ, 1 W on-board current sense resistor in series with the 12 V input power supply [47], which can be used to measure current flow to the board. The voltage across this resistor ($V_{10m\Omega}$) and the input power supply voltage (V_{in}) were measured using a standard multimeter and total power consumption (P) was calculated according to the equation (2).

$$Power(P) = \frac{V_{10m\Omega}}{10} \times V_{in} \tag{2}$$

Measurements have been taken for two different scenarios: before and after downloading both FPGA bitstream and ARM program. Collected readings are listed in Table 5. When the SoC device operates without any configuration, it consumes a fair amount of power due to leakage current of the transistors, which is called device static (leakage) power. The total power of the fully configured SoC device is the sum of the device static, design dynamic, and off-chip powers, which is in this case 2.85 W.

Next subsections will present some common experimental electrophysiology signals acquired using the system.

TABLE 5. Measured power consumption of the setup.

Condition	Voltage (mV)	Current (A)	Power (W)
Device static power	1.7	0.17	2.04
Total Power	2.4	0.24	2.85

E. ALPHA WAVES AND EYE BLINKS

EEG signals are quite complex and most of the time, patterns are not visible in the time domain. However, a clear pattern in the alpha band of the EEG signal can be seen from a relaxed waked human when the eyes are closed [58], [59]. Eye blinking or Electro-oculographic (EOG) can also be captured easily since it generates a strong signal compared to EEG [60], [61]. An electrode was placed at the O1 occipital region to record the alpha wave while the reference and ground electrodes were connected to the Pz location and left earlobe respectively. In order to capture the eye blinks simultaneously, an electrode was placed near to the top of the left eye to detect the activities of the superior rectus muscle. Since we are interested in capturing vertical eye movements as eye blinks, a single electrode is sufficient. The electrode placement for this test is shown in Fig. 11.

Test procedure was started by instructing the subject to close both eyes and stay relax. Recordings were initiated with closed eyes and asked to open and again close eyes while maintaining approximately 2 seconds between each event. In the LabVIEW software, 6th order Butterworth lowpass infinite impulse response filter [62] with a cutoff frequency of 40 Hz was set for the O1 and the EOG channels in order to remove unwanted high frequency components. Since the eyeball of the subject acts as a dipole, relatively large opposite polarized potentials can be identified for eye open and close as seen in Fig. 12 b. It has been more evident from Fig. 12 a. and c. that suppression of the typical alpha wave, which is loosely defined the activity of the 8-16 Hz frequency region of the occipital cortex area of the brain during the open eye condition. In this case, the effect of the eye blinking artifacts to the EEG signal is minimum since the source of the artifacts is far away from the EEG recording electrode.

These test results demonstrated the ability to record microvolt EEG signals as well as millivolt EOG signals simultaneously with the HiCCE-128v2.0 front-end electronic board along with the SoC without having crosstalk.

F. ECG SIGNAL ACQUISITION

Electrocardiography (ECG or EKG) test can be performed easily since the electrical signals produced by the cardiac muscles are much higher. Three disposable adhesive Ag/AgCl electrodes were placed on the chest region as depicted in Fig. 13 to record the electric activity during the heartbeats. Amplifier signal input and the reference are attached approximately 10 cm apart while the ground electrode was placed a few centimeters below the right shoulder.

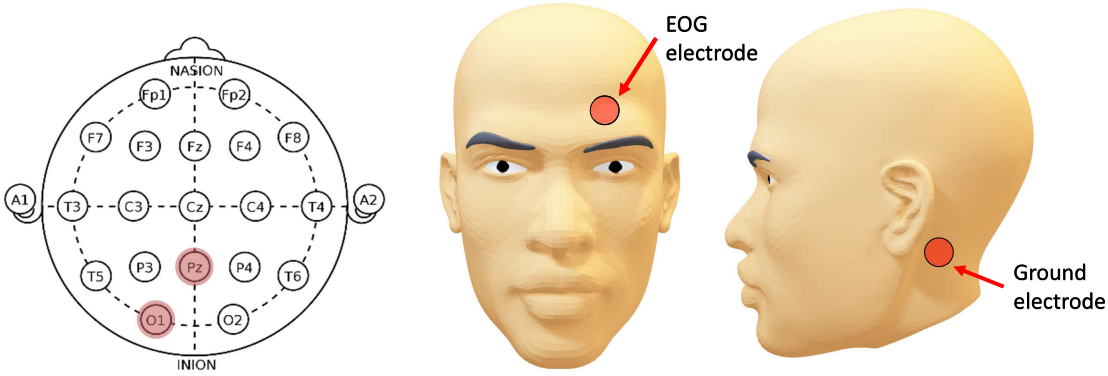

FIGURE 11. Electrodes placement for the alpha waves and eye blink detection.

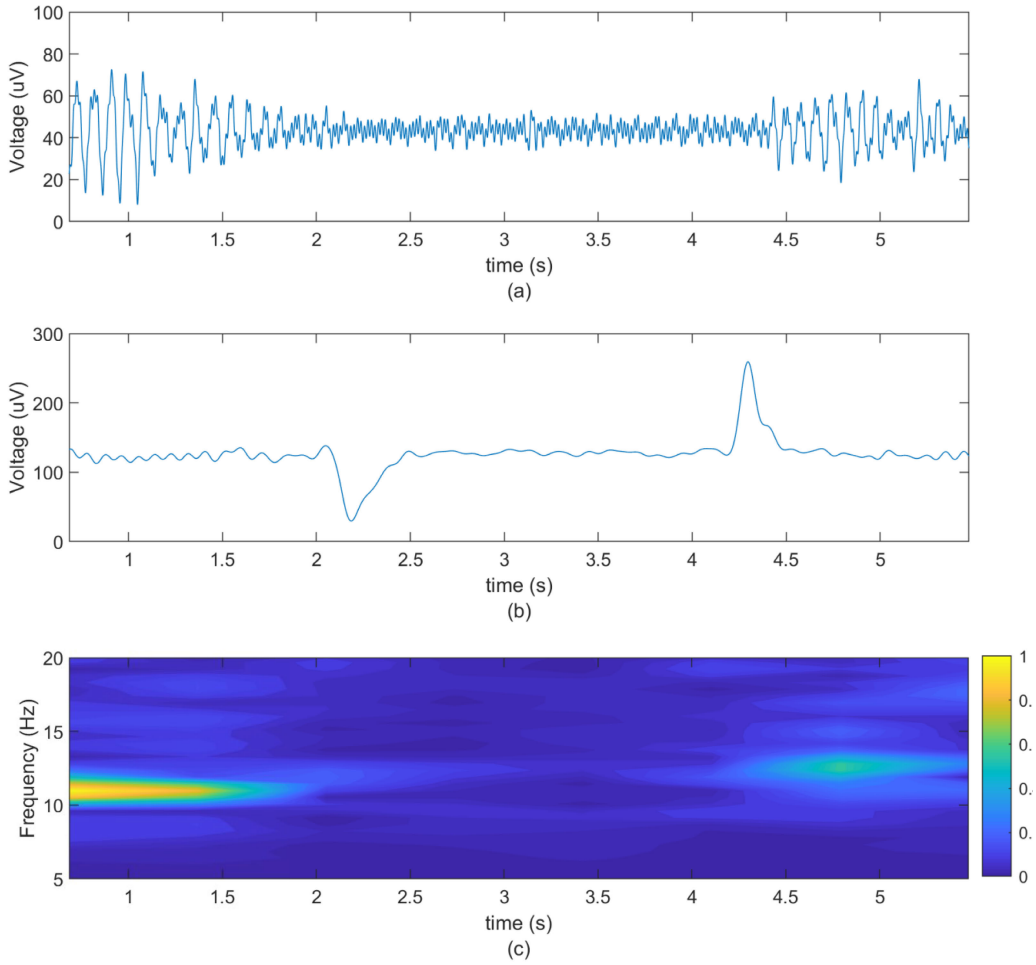

FIGURE 12. (a) Alpha signal, (b) EoG signal, and (c) time-frequency plot.

The same IIR filter used with EEG/EOG test was utilized with a cutoff frequency of 100 Hz for the ECG signal where ECG generally contains frequency components from 0.5 Hz to 100 Hz. It can be easily identified the ideal ECG signal characteristics such as the P wave, the QRS complex, and the T wave from the recorded data shown in Fig. 14.

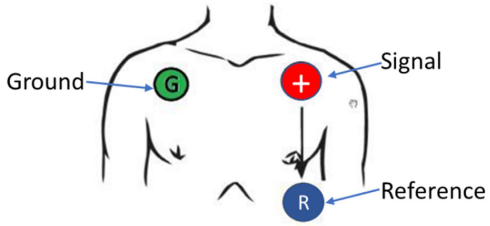

FIGURE 13. Electrode placement for the ECG test.

G. EMG TEST

Acquiring an electromyogram (EMG) signal is also uncomplicated because of the millivolt signal magnitudes. However, the signal may contain unwanted artifacts unless the subject does not follow a proper procedure. Three adhesive Ag/AgCl electrodes were located on the right-hand bicep and elbow as shown in Fig. 15. EMG signal recording was initiated by asking to relax the arm and make bicep contractions for approximately 2 seconds intervals.

In this test, a 10th order Butterworth bandpass IIR filter was employed with 5 Hz and 1 kHz lower and upper cutoff frequencies respectively. High amplitude disturbances of the EMG signal in Fig. 16 correspond to two bicep contractions, which confirms the sensitivity of the system for EMG activities.

These tests provided visual and qualitative evidence for the effectiveness and reliability of the system.

V. DISCUSSION

Qualitative as well as quantitative evidence to support the reliability of the recording system have been provided in the previous sections by means of the most common electrophysiology signals recording techniques and parameters.

The most important requirement of any medical recording instrument is to acquire and record data continuously without losing any data sample. The communication link between the HiCCE-128 acquisition system and the PC is based on the TCP/IP Ethernet protocol that provides more reliable data transfer in terms of data integrity and availability since it uses a three-way handshake, re-transmission, and error-detection mechanism to ensure uncorrupted data transfers. However, a replica of the data temporarily stored in the external DDR memory and an additional procedure was implemented in the ARM processing system to act accordingly in case of data drop. On the PC side, the GUI software provides TCP/IP drivers and efficient way of handling errors to ensure that no data will be lost during the run. To validate the lossless communication and recording, all the 128 channels of the system were stimulated with a 100 Hz sinusoidal signal and recorded the raw data at the maximum sampling rate of 31.25 kSPS along with the time stamp for 1 hour. Recordings were repeated several times and no samples were lost during the recording periods. This confirms the ability of the HiCCE-128 acquisition system to acquire data continuously for longer periods of time without losing data samples.

Although the sampling rate of 31.25 kS/s is more than enough for most of the electrophysiology experiments, any 4 channels (one channel from each chip) can be digitized at the highest ADC sampling rate of 1 MS/s. Moreover, the reconfigurable FPGA design allows users to dynamically access and record channels with any random sequence of the analog multiplexer which can be then used to digitize at a higher frequency than 31.25 kS/s at the expense of the number of channels.

It is often argued that electrophysiological data does not need to be sampled at high-frequency or too many bits of resolution. However, acquiring electrophysiological data with reasonably high sampling frequency and amplitude resolution is very important for a number of reasons. It may involve rare, unique or expensive experimental animals, it may involve human patients with rare or unique conditions, and it

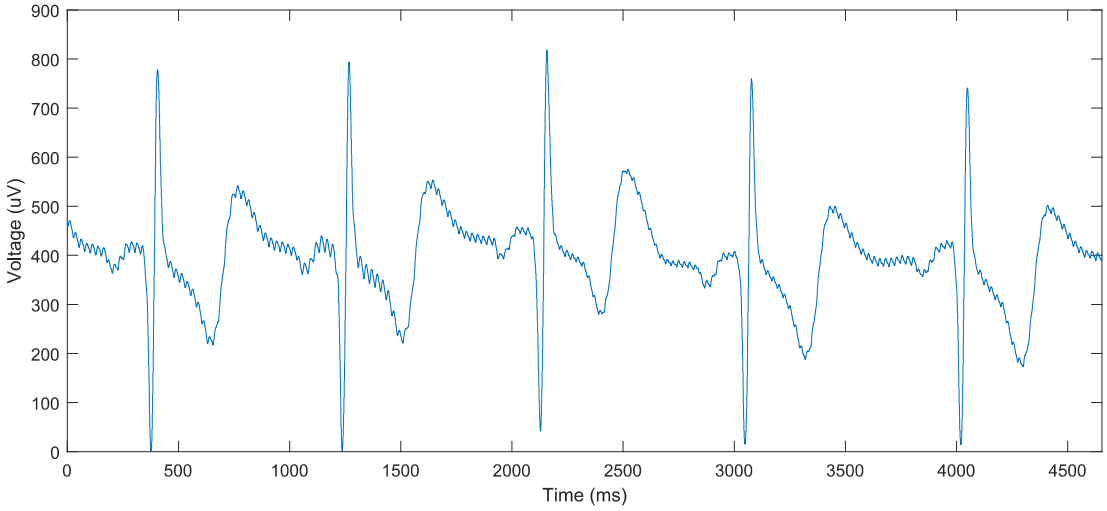

FIGURE 14. A section of the recorded ECG signal.

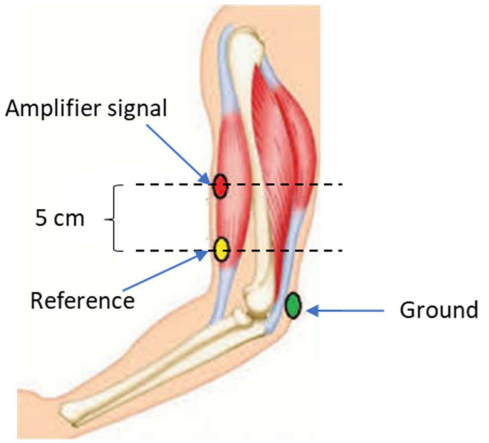

FIGURE 15. Electrodes placement at the right-hand bicep for the EMG test.

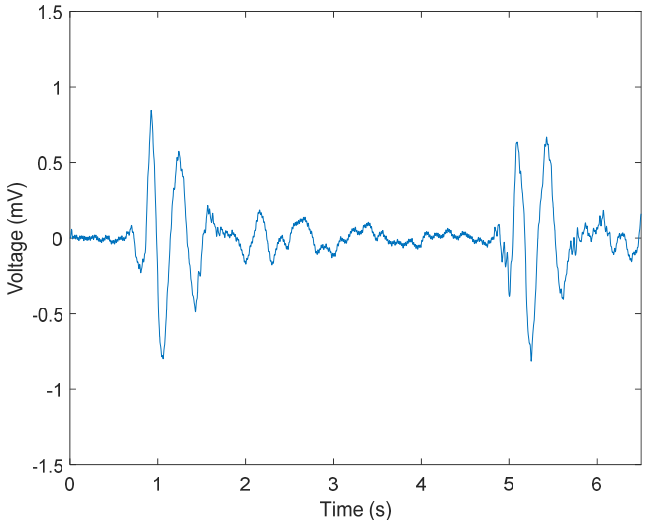

FIGURE 16. Two EMG contractions recorded with the system.

always involves an extraordinary amount of labor - surgeries, custom-crafting of electrophysiological arrays, patient care, and so forth. Because of this, many times these valuable data get re-analyzed for other purposes and studies well after initial findings. Therefore, it is very important that the irreversible digitization process be carried out, not just to the standards of the current purpose of the recording, but to the state of the art. Future studies that may require high time or amplitude resolutions will definitely benefit from these high quality recorded data. Thus, it is wise not to limit the specifications for a design of a new research instrument (like our HiCCE-128) considering standard or simplistic engineering criteria.

Electrophysiology is a vast field of study and most of the applications need customizable software solutions to adjust according to their requirements. However, researchers in the field of electrophysiology may not be experts in computer programming languages, which requires software development and customization that can be a time consuming process.

Although the proposed architecture is targeted at the electrophysiological experiments, the modular hardware and block-based design methodology emphasize the design reuse with a variety of instruments for advanced scientific researches, which have similar characteristics.

Designing a PCB for electrophysiology instruments is a challenging task, where the noise introduced by the signal paths and electronics needs to be minimum. According to the input referenced voltage noise measurements, we showed that the noise measured on the PCB is 1 μV on average over the reported intrinsic noise of the front-end chip that is about 2 μV. To achieve such a good design, few strategies were followed while designing the PCB, as follows:

- Crossing digital and analog signals each other on any adjacent two layers was avoided to insulate the signals coupling from each other.
- Most of the analog inputs placed between two solid grounds or power planes to further isolated analog signals from digital crosstalk and background noise.
- A solid ground plane was used on the second layer, which also acts as a thermal conductor and a heat sink to keep temperature levels of all the attached devices minimum.
- By carefully calculating trace widths and via sizes, the characteristic impedance of the PCB was managed.

For an experiment which requires more channels than described system offers, it can be facilitated by migrating to a different SoC board with multiple FMC connectors. With the proposed FPGA modular design strategy along with standard FMC and Ethernet links allow to upgrade or reutilize embedded software programs and associated FPGA design for a board with not only different device families but also different vendors.

Most of the time this kind of multichannel instrument, number of channels bounds by the speed of the communication link between the acquisition board and the PC or storing unit. The standard Gigabit Ethernet with secure TCP/IP protocol that employed in the system is capable of transferring data approximately 940 Mbps both in transmission and reception in baremetal mode as the results of the iperf network benchmarking test indicates [63]. Even though practically these numbers are much lower because of the other activities of the processor, data from 512 channels produced at 31.25 kS/s could be managed by the current communication link.

Furthermore, the system can be easily adapted to wireless data transfer through a Wi-Fi or a Bluetooth link. However, the number of channels or sampling rate needs to be reduced since the data rates of wireless links are much lower than the wired Ethernet communications.

The ZedBoard is a cost-effective commercial development board that comprises several on-board peripherals such as display, audio, LEDs, switches, etc. as well as expansion connectors. Most of these peripherals and connectors may not be essential for low power portable applications, where a customized carrier would be beneficial. CIAA-ACC [64]

is an open source FPGA hardware based on Xilinx's Zynq-7030, which might be a good replacement since not only the number of peripherals but also the physical size of the board is smaller compared to the ZedBoard.

Modular hardware and software architecture of the HiCCE-128 electrophysiology system enables unlimited research opportunities from advanced closed loop experiments to clinical research. Especially in closed loop experiments require high speed acquisition and processing in order to make decisions at the lowest latency for controlling external hardware or stimulator.

The total latency of a system mainly depends on the type of online processing related to the target application and some constant overheads defined by front-end electronics, data transfer links, and hardware delays. The presented system comprises three main processing elements (FPGA, uP, and PC) and any data processing could be distributed to some or all of these elements whereas the shortest latency is achieved when only the FPGA is involved. Although the presented design does not offer online processing in the FPGA, the implemented modular FPGA architecture provides the infrastructure to realize such processing.

The latency in the HiCCE-128v2.0 front-end board with the maximum sampling frequency is approximately 0.86 μs. The FPGA design of the proposed system sends data to PC through the processor and Ethernet as a block of user defined N samples of data stored in a FIFO (First In, First Out), where all the experiments present in this paper were conducted with $N = 512$. The time delay for filing the FIFO makes the largest latency contribution to the system, which is approximately 1.07 ms with the tested settings.

One promising research that could utilize the full capacity of the system is the simultaneous signal acquisition for motor control evaluation [32], [33], [65]–[69]. Such an experiment needs a system that able to synchronously monitor and track signals from different parts of the patient's body, where each section may require different number of channels with various sampling rates. Typical signals collection is shown in Fig. 17 with relevant properties. These kinds of research are normally done using expensive non customizable acquisition systems dedicated for each signal type while losing the synchronicity between the data also.

Table 6 provides a summary of the most important functionalities of the proposed system with a comparison between other systems discussed in the literature. It should be noted that all the other's works are non-scalable, except [23], which however, does not facilitate local data processing or calculations. As presented in the Table 6, most of the listed properties are better in the HiCCE-128 acquisition system than the other compared systems. Thus, it can be expected higher performance and reliable electrophysiological acquisitions from the proposed system compared to other listed systems.

The analog front-end electronics (AFEs) in the majority of the listed systems were developed based on the Texas Instruments ADS1298/ADS1299 chips [70], [71] that has a maximum of 24-bit resolution in the sampled data. However, this resolution decreases with higher sampling rates due to the sigma-delta decimation used internally. The ADC resolution

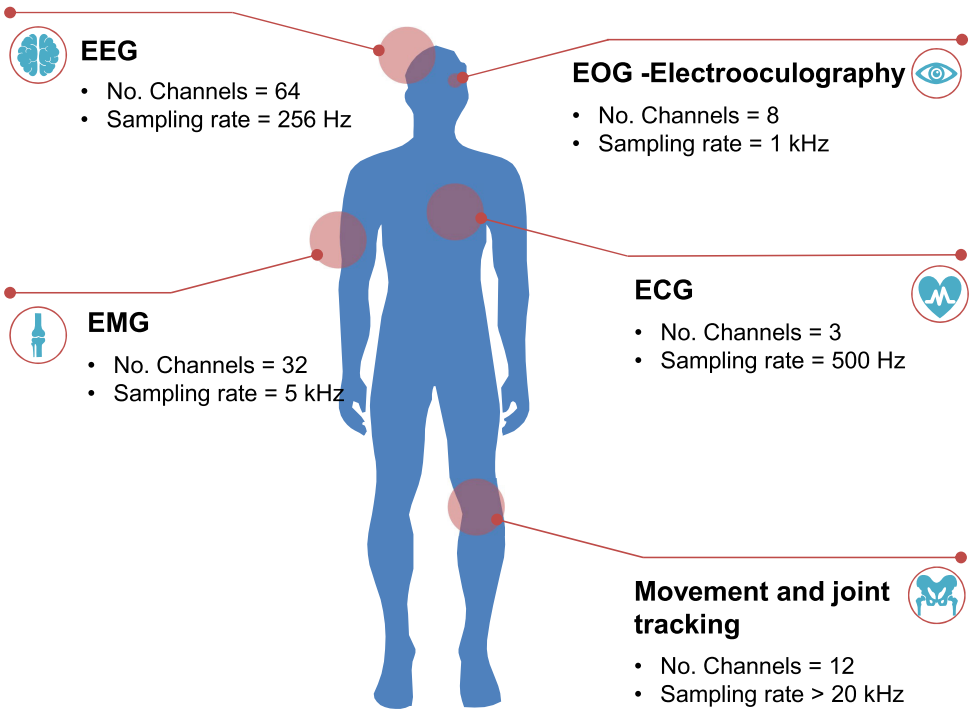

FIGURE 17. Typical simultaneous signal collection for motor control evaluation application.

TABLE 6. Comparison with existing systems.

Property	Proposed system	Pinho et al. [21]	Feng et al. [22]	Vo et al. [23]	Wild et al. [24]	Nathan et al. [25]	Shyu et al. [26], [28]	Khurana et al. [27]	Annese et al. [7]
Modular	Yes	No	No	Yes	No	No	No	No	No
Channels	128	32	16	8	4	16	2	N/A	16
Sampling frequency, Hz	31.25k	1000	1024	250	250	N/A	8k	250	500
ADC number of bits	18	24	24	24	24	24	12	N/A	16/24
Connectivity	Ethernet	Wi-Fi 802.11 b/g/n	Wi-Fi 802.11 b/g/n	Bluetooth	Bluetooth	Bluetooth	413 MHz RF	Ethernet	N/A
Processing device	Xilinx Zynq 7020	Texas Instruments DM3730	BeagleBone Black	ST Microelectronics STM32F4	Microchip ATmega328p	Texas Instruments MSP430	Altera Cyclone II FPGA	Xilinx Spartan 3E FPGA	Altera Cyclone V FPGA
CMRR, dB	-81	-115	N/A	-110	-110	-110	130	N/A	N/A
Local processing[a]	Yes	Yes	No	No	No	No	Yes	Yes	Yes

[a]In addition to acquisition and transmission.

of such an AFE reduces from 24-bits to 17-bits, when sampling frequency increases from 8 kSPS to 32 kSPS, which is a tradeoff between the sampling rate and the resolution whereas corresponding values of the proposed system does not vary with the sampling frequency. Moreover, higher sampling resolution like 24-bits offered by the TI chip is not necessarily required since such a high discretization resolution cannot be usually achieved due to much higher noise contributed by various sources. The least significant bit (LSB) of the proposed 18-bit system corresponds to a value of about 0.04 μV input referred voltage, which is well below the typical 2 μV intrinsic input referred noise of the front-end chips. It is also understandable that all the listed 24-bits systems use lower sampling frequencies, which is due to large dependency of the input referred noise with the sampling rate of the analog front-end chip.

A fair amount of power of the 12 V power supply of the ZedBoard is wasted on the voltage down converters and regulators, where some of these conversions do not need for the proposed HiCCE-128 electrophysiological acquisition system. Even with these issues, the present proposed system shows reasonable power consumption, which is approximately 2.85 W power in total thereby each channel utilized about 22 mW. Hence, a miniature SoC carrier board, which has optimized power supply circuitry along with the HiCCE-128v2.0 FMC board could be a better option for portable electrophysiology applications.

As discussed in the Section IV, the memory subsystem of the processing system consumes most of the power of the SoC chip compared to other components of the chip. The total power can be significantly reduced by utilizing Low Power DDR2 (LPDDR2) SDRAM with associated controllers instead of the DDR3 memory system since numerous optimization techniques are employed in the LPDDR2 to achieve lower power [72], [73].

The local processing may be important in some time-critical applications, where accessing to a sophisticated PC that can generate the desired responses might be difficult. Some of these applications may require processing 128 channels with extensive algorithms in parallel and real-time. General-purpose PCs are not suitable for such applications since real-time support is not available; thus, the latency will drastically increase. Even though multi-core PCs can process data in parallel to some extent, within the single core, the processings are not truly parallel. The developed system can be adapted to such situations by implementing the time-critical process in the FPGA as local processing preserving real-time features.

Open source modular hardware and software architecture of the HiCCE-128 electrophysiological signal acquisition system along with high spatial and temporal resolution brings many electrophysiological experiments paradigms within reach. Moreover, high response and low power HiCCE-128v2.0 analog front-end board provide additional attraction on top of the capability of processing multiple channels simultaneously in locally and easily reconfigurable SoC design.

VI. CONCLUSION

In this paper, we presented a modular and scalable high-response data acquisition and processing system for High-Channel Count Electrophysiology capable of simultaneously

acquire, process and transfer electrophysiological signals at high channel counts for long uninterrupted periods of time. The system consists of a custom-made front-end electronic board called HiCCE-128v2.0 compliant with the industrial FMC mezzanine standard and a commercial FMC carrier based on a modern programmable system on chip.

The electrical characteristics of the developed board showed a low input-referred noise of 3 μV on average in the frequency range from 0.75 Hz to 20 kHz and a common-mode rejection ratio of 81 dB that sufficient for most of the electrophysiology applications. It is also verified that the system can distinguish very low signals such as 76 μV referred to input signals from the noise. These tests proved that the developed system works properly and does not degrade overall features compared to the features of the Intan front-end device offers.

The system has been thoroughly evaluated by means of common electrophysiological applications such as EEG alpha wave, EoG eye blinking, ECG and EMG signal tests. The results confirmed the ability of the system to correctly and effectively capture electrophysiological signals.

With the on-chip power estimation and real power consumption tests verified that by choosing an appropriate FMC carrier board, the HiCCE-128 acquisition system can be adapted to low power portable electrophysiological applications.

The design of the SoC has been improved with the Comblock based architecture, which efficiently partitions the FPGA and processor subsystems by hiding the complexities of the SoC device architecture. This makes not only the hardware but also the FPGA design modular, and portable across several FPGA SoC devices and vendors.

The HiCCE-128 acquisition system is well suitable for neurological rehabilitation, which requires synchronous signal acquisition for different parts of the body at various sampling rates and number of channels. Besides the recording, the reconfigurable nature of the SoC devices allows implementing parallel online data processors with high computing capabilities.

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