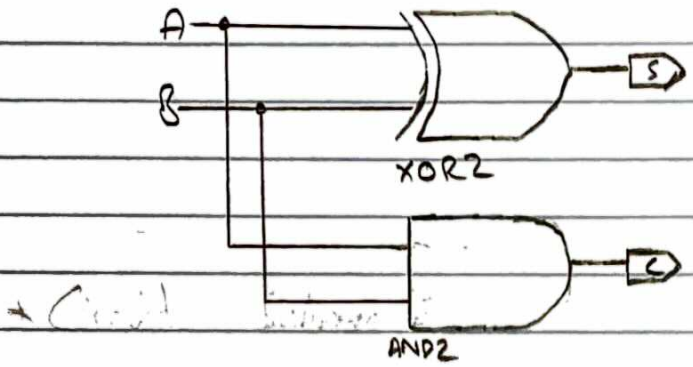
Abdullah Rizk
22001296
section: 01

CS 223

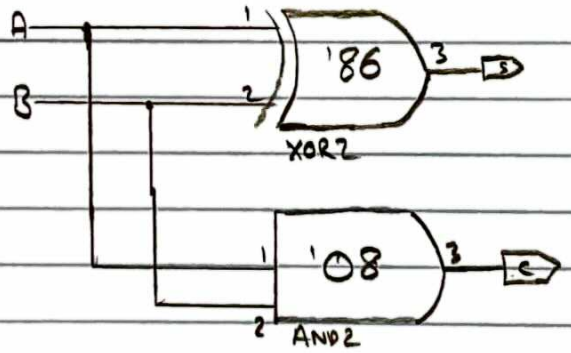
Lab 1 : Preliminary Report

① Half Adder

* Logic Diagram



* Circuit Schematic

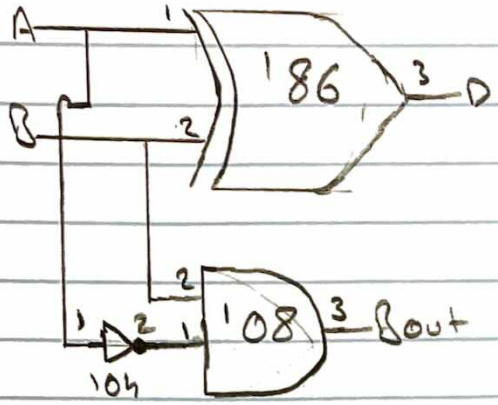


* IC List

① One 7486 Quad 2-input XOR gate
② One 7408 Quad 2-input AND gate

* 7486 7408
GND-7 GND-7
+5V-14 +5V-14

② Half Subtractor

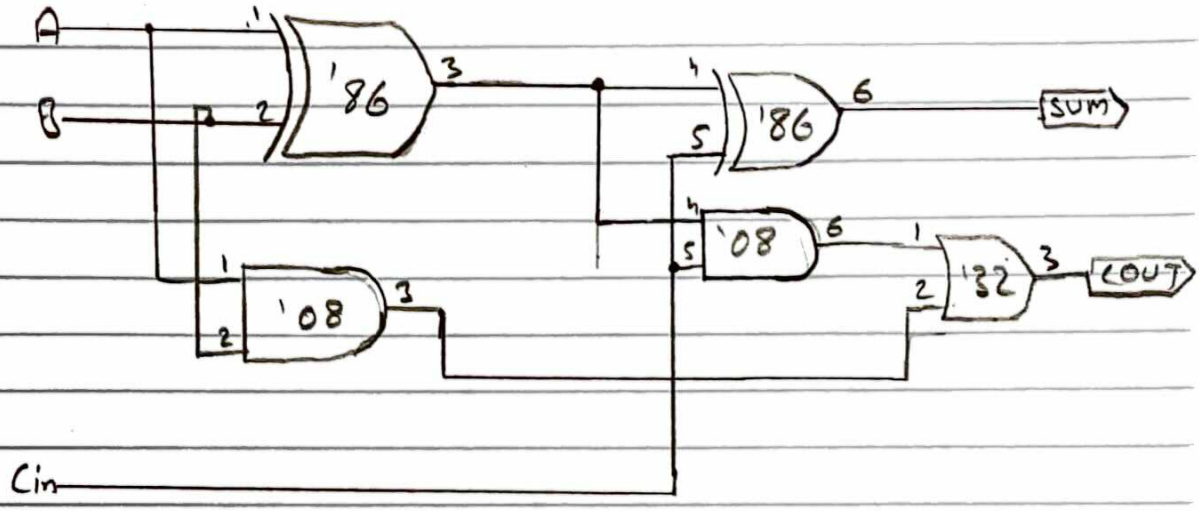


* IC List

① One 7486 Quad 2-input XOR gate
② One 7404 Hex inverter gate
③ One 7408 Quad 2-input AND gate

* 7486	7404	7408
GND-7	GND-7	GND-7
+5V-14	+5V-14	+5V-14

③ Full Adder

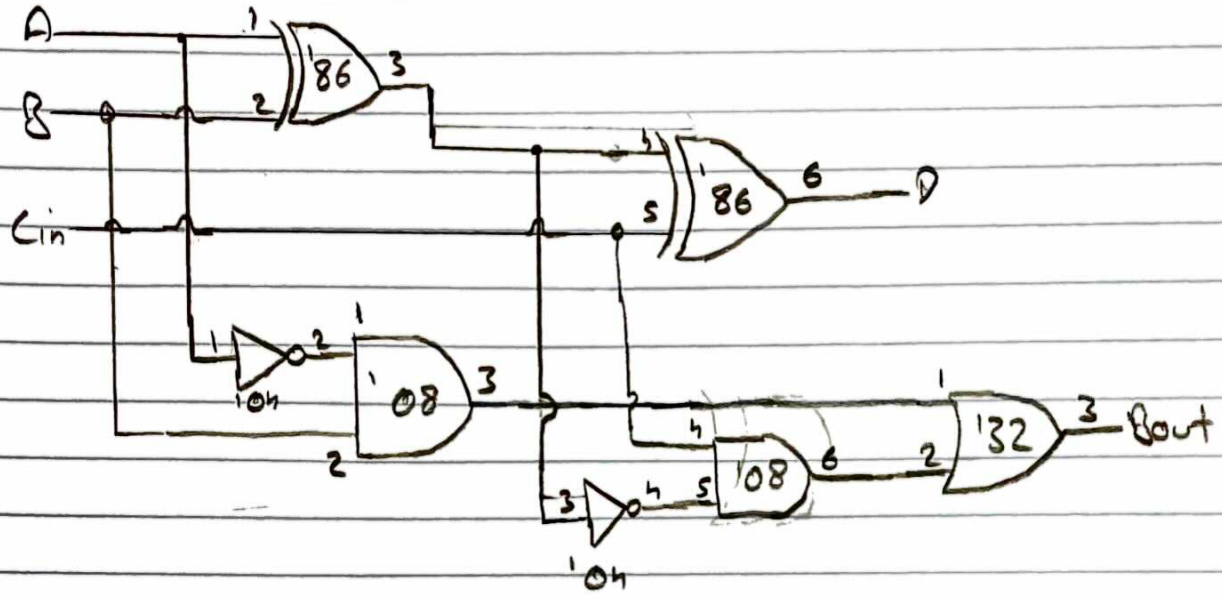


*IC List

① One 7486 Quad 2-input XOR gate
② One 7408 Quad 2-input AND gate
③ One 7432 Quad 2-input OR gate

* 7486	7408	7432
GND-7	GND-7	GND-7
+5V -14	+5V -14	+5V -14

⑤ Full Subtractor



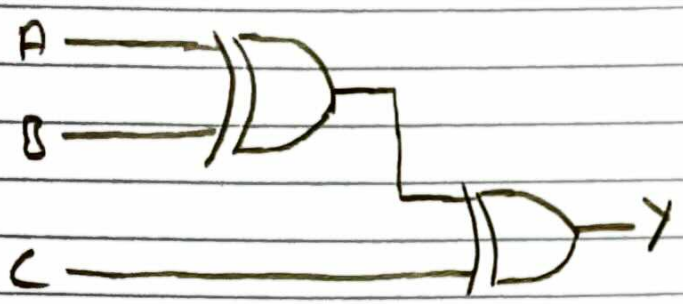
*IC List

① One 7486 Quad 2-input XOR gate
② One 7404 Hex Inverter gate
③ One 7408 Quad 2-input AND gate
④ One 7432 Quad 2-input OR gate

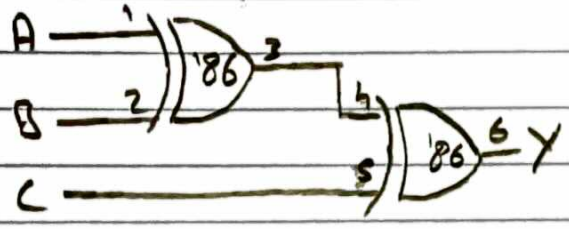
7486	7404	7408	7432
GND-7	GND-7	GND-7	GND-7
+5V-14	+5V-14	+5V-14	+5V-14

(5) 3-input XOR gate

* Logic Diagram



* Circuit Diagram



*IC List

(1) One 7486 Quad 2-input XOR Gate

7486
GND - 7
+5V - 14