2021–2022 SPRING SEMESTER

CS224 – LAB 6 PRELIMINARY DESIGN REPORT

EXAMINING THE EFFECT OF CACHE PARAMETERS AND PROGRAM FACTORS ON CACHE HIT RATE

NAME: ABDULLAH RIAZ
ID : 22001296
COURSE:CS224- COMPUTER ORGANIZATION
SECTION: 06
DATE: 24/04/2022

Q1)

No.	Cache Size KB	N way cache	Word Size (no. of bits)	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Block Offset Size in bits[1]	Byte Offset Size in bits[2]	Block Replacement Policy Needed (Yes/No)
1	64	1	32	4	4096	15	12	2	2	No
2	64	2	32	4	2048	16	11	2	2	Yes
3	64	4	32	8	512	17	9	3	2	Yes
4	64	Full	32	8	1	26	0	3	2	Yes
9	128	1	16	4	16384	14	14	2	1	No
10	128	2	16	4	8192	15	13	2	1	Yes
11	128	4	16	16	1024	16	10	4	1	Yes
12	128	Full	16	16	1	26	0	4	1	Yes

Q2)

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw $t1, 0x24($0)	Compulsory	None(hit)	None(hit)	None(hit)	None(hit)
lw $t2, 0xAC($0)	Compulsory	None(hit)	None(hit)	None(hit)	None(hit)
lw $t3, 0xC8($0)	Compulsory	None(hit)	None(hit)	None(hit)	None(hit)

b)

4GB = 2^{32} Bytes

Instruction Address Size = $\log_2(2^{32})$ = 32 bits

Cache Blocks = (16 * 4) / (4* 4) = 4 Blocks

Sets = 4/2 = 2 Set

Byte Offset = 2 bits

Block Offset = 2 bits

Set No. = $\log_2(2)$ = 1 bit

Tag = 32 - 1 – 2 - 2 = 27 bits

1 + 27 + 4 * 32 = 156 *2 = 312 bits per set (multiply by 2 since 2-way)

2 * 312 = 624 total cache memory size

C) 2 AND Gate, 2 Comparator, 1 OR gate , 2 32-Bit 4:1 mux, 1 32-Bit 2:1 Mux

3a)

Instruction	Iteration No.				
	1	2	3	4	5
lw $t1, 0x24($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t2, 0xAC($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t3, 0xC8($0)	Capacity	Capacity	Capacity	Capacity	Capacity

b) LRU policy needs 1 bit.

4GB = 2^{32} Bytes

Instruction Address Size = $\log_2(2^{32})$ = 32 bits

Cache Blocks = (2* 4) / (1* 4) = 2 Blocks

Sets = 1 set ;

Byte Offset = 2 bits

LRU = 1 bit

Valid = 1 bit

Tag = 32 - 0 – 0 - 2 = 30 bits

1 + 1 + 30 + 32 = 64 Way 1

1 + 0 + 30 + 32 = 63 Way 2

127 Bit Cache Memory Size

c) 2 AND Gate, 2 Comparator, 1 OR gate , 1 32-Bit 2:1 Mux

4) AMAT = 2.5 Cycles

Time needed = 12.5s