

ELG4137 - Winter 2023

Assignment 2

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Solve the following problems from the textbook.

- 1.17
- 1.19
- 4.3
- 4.10

1.17 Consider the design of a CMOS compound OR-OR-AND-INVERT (OAI22) gate computing $F = \overline{(A+B)} \cdot (C+D)$.

- sketch a transistor-level schematic
 - sketch a stick diagram
 - estimate the area from the stick diagram
 - layout your gate with a CAD tool using unit-sized transistors
 - compare the layout size to the estimated area
- 3 don't have to do*

$$g) F = \overline{(A+B)} \cdot (C+D)$$

Taking the non-invert function we get $(A+B) \cdot (C+D)$

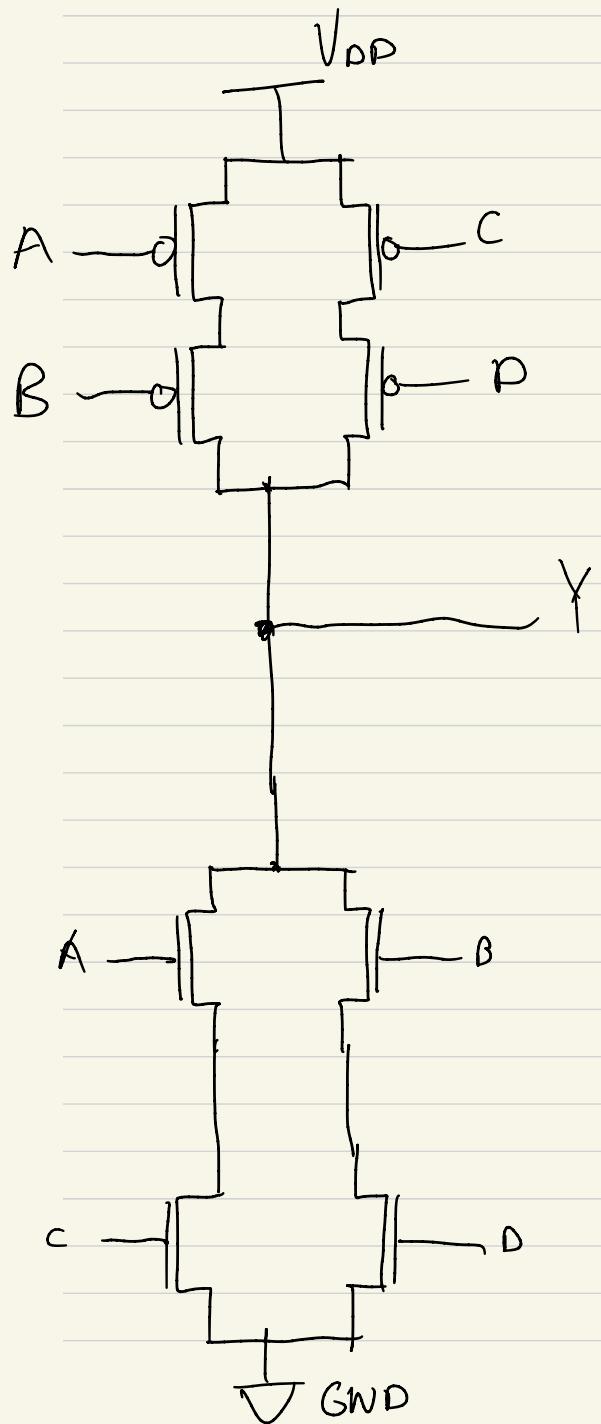
→ Starting with pull-down network (nMOS)

pMOS

AND → series

OR → parallel

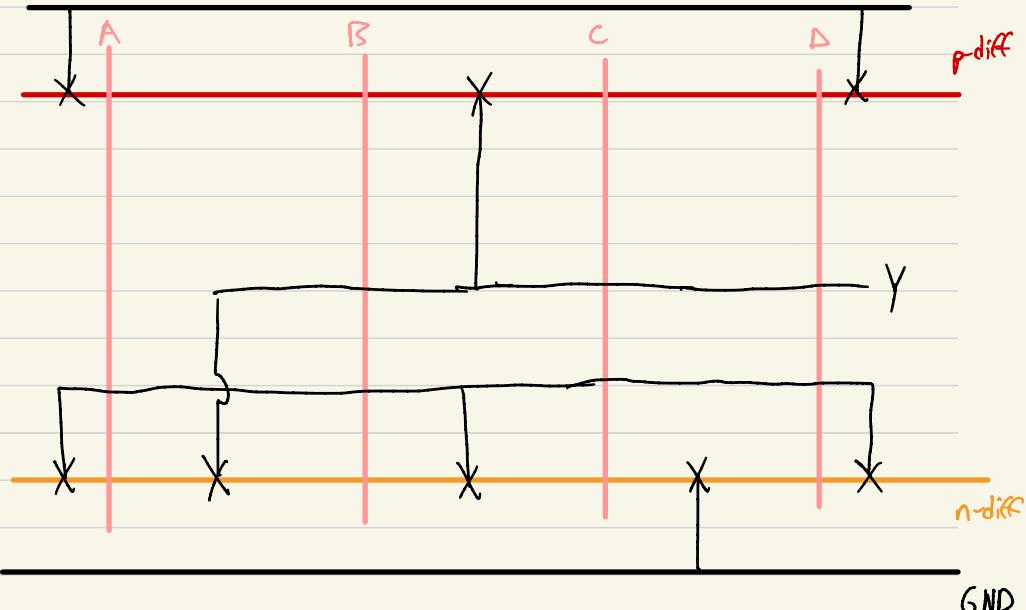
So we have $A \& B$ in parallel } Both or these
in series with one another,
 $C \& D$ in parallel }



* have to check

b)

$\sqrt{D_D}$



GND

c) from the stick diagram, horizontally it has 5 metal rectangles. If each rectangle is 4λ & spacing between them is 4λ

$$5 \times (4\lambda + 4\lambda) = 40\lambda$$

Vertically the diagram has 6 metal rectangles, so if each rectangle is 4λ tall & spacing is 4λ

$$6 \times (4\lambda + 4\lambda) = 48\lambda$$

$$A = W H$$
$$= (40\lambda)(48\lambda)$$

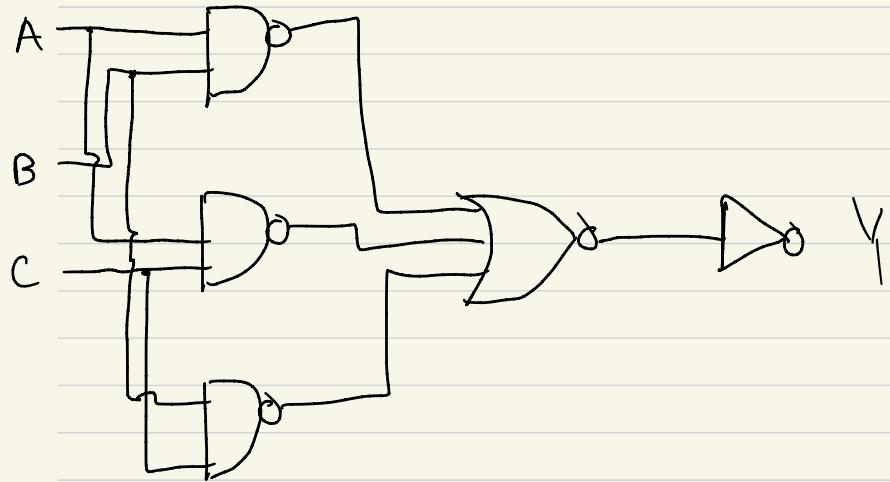
$$A = 1920\lambda^2$$

∴ the area of the stick diagram is $1920\lambda^2$

- 1.19 Design a 3-input minority gate using CMOS NANDs, NORs, and inverters. How many transistors are required? How does this compare to a design from Exercise 1.18(a)?

let $Y = \overline{A(\overline{B+C}) + BC} \dots \textcircled{1}$

CMOS logic gate for equation ①:



for K-input NAND gate, we need K-nMOS transistors
K pMOS transistors.

So for each 2-input NAND gate, we need 4
transistors. 3 NAND gates $\rightarrow 3 \times 4 = 12$ transistors

The same applies for a NOR gate

k-input NOR gate has K-nMOS & K-pMOS transistors. So a 3-input NOR gate has $3+3=6$ transistors

An inverter requires 1pMOS & 1nMOS transistor. So $1+1=2$

$$12+6+2 = 20$$

∴ 20 resistors are required

When we look at the design from exercise

1.18 (a), to implement the minority function

$$Y = \overline{A(B+C)} + BC \text{ less transistors are needed}$$

for nMOS

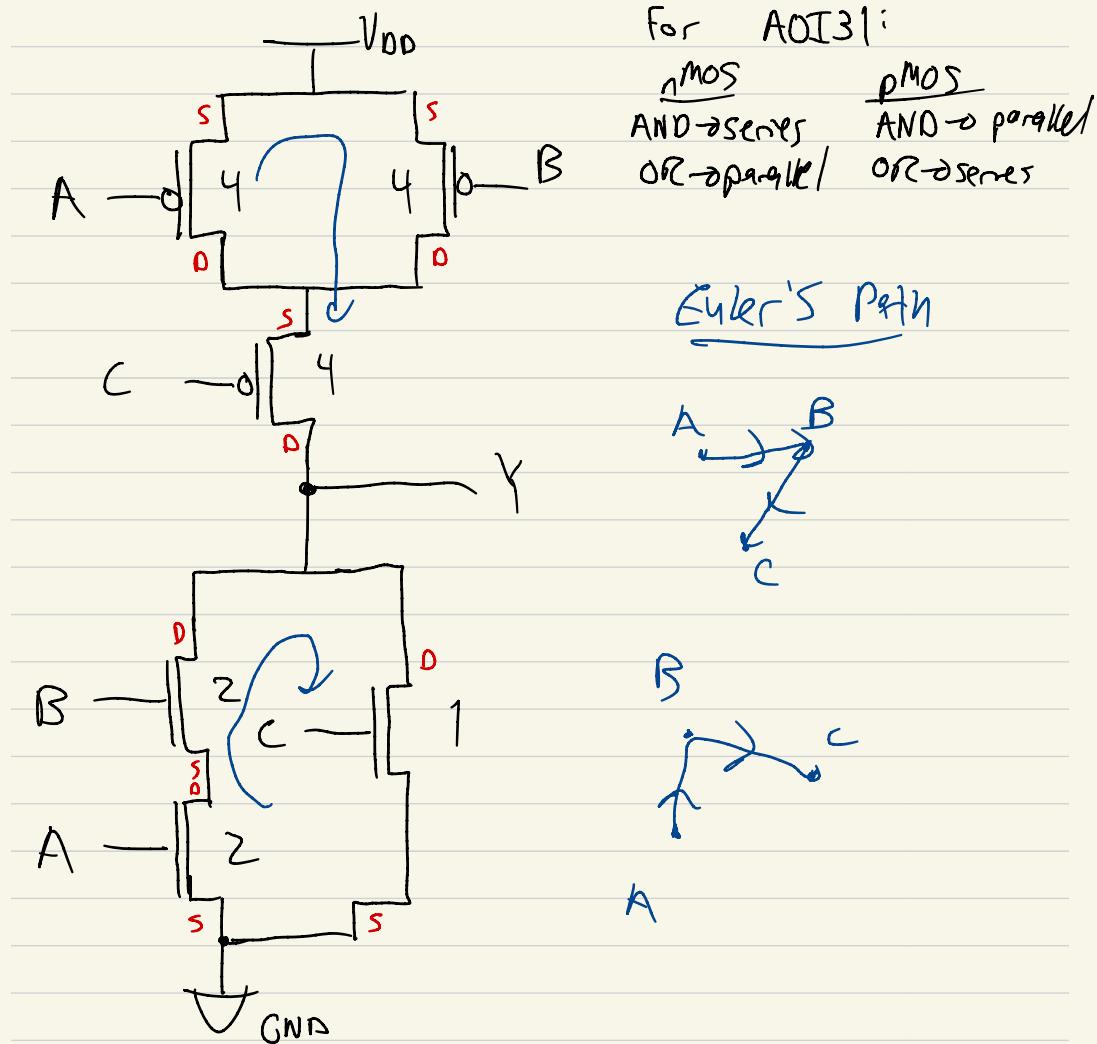
$B+C$ are in parallel ... 2 transistors
 $B \cdot C$ are in series ... 2 transistors
A is in series with $(B+C)$... 1 transistor

If pull-down network has S transistors, then
the pull-up network will also have S.

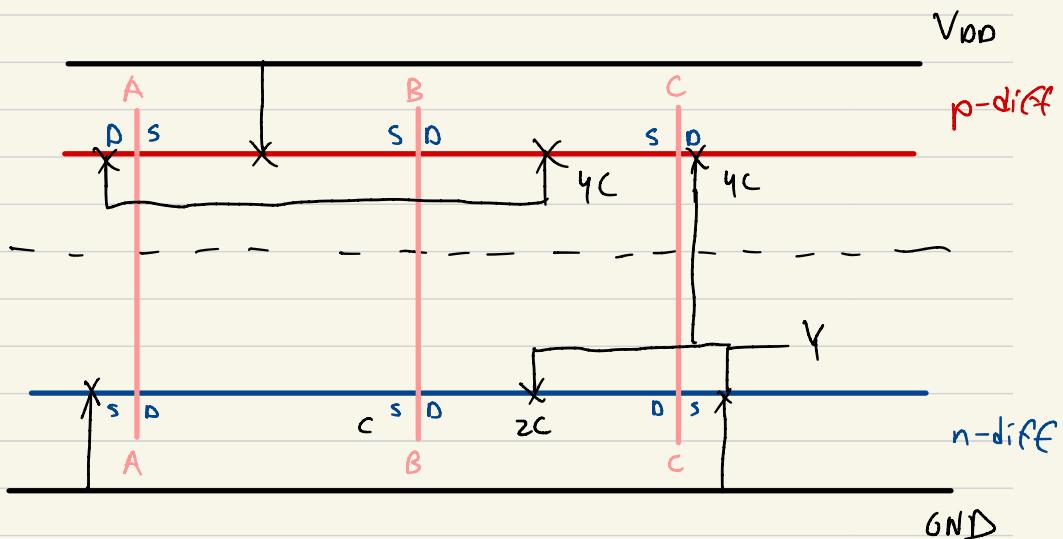
$$S + S = 10 \text{ transistors}$$

Thus, the amount of transistors needed to implement
the logic expression shown in equation ① using
the CMOS compound gate is less than the number
of transistors required to implement the CMOS logic
gate level schematic shown.

- 4.3 Find the rising and falling propagation delays of an unloaded AND-OR-INVERT gate using the Elmore delay model. Estimate the diffusion capacitance based on a stick diagram of the layout.



Stick diagram



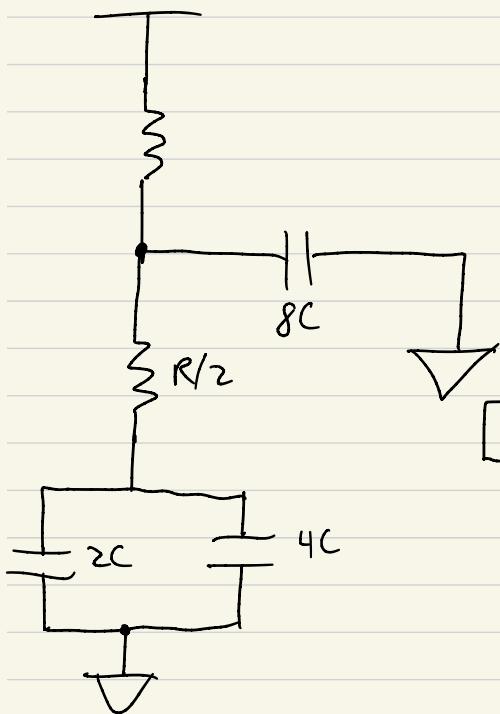
Rising delay

$$t_{pdR} = \sum_i R_{is} C_i$$

$$= \frac{R}{2} 8C + R(2C + 4C)$$

$$= 4RC + 2RC + 4RC$$

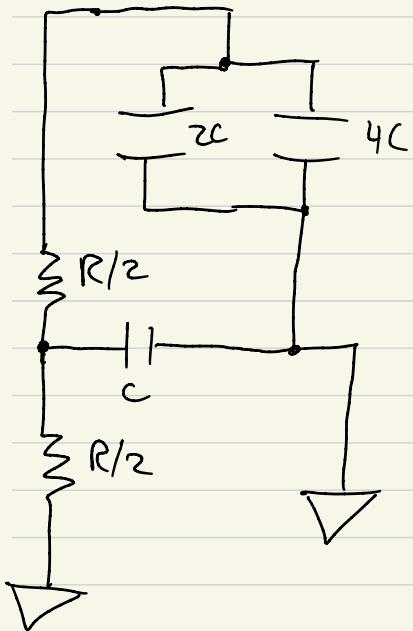
$$\therefore t_{pdR} = 10RC$$



falling delay

$$t_{\text{par}} = \sum_i R_i C_i$$

$$= \frac{R}{2} C + R(2C + 4C)$$



$$= \frac{RC}{2} + 6RC$$

$$= \frac{13}{2} RC$$

∴ the delay is $\frac{13}{2} RC$

- 4.10 Consider the two designs of a 2-input AND gate shown in Figure 4.39. Give an intuitive argument about which will be faster. Back up your argument with a calculation of the path effort, delay, and input capacitances x and y to achieve this delay.

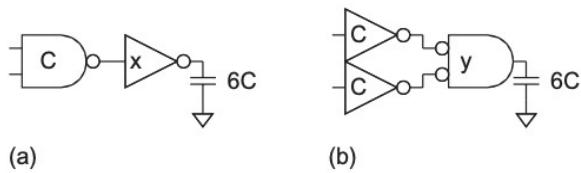


FIGURE 4.39 2-input AND gate

By comparing the two designs of a 2-input AND gate shown in Figure 4.39, circuit (a) should be faster than circuit (b). This is due to the fact that NAND gates require lower logical effort than the NOR.

Calculation to back it up:

In both designs we have $H = 6 \rightarrow H = h_1 h_2 = \frac{x}{c} \frac{6c}{x}$
 $B = 1$
 $P = 1 + 2 = 3$

$$\text{For (a)} \quad G = \left(\frac{4}{3}\right) \times 1 = \frac{4}{3}$$

Since there is no branching, get the path effort by multiplying G & H

$$F = GH = \frac{4}{3} \cdot 6 = 8 \rightarrow F = 8$$

To find the optimal effort f_i for each stage, we take the square root of 8

$$\sqrt{8} = 2.83$$

The parasitic delay for an inverter is 1 K for a NAND gate it is 2. Therefore the total parasitic delay P is 3

Total path delay D :

$$D = P + \sum_{i=1}^2 f_i \\ = 3 + \sum_{i=1}^2 2.83 \\ = 8.66$$

∴ the total path delay is $D = 8.66$

capacitance X =

$$f_1 = h_1 g_1$$

$$2.83 = \frac{x}{C} \cdot \frac{4}{3}$$

$$2.122 = \frac{x}{C}$$

$$\therefore x = 2.122 C$$

Now let's calculate the electrical effort for the circuit with the NOR gate.

$$H = h_1 h_2 = \frac{y}{c} \frac{6c}{y}$$

$$= 6$$

$$G = g_1 g_2 = \left(\frac{5}{3}\right) 1 = \left(\frac{5}{3}\right)$$

Since there is also no branching in this design as well,

the path effort is $f = GH$

$$= \frac{5}{3} 6$$

$$= \frac{30}{3}$$

$$f = 10$$

$$\text{since } f = 10, f_i = \sqrt{10} = 3.16$$

We know the parasitic delay for an inverter is 1 μ s for a NOR gate it is 2.

$$\text{Thus, } P = 1 + 2 = 3$$

$$\text{Total path delay } D = P + \sum_{i=1}^2 f_i$$

$$= 3 + \sum_{i=1}^2 3.16 \\ = 3 + 2(3.16)$$

$$\boxed{\therefore D = 9.32}$$

$$\rightarrow f_i = h_i g_i$$

$$3.16 = \frac{y}{c} \mid$$

$$3.16 = \frac{y}{c}$$

$$y = 3.16c \rightarrow \therefore \text{the stage effort } y = 3.16c$$

when we compare the total path delay,
 $8.66 < 9.32$. Thus this confirms that design
(a) is faster than design (b), hence
backing up my argument