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ELG4137 Winter 2023 Assignment 1

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The following document indicates the size of the transistors (W/L) and the reasoning behind why they were used in the NAND logic gate design.

Gate size - defined as...

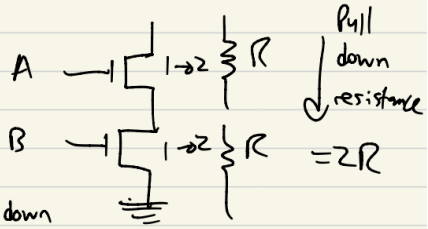
$$\text{Gate size} = \frac{R}{\text{largest fall or largest rise resistance}}$$

if Gate size = 1

Then the sizes of the Nmos & Pmos transistors are selected to ensure that the largest rise & fall resistance is equal to R

→ according to the formula for Gate size, we need to increase transistor size from 1 to 2. Doing so will change the pull down resistance to R/2 & R/2. R/2 + R/2 = R → ∴ the formula for gate size is satisfied

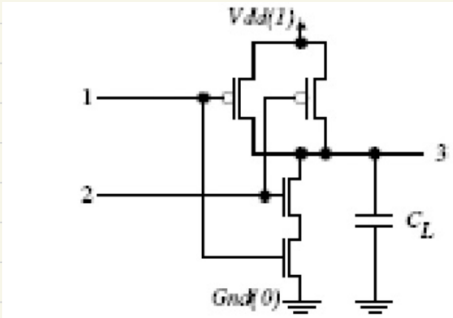
designed to be equal



is satisfied

Calculating W/L ratio of a transistor

CMOS NAND Gate



Va	Vb	Vout
1	2	3
0	0	1
0	1	1
1	0	1
1	1	0

→ we have 2 pmos transistors in parallel & 2 nmos transistors in series

$\left(\frac{W}{L}\right)_{eff}$ of nmos $= \frac{1}{1}$

→ 2 nmos transistors in series (consider 2 ratios)

$$\frac{1}{1} = \frac{1}{\frac{L}{W} + \frac{L}{W}}$$

$$\frac{1}{1} = \frac{1}{\frac{2L}{W}}$$

$$\frac{1}{1} = \frac{W}{2L}$$

$$\frac{1}{1} = \frac{W}{L} \cdot \frac{1}{2}$$

$$\frac{\frac{1}{1}}{\frac{1}{2}} = \frac{W}{L} \rightarrow \frac{1}{1} \times 2 = \frac{W}{L}$$

→ $\boxed{\frac{2}{1} = \frac{W}{L}}$ ∴ the ratio of the $\frac{W}{L}$ for the nmos transistor is $\frac{2}{1}$

For PMOS

From before, we know that,

$$\frac{2}{1} = \left(\frac{W}{L}\right)_{eff}$$

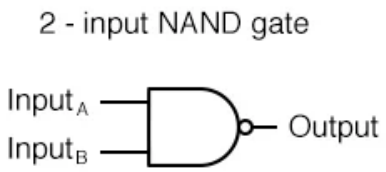
→ pmos transistors in parallel

$$\frac{2}{1} = \frac{1}{\frac{L}{W}} \rightarrow \frac{2}{1} = \frac{W}{L}$$ → ∴ the ratio $\frac{W}{L}$ for the pmos transistor is $\frac{2}{1}$

Since we now know the transistor $\frac{W}{L}$ ratio's, we can implement certain sizes into virtuoso design.

→ since smaller transistor sizes offer several benefits such as improved performance (faster switching speeds & lower power consumption), I have chosen transistor width of 200 nm & length of 100 nm

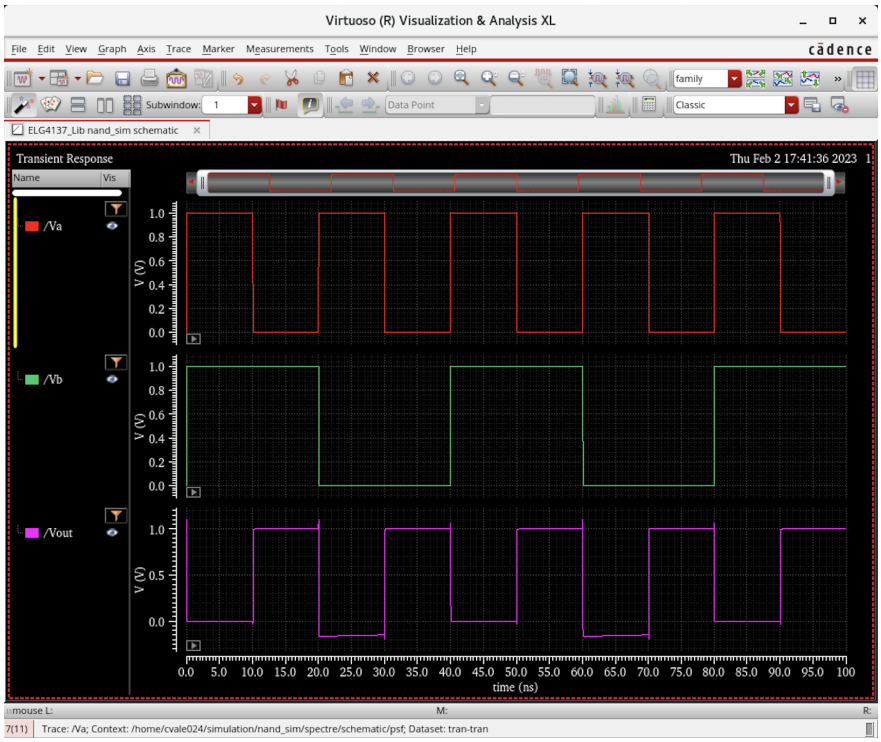
To observe the different ways in which the output of the gate rises to 1 or falls to 0, let's take a look at a NAND2 logical gate truth table



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

When both inputs are 0, the output is 1. When either input has a value of 1, the output is also 1. Lastly, when both inputs are 1, the output is 0.

Now let's take a look at our testbench simulation for input values 0 or Vdd, for comparison.



From this simulation we can see that when Va = 0, Vb =0, and Vout = 1

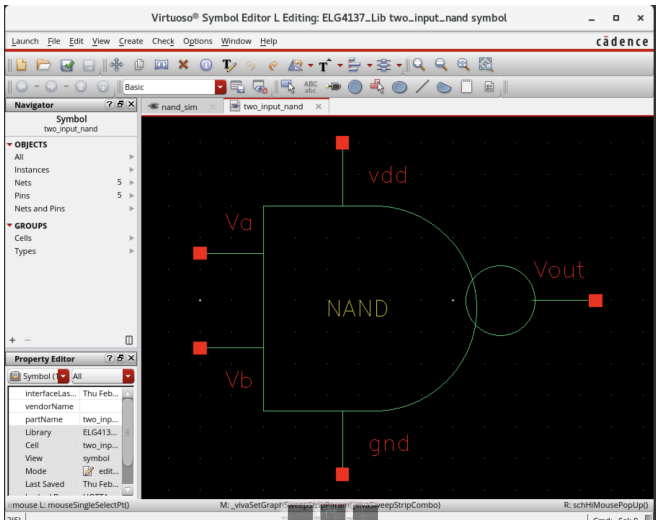
When Va = 0, Vb =1, and Vout = 1

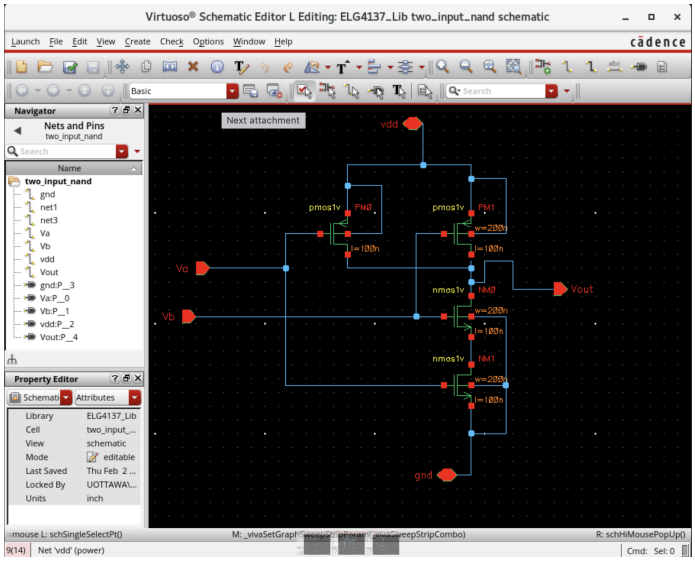
When Va =1, Vb =0, and Vout =0. This is incorrect as Vout should be 1.

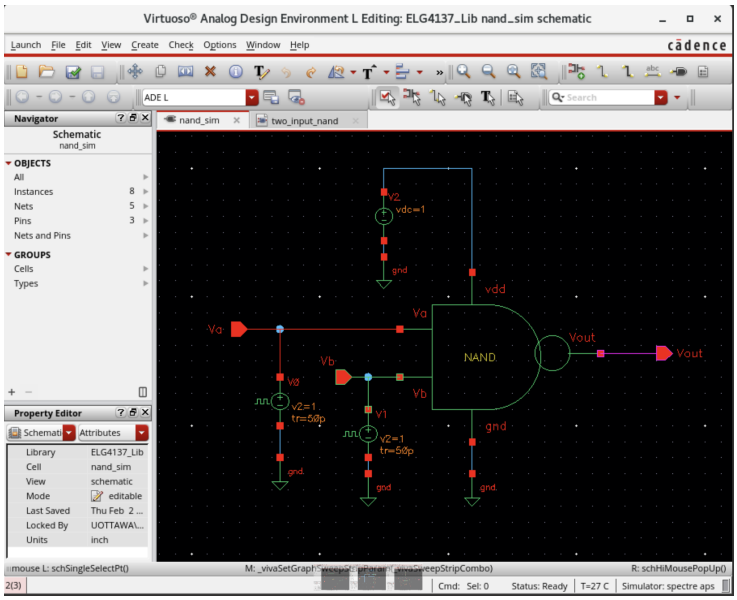
When Va =1, Vb =1, and Vout = 0.

After comparing the simulation to the NAND truth table, all of the cases are correct except for one. Therefore, the gate is non-conclusive and the gate cannot be verified as a properly operating NAND gate.

The virtuoso schematic files have been added to the zipped folder this pdf document is in. Below are just some screenshots.



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Navigator
Schematic
nand_sim
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Instances 8
Nets 5
Pins 3
Nets and Pins
GROUPS
Cells
Types
Property Editor
Schemati
Attributes
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Cell nand_sim
View schematic
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two_input_nand
V2
vdc=1
gnd
vdd
Va
Vb
NAND
Vout
V0
v2=1
tr=50p
V1
gnd
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R: schHiMousePopUp()
Cmd: Sel: 0
Status: Ready
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Simulator: spectre aps