Question 1

A. 209_{dec} to binary

209/2 = 104 r 1
104/2 = 52 r 0
52/2 = 26 r 0
26/2 = 13 r 0
13/2 = 6 r 1
6/2 = 3 r 0
3/2 = 1 r 1
1/2 = 0 r 1

$209_{10} = 11010001_2$

1101 0001

B. -117 in signed magnitude

first bit is 1 because negative

117/2 = 58 r 1
58/2 = 29 r 0
29/2 = 14 r 1
14/2 = 7 r 0
7/2 = 3 r 1
3/2 = 1 r 1
1/2 = 0 r 1

1110101, in signed magnitude is

1111 0101

C. -117 in two complement

117 in 8 bits is 0111 0101

bits slipped 1000 1010

$+$ 0000 0001

1000 1011

1000 1011

D 4.75

4 in 4bit binary = 0100

2^{-1} 2^{-2} 2^{-3} 2^{-4}

0.5 0.25 0

0.75 = 1100

therefore 4.75 = **0100 1100**

E. Fish in ascii

		Parity bit
F = 01000110	odd	1
i = 01101001	even	0
s = 01110011	odd	1
h = 01101000	odd	1

F i s h

1100 0110 0110 1001 1011 0011 1110 1000

F. F7 in binary

F in binary is 1111 (15)

7 in binary is 0111

2^2 2^1 2^0

4 + 2 + 1

F7 = 1111 0111

G) 123_8 to base2

A
1 = 001
2 = 010
3 = 011

combined this gives us 001010011

as this is 9 digits we can remove a leading 0 to give us

01010011
or 0101 0011

Question 2

A) Truth table

M	N	O	BUY
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

B) KMap

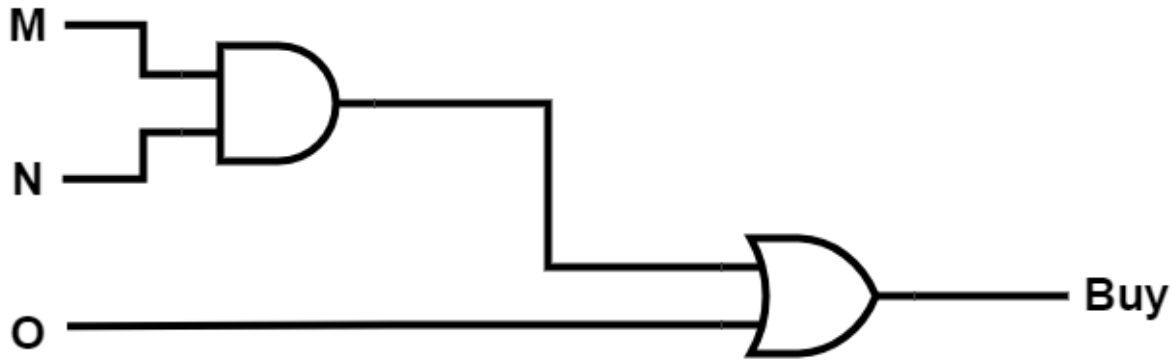
M \ NO	00	01	11	10
00	0	1	1	0
01	0	1	1	1

C) Simplify Expression

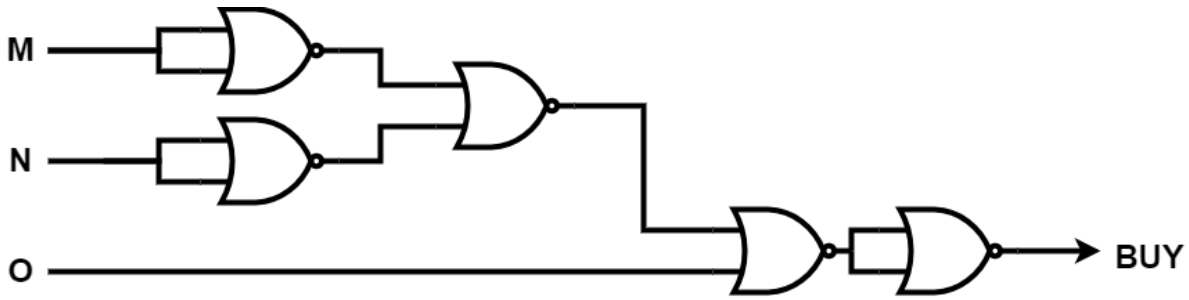
The first group is O, the second group is M and N.

Therefore our simplified expression is O + MN

D) Implement circuit diagram



E) Reimplement with only NOR gates



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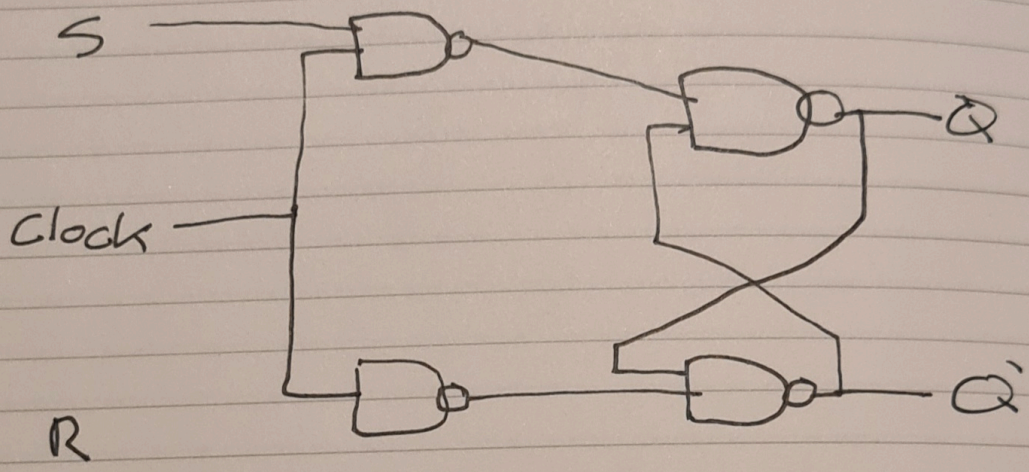


Clock	R	S	Q
0	-	-	Previous
1	0	0	Previous
1	0	1	1
1	1	0	0
1	1	1	Wont work

3) Part 2

A clocked SR flip flop will only update its output when the clock signal is set to 1, this is because the first set of NAND gates will always output a 1 unless both inputs are a 1. By setting S to 1 and Clock to 1, Q is set to 1. By setting R to 1 and clock to 1, Q is reset to 0.

4

part 1

x	y	z	parity
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

x \ yz

x \ yz	00	01	11	10
0		1		1
1	1		1	

cant be simplified

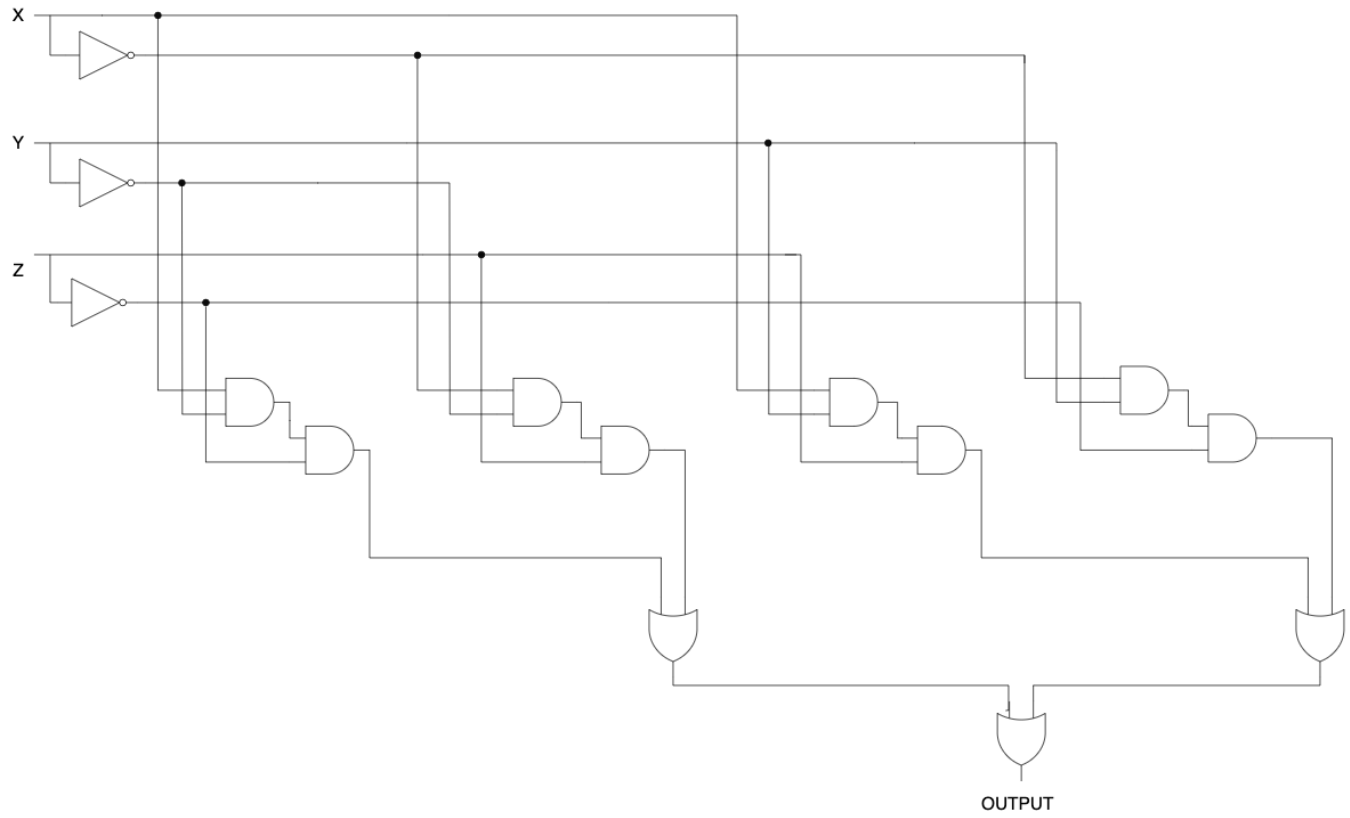
Therefore

$xy\bar{z} + \bar{x}\bar{y}z + xyz + \bar{x}y\bar{z}$

x

y

z



The parity bit generator table given is for an even parity bit system, this means if there is an odd number of 1s in a sequence then the parity bit must also be a 1. The circuit above does this by giving each input two outputs, its regular output and its complement. These are then fed into a series of AND gates which check how many 1s are in the input.

The first three sets of AND gates check that there is only one 1 in the sequence, the final set of and gates check to see if there are three 1s. Finally each of these sets of and gates are combined with multiple OR gates.