

# Parallel & Distributed Computing: Lecture 5

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Center

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# Concepts and Terminology

- 1 General concepts
- 2 Limits and Costs of Parallel Programming
- 3 Sequential implementation of domain integration of polynomials

# General concepts

# von Neumann Computer Architecture

- Named after the Hungarian mathematician/genius **John von Neumann** who first authored the general requirements for an electronic computer in his 1945 papers.



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- Since then, virtually all computers have followed this basic design



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- Four main components:

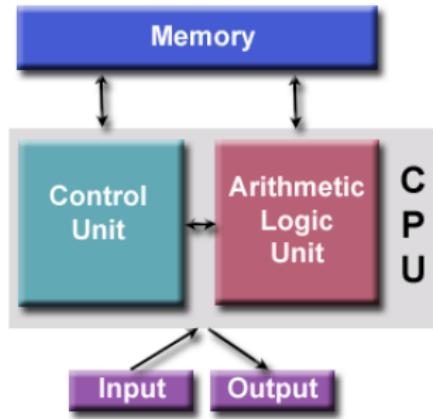


Figure 2: von Neumann  
Architecture

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- Four main components:
  - Memory

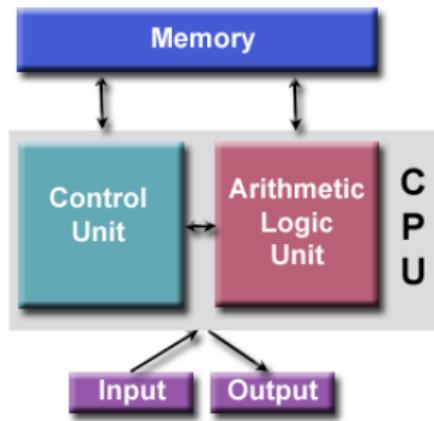


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- Four main components:

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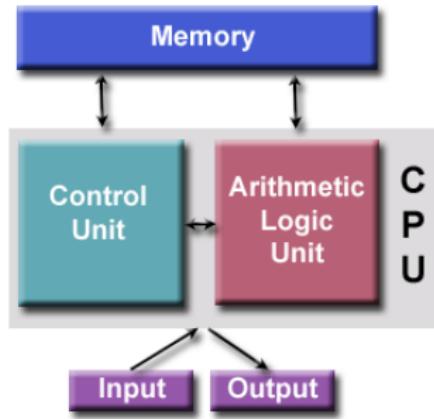


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- Four main components:

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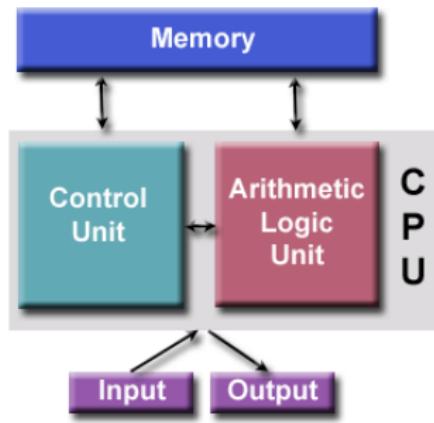


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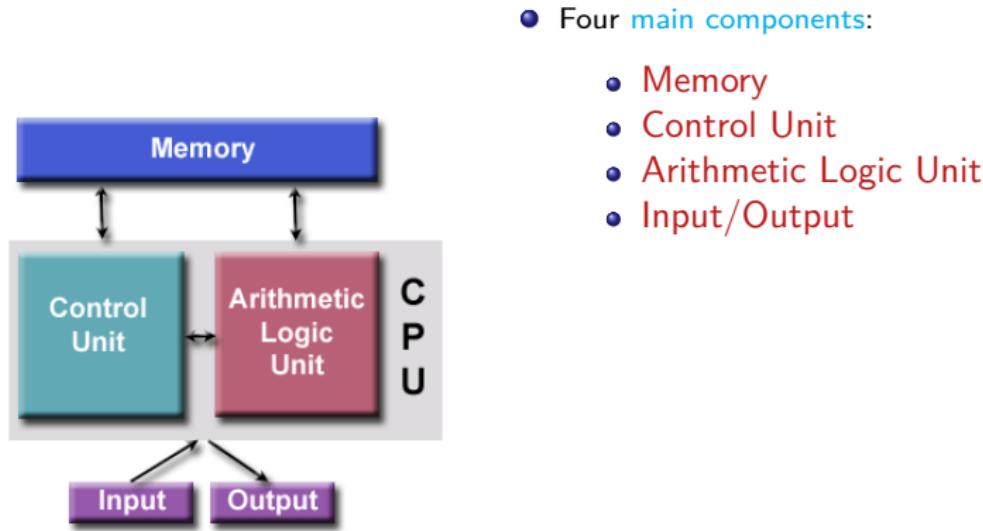
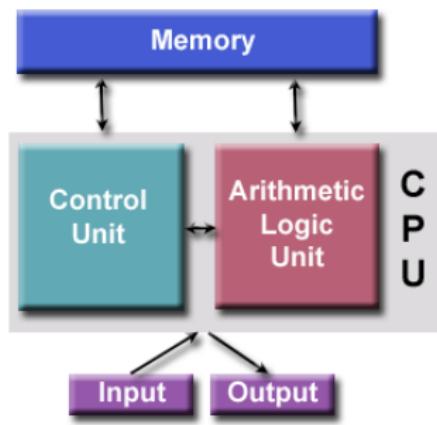


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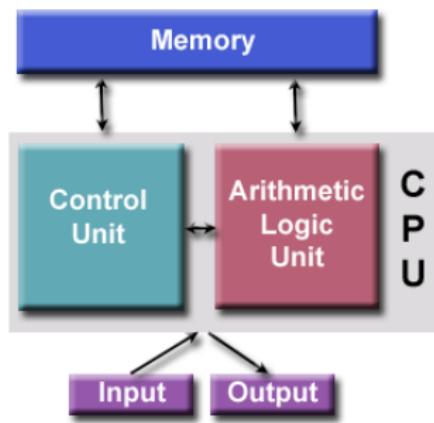
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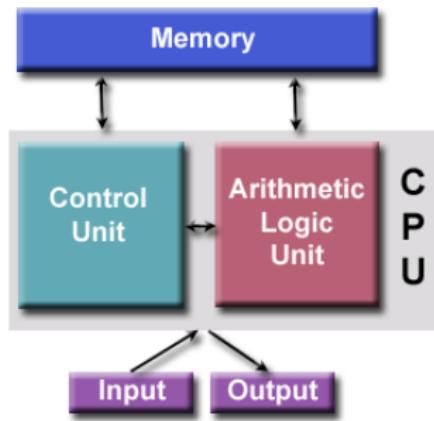
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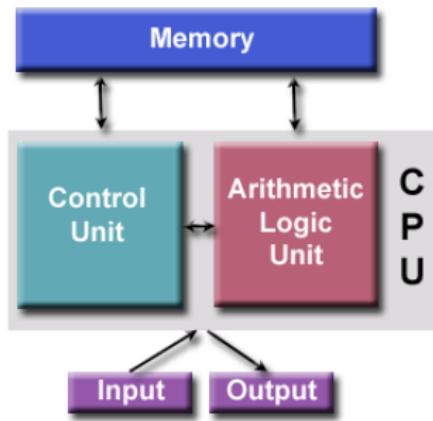


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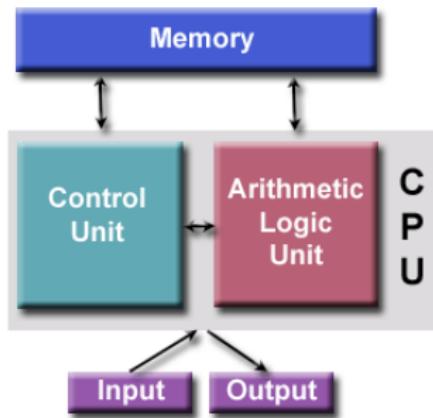


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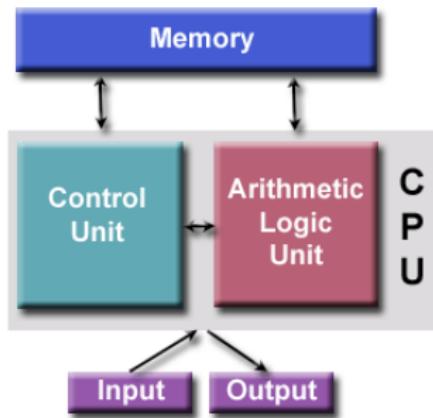


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- Arithmetic Unit performs basic arithmetic operations
- Input/Output is the interface to the human operator

# Flynn's Classical Taxonomy

- There are different ways to classify parallel computers. Examples available [HERE](#).

S I S D	S I M D
Single Instruction stream Single Data stream	Single Instruction stream Multiple Data stream
M I S D	M I M D
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- Flynn's taxonomy distinguishes multi-processor computer architectures according to how they can be classified along the two independent dimensions of **Instruction Stream** and **Data Stream**.
- Each dimension can have only two possible states: **Single** or **Multiple**.

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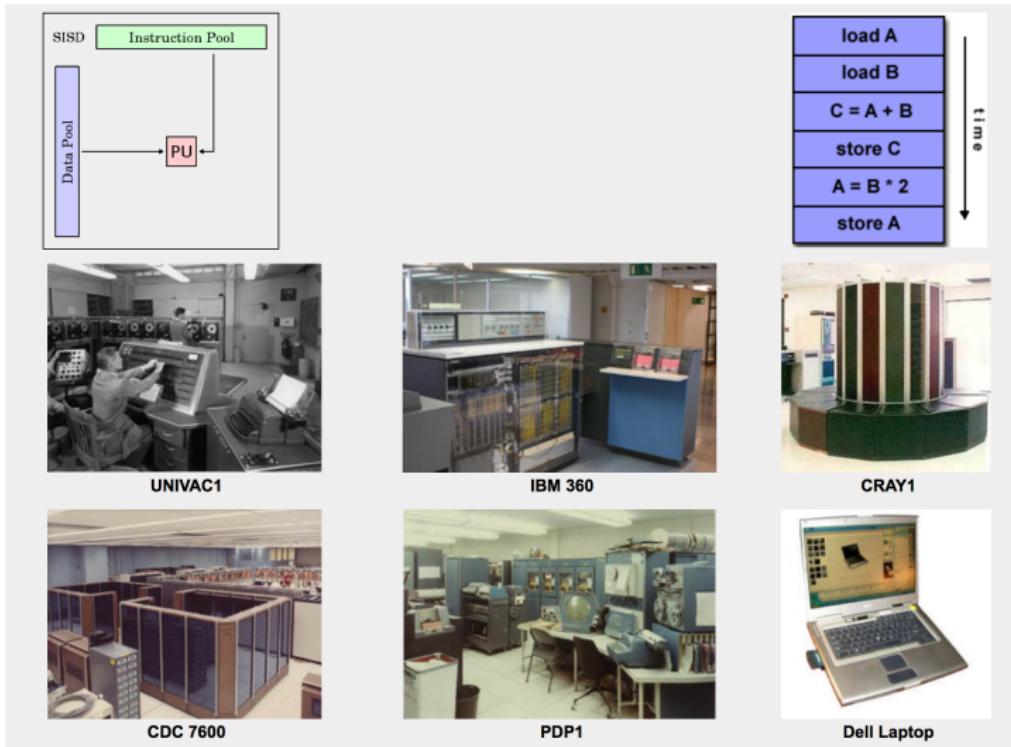


Figure 4. Single Instruction, Single Data (SISD)

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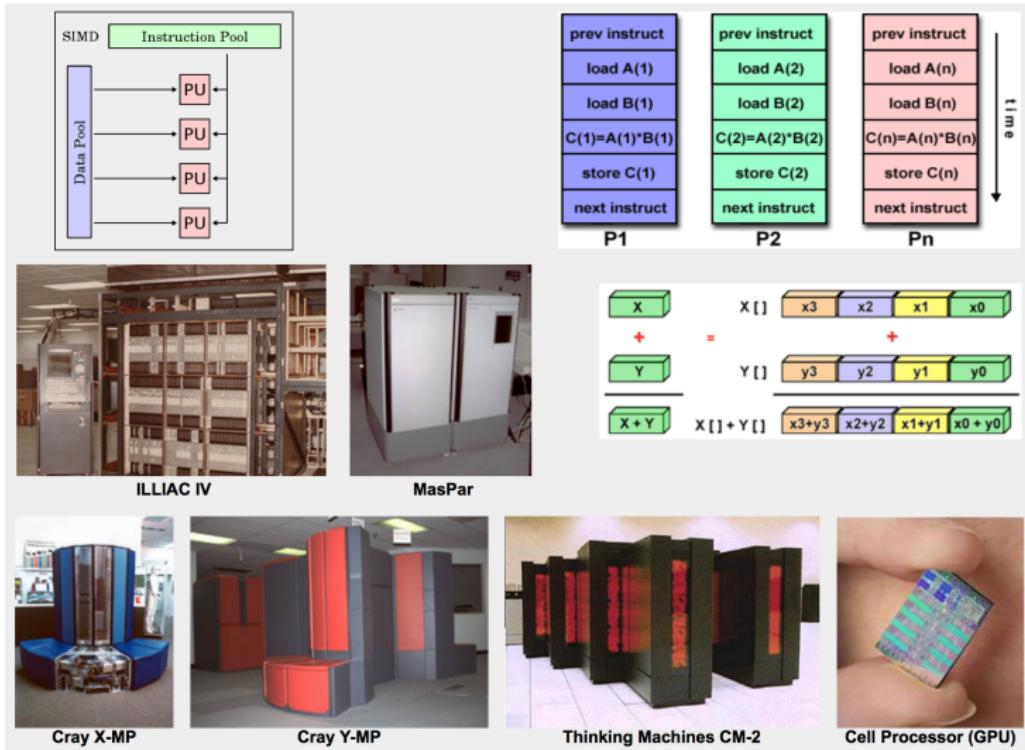
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- **Most modern computers**, particularly those with **graphics processor units (GPUs)** use SIMD

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  - **multiple cryptography algorithms** attempting to crack a single coded message.

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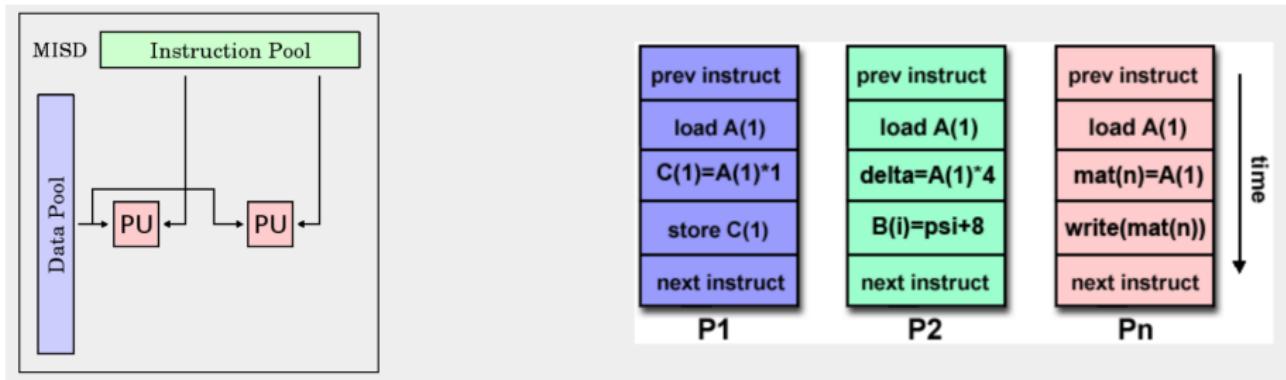


Figure 6: Multiple Instruction, Single Data (MISD)

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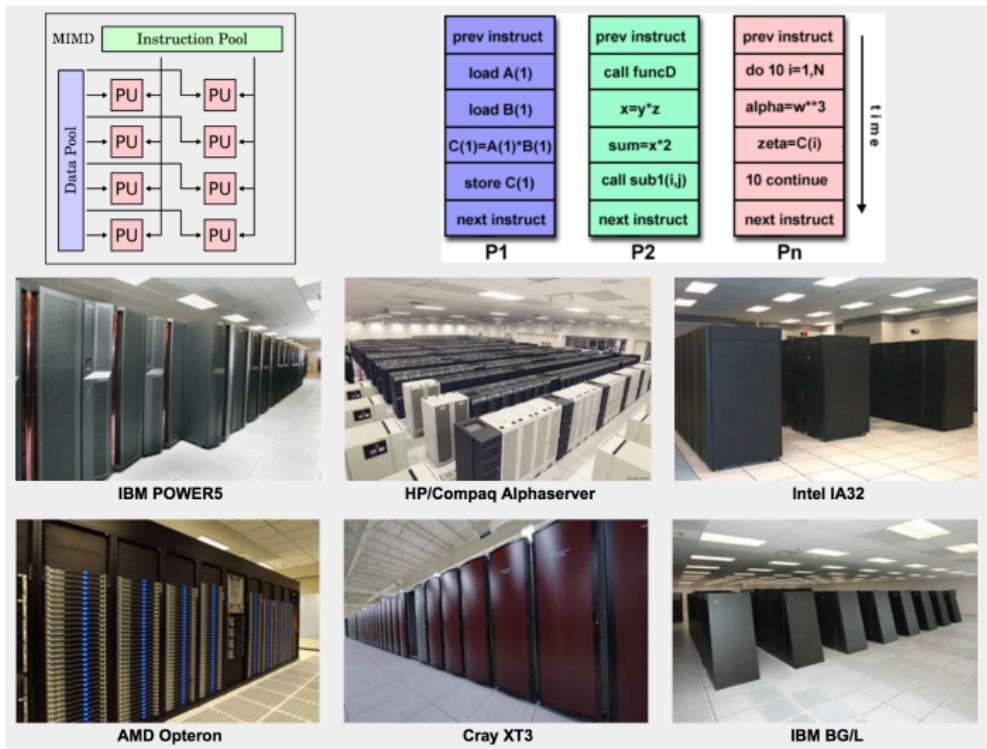
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- Note: many MIMD architectures also include **SIMD execution sub-components**

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**Supercomputing / High Performance Computing (HPC)** Using the world's fastest and largest computers to solve large problems.

**Node** A standalone “computer in a box”. Usually comprised of multiple CPUs/processors/cores, memory, network interfaces, etc.  
Nodes are networked together to produce a supercomputer.

# Some General Parallel Terminology

CPU / Socket / Processor / Core This varies, depending upon who you talk to.

In the past, a CPU (Central Processing Unit) was a singular execution component for a computer.

Then, multiple CPUs were incorporated into a node.

Then, individual CPUs were subdivided into multiple “cores”, each being a unique execution unit. CPUs with multiple cores are sometimes called “sockets” - vendor dependent.

The result is a node with multiple CPUs, each containing multiple cores. The nomenclature is confused at times.

Wonder why?

# Some General Parallel Terminology



Supercomputer - each blue light is a node

Node - standalone  
Von Neumann computer

CPU / Processor / Socket - each has multiple cores / processors.

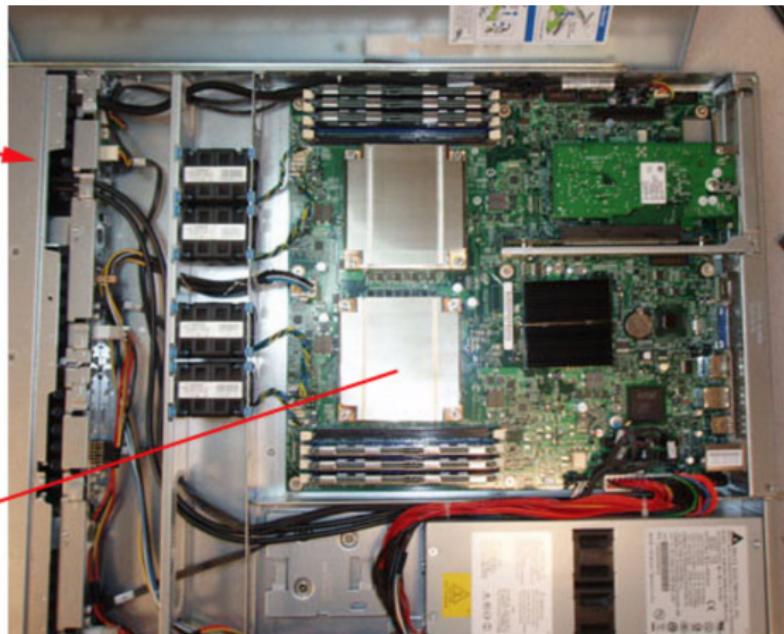
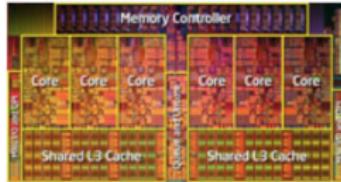


Figure 8: CPU / Socket / Processor / Core

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A task is typically a program or **program-like set of instructions** that is executed by a processor. A **parallel program** consists of **multiple tasks** running on **multiple processors**.

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**Pipelining** Breaking a task into steps performed by different processor units, **with inputs streaming** through, much like an assembly line; **a type of parallel computing**.

# Some General Parallel Terminology

**Shared Memory** From a strictly hardware point of view, describes a computer architecture where **all processors** have direct (usually bus based) access to **common physical memory**. In a programming sense, it describes a model where **parallel tasks** all have the **same “picture” of memory** and can directly address and access the same logical memory locations **regardless of where** the physical memory actually exists.

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**Symmetric Multi-Processor (SMP)** Shared memory hardware architecture where **multiple processors share a single address space** and have **equal access to all resources**.

# Some General Parallel Terminology

**Distributed Memory** In hardware, refers to network based memory access for physical memory that is not common.

As a programming model, tasks can only logically “see” local machine memory and must use communications to access memory on other machines where other tasks are executing.

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**Communications** Parallel tasks typically **need to exchange data**.

There are several ways this can be accomplished, such as through a **shared memory bus** or over a **network**, however the actual event of data exchange is commonly referred to as **communications** regardless of the method employed.

# Some General Parallel Terminology

**Synchronization** The coordination of parallel tasks in real time, very often associated with communications.

Often implemented by establishing a synchronization point within an application where a task may not proceed further until another task(s) reaches the same or logically equivalent point.

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- **Coarse:** relatively large amounts of computational work are done between communication events
- **Fine:** relatively small amounts of computational work are done between communication events

# Some General Parallel Terminology

**Observed Speedup** Observed speedup of a code which has been parallelized, defined as:

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**Observed Speedup** Observed speedup of a code which has been parallelized, defined as:

$$\frac{\text{wall-clock time of serial execution}}{\text{wall-clock time of parallel execution}}$$

One of the simplest and most widely used indicators for a parallel program's performance.

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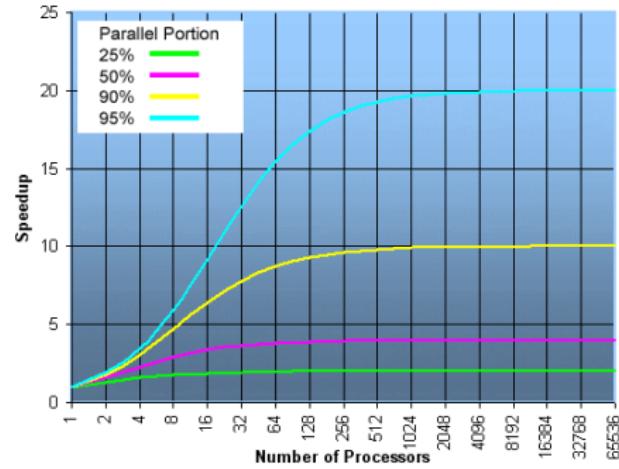
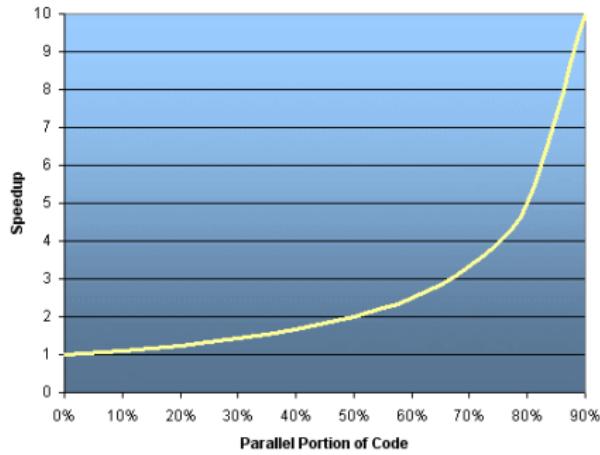
- Hardware - particularly memory-cpu bandwidths and network communication properties
- Application algorithm
- Parallel overhead related
- Characteristics of your specific application

# Limits and Costs of Parallel Programming

# Amdahl's Law

**Amdahl's Law** states that potential program speedup is defined by the fraction of code ( $P$ ) that can be parallelized:

$$\text{speedup} = \frac{1}{1 - P}$$

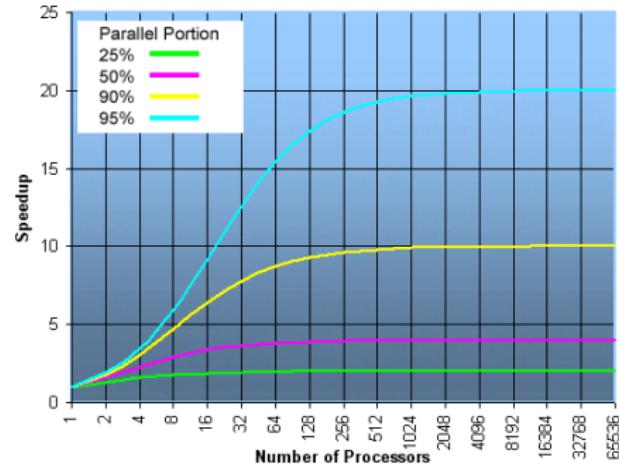
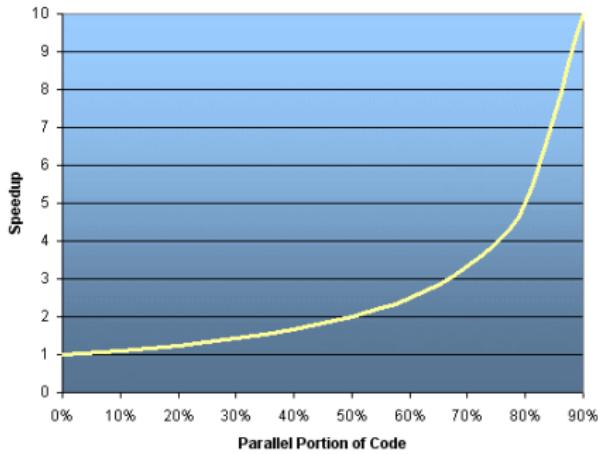


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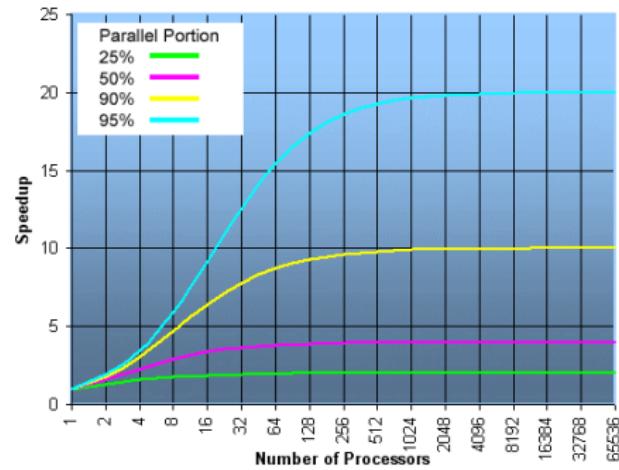
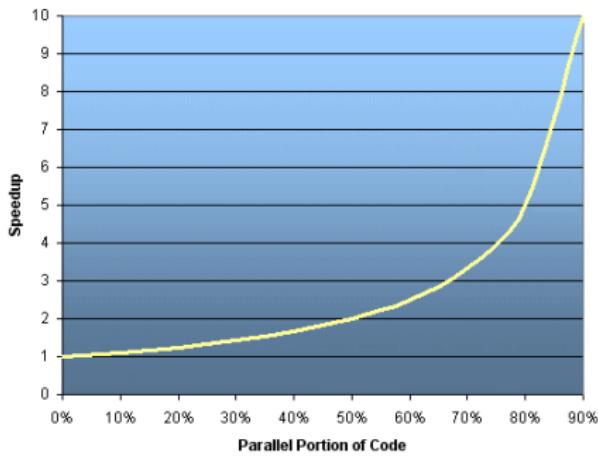


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- If all code is parallelized,  $P = 1$  and the speedup =  $\infty$  (in theory).
- If 50% of code can be parallelized,  $\max(\text{speedup}) = 2$ , meaning the code may run twice as fast.

# Amdahl's Law

Introducing the number  $N$  of processors performing the parallel fraction of work, the relationship can be modeled by:

$$\text{speedup} = \frac{1}{\frac{P}{N} + S}$$

where  $P$  = parallel fraction,  $N$  = number of processors and  $S$  = serial fraction.

# Amdahl's Law

It soon becomes obvious that **there are limits** to the scalability of parallelism.

For example:

N	speedup		
	P = .50	P = .90	P = .99
10	1.82	5.26	9.17
100	1.98	9.17	50.25
1,000	1.99	9.91	90.99
10,000	1.99	9.91	99.02
100,000	1.99	9.99	99.90

Figure 9: Speedup table

## Amdahl's Law

However, certain problems demonstrate increased performance by increasing the problem size. For example:

2D Grid Calculations	85 seconds	85%
Serial fraction	15 seconds	15%

We can increase the problem size by doubling the grid dimensions and halving the time step. This results in four times the number of grid points and twice the number of time steps. The timings then look like:

2D Grid Calculations	680 seconds	97.84%
Serial fraction	15 seconds	2.16%

Problems that increase the percentage of parallel time with their size are more scalable than problems with a fixed percentage of parallel time.

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- The costs of complexity are measured in programmer time in virtually every aspect of the software development cycle:
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  - Maintenance
- Adhering to “good” software development practices is essential when working with parallel applications - especially if somebody besides you will have to work with the software.

# Portability

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- Hardware architectures are characteristically highly variable and can affect portability.

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- For short running parallel programs, there can actually be a decrease in performance compared to a similar serial implementation. The overhead costs associated with setting up the parallel environment, task creation, communications and task termination can comprise a significant portion of the total execution time for short runs.

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  - Communications network bandwidth
  - Amount of memory available on any given machine or set of machines
  - Processor clock speed
- Parallel support libraries and subsystems software can limit scalability independent of your application.

# Sequential implementation of domain integration of polynomials

# Domain integration of polynomials

Finite formulae for evaluation of integrals:

$$II_S \equiv \iint_S f(\mathbf{p}) dS, \quad III_P \equiv \iiint_P f(\mathbf{p}) dV, \quad (1)$$

The integrating function is a trivariate polynomial

$$f(\mathbf{p}) = \sum_{\alpha=0}^n \sum_{\beta=0}^m \sum_{\gamma=0}^p a_{\alpha\beta\gamma} x^\alpha y^\beta z^\gamma,$$

where  $\alpha, \beta, \gamma$  are non-negative integers. Since the extension to  $f(\mathbf{p})$  is straightforward, we focus on integrals of monomials:

$$II_S^{\alpha\beta\gamma} \equiv \iint_S x^\alpha y^\beta z^\gamma dS, \quad III_P^{\alpha\beta\gamma} \equiv \iiint_P x^\alpha y^\beta z^\gamma dV. \quad (2)$$

From Cattani, Paoluzzi. "Boundary integration over linear polyhedra", CAD, 1990

# Basic integration functions

structure product over a polyhedral surface  $S$ , open or closed, is a summation of structure products (3) over the 2-simplices of a triangulation  $K_2$  of  $S$ :

$$II_S^{\alpha\beta\gamma} = \iint_S x^\alpha y^\beta z^\gamma dS = \sum_{\tau \in K_2} II_\tau^{\alpha\beta\gamma}$$

```

function II(P, alpha, beta, gamma, signedInt=false)
    w = 0
    V, FV = P
    if typeof(P) == PyCall.PyObject
        if typeof(V) == Array{Any,2}
            V = V'
        end
        if typeof(FV) == Array{Any,2}
            FV = [FV[k,:] for k=1:size(FV,1)]
            FV = FV+1
        end
    end
    if typeof(FV) == Array{Int64,2}
        FV = [FV[:,k] for k=1:size(FV,2)]
    end
    for i=1:length(FV)
        tau = hcat([V[:,v] for v in FV[i]]...)
        if size(tau,2) == 3
            term = TT(tau, alpha, beta, gamma, signedInt)
            if signedInt
                w += term
            else
                w += abs(term)
            end
        elseif size(tau,2) > 3
            println("ERROR: FV[$(i)] is not a triangle")
        else
            println("ERROR: FV[$(i)] is degenerate")
        end
    end
    return w
end

```

# Basic integration functions

$$III_P^{\alpha\beta\gamma} = \iiint_P x^\alpha y^\beta z^\gamma dx dy dz$$

$$= \frac{1}{\alpha+1} \sum_{\tau \in K_2} \left[ \frac{(\mathbf{a} \times \mathbf{b})_x}{|\mathbf{a} \times \mathbf{b}|} \right]_\tau II_\tau^{\alpha+1, \beta, \gamma}$$

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            FV = FV+1
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    end
    for i=1:length(FV)
        tau = hcat([V[:,v] for v in FV[i]]...)
        vo,va,vb = tau[:,1],tau[:,2],tau[:,3]
        a = va - vo
        b = vb - vo
        c = cross(a,b)
        w += c[1]/vecnorm(c) * TT(tau, alpha+1, beta, gamma)
    end
    return w/(alpha + 1)
end

```

# Basic integration functions

$$\begin{aligned}
 II_{\tau}^{\alpha\beta\gamma} &= |a \times b| \sum_{h=0}^{\alpha} \binom{\alpha}{h} x_o^{\alpha-h} \cdot \\
 &\quad \cdot \sum_{k=0}^{\beta} \binom{\beta}{k} y_o^{\beta-k} \cdot \\
 &\quad \cdot \sum_{m=0}^{\gamma} \binom{\gamma}{m} z_o^{\gamma-m} \cdot \\
 &\quad \cdot \sum_{i=0}^h \binom{h}{i} a_x^{h-i} b_x^i \cdot \\
 &\quad \cdot \sum_{j=0}^k \binom{k}{j} a_y^{k-j} b_y^j \cdot \\
 &\quad \cdot \sum_{l=0}^m \binom{m}{l} a_z^{m-l} b_z^l \cdot \\
 &\quad \cdot II^{\mu\nu}
 \end{aligned}$$

```

function TT(tau::Array{Float64,2}, alpha, beta, gamma, signedInt=false)
    vo,va,vb = tau[:,1],tau[:,2],tau[:,3]
    a = va - vo
    b = vb - vo
    s1 = 0.0
    for h=0:alpha
        for k=0:beta
            for m=0:gamma
                s2 = 0.0
                for i=0:h
                    s3 = 0.0
                    for j=0:k
                        s4 = 0.0
                        for l=0:m
                            s4 += binomial(m,l) * a[3]^(m-l) * b[3]^l *
                                M( h+k+m-i-j-l, i+j+l )
                        end
                        s3 += binomial(k,j) * a[2]^(k-j) * b[2]^j * s4
                    end
                    s2 += binomial(h,i) * a[1]^(h-i) * b[1]^i * s3;
                end
                s1 += binomial(alpha,h) * binomial(beta,k) * binomial(gamma,m) *
                    vo[1]^(alpha-h) * vo[2]^(beta-k) * vo[3]^(gamma-m) * s2
            end
        end
    end
    c = cross(a,b)
    if signedInt == true
        return s1 * vecnorm(c) * sign(c[3])
    else return s1 * vecnorm(c) end
end

```

# Basic integration functions

$$II^{\alpha\beta} = \frac{1}{\alpha+1} \sum_{h=0}^{\alpha+1} \binom{\alpha+1}{h} \frac{(-1)^h}{h+\beta+1},$$

```
function M(alpha, beta)
    a = 0
    for l=1:(alpha + 2)
        a += binomial(alpha+1,l) * (-1)^l/(l+beta+1)
    end
    return a/(alpha + 1)
end
```