CS-341 Lecture 18

April 6, 2001

Administrivia

- Second Exam will be April 24.
- Homework
  - Understand and be able to reproduce Figure 3-19 on page 138.
  - Read through page 154.
  - Try problems 14-18 at the end of Chapter 3.
    - Will not be collected.

Parallel ALU Design

- Parallel 1-bit ALUs
  - Three data inputs (A, B, C_{in}) like full adder.
  - Control inputs
    - INV A
    - ENA, ENB
    - F_0 and F_1
      00 AND
      01 Not B
      10 OR
      11 Add/Sub
    - INC = C_{in} of rightmost unit
  - Outputs: result and carry out

Combinations of ALU Controls

(Table 4-2; page 206)

F0	F1	ENA	ENB	INVA	INC	Description
0	1	1	0	0	0	A
0	1	0	1	0	0	B
0	1	1	0	1	0	~A
1	0	1	1	0	0	~B
1	1	1	1	0	0	A + B
1	1	1	1	0	1	A + B + 1
1	1	1	0	0	1	A + 1
1	1	0	1	0	1	B + 1
1	1	1	1	1	1	B - A
1	1	0	1	1	0	B - 1
1	1	1	0	1	1	-A
0	0	1	1	0	0	A AND B
0	1	1	1	0	0	A OR B
0	1	0	0	0	0	0
0	1	0	0	0	1	1
0	1	0	0	1	0	-1