# CS-341 Lecture 23

May 4, 2001

## Exam Results

- Mean was 73.5, Median was 78.5
- 6, 7, 4, 5, 12 ➔ F, D, C, B, A
- Check grades on web to see your current, min, and max averages for the course.

# Register Design

- Two operations
  - Select two registers to connect to the ALU
    - Two sets of Multiplexers
  - Select registers to receive the output of the ALU.
    - Connect ALU to D inputs of all registers and enable the clock inputs on the ones to receive the result.

# Memory Design

- Static *vs* Dynamic RAM
- Static RAM Design (Figure 3-29)
  - One flip-flop per bit
  - Decode the address to select a word
  - Use RD to read (false means write)
  - CS to select a chip
  - OE to enable outputs
    - Tristate buffers
  - Write Gate = CS · ~RD · Word Select
    - Goes to all clocks in a word
  - Read Gate = Data Value · Word Select
    - Gets OR'd with other bits in the same "slice."
  - Data Input and Data Output Lines