CS-341 Lecture 15

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Programmable Logic Devices

- Programmable Logic Array (PLA)
  - Fuses between inputs and AND gates
  - Fuses between AND Gates and OR gates
- Programmable Array Logic (PAL)
  - Fuses between inputs and AND gates
- Programmable Read Only Memory (PROM)
  - Fuses between AND gates and OR gates

PLA Properties

I inputs; *A* AND gates; *O* OR gates

- *A*2*I+A*O* fuses
  - *A*2*I* fuses between inputs and ANDs
  - *A*O* fuses between ANDs and ORs
- Fan-in of each AND is *2*I*
- Fan-in of each OR is *A*
- Fan-out of each AND must be O or greater
- May be used to implement up to *O* functions of *I* variables, provided no more than *A* rows of the truth table have minterms in them.

PAL Properties

I inputs; *A/O* AND gates per OR gate; *O* OR gates

- *A/O*O*2*I* fuses
  - No fuses between AND and OR gates
- Fan-in of each AND is 2*I
- Fan-in of each OR is *A/O*
- Fan-out of each AND needs to be just one
- Can implement up to *O* functions of *I* variables, provided each function has no more than *A/O* minterms.

PROM Properties

I inputs; *O* outputs

- Inputs are addresses; Outputs are data
- There are always 2^I AND gates
  - No fuses between inputs and AND gates
  - The fan-in of each AND gate is *I*
- There are 2^I * O fuses between the AND gates and the OR gates
- Each AND gate must have a fan-out of O or greater
- Each OR gate has a fan-in of 2^I
- Can be used as a memory, or to implement up to *O* functions of *I* variables. No limit on the number of minterms