CS-341 Lecture 22

May 1, 2001

Flip-Flops

- Solves the problem of outputs changing while clock is true. Needed for registers.
- D Master-Slave flip-flop.
  - Master operates during clock pulse, but ignores input changes when clock is false.
  - Slave operates when clock is false, but ignores input changes during clock pulse.

Register Design

- Two operations
  - Select two registers to connect to the ALU
    - Two sets of Multiplexers
  - Select registers to receive the output of the ALU.
    - Connect ALU to D inputs of all registers and enable the clock inputs on the ones to receive the result.

Memory Design

- Static *vs* Dynamic RAM
- Static RAM Design (Figure 3-29)
  - One flip-flop per bit
  - Decode the address to select a word
  - Use RD to read (false means write)
  - CS to select a chip
  - OE to enable outputs
    - Tristate buffers
  - Write Gate = CS · ~RD · Word Select
    - Goes to all clocks in a word
  - Read Gate = Data Value · Word Select
    - Gets OR'd with other bits in the same "slice."
  - Data Input and Data Output Lines