CS-341 Lecture 24

May 8, 2001

Administrivia

- Final Exam will be Monday the 21st
  - 4:00 to 6:00 PM
  - SB ***Room B-145***
- Need someone to administer course evaluations today.
- When we finish memory design, skip to Chapter 4; start reading at the beginning.
- Last Homework: Exercises 2-8 at the end of Chapter 4.

Tristate Gates

- Output is either a normal logic value, or a special third state, in which the output is effectively disconnected from the circuit.
  - An extra input determines whether the output is a logic value or is "tristated" (also called "floating"). 1 means logic; 0 means float.
  - Makes it possible to connect output of gates together without causing short circuits.
  - No more than one tristate gate in a group may generate a logic value at a time.
    - Decoders are good for controlling this.

Memory Design

- Static *vs* Dynamic RAM
- Static RAM Design (Figure 3-29)
  - One flip-flop per bit
  - Decode the address to select a word
  - Use RD to read (false means write)
  - CS to select a chip
  - OE to enable outputs
    - Tristate buffers
  - Write Gate = CS · ~RD · Word Select
    - Goes to all clocks in a word
  - Read Gate = Data Value · Word Select
    - Gets OR'd with other bits in the same "slice."
  - Data Input and Data Output Lines

The IJVM Datapath

- Registers, ALU, and Shifter were designed in Chapter 3.
- B and C busses, but no A bus (register H instead)
- Memory Interface
  - MAR/MDR for reading and writing words
  - PC/MBR for reading bytes from the instruction stream.
  - SP/TOS for Stack Operations
- Microprogrammed Control