CS-343 Assignment 7

Introduction

This is an exercise in working with the parameters that describe cache designs. For each column of the following table, you are to fill in the values for the machines listed below. The first column is filled in for the parameters for the cache shown in Figure 7.9 of the text.

1. Machine M-1 has 2^{24} bytes of byte-addressable memory with two bytes per word. Each cache line is 32 bytes wide. The cache is 4-way set associative, and there are 64 cache sets.

2. Machine M-2 has a word addressable memory with 64G 48-bit words. Each cache line holds 32 words of memory. The cache is fully associative, and there are 6,272 bits of cache memory, which includes the valid bit for each line, all the tags, and all the data bits.

3. Machine M-3 is byte addressable with 64 bits per word. There can be up to 2^{40} words of memory. The cache is organized as an 8-way set associative design with 64 words per cache line, and a total of 2^{12} cache lines.

Name [   ]   ID [   ]   ID:

Cache Parameters

Parameter	Fig. 7.9	M-1	M-2	M-3
Number of Memory Words	2^{30}			
Number of Bytes per Word	2^{2}			
Number of Words per Cache Line	2^{4}			
Number of Cache Lines	2^{8}			
Number of Tag Bits	18			
Number of Index Bits	8			
Number of Block Offset Bits	4			
Number of Byte Offset Bits	2			
Total Number of Address Bits	18+8+4+2 = 32			
Data Bits per Cache Line	512			
Total Bits per Cache Line	1+18+512 = 531			
Total Bits in Cache	$2^{8}*531$ = 135,936			
Set Size	1			
Direct Mapped?	Yes			
Fully Associative?	No			