



# RC200

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## RC200 Hardware and Installation Manual

For PDK v2.0

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## Conventions

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# Conventions

A number of conventions are used in this document. These conventions are detailed below.



Warning Message. These messages warn you that actions may damage your hardware.



Handy Note. These messages draw your attention to crucial pieces of information.

Hexadecimal numbers will appear throughout this document. The convention used is that of prefixing the number with '0x' in common with standard C syntax.

Sections of code or commands that you must type are given in typewriter font like this:

```
void main();
```

Information about a type of object you must specify is given in italics like this:

copy *SourceFileName* *DestinationFileName*

Optional elements are enclosed in square brackets like this:

```
struct [type_Name]
```

Curly brackets around an element show that it is optional but it may be repeated any number of times.

*string* ::= "{ *character* }"



## Assumptions

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## Assumptions

This manual assumes that you:

- have used Handel-C or have the Handel-C Language Reference Manual
- are familiar with common programming terms (e.g. functions)
- are familiar with MS Windows

## Omissions

This manual does not include description of the RC200 Platform Support Library, PAL and DSM support for the RC200 or the FTU2 file transfer utility. Refer to **section 1.3** for details of other RC200 documentation.



# 1. Introduction

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## 1. Introduction

This manual gives basic information about:

- installation
- devices on the RC200
- how to program the FPGA
- how to transfer data between the host, SmartMedia and FPGA

It is recommended that you use the RC200 Platform Support Library to program the board. The library is described in the RC200 Platform Support Library Reference Manual in *InstallDir\PDK\Documentation\PSL\RC200\Manuals*.

### 1.1 Board overview

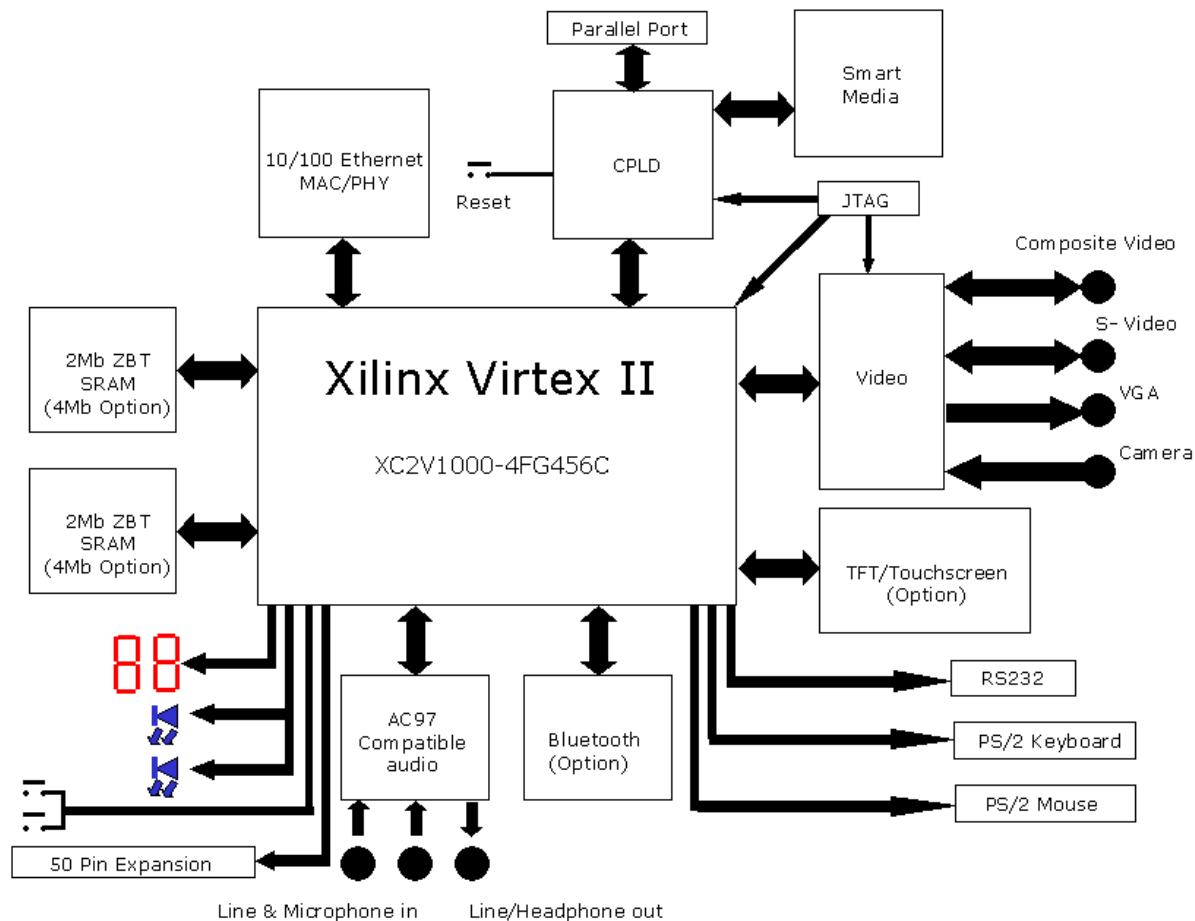


FIGURE 1: CONNECTIONS BETWEEN DEVICES ON THE RC200

# 1. Introduction

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The devices and connectors on the board are shown in **section 3.1**.

The RC200 is available in 3 versions:

- Standard (part number RC-I-200-2V1K4S)
- Professional (part number RC-I-200-2V1K4P)
- Expert (part number RC-I-200-2V1K4E)

## 1.1.1 RC200 Standard kit

- Virtex-II 2V1000-4 FPGA
- Ethernet MAC/PHY with 10/100baseT socket
- 2 banks of ZBT SRAM providing a total of 4-MB
- Video support including:
  - Composite video in/out
  - S-Video in/out
  - VGA out
  - Camera in (Camera socket provides camera power)
- AC'97 compatible Audio including
  - Microphone in
  - Line in (Stereo)
  - Line/Headphone out (Stereo)
- Connector for SmartMedia Flash memory for storage of BIT files
- CPLD for configuration/reconfiguration and SmartMedia management
  - Power-on load from SmartMedia
  - Load when SmartMedia installed
  - Reconfigure on demand from FPGA
- Parallel port connector and cable, for BIT-file download and host communication with FPGA
- RS232
- PS/2 keyboard and mouse connectors
- 2 seven-segment displays
- 2 blue LEDs
- 2 momentary contact switches
- 50 pin expansion header including:
  - 33 general I/O pins
  - 3 power pins (+12V, +5V, +3.3V)
  - 2 clock pins
- JTAG connector
- Perspex top and bottom covers
- Universal 110/240V power supply (IEC Mains lead not included)

# 1. Introduction

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- Celoxica Platform Developer's Kit including:
  - Platform Support Library for RC200
  - Platform Abstraction Layer for RC200
  - Data Stream Manager for MicroBlaze soft-core microprocessor
  - FTU2 BIT file transfer utility (for Windows NT4, Windows 2000 and Windows XP)

## ***1.1.2 RC200 Professional kit***

This provides the following features in addition to the Standard kit:

- Headphone/microphone set
- Mouse
- 16-MB SmartMedia card
- Colour camera

## ***1.1.3 RC200 Expert kit***

This provides the following features in addition to the Professional Kit:

- Bluetooth wireless module
- Memory banks expanded to 4-MB each giving a board total of 8-MB
- TFT flat panel display or touch screen

## **1.2 RC200 support software**

The following software support for the RC200 is provided as part of the Platform Developer's Kit:

- RC200 Platform Support Library (PSL)
- RC200 Platform Abstraction Layer (PAL) implementation
- RC200 Data Stream Manager (DSM) implementation for the Xilinx MicroBlaze softcore
- FTU2 program: allows you to download BIT files onto the FPGA

## **1.3 RC200 documentation**

The following documentation is available in addition to this manual:

- RC200 Platform Support Library Reference Manual: available in *Install Dir\SDK\Documentation\PSL\RC200\Manuals*.
- PAL User Manual, API Reference and Tutorial Guide: available in *Install Dir\SDK\Documentation\PAL*.

## 1. Introduction

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- DSM User Manual, API Reference and Tutorial Guide: available in *Install Dir\PDK\Documentation\DSM*.
- Schematic diagrams showing RC200 pin connections: available in *Install Dir\PDK\Documentation\PSL\RC200\Schematics*.
- FTU2 User Guide: available in *Install Dir\PDK\Documentation\PSL\FTU2*.

## 2. Installation and set-up

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## 2. Installation and set-up

### Unpacking the board

You should take care to avoid static discharge when handling the RC200 board, as this may damage it. You are recommended to use an earth strap. If an earth strap is not available, ensure that you make contact with earth before and during handling of the board, and only handle the board by its edges.

### Connecting the cables

The board must be powered down before you attach cables. The connectors are labelled on the board and in **Figure 3** within **section 3.1**.

You will need to connect the board to your PC with an IEEE 1284-compliant parallel port cable if you want to use the Celoxica FTU2 program to download BIT files, or to read from or write to SmartMedia memory. A cable is provided as part of the RC200 kit.

### Switching on the power

You need a 12V DC power supply with a 2.1mm, centre-positive plug. The power supply must be able to source at least 2A.

Peripheral devices should be connected before the RC200 Board is turned on. Otherwise the devices may not function correctly.

LED D2 will light up when the power is on. This is the lower of the 2 LEDS to the left of the Celoxica copyright printed on the board.

### System requirements

- DK Design Suite. Only required if you want to use the PAL, DSM and RC200 Platform Support libraries.
- Microsoft Windows NT4, Windows 2000 or Windows XP for the FTU2 program and for use of the DK Design Suite.

## 3. Hardware description

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### 3. Hardware description

This chapter describes the devices on the RC200, how to program the FPGA and how to transfer data between the host, SmartMedia and FPGA.

Schematics for the board are available in  
*InstallDir\PDK\Documentation\PSL\RC200\Schematics\RC200VBD0C.pdf*.

A list of data sheets for the devices is given in **Appendix A**.

#### 3.1 Overview of devices and connectors

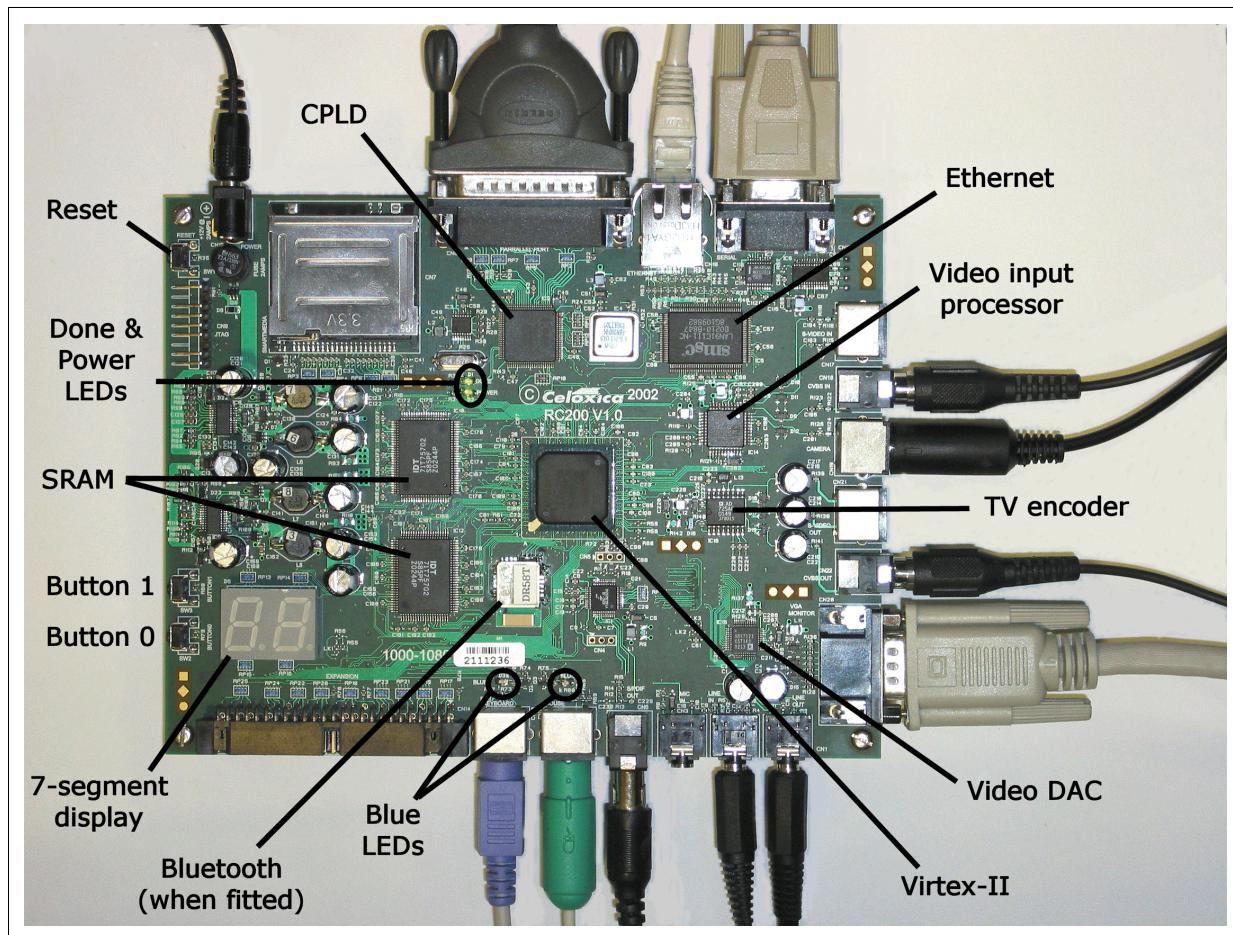


FIGURE 2: DEVICES ON THE RC200

### 3. Hardware description

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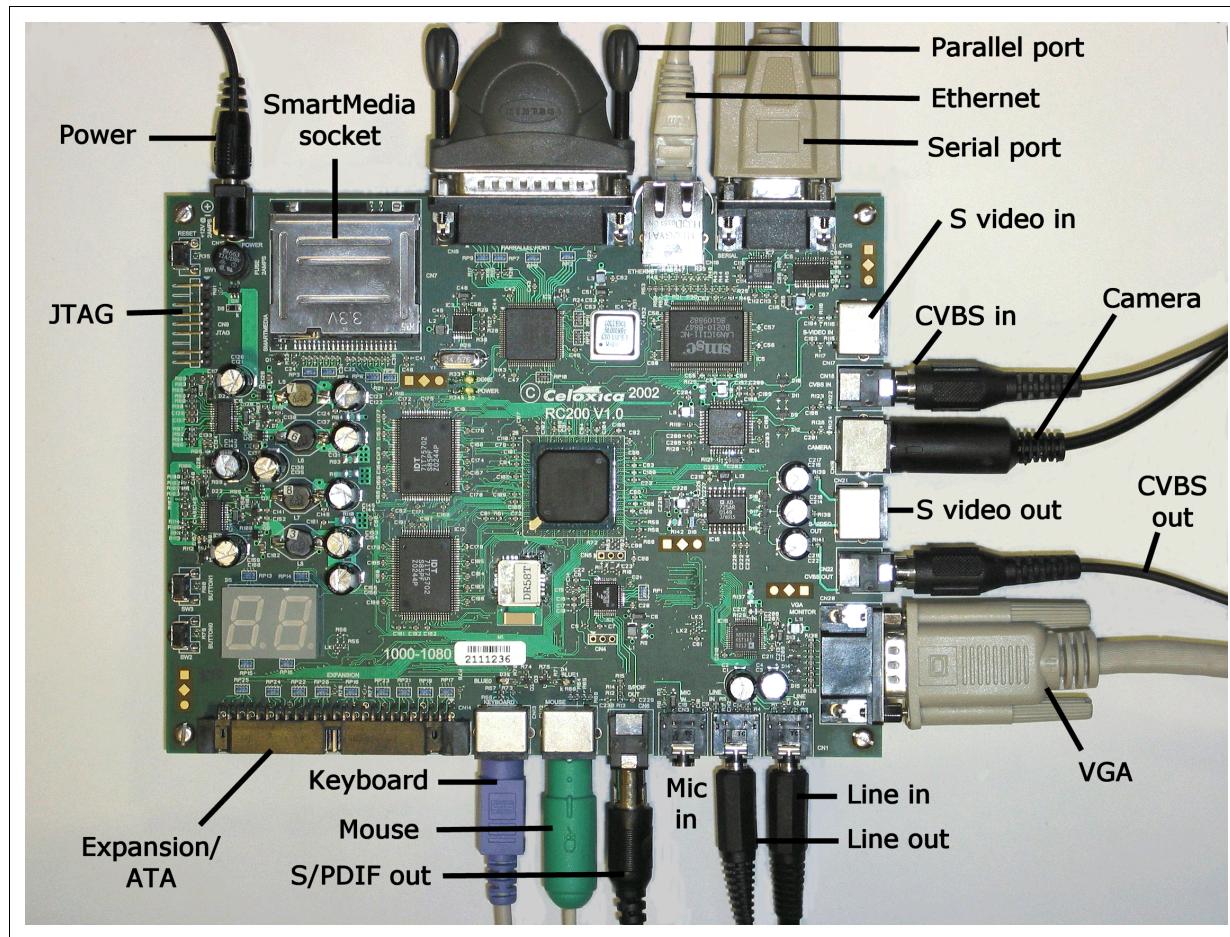


FIGURE 3: CONNECTORS ON THE RC200

#### 3.2 CPLD

The RC200 has a Xilinx XC95144XL 3.3V CPLD.

The CPLD is connected to:

- FPGA
- Parallel port
- SmartMedia Flash RAM
- A JTAG chain

The CPLD can configure the FPGA with data received from SmartMedia memory, or via the parallel port (see **section 3.3**).

### 3. Hardware description

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#### 3.2.1 Control and data pins

The CPLD has 10 control lines and 8 data lines. 3 of the control lines are used as an address bus. The control lines have two meanings, depending on whether the FPGA is directly controlling the parallel port or not (see [section 3.3.1](#)). The FPGA operation mode is determined by whether the CPLD pin P9 is set high or low.

CPLD control line	FPGA pin	Function (normal FPGA operation)	Function (parallel port control mode)
P0	Y19	CCLK	Not used
P1	AA3	PnCS (Parallel Not Chip Select) - Input	nWR (Not Write) - Input
P2	Y4	nRDWR (Not Read Write) – Input/Output	nRDWR (Not Read Write) - Output
P3	A2	nPROG	Not used
P4	AB20	DONE	Not used
P5	AA19	Address [0] – Output	nINIT – Output
P6	AB19	Address [1] – Output	nWAIT – Output
P7	R22	Address [2] – Output	nADDR – Input
P8	V22	nCS (Not Chip Select) – Output	nDATA – Output
P9	T18	Set high	Set low

CPLD data line	FPGA pin
FD0	V18
FD1	V17
FD2	W18
FD3	Y18
FD4	Y5
FD5	W5
FD6	AB4
FD7	AA4

#### 3.2.2 CPLD clock

The CPLD has a clock input of 50MHz from a 50MHz crystal oscillator module. This is divided by 2 to give an internal clock speed of 25MHz.

### 3. Hardware description

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#### **3.2.3 Register map in the CPLD for the FPGA**

The CPLD has 3 address lines:

CPLD pins	FPGA pins
P5 Addr[0]	AA19
P6 Addr[1]	AB19
P7 Addr[2]	R22

Only the lower 5 of the 8 possible values within the 3-bit CPLD address are used by the FPGA:

- |   |   |
|---|---|
| 0 | Control of SmartMedia and PLL   |
|   | Bit 0: SmartMedia nCS signal  |
|   | Bit 1: SmartMedia CLE signal  |
|   | Bit 2: SmartMedia ALE signal  |
|   | Bit 3: Disable SmartMedia state machine   |
|   | Bit 4: Not used (Write 0)   |
|   | Bit 5: Not used (Write 0)   |
|   | Bit 6: PLL clock pin ( $I^2C$ bus)  |
|   | Bit 7: PLL data pin ( $I^2C$ bus 1 = Tristate (input) 0=0)                      |
| 1 | Read status Register  |
|   | Bit 0: Master FPGA DONE signal  |
|   | Bit 1: (not used; undefined)  |
|   | Bit 2: FPGA nINIT signal  |
|   | Bit 3: SmartMedia nBUSY signal  |
|   | Bit 4: SmartMedia Detect (1 = SmartMedia inserted)                              |
|   | Bit 5: SmartMedia not Write Protect   |
|   | Bit 6: SmartMedia state machine disable status                                  |
|   | Bit 7: PLL data line ( $I^2C$ bus)  |
| 2 | Data bus access of the SmartMedia   |
| 3 | Upper byte of Block address for the SmartMedia (only the lower 5 bits are used) |
| 4 | Lower byte of Block address for the SmartMedia                                  |
| 5 | Read from this address to start reprogramming of the FPGA from SmartMedia       |

### 3. Hardware description

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#### **3.2.4 CPLD / parallel port interface**

The CPLD supports an EPP (Enhanced Parallel Port) interface.

The parallel port is connected to the CPLD on the following pins:

CPLD pins	Signal	Parallel port pins
76	ParSCTL	13
77	ParPE	12
78	Parnwait	11
79	ParINIT	10
80	Pardata7	9
81	Pardata6	8
82	Pardata5	7
85	Pardata4	6
86	Pardata3	5
89	Paraddr	17
90	Pardata2	4
91	Parnreset	16
92	Pardata1	3
93	Parerror	15
94	Pardata0	2
95	Parndata	14
96	Parnwrite	1

The CPLD has 3 address pins. When the CPLD is communicating with the parallel port data lines, the 8 values within the 3-bit CPLD address are used as follows:

Address value	Description
0	Read and write (i.e. data pins) when FPGA is in parallel port control mode
1	Read and write from host for SmartMedia
2	Not used

### 3. Hardware description

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Address value	Description
3	<p>Read status of signals (8-bit data line from CPLD):</p> <ul style="list-style-type: none"> <li>Bit 0: Master FPGA DONE signal</li> <li>Bit 1: (not used; undefined)</li> <li>Bit 2: FPGA nINIT signal</li> <li>Bit 3: SmartMedia nBUSY signal</li> <li>Bit 4: SmartMedia Detect (1 = SmartMedia inserted)</li> <li>Bit 5: SmartMedia not Write Protect</li> <li>Bit 6: SmartMedia state machine disable status</li> <li>Bit 7: PLL data line (<math>I^2C</math> bus)</li> </ul> <p>Write status of signals:</p> <ul style="list-style-type: none"> <li>Bit 0: SmartMedia nCS signal</li> <li>Bit 1: SmartMedia CLE signal</li> <li>Bit 2: SmartMedia ALE signal</li> <li>Bit 3: Disable SmartMedia state machine</li> <li>Bit 4: Master FPGA nPROG pin (inverted by CPLD)</li> <li>Bit 5: Not used (Write 0)</li> <li>Bit 6: PLL clock pin (<math>I^2C</math> bus)</li> <li>Bit 7: PLL data pin (<math>I^2C</math> bus 1 = Tristate (input) 0=0)</li> </ul>
4	Not used
5	Not used
6	Not used
7	CPLD version ID (0x51)

#### 3.3 FPGA

The RC200 board has a Xilinx Virtex-II FPGA (part: XC2V1000-4FG456C). The device has direct connections to the following devices:

- CPLD
- ZBT RAM
- Ethernet
- Clock generator
- Video input
- Video DAC
- RGB to PAL/NTSC encoder
- Audio codec
- RS232

### 3. Hardware description

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- PS/2 connectors
- Expansion header
- 2 seven-segment displays
- 2 blue LEDs
- 2 contact switches
- Bluetooth (if fitted)
- TFT Flat screen (if fitted)
- Touchscreen (if fitted)

Details of pin connections are given in the sections about these devices below.



If you are programming the board using Handel-C, remember that the pins should be listed in reverse (descending) order.

The FPGA also has access to the parallel port and to the SmartMedia Flash memory through the CPLD.

You can program the FPGA via the CPLD from the SmartMedia Flash memory, or from the parallel port.

#### *3.3.1 FPGA operation modes*

The FPGA has two modes of operation:

- normal operation: communicates with the SmartMedia and PLL and is a parallel port slave
- parallel port control operation: becomes parallel port master and drives all parallel port signals

The operation mode is set by control line P9 on the CPLD. If P9 is high, the FPGA is in normal operation mode. If P9 is low, the FPGA is in parallel port control operation mode.

The function of the other CPLD control lines changes, depending on whether P9 is high or low (see [section 3.2.1](#)).

#### *3.3.2 Programming the FPGA using the FTU2 program*

Celoxica provides a File Transfer Utility program, FTU2, which simplifies the process of programming the FPGA via the parallel port. The FTU2 program is described in the FTU2 User Guide. This is in ***InstallDir\PDK\Documentation\PSL\FTU2***.

## 3. Hardware description

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### ***3.3.3 Programming the FPGA from the parallel port***

The parallel port / CPLD interface is described in **section 3.2.4**. To program the Virtex-II from the parallel port:

1. Check that the board is connected and powered by reading the CPLD version ID (CPLD address value 7).  
The board may not return the ID if the FPGA is controlling the parallel port. If this happens, eject the SmartMedia card and press the Reset button.
2. Disable and clear the FPGA by asserting nPROG (CPLD address 3, bit 4). Leave nPROG asserted.
3. Disable the SmartMedia state machine by asserting CPLD address 3, bit 3 and leave this asserted during programming.
4. Wait at least 1mS.
5. Deassert nPROG.
6. Wait for nINIT (CPLD address 3, bit 2) to go high, showing that the FPGA has cleared its memory. For timeouts this is 4uS per frame, giving a total of 4.9mS for the Virtex II XC2V1000.
7. The entire BIT file without the header can now be transferred directly to address 0. The CPLD times the nCS, nWR and CCLK signals such the FPGA may be programmed.
8. After programming the FPGA, you need to wait at least 100μS before accessing the CPLD. Alternatively, wait 1μS and check that PnCS is high (i.e. that there is no access to the parallel port).

If programming is successful, DONE (CPLD address 3, bit 0) will be high, lighting the DONE LED. The SmartMedia state machine can then be re-enabled by setting the Disable SmartMedia state machine signal low (address 3, bit 3). If there is an error during programming the FPGA will signal a CRC error by lowering nINIT (unless the FPGA is accessing the CPLD).

### ***3.3.4 Programming the FPGA from SmartMedia***

You can program the Virtex-II from BIT files loaded onto the SmartMedia device. The BIT files can be in exactly the same format as if you were programming from the parallel port. There is no need to change or remove the header.

To program the Virtex-II from page 1 on the SmartMedia Flash, use one of the following:

- Apply power to the board
- Press the Reset button on the board
- Insert the SmartMedia card whilst the board is switched on

### 3. Hardware description

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To program from a specific address in the SmartMedia:

1. Set a block address in the CPLD using Address 4 for the lower byte of the address and Address 3 for the upper byte (only the lower 5 bits of this byte are used).  
(The CPLD register map for the FPGA is given in **section 3.2.3.**)
2. Read from Address 5.

These steps will cause the CPLD to read from the relevant address in the SmartMedia and write the data to the FPGA. Data is written using following steps:

- CPLD sets up the FPGA for programming.
- CPLD reads the ID register of the code to find out if 4-word addresses are required.
- CPLD reads the page valid byte ( $512+5$ ) to see if it is valid.  
If the page valid byte is invalid it searches though the block checking the page valid byte until it finds a page that is valid.  
The first valid page is skipped (if programming from address zero this is the CIS page).
- Data is copied to the FPGA until the FPGA is DONE. Bad pages are skipped.

The CPLD automatically adds 16 clock cycles after DONE to complete programming. If the FPGA signals an error during programming, the FPGA is reset and the CPLD waits until a new SmartMedia is inserted.

It is assumed that if a single page is invalid then the entire block is invalid, and all the pages within the block will have the block invalid byte set. The CPLD doesn't check the SmartMedia ECC (Error Correcting Code) as the FPGA programming datastream has its own CRC (Cyclical Redundancy Checking) which checks that the data stream is correct.

#### ***3.3.5 Reading data from the CPLD to the FPGA***

To read data from the CPLD:

1. Set up the address and tristate the data bus.
2. Wait at least 10ns.
3. Set nCS low.
4. Wait at least 10ns.
5. Set nRDWR low.
6. Wait at least 40ns before reading data.
7. Tristate nRDWR.
8. Set nCS high.

## 3. Hardware description

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### ***3.3.6 Writing data to the CPLD from the FPGA***

To write to the CPLD:

1. Set up the address and data bus if not already tristated.
2. Wait at least 10ns.
3. Set nCS low.
4. Wait at least 10ns.
5. Set nRDWR high and enable the data bus.
6. Wait at least 40ns.
7. Tristate nRDWR.
8. Set nCS high.
9. Tristate the data bus.

### ***3.3.7 Transferring data between the FPGA and host***

The parallel port can read and write data to the FPGA by accessing CPLD address 0. The process is controlled by the CPLD.

To write data from the host (via the parallel port) to the FPGA:

1. Set nRDWR low.
2. Set PnCS low.
3. Send the data.
4. Set PnCS high.
5. Set nRDWR high.

To read data from the FPGA and write it to the host via the parallel port:

1. Set nRDWR high.
2. Set PnCS low.
3. Read the data.
4. Set PnCS high.
5. Set nRDWR low.

### ***3.3.8 Using the FPGA in parallel port control mode***

When the CPLD control line P9 is set low the FPGA has direct control over the parallel port. The nRDWR signal (CPLD control line P2) defines the direction of the databus.

The mapping of the EPP control onto the CPLD control signals is described in **section 3.2.1**.

## 3. Hardware description

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### 3.4 Parallel port

The RC200 has an IEEE 1284-compatible parallel port. You can use the parallel port to:

- program the FPGA (see [section 3.3.3](#))
- program the SmartMedia card (see [section 3.5.3](#))
- read data from and write data to the FPGA (see [section 3.3.7](#))

### 3.5 SmartMedia Flash memory

The RC200 has a socket for a SmartMedia Flash memory device (connector CN7 at the top left of the board). The Professional and Expert versions of the RC200 are provided a 16-MB SmartMedia card. You can use any SmartMedia device between 4 and 128 megabytes.



The RC200 Platform Support Library abstracts away some of the intricacies of the physical layer control mechanism within the SmartMedia driver. The library also allows you to use logical addressing, which has the further advantages of preserving the CIS and IDI fields, and skipping invalid blocks.

For more information on SmartMedia devices, please refer to [Appendix A, Data sheets and device specifications](#).

#### *3.5.1 Connections to the CPLD*

The SmartMedia is connected to the CPLD on the following pins:

SmartMedia pins	Signals	CPLD pins
2	CLE	17
3	ALE	15
4	SMnWE	13
5	nWP	11
6	SMD0	10
7	SMD1	9
8	SMD2	7
9	SMD3	4
13	SMD4	2
14	SMD5	3
15	SMD6	6
16	SMD7	8
19	R/nB	12

### 3. Hardware description

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SmartMedia pins	Signals	CPLD pins
20	SMnRD	14
21	SMnCS	16

#### 3.5.2 FPGA access of SmartMedia

The SmartMedia is accessed by the FPGA via the CPLD. The register map for the FPGA in the CPLD is described in [section 3.2.3](#).

A typical sequence of events might be:

1. Disable SmartMedia state machine by writing 1 on CPLD control address 0, bit 3.
2. Check the SmartMedia is fitted by reading the status of CPLD address 1, bit 4. A value of 1 means that the SmartMedia has been successfully detected.
3. Assert nCS (CPLD address 0, bit 0).
4. Deassert ALE (CPLD address 0, bit 2).
5. Assert CLE (CPLD address 0, bit 1).
6. Write a command to address 2.
7. Deassert CLE.
8. Read or write to SmartMedia using address 2.

#### 3.5.3 Parallel port access of SmartMedia

The SmartMedia is accessed from the parallel port via the CPLD. The CPLD / parallel port interface is described in [section 3.2.4](#).

A typical sequence of events for programming the SmartMedia from the parallel port might be:

1. Check the SmartMedia device is fitted (address 3, bit 4).
2. Disable the FPGA from accessing the SmartMedia by asserting nPROG (address 3, bit 4).
3. Disable the SmartMedia state machine by asserting address 3, bit 3.
4. Wait for at least 1mS.
5. Assert nCS (address 3, bit 0).
6. Deassert ALE (address 3, bit 2).
7. Assert CLE (address 3, bit 1).
8. Write a SmartMedia command to CPLD address 2.  
For example, refer to the SmartMedia Electrical Specification issued by the SSFDC forum: [www.ssfdc.or.jp](http://www.ssfdc.or.jp).

### 3. Hardware description

---

9. Deassert CLE.
10. Write a SmartMedia address.



You need to carry out steps 1 to 4 for any access to the SmartMedia.

#### 3.6 ZBT SRAM banks

The RC200 is fitted with 2 ZBT RAM banks, capable of operating at up to 100MHz. The RC200 Standard and Professional boards have two 2-MB banks fitted and the RC200 Expert board has two 4-MB banks. The RAM banks are IDT71T75702 devices, with 512K or 1024K 36-bit words. All the lines are mapped directly to the FPGA. For more information on the devices, please refer to **Appendix A, Data sheets and device specifications**.

The pins on bank 0 and bank 1 are listed below.

##### Pins connecting RAM bank 0 to the FPGA

SSRAM pin	Function	FPGA Pins (in ascending order)
S0D0 – S0D35	Data [35:0]	K20, L19, L20, K18, L18, E18, F18, G18, H18, J18, J17, K17, B12, A13, B13, A14, B14, B15, A16, B16, A17, B17, B18, A19, B19, C12, D12, C13, D13, C14, D14, C15, D15, C16, D16, C17
S0A0 – S0A19	Address [19:0]	C21, C22, D21, D22, E21, F21, F22, G21, G22, H21, J21, J22, K21, K22, L22, L21, E19, E20, F19, F20
S0C0	CLK	F12
S0C1	nCS2 (not Chip Select)	G19
S0C2	R/nW (Read not Write)	G20
S0C4 – S0C7	Not Byte Enable pins	H20, J19, J20, K19

### 3. Hardware description

---

#### Pins connecting RAM bank 1 to the FPGA

SSRAM Pin	Function	FPGA Pins (in ascending order)
S1D0 – S1D35	Data [35:0]	D7, C7, D8, C8, D9, C9, D10, C10, E11, F11, E4, E5, E6, E7, E8, E9, E10, F9, F10, C2, C1, D2, D1, E2, F2, F1, G2, G1, H2, J2, J1, K2, K1, L2, E3, F4
S1A0 – S1A19	Address [19:0]	D17, C18, D18, F13, F14, E13, E14, E15, E16, E17, B4, A4, B5, B6, A6, B7, A7, B8, B9, A9
S1C0	CLK	D11
S1C1	nCS2 (not Chip Select)	B10
S1C2	R/nW (Read not Write)	A10
S1C4 – S1C7	Not Byte Enable pins	C4, C5, D6, C6

### 3.7 Clock generator (PLL)

The RC200 board has a Cypress CY22393 Programmable Clock Generator. The generator is programmed to provide the following clocks:

Clock generator pin	Description	FPGA pin
GCLK2P	CLKUSER. Clock used to feed the FPGA.	Y12
GCLK5P	24.576MHz clock. Used to feed video input and audio chip.	B11
GCLK6S	25.175MHz clock. Used to feed VGA output (640 x 480 at 60Hz).	C11
GCLK0P	27MHz video input clock.	AB12
GCLK1P	50MHz crystal clock. This is used to feed the CPLD.	E12
GCLK7S	Expansion clock 0	AA11
GCLK5S	Expansion clock 1	W11

The clock control pin on the FPGA is V19.

#### TV clock rates

The clock generator also produces 14.318MHz and 17.7MHz clocks for the RGB to PAL/NTSC encoder. You can select between these values using the CLKCTRL signal (pin 15 on the clock generator, pin v19 on the FPGA).

## 3. Hardware description

---

### FPGA clock: CLKUSER

CLKUSER has a default value of 133MHz. CLKUSER is connected to pin Y12 on the FPGA. You can change the default value of CLKUSER by programming the PLL from the FPGA or parallel port.

#### *3.7.1 Programming the PLL via the parallel port or FPGA*

The PLL chip can be soft programmed by either the FPGA or the parallel port. It reverts to factory settings on a power on reset. The PLL chip supports a form of I<sup>2</sup>C.

If you are programming from the parallel port, the FPGA should be disabled by asserting nPROG if there is any chance of it interfering with the programming of the PLL.

 If you program any of the clocks apart from CLKUSER, you could stop the devices from working, or damage them.

### Programming the PLL from the parallel port

Three bits in the CPLD are used during PLL programming. The CPLD / parallel port interface is described in **section 3.2.4**. The state of the data line can be monitored at any time by reading bit 7 from address 3. The clock line for the data is bit 6 of address 3. The bit for writing zeros is bit 7 of address 3. The data line is pulled up by a resistor, so by writing 3[7]=1 a one will be written. When data is to be read from the PLL chip, bit 7 of address 3 should be set to 1 so that the PLL chip can pull the data line to zero if required.

### Programming the PLL from the FPGA

Programming the PLL from the FPGA is the same as programming from the parallel port except that the registers are at a different address in the CPLD. The register map for the FPGA is described in **section 3.2.3**. The data line is monitored by reading bit 7 from address 1 and the clock line for the data is bit 6 of address 0. The data line is bit 7 of address 0.

## 3.8 Ethernet

The RC200 is fitted with a Standard Microsystems Corporation LAN91C111 Ethernet device. It supports 8-bit and 16-bit access to the FPGA. The device has a clock input of 25MHz, generated from the CPLD. For more information about the device, refer to the data sheet listed in **Appendix A**. The connections between the Ethernet and FPGA are listed below.

### 3. Hardware description

---

Ethernet pins	Function	FPGA Pins (in ascending order)
ED0 – ED15	Data [15:0]	M21, N22, N21, P22, P21, R21, T22, T21, U22, U21, V21, W22, W21, Y22, Y21, M17
EC0-EC2	Address [2:0]	M18, M20, M19
EC3 and EC4	Not byte enable	N20, N19
EC5	Not Read	P20
EC6	Not Write	P19
EC7	Interrupt	R20
EC8	Asynchronous ready pin (Ardy)	R19
EC9	Reset	T20

### 3.9 Video input processor

The board is fitted with a Philips SAA7113H Video Input Processor, enabling the FPGA to capture S Video, CVBS and Camera input.

The FPGA can decode RGB to:

- NTSC or PAL using the AD725 RGB to NTSC/PAL encoder
- VGA output using the ADV7123 RGB to VGA encoder

#### Video input control and data pins

The video input has 8 data pins and 6 control lines:

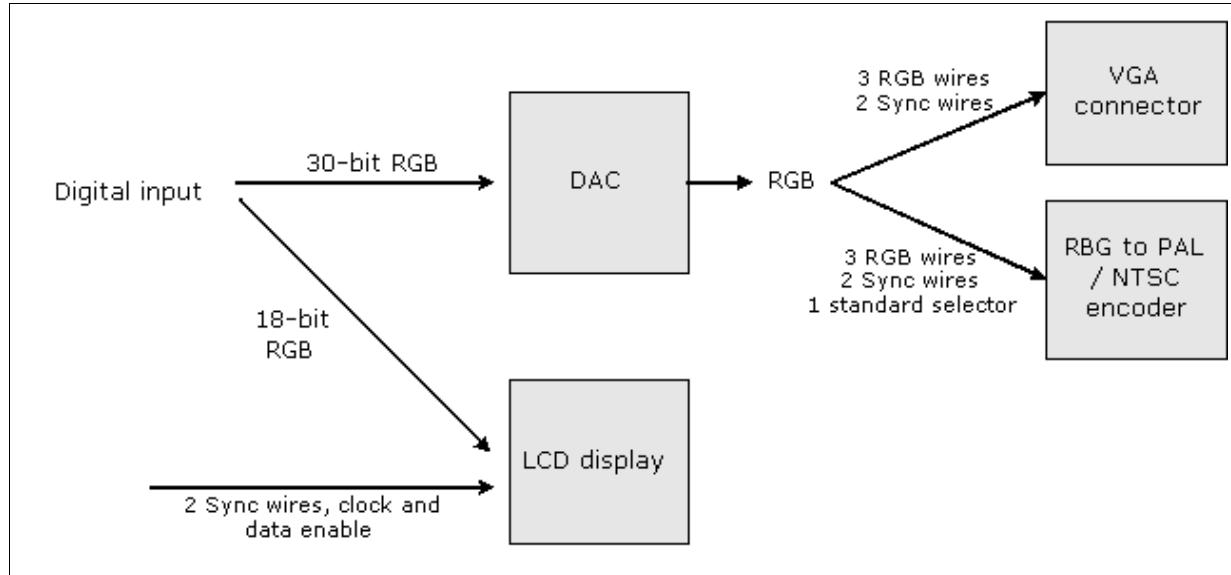
Video input pins	Function	FPGA Pins (in ascending order)
VIND0 – VIND7	Data pins [7:0]	AA20, AA18, AA17, AB17, AA16, AB16, AA15, AA14
VINCO	RTS1	W20
VINC1	RTS0	N17
VINC2	RTCO	P17
VINC3	SCL	N18
VINC4	SDA	P18
VINC5	CEP	R18

### 3. Hardware description

---

#### 3.10 Video output processors

The RC200 can convert digital RGB input into outputs for a VGA screen, a TV (PAL or NTSC) or an LCD screen.



**FIGURE 4: OVERVIEW OF VIDEO OUTPUT PROCESSING**

##### 3.10.1 Digital / Analogue converter

The Analog Devices ADV7123 High speed video DAC can convert 30-bit digital input to VGA output or RGB input for the NTSC/PAL encoder.

For more information on this device, please refer to **Appendix A, Data sheets and device specifications**.

DAC pins	Function	FPGA Pins (in ascending order)
RGB0 – RGB9	Red [9:0]	U18, V16, V15, V14, V13, U14, U13, AB10, AA10, AB9
RGB10 – RGB19	Green [9:0]	AA9, AA8, U11, V11, Y11, Y10, W10, AB18, AB15, Y9
RGB20 – RGB29	Blue [9:0]	W9, Y8, W8, Y7, W7, Y6, W6, AB8, AB5, U10
RGB30	Clock pin	U9
RGB31	Not blank pin	V10
RGB32	Not Sync pin	V9
RGB33	VSync pin	V8
RGB34	HSync pin	V7

### 3. Hardware description

---

DAC pins	Function	FPGA Pins (in ascending order)
RGB35	Monitor SDA pin	V6
RGB36	Monitor SCL pin	V5

#### 3.10.2 RGB to NTSC/PAL encoder

The RC200 has an Analog Devices AD725 RGB to NTSC/PAL Encoder. This receives RGB input from the video DAC.

For more information on this device, please refer to **Appendix A, Data sheets and device specifications**.

NTSC/PAL encoder pins	Function	FPGA pins
TV0	Standard pin	AB14
TV1	Hsync pin	AA13
TV2	Vsync pin	AB13

#### 3.10.3 TFT flat panel display

An Optrex T-51382D064J-FW-P-AA thin film transistor (TFT) flat panel display is provided as an optional feature with the RC200 Expert board. It is connected directly to the FPGA.

TFT control pins	Function	FPGA pins
LCD0	Clock pin	AA12
LCD1	Hsync pin	W17
LCD2	Vsync pin	Y17
LCD3	Data enable pin	W16

The TFT has 18 data pins: RGB4 - RGB9, RGB14 - RGB19 and RGB24 - RGB29. These pins are shared by the TFT and the DAC on the FPGA.

## 3. Hardware description

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### 3.11 Audio codec

The Cirrus Logic CS4202 is an AC'97-compliant stereo audio codec, which includes surround sound and multi-channel applications for the PC.

Audio codec pins	Function	FPGA pins
AC0	SDATA_OUT	AA5
AC1	BIT_CLK	AA6
AC2	SDATA_IN	AB6
AC3	SYNC	AA7
AC4	nRESET	AB7

### 3.12 RS-232 serial transmission

The board has a MAXIM MAX3222CAP RS-232 transceiver. The pins on the RS-232 port are:

Description	Function	FPGA pins
Serial0	CTS (Clear To Send)	T19
Serial1	RxD (Receive data)	U20
Serial2	RTS (Ready To Send)	U19
Serial3	TxD (Transmit data)	V20

### 3.13 Mouse and keyboard PS/2 ports

The board has two PS/2 ports, labelled Mouse and Keyboard on the PCB. These are 6-pin mini DIN sockets that will accept any standard PS/2 mouse or keyboard. The DATA and CLK lines of these sockets are mapped directly through to the FPGA. The board supplies +5v to power the devices, but they should not use more than 100mA.

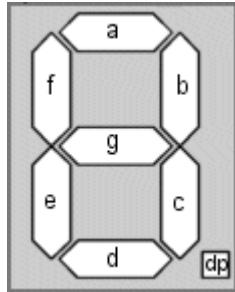
PS/2 pins	Description	FPGA pins
KM0	Mouse DATA	P5
KM1	Mouse CLK	R5
KM2	Keyboard DATA	T5
KM3	Keyboard CLK	U5

### 3. Hardware description

---

#### 3.14 7-segment displays

There are two 7-segment displays on the RC200. The segments on the display are numbered as follows:



The 7-segment displays are connected to the FPGA as follows:

Display 0 (display on left-hand side)

7-segment pins	Display segment	FPGA pins
A1	a	G3
B1	b	H4
C1	c	L3
D1	d	L4
E1	e	K3
F1	f	F3
G1	g	G4
DP1	decimal place	L5

Display 1 (display on right-hand side)

7-segment pins	Display segment	FPGA pins
A2	a	J4
B2	b	J3
C2	c	H5
D2	d	F5
E2	e	L6
F2	f	H3
G2	g	G5
DP2	decimal place	K4

### 3. Hardware description

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#### 3.15 ATA / Expansion header

The RC200 has a 50-pin expansion header including 34 general I/O pins, 3 power pins (+12V, +5V, +3.3V) and 2 clock pins.

You can also use 40 of the pins for ATA, but only UDMA4 or higher devices are supported.



The FPGA expansion header pins can only accept signals up to 3.3v. Signals greater than 3.3v may damage the FPGA.

Expansion header pins	ATA function	Expansion header function	FPGA pins
1	Reset	IO0	R2
2	GND	GND	-
3	D7	IO2	M2
4	D8	IO1	M1
5	D6	IO4	N2
6	D9	IO3	N1
7	D5	IO6	P2
8	D10	IO5	P1
9	D4	IO8	M4
10	D11	IO7	M3
11	D2	IO10	N4
12	D12	IO9	N3
13	D2	IO12	P3
14	D13	IO11	P4
15	D1	IO14	R4
16	D14	IO13	R3
17	D0	IO16	T3
18	D15	IO15	T2
19	GND	GND	-
20	Keypin	Pin removed	-
21	DMARQ	IO17	T1
22	GND	GND	-
23	nDIOW	IO18	U1
24	GND	GND	-
25	nDIOR	IO19	T4
26	GND	GND	-

### 3. Hardware description

---

Expansion header pins	ATA function	Expansion header function	FPGA pins
27	IORDY	IO20	U4
28	CSEL	IO21	V3
29	nDMACK	IO22	V4
30	GND	GND	-
31	INTRQ	IO23	W1
32	Reserved	IO24	W2
33	DA1	IO25	U2
34	nPDIAG	IO26	U3
35	DAO	IO27	N6
36	DA2	IO28	P6
37	nCS0	IO29	M5
38	nCS1	IO30	V2
39	nDASP1	IO31	R1
40	GND	GND	-
41	Pin removed	Pin removed	-
42	Pin removed	Pin removed	-
43	IO32	IO32	V1
44	+3.3v	+3.3v (0.5Amps max)	-
45	IO33	IO33	N5
46	+5v	+5v (0.5Amps max)	-
47	CLK0	CLK0	AA11
48	+12v	+12v (0.5Amps max)	-
49	CLK1	CLK1	W11
50	GND	GND	-

#### 3.16 LEDs

The board has two blue LEDs that can be directly controlled from the FPGA. These are connected as follows:

LED pins	FPGA Pins
Blue0	J6
Blue1	K6

### 3. Hardware description

---

The LED pins should be set high to turn the LEDs on.

There are also two LEDs indicating when power is on for the board (LED D2) and when the FPGA has been programmed (LED D1). These are located to the left of the Celoxica copyright mark on the board. They are controlled by the CPLD and you cannot program them from the FPGA.

#### 3.17 Contact switches

There are two buttons in the lower left corner of the board (Button 0 and Button 1). When pressed, these act as momentary high inputs into the FPGA.

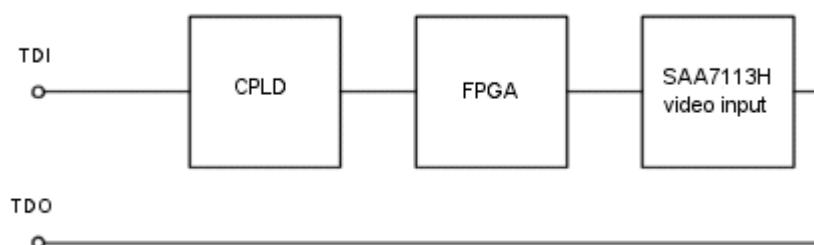
Description	FPGA Pins
Button0	J5
Button1	K5

#### 3.18 Reset button

The reset button on the RC200 is next to the power input. It clears the FPGA program, and reboots the FPGA from SmartMedia, if a SmartMedia card is present.

#### 3.19 JTAG connector

Some of the RC200 devices are connected into a JTAG chain. The chain is as follows:



The order of the devices in the JTAG chain is: CPLD (0), FPGA (1), Video Decoder chip (2). The instruction register (IR) length for these devices is 5, 5, 3 respectively.

#### 3.20 Camera and camera socket

The RC200 camera connector takes a standard Composite PAL or NTSC video signal (1v pp) terminated into 75 Ohms.

### 3. Hardware description

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A 3-pin connector is used so that power can be supplied to the camera (+12v, 50mA). Looking at the connector on the board:

- Pin 1, on the right, is ground
- Pin 2, on the left, is the power
- Pin 3, in the middle, is the video input

The camera supplied with the RC200 Professional and Expert boards is a 330 Line CCD camera.

#### 3.21 Bluetooth module

A Mitsumi WML-C09 Bluetooth module is provided on the RC200 Expert board. It is connected directly to the FPGA.

Bluetooth pins	Function	FPGA pins
BT0	RX pin	W13
BT1	TX pin	Y13
BT2	RTS pin	W12
BT3	CTS pin	V12
BT4	Reset pin	U12

#### 3.22 Touch screen

A Fujitsu Components N010-0554-T042 6.4 inch touch screen is provided as an optional feature with the RC200 Expert board.

The touch screen controller is a Burr Brown Products TSC2200. It is connected directly to the FPGA.

For more details on these devices, refer to the data sheets in Appendix A.

Touch screen	FPGA pins
nPENIRQ	Y14
nCSTOUCH	W14
SPI CLK	Y16
SPI DIN	W15
SPI DOUT	Y5

## Appendices

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# Appendix A Data sheets and device specifications

The following documents contain more information about the devices on the RC200 (URLs may be subject to change).

Device	Information
Xilinx XC95144XL CPLD	Click on the XC9500XL link at: <a href="http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp">http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp</a> then choose the XC95144XL PDF
Xilinx Virtex-II FPGA part: XC2V1000-4FG456C	Click on the Virtex-II link at: <a href="http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp">http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp</a>
IEEE 1284 Parallel Port specification	<a href="http://www.fapo.com/ieee1284.htm">http://www.fapo.com/ieee1284.htm</a>
SmartMedia	<a href="http://www.ssfdc.or.jp/english/">http://www.ssfdc.or.jp/english/</a>
IDT IDT71T75702 ZBT RAM	<a href="http://www.idt.com/docs/71T75702_DS_59004.pdf">http://www.idt.com/docs/71T75702_DS_59004.pdf</a>
Cypress PLL Serial Programmable Flash programmable Clock Generator CY22393	<a href="http://www.cypress.com/cfuploads/img/products/38-07186.pdf">http://www.cypress.com/cfuploads/img/products/38-07186.pdf</a>
Standard MicroSystems 10/100 Non-PCI Ethernet single chip MAC + PHY LAN91C111	<a href="http://www.smsc.com/main/datasheets/91c111.pdf">http://www.smsc.com/main/datasheets/91c111.pdf</a>
Philips SAA7113H Video Input Processor	<a href="http://www.semiconductors.philips.com/pip/SAA7113H_V1.html">http://www.semiconductors.philips.com/pip/SAA7113H_V1.html</a>
Analog Devices ADV7123 High Speed Video DAC	<a href="http://www.analog.com/productSelection/pdf/ADV7123_b.pdf">http://www.analog.com/productSelection/pdf/ADV7123_b.pdf</a>
Analog Devices AD725 RGB to NTSC/PAL encoder	<a href="http://www.analog.com/productSelection/pdf/2302_0.pdf">http://www.analog.com/productSelection/pdf/2302_0.pdf</a>
Optrex T-51382D064J-FW-P-AA thin film transistor	<a href="http://www.optrex.com/SiteImages/PartList/SPEC/51382AA.pdf">http://www.optrex.com/SiteImages/PartList/SPEC/51382AA.pdf</a>
Cirrus Logic Audio Codec Crystal CS4202-JQ	<a href="http://www.cirrus.com/en/pubs/proDatasheet/cs4202-1.pdf">http://www.cirrus.com/en/pubs/proDatasheet/cs4202-1.pdf</a>
MAXIM MAX3222 RS-232 Serial Transceiver	<a href="http://pdfserv.maxim-ic.com/arpdf/MAX3222-MAX3241.pdf">http://pdfserv.maxim-ic.com/arpdf/MAX3222-MAX3241.pdf</a>
AT Attachment storage interface specification	<a href="http://www.t13.org/">http://www.t13.org/</a>

## Appendices

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Device	Information
Mitsumi Bluetooth module WML-C09	<a href="http://www.mitsumi.co.jp/Catalog/hifreq/commun/wml/c09/text01e.pdf">http://www.mitsumi.co.jp/Catalog/ hifreq/commun/wml/c09/text01e.pdf</a>
Fujitsu Components N010- 0554-T042 touch screen	<a href="http://www.fceu.fujitsu.com/pdf/Datasheet_4Wire_TouchPanels.pdf">http://www.fceu.fujitsu.com/pdf/Datasheet_4Wire_TouchPanels.pdf</a>
Burr Brown Products TSC2200 Touch Screen controller	<a href="http://www-s.ti.com/sc/ds/tsc2200.pdf">http://www-s.ti.com/sc/ds/tsc2200.pdf</a>

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