CS-341 Lecture 21

April 27, 2001

Administrivia

- Exams – not yet.
- Homework for May 4
  - Chapter 3, Exercises 19 (“quiescent” means “Not being actively set or reset”), 20, 22, 23 (think in terms of providing the chip with just half the address bits at a time), and 24.

Latches

- R-S Latch
  - Pulse on R resets it; pulse on S Sets it
  - Simultaneous pulses on R & S make both outputs false.
  - Could be built using NAND gates instead of NOR gates, but see homework.
- Clocked R-S Latch
  - Does not respond to changes of R and S when clock is false.
- D Latch
  - No such thing as an un-clocked D Latch
  - Solves the "race" problem of Clocked R-S Latches

Flip-Flops

- Solves the problem of outputs changing while clock is true. Needed for registers.
- D Master-Slave flip-flop.
  - Master operates during clock pulse, but ignores input changes when clock is false.
  - Slave operates when clock is false, but ignores input changes during clock pulse.