Documentation Model

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1 Allgemein

1.1 Cycle Model

Lines of Code from Cycle Model. This model represents an equivalent RTL Model with full timing requirements. All the transactions are done random with random wait and access timings.

```
 95  ../cycle_master_slave/main.cpp
111  ../cycle_master_slave/testbench.cpp
 59  ../cycle_master_slave/wb_master.cpp
 56  ../cycle_master_slave/wb_slave.cpp
321  total
 44  ../cycle_master_slave/testbench.h
 47  ../cycle_master_slave/wb_master.h
 44  ../cycle_master_slave/wb_slave.h
135  total
```

1.1.1 execution

Execution and results of the cycle RTL-similar model.

language=shell,label= ,caption= ,captionpos=b,numbers=none ../cycle$_{m}aster_{s}lave/bin/cycle_{m}ast$

```
Info:    (I702)  default  timescale  unit  used  for  tracing:  1
Test     wishbone  bus  with  tests:  1000000
Run      with  seed:  1554812767

Info:    (I704)  VCD  delta  cycle  tracing  with  pseudo  timeste
Time:    58532  ms
Check    Logfile  ...
End      of  test  with  0  Error(s)!
Occured  Deltas:  80784850

Info:    /OSCI/SystemC:  Simulation  stopped  by  user.
```

1.2 TLM Block Model

The TLM Block Model can be controled via Definitios if it's should simulate acurate timing or loosly timed.

```
  21  ../tlm_block_master_slave/main.cpp
  17  ../tlm_block_master_slave/bus_spec.h
 252  ../tlm_block_master_slave/master.h
 113  ../tlm_block_master_slave/slave.h
1047  ../tlm_block_master_slave/tlm2_base_protocol_checker.h
  35  ../tlm_block_master_slave/top.h
1464  total
```

1.2.1 execution

Execution of the results.