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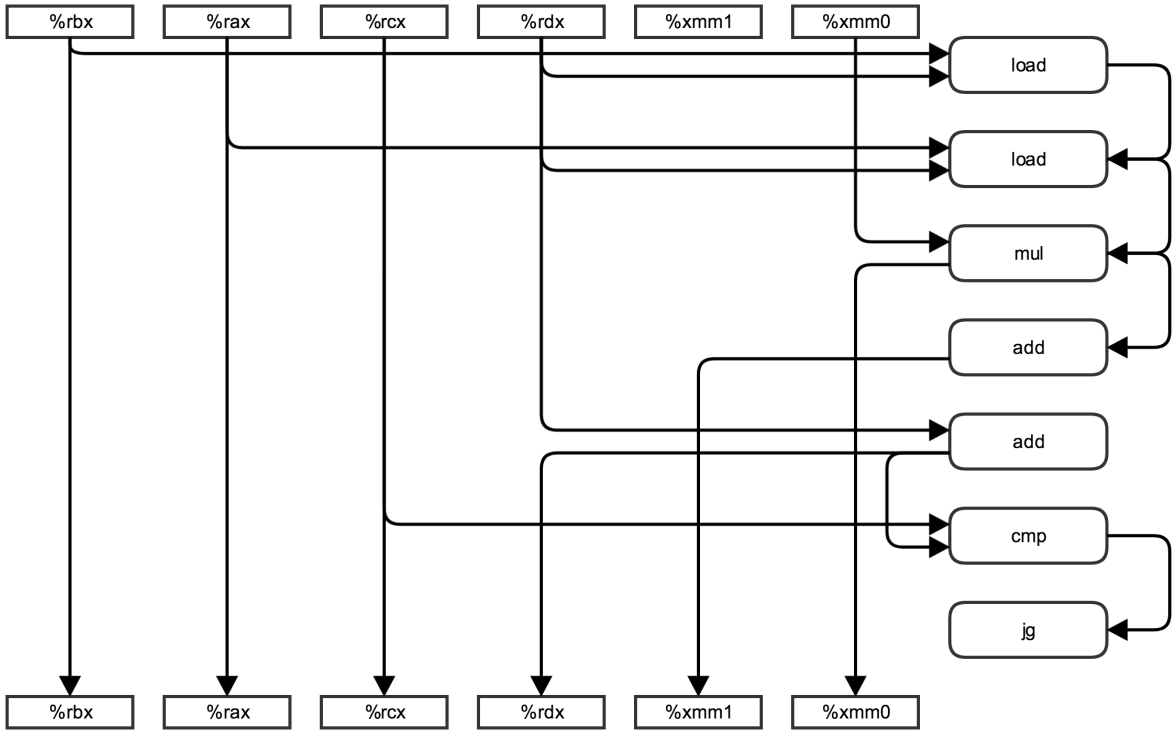
CIS 314
Assignment 7

(Question #1)

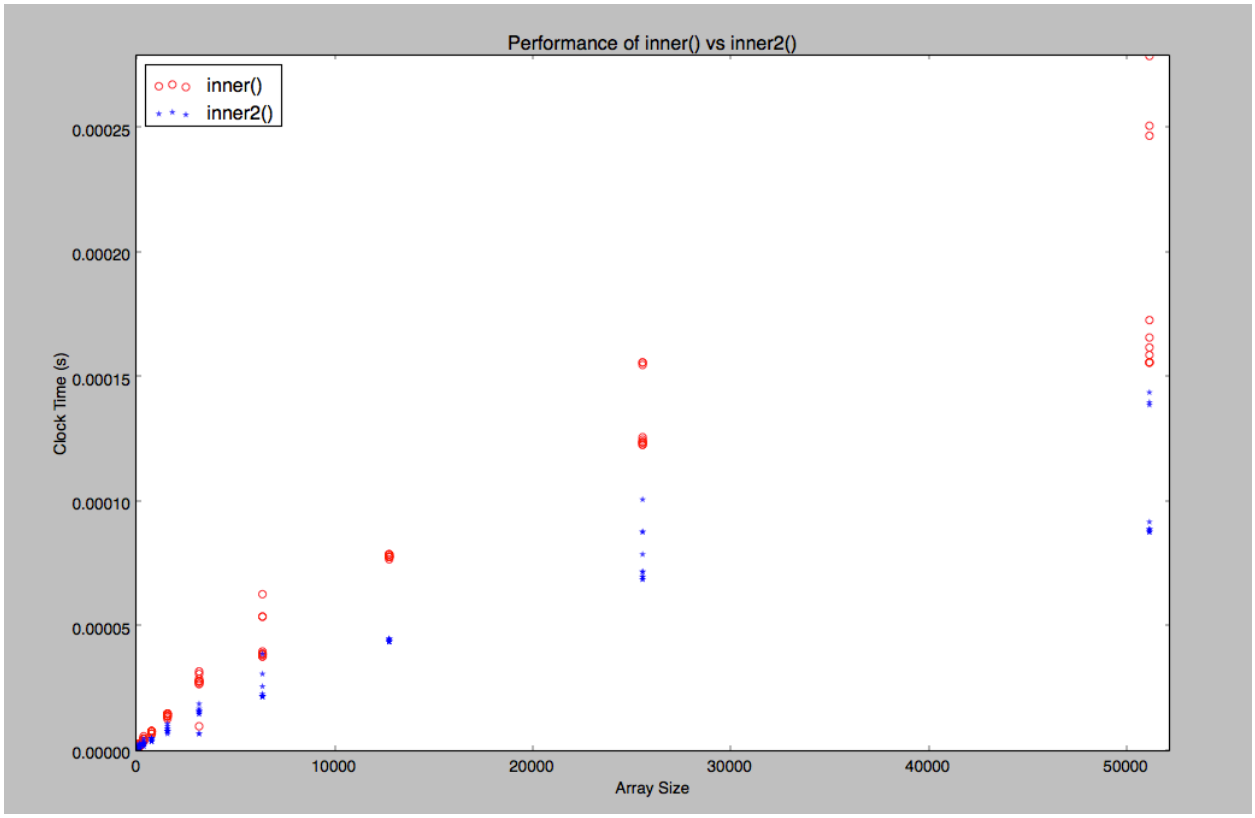


(Question #2) The adds instruction cannot be pipelined because of the data dependency for register %xmm0. The cmpq instruction cannot be pipelined because it needs to read register %rdx. Thus the lower latency bound is 5 + 3 + 1 = 9, because the latency will be combination of the CPE's from the multiply, the addition and the comparison.

(Question #3) See source file 7-1.c

(Question #4)

The function inner2() seems to achieve more efficient results, at least for larger array sizes. This is because of the loop unrolling and parallelization optimizations. The average speedup was about 1.7x. See my scatterplot below:


Performance of inner() vs inner2()
inner()
inner2()
Clock Time (s)
0.00025
0.00020
0.00015
0.00010
0.00005
0.00000
0
10000
20000
30000
40000
50000
Array Size